

INA12x 低功耗精密仪表放大器

此器件的新版本现已上市: [INA828](#)

1 特性

- 此器件的新版本现已上市: [INA828](#)
- 低失调电压: 50 μ V (最大值)
- 低漂移: 0.5 μ V/ $^{\circ}$ C (最大值)
- 低输入偏置电流: 5nA (最大值)
- 高 CMR: 120dB (最小值)
- 输入保护电压可达 ± 40 V
- 宽电源电压范围: ± 2.25 V 至 ± 18 V
- 低静态电流: 700 μ A
- 封装: 8 引脚塑料 DIP, SO-8

2 应用

- 桥式放大器
- 热电偶放大器
- RTD 传感器放大器
- 医疗器械
- 数据采集

3 说明

INA128 和 INA129 均为具备出色精度的低功耗通用仪表放大器。该器件采用多功能三级运算放大器设计, 尺寸小巧, 适用于各种应用。即使在高增益 (200 kHz at $G = 100$) 情况下, 电流反馈输入电路也可提供宽带宽。

可通过单个外部电阻器在 1 到 10,000 范围内设置任意增益。INA128 提供行业标准增益方程; INA129 增益方程与 AD620 兼容。

INA12x 采用 8 引脚塑料 DIP 和 SO-8 表面贴装式封装, 专门适用于 -40° C 至 $+85^{\circ}$ C 温度范围。INA128 也适用于双路配置 INA2128。

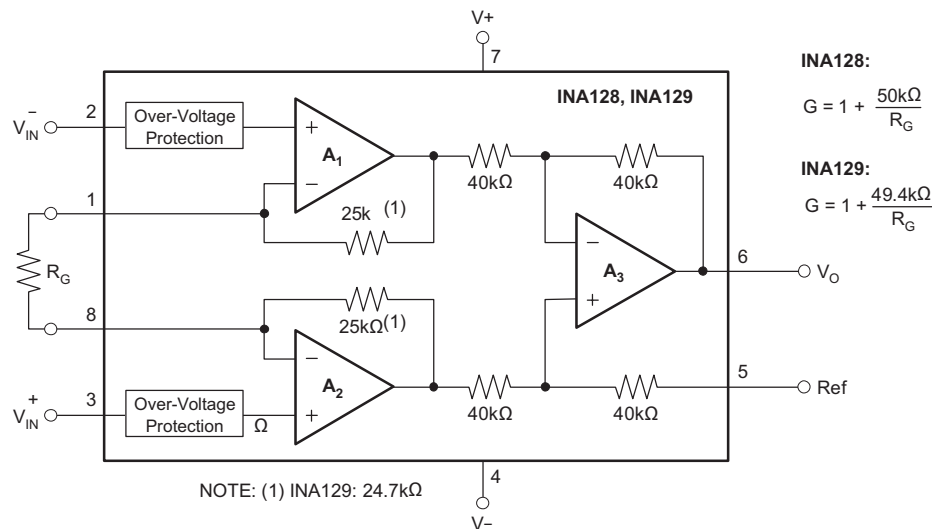
升级后的 [INA828](#) 在相同的静态电流下可提供低输入偏置电流 (最大值 0.6nA) 并且具有更低的噪声 (7nV/ $\sqrt{\text{Hz}}$)。请参阅[器件比较](#), 了解德州仪器 (TI) 提供的精密仪表放大器精选产品。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
INA128、 INA129	SOIC (8)	3.91mm $\times$ 4.90mm
	PDIP (8)	6.35mm $\times$ 9.81mm

(1) 要了解所有可用封装, 请参见数据表末尾的封装选项附录。

简化原理图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (January 2018) to Revision E	Page
• 已添加 添加了有关全新升级的 INA828 的信息	1
• Added <i>Device Comparison Table</i>	3
Changes from Revision C (October 2015) to Revision D	Page
• 已添加 向 TI 参考设计添加了顶部导航图标	1
• Changed "±0.5±0/G" to "±0.5±20/G" in MAX column of Offset voltage RTI vs temperature row of <i>Electrical Characteristics</i>	5
Changes from Revision B (February 2005) to Revision C	Page
• 添加了 <i>ESD</i> 额定值表、特性说明部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分.....	1

5 Device Comparison Table

DEVICE	DESCRIPTION	GAIN EQUATION	RG PINS AT PIN
INA828	50-μV Offset, 0.5 μV/°C V_{OS} drift, 7-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier	$G = 1 + 50 \text{ k}\Omega / R_G$	1, 8
INA819	35-μV Offset, 0.4 μV/°C V_{OS} drift, 8-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier	$G = 1 + 50 \text{ k}\Omega / R_G$	2, 3
INA821	35-μV Offset, 0.4 μV/°C V_{OS} drift, 7-nV/√Hz Noise, High-Bandwidth, Precision Instrumentation Amplifier	$G = 1 + 49.4 \text{ k}\Omega / R_G$	2, 3
INA828	50-μV Offset, 0.5 μV/°C V_{OS} drift, 7-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier	$G = 1 + 50 \text{ k}\Omega / R_G$	1, 8
INA333	25-μV V_{OS} , 0.1 μV/°C V_{OS} drift, 1.8-V to 5-V, RRO, 50-μA I_Q , chopper-stabilized INA	$G = 1 + 100 \text{ k}\Omega / R_G$	1, 8
PGA280	20-mV to ±10-V programmable gain IA with 3-V or 5-V differential output; analog supply up to ±18 V	digital programmable	N/A
INA159	$G = 0.2 \text{ V}$ differential amplifier for ±10-V to 3-V and 5-V conversion	$G = 0.2 \text{ V/V}$	N/A
PGA112	Precision programmable gain op amp with SPI	digital programmable	N/A

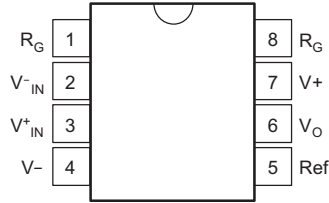
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6 Pin Configuration and Functions

**D and P Packages
8-Pin SOIC and PDIP
Top View**

**Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
REF	5	I	Reference input. This pin must be driven by low impedance or connected to ground.
R _G	1,8	—	Gain setting pin. For gains greater than 1, place a gain resistor between pin 1 and pin 8.
V ₋	4	—	Negative supply
V ₊	7	—	Positive supply
V _{IN-}	2	I	Negative input
V _{IN+}	3	I	Positive input
V _O	6	I	Output

7 Specifications**7.1 Absolute Maximum Ratings**over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

	MIN	MAX	UNIT
Supply voltage		±18	V
Analog input voltage		±40	V
Output short circuit (to ground)		continuous	
Operating temperature	-40	125	°C
Junction temperature		150	°C
Lead temperature (soldering, 10 seconds)		300	°C
Storage temperature, T _{stg}	-55	125	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±50	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V power supply	±2.25	±15	±18	V
Input common-mode voltage range for $V_O = 0$	$V - 2\text{ V}$		$V + -2\text{ V}$	
T_A operating temperature INA128-HT	-55		175	°C
T_A operating temperature INA129-HT	-55		210	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		INA12x		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110	46.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57	34.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54	23.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	11	11.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	53	23.2	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

7.5 Electrical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
Offset voltage, RTI	Initial	T _A = 25°C	INA128P, U INA129P, U	±10±100/G	±50±500/G		μV
			INA128PA, UA INA129PA, UA	±25±100/G	±125±1000/G		
	vs temperature	T _A = T _{MIN} to T _{MAX}	INA128P, U INA129P, U	±0.2±2/G	±0.5±20/G		μV/°C
			INA128PA, UA INA129PA, UA	±0.2±5/G	±1±20/G		
	vs power supply	V _S = ±2.25 V to ±18 V	INA128P, U INA129P, U	±0.2±20/G	±1±100/G		μV/V
			INA128PA, UA INA129PA, UA		±2±200/G		
	Long-term stability				±0.1±3/g		μV/mo
Impedance	Differential			10 ¹⁰ 2			Ω pF
	Common mode			10 ¹¹ 9			
Common-mode voltage range ⁽¹⁾		V _O = 0 V		(V+) - 2	(V+) - 1.4		V
				(V...) + 2	(V-) + 1.7		
Safe input voltage					±40		V

(1) Input common-mode range varies with output voltage; see [Typical Characteristics](#).

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Electrical Characteristics (continued)at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Common-mode rejection		$V_{CM} = \pm 13\text{ V}$, $\Delta R_S = 1\text{ k}\Omega$	G = 1	INA128P, U INA129P, U	80	86	dB
				INA128PA, UA INA129PA, UA	73		
			G = 10	INA128P, U INA129P, U	100	106	
				INA128PA, UA INA129PA, UA	93		
			G = 100	INA128P, U INA129P, U	120	125	
				INA128PA, UA INA129PA, UA	110		
			G = 1000	INA128P, U INA129P, U	120	130	
				INA128PA, UA INA129PA, UA	110		
Bias current		INA128P, U INA129P, U			± 2	± 5	nA
		INA128PA, UA INA129PA, UA				± 10	
Bias current vs temperature					± 30		pA/°C
Offset current		INA128P, U INA129P, U			± 1	± 5	nA
		INA128PA, UA INA129PA, UA				± 10	
Offset current vs temperature					± 30		pA/°C
Noise voltage, RTI	f = 10 Hz	G = 1000, $R_S = 0\Omega$			10	nV/ $\sqrt{\text{Hz}}$	
	f = 100 Hz				8		
	f = 1 kHz				8		
	$f_B = 0.1\text{ Hz to }10\text{ Hz}$				0.2	μV_{PP}	
Noise current	f = 10 Hz				0.9	pA/ $\sqrt{\text{Hz}}$	
	f = 1 kHz				0.3		
	$F_B = 0.1\text{ Hz to }10\text{ Hz}$				30	pA _{PP}	
GAIN ⁽²⁾							
Gain equation	INA128			$1 + (50\text{ k}\Omega/R_G)$		V/V	
	INA129			$1 + (49.4\text{ k}\Omega/R_G)$			
Range of gain				1	10000	V/V	
Gain error		G = 1	INA128P, U INA129P, U	$\pm 0.01\%$	$\pm 0.024\%$		
			INA128PA, UA INA129PA, UA		$\pm 0.01\%$		
		G = 10	INA128P, U INA129P, U	$\pm 0.02\%$	$\pm 0.4\%$		
			INA128PA, UA INA129PA, UA		$\pm 0.5\%$		
		G = 100	INA128P, U INA129P, U	$\pm 0.05\%$	$\pm 0.5\%$		
			INA128PA, UA INA129PA, UA		$\pm 0.7\%$		
		G = 1000	INA128P, U INA129P, U	$\pm 0.5\%$	$\pm 1\%$		
			INA128PA, UA INA129PA, UA		$\pm 2\%$		

(2) Nonlinearity measurements in G = 1000 are dominated by noise. Typical non-linearity is $\pm 0.001\%$.

Electrical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Gain vs temperature ⁽³⁾		G = 1			±1	±10	ppm/°C
		50-kΩ (or 49.4-kΩ) Resistance ⁽³⁾⁽⁴⁾			±25	±100	
Nonlinearity		V _O = ±13.6 V, G = 1	INA128P, U INA129P, U		±0.0001	±0.001	% of FSR
			INA128PA, UA INA129PA, UA			±0.002	
		G = 10	INA128P, U INA129P, U		±0.0003	±0.002	
			INA128PA, UA INA129PA, UA			±0.004	
		G = 100	INA128P, U INA129P, U		±0.0005	±0.002	
			INA128PA, UA INA129PA, UA			±0.004	
		G = 1000				±0.001	
OUTPUT ⁽²⁾							
Voltage	Positive	R _L = 10 kΩ		(V+) – 1.4	(V+) – 0.9		V
	Negative	R _L = 10 kΩ		(V–) + 1.4	(V–) + 0.8		
Load capacitance stability					1000		pF
Short-circuit current					6/–15		mA
FREQUENCY RESPONSE							
Bandwidth, –3 dB		G = 1			1.3		MHz
		G = 10			700		kHz
		G = 100			200		
		G = 1000			20		
Slew rate		V _O = ±10 V, G = 10			4		V/μs
Settling time, 0.01%		G = 1			7		μs
		G = 10			7		
		G = 100			9		
		G = 1000			80		
Overload recovery		50% overdrive			4		μs
POWER SUPPLY							
Voltage range				±2.25	±15	±18	V
Current, total		V _{IN} = 0 V			±700	±750	μA
TEMPERATURE RANGE							
Specification				–40		85	°C
Operating				–40		125	°C

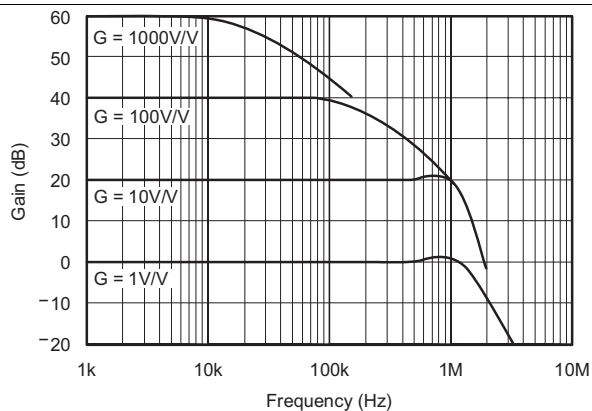
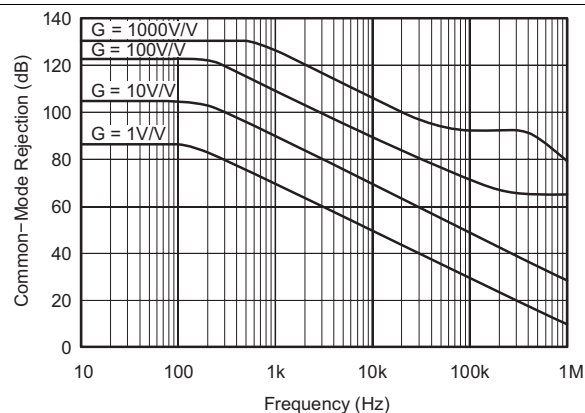
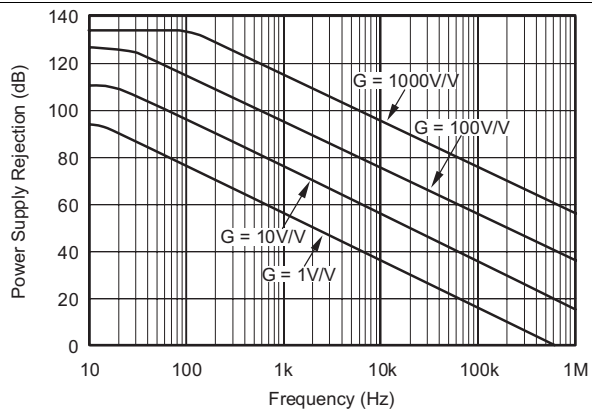
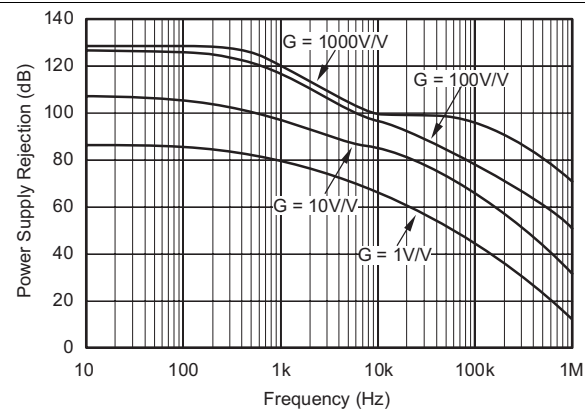
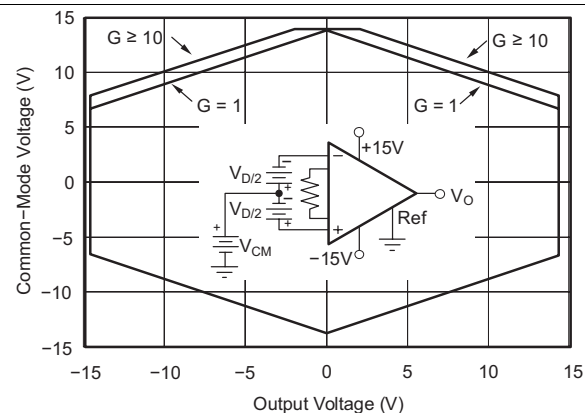
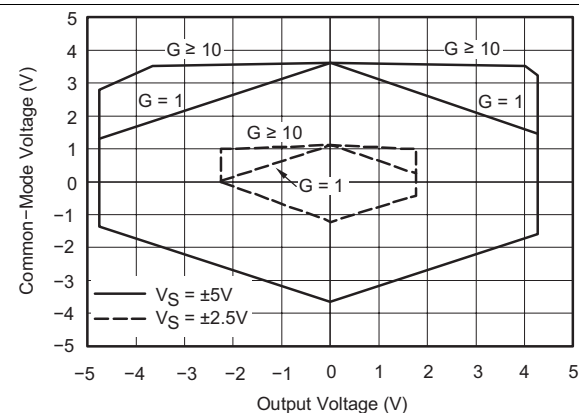
(3) Specified by wafer test.

(4) Temperature coefficient of the 50 k Ω (or 49.4 k Ω) term in the gain equation.

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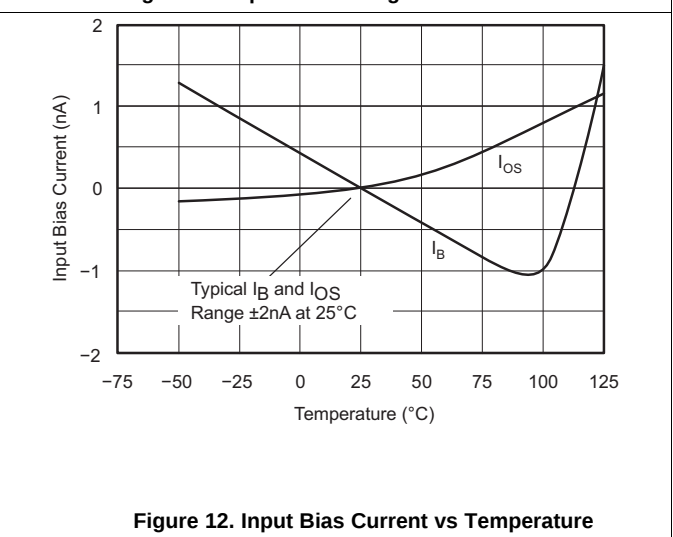
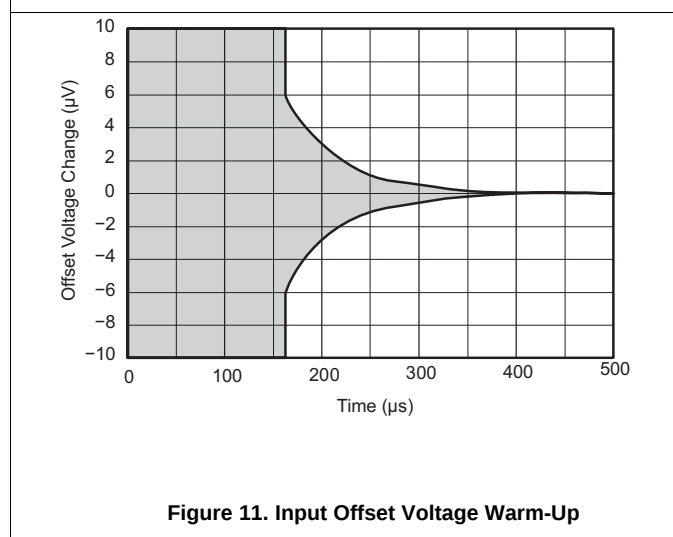
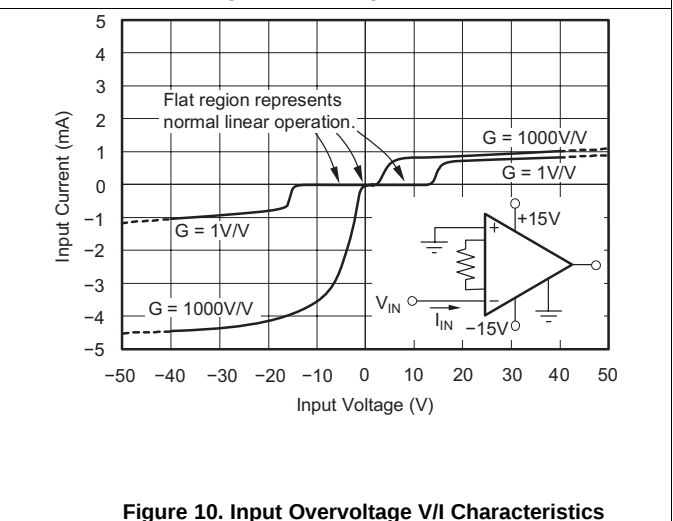
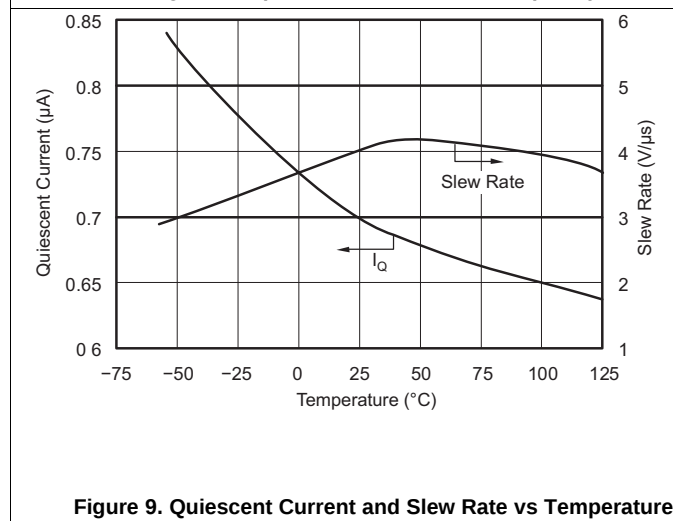
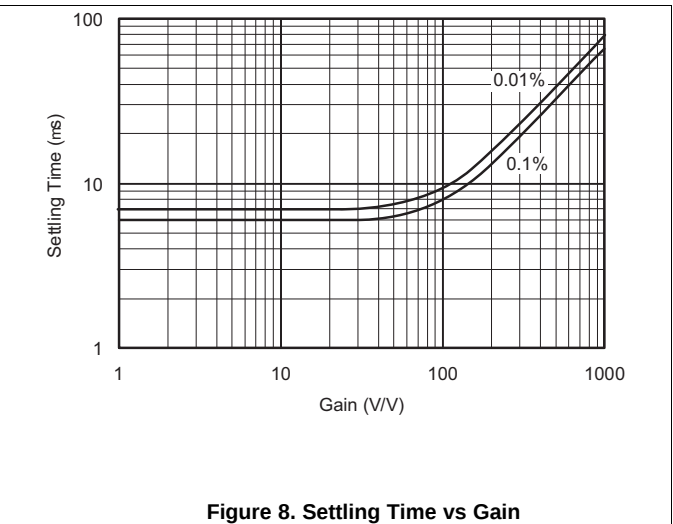
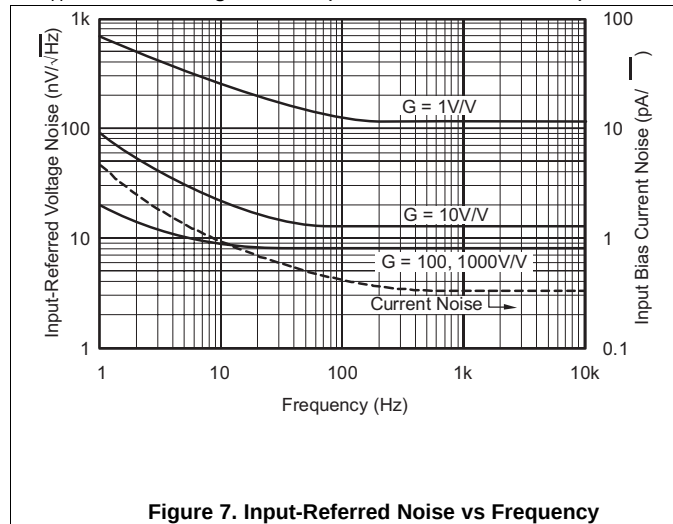
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7.6 Typical Characteristicsat $T_A = 25^\circ\text{C}$ and $V_S = \pm 15\text{ V}$ (unless otherwise noted)**Figure 1. Gain vs Frequency****Figure 2. Common-Mode Rejection vs Frequency****Figure 3. Positive Power Supply Rejection vs Frequency****Figure 4. Negative Power Supply Rejection vs Frequency****Figure 5. Input Common-Mode Range vs Output Voltage,
 $V_S = \pm 15\text{ V}$** **Figure 6. Input Common-Mode Range vs Output Voltage,
 $V_S = \pm 5\text{ V}, \pm 2.5\text{ V}$**

Typical Characteristics (continued)

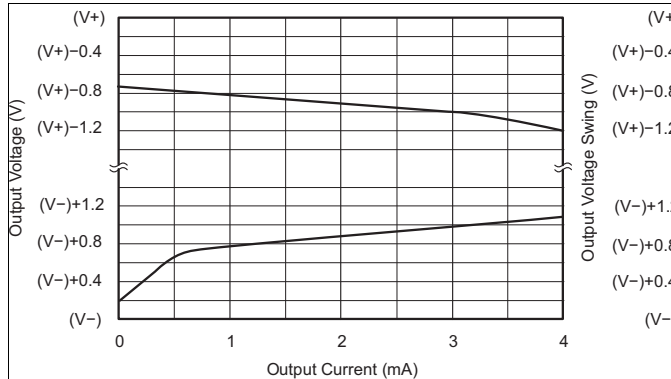
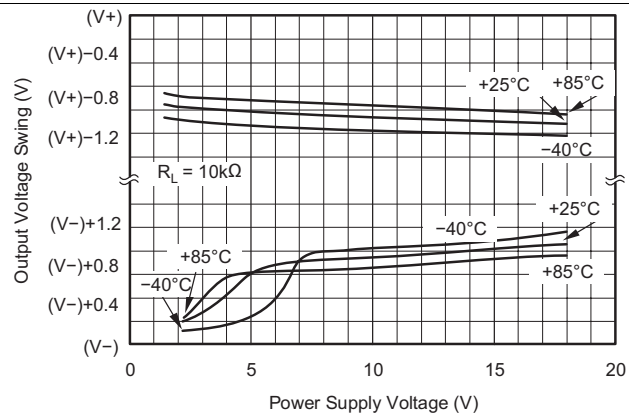
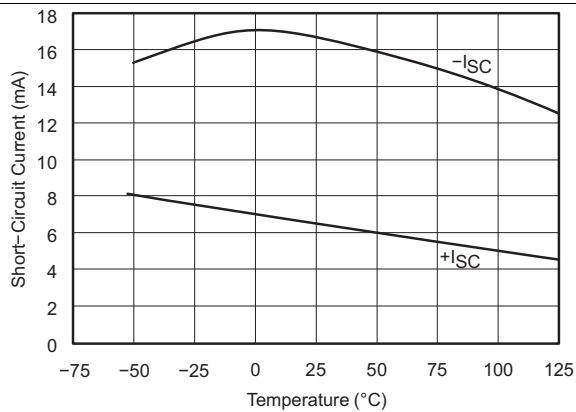
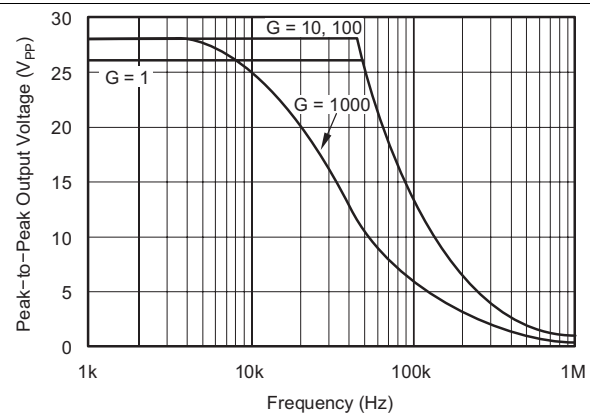
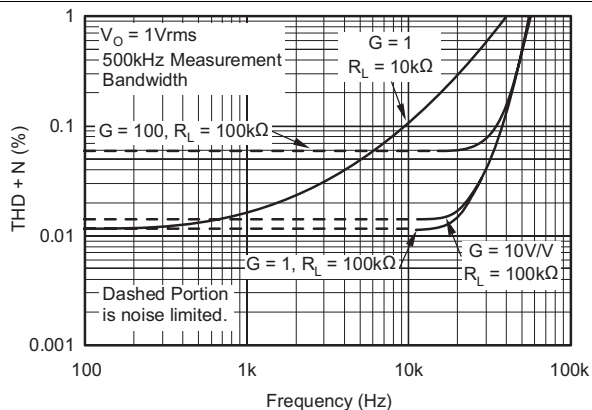
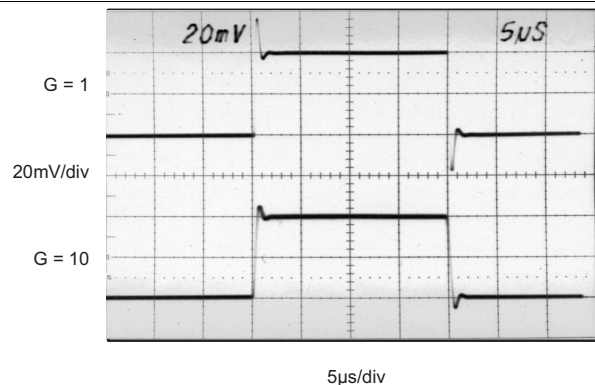
at $T_A = 25^\circ\text{C}$ and $V_S = \pm 15\text{ V}$ (unless otherwise noted)



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Typical Characteristics (continued)at $T_A = 25^\circ\text{C}$ and $V_S = \pm 15\text{ V}$ (unless otherwise noted)**Figure 13. Output Voltage Swing vs Output Current****Figure 14. Output Voltage Swing vs Power Supply Voltage****Figure 15. Short Circuit Output Current vs Temperature****Figure 16. Maximum Output Voltage vs Frequency****Figure 17. Total Harmonic Distortion + Noise vs Frequency****Figure 18. Small Signal (G = 1, 10)**

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$ and $V_S = \pm 15\text{ V}$ (unless otherwise noted)

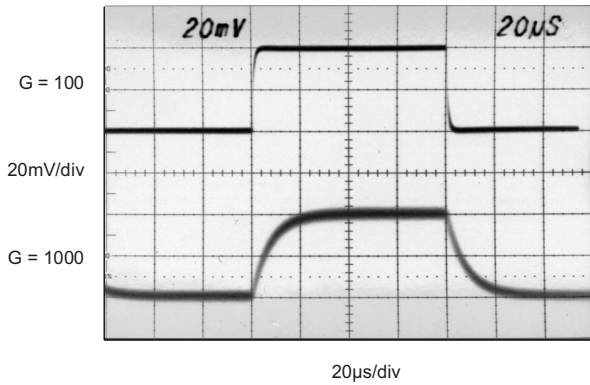


Figure 19. Small Signal ($G = 100, 1000$)

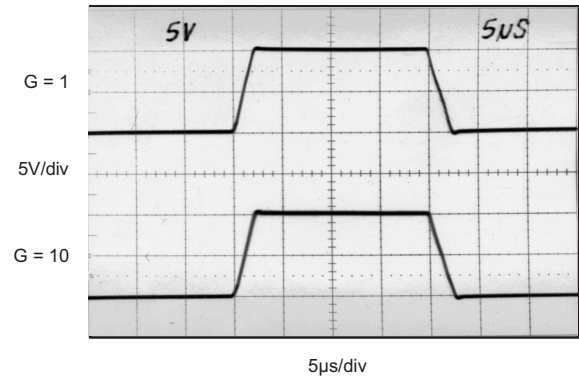


Figure 20. Large Signal ($G = 1, 10$)

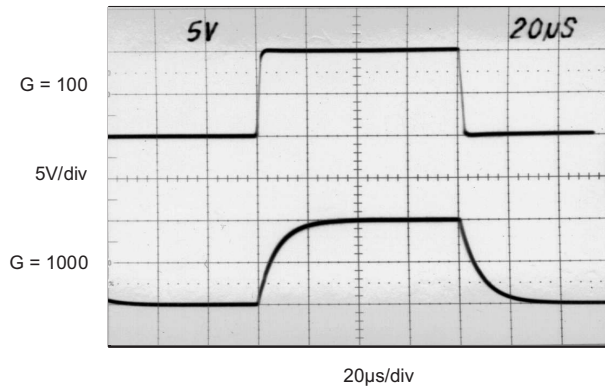


Figure 21. Large Signal ($G = 100, 1000$)

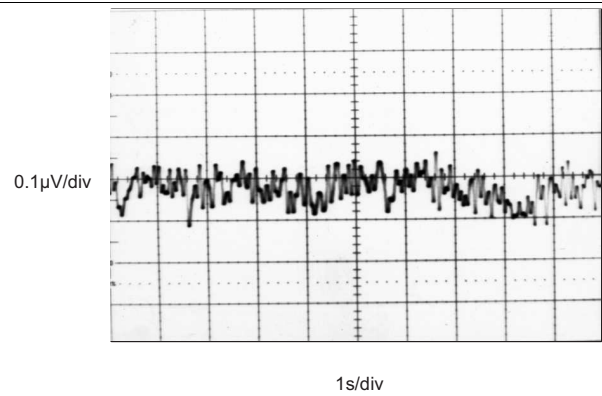


Figure 22. Voltage Noise 0.1 to 10-Hz Input-Referred, $G \geq 100$

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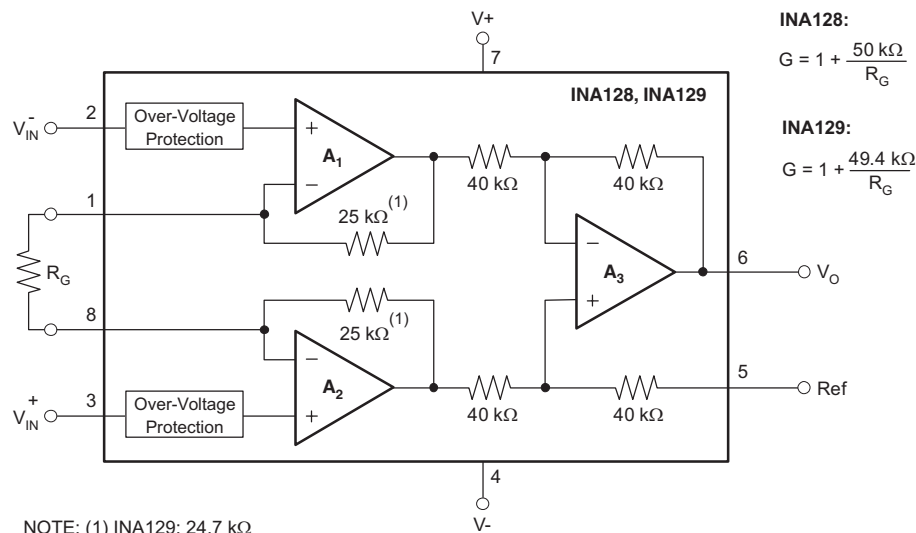
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8 Detailed Description

8.1 Overview

The INA12x instrumentation amplifier is a type of differential amplifier that has been outfitted with input protection circuit and input buffer amplifiers, which eliminate the need for input impedance matching and make the amplifier particularly suitable for use in measurement and test equipment. Additional characteristics of the INA128 include a very low DC offset, low drift, low noise, very high open-loop gain, very high common-mode rejection ratio, and very high input impedances. The INA12x is used where great accuracy and stability of the circuit both short and long term are required.

8.2 Functional Block Diagram



8.3 Feature Description

The INA12x devices are low power, general-purpose instrumentation amplifiers offering excellent accuracy. The versatile three-operational-amplifier design and small size make the amplifiers ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth, even at high gain. A single external resistor sets any gain from 1 to 10,000. The INA128 is laser trimmed for very low offset voltage (25 μV typical) and high common-mode rejection (93 dB at $G \geq 100$). These devices operate with power supplies as low as ±2.25 V, and quiescent current of 2 mA, typically. The internal input protection can withstand up to ±40 V without damage.

8.4 Device Functional Modes

8.4.1 Noise Performance

The INA12x provides very low noise in most applications. Low-frequency noise is approximately $0.2 \mu\text{V}_{\text{PP}}$ measured from 0.1 to 10 Hz ($G \geq 100$). This provides dramatically improved noise when compared to state-of-the-art chopper-stabilized amplifiers.

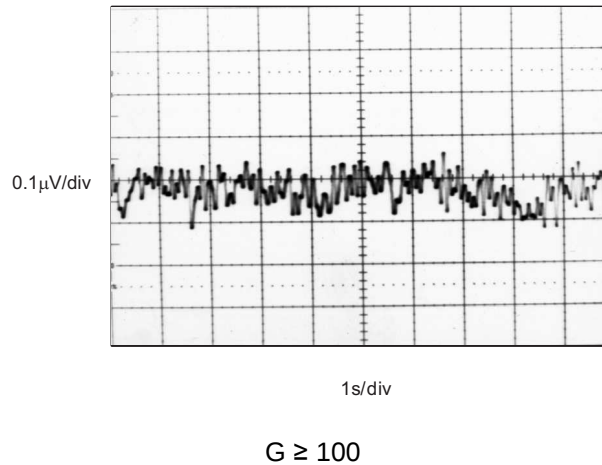


Figure 23. 0.1-Hz to 10-Hz Input-Referred Voltage Noise

8.4.2 Input Common-Mode Range

The linear input voltage range of the input circuitry of the INA12x is from approximately 1.4 V below the positive supply voltage to 1.7 V above the negative supply. As a differential input voltage causes the output voltage increase, however, the linear input range is limited by the output voltage swing of amplifiers A_1 and A_2 . Thus the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage (see performance curve [Figure 6](#)).

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of A_3 will be near 0 V even though both inputs are overloaded.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The INA12x measures small differential voltage with high common-mode voltage developed between the noninverting and inverting input. The high-input voltage protection circuit in conjunction with high input impedance make the INA12x suitable for a wide range of applications. The ability to set the reference pin to adjust the functionality of the output signal offers additional flexibility that is practical for multiple configurations.

9.2 Typical Application

Figure 24 shows the basic connections required for operation of the INA12x. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown. The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 8 Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR ($G = 1$).

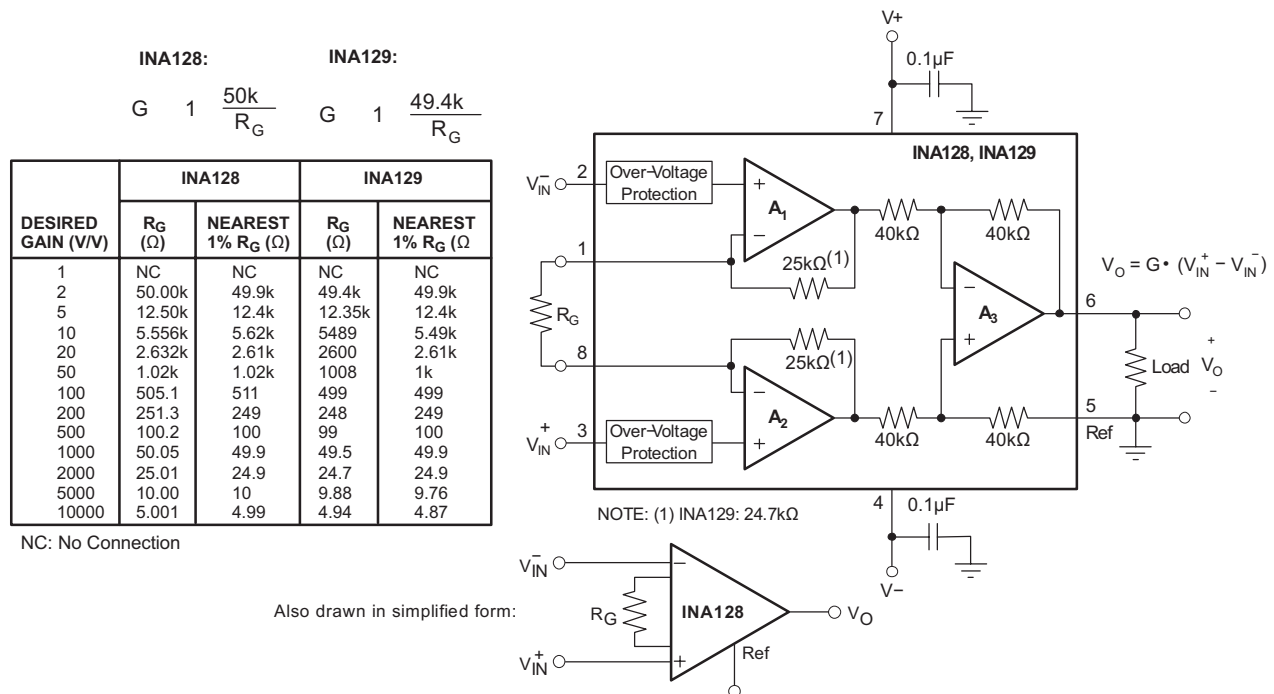


Figure 24. Basic Connections

Typical Application (continued)

9.2.1 Design Requirements

The device can be configured to monitor the input differential voltage when the gain of the input signal is set by the external resistor R_G . The output signal references to the Ref pin. The most common application is where the output is referenced to ground when no input signal is present by connecting the Ref pin to ground, as Figure 24 shows. When the input signal increases, the output voltage at the OUT pin increases, too.

9.2.2 Detailed Design Procedure

9.2.2.1 Setting the Gain

Gain is set by connecting a single external resistor, R_G , connected between pins 1 and 8:

$$\text{INA128: } g = 1 + 50 \text{ k}\Omega / R_G \quad (1)$$

Commonly used gains and resistor values are shown in Figure 24.

The 50-k Ω term in Equation 1 comes from the sum of the two internal feedback resistors of A_1 and A_2 . These on-chip metal film resistors are laser-trimmed to accurate absolute values. The accuracy and temperature coefficient of these internal resistors are included in the gain accuracy and drift specifications of the INA128.

The stability and temperature drift of the external gain setting resistor, R_G , also affects gain. The contribution of R_G to gain accuracy and drift can be directly inferred from Equation 1. Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance, which contributes additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

9.2.2.2 Dynamic Performance

The typical performance curve Figure 1 shows that, despite its low quiescent current, the INA12x achieves wide bandwidth even at high gain. This is due to the current-feedback topology of the input stage circuitry. Settling time also remains excellent at high gain.

9.2.2.3 Offset Trimming

The INA12x is laser-trimmed for low-offset voltage and offset voltage drift. Most applications require no external offset adjustment. Figure 25 shows an optional circuit for trimming the output offset voltage. The voltage applied to the Ref terminal is summed with the output. The op amp buffer provides low impedance at the Ref terminal to preserve good common-mode rejection.

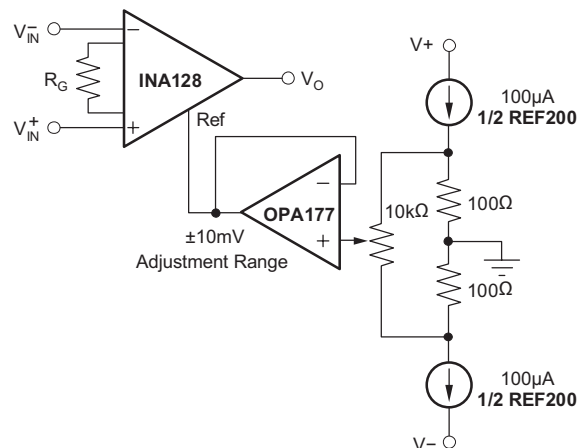


Figure 25. Optional Trimming of Output Offset Voltage

9.2.2.4 Input Bias Current Return Path

The input impedance of the INA12x is extremely high: approximately $10^{10} \Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is approximately $\pm 2 \text{ nA}$. High input impedance means that this input bias current changes very little with varying input voltage.

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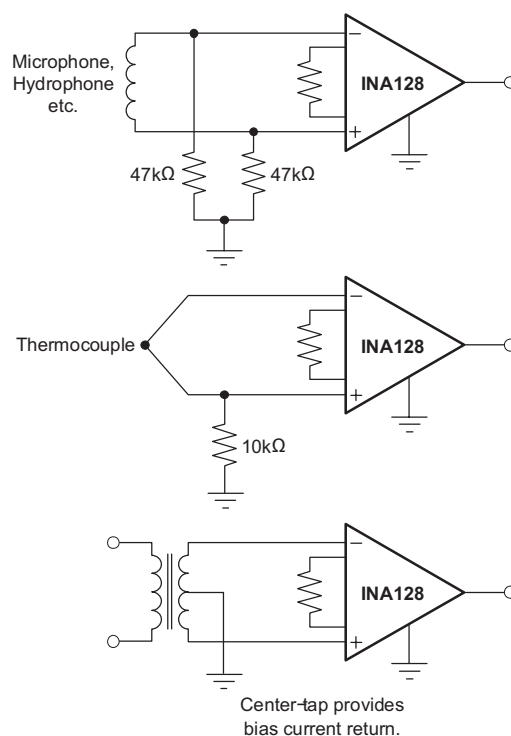
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Typical Application (continued)

Input circuitry must provide a path for this input bias current for proper operation. Figure 26 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the common-mode range, and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 26). With higher source impedance, using two equal resistors provides a balanced input, with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

**Figure 26. Providing an Input Common-Mode Current Path**

Typical Application (continued)

9.2.3 Application Curves

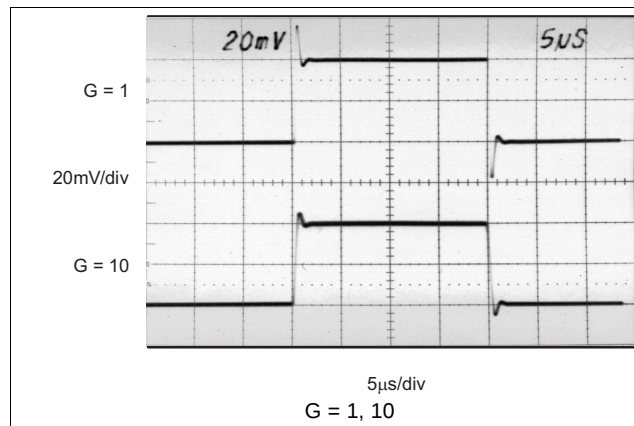


Figure 27. Small Signal

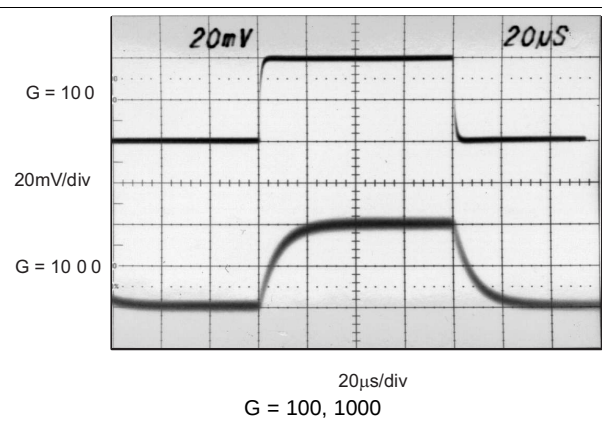


Figure 28. Small Signal

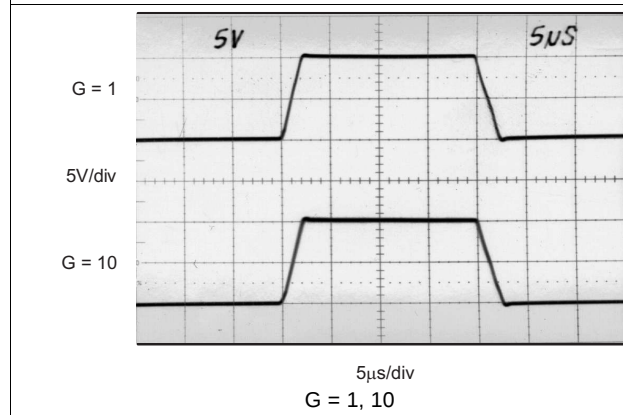


Figure 29. Large Signal

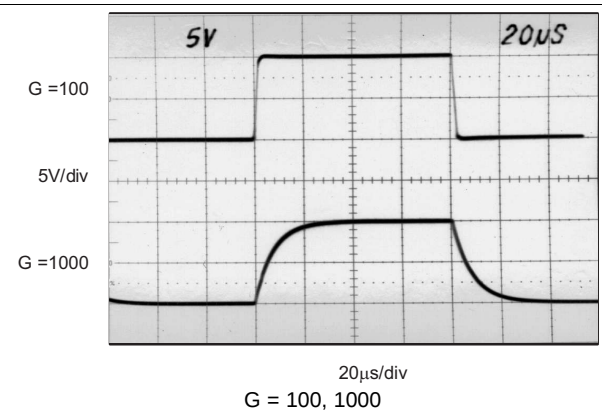


Figure 30. Large Signal

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10 Power Supply Recommendations

The minimum power supply voltage for INA12x is ± 2.25 V and the maximum power supply voltage is ± 18 V. This minimum and maximum range covers a wide range of power supplies; but for optimum performance, ± 15 V is recommended. TI recommends adding a bypass capacitor at the input to compensate for the layout and power supply source impedance.

10.1 Low Voltage Operation

The INA12x can be operated on power supplies as low as ± 2.25 V. Performance remains excellent with power supplies ranging from ± 2.25 V to ± 18 V. Most parameters vary only slightly throughout this supply voltage range—see [Typical Characteristics](#).

Operation at very low supply voltage requires careful attention to assure that the input voltages remain within their linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power supply voltage. [Figure 6](#) shows the range of linear operation for ± 15 -V, ± 5 -V, and ± 2.5 -V supplies.

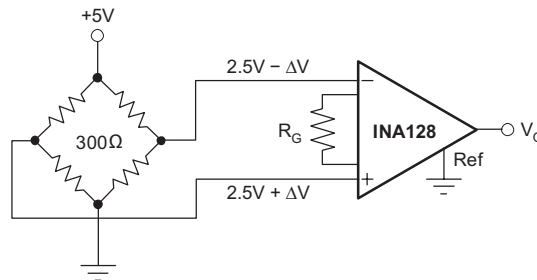


Figure 31. Bridge Amplifier

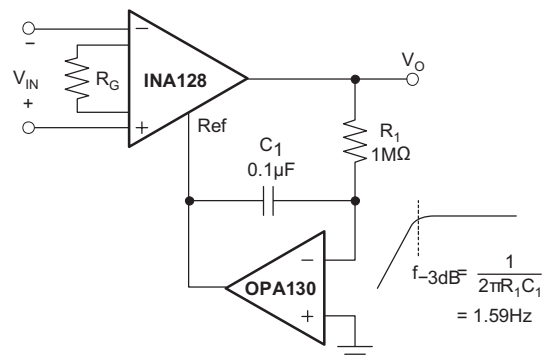


Figure 32. AC-Coupled Instrumentation Amplifier

Low Voltage Operation (continued)

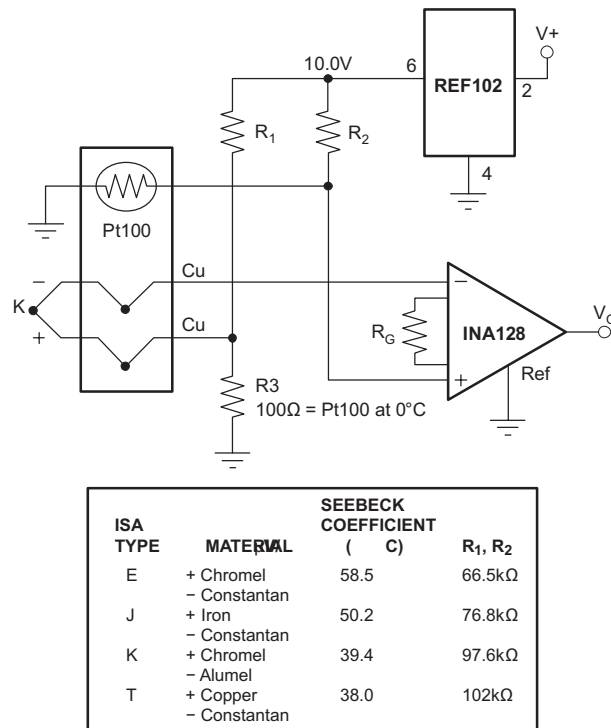


Figure 33. Thermocouple Amplifier With RTD Cold-Junction Compensation

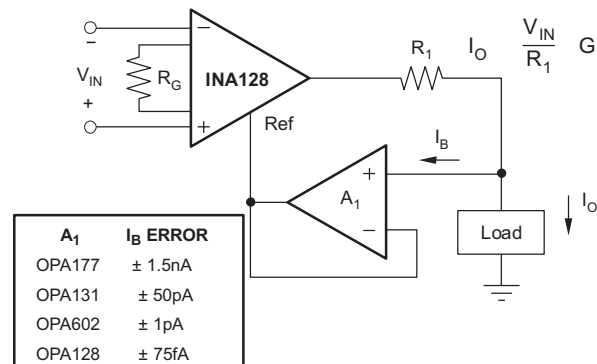
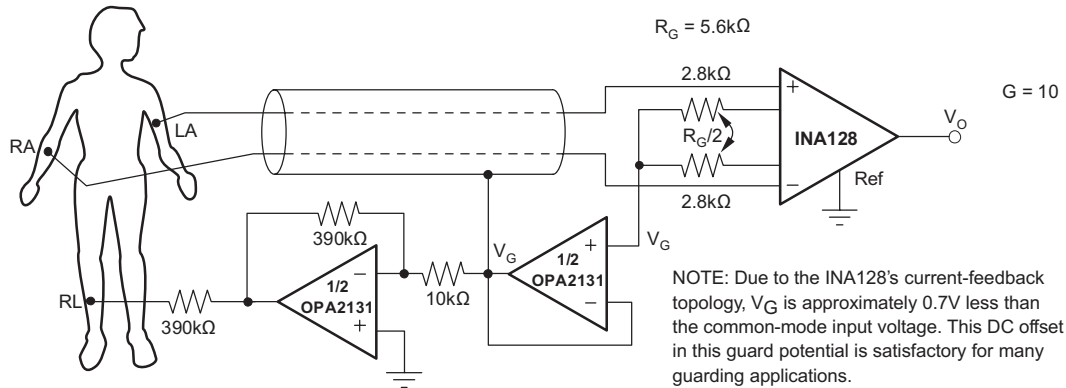


Figure 34. Differential Voltage to Current Converter

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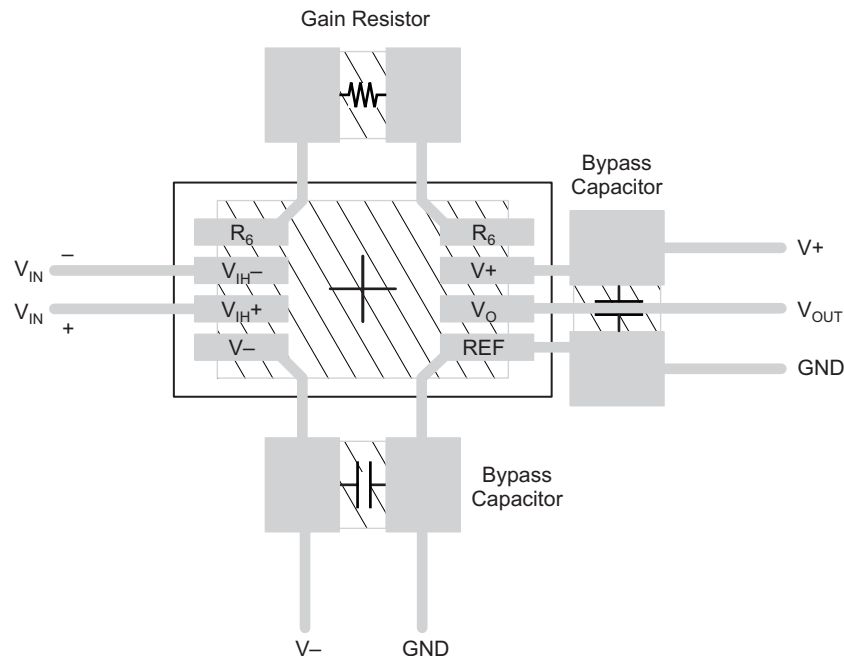
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Low Voltage Operation (continued)**Figure 35. ECG Amplifier With Right-Leg Drive****11 Layout****11.1 Layout Guidelines**

Place the power-supply bypass capacitor as closely as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1 μF to 1 μF . If necessary, additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies. These decoupling capacitors must be placed between the power supply and INA12x devices.

The gain resistor must be placed close to pin 1 and pin 8. This placement limits the layout loop and minimizes any noise coupling into the part.

11.2 Layout Example**Figure 36. Recommended Layout**

12 器件和文档支持

12.1 相关链接

表 1 列出了快速访问链接。类别包括技术文档、支持与社区资源、工具与软件，以及申请样片或购买产品的快速链接。

表 1. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持和社区
INA128	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
INA129	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.2 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](#) 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商标

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All other trademarks are the property of their respective owners.

12.5 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 术语表

SLYZ022 — *TI* 术语表。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA128P	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		INA128P	Samples
INA128PA	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		INA128P A	Samples
INA128PG4	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		INA128P	Samples
INA128U	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 128U	Samples
INA128U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 128U	Samples
INA128U/2K5G4	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 128U	Samples
INA128UA	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 125	INA 128U A	Samples
INA128UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 125	INA 128U A	Samples
INA128UA/2K5E4	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 125	INA 128U A	Samples
INA128UA/2K5G4	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 125	INA 128U A	Samples
INA128UAE4	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 125	INA 128U A	Samples
INA128UAG4	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 125	INA 128U A	Samples
INA128UG4	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 128U	Samples
INA129P	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		INA129P	Samples
INA129PA	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		INA129P	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										A	
INA129PG4	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		INA129P	Samples
INA129U	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 129U	Samples
INA129U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 129U	Samples
INA129UA	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 125	INA 129U A	Samples
INA129UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 125	INA 129U A	Samples
INA129UA/2K5G4	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 125	INA 129U A	Samples
INA129UAE4	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 125	INA 129U A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF INA128, INA129 :

- Enhanced Product : [INA129-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

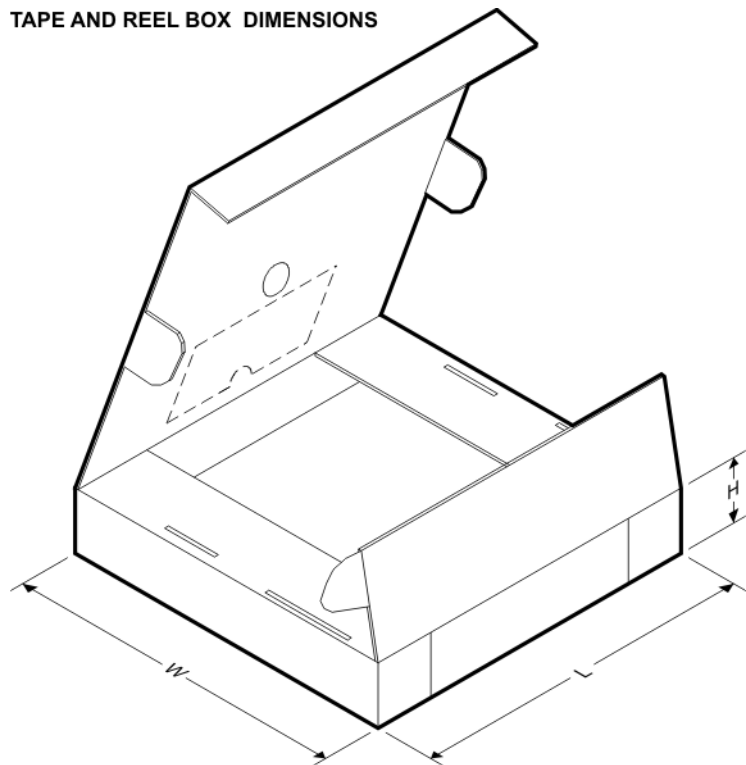
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA128U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA128UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA129U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA129UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

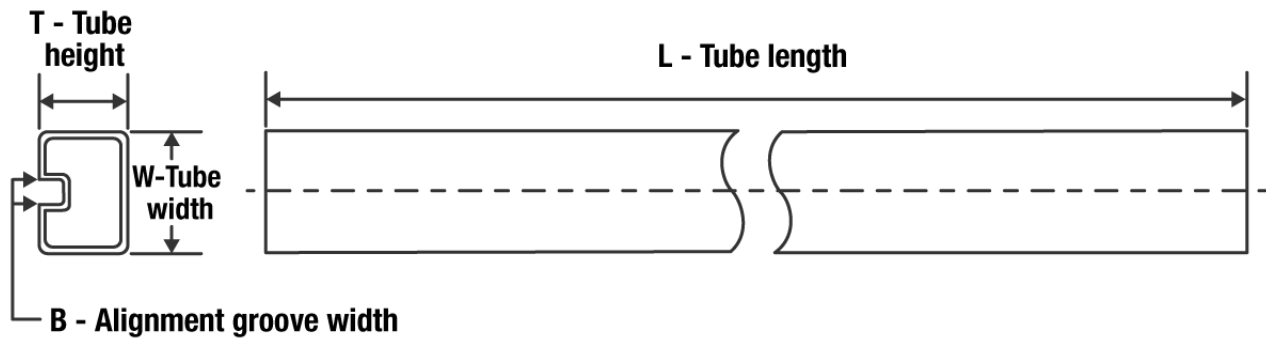
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA128U/2K5	SOIC	D	8	2500	853.0	449.0	35.0
INA128UA/2K5	SOIC	D	8	2500	853.0	449.0	35.0
INA129U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
INA129UA/2K5	SOIC	D	8	2500	853.0	449.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
INA128P	P	PDIP	8	50	506	13.97	11230	4.32
INA128PA	P	PDIP	8	50	506	13.97	11230	4.32
INA128PG4	P	PDIP	8	50	506	13.97	11230	4.32
INA128U	D	SOIC	8	75	506.6	8	3940	4.32
INA128UA	D	SOIC	8	75	506.6	8	3940	4.32
INA128UAE4	D	SOIC	8	75	506.6	8	3940	4.32
INA128UAG4	D	SOIC	8	75	506.6	8	3940	4.32
INA128UG4	D	SOIC	8	75	506.6	8	3940	4.32
INA129P	P	PDIP	8	50	506	13.97	11230	4.32
INA129PA	P	PDIP	8	50	506	13.97	11230	4.32
INA129PG4	P	PDIP	8	50	506	13.97	11230	4.32
INA129U	D	SOIC	8	75	506.6	8	3940	4.32
INA129UA	D	SOIC	8	75	506.6	8	3940	4.32
INA129UAE4	D	SOIC	8	75	506.6	8	3940	4.32

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



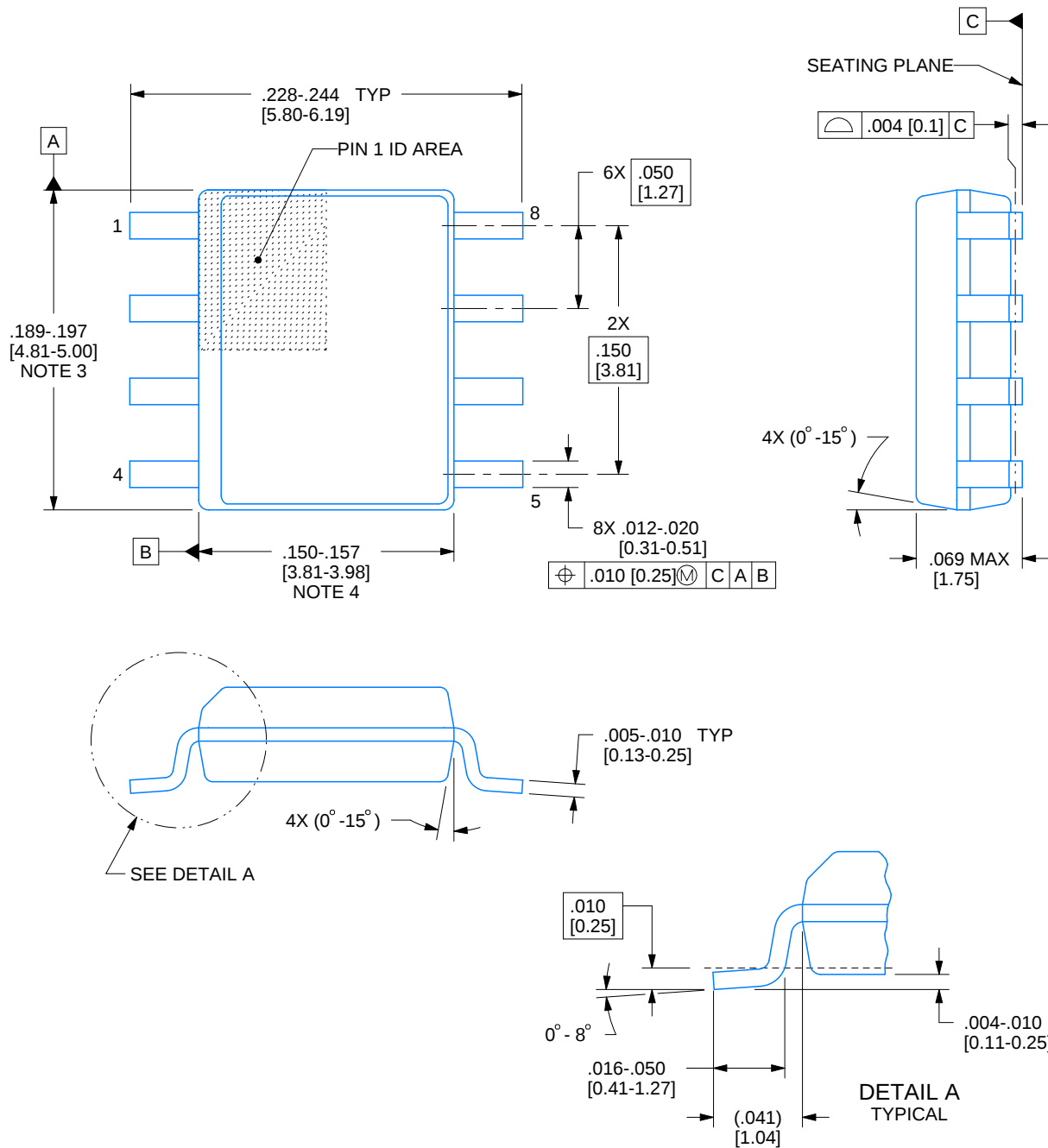
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

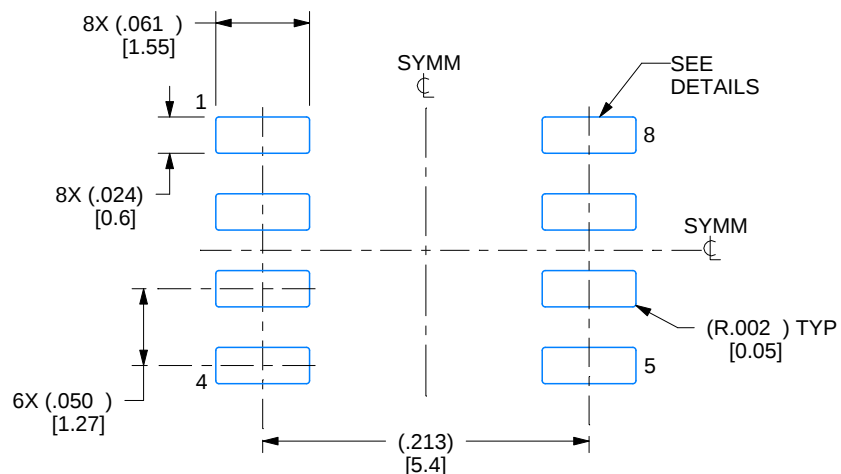
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

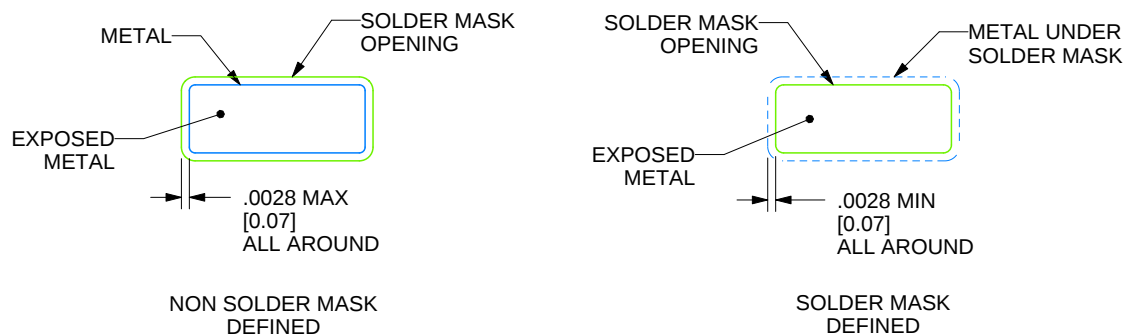
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

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