MSP430AFE253, MSP430AFE252, MSP430AFE251
MSP430AFE233, MSP430AFE232, MSP430AFE231
MSP430AFE223, MSP430AFE222, MSP430AFE221
ZHCS136B – NOVEMBER 2010 – REVISED JUNE 2018

MSP430AFE2x3、MSP430AFE2x2、MSP430AFE2x1 混合信号微控制器

1 器件概述

1.1 特性

- 低电源电压范围：1.8V 至 3.6V
- 超低功耗
  - 激活模式：220µA（在 1MHz 频率和 2.2V 电压条件下）
  - 待机模式：0.5µA
  - 关闭模式（RAM 保持）：0.1µA
- 5 种省电模式
- 可在不到 1µs 的时间内超快速地从待机模式唤醒
- 16 位精简指令集 (RISC) 架构，高达 12MHz 系统时钟
- 基本时钟模块配置
  - 带有两个已校准频率的高达 12MHz 的内部频率
  - 内部超低功耗低频 (LF) 振荡器
  - 高达 16MHz 的高频 (HF) 晶振
  - 谐振器
  - 外部数字时钟源
- 多达三个具有差分 PGA 输入的 24 位 Σ-Δ 模数转换器 (ADC)
- 具有 3 个捕获/比较寄存器的 16 位 Timer_A
- 串行通信接口 (USART)，可用软件来选择异步 UART 或同步 SPI
- 16 位硬件乘法器
- 欠压检测器
- 具有可编程电平检测功能的电源电压监控器和监视器
- 串行板上编程，无需从外部进行电压编程，利用安全熔丝实现可编程代码保护
- 片上仿真模块
- 器件比较 汇总了可用的产品系列成员
- 如需完整的模块说明，请参阅 *《MSP430x2xx 系列用户指南》*

1.2 应用

- 单相电表
- 数字电源监控
- 传感器 应用

1.3 说明

TI MSP 系列超低功耗微控制器种类繁多，各成员器件配备不同的外设集以满足各类应用的 需求。该架构与五种低功耗模式配合使用，是延长便携式测量应用电池寿命的最优 选择。该器件 采用 一个强大的 16 位精简指令集 (RISC) CPU，使用 16 位寄存器以及常数发生器，以便获得最高编码效率。数控振荡器 (DCO) 可使该器件在不到 1µs 的时间内实现从低功率模式唤醒至激活模式。

MSP430AFE2x3 器件是超低功耗混合信号微控制器，集成了三个独立的 24 位 Σ-Δ ADC、一个 16 位计时器、一个 16 位硬件乘法器、USART 通信接口、看门狗计时器和 11 个 I/O 引脚。

MSP430AFE2x2 器件与 MSP430AFE2x3 基本相同，唯一的差异是前者仅集成了两个 24 位 Σ-Δ ADC。

MSP430AFE2x1 器件与 MSP430AFE2x3 基本相同，唯一的差异是前者仅集成了一个 24 位 Σ-Δ ADC。

器件信息(1)

器件型号	封装	封装尺寸
MSP430AFE253IPW	TSSOP (24)	7.8mm × 4.4mm

(1) 有关更多信息，请参阅节 8*机械、封装和可订购信息*。

1.4 功能框图

图 1-1 给出了功能框图。

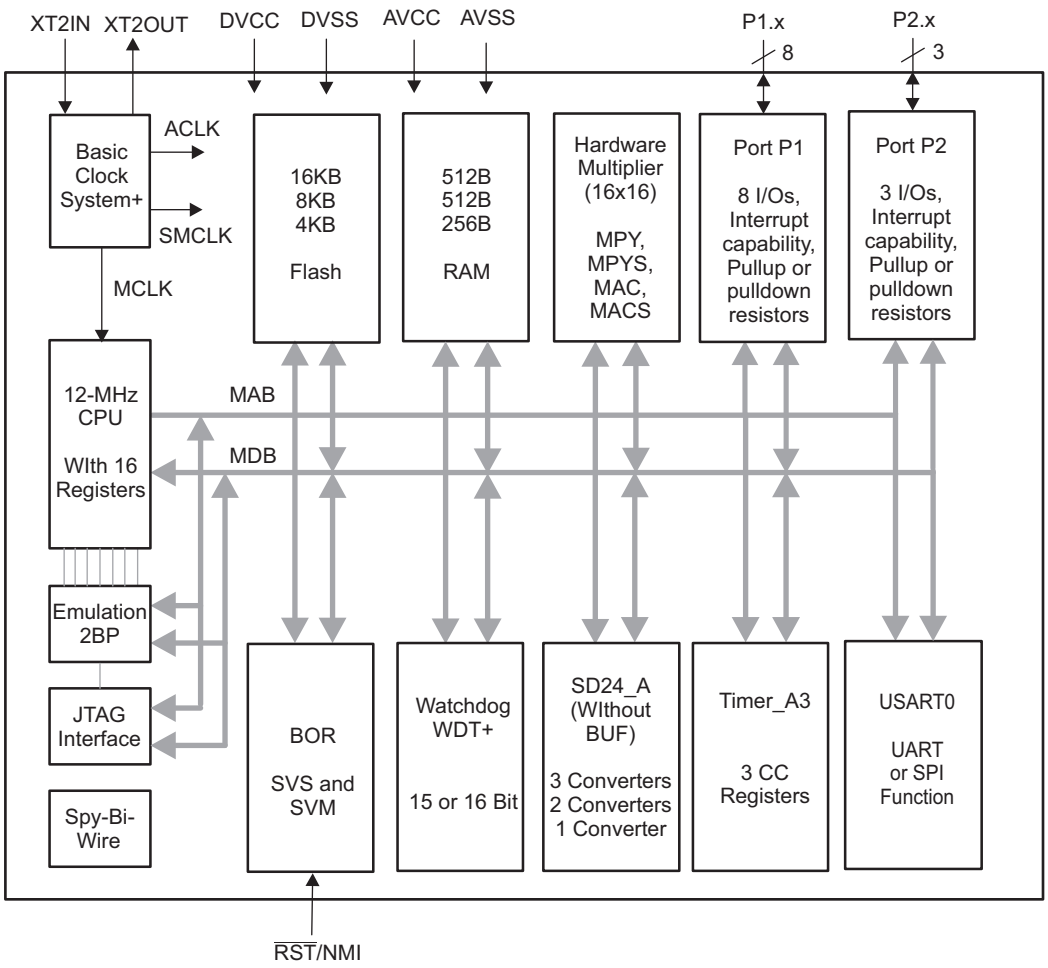


图 **1-1.** 功能框图

内容

2 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from March 21, 2011 to June 11, 2018 **Page**

- 通篇更改文档格式，其中包括添加章节编号 1
- 添加了节 1.2*应用*..... 1
- 添加了节 1.4*功能框图*，并将功能框图移到此部分 2
- Added Section 3.1, *Related Products* 5
- Added Section 5, *Specifications*, and moved all electrical specifications to it 9
- Added Section 5.2, *ESD Ratings* 9
- Added Section 5.4, *Thermal Resistance Characteristics* 10
- Removed figure *Oscillation Allowance vs Crystal Frequency* 22
- 添加了节 7*器件和文档支持*..... 48
- 添加了节 8*机械、封装和可订购信息* 53

3 Device Comparison

Table 3-1 summarizes the available family members.

Table 3-1. Device Comparison(1)

DEVICE	FLASH (KB)	SRAM (Byte)	EEM	SD24_A CONVERTERS	16-BIT MPY	Timer_A(2)	USART (UART, SPI)	CLOCKS	I/O	PACKAGE
MSP430AFE253IPW	16	512	1	3	1	3	1	HF, DCO, VLO	11	24-TSSOP
MSP430AFE233IPW	8	512	1	3	1	3	1	HF, DCO, VLO	11	24-TSSOP
MSP430AFE223IPW	4	256	1	3	1	3	1	HF, DCO, VLO	11	24-TSSOP
MSP430AFE252IPW	16	512	1	2	1	3	1	HF, DCO, VLO	11	24-TSSOP
MSP430AFE232IPW	8	512	1	2	1	3	1	HF, DCO, VLO	11	24-TSSOP
MSP430AFE222IPW	4	256	1	2	1	3	1	HF, DCO, VLO	11	24-TSSOP
MSP430AFE251IPW	16	512	1	1	1	3	1	HF, DCO, VLO	11	24-TSSOP
MSP430AFE231IPW	8	512	1	1	1	3	1	HF, DCO, VLO	11	24-TSSOP
MSP430AFE221IPW	4	256	1	1	1	3	1	HF, DCO, VLO	11	24-TSSOP

(1) For the most current package and ordering information, see the *Package Option Addendum* in 节 8, or see the TI website at www.ti.com.
(2) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.

3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

Products for MSP430 ultra-low-power sensing and measurement MCUs One platform. One ecosystem. Endless possibilities.

Products for MSP430 ultra-low-power MCUs MCUs for metrology, monitoring, system control, and communications

Companion Products for MSP430AFE253 Review products that are frequently purchased or used in conjunction with this product.

Reference Designs for MSP430AFE253 TI reference designs leverage the best in TI technology – from analog and power management to embedded processors. All designs include a schematic, test data, and design files. Search and download designs at ti.com/tidesigns.

4 Terminal Configuration and Functions

4.1 Pin Diagrams

Figure 4-1 shows the pinout of the MSP430AFE2x3 devices in the 24-pin PW (TSSOP) package.

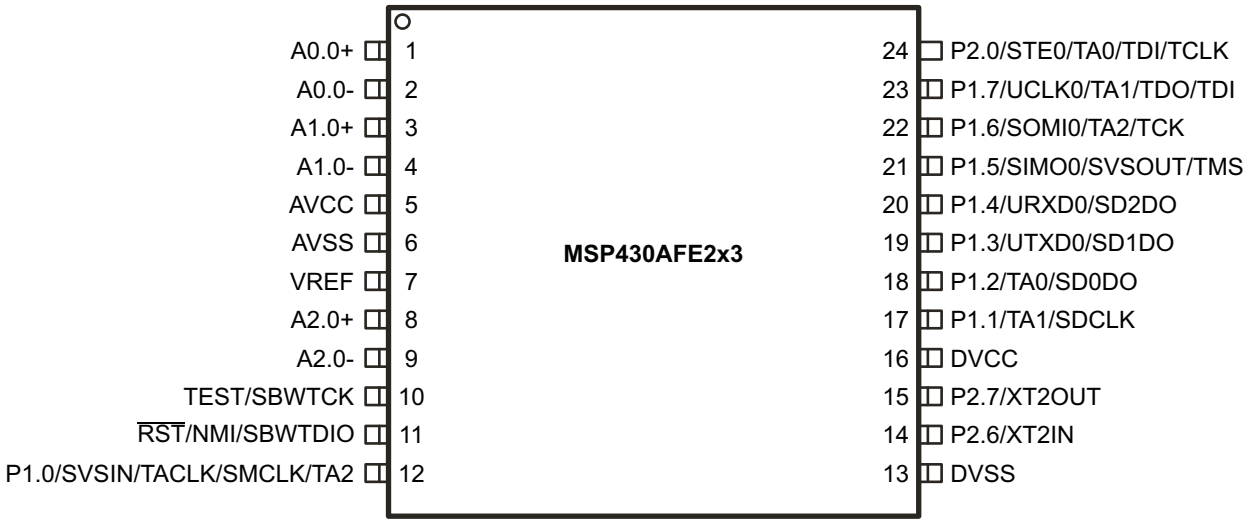
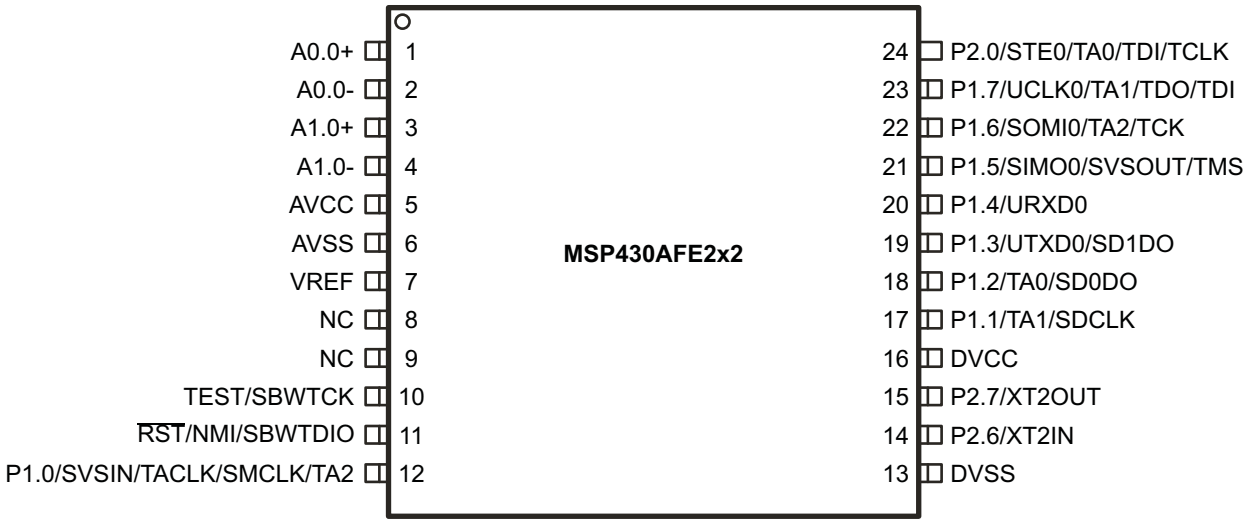


Figure 4-1. 24-Pin PW Package (Top View), MSP430AFE2x3

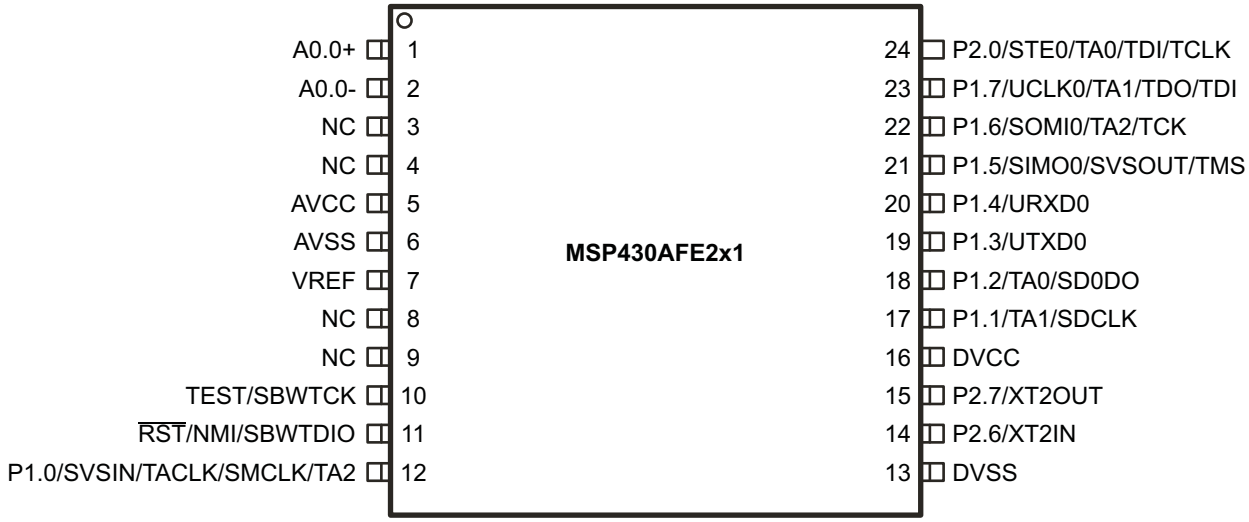
Figure 4-2 shows the pinout of the MSP430AFE2x2 devices in the 24-pin PW (TSSOP) package.



NOTE: Connect NC pins to analog ground (AVSS)

Figure 4-2. 24-Pin PW Package (Top View), MSP430AFE2x2

Figure 4-3 shows the pinout of the MSP430AFE2x1 devices in the 24-pin PW (TSSOP) package.



NOTE: Connect NC pins to analog ground (AVSS)

Figure 4-3. 24-Pin PW Package (Top View), MSP430AFE2x1

4.2 Signal Descriptions

Table 4-1 describes the signals for all device variants.

Table 4-1. Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
A0.0+	1	I	SD24_A positive analog input A0.0(1)
A0.0-	2	I	SD24_A negative analog input A0.0(1)
A1.0+	3	I	SD24_A positive analog input A1.0 (not available on MSP430AFE2x1)(1)
A1.0-	4	I	SD24_A negative analog input A1.0 (not available on MSP430AFE2x1)(1)
AVCC	5		Analog supply voltage, positive terminal. Must not power up prior to DVCC.
AVSS	6		Analog supply voltage, negative terminal
VREF	7	I/O	Input for an external reference voltage output for internal reference voltage (can be used as mid-voltage)
A2.0+	8	I	SD24_A positive analog input A2.0 (not available on MSP430AFE2x2 and MSP430AFE2x1)(1)
A2.0-	9	I	SD24_A negative analog input A2.0 (not available on MSP430AFE2x2 and MSP430AFE2x1)(1)
TEST/SBWTCK	10	I	Selects test mode for JTAG pins on P1.5 to P1.7 and P2.0. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input for device programming and test.
RST/NMI/SBWTDIO	11	I	Reset or nonmaskable interrupt input Spy-Bi-Wire test data input/output for device programming and test.
P1.0/SVSIN/TACLK/SMCLK/TA2	12	I/O	General-purpose digital I/O pin Analog input to supply voltage supervisor Timer_A3, clock signal TACLK input SMCLK signal output Timer_A3, compare: Out2 Output
DVSS	13		Digital supply voltage, negative terminal
P2.6/XT2IN	14	I/O	Input terminal of crystal oscillator General-purpose digital I/O pin
P2.7/XT2OUT	15	I/O	Output terminal of crystal oscillator General-purpose digital I/O pin

(1) TI recommends shorting unused analog input pairs and connecting them to analog ground.

Table 4-1. Terminal Functions (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
DVCC	16		Digital supply voltage, positive terminal.
P1.1/TA1/SDCLK	17	I/O	General-purpose digital I/O pin Timer_A3, capture: CCI1A and CCI1B inputs, compare: Out1 output SD24_A bit stream clock output
P1.2/TA0/SD0DO	18	I/O	General-purpose digital I/O pin Timer_A3, capture: CCI0A and CCI0B inputs, compare: Out0 output SD24_A bit stream data output for channel 0
P1.3/UTXD0/SD1DO	19	I/O	General-purpose digital I/O pin Transmit data out - USART0 in UART mode SD24_A bit stream data output for channel 1 (not available on MSP430AFE2x1)
P1.4/URXD0/SD2DO	20	I/O	General-purpose digital I/O pin Receive data in - USART0 in UART mode SD24_A bit stream data output for channel 2 (not available on MSP430AFE2x2 and MSP430AFE2x1)
P1.5/SIMO0/SVSOUT/TMS	21	I/O	General-purpose digital I/O Slave in/master out of USART0 in SPI mode SVS: output of SVS comparator JTAG test mode select. TMS is used as an input port for device programming and test.
P1.6/SOMI0/TA2/TCK	22	I/O	General-purpose digital I/O pin Slave out/master in of USART0 in SPI mode Timer_A3, compare: Out2 output JTAG test clock. TCK is the clock input port for device programming and test.
P1.7/UCLK0/TA1/TDO/TDI	23	I/O	General-purpose digital I/O pin External clock input - USART0 in UART or SPI mode, clock output - USART0/SPI mode. Timer_A3, compare: Out1 output JTAG test data output port. TDO/TDI data output or programming data input terminal.
P2.0/STE0/TA0/TDI/TCLK	24	I/O	General-purpose digital I/O pin Slave transmit enable - USART0 in SPI mode. Timer_A3, compare: Out0 output JTAG test data input or test clock input for device programming and test.

5 Specifications

5.1 Absolute Maximum Ratings(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
Voltage applied at V_{CC} to V_{SS}		–0.3	4.1	V
Voltage applied to any pin(2)		–0.3	V_{CC} + 0.3	V
Diode current at any device terminal		–2	2	mA
Storage temperature, T_{stg}	Unprogrammed device	–55	150	°C
	Programmed device	–40	85	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to VSS. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.

5.2 ESD Ratings

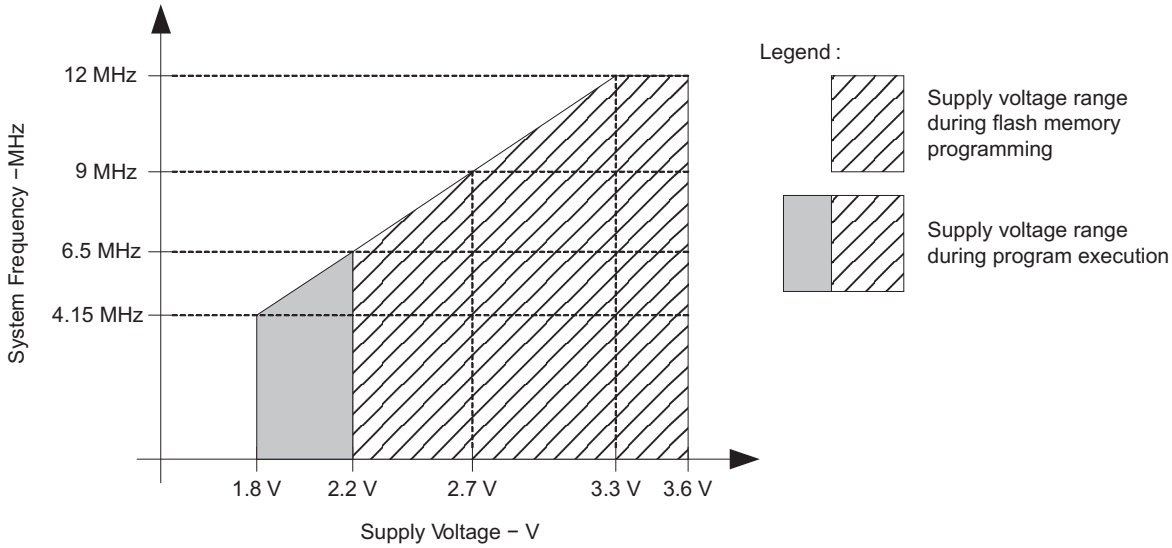
			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions(1)(2)

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	AVCC = DVCC = V_{CC}(1)	During program execution(3)	1.8		3.6	V
			During program or erase of flash memory	2.2		3.6	
V_{SS}	Supply voltage	AVSS = DVSS = V_{SS}			0		V
T_A	Operating free-air temperature			–40		85	°C
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)(1)(2) (see Figure 5-1)	V_{CC} = 1.8 V, Duty cycle = 50% ±10%		dc		4.15	MHz
		V_{CC} = 2.7 V, Duty cycle = 50% ±10%		dc		9	
		V_{CC} ≥ 3.3 V, Duty cycle = 50% ±10%		dc		12	

(1) The MSP430 CPU is clocked directly with MCLK. Both the high and low phases of MCLK must not exceed the pulse duration of the specified maximum frequency.
(2) Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.
(3) The operating voltage range for SD24_A is 2.5 V to 3.6 V



A. Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

B. If high frequency crystal used is above 12 MHz and selected to source CPU clock then MCLK divider should be programmed appropriately to run CPU below 8 MHz.

Figure 5-1. Operating Area

5.4 Thermal Resistance Characteristics for PW-24 Package

THERMAL METRIC(1) (2)		VALUE(3)	UNIT
$R\theta_{JA}$	Junction-to-ambient thermal resistance, still air	76.4	°C/W
$R\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance	21.1	°C/W
$R\theta_{JC(BOT)}$	Junction-to-case (bottom) thermal resistance	31.7	°C/W
$R\theta_{JB}$	Junction-to-board thermal resistance	31.1	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter	1.0	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment and application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(3) N/A = Not applicable

5.5 Active Mode Supply Current (Into DVCC and AVCC) Excluding External Current(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{AM,\ 1MHz}$	Active mode (AM) current at 1 MHz	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = DCO default frequency (approximately 1 MHz), $f_{ACLK} = f_{VLO}$ = 12 kHz, Program executes in flash, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	2.2 V		220		µA
			3 V		350		
$I_{AM,\ 12MHz}$	Active mode (AM) current at 12 MHz	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 12 MHz, $f_{ACLK} = f_{VLO}$ = 12 kHz, Program executes in flash, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	3.3 V		4.0	4.5	mA

(1) All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.

5.6 Typical Characteristics – Active-Mode Supply Current (Into DVCC and AVCC)

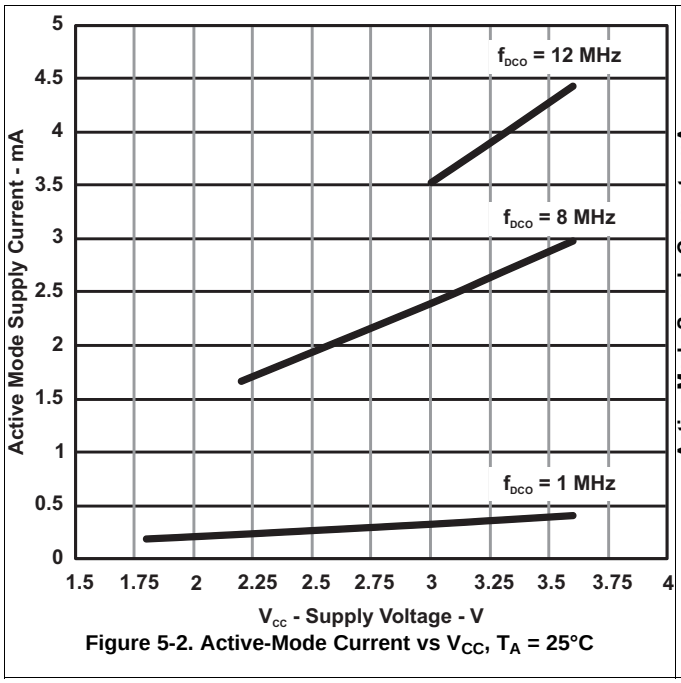


Figure 5-2. Active-Mode Current vs V_{CC}, T_A = 25°C

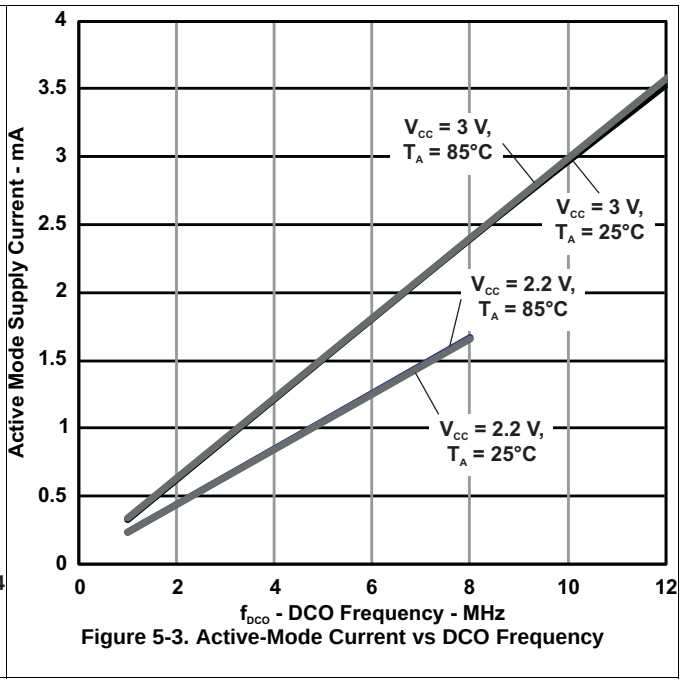


Figure 5-3. Active-Mode Current vs DCO Frequency

5.7 Low-Power-Mode Supply Currents (Into V_{CC}) Excluding External Current(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
I_{LPM0}	Low-power mode 0 (LPM0) current(2)	f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = DCO default frequency (approximately 1 MHz), f_{ACLK} = f_{VLO} = 12 kHz, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0	25°C	2.2 V		65		µA
I_{LPM2}	Low-power mode 2 (LPM2) current(3)	f_{MCLK} = f_{SMCLK} = 0 MHz, f_{DCO} = DCO default frequency (approximately 1 MHz), f_{ACLK} = f_{VLO} = 12 kHz, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	25°C	2.2 V		22		µA
$I_{LPM3,VLO}$	Low-power mode 3 (LPM3) current(3)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = f_{VLO} = 12 kHz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	25°C	2.2 V		0.5	1.0	µA
I_{LPM4}	Low-power mode 4 (LPM4) current(4)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = f_{VLO} = 0 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	25°C	2.2 V		0.1	0.7	µA
			85°C			1.1	2.5	

(1) All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.
(2) Current for brownout and WDT clocked by SMCLK included.
(3) Current for brownout and WDT clocked by ACLK included.
(4) Current for brownout included.

5.8 Typical Characteristics – LPM4 Current

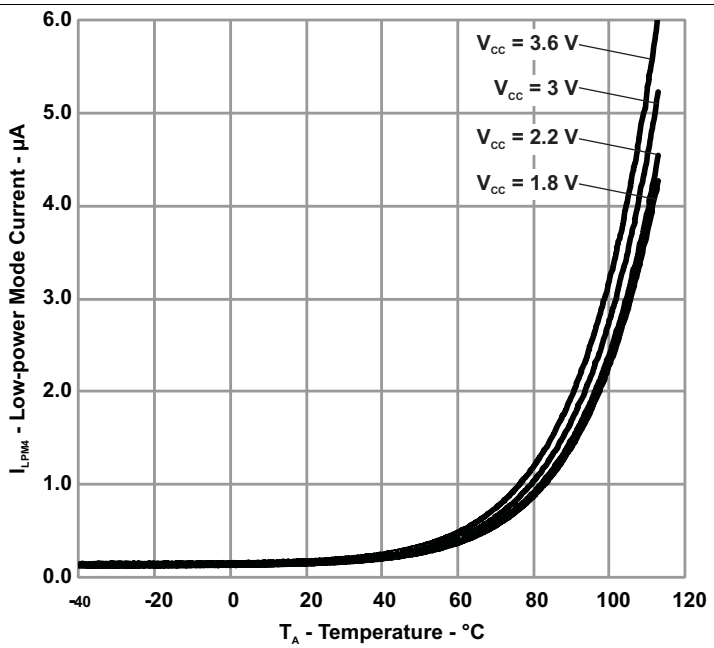


Figure 5-4. I_{LPM4} -- LPM4 Current vs Temperature

5.9 Schmitt-Trigger Inputs (Ports Px and $\overline{RST}$/NMI)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage			0.45 V_{CC}		0.75 V_{CC}	V
			3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage			0.25 V_{CC}		0.55 V_{CC}	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis ($V_{IT+} – V_{IT–}$)		3 V	0.3		1.0	V
R_{Pull}	Pullup or pulldown resistor (not $\overline{RST}$/NMI pin)	For pullup: $V_{IN} = V_{SS}$, For pulldown: $V_{IN} = V_{CC}$	3 V	20	35	50	kΩ
C_I	Input capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF

5.10 Leakage Current (Ports Px)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$I_{lkg(Px.y)}$	High-impedance leakage current	See (1) (2)	3 V		±50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin, unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

5.11 Outputs (Ports Px)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)}$ = –6 mA(1)	3 V		V_{CC} – 0.2		V
V_{OL}	Low-level output voltage	$I_{OL(max)}$ = 6 mA(1)	3 V		V_{SS} + 0.2		V

(1) The maximum total current ($I_{OH(max)}$ and $I_{OL(max)}$) for all outputs combined cannot exceed ±48 mA to hold the maximum voltage drop specified.

5.12 Output Frequency (Ports Px)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	Px.y, C_L = 20 pF, R_L = 1 kΩ(1)(2)	3 V		12		MHz
f_{Port_CLK}	Clock output frequency	Px.y, C_L = 20 pF(2)	3 V		16		MHz

(1) A resistive divider with two 0.5-kΩ resistors between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

5.13 Typical Characteristics – Outputs

One output loaded at a time.

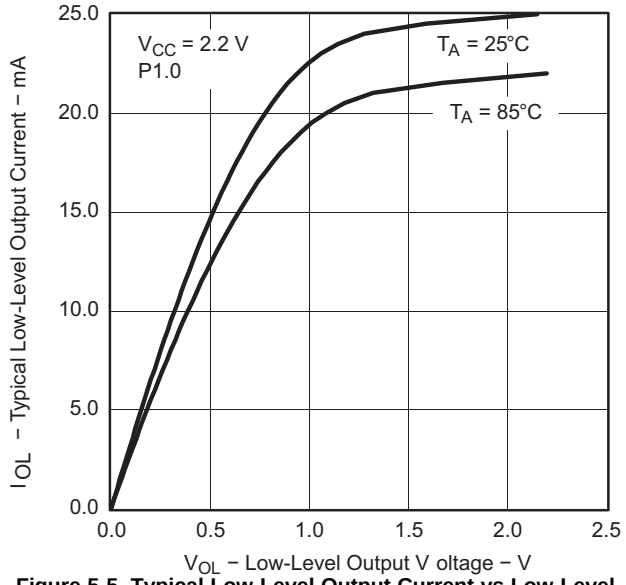


Figure 5-5. Typical Low-Level Output Current vs Low-Level Output Voltage

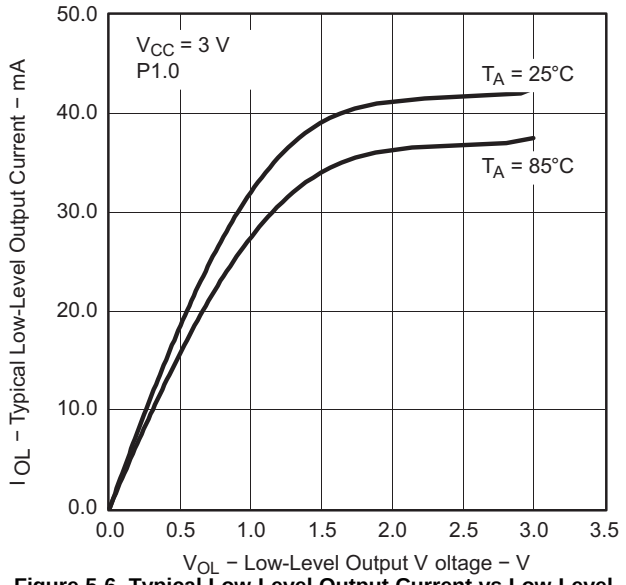


Figure 5-6. Typical Low-Level Output Current vs Low-Level Output Voltage

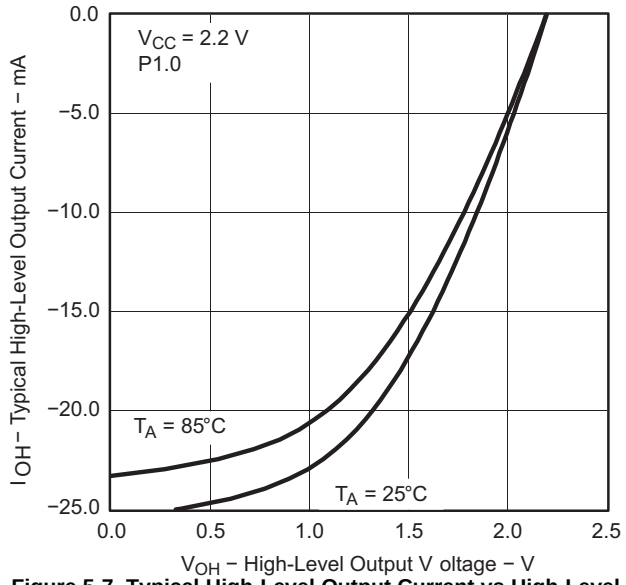


Figure 5-7. Typical High-Level Output Current vs High-Level Output Voltage

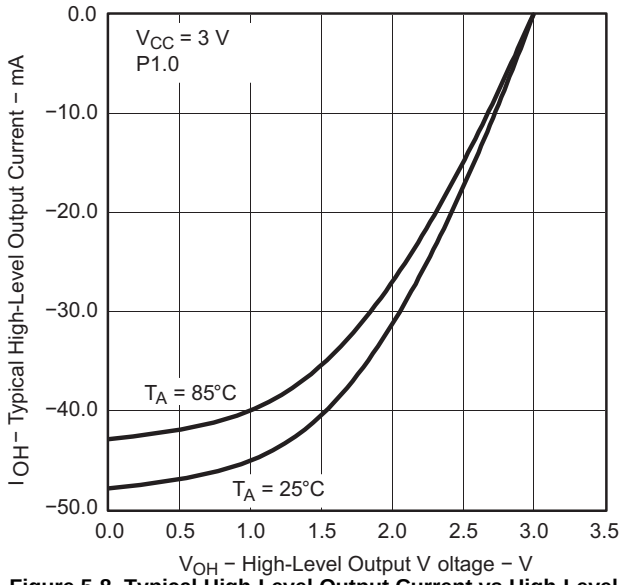


Figure 5-8. Typical High-Level Output Current vs High-Level Output Voltage

5.14 POR, BOR(1)(2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(start)}$	See Figure 5-9	$dV_{CC}/dt \le 3$ V/s			0.7 × $V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$	See Figure 5-9 through Figure 5-11	$dV_{CC}/dt \le 3$ V/s			1.42		V
$V_{hys(B\_IT-)}$	See Figure 5-9	$dV_{CC}/dt \le 3$ V/s			120		mV
$t_{d(BOR)}$	See Figure 5-9				2000		µs
$t_{(reset)}$	Pulse duration needed at $\overline{RST}$/NMI pin to accepted reset internally		3 V	2			µs

(1) The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)}$ + $V_{hys(B\_IT-)}$ is ≤ 1.8 V.

(2) During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$. The default DCO settings must not be changed until $V_{CC} \ge V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency.

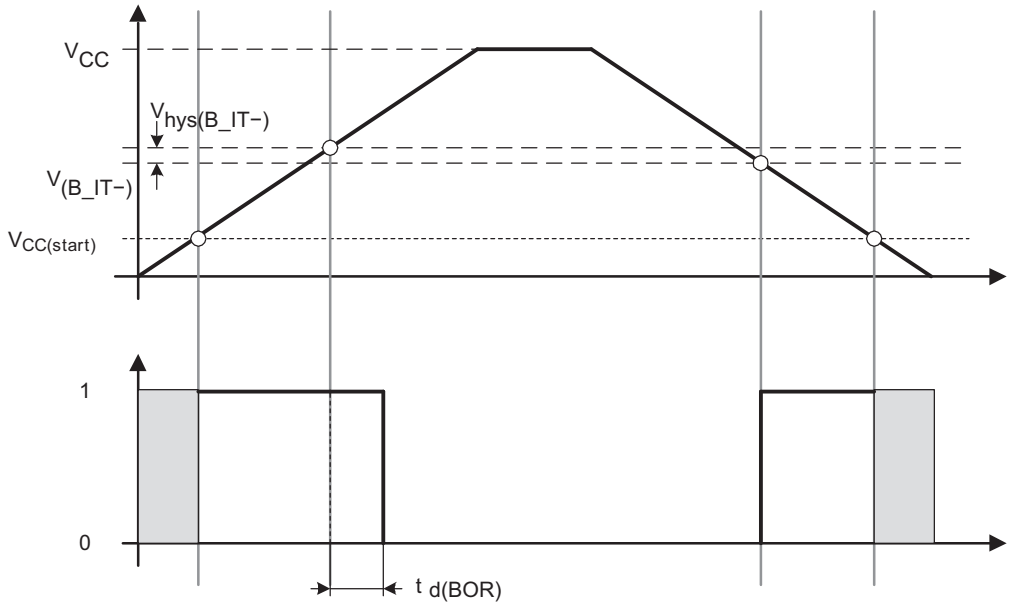


Figure 5-9. POR, BOR vs Supply Voltage

5.15 Typical Characteristics – POR, BOR

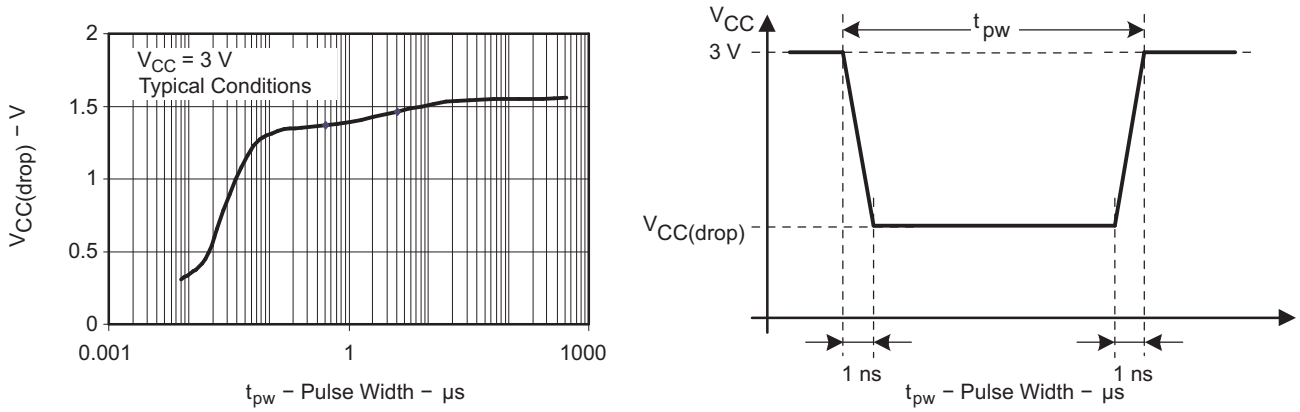


Figure 5-10. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR or BOR Signal

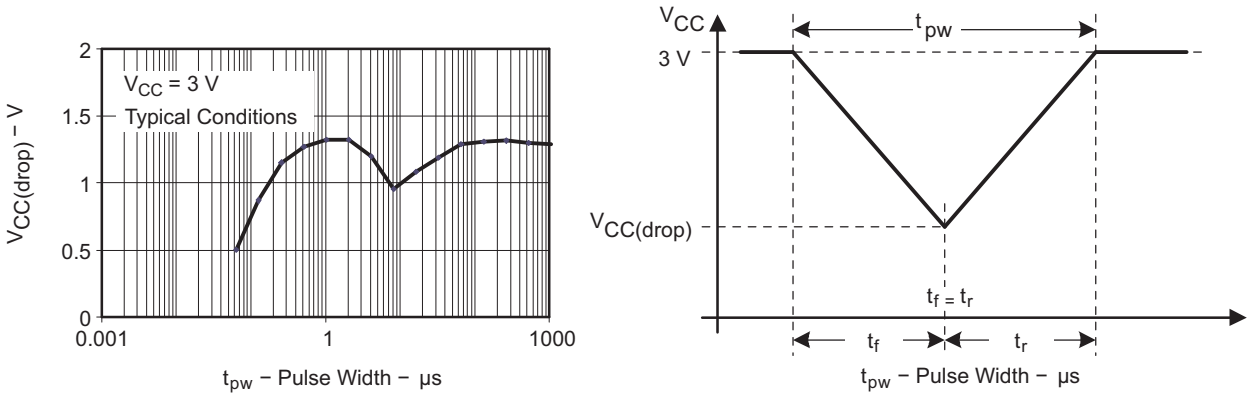


Figure 5-11. $V_{CC(drop)}$ Level With a Triangular Voltage Drop to Generate a POR or BOR Signal

5.16 Supply Voltage Supervisor (SVS), Supply Voltage Monitor (SVM)(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(SVSR)}$	dV_{CC}/dt > 30 V/ms (see Figure 5-12)			100		µs
	dV_{CC}/dt ≤ 30 V/ms			2000		
$t_{d(SVSon)}$	SVS on, switch from VLD = 0 to VLD ≠ 0, V_{CC} =3 V			100		µs
t_{settle}	VLD ≠ 0(2)			12		µs
$V_{(SVSstart)}$	VLD ≠ 0, V_{CC}/dt ≤ 3 V/s (see Figure 5-12)			1.55	1.7	V
$V_{hys(SVS\_IT-)}$	V_{CC}/dt ≤ 3 V/s (see Figure 5-12)	VLD = 1		120		mV
		VLD = 2 to 14		15		
	V_{CC}/dt ≤ 3 V/s (see Figure 5-12), external voltage applied on SVSIN	VLD = 15		10		
$V_{(SVS\_IT-)}$	V_{CC}/dt ≤ 3V/s (see Figure 5-12)	VLD = 1	1.8	1.9	2.05	V
		VLD = 2		2.1		
		VLD = 3		2.2		
		VLD = 4		2.3		
		VLD = 5	2.24	2.4	2.6	
		VLD = 6		2.5		
		VLD = 7		2.65		
		VLD = 8		2.8		
		VLD = 9	2.69	2.9	3.13	
		VLD = 10		3.05		
		VLD = 11		3.2		
		VLD = 12		3.35		
		VLD = 13	3.24	3.5	3.76(3)	
		VLD = 14		3.7(3)		
	V_{CC}/dt ≤ 3 V/s (see Figure 5-12), external voltage applied on SVSIN	VLD = 15	1.1	1.2	1.3	
$I_{CC(SVS)}$(1)	VLD ≠ 0, V_{CC} = 3 V			12	17	µA

(1) The current consumption of the SVS module is not included in the I_{CC} current consumption data.
(2) t_{settle} is the settling time that the comparator operational amplifier needs to have a stable level after VLD is switched from VLD ≠ 0 to a different VLD value between 2 and 15. The overdrive is assumed to be greater than 50 mV.
(3) The recommended operating voltage range is limited to 3.6 V.

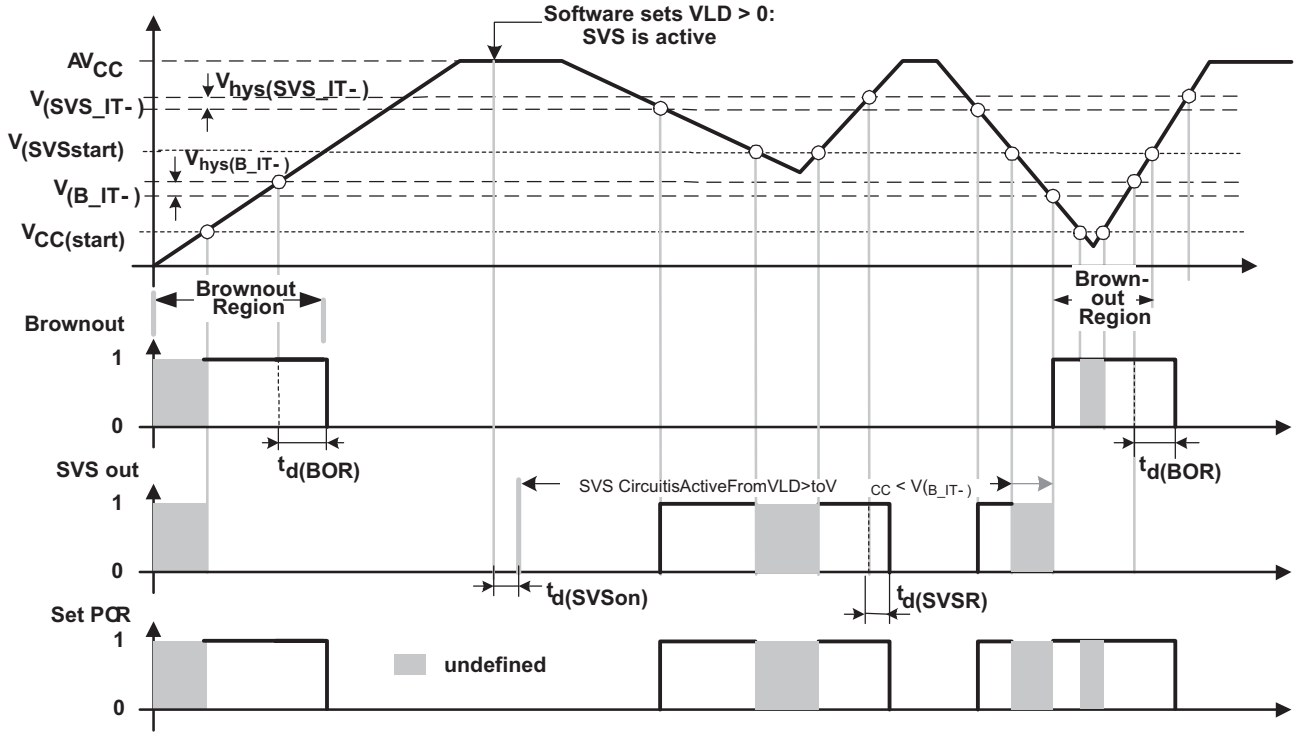


Figure 5-12. SVS Reset (SVSR) vs Supply Voltage

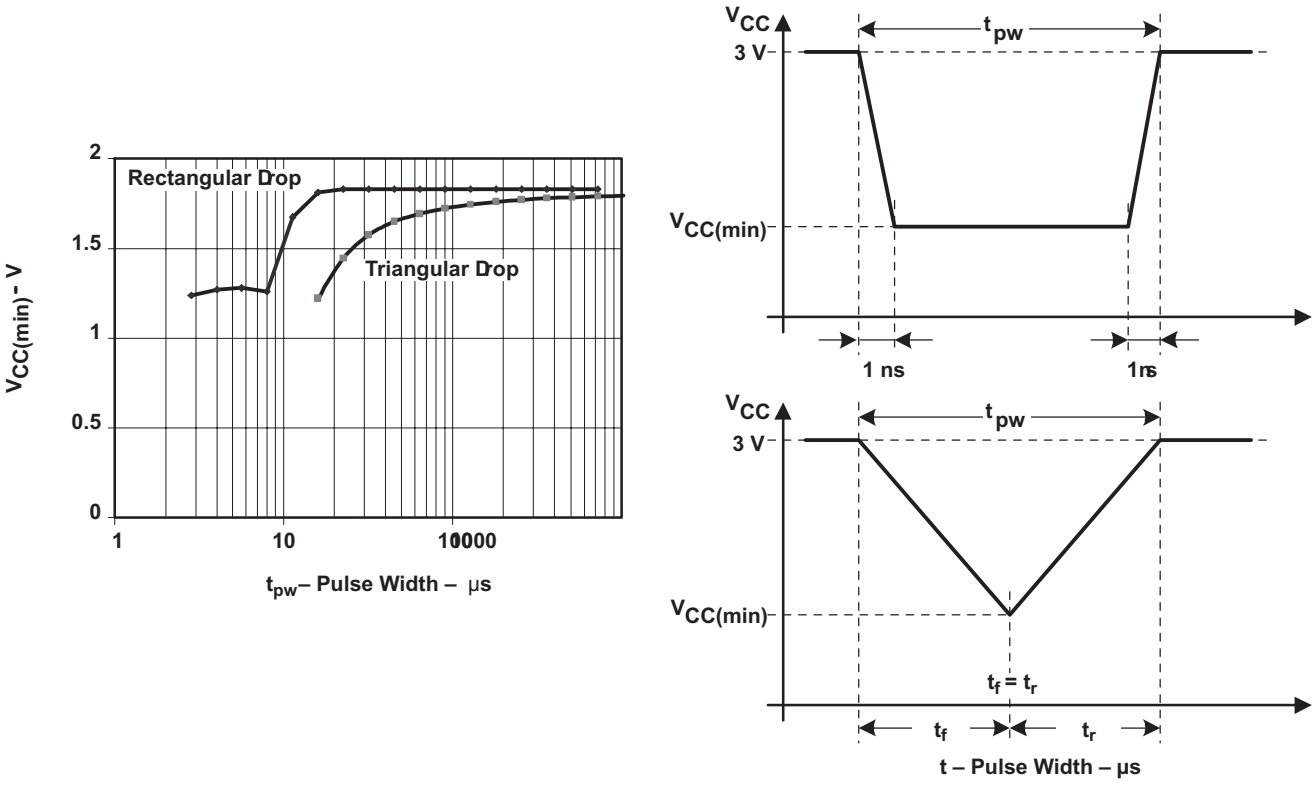


Figure 5-13. $V_{CC(min)}$ With a Square Voltage Drop and a Triangular Voltage Drop to Generate an SVS Signal

5.17 Main DCO Characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S_{DCO}.
- Modulation control bits MODx select how often $f_{DCO(RSEL,DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{DCO(RSEL,DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{DCO(RSEL,DCO)} \times f_{DCO(RSEL,DCO+1)}}{MOD \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO+1)}}$$

5.18 DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range	RSELx < 14		1.8		3.6	V
		RSELx = 14		2.2		3.6	
		RSELx = 15		3.0		3.6	
$f_{DCO(0,0)}$	DCO frequency (0, 0)	RSELx = 0, DCOx = 0, MODx = 0	3.3 V	0.06	0.10	0.14	MHz
$f_{DCO(0,3)}$	DCO frequency (0, 3)	RSELx = 0, DCOx = 3, MODx = 0	3.3 V		0.12		MHz
$f_{DCO(1,3)}$	DCO frequency (1, 3)	RSELx = 1, DCOx = 3, MODx = 0	3.3 V		0.15		MHz
$f_{DCO(2,3)}$	DCO frequency (2, 3)	RSELx = 2, DCOx = 3, MODx = 0	3.3 V		0.21		MHz
$f_{DCO(3,3)}$	DCO frequency (3, 3)	RSELx = 3, DCOx = 3, MODx = 0	3.3 V		0.30		MHz
$f_{DCO(4,3)}$	DCO frequency (4, 3)	RSELx = 4, DCOx = 3, MODx = 0	3.3 V		0.41		MHz
$f_{DCO(5,3)}$	DCO frequency (5, 3)	RSELx = 5, DCOx = 3, MODx = 0	3.3 V		0.58		MHz
$f_{DCO(6,3)}$	DCO frequency (6, 3)	RSELx = 6, DCOx = 3, MODx = 0	3.3 V		0.80		MHz
$f_{DCO(7,3)}$	DCO frequency (7, 3)	RSELx = 7, DCOx = 3, MODx = 0	3.3 V		1.15		MHz
$f_{DCO(8,3)}$	DCO frequency (8, 3)	RSELx = 8, DCOx = 3, MODx = 0	3.3 V		1.60		MHz
$f_{DCO(9,3)}$	DCO frequency (9, 3)	RSELx = 9, DCOx = 3, MODx = 0	3.3 V		2.30		MHz
$f_{DCO(10,3)}$	DCO frequency (10, 3)	RSELx = 10, DCOx = 3, MODx = 0	3.3 V		3.40		MHz
$f_{DCO(11,3)}$	DCO frequency (11, 3)	RSELx = 11, DCOx = 3, MODx = 0	3.3 V		4.25		MHz
$f_{DCO(12,3)}$	DCO frequency (12, 3)	RSELx = 12, DCOx = 3, MODx = 0	3.3 V		5.80		M Hz
$f_{DCO(13,3)}$	DCO frequency (13, 3)	RSELx = 13, DCOx = 3, MODx = 0	3.3 V		7.80		MHz
$f_{DCO(14,3)}$	DCO frequency (14, 3)	RSELx = 14, DCOx = 3, MODx = 0	3.3 V	8.6	11.25	13.9	MHz
$f_{DCO(15,3)}$	DCO frequency (15, 3)	RSELx = 15, DCOx = 3, MODx = 0	3.3 V		15.30		MHz
$f_{DCO(15,7)}$	DCO frequency (15, 7)	RSELx = 15, DCOx = 7, MODx = 0	3.3 V		21.00		MHz
S_{RSEL}	Frequency step between range RSEL and RSEL+1	$S_{RSEL} = f_{DCO(RSEL+1,DCO)}/f_{DCO(RSEL,DCO)}$	3.3 V		1.35		ratio
S_{DCO}	Frequency step between tap DCO and DCO+1	$S_{DCO} = f_{DCO(RSEL,DCO+1)}/f_{DCO(RSEL,DCO)}$	3.3 V		1.08		ratio
	Duty cycle	Measured at SMCLK output	3.3 V		50		%

5.19 Calibrated DCO Frequencies – Tolerance

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
8-MHz tolerance over temperature(1)	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3.3 V	0°C to 85°C	3.3 V	7.76	8	8.24	MHz
8-MHz tolerance over V_{CC}	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3.3 V	30°C	2.7 V to 3.6 V	7.76	8	8.24	MHz
8-MHz tolerance overall	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3.3 V	–40°C to 85°C	2.7 V to 3.6 V	7.52	8	8.48	MHz
12-MHz tolerance over temperature(1)	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3.3 V	0°C to 85°C	3.3 V	11.64	12	12.36	MHz
12-MHz tolerance over V_{CC}	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3.3 V	30°C	3.3 V to 3.6 V	11.64	12	12.36	MHz
12-MHz tolerance overall	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3.3 V	–40°C to 85°C	3.3 V to 3.6 V	11.28	12	12.72	MHz

(1) This is the frequency change from the measured frequency at 30°C over temperature.

5.20 Wake-up Times From Lower-Power Modes (LPM3, LPM4)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{DCO,LPM3/4}$	DCO clock wake-up time from LPM3 or LPM4(1)	f_{DCO} = DCO default frequency (approximately 1 MHz)	3 V		1.5		µs
$t_{CPU,LPM3/4}$	CPU wake-up time from LPM3 or LPM4(2)				$1 / f_{MCLK} + t_{DCO,LPM3/4}$		µs

(1) The DCO clock wake-up time is measured from the edge of an external wake-up signal (for example, a port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
(2) Parameter applicable only if DCOCLK is used for MCLK.

5.21 Typical Characteristics – DCO Clock Wake-up Time

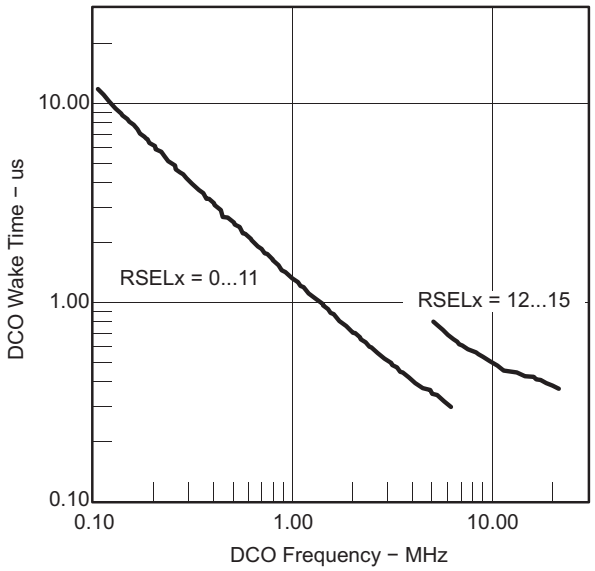


Figure 5-14. Clock Wake-up Time From LPM3 vs DCO Frequency

5.22 Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		T_A	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	–40°C to 85°C	3 V	4	12	22	kHz
df_{VLO}/dT	VLO frequency temperature drift(1)	–40°C to 85°C	3 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift(2)	25°C	1.8 V to 3.6 V		4		%/V

(1) Calculated using the box method: [MAX(–40°C to 85°C) – MIN(–40°C to 85°C)] / MIN(–40°C to 85°C) / [85°C – (–40°C)]
(2) Calculated using the box method: [MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)] / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

5.23 Crystal Oscillator (XT2)(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{XT2,HF0}$	XT2 oscillator crystal frequency, HF mode 0	XT2OFF = 0, XT2Sx = 0	1.8 V to 3.6 V	0.4		1	MHz
$f_{XT2,HF1}$	XT2 oscillator crystal frequency, HF mode 1	XT2OFF = 0, XT2Sx = 1	1.8 V to 3.6 V	1		4	MHz
$f_{XT2,HF2}$	XT2 oscillator crystal frequency, HF mode 2	XT2OFF = 0, XT2Sx = 2	1.8 V to 2.2 V	2		10	MHz
			2.2 V to 3.0 V	2		12	
			3.0 V to 3.6 V	2		16	
$f_{XT2,HF,logic}$	XT2 oscillator logic-level square-wave input frequency, HF mode	XT2OFF = 0, XT2Sx = 3	1.8 V to 2.2 V	0.4		10	MHz
			2.2 V to 3.0 V	0.4		12	
			3.0 V to 3.6 V	0.4		16	
OA_{HF}	Oscillation allowance for HF crystals (see Figure 5-15)	XT2OFF = 0, XT2Sx = 0 $f_{XT2,HF}$ = 1 MHz, $C_{L,eff}$ = 15 pF			2700		Ω
		XT2OFF = 0, XT2Sx = 1 $f_{XT2,HF}$ = 4 MHz, $C_{L,eff}$ = 15 pF			800		
		XT2OFF = 0, XT2Sx = 2 $f_{XT2,HF}$ = 16 MHz, $C_{L,eff}$ = 15 pF			300		
$C_{L,eff}$	Integrated effective load capacitance, HF mode(2)	XT2OFF = 0(3)			1		pF
	Duty cycle	XT2OFF = 0, Measured at P1.0/SVSIN/TACLK/SMCLK/TA2, $f_{XT2,HF}$ = 10 MHz	3 V	40	50	60	%
		XT2OFF = 0, Measured at P1.0/SVSIN/TACLK/SMCLK/TA2, $f_{XT2,HF}$ = 16 MHz		40	50	60	
$f_{Fault,HF}$	Oscillator fault frequency (4)	XT2OFF = 0, XT2Sx = 3(5)	3 V	30		300	kHz

(1) To improve EMI on the XT2 oscillator, observe the following guidelines:
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XT2IN and XT2OUT.
- Avoid running PCB traces underneath or adjacent to the XT2IN and XT2OUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XT2IN and XT2OUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, TI recommends verifying the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
(3) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
(4) Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag, and frequencies in between might set the flag.
(5) Measured with logic-level input frequency, but also applies to operation with crystals.

5.24 Typical Characteristics – XT2 Oscillator

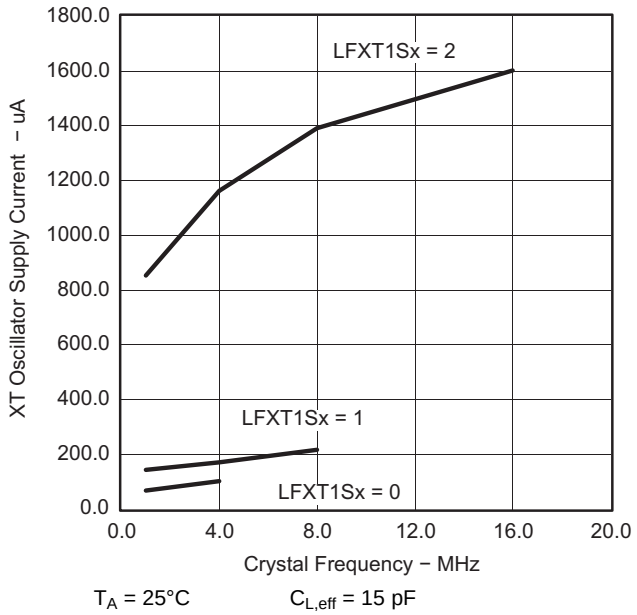


Figure 5-15. XT2 Oscillator Supply Current vs Crystal Frequency

5.25 SD24_A, Power Supply

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	$AV_{CC} = DV_{CC}$ $AV_{SS} = DV_{SS} = 0$ V			2.5		3.6	V
I_{SD24}	Analog supply current: 1 active SD24_A channel including internal reference	SD24LP = 0, f_{SD24} = 1 MHz, SD24OSR = 256	GAIN: 1, 2	3 V		800	1100	µA
			GAIN: 4, 8, 16			900		
			GAIN: 32			1200		
		SD24LP = 1, f_{SD24} = 0.5 MHz, SD24OSR = 256	GAIN: 1			800		
			GAIN: 32			900		
f_{SD24}	Analog front-end input clock frequency	SD24LP = 0 (low-power mode disabled)		3 V	0.03	1	1.1	MHz
		SD24LP = 1 (low-power mode enabled)			0.03	0.5		

5.26 SD24_A, Input Range(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$V_{ID,FSR}$	Differential full-scale input voltage range	Bipolar mode, SD24UNI = 0			$-V_{REF}$ / 2GAIN		$+V_{REF}$ / 2GAIN	mV
		Unipolar mode, SD24UNI = 1			0		$+V_{REF}$ / 2GAIN	
V_{ID}	Differential input voltage range for specified performance(2)	SD24REFON = 1	SD24GAINx = 1			±500		mV
			SD24GAINx = 2			±250		
			SD24GAINx = 4			±125		
			SD24GAINx = 8			±62		
			SD24GAINx = 16			±31		
			SD24GAINx = 32			±15		
Z_I	Input impedance (one input pin to AVSS)	f_{SD24} = 1 MHz	SD24GAINx = 1	3 V		200		kΩ
			SD24GAINx = 32			75		
Z_{ID}	Differential input impedance (IN+ to IN-)	f_{SD24} = 1 MHz	SD24GAINx = 1	3 V	300	400		kΩ
			SD24GAINx = 32		100	150		
V_I	Absolute input voltage range				AVSS – 1		AVCC	V
V_{IC}	Common-mode input voltage range				AVSS – 1		AVCC	V

(1) All parameters pertain to each SD24_A channel.
(2) The full-scale range is defined by $V_{FSR+} = +(V_{REF} / 2) / GAIN$ and $V_{FSR-} = -(V_{REF} / 2) / GAIN$. If VREF is sourced externally, the analog input range cannot exceed 80% of V_{FSR+} or V_{FSR-}; that is, $V_{ID} = 0.8 \times V_{FSR-}$ to $0.8 \times V_{FSR+}$. If VREF is sourced internally, the given V_{ID} ranges apply.

5.27 SD24_A, Performance

f_{SD24} = 1 MHz, SD24OSRx = 256, SD24REFON = 1, over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
G	Nominal gain	SD24GAINx = 1	3 V		1		
		SD24GAINx = 2			1.96		
		SD24GAINx = 4			3.86		
		SD24GAINx = 8			7.62		
		SD24GAINx = 16			15.04		
		SD24GAINx = 32			28.35		
E_{OS}	Offset error	SD24GAINx = 1	3 V			±0.2	%FSR
		SD24GAINx = 32				±1.5	
ΔEOS/ΔT	Offset error temperature coefficient	SD24GAINx = 1	3 V		±4	±20	ppm FSR/°C
		SD24GAINx = 32			±20	±100	
CMRR	Common-mode rejection ratio	SD24GAINx = 1, Common-mode input signal: V_{ID} = 500 mV, f_{IN} = 50 Hz or 100 Hz	3 V		>90		dB
		SD24GAINx = 32, Common-mode input signal: V_{ID} = 16 mV, f_{IN} = 50 Hz or 100 Hz			>75		
AC PSRR	AC power supply rejection ratio	SD24GAINx = 1, V_{CC} = 3 V ±100 mV, f_{VCC} = 50 Hz	3 V		>80		dB
XT	Crosstalk	SD24GAINx = 1, V_{ID} = 500 mV, f_{IN} = 50 Hz or 100 Hz	3 V		<–100		dB

5.28 SD24_A, Temperature Sensor and Built-In V_{CC} Sense

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
TC_{Sensor}	Sensor temperature coefficient			1.18	1.32	1.46	mV/°C
$V_{Offset,sensor}$	Sensor offset voltage			–100		100	mV
V_{Sensor}	Sensor output voltage(1)(2)	Temperature sensor voltage at T_A = 85°C	3 V	420	475	515	mV
		Temperature sensor voltage at T_A = 30°C		350	402	442	
$V_{CC,Sense}$	V_{CC} divider at input 5	f_{SD24} = 1 MHz, SD24OSRx = 256, SD24REFON = 1			V_{CC}/1 1		V
$R_{Source,VCC}$	Source resistance of V_{CC} divider at input 5				20		kΩ

(1) The following formula can be used to calculate the temperature sensor output voltage:
$V_{Sensor,typ} = TC_{Sensor}$ (273 + T [°C]) + $V_{Offset,sensor}$ [mV]
(2) Results based on characterization and/or production test, not TC_{Sensor} or $V_{Offset,sensor}$. Measured with f_{SD24} = 1 MHz, SD24OSRx = 256, SD24REFON = 1.

5.29 SD24_A, Built-In Voltage Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF}	Internal reference voltage	SD24REFON = 1, SD24VMIDON = 0	3 V	1.14	1.2	1.26	V
I_{REF}	Reference supply current	SD24REFON = 1, SD24VMIDON = 0	3 V		200	320	µA
TC	Temperature coefficient	SD24REFON = 1, SD24VMIDON = 0(1)	3 V		18	50	ppm/°C
C_{REF}	V_{REF} load capacitance	SD24REFON = 1, SD24VMIDON = 0(2)			100		nF
I_{LOAD}	$V_{REF(I)}$ maximum load current	SD24REFON = 1, SD24VMIDON = 0	3 V			±200	nA
t_{ON}	Turn-on time	SD24REFON = 0→1, SD24VMIDON = 0, C_{REF} = 100 nF	3 V		5		ms
DC PSR	DC power supply rejection $\Delta V_{REF}/\Delta V_{CC}$	SD24REFON = 1, SD24VMIDON = 0, V_{CC} = 2.5 V to 3.6 V			100		µV/V

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(2) There is no capacitance required on V_{REF}. However, a capacitance of at least 100 nF is recommended to reduce any reference voltage noise.

5.30 SD24_A, Reference Output Buffer

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{REF,BUF}$	Reference buffer output voltage	SD24REFON = 1, SD24VMIDON = 1	3 V		1.2		V
$I_{REF,BUF}$	Reference supply + reference output buffer quiescent current	SD24REFON = 1, SD24VMIDON = 1	3 V		430	650	µA
$C_{REF(O)}$	Required load capacitance on VREF	SD24REFON = 1, SD24VMIDON = 1		470			nF
$I_{LOAD,Max}$	Maximum load current on VREF	SD24REFON = 1, SD24VMIDON = 1	3 V			±1	mA
	Maximum voltage variation vs load current	$\|I_{LOAD}\|$ = 0 to 1 mA	3 V	–15		+15	mV
t_{ON}	Turnon time	SD24REFON = 0→1, SD24VMIDON = 0→1, C_{REF} = 470 nF	3 V		100		µs

5.31 SD24_A, External Reference Input

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{REF(I)}$	Input voltage range	SD24REFON = 0	3 V	1.0	1.25	1.5	V
$I_{REF(I)}$	Input current	SD24REFON = 0	3 V			50	nA

5.32 USART0

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{USART}	USART clock frequency				8	MHz
$t_{(\tau)}$	USART0: deglitch time(1)	V_{CC} = 3 V, SYNC = 0, UART mode	150	280	500	ns

(1) The signal applied to the USART0 receive signal/terminal (URXD0) should meet the timing requirements of $t_{(\tau)}$ to ensure that the URXS flip-flop is set. The URXS flip-flop is set with negative pulses meeting the minimum-timing condition of $t_{(\tau)}$. The operating conditions to set the flag must be met independently from this timing constraint. The deglitch circuitry is active only on negative transitions on the URXD0 line.

5.33 Timer_A3

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A3 clock frequency	SMCLK, Duty cycle = 50% ±10%			f_{SYSTEM}		MHz
$t_{TA,cap}$	Timer_A3, capture timing	TA0, TA1	3 V	20			ns

5.34 Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and erase supply voltage			2.2		3.6	V
f_{FTG}	Flash timing generator frequency			257		476	kHz
I_{PGM}	Supply current from V_{CC} during program		2.2 V, 3.6 V		1	5	mA
I_{ERASE}	Supply current from V_{CC} during erase		2.2 V, 3.6 V		1	7	mA
t_{CPT}	Cumulative program time (1)		2.2 V, 3.6 V			10	ms
$t_{CMErase}$	Cumulative mass erase time		2.2 V, 3.6 V	20			ms
	Program and erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	See (2)			30		t_{FTG}
$t_{Block, 0}$	Block program time for first byte or word	See (2)			25		t_{FTG}
$t_{Block, 1-63}$	Block program time for each additional byte or word	See (2)			18		t_{FTG}
$t_{Block, End}$	Block program end-sequence wait time	See (2)			6		t_{FTG}
$t_{Mass\ Erase}$	Mass erase time	See (2)			10593		t_{FTG}
$t_{Seg\ Erase}$	Segment erase time	See (2)			4819		t_{FTG}

(1) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
(2) These values are hardwired into the state machine of the flash controller (t_{FTG} = 1 / f_{FTG}).

5.35 RAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{(RAMh)}$	RAM retention supply voltage (1)	CPU halted	1.6		V

(1) This parameter defines the minimum supply voltage V_{CC} when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

5.36 JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency	3 V	0		20	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse duration	3 V	0.025		15	µs
$t_{SBW,En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge(1))	3 V			1	µs
$t_{SBW,Ret}$	Spy-Bi-Wire return to normal operation time	3 V	15		100	µs
f_{TCK}	TCK input frequency(2)	3 V	0		10	MHz
$R_{Internal}$	Internal pulldown resistance on TEST	3 V	25	60	90	kΩ

(1) Tools accessing the Spy-Bi-Wire interface must wait for the maximum $t_{SBW,En}$ time after pulling the TEST/SBWCLK pin high before applying the first SBWCLK clock edge.
(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

5.37 JTAG Fuse(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C	2.5		V
V_{FB}	Voltage level on TEST for fuse blow		6	7	V
I_{FB}	Supply current into TEST during fuse blow			100	mA
t_{FB}	Time to blow fuse			1	ms

(1) Afterthe fuse is blown, no further access to the JTAG Test, Spy-Bi-Wire, or emulation features is possible, and JTAG is switched to bypass mode.

6 Detailed Description

6.1 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock. Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers (see Figure 6-1).

Peripherals are connected to the CPU using data, address, and control buses and can be handled with all instructions.

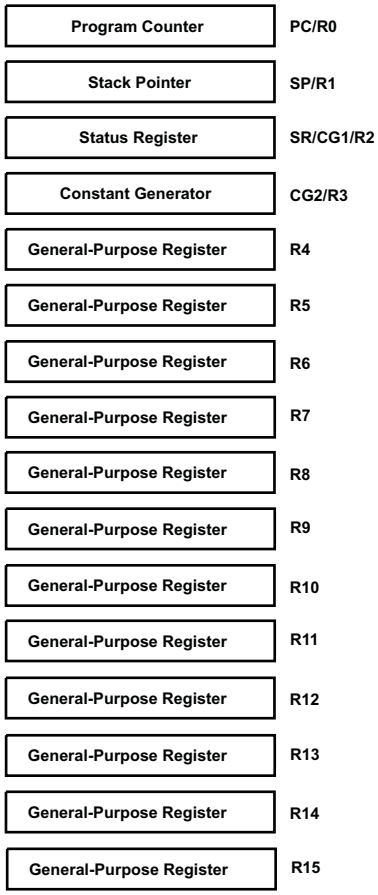


Figure 6-1. CPU Registers

6.2 Instruction Set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 6-1 lists examples of the three types of instruction formats. Table 6-2 lists the address modes.

Table 6-1. Instruction Word Formats

INSTRUCTION FORMAT	EXAMPLE	OPERATION
Dual operands, source-destination	ADD R4,R5	R4 + R5 → R5
Single operands, destination only	CALL R8	PC → (TOS), R8 → PC
Relative jump, unconditional or conditional	JNE	Jump-on-equal bit = 0

Table 6-2. Address Mode Descriptions

ADDRESS MODE	S(1)	D(2)	SYNTAX	EXAMPLE	OPERATION
Register	✓	✓	MOV Rs,Rd	MOV R10,R11	R10 → R11
Indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5) → M(6+R6)
Symbolic (PC relative)	✓	✓	MOV EDE,TONI		M(EDE) → M(TONI)
Absolute	✓	✓	MOV &MEM,&TCDAT		M(MEM) → M(TCDAT)
Indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) → M(Tab+R6)
Indirect autoincrement	✓		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) → R11 R10 + 2 → R10
Immediate	✓		MOV #X,TONI	MOV #45,TONI	#45 → M(TONI)

(1) S = source
(2) D = destination

6.3 Operating Modes

These microcontrollers have one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

Software can configure the following operating modes:

- Active mode (AM)
  - All clocks are active.
- Low-power mode 0 (LPM0)
  - CPU is disabled.
  - ACLK and SMCLK remain active. MCLK is disabled.
- Low-power mode 1 (LPM1)
  - CPU is disabled ACLK and SMCLK remain active. MCLK is disabled.
  - DC generator of the DCO is disabled if DCO not used in active mode.
- Low-power mode 2 (LPM2)
  - CPU is disabled.
  - MCLK and SMCLK are disabled.
  - DC generator of the DCO remains enabled.
  - ACLK remains active.
- Low-power mode 3 (LPM3)
  - CPU is disabled.
  - MCLK and SMCLK are disabled.
  - DC generator of the DCO is disabled.
  - ACLK remains active.
- Low-power mode 4 (LPM4)
  - CPU is disabled.
  - ACLK is disabled.
  - MCLK and SMCLK are disabled.
  - DC generator of the DCO is disabled.
  - Crystal oscillator is stopped.

6.4 Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are in the address range of 0FFFFh to 0FFE0h (see Table 6-3). The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (at address 0FFFEh) contains 0FFFFh (for example, if flash is not programmed), the CPU goes into LPM4 immediately after power up.

Table 6-3. Interrupt Vector Addresses

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power up External reset Watchdog Flash key violation PC out-of-range(1)	PORIFG RSTIFG WDTIFG KEYV (2)	Reset	0FFFEh	15, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG (2) (3)	(Non)maskable, (Non)maskable, (Non)maskable	0FFFCh	14
			0FFFAh	13
SD24_A	SD24CCTLx SD24OVIFG, SD24CCTLx SD24IFG(2) (4)	Maskable	0FFF8h	12
			0FFF6h	11
Watchdog Timer	WDTIFG	Maskable	0FFF4h	10
USART0 Receive	URXIFG0	Maskable	0FFF2h	9
USART0 Transmit	UTXIFG0	Maskable	0FFF0h	8
			0FFEEh	7
Timer_A3	TA0CCR0 CCIFG(4)	Maskable	0FFECh	6
Timer_A3	TA0CCR1 CCIFG, TA0CCR2 CCIFG, TA0CTL TAIFG (2) (4)	Maskable	0FFEAh	5
I/O Port P1 (eight flags)	P1IFG.0 to P1IFG.7(2) (4)	Maskable	0FFE8h	4
			0FFE6h	3
			0FFE4h	2
I/O Port P2 (three flags)	P2IFG.0 to P2IFG.2(2) (4)	Maskable	0FFE2h	1
			0FFE0h	0, lowest

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address range.
(2) Multiple source flags
(3) (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.
(4) Interrupt flags are in the module.

6.5 Special Function Registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

Legend

rw	Bit can be read and written.
rw-0, rw-1	Bit can be read and written. It is reset or set by PUC.
rw-(0), rw-(1)	Bit can be read and written. It is reset or set by POR.
	SFR bit is not present in device.

Figure 6-2. Interrupt Enable Register 1 (Address 00h)

7	6	5	4	3	2	1	0
UTXIE0	URXIE0	ACCVIE	NMIIE			OFIE	WDTIE
rw-0	rw-0	rw-0	rw-0			rw-0	rw-0

Table 6-4. Interrupt Enable Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	UTXIE0	RW	0h	USART0: UART and SPI transmit interrupt enable
6	URXIE0	RW	0h	USART0: UART and SPI receive interrupt enable
5	ACCVIE	RW	0h	Flash access violation interrupt enable
4	NMIIE	RW	0h	(Non)maskable interrupt enable
3-2	Unused			
1	OFIE	RW	0h	Oscillator fault interrupt enable
0	WDTIE	RW	0h	Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode.

Figure 6-3. Interrupt Enable Register 2 (Address 01h)

7	6	5	4	3	2	1	0

Figure 6-4. Interrupt Flag Register 1 (Address 02h)

7	6	5	4	3	2	1	0
UTXIFG0	URXIFG0		NMIIFG	RSTIFG	PORIFG	OFIFG	WDTIFG
rw-1	rw-0		rw-0	rw-(0)	rw-(1)	rw-1	rw-(0)

Table 6-5. Interrupt Flag Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	UTXIFG0	RW	1h	USART0: UART and SPI transmit interrupt flag
6	URXIFG0	RW	0h	USART0: UART and SPI receive interrupt flag
5	Unused			
4	NMIIFG	RW	0h	Set by $\overline{\text{RST}}$/NMI pin
3	RSTIFG	RW	0h	Power-on reset interrupt flag. Set on V_{CC} power up.
2	PORIFG	RW	1h	External reset interrupt flag. Set on a reset condition at $\overline{\text{RST}}$/NMI pin in reset mode. Reset on V_{CC} power up.
1	OFIFG	RW	1h	Flag set on oscillator fault
0	WDTIFG	RW	0h	Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on V_{CC} power-up or a reset condition at $\overline{\text{RST}}$/NMI pin in reset mode.

Figure 6-5. Interrupt Flag Register 2 (Address 03h)

7	6	5	4	3	2	1	0

Figure 6-6. Module Enable Register 1 (Address 04h)

7	6	5	4	3	2	1	0
UTXE0	URXE0 USPIE0						
rw-0	rw-0						

Table 6-6. Module Enable Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	UTXE0	RW	0h	USART0: UART mode transmit enable
6	URXE0 USPIE0	RW	0h	USART0: UART mode receive enable USART0: SPI mode transmit and receive enable
5-0	Unused			

Figure 6-7. Module Enable Register 2 (Address 05h)

7	6	5	4	3	2	1	0

6.6 Memory Organization

Table 6-7 summarizes the memory map of all device variants.

Table 6-7. Memory Organization

		MSP430AFE22x	MSP430AFE23x	MSP430AFE25x
Memory Main: interrupt vector Main: code memory	Size Flash Flash	4KB FFFFh to FFE0h FFFFh to F000h	8KB FFFFh to FFE0h FFFFh to E000h	16KB FFFFh to FFE0h FFFFh to C000h
Information memory	Size Flash	256 Byte 10FFhh to 1000h	256 Byte 10FFhh to 1000h	256 Byte 10FFhh to 1000h
RAM	Size	256 bytes 02FFh to 0200h	512 bytes 03FFh to 0200h	512 bytes 03FFh to 0200h
Peripherals	16-bit 8-bit 8-bit SFR	01FFh to 0100h 00FFh to 0010h 000Fh to 0000h	01FFh to 0100h 00FFh to 0010h 000Fh to 0000h	01FFh to 0100h 00FFh to 0010h 000Fh to 0000h

6.7 Flash Memory

The flash memory can be programmed through the Spy-Bi-Wire or JTAG port or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has *n* segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to *n* may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to *n*.
  Segments A to D are also called *information memory*.
- Segment A contains calibration data. After reset, segment A is protected against programming and erasing. It can be unlocked, but do not erase this segment if the device-specific calibration data is required.

6.8 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. Peripherals can be managed using all instructions. For complete module descriptions, see the *MSP430x2xx Family User's Guide*.

6.9 Oscillator and System Clock

The clock system is supported by the Basic Clock module that includes support for an internal digitally controlled oscillator (DCO), a high-frequency crystal oscillator, and an internal very-low-power low-frequency oscillator (VLO). The clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turnon clock source and stabilizes in less than 1 µs. The clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from the VLO
- Main clock (MCLK), the system clock used by the CPU
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules

Table 6-8 lists the addresses of the available DCO calibration data.

Table 6-8. DCO Calibration Data (Provided From Factory in Flash Information Memory Segment A)

DCO FREQUENCY	CALIBRATION REGISTER	SIZE	ADDRESS
8 MHz	CALBC1_8MHZ	byte	010FDh
	CALDCO_8MHZ	byte	010FCh
12 MHz	CALBC1_12MHZ	byte	010FBh
	CALDCO_12MHZ	byte	010FAh

6.10 Brownout, Supply Voltage Supervisor

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off. The supply voltage supervisor (SVS) circuitry detects if supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM) (the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However, V_{CC} may not have ramped to $V_{CC(min)}$ at that time. The user must make sure that the default DCO settings are not changed until V_{CC} reaches $V_{CC(min)}$. If desired, the SVS circuit can be used to determine when V_{CC} reaches $V_{CC(min)}$.

6.11 Digital I/O

Two I/O ports are implemented: 8-bit port P1 and 3-bit port P2.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition is possible.
- Edge-selectable interrupt input capability for all eight bits of port P1 and three bits of port P2.
- Read and write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup or pulldown resistor.

Because there are only three I/O pins implemented from port P2, bits [5:1] of all port P2 registers read as 0, and write data is ignored.

6.12 Watchdog Timer (WDT+)

The primary function of the WDT+ module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

6.13 Timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing (see Table 6-9). Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-9. Timer_A3 Signal Connections

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER
24-PIN PW					24-PIN PW
12 - P1.0	TACLK	TACLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
12 - P1.0	$\overline{\text{TACLK}}$	INCLK			
18 - P1.2	TA0	CCI0A	CCR0	TA0	18 - P1.2
18 - P1.2	TA0	CCI0B			24 - P2.0
	DVSS	GND			
	DVCC	VCC			
17 - P1.1	TA1	CCI1A	CCR1	TA1	17 - P1.1
17 - P1.1	TA1	CCI1B			23 - P1.7
	DVSS	GND			
	DVCC	VCC			
	DVSS	CCI2A	CCR2	TA2	12 - P1.0
	ACLK (internal)	CCI2B			22 - P1.6
	DVSS	GND			
	DVCC	VCC			

6.14 USART0

The MSP430AFE2xx devices have one hardware universal synchronous/asynchronous receive transmit (USART0) peripheral module that is used for serial data communication. The USART0 module supports synchronous SPI (3-pin or 4-pin) and asynchronous UART communication protocols, using double-buffered transmit and receive channels. The maximum operational frequency for the USART0 module is 8 MHz.

6.15 Hardware Multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs 16×16-, 16×8-, 8×16-, and 8×8-bit operations. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

6.16 SD24_A

The SD24_A module integrates up to three independent 24-bit sigma-delta ADCs. Each channel is designed with fully differential analog input pair and programmable gain amplifier input stage. In addition to external analog inputs, an internal VCC sense and temperature sensor are also available.

6.17 Peripheral File Map

Table 6-10 lists the peripheral registers with word access. Table 6-11 lists the peripheral registers with byte access. Some registers are included in both tables.

Table 6-10. Peripherals With Word Access

PERIPHERAL	REGISTER NAME	ACRONYM	ADDRESS
Timer_A3	Capture/compare register 2	TACCR2	0176h
	Capture/compare register 1	TACCR1	0174h
	Capture/compare register 0	TACCR0	0172h
	Timer_A register	TAR	0170h
	Capture/compare control 2	TACCTL2	0166h
	Capture/compare control 1	TACCTL1	0164h
	Capture/compare control 0	TACCTL0	0162h
	Timer_A control	TACTL	0160h
	Timer_A interrupt vector	TAIV	012Eh
Hardware Multiplier	Sum extend	SUMEXT	013Eh
	Result high word	RESHI	013Ch
	Result low word	RESLO	013Ah
	Second operand	OP2	0138h
	Multiply signed + accumulate/operand 1	MACS	0136h
	Multiply + accumulate/operand 1	MAC	0134h
	Multiply signed/operand 1	MPYS	0132h
	Multiply unsigned/operand 1	MPY	0130h
Flash Memory	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
Watchdog Timer+	Watchdog/timer control	WDTCTL	0120h
SD24_A (also see Table 6-11)	General Control	SD24CTL	0100h
	Channel 0 Control	SD24CCTL0	0102h
	Channel 1Control	SD24CCTL1	0104h
	Channel 2 Control	SD24CCTL2	0106h
	Channel 0 conversion memory	SD24MEM0	0110h
	Channel 1 conversion memory	SD24MEM1	0112h
	Channel 2 conversion memory	SD24MEM2	0114h
	SD24 Interrupt vector word register	SD24IV	01AEh

Table 6-11. Peripherals With Byte Access

PERIPHERAL	REGISTER NAME	ACRONYM	ADDRESS
SD24_A (also see Table 6-10)	Channel 0 Input Control	SD24INCTL0	00B0h
	Channel 1 Input Control	SD24INCTL1	00B1h
	Channel 2 Input Control	SD24INCTL2	00B2h
	Channel 0 Preload	SD24PRE0	00B8h
	Channel 1 Preload	SD24PRE1	00B9h
	Channel 2 Preload	SD24PRE2	00BAh
	Reserved (Internal SD24_A Configuration 1)	SD24CONF1	00BFh
USART0	Transmit buffer	U0TXBUF	0077h
	Receive buffer	U0RXBUF	0076h
	Baud rate	U0BR1	0075h
	Baud rate	U0BR0	0074h
	Modulation control	U0MCTL	0073h
	Receive control	U0RCTL	0072h
	Transmit control	U0TCTL	0071h
	USART control	U0CTL	0070h
Basic Clock System+	Basic clock system control 3	BCSCTL3	0053h
	Basic clock system control 2	BCSCTL2	0058h
	Basic clock system control 1	BCSCTL1	0057h
	DCO clock frequency control	DCOCTL	0056h
Brownout, SVS	SVS control register (reset by brownout signal)	SVSCTL	0055h
Port P2	Port P2 selection 2	P2SEL2	0042h
	Port P2 resistor enable	P2REN	002Fh
	Port P2 selection	P2SEL	002Eh
	Port P2 interrupt enable	P2IE	002Dh
	Port P2 interrupt edge select	P2IES	002Ch
	Port P2 interrupt flag	P2IFG	002Bh
	Port P2 direction	P2DIR	002Ah
	Port P2 output	P2OUT	0029h
	Port P2 input	P2IN	0028h
Port P1	Port P1 selection 2 register	P1SEL2	0041h
	Port P1 resistor enable	P1REN	0027h
	Port P1 selection	P1SEL	0026h
	Port P1 interrupt enable	P1IE	0025h
	Port P1 interrupt edge select	P1IES	0024h
	Port P1 interrupt flag	P1IFG	0023h
	Port P1 direction	P1DIR	0022h
	Port P1 output	P1OUT	0021h
	Port P1 input	P1IN	0020h
Special Function	SFR module enable 2	ME2	0005h
	SFR module enable 1	ME1	0004h
	SFR interrupt flag 2	IFG2	0003h
	SFR interrupt flag 1	IFG1	0002h
	SFR interrupt enable 2	IE2	0001h
	SFR interrupt enable 1	IE1	0000h

6.18 I/O Port Schematics

6.18.1 Port P1 Pin Schematic: P1.0 Input/Output With Schmitt Trigger

Figure 6-8 shows the port schematic. Table 6-12 summarizes the selection of the pin functions.

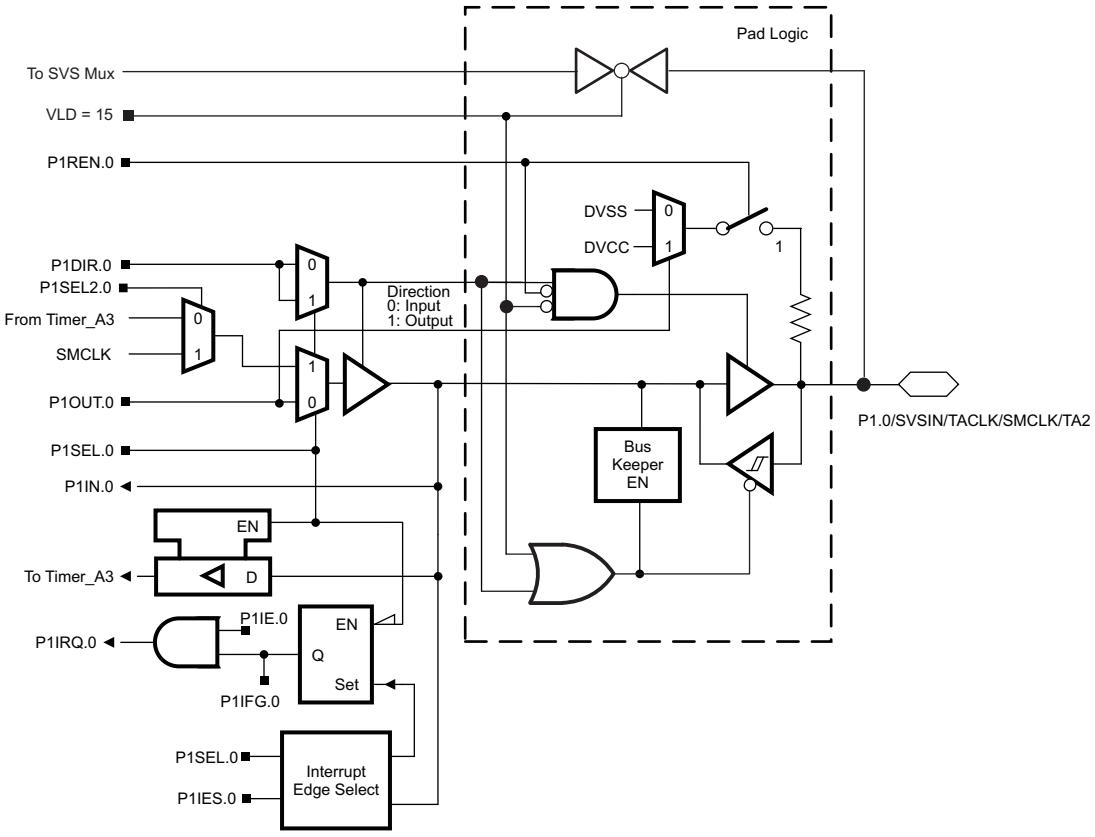


Figure 6-8. Port P1 (P1.0) Schematic

Table 6-12. Port P1 (P1.0) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P1DIR.x	P1SEL.x	P1SEL2.x
P1.0/SVSIN/TACLK/SMCLK/TA2	0	P1.0 (I/O)	I: 0, O: 1	0	X
		SVSIN (VLD = 15)	X	X	X
		Timer_A3.TACLK	0	1	0
		SMCLK	1	1	1
		Timer_A3.TA2	1	1	0

(1) X = don't care

6.18.2 Port P1 Pin Schematic: P1.1 and P1.2 Input/Output With Schmitt Trigger

Figure 6-9 shows the port schematic. Table 6-13 summarizes the selection of the pin functions.

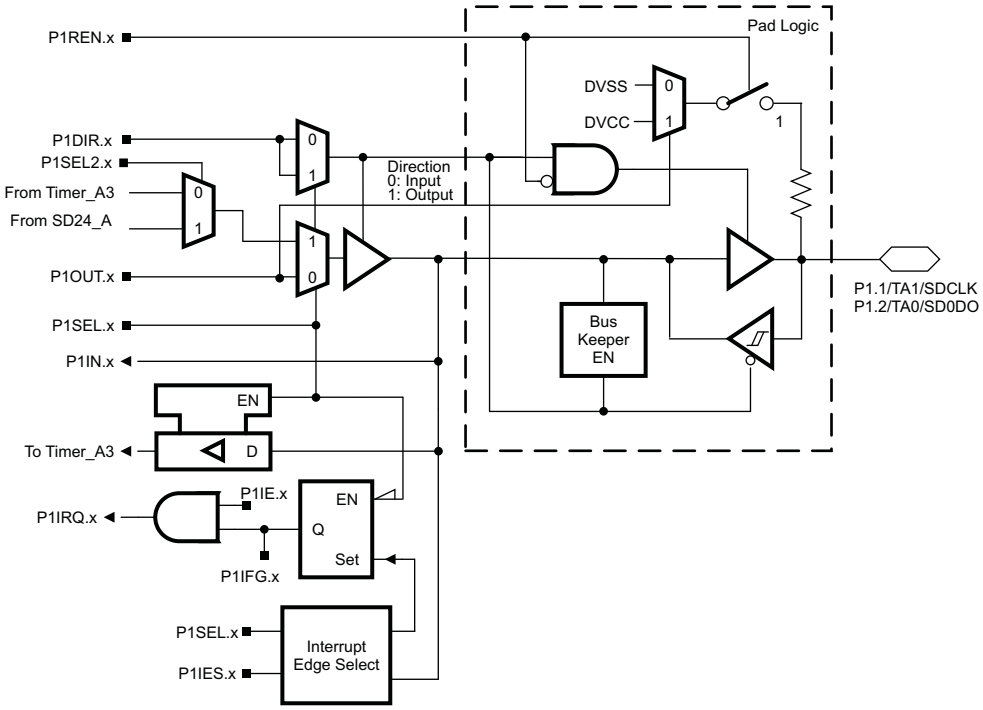


Figure 6-9. Port P1 (P1.1 and P1.2) Schematic

Table 6-13. Port P1 (P1.1 and P1.2) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS / SIGNAL(1)		
			P1DIR.x	P1SEL.x	P1SEL2.x
P1.1/TA1/SDCLK	1	P1.1 (I/O)	I: 0, O: 1	0	X
		Timer_A3.CCI1A and CCI1B	0	1	0
		Timer_A3.TA1	1	1	0
		SDCLK	1	1	1
P1.2/TA0/SD0DO	2	P1.2 (I/O)	I: 0, O: 1	0	X
		Timer_A3.CCI0A and CCI0B	0	1	0
		Timer_A3.TA0	1	1	0
		SD0DO	1	1	1

(1) X = don't care

6.18.3 Port P1 Pin Schematic: P1.3 Input/Output With Schmitt Trigger

Figure 6-10 shows the port schematic. Table 6-14 summarizes the selection of the pin functions.

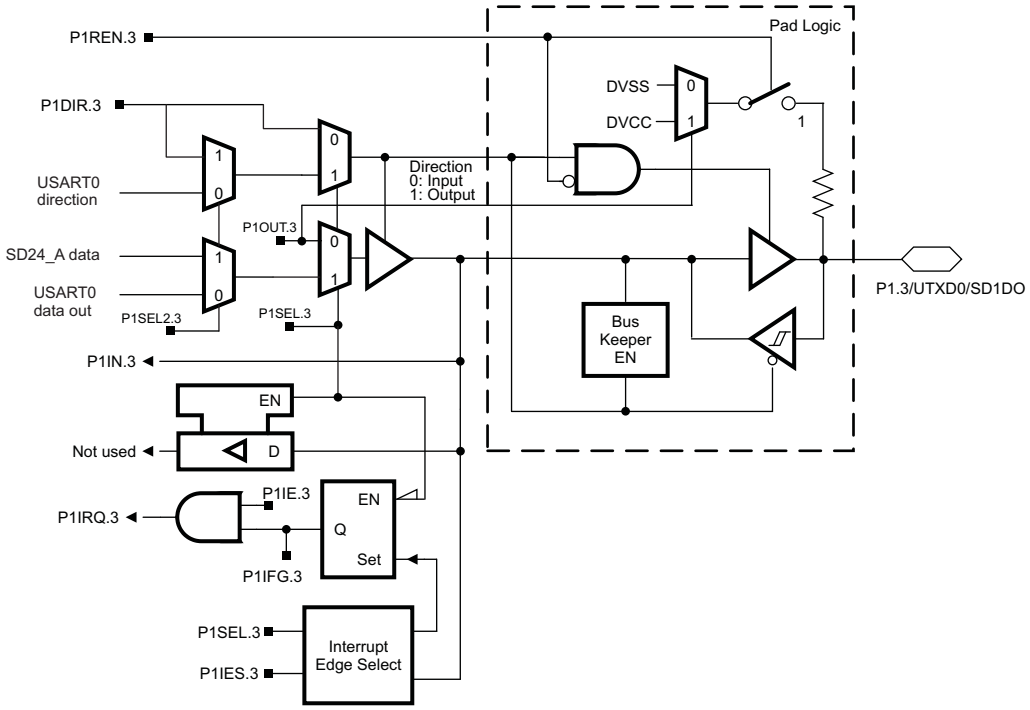


Figure 6-10. Port P1 (P1.3) Schematic

Table 6-14. Port P1 (P1.3) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P1DIR.x	P1SEL.x	P1SEL2.x
P1.3/UTXD0/SD1DO	3	P1.3 (I/O)	I: 0, O: 1	0	X
		UTXD0	X	1	0
		SD1DO	1	1	1

(1) X = don't care

6.18.4 Port P1 Pin Schematic: P1.4 Input/Output With Schmitt Trigger

Figure 6-11 shows the port schematic. Table 6-15 summarizes the selection of the pin functions.

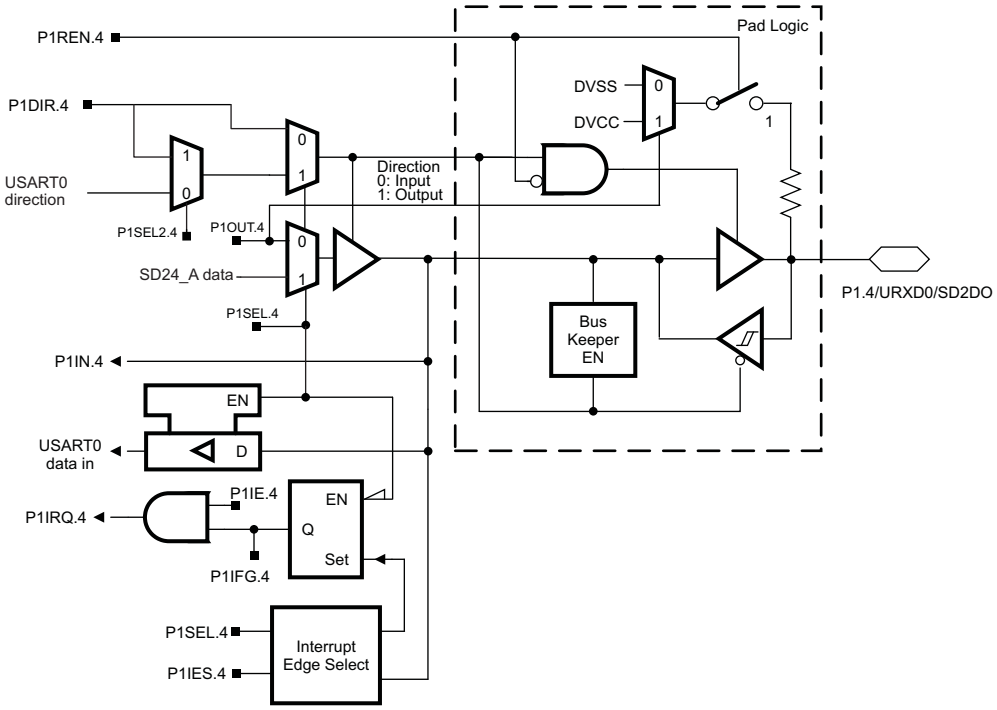


Figure 6-11. Port P1 (P1.4) Schematic

Table 6-15. Port P1 (P1.4) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P1DIR.x	P1SEL.x	P1SEL2.x
P1.4/URXD0/SD2DO	4	P1.4 (I/O)	I: 0, O: 1	0	X
		URXD0	X	1	0
		SD2DO	1	1	1

(1) X = don't care

6.18.5 Port P1 Pin Schematic: P1.5 to P1.7 Input/Output With Schmitt Trigger

Figure 6-12 shows the port schematic. Table 6-16 summarizes the selection of the pin functions.

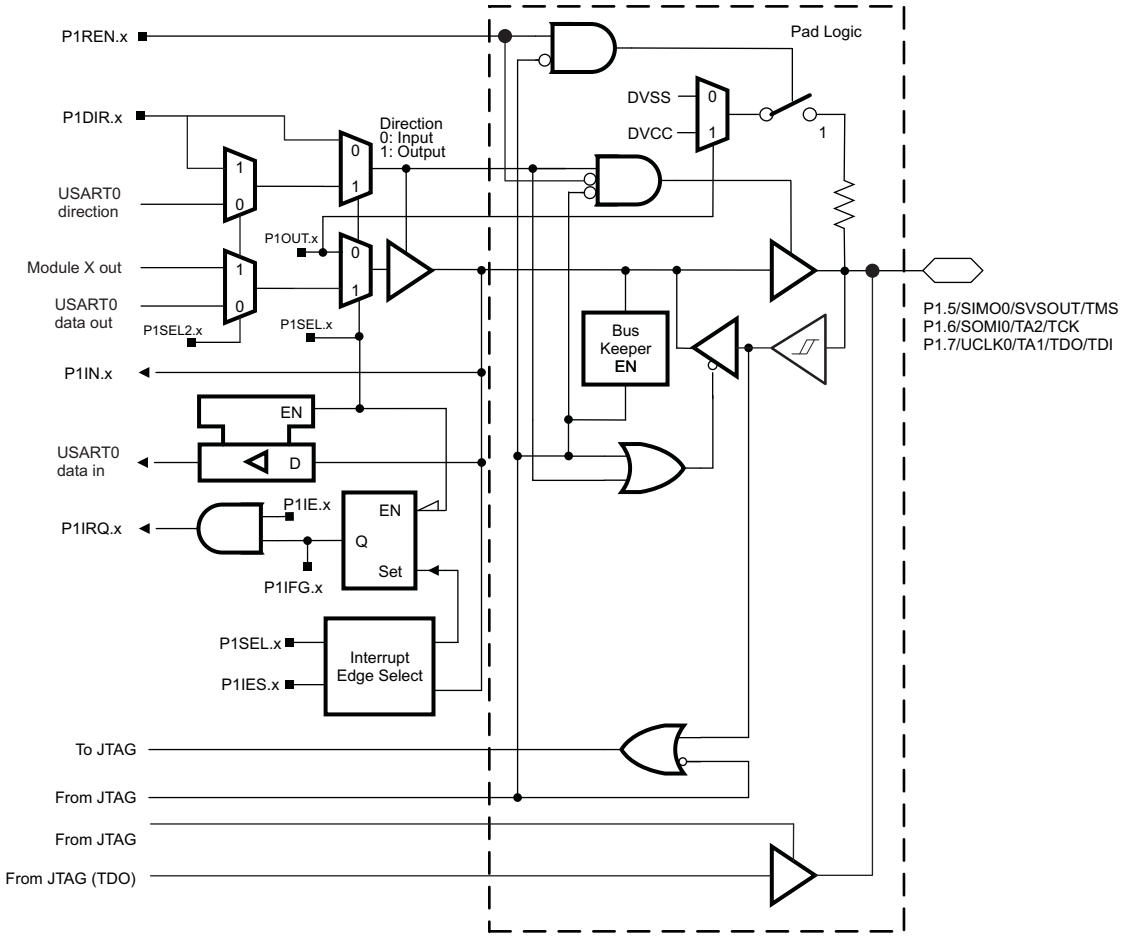


Figure 6-12. Port P1 (P1.5 to P1.7) Schematic

Table 6-16. Port P1 (P1.5 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P1DIR.x	P1SEL.x	P1SEL2.x	JTAG Mode(2)
P1.5/SIMO0/SVSOUT/TMS	5	P1.5 (I/O)	I: 0; O: 1	0	X	0
		SIMO0	X	1	0	0
		SVSOUT	1	1	1	0
		TMS	X	X	X	1
P1.6/SOMI0/TA2/TCK	6	P1.6 (I/O)	I: 0; O: 1	0	X	0
		SOMI0	X	1	0	0
		Timer_A3.TA2	1	1	1	0
		TCK	X	X	X	1
P1.7/UCLK0/TA1/TDO/TDI	7	P1.7 (I/O)	I: 0; O: 1	0	X	0
		UCLK0	X	1	0	0
		Timer_A3.TA1	1	1	1	0
		TDO/TDI	X	X	X	1

(1) X = don't care
(2) JTAG Mode is not a register bit but signal generated internally when the 4-wire JTAG option is selected in the IDE.

6.18.6 Port P2 Pin Schematic: P2.0 Input/Output With Schmitt Trigger

Figure 6-13 shows the port schematic. Table 6-17 summarizes the selection of the pin functions.

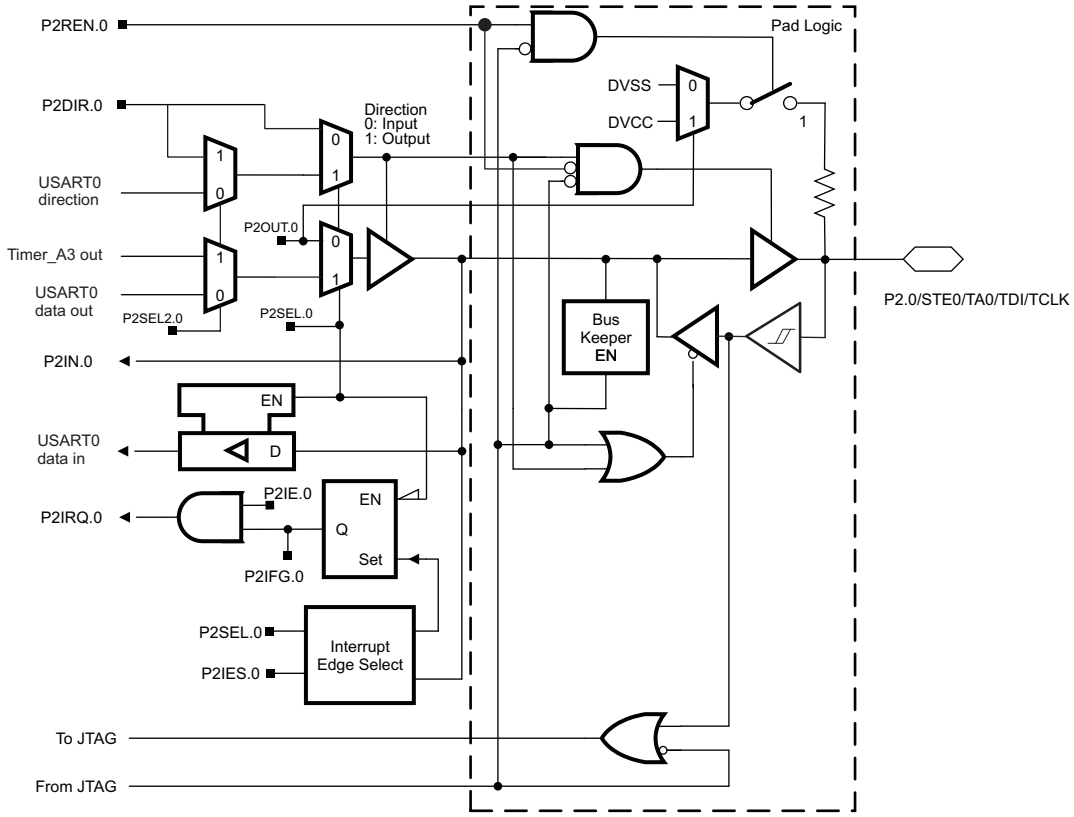


Figure 6-13. Port P2 (P2.0) Schematic

Table 6-17. Port P2 (P2.0) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P2DIR.x	P2SEL.x	P2SEL2.x	JTAG Mode(2)
P2.0/STE0/TA0/TDI/TCLK	0	P2.0 (I/O)	I: 0; O: 1	0	X	0
		STE0	X	1	0	0
		Timer_A3.TA0	1	1	1	0
		TDI/TCLK	X	X	X	1

(1) X = don't care
(2) JTAG Mode is not a register bit but signal generated internally when the 4-wire JTAG option is selected in the IDE.

6.18.7 Port P2 Pin Schematic: P2.6, Input/Output With Schmitt Trigger

Figure 6-14 shows the port schematic. Table 6-18 summarizes the selection of the pin functions.

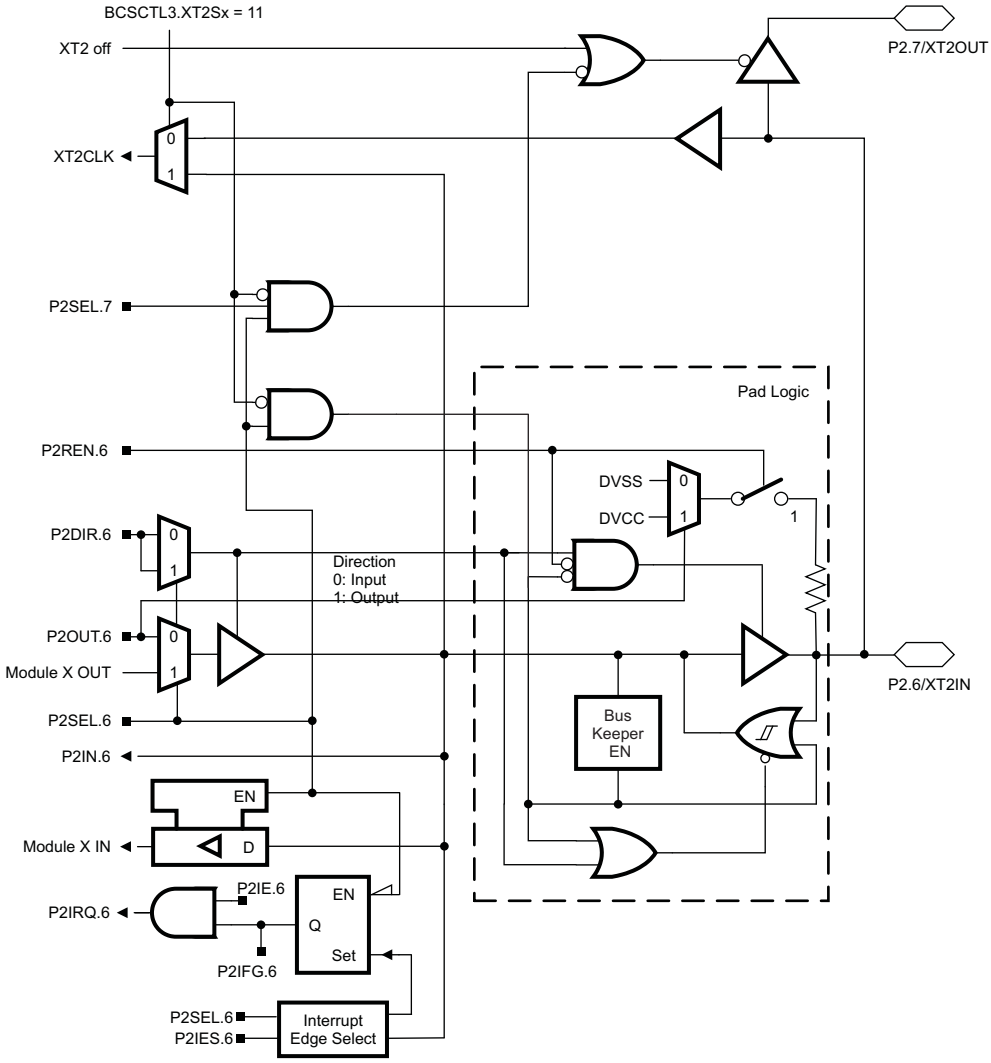


Figure 6-14. Port P2 (P2.6) Schematic

Table 6-18. Port P2 (P2.6) Pin Functions

Pin Name (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS	
			P2DIR.6	P2SEL.6
P2.6/XT2IN	6	P2.6 (I/O)	I: 0; O: 1	0
		XT2IN (default)	0	1

6.18.8 Port P2 Pin Schematic: P2.7, Input/Output With Schmitt Trigger

Figure 6-15 shows the port schematic. Table 6-19 summarizes the selection of the pin functions.

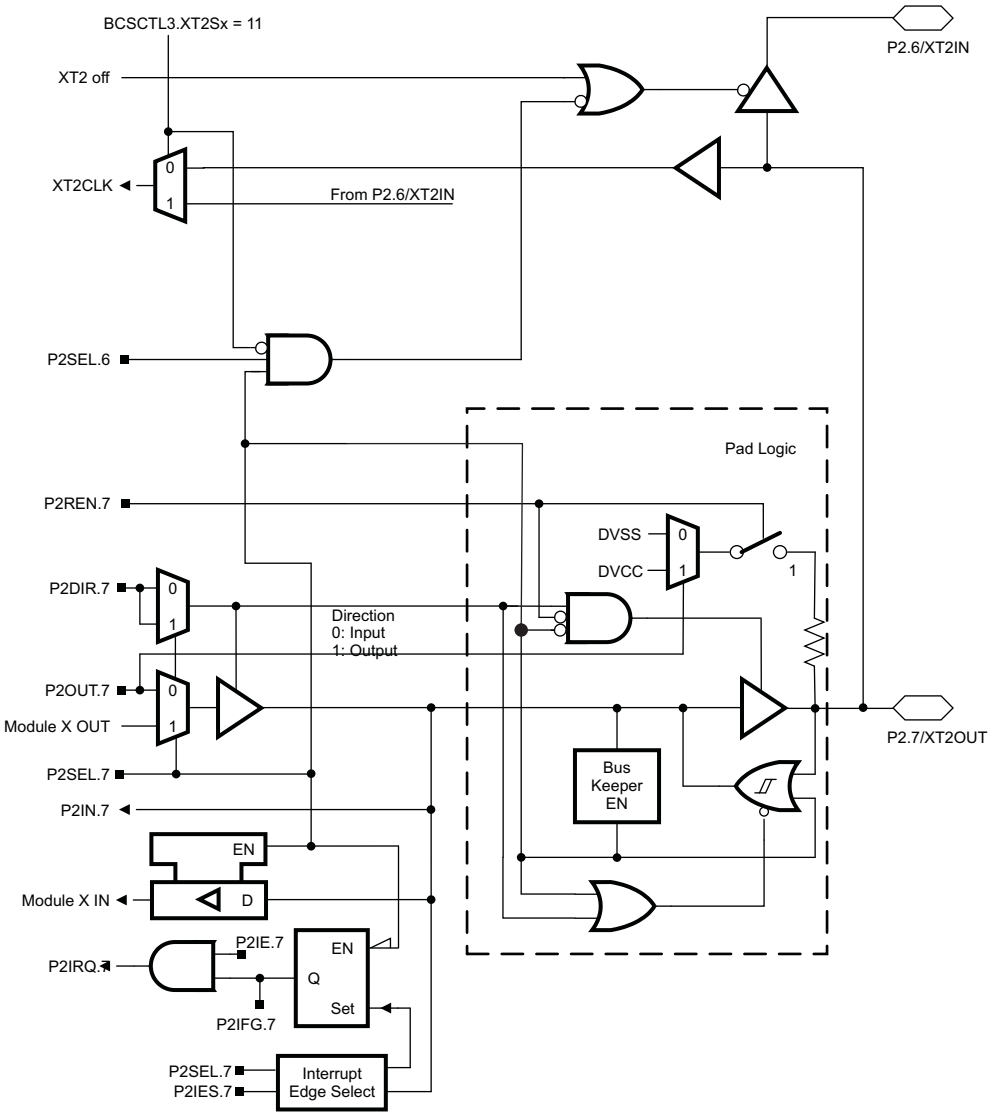


Figure 6-15. Port P2 (P2.7) Schematic

Table 6-19. Port P2 (P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS	
			P2DIR.7	P2SEL.7
P2.7/XT2OUT	7	P2.7 (I/O)	I: 0, O: 1	0
		XT2OUT (default)	0	1

6.18.9 JTAG Fuse Check Mode

MSP430 devices that have the fuse on the TEST terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF} , of 1 mA at 3 V or 2.5 mA at 5 V can flow from the TEST pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

When the TEST pin is again taken low after a test or programming session, the fuse check mode and sense currents are terminated.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR, the fuse check mode has the potential to be activated.

The fuse check current flow only when the fuse check mode is active and the TMS pin is in a low state (see Figure 6-16). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

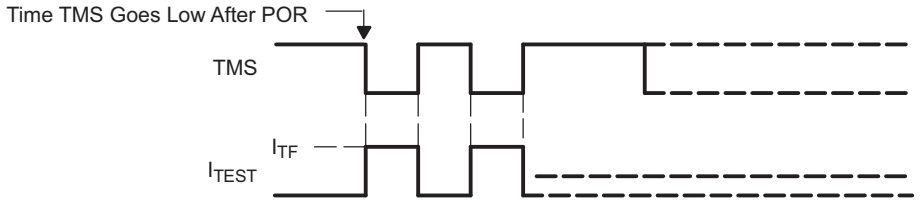


Figure 6-16. Fuse Check Mode Current

NOTE

The CODE and RAM data protection is ensured if the JTAG fuse is blown.

7 器件和文档支持

7.1 使用入门

要获得 MSP430™系列器件以及有助于开发工作的工具和库的更多信息，请访问概述页面。

7.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP430 MCU devices and support tools. Each MSP430 MCU commercial family member has one of three prefixes: MSP, PMS, or XMS (for example, MSP430F5438A). TI recommends two of three possible prefix designators for its support tools: MSP and MSPX. These prefixes represent evolutionary stages of product development from engineering prototypes (with XMS for devices and MSPX for tools) through fully qualified production devices and tools (with MSP for devices and MSP for tools).

Device development evolutionary flow:

XMS – Experimental device that is not necessarily representative of the electrical specifications for the final device

PMS – Final silicon die that conforms to the electrical specifications for the device but has not completed quality and reliability verification

MSP – Fully qualified production device

Support tool development evolutionary flow:

MSPX – Development-support product that has not yet completed TI's internal qualification testing.

MSP – Fully-qualified development-support product

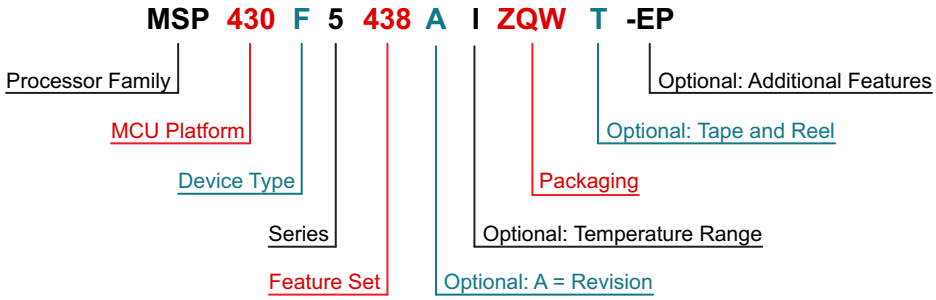
XMS and PMS devices and MSPX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices and MSP development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS and PMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PZP) and temperature range (for example, T). 图 7-1 provides a legend for reading the complete device name for any family member.



Processor Family	CC = Embedded RF Radio MSP = Mixed-Signal Processor XMS = Experimental Silicon PMS = Prototype Device	
MCU Platform	430 = MSP430 low-power microcontroller platform	
Device Type	**Memory Type** C = ROM F = Flash FR = FRAM G = Flash or FRAM (Value Line) L = No Nonvolatile Memory	**Specialized Application** AFE = Analog Front End BQ = Contactless Power CG = ROM Medical FE = Flash Energy Meter FG = Flash Medical FW = Flash Electronic Flow Meter
Series	1 = Up to 8 MHz 2 = Up to 16 MHz 3 = Legacy 4 = Up to 16 MHz with LCD	5 = Up to 25 MHz 6 = Up to 25 MHz with LCD 0 = Low-Voltage Series
Feature Set	Various levels of integration within a series	
Optional: A = Revision	N/A	
Optional: Temperature Range	S = 0°C to 50°C C = 0°C to 70°C I = –40°C to 85°C T = –40°C to 105°C	
Packaging	http://www.ti.com/packaging	
Optional: Tape and Reel	T = Small reel R = Large reel No markings = Tube or tray	
Optional: Additional Features	-EP = Enhanced Product (–40°C to 105°C) -HT = Extreme Temperature Parts (–55°C to 150°C) -Q1 = Automotive Q100 Qualified	

图 **7-1. Device Nomenclature**

7.3 工具与软件

所有 MSP 微控制器均受多种软件和硬件开发工具的支持。相关工具由 TI 以及多家第三方供应商提供。可从低功耗 MCU 开发套件和软件获取全部信息。

表 7-1 列出 了 MSP430AFE2xx MCU 的调试功能。关于可用特性的详细信息，请参见《*适用于 MSP430 的 Code Composer Studio 用户指南*》。

表 7-1. 硬件调试 特性

MSP430 架构	4 线 JTAG	2 线 JTAG	断点 (N)	范围断点	时钟控制	状态序列发生器	跟踪缓冲器
MSP430	有	有	2	否	是	否	否

设计套件与评估模块

MSP-TS430PW24 - 适用于 MSP430AFEx MCU 的 24 引脚目标开发板 MSP-TS430PW24 是一款独立的 ZIF 插座目标板，用于通过 JTAG 接口或 Spy-Bi-Wire（双线制 JTAG）协议对 MSP430 MCU 系统内置器件进行编程和调试。

MSP430AFE253 嵌入式计量（分项计量表）EVM 该嵌入式计量（分项计量表/电表）EVM 基于 MSP430AFE253 而设计。该 EVM 可直接连接至市电（或直流电源）和负载。该 EVM 会测量负载的电气参数且测量结果可从 UART 端口处读取。该 EVM 配备了内置电源和独立的串行连接，方便用户快速开始在嵌入式计量应用中评估 MSP430AFE253。

软件

MSP430Ware™ 软件 MSP430Ware 软件集合了所有 MSP430 器件的代码示例、数据表以及其他设计资源，打包提供给用户。除了提供已有 MSP430 MCU 设计资源的完整集合外，MSP430Ware 软件还包含名为 MSP 驱动程序库的高级 API。借助该库可以轻松地对 MSP430 硬件进行编程。MSP430Ware 软件以 CCS 组件或独立软件包两种形式提供。

MSP430AFE2x3、MSP430AFE2x2、MSP430AFE2x1 代码示例 根据不同应用需求配置各集成外设的每个 MSP 器件均具备相应的 C 代码示例。

适用于 MSP 的定点数学库 TI MSP IQmath 和 Qmath 库是为 C 语言开发者提供的一套经过高度优化的高精度数学运算函数集合，能够将浮点算法无缝嵌入 MSP430 和 MSP432 器件的定点代码中。这些例程通常用于计算密集的实时 应用， 而优化的执行速度、高精度以及超低能耗通常是影响这些实时应用的关键因素。与使用浮点数学算法编写的同等代码相比，使用 IQmath 和 Qmath 库可以大幅提高执行速度并显著降低能耗。

适用于 MSP 微控制器的数字信号处理 (DSP) 库 该数字信号处理库是一组经高度优化的函数，可针对 MSP430 微控制器对定点数字执行许多常见的信号处理操作。这种功能集通常 用于 要求完成实时密集处理转换，从而以最低能耗实现高精度的应用。该库可针对定点数学对 MSP 系列固有硬件进行最佳利用，从而极大地提高性能。

开发工具

适用于 MSP 微控制器的 Code Composer Studio™ 集成开发环境 Code Composer Studio (CCS) 是一种集成开发环境 (IDE)，支持所有 MSP 微控制器器件。CCS 包含一整套用于开发和调试嵌入式应用。CCS 包含了优化的 C/C++ 编译器、源代码编辑器、项目构建环境、调试器、描述器以及其他众多 功能。

MSP Flasher - 命令行编程器 MSP Flasher 是一款基于 shell 的开源接口，可使用 JTAG 或 Spy-Bi-Wire (SBW) 通信通过 FET 编程器或 eZ430 对 MSP 微控制器进行编程。MSP Flasher 可用于将二进制文件（.txt 或 .hex 文件）直接下载到 MSP 微控制器，而无需使用 IDE。

MSP MCU 编程器和调试器 MSP-FET 是一款强大的仿真开发工具（通常称为调试探针），可帮助用户在 MSP 低功耗微控制器 (MCU) 中快速开发应用。创建 MCU 软件通常需要将生成的二进制程序下载到 MSP 器件中，从而进行验证和调试。

MSP-GANG 生产编程器 MSP Gang 编程器是一款 MSP430 或 MSP432 器件编程器，可同时对多达八个完全相同的 MSP430 或 MSP432 闪存或 FRAM 器件进行编程。MSP Gang 编程器可使用标准的 RS-232 或 USB 连接与主机 PC 相连并提供灵活的编程选项，允许用户完全自定义流程。

7.4 文档支持

以下文档对 MSP430AFE2xx MCU 进行了介绍。www.ti.com.cn 网站上提供了这些文档的副本。

接收文档更新通知

要接收文档更新通知（包括芯片勘误表），请转至 ti.com.cn 上您的器件对应的产品文件夹（关于产品文件夹的链接，请参见节 7.5）。请单击右上角的“通知我”按钮。点击后，您将每周定期收到已更改的产品信息（如果有的话）。有关更改的详细信息，请查阅已修订文档的修订历史记录。

勘误

《MSP430AFE253 器件勘误表》 介绍功能规格的已知例外情况。

《MSP430AFE252 器件勘误表》 介绍功能规格的已知例外情况。

《MSP430AFE251 器件勘误表》 介绍功能规格的已知例外情况。

《MSP430AFE233 器件勘误表》 介绍功能规格的已知例外情况。

《MSP430AFE232 器件勘误表》 介绍功能规格的已知例外情况。

《MSP430AFE231 器件勘误表》 介绍功能规格的已知例外情况。

《MSP430AFE223 器件勘误表》 介绍功能规格的已知例外情况。

《MSP430AFE222 器件勘误表》 介绍功能规格的已知例外情况。

《MSP430AFE221 器件勘误表》 介绍功能规格的已知例外情况。

用户指南

《MSP430x2xx 系列用户指南》 详细介绍了该器件系列提供的模块和外设。

《使用引导加载程序 (BSL) 对 MSP430 进行编程》 MSP430 引导加载程序（bootloader，简称 BSL，以前称为 bootstrap loader）允许用户在原型设计、最终生产和投用阶段与 MSP430 微控制器中的嵌入式存储器进行通信。可编程存储器（闪存）和数据存储器 (RAM) 能够按照要求进行变更。不要将此处的引导加载程序与某些数字信号处理器 (DSP) 中将外部存储器中的程序代码（和数据）自动加载到 DSP 内部存储器的引导装载程序混为一谈。

《通过 JTAG 接口对 MSP430 进行编程》 本文档介绍了使用 JTAG 通信端口擦除、编程和验证基于 MSP430 闪存和 FRAM 的微控制器系列的存储器模块所需的功能。此外，该文档还描述了如何设定所有 MSP430 器件提供的 JTAG 访问安全熔丝。本文档介绍了使用标准 4 线 JTAG 接口和 2 线 JTAG 接口（也称为 Spy-Bi-Wire (SBW)）访问 MCU。

《MSP430 硬件工具用户指南》 本手册介绍了 TI MSP-FET430 闪存仿真工具 (FET) 的硬件。FET 是针对 MSP430 超低功耗微控制器的程序开发工具。对提供的接口类型，即并行端口接口和 USB 接口进行了说明。

应用报告

MSP430 32kHz 晶体振荡器 对于稳定的晶体振荡器，选择合适的晶振、正确的负载电路和适当的电路板布局布线至关重要。该应用报告总结了晶体振荡器的功能，介绍了为实现 MSP430 超低功耗运行而选择正确晶体的参数。此外，还给出了正确电路板布局布线的提示和示例。本文档还包含与可能振荡器测试相关的详细信息以确保大批量生产中的稳定振荡器运行。

《MSP430 系统级 ESD 注意事项》 系统级 ESD 对于低电压下的硅晶技术以及经济高效型和超低功耗组件的需求日益增加。该应用报告提出了三项不同的 ESD 主题，旨在帮助电路板设计人员和 OEM 理解并设计出稳健耐用的系统级设计。

7.5 相关链接

表 7-2 列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件以及申请样片或购买产品的快速访问链接。

表 7-2. 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
MSP430AFE253	单击此处	单击此处	单击此处	单击此处	单击此处
MSP430AFE252	单击此处	单击此处	单击此处	单击此处	单击此处
MSP430AFE251	单击此处	单击此处	单击此处	单击此处	单击此处
MSP430AFE233	单击此处	单击此处	单击此处	单击此处	单击此处
MSP430AFE232	单击此处	单击此处	单击此处	单击此处	单击此处
MSP430AFE231	单击此处	单击此处	单击此处	单击此处	单击此处
MSP430AFE223	单击此处	单击此处	单击此处	单击此处	单击此处
MSP430AFE222	单击此处	单击此处	单击此处	单击此处	单击此处
MSP430AFE221	单击此处	单击此处	单击此处	单击此处	单击此处

7.6 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参见 TI 的 《使用条款》。

TI E2E™ 社区

TI 的工程师交流 (E2E) 社区. 此社区的创建目的是为了促进工程师之间协作。在 e2e.ti.com 中，您可以提问、共享知识、拓展思路，在同领域工程师的帮助下解决问题。

TI 嵌入式处理器维基网页

德州仪器 (TI) 嵌入式处理器维基网页。此网站的建立是为了帮助开发人员熟悉德州仪器 (TI) 的嵌入式处理器，并且也为了促进与这些器件相关的硬件和软件的总体知识的创新和增长。

7.7 商标

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7.8 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.9 术语表

TI 术语表 这份术语表列出并解释术语、缩写和定义。

8 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请参阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP4301103IPWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430AFE253	Samples
MSP430AFE221IPW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430AFE221	Samples
MSP430AFE221IPWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430AFE221	Samples
MSP430AFE222IPW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430AFE222	Samples
MSP430AFE222IPWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430AFE222	Samples
MSP430AFE223IPW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430AFE223	Samples
MSP430AFE223IPWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430AFE223	Samples
MSP430AFE231IPW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430AFE231	Samples
MSP430AFE231IPWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430AFE231	Samples
MSP430AFE232IPW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430AFE232	Samples
MSP430AFE232IPWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430AFE232	Samples
MSP430AFE233IPW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430AFE233	Samples
MSP430AFE233IPWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430AFE233	Samples
MSP430AFE251IPW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430AFE251	Samples
MSP430AFE251IPWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430AFE251	Samples
MSP430AFE252IPW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430AFE252	Samples
MSP430AFE252IPWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430AFE252	Samples
MSP430AFE253IPW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430AFE253	Samples
MSP430AFE253IPWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	430AFE253	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

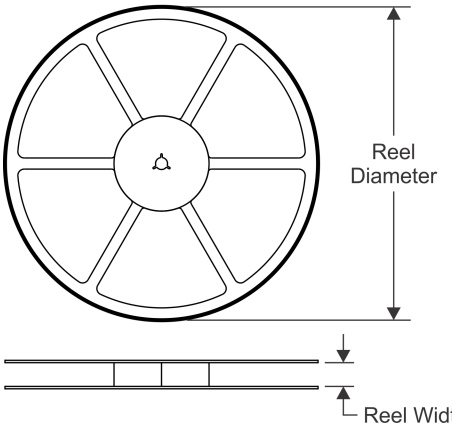
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

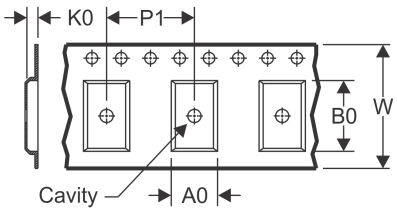
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

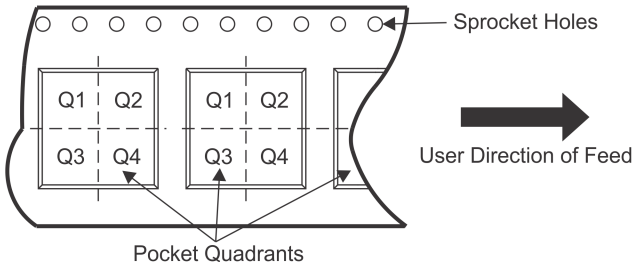


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

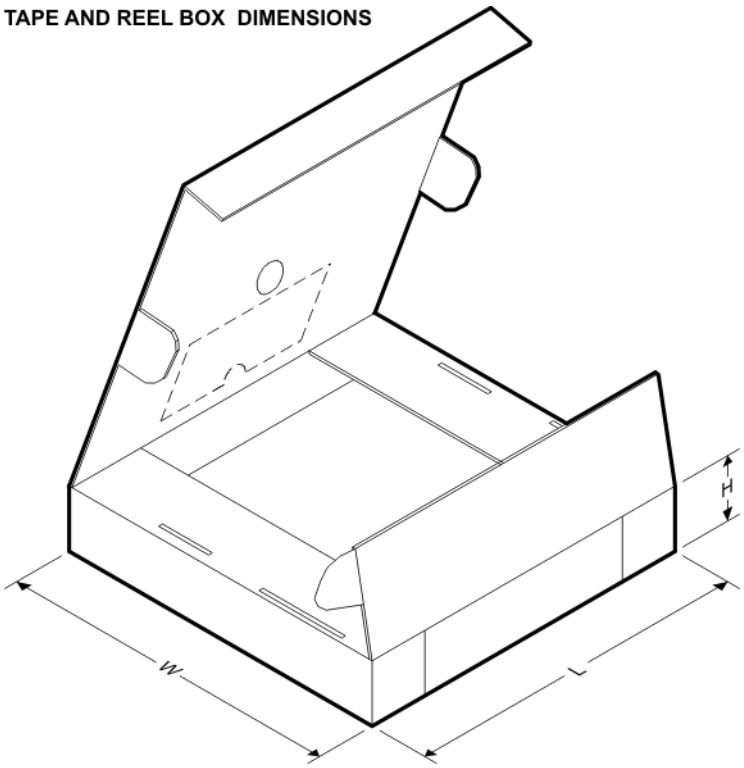
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430AFE221IPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
MSP430AFE222IPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
MSP430AFE223IPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
MSP430AFE231IPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
MSP430AFE232IPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
MSP430AFE233IPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
MSP430AFE251IPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
MSP430AFE252IPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
MSP430AFE253IPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

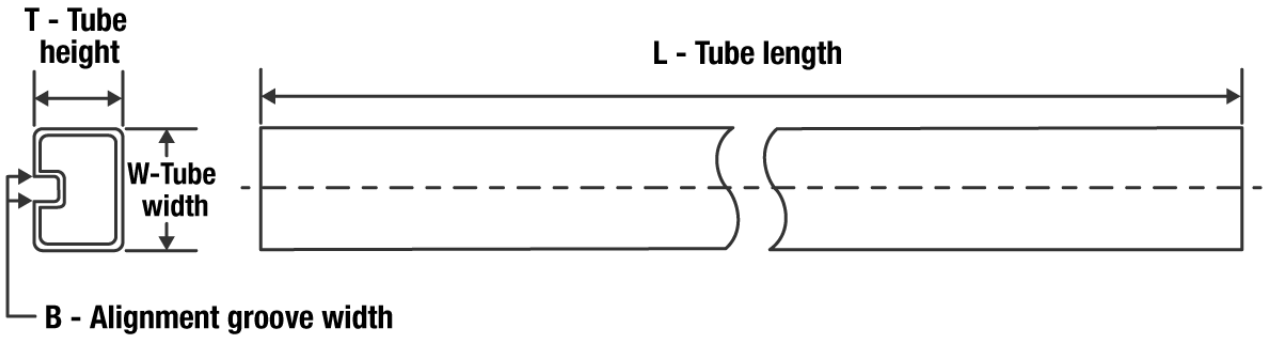
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430AFE221IPWR	TSSOP	PW	24	2000	350.0	350.0	43.0
MSP430AFE222IPWR	TSSOP	PW	24	2000	350.0	350.0	43.0
MSP430AFE223IPWR	TSSOP	PW	24	2000	350.0	350.0	43.0
MSP430AFE231IPWR	TSSOP	PW	24	2000	350.0	350.0	43.0
MSP430AFE232IPWR	TSSOP	PW	24	2000	350.0	350.0	43.0
MSP430AFE233IPWR	TSSOP	PW	24	2000	350.0	350.0	43.0
MSP430AFE251IPWR	TSSOP	PW	24	2000	350.0	350.0	43.0
MSP430AFE252IPWR	TSSOP	PW	24	2000	350.0	350.0	43.0
MSP430AFE253IPWR	TSSOP	PW	24	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

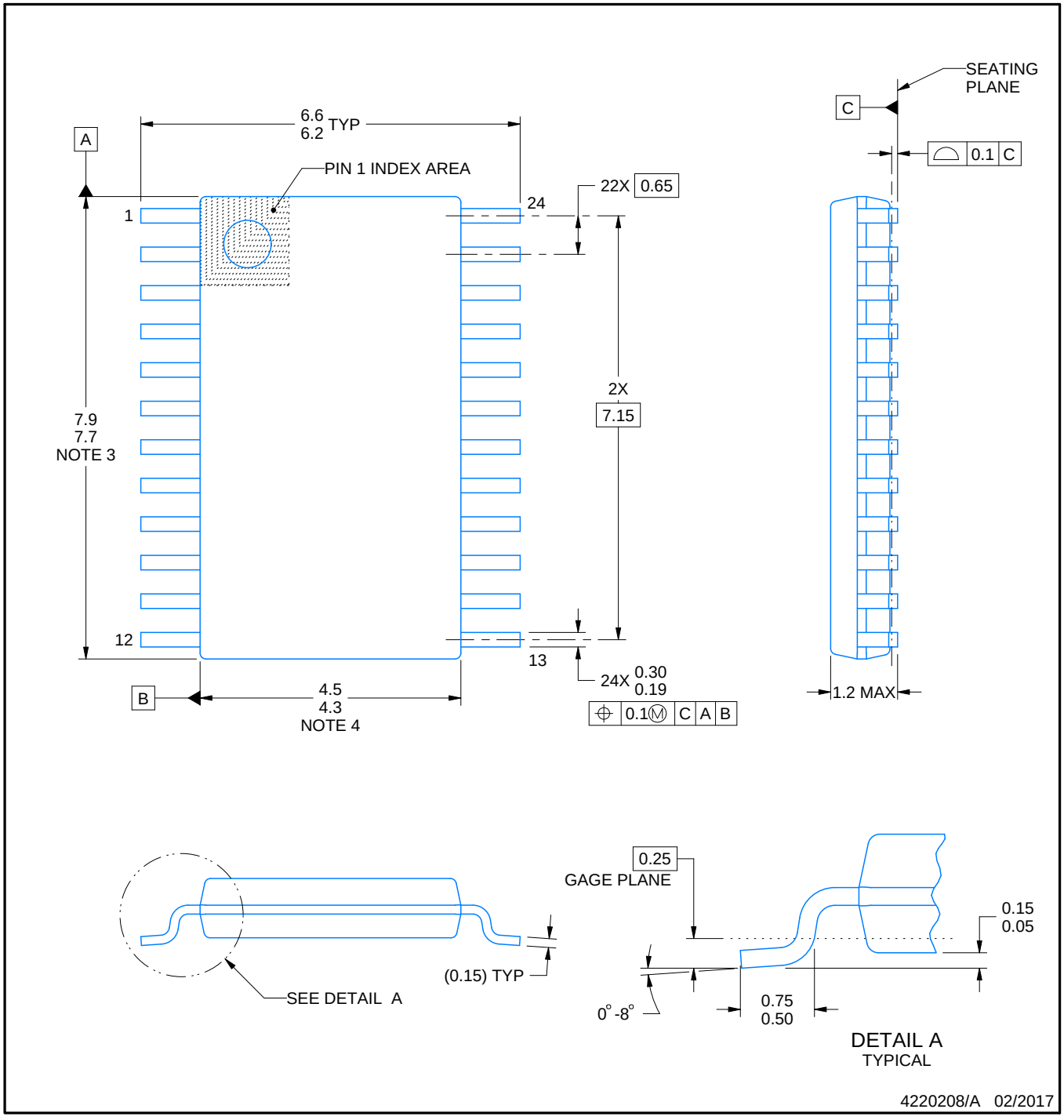
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MSP430AFE221IPW	PW	TSSOP	24	60	530	10.2	3600	3.5
MSP430AFE222IPW	PW	TSSOP	24	60	530	10.2	3600	3.5
MSP430AFE223IPW	PW	TSSOP	24	60	530	10.2	3600	3.5
MSP430AFE231IPW	PW	TSSOP	24	60	530	10.2	3600	3.5
MSP430AFE232IPW	PW	TSSOP	24	60	530	10.2	3600	3.5
MSP430AFE233IPW	PW	TSSOP	24	60	530	10.2	3600	3.5
MSP430AFE251IPW	PW	TSSOP	24	60	530	10.2	3600	3.5
MSP430AFE252IPW	PW	TSSOP	24	60	530	10.2	3600	3.5
MSP430AFE253IPW	PW	TSSOP	24	60	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0024A

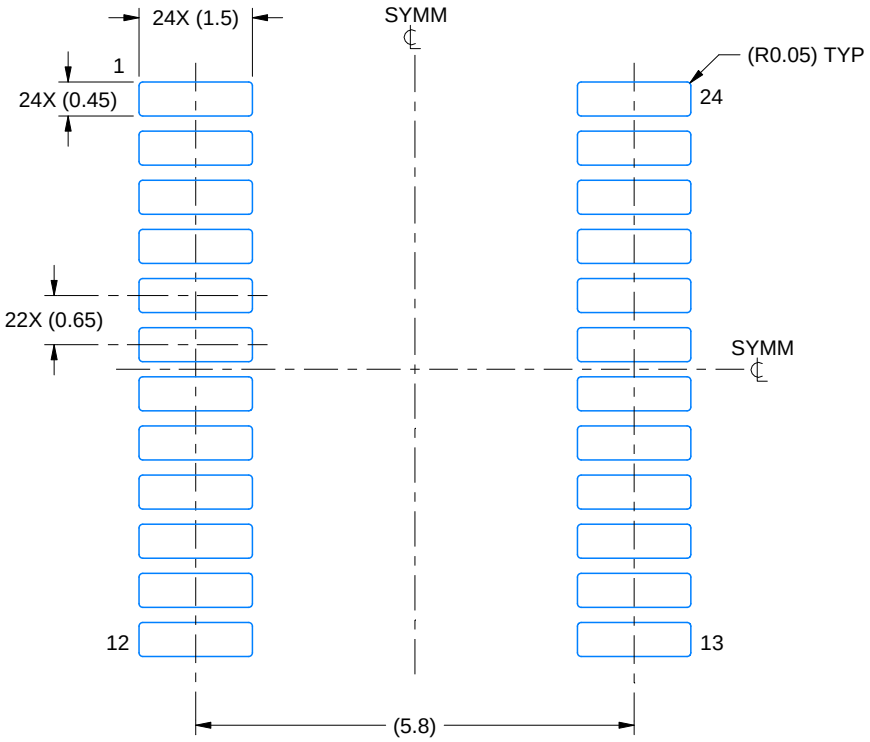
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

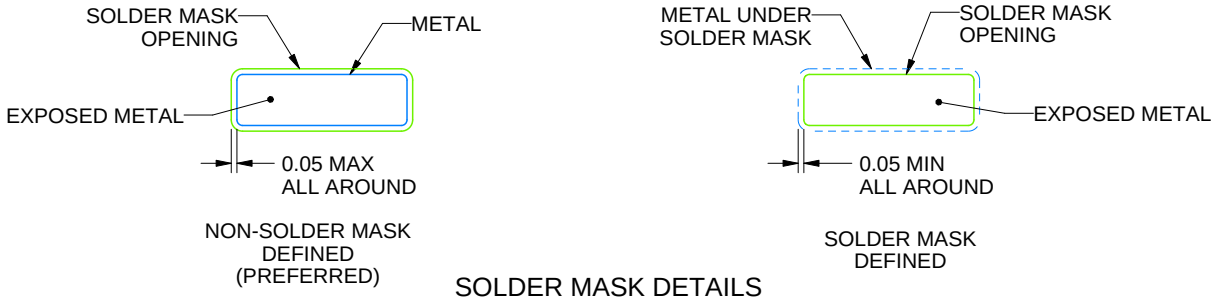


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

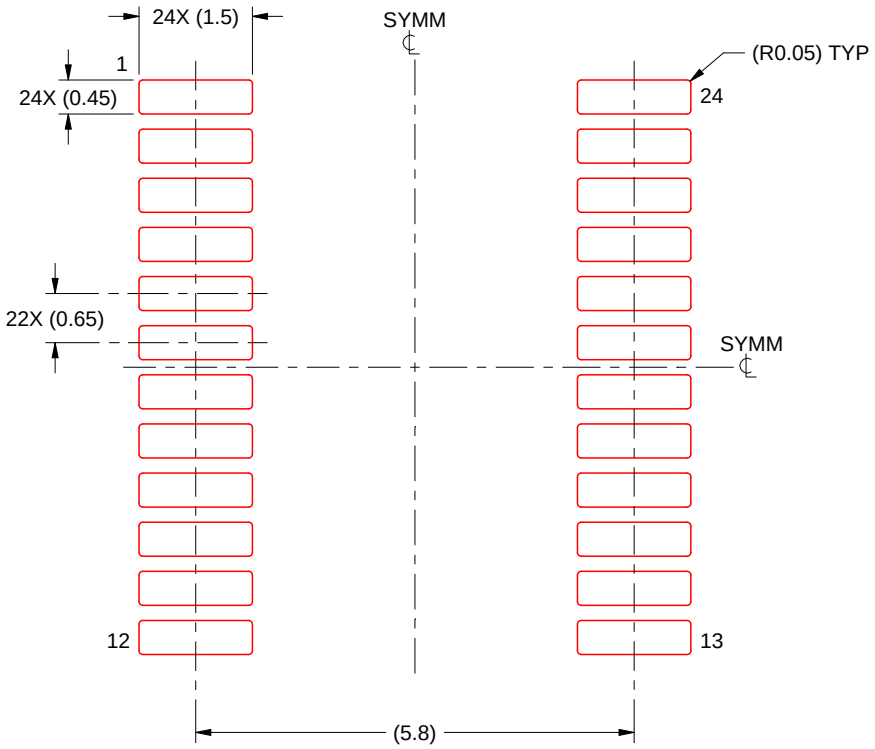


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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