Dual, 12-Bit, 3+3 or 2+2 Channel, Simultaneous Sampling Analog-to-Digital Converter

Check for Samples: ADS7865

FEATURES

- **Six Pseudo- or Four Fully Differential Inputs**
- **SNR: 71.7dB, THD: –87dB**
- **Programmable Channel Sequencer**
- **Programmable and Buffered Internal 2.5V Reference**
- **Flexible Power-Down Features**
- **Variable Power-Supply Ranges: 2.7V to 5.5V**
- **Low-Power Operation: 44mW Maximum at 5V**
- **Operating Temperature Range: –40°C to +125°C**
- **Pin-Compatible Upgrade for the ADS7862**

APPLICATIONS

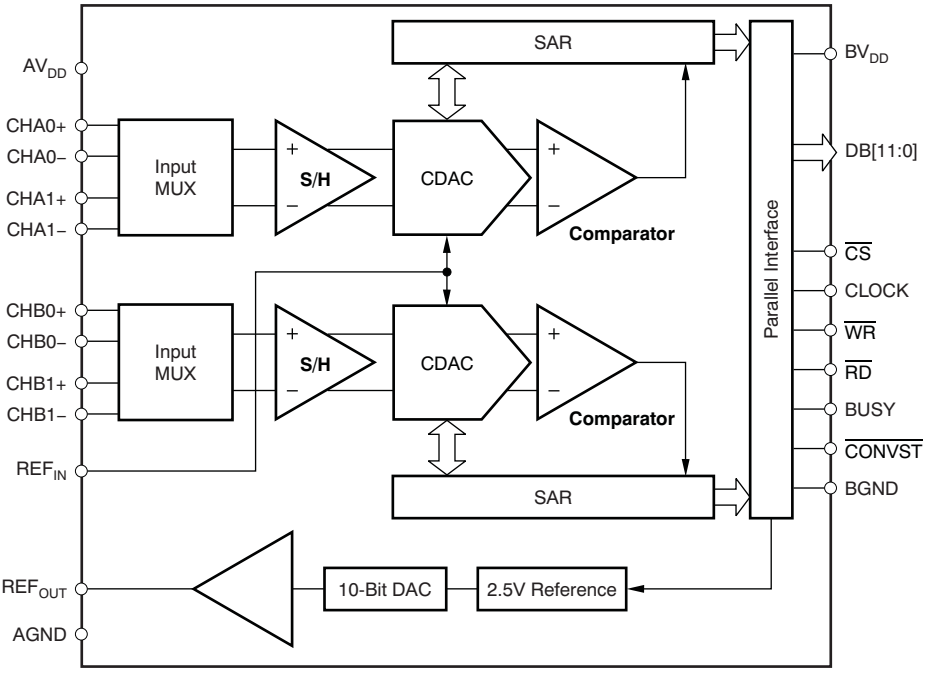
- **Motor Control**
- **Multi-Axis Positioning Systems**
- **Three-Phase Power Control**

DESCRIPTION

The ADS7865 is a dual, 12-bit, 2MSPS analog-to-digital converter (ADC) with four fully differential or six pseudo-differential input channels grouped into two pairs for high-speed, simultaneous signal acquisition. Inputs to the sample-and-hold (S/H) amplifiers are fully differential and are maintained differentially to the input of the ADC. This architecture provides excellent common-mode rejection of 72dB at 100kHz, which is a critical performance characteristic in noisy environments.

The ADS7865 is pin-compatible with the ADS7862, but offers additional features such as a programmable channel sequencer and reference output, flexible supply voltage (2.7V to 5.5V for AV_{DD} and BV_{DD}), a pseudo-differential input multiplexer with three channels per ADC, and several power-down features.

The ADS7865 is offered in a TQFP-32 package. It is specified over the extended operating temperature range of –40°C to +125°C.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		ADS7865	UNIT
Supply voltage, AV_{DD} to AGND		–0.3 to +6	V
Supply voltage, BV_{DD} to BGND		–0.3 to +6	V
Supply voltage, BV_{DD} to AV_{DD}		1.5 × AVDD	V
Analog and reference input voltage with respect to AGND		AGND – 0.3 to AVDD + 0.3	V
Digital input voltage with respect to BGND		BGND – 0.3 to BVDD + 0.3	V
Ground voltage difference |AGND – BGND|		0.3	V
Input current to all pins except power-supply pins		–10 to +10	mA
Maximum virtual junction temperature, T_J		+150	°C
ESD ratings	Human body model (HBM), JEDEC standard 22, test method A114-C.01, all pins	±4000	V
	Charged device model (CDM), JEDEC standard 22, test method C101, all pins	±1500	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range, unless otherwise noted.

PARAMETER		ADS7865 MIN	ADS7865 NOM	ADS7865 MAX	UNIT
Supply voltage, AV_{DD} to AGND		2.7	5.0	5.5	V
Supply voltage, BV_{DD} to BGND	Low voltage levels	2.7		3.6	V
	5V logic levels	4.5	5.0	5.5	V
Reference input voltage on REF_{IN}		0.5	2.5	2.525	V
Analog differential input voltage (CHXX+) – (CHXX–)		$–V_{REF}$		$+V_{REF}$	V
Operating ambient temperature range, T_A		–40		+125	°C

THERMAL CHARACTERISTICS(1)

Over operating free-air temperature range, unless otherwise noted.

PARAMETER			ADS7865	UNIT
θ_{JA}	Junction-to-air thermal resistance	High-K thermal resistance	56.4	°C/W
θ_{JC}	Junction-to-case thermal resistance		20.8	°C/W
P_D	Device power dissipation at AVDD = 5V and BVDD = 3.3V		44	mW

(1) Tested in accordance with the High-K thermal metric definitions of EIA/JESD51-3 for leaded surface-mount packages with a 3×3 via array.

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ELECTRICAL CHARACTERISTICS

At T_A = –40°C to +125°C; over entire power-supply voltage range, V_{REF} = 2.5V (internal), f_{CLK} = 32MHz, and f_{DATA} = 2MSPS, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS7865			UNIT
			MIN	TYP(1)	MAX	
RESOLUTION			12			Bits
ANALOG INPUT						
FSR	Full-scale differential input range	(CHxx+) – (CHxx–)	$–V_{REF}$		$+V_{REF}$	V
V_{IN}	Absolute input voltage	CHxx+ or CHxx– to AGND	–0.1		AV_{DD} + 0.1	V
C_{IN}	Input capacitance	CHxx+ or CHxx– to AGND		2		pF
C_{ID}	Differential input capacitance			4		pF
I_{IL}	Input leakage current		–50		50	nA
CMRR	Common-mode rejection ratio	Both ADCs, dc to 100kHz		72		dB
DC ACCURACY						
INL	Integral nonlinearity	–40°C < T_A < +125°C	–1.25	±0.6	+1.25	LSB
		–40°C < T_A < +85°C	–1	±0.5	+1	LSB
DNL	Differential nonlinearity		–1	±0.4	+1	LSB
V_{OS}	Input offset error		–3	±0.5	+3	LSB
	Match		–3	±0.5	+3	LSB
dV_{OS}/dT	Input offset thermal drift			±2		µV/°C
G_{ERR}	Gain error		–0.6	0.15	+0.6	%
	Match		–0.6	±0.1	+0.6	%
G_{ERR}/dT	Gain error thermal drift			±2		ppm/°C
PSRR	Power-supply rejection ratio	AV_{DD} = 5V		70		dB
AC ACCURACY						
SINAD	Signal-to-noise + distortion	V_{IN} = $5V_{PP}$ at 100kHz	69	71.3		dB
SNR	Signal-to-noise ratio	V_{IN} = $5V_{PP}$ at 100kHz	70	71.7		dB
THD	Total harmonic distortion	V_{IN} = $5V_{PP}$ at 100kHz		–87	–74	dB
SFDR	Spurious-free dynamic range	V_{IN} = $5V_{PP}$ at 100kHz	74	88		dB
SAMPLING DYNAMICS						
t_{CONV}	Conversion time per ADC	1MHz < f_{CLK} ≤ 32MHz	13			Clocks
t_{ACQ}	Acquisition time		62.5			ns
f_{DATA}	Data rate	1MHz < f_{CLK} ≤ 32MHz	62.5		2000	kSPS
t_A	Aperture delay				6	ns
	Match			50		ps
t_{AJIT}	Aperture jitter			50		ps
f_{CLK}	Clock frequency on CLOCK		1		32	MHz

(1) All values at T_A = +25°C.

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ELECTRICAL CHARACTERISTICS (continued)

At T_A = –40°C to +125°C; over entire power-supply voltage range, V_{REF} = 2.5V (internal), f_{CLK} = 32MHz, and f_{DATA} = 2MSPS, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS7865			UNIT
			MIN	TYP(1)	MAX	
INTERNAL VOLTAGE REFERENCE						
Resolution	Reference output DAC resolution		10			Bits
V_{REFOUT}	Reference output voltage	Over 20% to 100% DAC range	0.496		2.515	V
		DAC = 0x3FF, –40°C < T_A < +125°C	2.485	2.500	2.515	V
		DAC = 0x3FF at +25°C	2.495	2.500	2.505	V
dV_{REFOUT}/dT	Reference voltage drift			±10		ppm/°C
DNL_{DAC}	DAC differential linearity error		–4	±1	4	LSB
INL_{DAC}	DAC integral linearity error		–4	±0.5	4	LSB
V_{OSDAC}	DAC offset error	V_{REFOUT} = 0.5V	–4	±1	4	LSB
PSRR	Power-supply rejection ratio			73		dB
I_{REFOUT}	Reference output dc current		–2		+2	mA
I_{REFSC}	Reference output short-circuit current			50		mA
t_{REFON}	Reference output settling time			0.5		ms
VOLTAGE REFERENCE INPUT						
V_{REF}	Reference input voltage range		0.5		2.525	V
I_{REF}	Reference input current			50		µA
C_{REF}	Reference input capacitance			10		pF
DIGITAL INPUTS						
	Logic family	CMOS				
V_{IH}	High-level input voltage		0.7 × BV_{DD}		BV_{DD} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 × BV_{DD}	V
I_{IN}	Input current	V_I = BV_{DD} to BGND	–50		+50	nA
C_I	Input capacitance			5		pF
DIGITAL OUTPUTS						
	Logic family	CMOS				
V_{OH}	High-level output voltage	I_{OH} = –100µA	BV_{DD} – 0.2			V
V_{OL}	Low-level output voltage	I_{OH} = 100µA			0.2	V
I_{OZ}	High-impedance-state output current	V_I = BV_{DD} to BGND	–50		+50	nA
C_O	Output capacitance			5		pF
C_L	Load capacitance				30	pF

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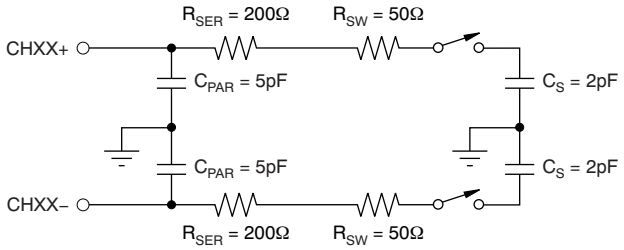
ELECTRICAL CHARACTERISTICS (continued)

At T_A = –40°C to +125°C; over entire power-supply voltage range, V_{REF} = 2.5V (internal), f_{CLK} = 32MHz, and f_{DATA} = 2MSPS, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS7865			UNIT
			MIN	TYP(1)	MAX	
POWER SUPPLY						
AV_{DD}	Analog supply voltage	AV_{DD} to AGND	2.7	5.0	5.5	V
BV_{DD}	Buffer I/O supply current	BV_{DD} to BGND	2.7	3.0	5.5	V
AI_{DD}	Analog supply current	AV_{DD} = 2.7V		4.1	6.0	mA
		AV_{DD} = 5V		5.6	7.5	mA
		AV_{DD} = 2.7V, NAP power-down		0.9	1.6	mA
		AV_{DD} = 5V, NAP power-down		1.1	1.8	mA
		AV_{DD} = 2.7V, deep power-down			0.001	mA
		AV_{DD} = 5V, deep power-down			0.001	mA
BI_{DD}	Buffer I/O supply current	BV_{DD} = 2.7V, C_{LOAD} = 10pF		0.6	1.7	mA
		BV_{DD} = 3.3V, C_{LOAD} = 10pF		0.8	1.9	mA
P_D	Power dissipation	AV_{DD} = 2.7V, BV_{DD} = 2.7V		12.7	21	mA
		AV_{DD} = 5.0V, BV_{DD} = 3.0V		30.6	44	mW

EQUIVALENT INPUT CIRCUIT



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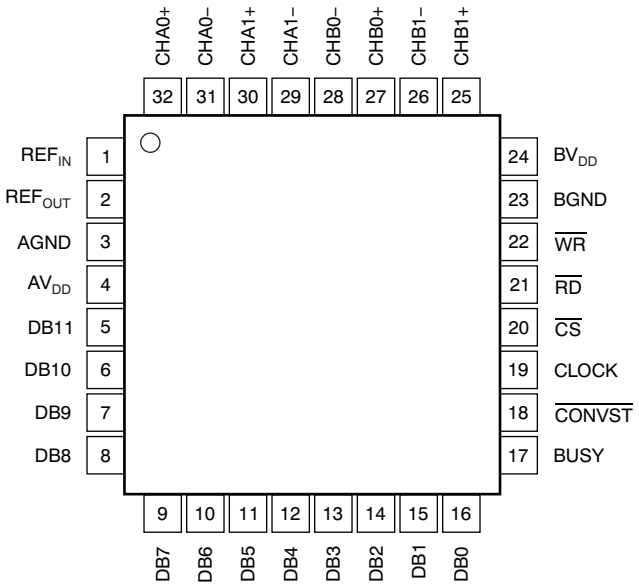
DEVICE INFORMATION

PBS PACKAGE
TQFP-32
(TOP VIEW)



TERMINAL FUNCTIONS

PIN NUMBER	NAME	DESCRIPTION
1	REF_{IN}	Reference voltage input. A ceramic capacitor of 470nF (min) is required at this terminal.
2	REF_{OUT}	Reference voltage output. The programmable internal voltage reference output is available on this pin.
3	AGND	Analog ground. Connect to analog ground plane.
4	AV_{DD}	Analog power supply, 2.7V to 5.5V. Decouple to AGND with a 1µF ceramic capacitor.
5	DB11	Data bit 11, MSB
6	DB10	Data bit 10
7	DB9	Data bit 9
8	DB8	Data bit 8
9	DB7	Data bit 7
10	DB6	Data bit 6
11	DB5	Data bit 5
12	DB4	Data bit 4
13	DB3	Data bit 3
14	DB2	Data bit 2
15	DB1	Data bit 1
16	DB0	Data bit 0
17	BUSY	ADC busy indicator. BUSY goes high when the inputs are in hold mode and returns to low after the conversion has been finished.
18	$\overline{CONVST}$	Conversion start. The ADC switches from the sample into the hold mode on the falling edge of $\overline{CONVST}$, independent of the status of the CLOCK. The conversion itself starts with the next rising edge of CLOCK.
19	CLOCK	External clock input.
20	$\overline{CS}$	Chip select. When low, the parallel interface of the device is active; when high, input signals are ignored and output signals are 3-state.
21	$\overline{RD}$	Read data. Falling edge active synchronization pulse for the parallel data outputs. $\overline{RD}$ only triggers, when $\overline{CS}$ is low.
22	$\overline{WR}$	Write data. Rising edge latches in the parallel data inputs. $\overline{WR}$ only triggers, when $\overline{CS}$ is low.

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TERMINAL FUNCTIONS (continued)

PIN NUMBER	NAME	DESCRIPTION
23	BGND	Buffer I/O ground. Connect to digital ground plane.
24	BV_{DD}	Buffer I/O power supply, 2.7V to 5.5V. Decouple to BGND with a 1µF ceramic capacitor.
25	CHB1+	Noninverting analog input channel B1
26	CHB1–	Inverting analog input channel B1
27	CHB0+	Noninverting analog input channel B0
28	CHB0–	Inverting analog input channel B0
29	CHA1–	Inverting analog input channel A1
30	CHA1+	Noninverting analog input channel A1
31	CHA0–	Inverting analog input channel A0
32	CHA0+	Noninverting analog input channel A0

TIMING CHARACTERISTICS

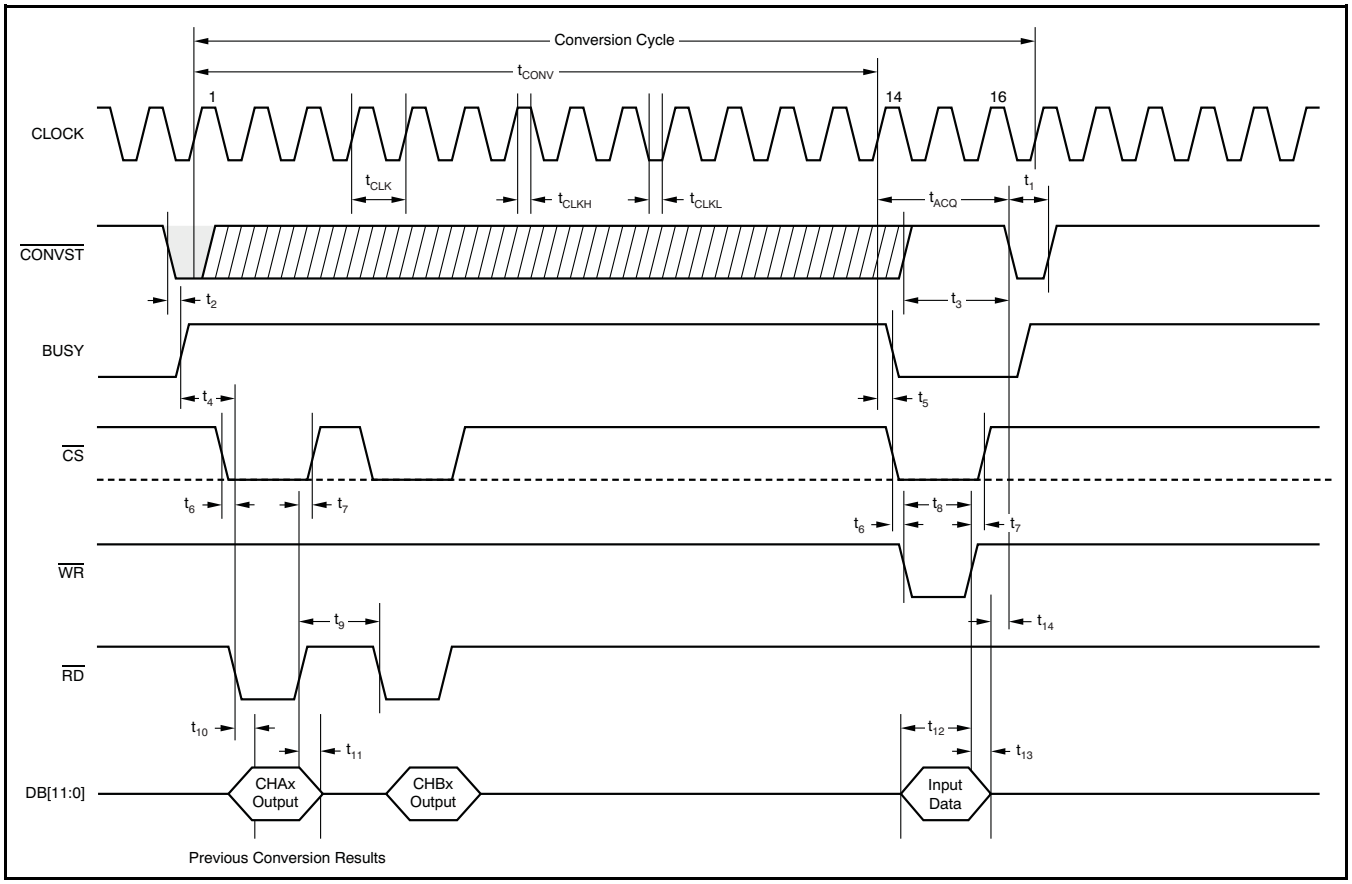

Figure 1. Interface Timing Diagram

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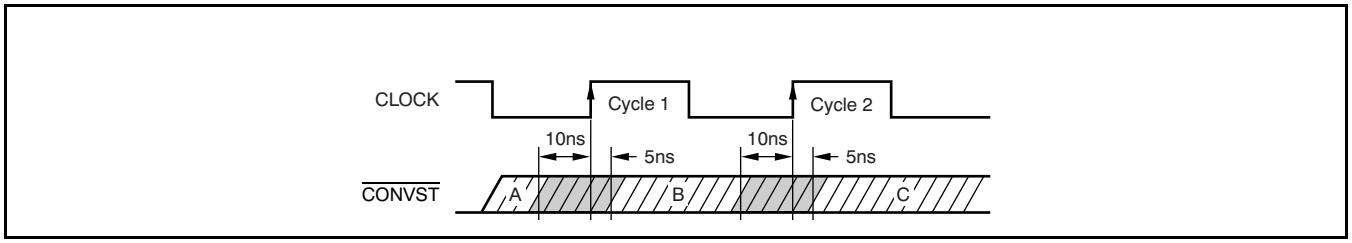
TIMING REQUIREMENTS(1)

PARAMETER		TEST CONDITIONS	ADS7865			UNIT
			MIN	TYP	MAX	
t_{CONV}	Conversion time	f_{CLOCK} = 32MHz		13		t_{CLK}
t_{ACQ}	Acquisition time	See Figure 1	62.5			ns
f_{CLK}	CLOCK frequency		1		32	MHz
t_{CLK}	CLOCK period		31.25		1000	ns
t_{CLKL}	CLOCK low time		9.4			ns
t_{CLKH}	CLOCK high time		9.4			ns
t_1	$\overline{CONVST}$ low time		20			ns
t_2	$\overline{CONVST}$ falling edge to BUSY high delay(2)		3			ns
t_3	$\overline{CONVST}$ high time		20			ns
t_4	$\overline{RD}$ falling edge to BUSY high setup time		1			t_{CLK}
t_5	14th CLOCK rising edge to BUSY low delay		3			ns
t_6	$\overline{CS}$ falling edge to $\overline{RD}$ or $\overline{WR}$ falling edge setup time		0			ns
t_7	$\overline{CS}$ rising edge to $\overline{RD}$ or $\overline{WR}$ rising edge hold time		0			ns
t_8	$\overline{WR}$ low time		10			ns
t_9	$\overline{RD}$ high time between two read accesses		10			ns
t_{10}	$\overline{RD}$ falling edge to output data valid delay				20	ns
t_{11}	Output data hold time		5			ns
t_{12}	Input data setup time		10			ns
t_{13}	Input data hold time		5			ns
t_{14}	Input data still valid to $\overline{CONVST}$ falling edge setup time		31.25			ns

(1) All input signals are specified with $t_R = t_F$ = 1.5ns (10% to 90% of BV_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) Not applicable in auto-Nap power-down mode.



NOTE: All $\overline{CONVST}$ commands that occur more than 10ns before the rising edge of cycle '1' of the external clock (Region 'A') initiate a conversion on the rising edge of cycle '1'. All $\overline{CONVST}$ commands that occur 5ns after the rising edge of cycle '1' or 10ns before the rising edge of cycle '2' (Region 'B') initiate a conversion on the rising edge of cycle '2'. All $\overline{CONVST}$ commands that occur 5ns after the rising edge of cycle '2' (Region 'C') initiate a conversion on the rising edge of the next clock period.
The $\overline{CONVST}$ pin should never be switched from LOW to HIGH in the region 10ns before the rising edge of the CLOCK and 5ns after the rising edge (gray areas). If $\overline{CONVST}$ is toggled in this gray area, the conversion could begin on either the same rising edge of the CLOCK or the following edge.

Figure 2. $\overline{CONVST}$ Timing

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TYPICAL CHARACTERISTICS

Over the entire supply voltage range; V_{REF} = 2.5V (internal), f_{CLK} = 32MHz, and f_{DATA} = 2MSPS, unless otherwise noted.

INTEGRAL NONLINEARITY vs DATA RATE

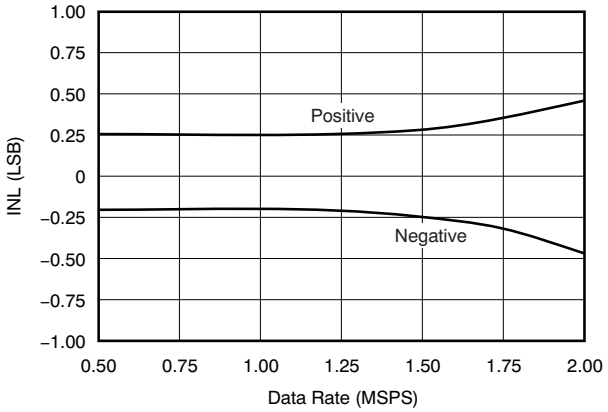

Figure 3.

INTEGRAL NONLINEARITY vs TEMPERATURE

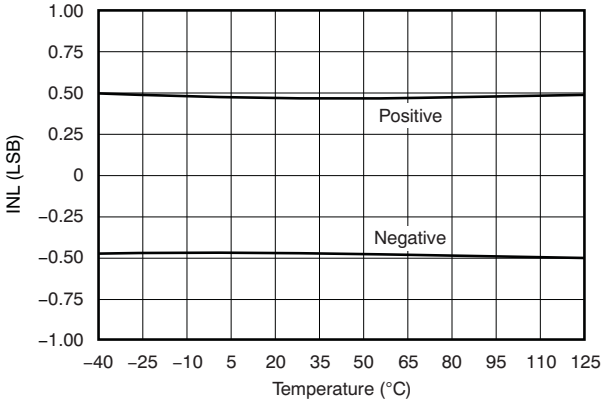

Figure 4.

INTEGRAL NONLINEARITY vs CODE

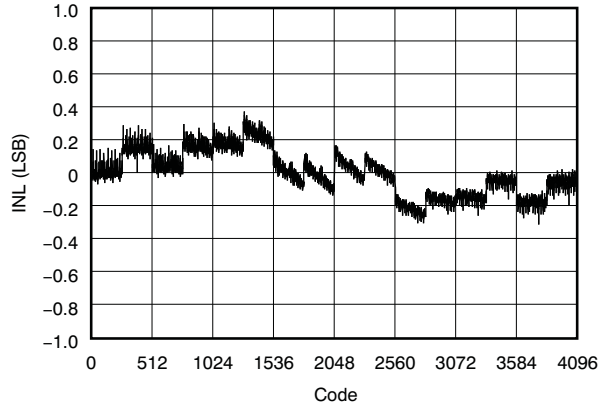

Figure 5.

DIFFERENTIAL NONLINEARITY vs CODE

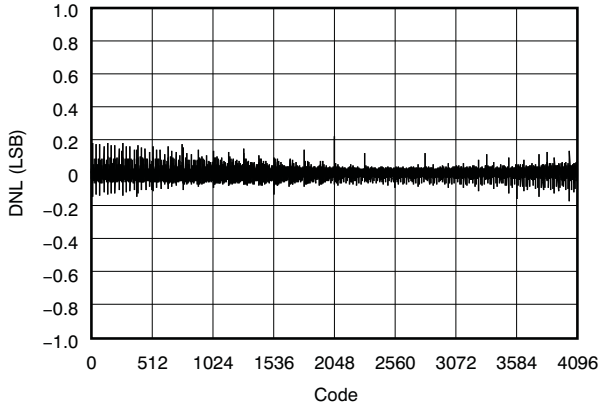

Figure 6.

DIFFERENTIAL NONLINEARITY vs DATA RATE

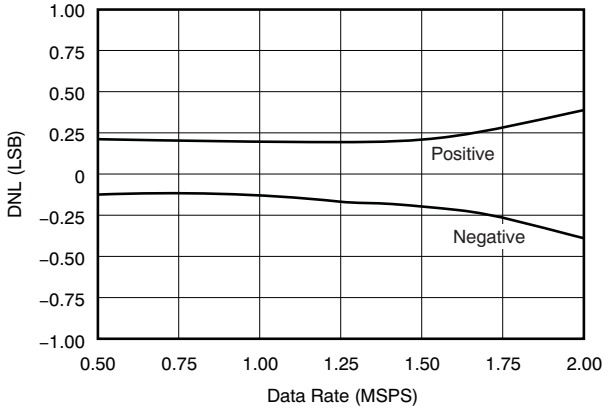

Figure 7.

DIFFERENTIAL NONLINEARITY vs TEMPERATURE

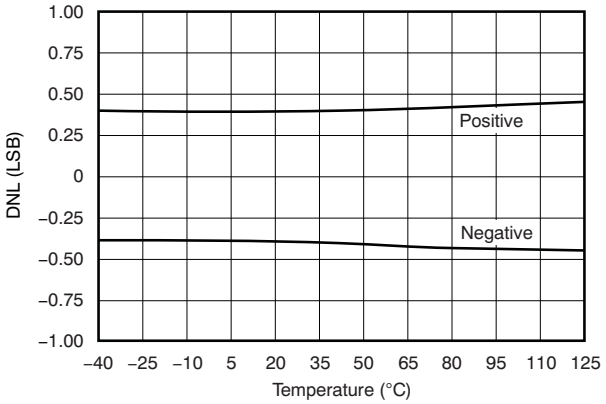

Figure 8.

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TYPICAL CHARACTERISTICS (continued)

Over the entire supply voltage range; V_{REF} = 2.5V (internal), f_{CLK} = 32MHz, and f_{DATA} = 2MSPS, unless otherwise noted.

OFFSET ERROR AND OFFSET MATCH vs ANALOG SUPPLY VOLTAGE

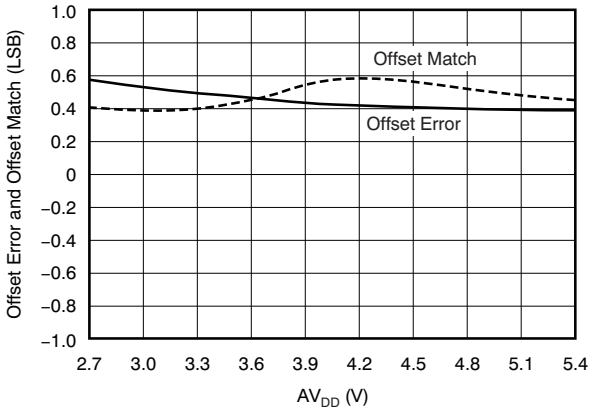

Figure 9.

OFFSET ERROR AND OFFSET MATCH vs TEMPERATURE

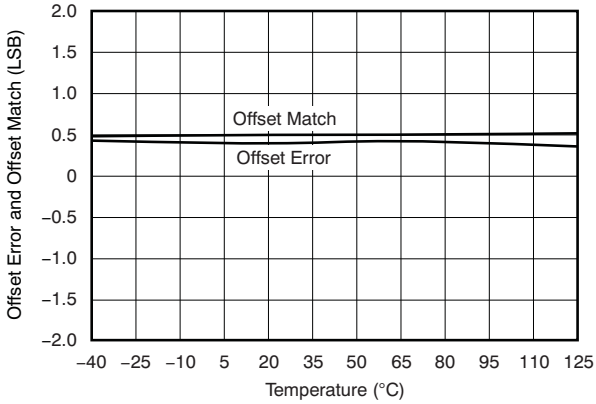

Figure 10.

GAIN ERROR AND GAIN MATCH vs ANALOG SUPPLY VOLTAGE

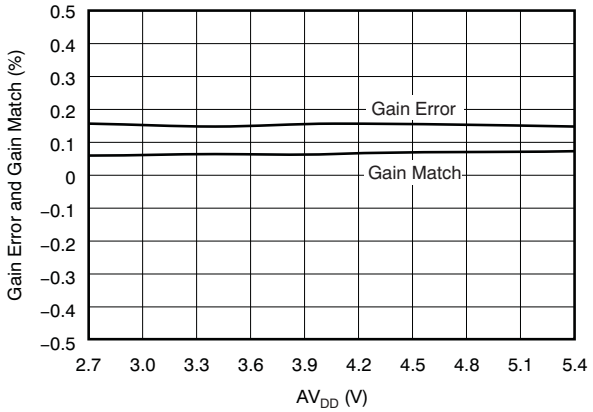

Figure 11.

GAIN ERROR AND GAIN MATCH vs TEMPERATURE

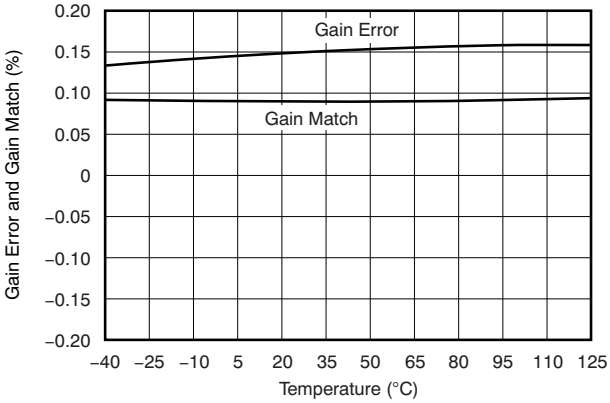

Figure 12.

COMMON-MODE REJECTION RATIO vs ANALOG SUPPLY VOLTAGE

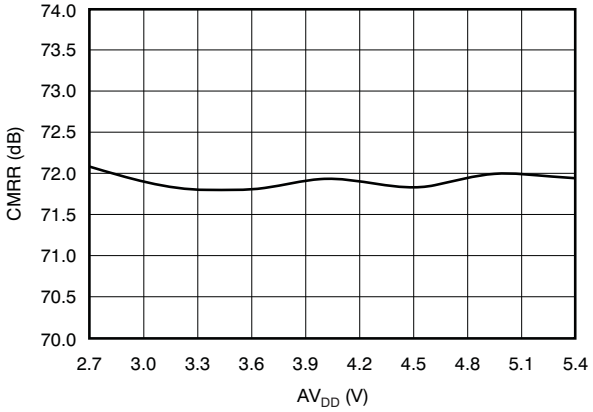

Figure 13.

COMMON-MODE REJECTION RATIO vs TEMPERATURE

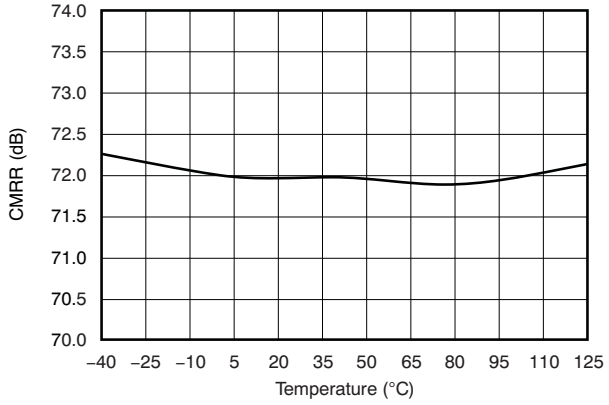

Figure 14.

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TYPICAL CHARACTERISTICS (continued)

Over the entire supply voltage range; V_{REF} = 2.5V (internal), f_{CLK} = 32MHz, and f_{DATA} = 2MSPS, unless otherwise noted.

FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 100kHz)

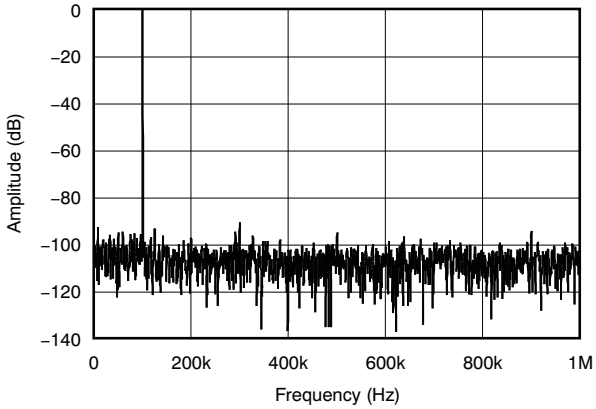

Figure 15.

FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 100kHz, f_{SAMPLE} = 1.5MSPS)

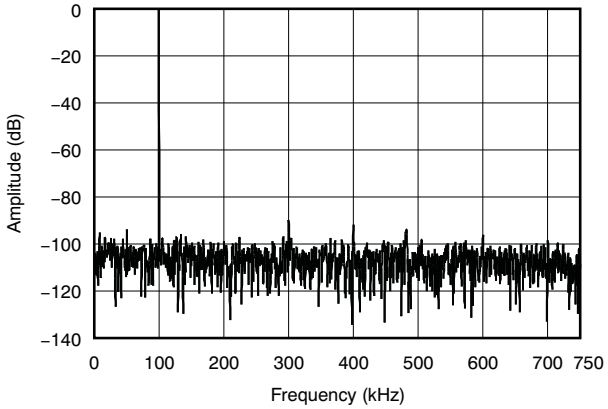

Figure 16.

SIGNAL-TO-NOISE RATIO AND DISTORTION
vs INPUT SIGNAL FREQUENCY

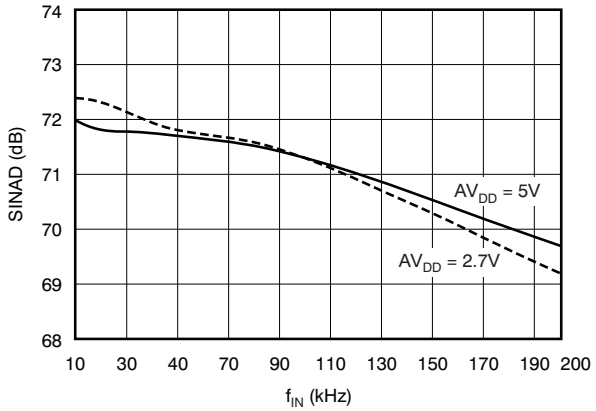

Figure 17.

SIGNAL-TO-RATIO AND DISTORTION
vs TEMPERATURE

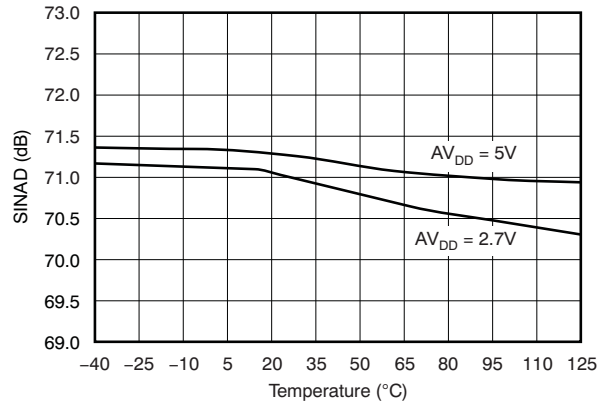

Figure 18.

SIGNAL-TO-NOISE RATIO
vs INPUT SIGNAL FREQUENCY

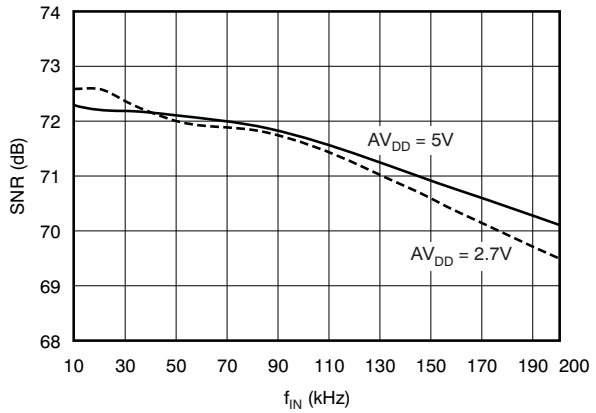

Figure 19.

SIGNAL-TO-NOISE RATIO
vs TEMPERATURE

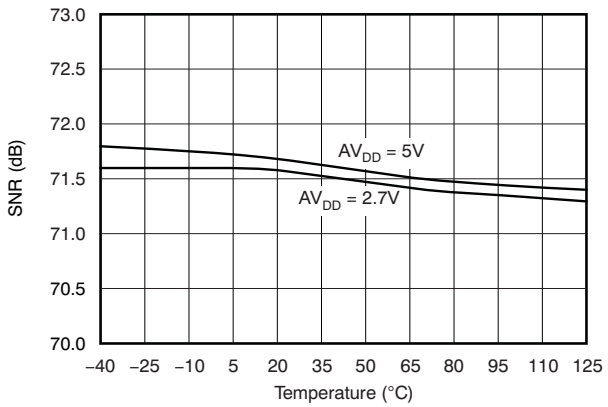

Figure 20.

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TYPICAL CHARACTERISTICS (continued)

Over the entire supply voltage range; V_{REF} = 2.5V (internal), f_{CLK} = 32MHz, and f_{DATA} = 2MSPS, unless otherwise noted.

TOTAL HARMONIC DISTORTION vs INPUT SIGNAL FREQUENCY

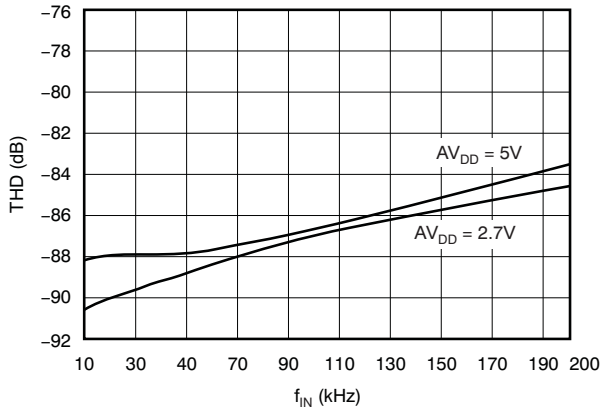

Figure 21.

TOTAL HARMONIC DISTORTION vs TEMPERATURE

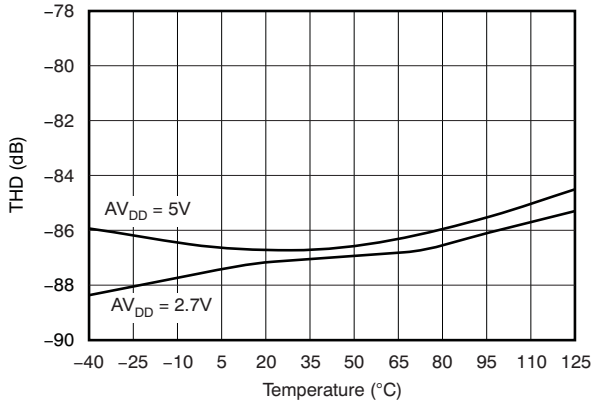

Figure 22.

SPURIOUS-FREE DYNAMIC RANGE vs INPUT SIGNAL FREQUENCY

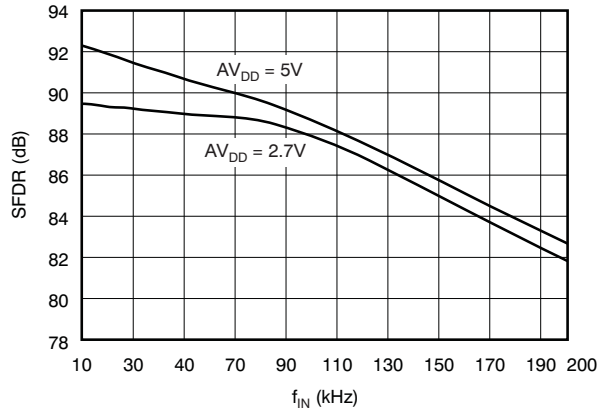

Figure 23.

SPURIOUS-FREE DYNAMIC RANGE vs TEMPERATURE

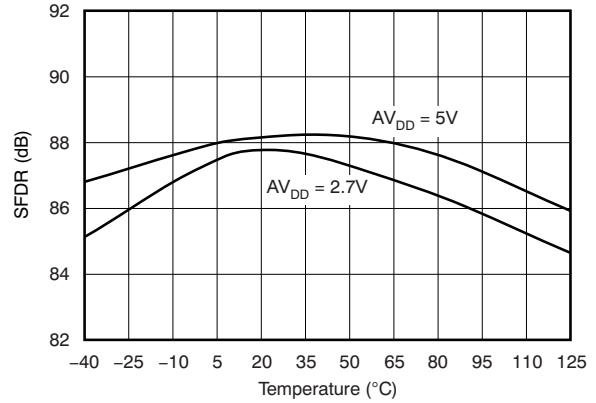

Figure 24.

ANALOG SUPPLY CURRENT vs TEMPERATURE

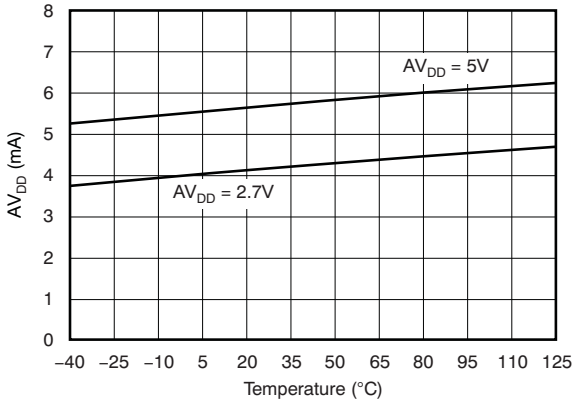

Figure 25.

DIGITAL SUPPLY CURRENT vs TEMPERATURE

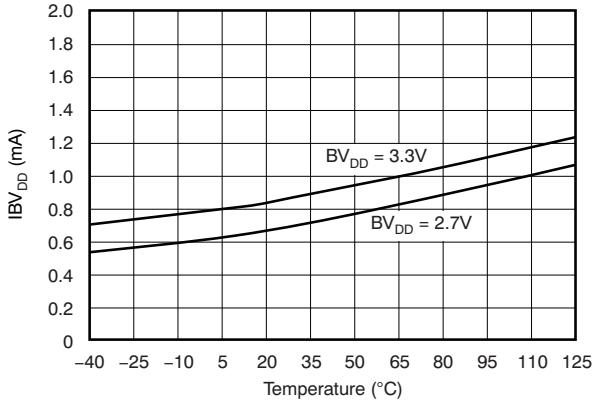

Figure 26.

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TYPICAL CHARACTERISTICS (continued)

Over the entire supply voltage range; V_{REF} = 2.5V (internal), f_{CLK} = 32MHz, and f_{DATA} = 2MSPS, unless otherwise noted.

ANALOG SUPPLY CURRENT vs DATA RATE (Auto-NAP Mode)

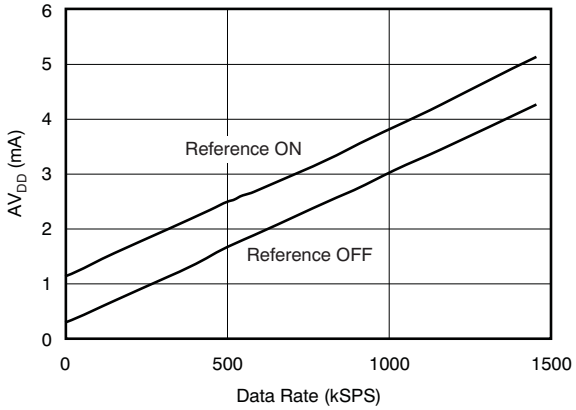

Figure 27.

ANALOG SUPPLY CURRENT vs TEMPERATURE (Auto-NAP Mode)

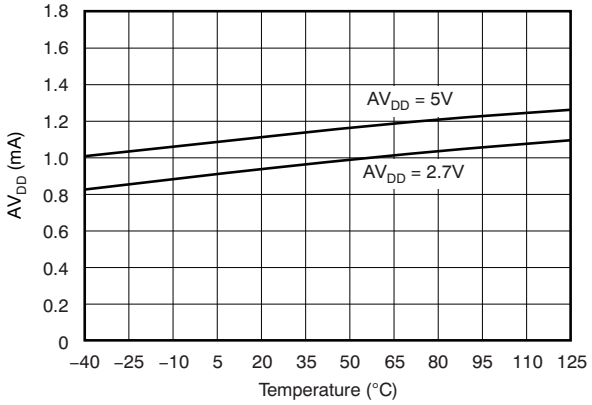

Figure 28.

ANALOG SUPPLY CURRENT vs DATA RATE (Deep Power-Down Mode)

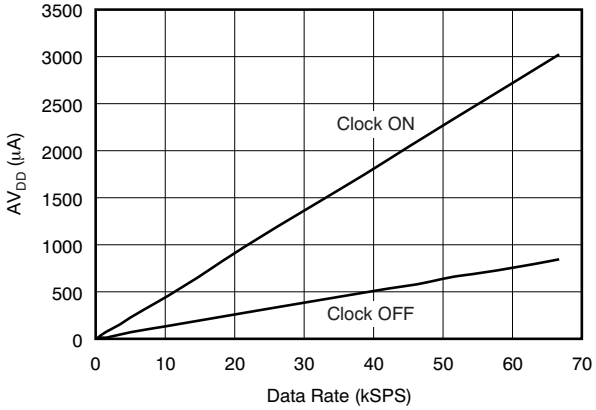

Figure 29.

REFERENCE OUTPUT VOLTAGE vs TEMPERATURE

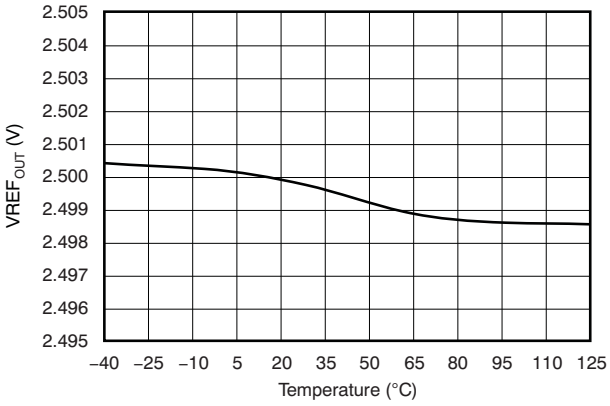

Figure 30.

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APPLICATION INFORMATION

GENERAL DESCRIPTION

The ADS7865 includes two 12-bit analog-to-digital converters (ADCs) that operate based on the successive-approximation register (SAR) principle. The ADCs sample and convert simultaneously. Conversion time can be as low as 406.25ns. Adding the acquisition time of 62.5ns and an additional clock cycle for setup/hold time requirements and skew results in a maximum conversion rate of 2MSPS.

Each ADC has a fully differential 2:1 multiplexer front-end. In many common applications, all negative input signals remain at the same constant voltage (for example, 2.5V). In this type of application, the multiplexer can be used in a pseudo-differential 3:1 mode, where CHx0– functions as a common-mode input and the remaining three inputs (CHx0+, CHx1–, and CHx1+) operate as separate inputs referred to the common-mode input.

The ADS7865 also includes a 2.5V internal reference. The reference drives a 10-bit digital-to-analog converter (DAC), allowing the voltage at the REF_{OUT} pin to be adjusted via the internal DAC register in 2.44mV steps. A low-noise operational amplifier with unity-gain buffers the DAC output voltage and drives the REF_{OUT} pin.

The ADS7865 offers a parallel interface that is pin-compatible with the ADS7862. However, instead of the A0 pin of the ADS7862 that controls channel selection, the ADS7865 offers a write data input ($\overline{WR}$) pin that supports additional functions described in the *Digital* section of this data sheet (see also the *ADS7862 Compatibility* section).

ANALOG

This section discusses the analog input circuit, the ADCs, and the reference design of the device.

Analog Inputs

Each ADC is fed by an input multiplexer, as shown in Figure 31. Each multiplexer is either used in a fully-differential 2:1 configuration (as described in Table 1) or a pseudo-differential 3:1 configuration (as shown in Table 2). The channel selection is performed using bits C1 and C0 in the configuration register (see also the *Configuration Register* section).

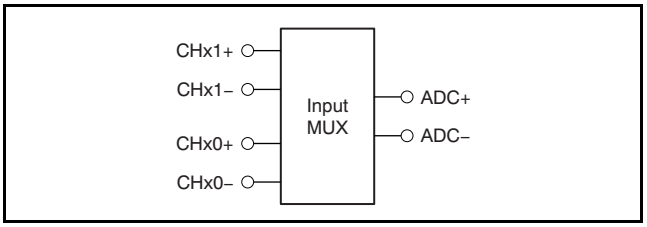

Figure 31. Input Multiplexer Configuration

Table 1. Fully Differential 2:1 Multiplexer Configuration

C1	C0	ADC+	ADC–
0	0	CHx0+	CHx0–
1	1	CHx1+	CHx1–

Table 2. Pseudo-Differential 3:1 Multiplexer Configuration

C1	C0	ADC+	ADC–
0	0	CHx0+	CHx0–
0	1	CHx1–	CHx0–
1	0	CHx1+	CHx0–

The input path for the converter is fully differential and provides a common-mode rejection of 72dB at 100kHz. The high CMRR also helps suppress noise in harsh industrial environments.

Each of the 2pF sample-and-hold capacitors (shown as C_S in the *Equivalent Input Circuit*) is connected via switches to the multiplexer output. Opening the switches holds the sampled data during the conversion process. After finishing the conversion, both capacitors are pre-charged for the duration of one clock cycle to the voltage present at the REF_{IN} pin. After the pre-charging, the multiplexer outputs are connected to the sampling capacitors again. The voltage at the analog input pin is usually different from the reference voltage; therefore, the sample capacitors must be charged to within one-half LSB for 12-bit accuracy during the acquisition time t_{ACQ} (see the Timing Characteristics).

Acquisition time is indicated with the BUSY signal being held low. It starts by closing the input switches (after finishing the previous conversion and pre-charging) and finishes with the rising edge of the $\overline{CONVST}$ signal. If the ADS7865 operates at full speed, the acquisition time is typically 62.5ns.

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The minimum –3dB bandwidth of the driving operational amplifier can be calculated as shown in Equation 1, with *n* = 12 being the resolution of the ADS7865:

$$f_{-3dB} = \frac{\ln(2) \times (n + 1)}{2\pi \times t_{ACQ}} \quad (1)$$

With t_{ACQ} = 62.5ns, the minimum bandwidth of the driving amplifier is 23MHz. The required bandwidth can be lower if the application allows a longer acquisition time.

A gain error occurs if a given application does not fulfill the settling requirement shown in Equation 1. As a result of pre-charging the capacitors, linearity and THD are not directly affected, however.

The OPA365 from Texas Instruments is recommended as a driver; in addition to offering the required bandwidth, it provides a low offset and also offers excellent THD performance.

The phase margin of the driving operational amplifier is usually reduced by the ADC sampling capacitor. A resistor placed between the capacitor and the amplifier limits this effect; therefore, an internal 200Ω resistor (R_{SER}) is placed in series with the switch. The switch resistance (R_{SW}) is typically 50Ω (see the *Equivalent Input Circuit*).

The differential input voltage range of the ADC is $\pm V_{REF}$, the voltage at the REF_{IN} pin.

It is important to keep the voltage to all inputs within the 0.1V limit below AGND and above AV_{DD} while not allowing dc current to flow through the inputs. Current is only necessary to recharge the sample-and-hold capacitors.

Analog-to-Digital Converter (ADC)

The ADS7865 includes two SAR-type, 2MSPS, 12-bit ADCs (shown in the Functional Block Diagram on the front page of this data sheet).

$\overline{\text{CONVST}}$

The analog inputs are held with the falling edge of the $\overline{\text{CONVST}}$ (conversion start) signal. The setup time of $\overline{\text{CONVST}}$ referred to the next rising edge of CLOCK (system clock) is 10ns (minimum). The conversion automatically starts with the rising CLOCK edge. $\overline{\text{CONVST}}$ should not be issued during a conversion, that is, when BUSY is high.

CLOCK

The ADC uses an external clock in the range of 1MHz to 32MHz. 12 clock cycles are needed for a complete conversion; the following clock cycle is used for pre-charging the sample capacitors and a minimum of two clock cycles are required for the sampling. With a minimum of 16 clocks used for the entire process, one clock cycle is left for the required setup and hold times along with some margin for delay caused by layout. The clock input can remain low between conversions (after applying the 16th falling edge to complete a running conversion). It can also remain low after applying the 14th falling edge during a DAC register write access if the device is not required to perform a conversion (for example, during an initiation phase after power-up).

The CLOCK duty cycle should be 50%. However, the ADS7865 functions properly with a duty cycle between 30% and 70%.

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RESET

The ADS7865 features an internal power-on-reset (POR) function. When the device is powered up, the POR sets the device to default mode when AVDD reaches 1.8V.

REF_{IN}

The reference input is not buffered and is directly connected to the ADC. The converter generates spikes on the reference input voltage because of internal switching. Therefore, an external capacitor to the analog ground (AGND) should be used to stabilize the reference input voltage. This capacitor should be at least 470nF. Ceramic capacitors (X5R type) with values up to 1µF are commonly available as SMD in 0402 size.

REF_{OUT}

The ADS7865 includes a low-drift, 2.5V internal reference source. This source feeds a 10-bit string DAC that is controlled via the DAC register. As a result of this architecture, the voltage at the REF_{OUT} pin is programmable in 2.44mV steps and can be adjusted to specific application requirements without the use of additional external components.

However, the DAC output voltage should not be programmed below 0.5V to ensure the correct functionality of the reference output buffer. This buffer is connected between the DAC and the REF_{OUT} pin, and is capable of driving the capacitor at the REF_{IN} pin. A minimum of 470nF is required to keep the reference stable (see the previous discussion of REF_{IN}). For applications that use an external reference source, the internal reference can be disabled using bit RP in the SDI Register (see the *Digital* section). The settling time of the REF_{OUT} pin is 500µs (max) with the reference capacitor connected. The default value of the REF_{OUT} pin after power-up is 2.5V.

For operation with a 2.7V analog supply and a 2.5V reference, the internal reference buffer requires a rail-to-rail input and output. Such buffers typically contain two input stages; when the input voltage passes the mid-range area, a transition occurs at the output because of switching between the two input stages. In this voltage range, rail-to-rail amplifiers generally show a very poor power-supply rejection.

As a result of this poor performance, the ADS7865 buffer has a fixed transition at DAC code 509 (0x1FD). At this code, the DAC may show a jump of up to 10mV in its transfer function.

Table 3 lists some examples of internal reference DAC settings.

Table 3. Reference DAC Setting Examples

V_{REFOUT}	DECIMAL CODE	BINARY CODE	HEXADECIMAL CODE
0.500V	205	00 1100 1101	CD
1.241V	508	01 1111 1100	1FC
1.240V	509	01 1111 1101	1FD
2.500V	1023	11 1111 1111	3FF

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DIGITAL

This section reviews the timing and control of the ADS7865 parallel interface.

Configuration Register

The configuration register can be set by issuing a write access on the parallel interface. The data present on DB[11:0] are latched with the rising edge of $\overline{WR}$. The data word width of the configuration register is 12 bits; its structure is shown in Table 4. The default value of this register after power-up is 0x000.

Table 4. Configuration Register Map

CONFIGURATION REGISTER BIT											
11	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
C1	C0	R1	R0	DP	N	AN	RP	X(1)	A2	A1	A0

(1) X = Don't care.

Table 5. C1 and C0: Channel Selection

		ADC A/B	
C1	**C0**	**POSITIVE INPUT**	**NEGATIVE INPUT**
0	0	CHA0+/CHB0+	CHA0–/CHB0–
0	1	CHA1–/CHB1–	CHA0–/CHB0–
1	0	CHA1+/CHB1+	CHA0–/CHB0–
1	1	CHA1+/CHB1+	CHA1–/CHB1–

Table 6. R1 and R0: Register Update Enable

R1	R0	FUNCTION
0	0	Register update disabled
0	1	Register update enabled
1	0	Reserved for factory test (don't use)
1	1	Register update disabled

DP: Deep power-down enable
('1' = device in deep power-down mode)

N: Nap power-down enable
('1' = device in nap power-down mode)

AN: AutoNap power-down enable
('1' = device in autonap power-down mode)

RP: Reference power-down
('1' = reference is turned off)

Table 7. A2, A1, and A0: DAC, Sequencer, and SW-Reset Control

A2	A1	A0	FUNCTION
0	0	0	Configuration register update only
0	0	1	Write to reference DAC register with next access
0	1	0	Configuration register update only
0	1	1	Read from reference DAC register with next access
1	0	0	Write to sequencer register
1	0	1	Device SW-reset
1	1	0	Read from sequencer register
1	1	1	Configuration register update only

All enabled power-down features are activated by the rising edge of the $\overline{WR}$ pulse immediately after writing to the configuration register.

Because two write accesses are required to program the reference DAC and the sequencer registers, these settings are updated with the rising edge of $\overline{WR}$ after the second write access. For more details, see the *Sequencer Register* and *Programming the Reference DAC* sections.

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Figure 32 shows a complete timing diagram consisting of a write access to set up the proper input channel, followed by an initiation of a conversion and the read access of both conversion results.

The input multiplexer updates with the rising edge of the $\overline{WR}$ input. The following falling edge of CONVST triggers the conversion of the previously selected channel. The data output register then updates with the falling edge of BUSY and can be read thereafter.

The digital output code format of the ADS7865 is in binary twos complement, as shown in Table 8. Conversion results can be read out only once. A second read access (without issuing a new conversion) results in 000h as the output value.

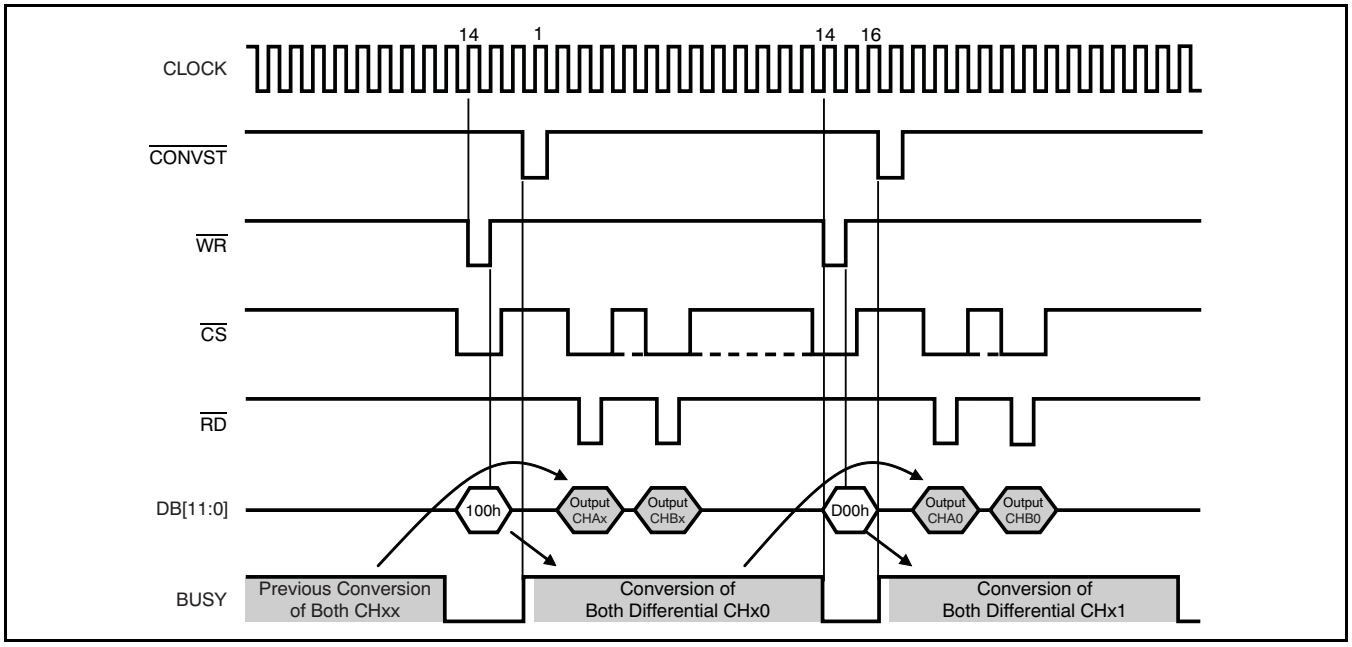

Figure 32. Channel Selection Timing Diagram

Table 8. ADS7865 Output Data Format

DESCRIPTION	DIFFERENTIAL INPUT VOLTAGE (CHXX+) – (CHXX–)	INPUT VOLTAGE AT CHXX+ (CHXX– = V_{REF} = 2.5V)	BINARY CODE	HEXADECIMAL CODE
Positive full-scale	V_{REF}	5V	0111 1111 1111	7FF
Midscale	0V	2.5V	0000 0000 0000	000
Midscale – 1LSB	$-V_{REF}/4096$	2.49878V	1111 1111 1111	FFF
Negative full-scale	$-V_{REF}$	0V	1000 0000 0000	800

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Sequencer Register

The ADS7865 features a programmable sequencer that controls the switching of the ADC input multiplexer. To set up the sequencer, two write accesses to the ADC are required. During the first write access, the programming of the sequencer must be enabled by setting R[1:0] = '01' and A[2:0] = '100' in the Configuration Register. The data applied to the data bus on the second write access contain the updated Sequencer Register content.

The structure of the Sequencer Register is shown in Table 9. The default value of this register after power-up is 0x000.

Detailed timing diagrams of the different sequencer modes are shown in Figure 33.

If the output data are read after the entire sequence has been converted, the output data are presented in *LIFO* manner (last in, first out); that is, the conversion results of ADC A is followed by ADC B data of the last channel in the sequence, followed by the ADC A/B data of the second-last channel in the sequence, and so on. Trying to read out more results (2, 4, or 6) than the actual sequence length results in 000h at the output of the converter. Older conversion results are overwritten if all data of a completed sequence have not been read out before issuing a new conversion start. Figure 34 shows an example where the sequencer is set to scan through the pseudo-differential inputs of the ADS7865 beginning with CHx1+, followed by CHx1– and CHx0+, while using a single $\overline{\text{CONVST}}$ and BUSY for the entire sequence. The internal LIFO pointer is reset with every BUSY signal rising edge. Therefore, to ensure proper data retrieval, the sequence results should either be read after completion of the entire sequence conversion or between two consecutive conversions within the sequence as indicated in Figure 34. Other read options may deliver incorrect results.

Table 9. Sequencer Register Map

SEQUENCER REGISTER BIT											
11	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
S1	S0	SL1	SL0	CH1	CM1	CH2	CM2	CH3	CM3	SP1	SP0

Table 10. S1 and S0: Sequencer Mode

S1	S0	FUNCTION
0	X	Individual $\overline{\text{CONVST}}$ and BUSY for each conversion
1	0	Single $\overline{\text{CONVST}}$ for entire sequence and individual BUSY for each conversion
1	1	Single $\overline{\text{CONVST}}$ and BUSY for entire sequence

Table 11. SL1 and SL0: Sequence Length

SL1	SL0	FUNCTION
0	0	Length = 0: Sequencer disabled
0	1	Length = 1: Cx1 (bits 6/7) enabled
1	0	Length = 2: Cx1 (bits 6/7) and Cx2 (bits 4/5) enabled
1	1	Length = 3: Cx1 (bits 6/7), Cx2 (bits 4/5), and Cx3 (bits 2/3) enabled

CH1: Signal input of the first channel in sequence; refer to Table 12 for details.

CM1: Common-mode input of the first channel in sequence; refer to Table 12 for details.

CH2: Signal input of the second channel in sequence; refer to Table 12 for details.

CM2: Common-mode input of the second channel in sequence; refer to Table 12 for details.

CH3: Signal input of the third channel in sequence; refer to Table 12 for details.

CM3: Common-mode input of the third channel in sequence; refer to Table 12 for details.

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Table 12. Channel Selection

CHx	CMx	ADC A/B	
		SIGNAL INPUT	COMMON-MODE INPUT
0	0	CHA0+/CHB0+	CHA0–/CHB0–
0	1	CHA1–/CHB1–	CHA0–/CHB0–
1	0	CHA1+/CHB1+	CHA0–/CHB0–
1	1	CHA1+/CHB1+	CHA1–/CHB1–

Table 13. SP1 and SP0: Sequence Position (Read-Only)

SP1	SP0	FUNCTION
0	0	Sequencer disabled
0	1	CH1/CM1 (bits 6/7) to be converted at next falling edge of $\overline{\text{CONVST}}$
1	0	CH2/CM2 (bits 4/5) to be converted at next falling edge of $\overline{\text{CONVST}}$
1	1	CH3/CM3 (bits 2/3) to be converted at next falling edge of $\overline{\text{CONVST}}$

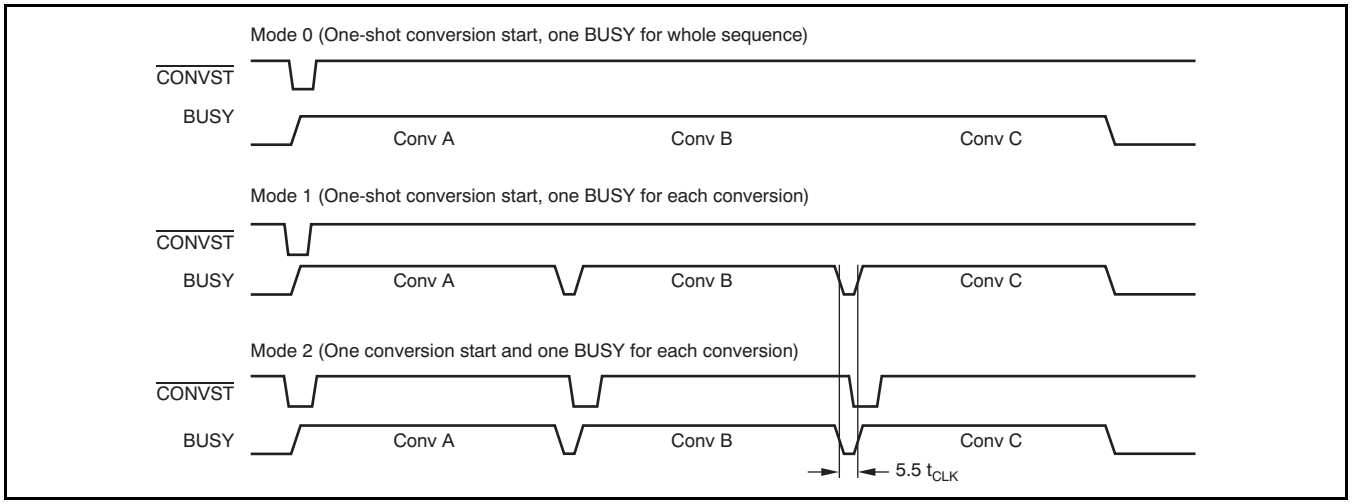

Figure 33. Sequencer Modes (Example: SL = '11')

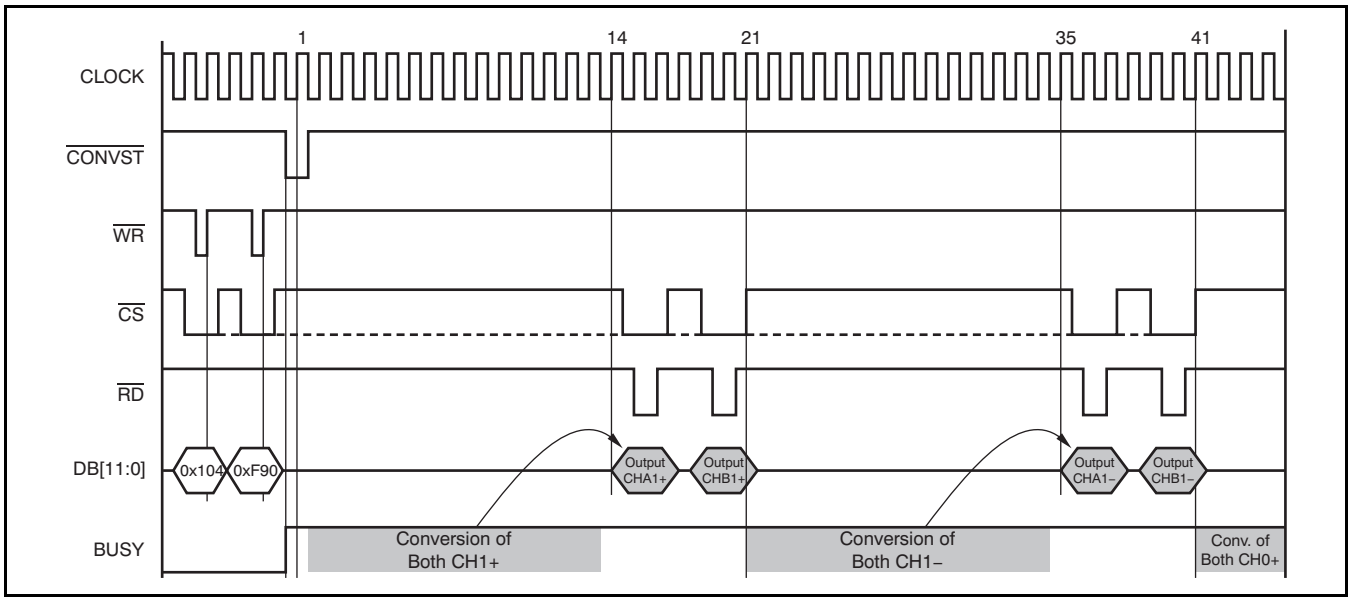

Figure 34. Sequencer Programming Example

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Programming the Reference DAC

The internal reference DAC can be set by issuing a $\overline{WR}$ pulse while providing a control word with R[1:0] = '01' and A[2:0] = '001' (see Table 4). Thereafter, a second $\overline{WR}$ pulse must be generated with the data bus bits DB[11:10] = '00' and DB[9:0] containing the actual 10-bit DAC value, with DB9 being the MSB (see Figure 35).

To verify the current DAC setting, a $\overline{WR}$ pulse must be generated while providing a control word containing R[1:0] = '01' and A[2:0] = '011' to initialize the DAC read access. Thereafter, triggering the $\overline{RD}$ line causes the data bus to provide the 10-bit DAC value on DB[9:0].

Table 14 shows the content of this register; the default value after power-up is 0x3FF (see also Table 3).

Table 14. DAC Register Contents

DAC REGISTER CONTENT											
11	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	MSB	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

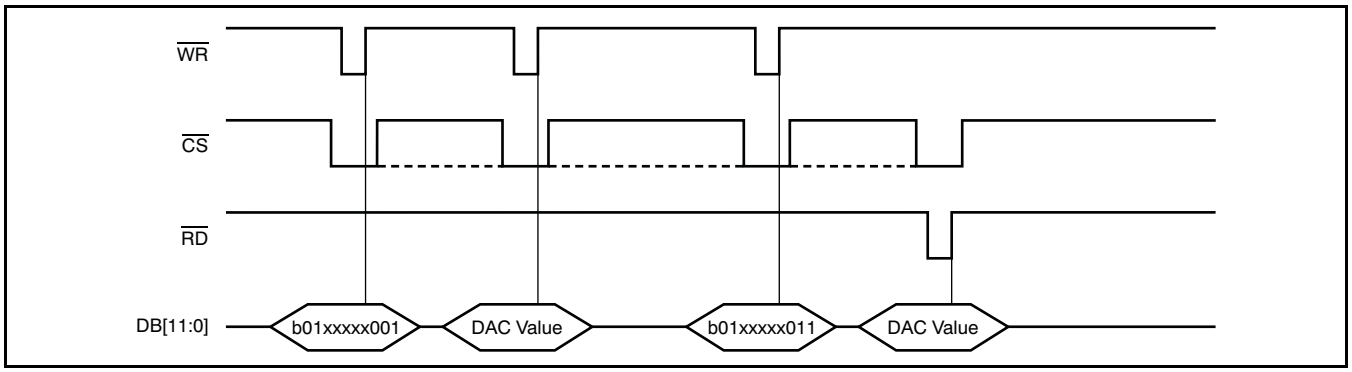

Figure 35. DAC Write and Read Access Timing Diagram

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Power-Down Modes and Reset

The ADS7865 has a comprehensive built-in power-down feature. There are three power-down modes: deep power-down, nap power-down, and auto-nap power-down. All three power-down modes are activated with the rising $\overline{WR}$ edge after having been activated by asserting the corresponding bit in the Configuration Register (DP = '1', N = '1', or AN = '1'). All modes are deactivated by de-asserting the respective bit in the Configuration Register. The contents of the Configuration Register are not affected by any of the power-down modes. Any ongoing conversion aborts when deep or nap power-down is initiated. Table 15 lists the differences among the three power-down modes.

In ***deep power-down mode,*** all functional blocks except the digital interface are disabled. The analog block has its bias currents turned off. In this mode, the power dissipation reduces to 1µA within 2µs. The wake-up time from deep power-down mode is 1µs.

In ***nap power-down mode,*** the ADS7865 turns off the biasing of the comparator and the mid-voltage buffer within 200ns. The device goes into nap power-down mode regardless of the conversion state.

The ***auto-nap power-down mode*** is very similar to the nap mode. The only differences are the methods of powering down and waking up the device. The Configuration Register bit AN is only used to enable/disable this feature. If the auto-nap mode is enabled, the ADS7865 turns off the biasing automatically after finishing a conversion; thus, the end of conversion actually activates the auto-nap power-down. The device powers down within 200ns in this mode, as well. Triggering a new conversion by applying a $\overline{CONVST}$ pulse returns the device to normal operation and automatically starts a new conversion six CLOCK cycles later. Therefore, a complete conversion cycle takes 22 CLOCK cycles; thus, the maximum throughput rate in auto-nap power-down mode is reduced to 1.45MSPS.

To issue a ***device reset***, a write access to the Configuration Register must be generated to set A[2:0] = '101'. With the rising edge of the $\overline{WR}$ input, the entire device is forced into reset. After approximately 20ns, the parallel interface becomes active again.

Table 15. Power-Down Modes

POWER-DOWN TYPE	ENABLED BY	ACTIVATED BY	ACTIVATION TIME	RESUMED BY	REACTIVATION TIME	DISABLED BY
Deep	DP = '1'	Rising $\overline{WR}$ edge	2µs	DP = '0'	1µs	DP = '0'
Nap	N = '1'	Rising $\overline{WR}$ edge	200ns	N = '0'	6 clocks	N = '0'
Auto-nap	AN = '1'	Each end of conversion	200ns	$\overline{CONVST}$ pulse	6 clocks	AN = '0'

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ADS7862 COMPATIBILITY

The ADS7865IPBS is pin-compatible with the ADS7862Y. However, there are some differences between the two devices that must be considered when migrating from the ADS7862 to the ADS7865 in an existing design.

$\overline{WR}$ versus A0

One of the differences is that pin 22, which triggers writing to the internal Configuration Register of the ADS7865 ($\overline{WR}$), is used to select the input channel on the ADS7862 (A0).

Channel selection on the ADS7865 can only be performed by setting bits C[1:0] in the Configuration Register or, automatically, by the sequencer (see the *Sequencer Register* section for details).

REF_{IN}

The ADS7865 offers an unbuffered REF_{IN} input with a code-dependent input impedance while featuring a programmable and buffered reference output (REF_{OUT}). The ADS7862 offers a high-impedance (buffered) reference input. If an existing ADS7862-based design uses the internal reference of the device and relies on an external resistor divider to adjust the input voltage range of the ADC, migration to the ADS7865 platform requires one of the following conditions:

- A software change to set up the internal reference DAC properly via the DAC register while removing the external resistors; ***or***
- An additional external buffer between the resistor divider and the required 470nF (minimum) capacitor on the REF_{IN} input.

In the latter case, while the capacitor stabilizes the reference voltage during the entire conversion, the buffer must recharge it by providing an average current only; thus, the required minimum bandwidth of the buffer can be calculated using Equation 2:

$$f_{-3dB} = \frac{\ln(2) \times 2}{2\pi \times 16 \times t_{CLK}} \quad (2)$$

The buffer must also be capable of driving the 470nF load while maintaining its stability.

Timing

The only timing requirement that may cause the ADS7865 to malfunction in an existing ADS7862-based design is the $\overline{CONVST}$ low time (t_1) which is specified to be 20ns minimum, while the ADS7862 works properly with a pulse as short as 15ns. All other required minimum setup and hold times are specified to be either the same as or lower than the ADS7865; therefore, there are no conflicts with the ADS7862 requirements.

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APPLICATION INFORMATION

The absolute minimum configuration of the ADS7865 in an application is shown in Figure 36. In this case, the ADS7865 is used in dual-channel mode only, with the default settings of the device after power up.

The input signal for the amplifiers must fulfill the common-mode voltage requirements of the ADS7865 in this configuration. The actual values of the resistors and capacitors depend on the bandwidth and performance requirements of the application.

Those values can be calculated using Equation 3, with *n* = 12 being the resolution of the ADS7865.

$$f_{FILTER} = \frac{\ln(2) \times (n + 1)}{2 \times \pi \times 2 \times R \times C} \quad (3)$$

It is recommended to use a capacitor value of at least 20pF.

Keep the acquisition time in mind; the resistor value can be calculated as shown in Equation 4 for each of the series resistors (with *n* = 12, the resolution of the ADS7865).

$$R = \frac{t_{ACQ}}{\ln(2) \times (n + 1) \times 2 \times C} \quad (4)$$

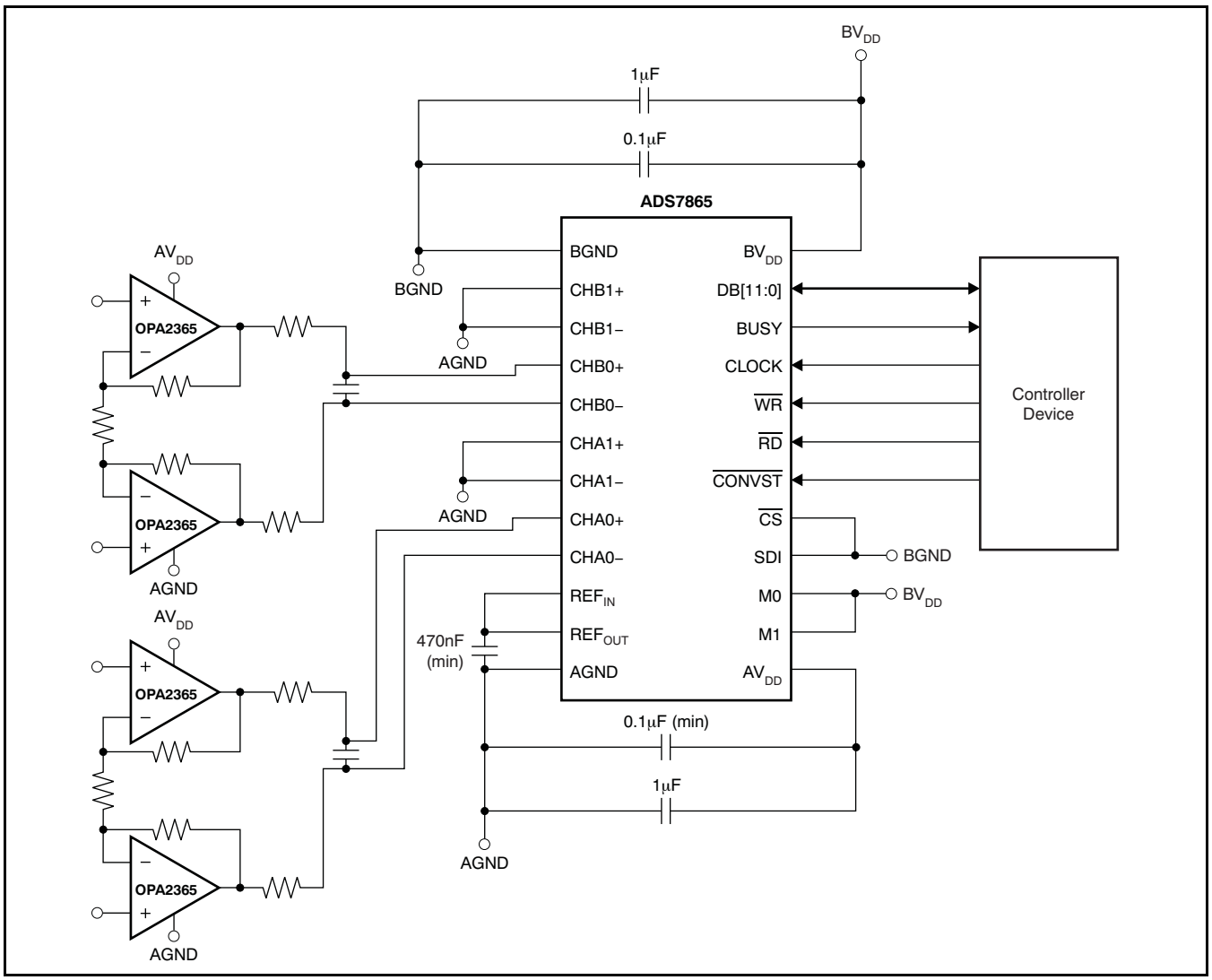

Figure 36. Minimum ADS7865 Configuration

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LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS7865 circuitry. This caution is particularly true if the CLOCK input approaches the maximum throughput rate. In this case, it is recommended to have a fixed phase relationship between CLOCK and $\overline{\text{CONVST}}$.

Additionally, the basic SAR architecture is quite sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just before latching the output of the analog comparator. Therefore, when driving any single conversion for an *n*-bit SAR converter, there are *n* windows in which large external transient voltages can affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, or high-power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. These errors can change if the external event also changes in time with respect to the CLOCK input.

With this possibility in mind, power to the ADS7865 should be clean and well-bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1µF to 10µF capacitor is recommended. If needed, an even larger capacitor and a 5Ω or 10Ω series resistor may be used to low-pass filter a noisy supply.

If the reference voltage is external and originates from an operational amplifier, be sure that it can drive the reference capacitor without oscillation. The connection between the output of the external reference driver and REF_{IN} should be of low resistance (10Ω max) to minimize any code-dependent voltage drop on this path.

Grounding

All ground (AGND and BGND) pins should be connected to a clean ground reference. These connections should be kept as short as possible to minimize the inductance of these paths. It is recommended to use vias connecting the pads directly to the ground plane. In designs without ground planes, the ground trace should be kept as wide as possible. Avoid connections that are too near the grounding point of a microcontroller or digital signal processor.

Depending on the circuit density of the board, placement of the analog and digital components, and the related current loops, a single solid ground plane for the entire printed circuit board (PCB) or a dedicated analog ground area may be used. In an instance of a separated analog ground area, ensure a low-impedance connection between the analog and digital ground of the ADC by placing a bridge underneath (or next to) the ADC. Otherwise, even short undershoots on the digital interface with a value lower than –300mV may lead to conduction of ESD diodes, causing current flow through the substrate and degrading the analog performance.

During the PCB layout process, care should also be taken to avoid any return currents crossing any sensitive analog areas or signals. No signal must exceed the limit of –300mV with regard to the respective ground plane. Figure 37 illustrates the recommended layout of the ground and power-supply connections.

Supply

The ADS7865 has two separate supplies: the BV_{DD} pin for the digital interface and the AV_{DD} pin for all remaining circuits.

BV_{DD} can range from 2.7V to 5.5V, allowing the ADS7865 to easily interface with processors and controllers. To limit the injection of noise energy from external digital circuitry, BV_{DD} should be filtered properly. Bypass capacitors of 0.1µF and 10µF should be placed between the BV_{DD} pin and the ground plane.

AV_{DD} supplies the internal analog circuitry. For optimum performance, a linear regulator (for example, the UA7805 family) is recommended to generate the analog supply voltage in the range of 2.7V to 5.5V for the ADS7865 and the necessary analog front-end circuitry.

Bypass capacitors should be connected to the ground plane such that the current is allowed to flow through the pad of the capacitor (that is, the vias should be placed on the opposite side of the connection between the capacitor and the power-supply pin of the ADC).

Digital Interface

To further optimize device performance, a series resistor of 10Ω to 100Ω can be used on each digital pin of the ADS7865. In this way, the slew rates of the input and output signals are reduced, limiting the noise injection from the digital interface.

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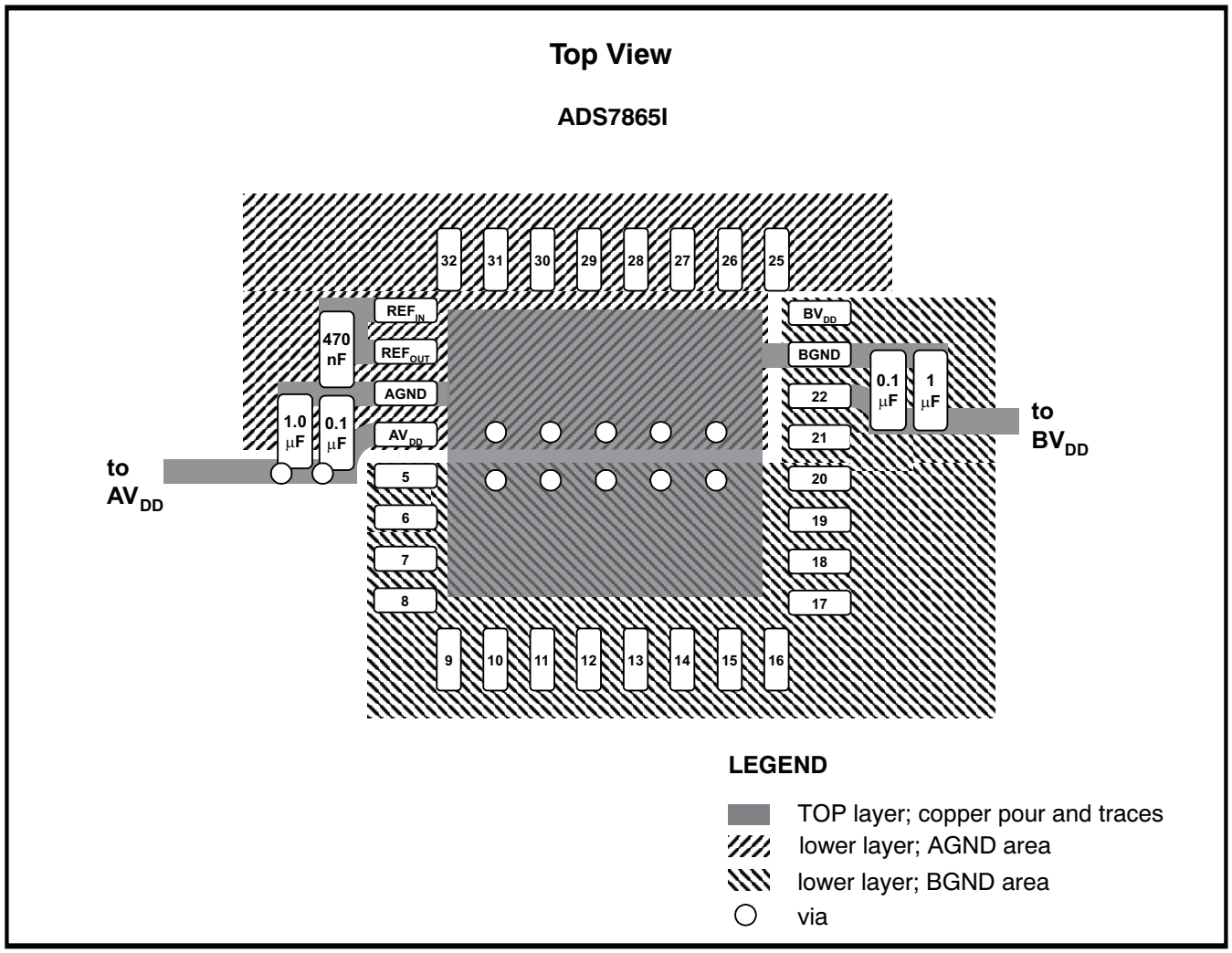

Figure 37. Optimized Layout Recommendation

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2010) to Revision C **Page**

- Deleted Ordering Information table 2

Changes from Revision A (June 2009) to Revision B **Page**

- Deleted footnote 2 from Electrical Characteristics table 3
- Changed *RESET* section of *Applications Information* 16
- Added last sentence in final paragraph of the *Configuration Register* section 18
- Changed last paragraph of *Sequencer Register* section 19
- Updated Figure 33 20
- Updated Figure 34 20

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7865IPBS	ACTIVE	TQFP	PBS	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7865I A	Samples
ADS7865IPBSG4	ACTIVE	TQFP	PBS	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7865I A	Samples
ADS7865IPBSR	ACTIVE	TQFP	PBS	32	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7865I A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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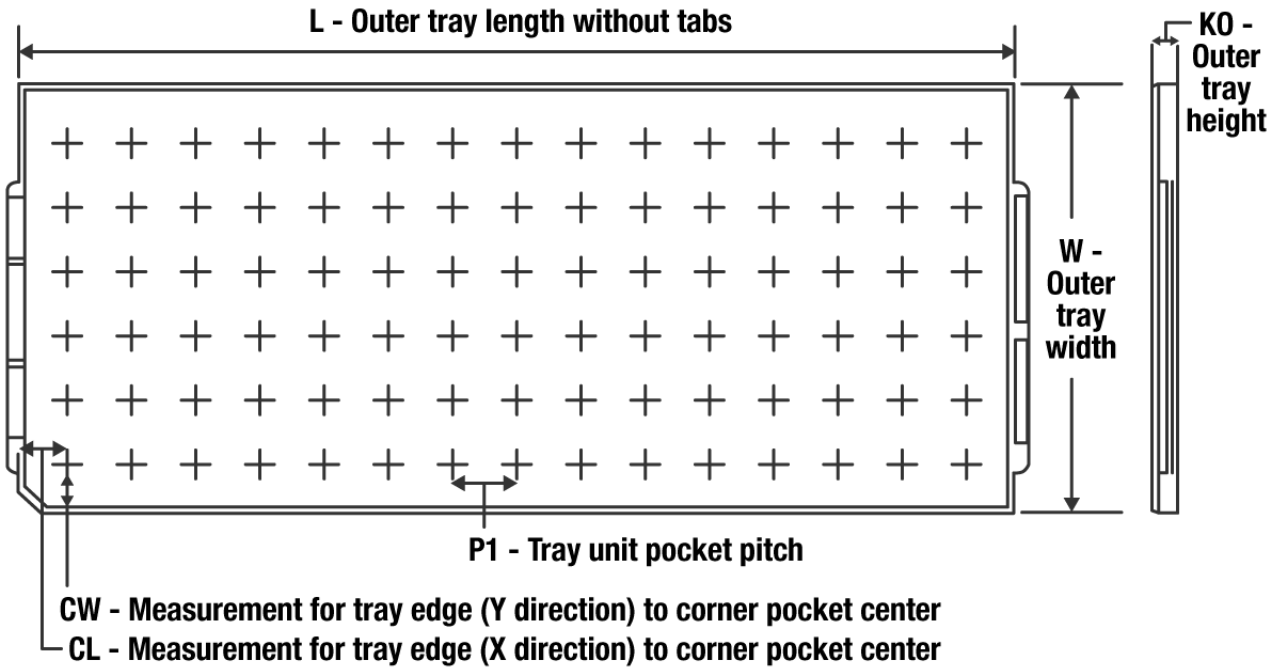
TRAY

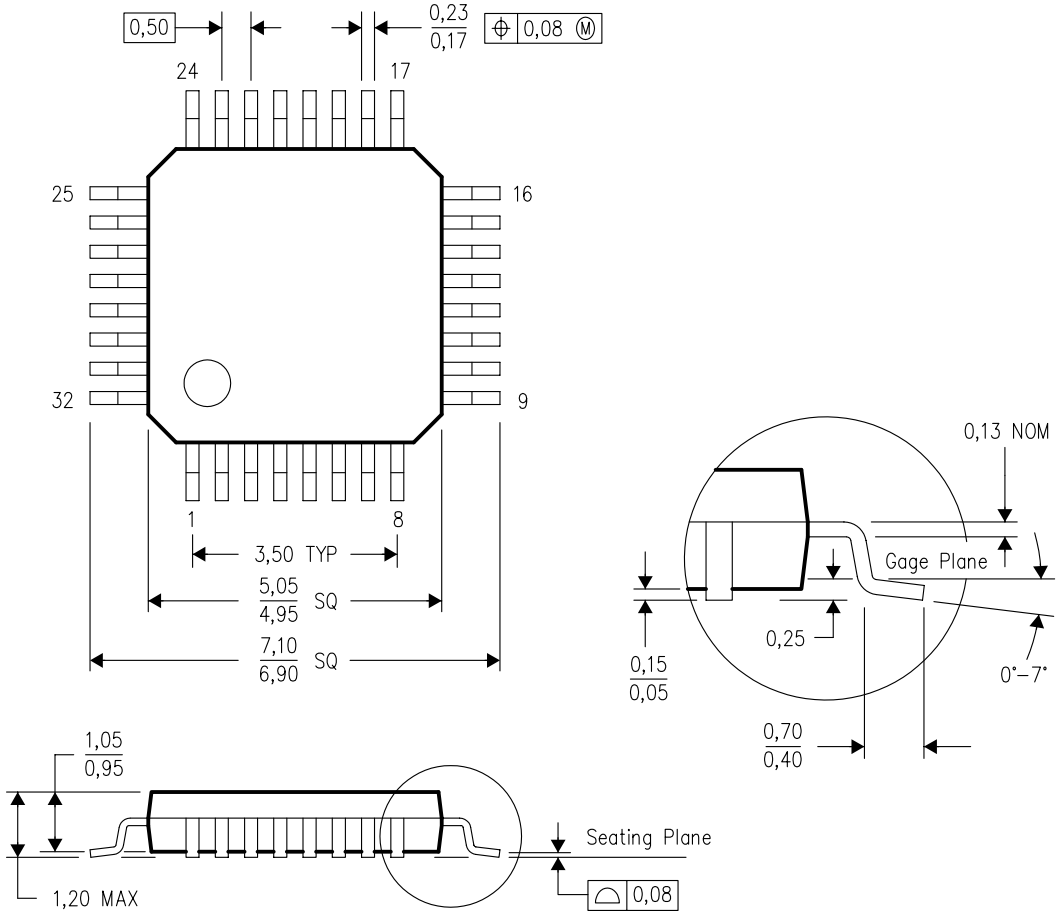


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADS7865IPBS	PBS	TQFP	32	250	10 X 25	150	315	135.9	7620	12.2	11.1	11.25
ADS7865IPBSG4	PBS	TQFP	32	250	10 X 25	150	315	135.9	7620	12.2	11.1	11.25

PBS (S–PQFP–G32) PLASTIC QUAD FLATPACK



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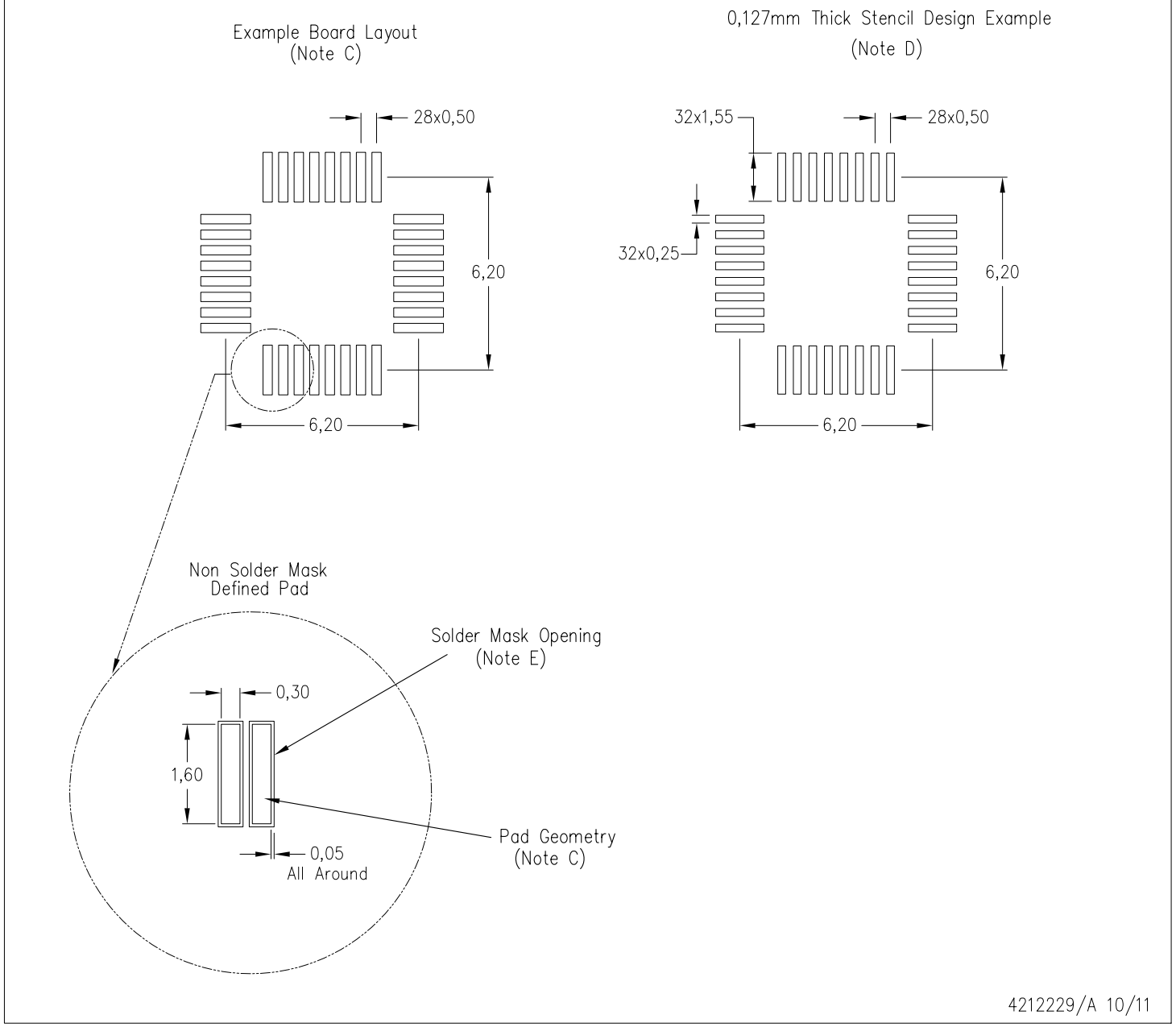
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

PBS (S–PQFP–G32) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances between and around signal pads.

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