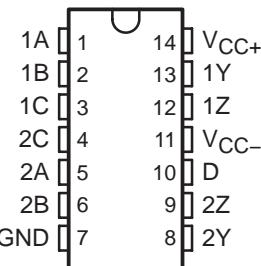


- Improved Stability Over Supply Voltage and Temperature Ranges
- Constant-Current Outputs
- High Speed
- Standard Supply Voltages
- High Output Impedance
- High Common-Mode Output Voltage Range . . . –3 V to 10 V
- TTL-Input Compatibility
- Inhibitor Available for Driver Selection
- Glitch Free During Power Up/Power Down
- SN75112 and External Circuit Meets or Exceeds the Requirements of CCITT Recommendation V.35

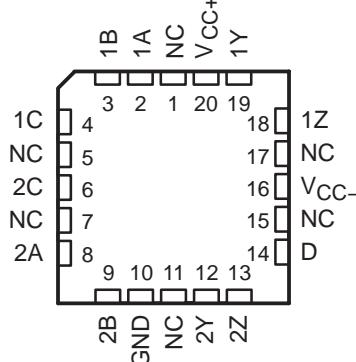
## description/ordering information

The SN55110A, SN75110A, and SN75112 dual line drivers have improved output current regulation with supply-voltage and temperature variations. In addition, the higher current of the SN75112 (27 mA) allows data to be transmitted over longer lines. These drivers offer optimum performance when used with the SN55107A, SN75107A, and SN75108A line receivers.

SN55110A . . . J OR W PACKAGE  
SN75110A . . . D, N, OR NS PACKAGE  
SN75112 . . . D OR N PACKAGE  
(TOP VIEW)



SN55110A . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## ORDERING INFORMATION

| TA             | PACKAGE†  |              | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-----------|--------------|-----------------------|------------------|
| 0°C to 70°C    | PDIP (N)  | Tube of 25   | SN75110AN             | SN75110AN        |
|                |           |              | SN75112N              | SN75112N         |
|                |           | Tube of 50   | SN75110AD             | SN75110A         |
|                |           | Reel of 2500 | SN75110ADR            |                  |
|                |           | Tube of 50   | SN75112D              | SN75112          |
|                | SOIC (D)  | Reel of 2500 | SN75112DR             |                  |
|                |           | Reel of 2000 | SN75110ANSR           | SN75110A         |
|                |           | CDIP (J)     | SN55110AJ             | SN55110AJ        |
|                |           |              | SNJ55110AJ            | SNJ55110AJ       |
|                |           | CFP (W)      | SNJ55110AW            | SNJ55110AW       |
| –55°C to 125°C | LCCC (FK) | Tube of 55   | SNJ55110AFK           | SNJ55110AFK      |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN55110A, SN75110A, SN75112 DUAL LINE DRIVERS

SLLS106G – DECEMBER 1975 – REVISED NOVEMBER 2004

## description/ordering information (continued)

These drivers feature independent channels with common voltage supply and ground terminals. The significant difference between the three drivers is in the output-current specification. The driver circuits feature a constant output current that is switched to either of two output terminals by the appropriate logic levels at the input terminals. The output current can be switched off (inhibited) by low logic levels on the enable inputs. The output current nominally is 12 mA for the '110A devices and is 27 mA for the SN75112.

The enable/inhibit feature is provided so the circuits can be used in party-line or data-bus applications. A strobe or inhibitor (enable D), common to both drivers, is included for increased driver-logic versatility. The output current in the inhibited mode,  $I_{O(off)}$ , is specified so that minimum line loading is induced when the driver is used in a party-line system with other drivers. The output impedance of the driver in the inhibited mode is very high. The output impedance of a transistor is biased to cutoff.

The driver outputs have a common-mode voltage range of –3 V to 10 V, allowing common-mode voltage on the line without affecting driver performance.

All inputs are diode clamped and are designed to satisfy TTL-system requirements. The inputs are tested at 2 V for high-logic-level input conditions and 0.8 V for low-logic-level input conditions. These tests ensure 400-mV noise margin when interfaced with TTL Series 54/74 devices.

The SN55110A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN75110A and SN75112 are characterized for operation from 0°C to 70°C.

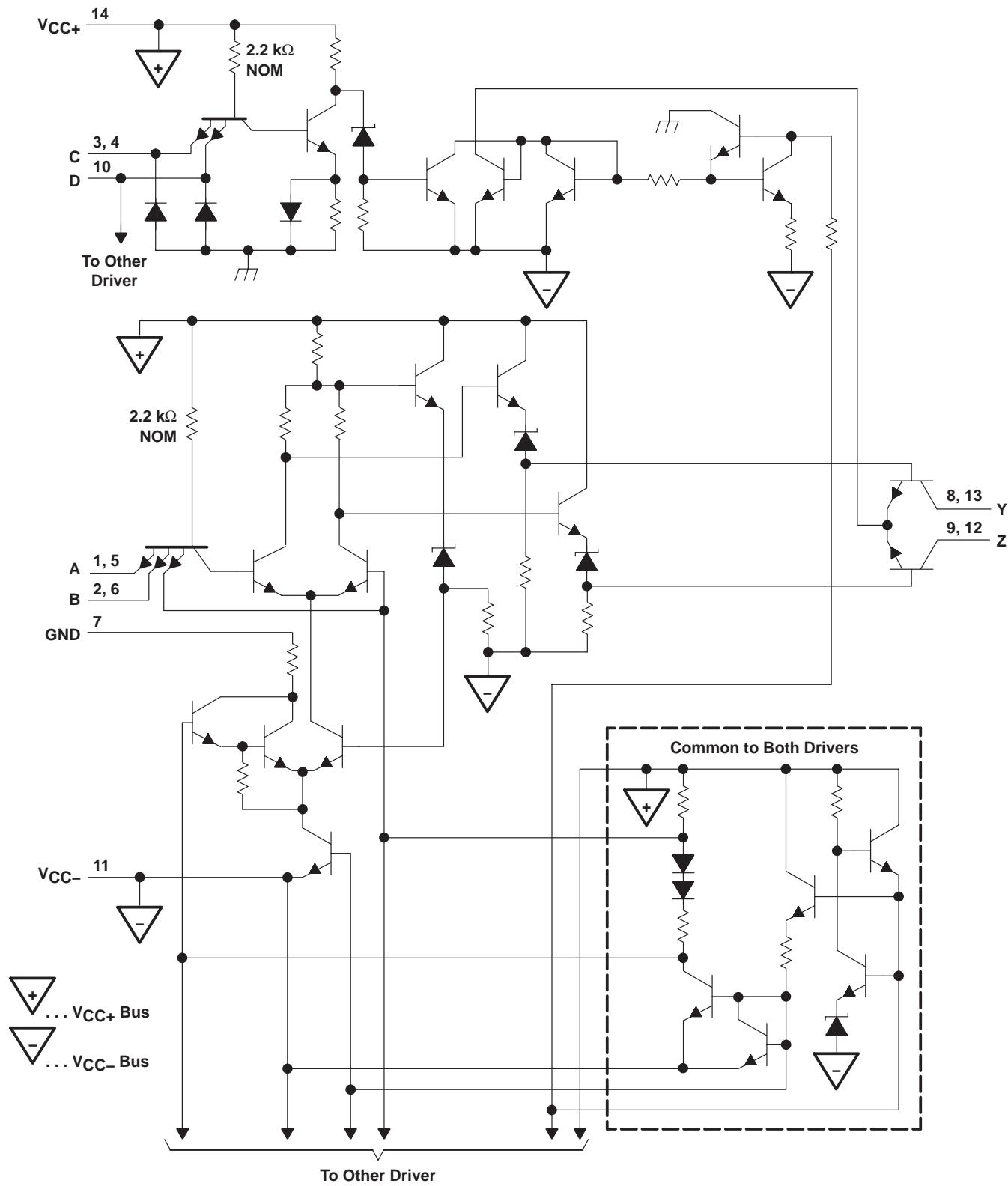
FUNCTION TABLE  
(each driver)

| LOGIC INPUTS |   | ENABLE INPUTS |   | OUTPUTS <sup>†</sup> |     |
|--------------|---|---------------|---|----------------------|-----|
| A            | B | C             | D | Y                    | Z   |
| X            | X | L             | X | Off                  | Off |
| X            | X | X             | L | Off                  | Off |
| L            | X | H             | H | On                   | Off |
| X            | L | H             | H | On                   | Off |
| H            | H | H             | H | Off                  | On  |

H = high level, L = low level, X = irrelevant

† When using only one channel of the line drivers,  
the other channel should be inhibited and/or have  
its outputs grounded.

schematic (each driver)



Pin numbers shown are for the D, J, N, NS, and W packages.

# SN55110A, SN75110A, SN75112 DUAL LINE DRIVERS

SLLS106G – DECEMBER 1975 – REVISED NOVEMBER 2004

## absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>

|  |                |
|--|----------------|
| Supply voltage: $V_{CC+}$ (see Note 1) .....                                       | 7 V            |
| $V_{CC-}$ (see Note 1) .....   | -7 V           |
| Input voltage, $V_I$ .....   | 5.5 V          |
| Output voltage range, $V_O$ .....  | -5 V to 12 V   |
| Package thermal impedance, $\theta_{JA}$ (see Notes 2 and 3): D package .....      | 86°C/W         |
| N package .....  | 80°C/W         |
| NS package .....   | 76°C/W         |
| Package thermal impedance, $\theta_{JC}$ (see Notes 4 and 5): FK package .....     | 13.42°C/W      |
| J package .....  | 15.05°C/W      |
| W package .....  | 14.65°C/W      |
| Operating virtual junction temperature .....                                       | 150°C          |
| Case temperature for 60 seconds: FK package .....                                  | 260°C          |
| Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds: J or W package ..... | 300°C          |
| Storage temperature range, $T_{stg}$ .....   | -65°C to 150°C |

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.

2. Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(max) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JC}$ , and  $T_C$ . The maximum allowable power dissipation at any allowable case temperature is  $P_D = (T_J(max) - T_C)/\theta_{JC}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
5. The package thermal impedance is calculated in accordance with MIL-STD-883.

## recommended operating conditions (see Note 6)

|                                      | SN55110A |     |      | SN75110A<br>SN75112 |     |       | UNIT |
|--------------------------------------|----------|-----|------|---------------------|-----|-------|------|
|                                      | MIN      | NOM | MAX  | MIN                 | NOM | MAX   |      |
| $V_{CC+}$ Supply voltage             | 4.5      | 5   | 5.5  | 4.75                | 5   | 5.25  | V    |
| $V_{CC-}$ Supply voltage             | -4.5     | -5  | -5.5 | -4.75               | -5  | -5.25 | V    |
| Positive common-mode output voltage  | 0        | 10  | 0    | 0                   | 10  | 0     | V    |
| Negative common-mode output voltage  | 0        | -3  | 0    | 0                   | -3  | 0     | V    |
| $V_{IH}$ High-level input voltage    | 2        |     |      | 2                   |     |       | V    |
| $V_{IL}$ Low-level output voltage    |          |     | 0.8  |                     |     | 0.8   | V    |
| $T_A$ Operating free-air temperature | -55      | 125 | 0    | 0                   | 70  | 0     | °C   |

NOTE 6: When using only one channel of the line drivers, the other channel should be inhibited and/or have its outputs grounded.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER             | TEST CONDITIONS <sup>†</sup>                          | SN55110A<br>SN75110A  |                  |      | SN75112 |                  |     | UNIT          |
|-----------------------|---|---|------------------|------|---------|------------------|-----|---------------|
|                       |   | MIN   | TYP <sup>‡</sup> | MAX  | MIN     | TYP <sup>‡</sup> | MAX |               |
| $V_{IK}$              | Input clamp voltage                                   | $V_{CC\pm} = \text{MIN}$ , $I_L = -12 \text{ mA}$   | -0.9             | -1.5 | -0.9    | -1.5             | -   | V             |
| $I_{O(\text{on})}$    | On-state output current                               | $V_{CC\pm} = \text{MAX}$ , $V_O = 10 \text{ V}$   | 12               | 15   | 27      | 40               | -   | mA            |
|                       |   | $V_{CC} = \text{MIN to MAX}$ ,<br>$V_O = -1 \text{ V to } 1 \text{ V}$ , $T_A = 25^\circ\text{C}$ | -                | -    | 24      | 28               | 32  |               |
|                       |   | $V_{CC\pm} = \text{MIN}$ , $V_O = -3 \text{ V}$   | 6.5              | 12   | 15      | 27               | -   |               |
| $I_{O(\text{off})}$   | Off-state output current                              | $V_{CC\pm} = \text{MIN}$ , $V_O = 10 \text{ V}$   | -                | 100  | -       | 100              | -   | $\mu\text{A}$ |
| $I_I$                 | Input current at maximum input voltage                | $V_{CC\pm} = \text{MAX}$ , $V_I = 5.5 \text{ V}$  | -                | 1    | -       | 1                | -   | mA            |
|                       | D input   |   | -                | 2    | -       | 2                | -   |               |
| $I_{IH}$              | High-level input current                              | $V_{CC\pm} = \text{MAX}$ , $V_I = 2.4 \text{ V}$  | -                | 40   | -       | 40               | -   | $\mu\text{A}$ |
|                       | D input   |   | -                | 80   | -       | 80               | -   |               |
| $I_{IL}$              | Low-level input current                               | $V_{CC\pm} = \text{MAX}$ , $V_I = 0.4 \text{ V}$  | -                | -3   | -       | -3               | -   | mA            |
|                       | D input   |   | -                | -6   | -       | -6               | -   |               |
| $I_{CC+(\text{on})}$  | Supply current from $V_{CC}$ with driver enabled      | $V_{CC\pm} = \text{MAX}$ ,<br>A and B inputs at 0.4 V,<br>C and D inputs at 2 V                   | 23               | 35   | 25      | 40               | -   | mA            |
| $I_{CC-(\text{on})}$  | Supply current from $V_{CC-}$ with driver enabled     | $V_{CC\pm} = \text{MAX}$ ,<br>A and B inputs at 0.4 V,<br>C and D inputs at 2 V                   | -34              | -50  | -65     | -100             | -   | mA            |
| $I_{CC+(\text{off})}$ | Supply current from $V_{CC-}$ with driver inhibited   | $V_{CC\pm} = \text{MAX}$ ,<br>A, B, C, and D inputs at 0.4 V                                      | 21               | -    | 30      | -                | -   | mA            |
| $I_{CC-(\text{off})}$ | Supply current from $V_{CC\pm}$ with driver inhibited | $V_{CC\pm} = \text{MAX}$ ,<br>A, B, C, and D inputs at 0.4 V                                      | -17              | -    | -32     | -                | -   | mA            |

<sup>†</sup> For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at  $V_{CC+} = 5 \text{ V}$ ,  $V_{CC-} = -5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

### switching characteristics, $V_{CC\pm} = \pm 5 \text{ V}$ , $T_A = 25^\circ\text{C}$ (see Figure 1)

| PARAMETER <sup>§</sup> | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS                             | MIN | TYP | MAX | UNIT |
|------------------------|--------------|-------------|---|-----|-----|-----|------|
| $t_{PLH}$              | A or B       | Y or Z      | $C_L = 40 \text{ pF}$ , $R_L = 50 \Omega$ , | 9   | 15  | -   | ns   |
| $t_{PHL}$              |              |             |   | 9   | 15  | -   |      |
| $t_{PLH}$              | C or D       | Y or Z      | $C_L = 40 \text{ pF}$ , $R_L = 50 \Omega$ , | 16  | 25  | -   | ns   |
| $t_{PHL}$              |              |             |   | 13  | 25  | -   |      |

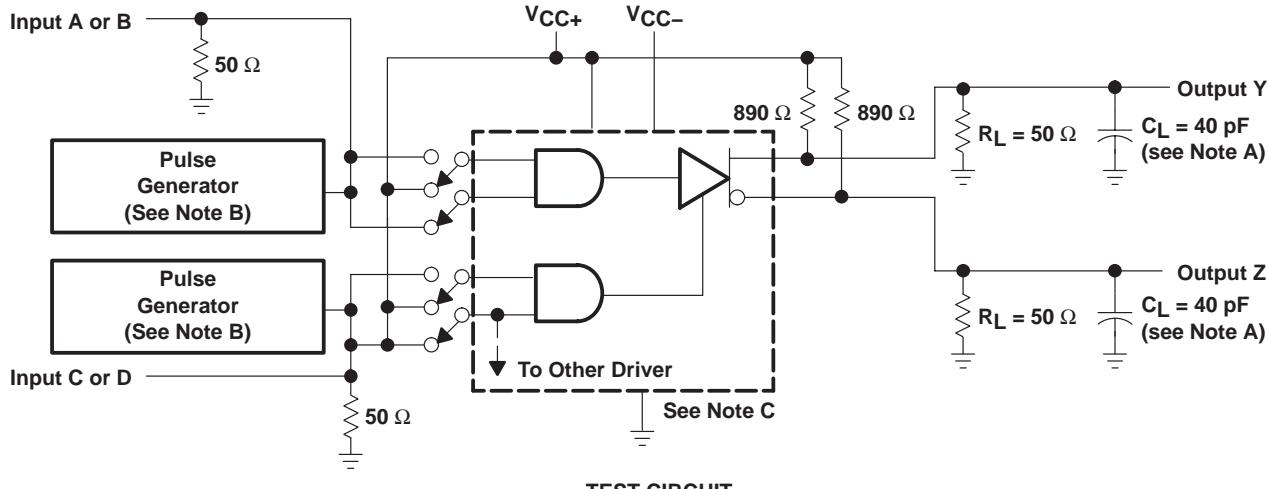
<sup>§</sup>  $t_{PLH}$  = propagation delay time, low- to high-level output

$t_{PHL}$  = propagation delay time, high- to low-level output

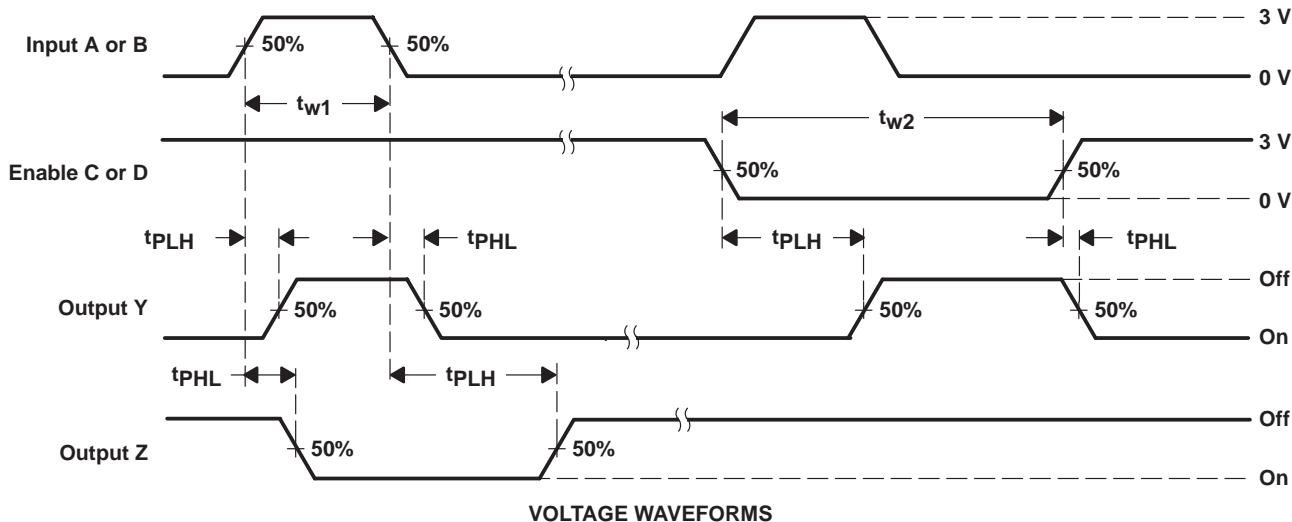
# SN55110A, SN75110A, SN75112 DUAL LINE DRIVERS

SLLS106G – DECEMBER 1975 – REVISED NOVEMBER 2004

## PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

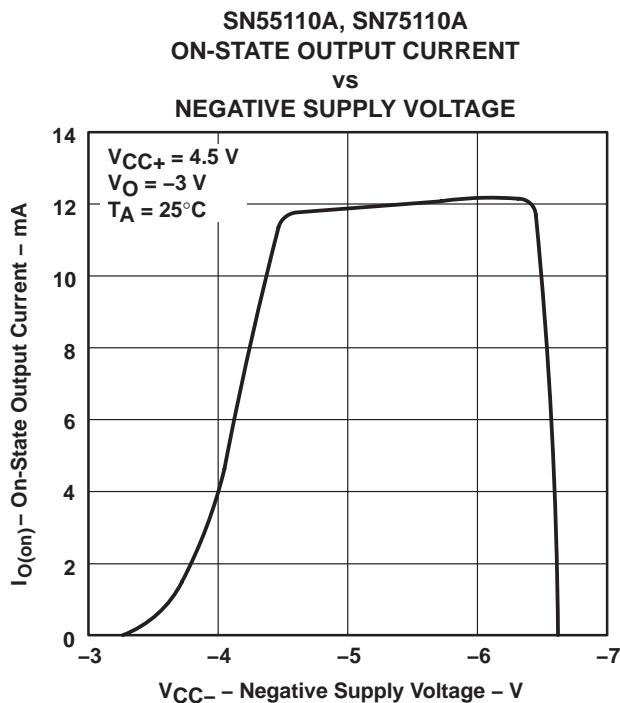


NOTES:

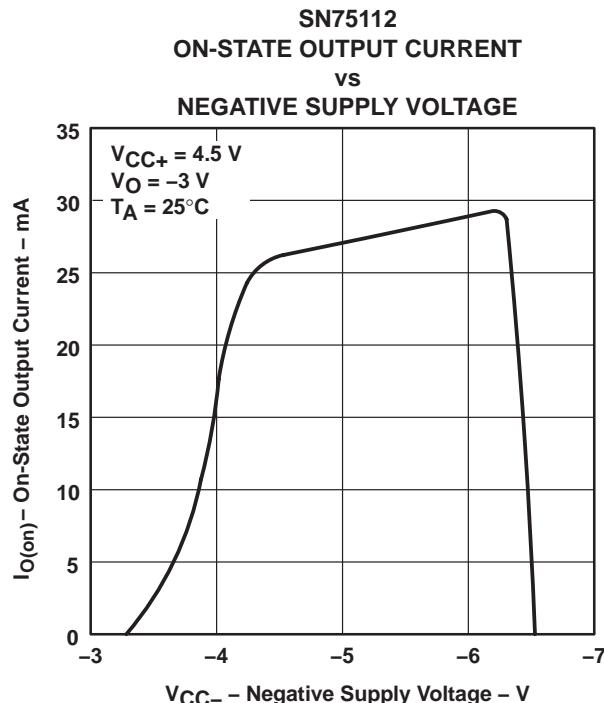
- $C_L$  includes probe and jig capacitance.
- The pulse generators have the following characteristics:  $Z_O = 50 \Omega$ ,  $t_r = t_f = 10 \pm 5 \text{ ns}$ ,  $t_{W1} = 500 \text{ ns}$ ,  $\text{PRR} \leq 1 \text{ MHz}$ ,  $t_{W2} = 1 \mu\text{s}$ ,  $\text{PRR} \leq 500 \text{ kHz}$ .
- For simplicity, only one channel and the enable connections are shown.

Figure 1. Test Circuit and Voltage Waveforms

**TYPICAL CHARACTERISTICS**



**Figure 2**



**Figure 3**

# SN55110A, SN75110A, SN75112 DUAL LINE DRIVERS

SLLS106G – DECEMBER 1975 – REVISED NOVEMBER 2004

## APPLICATION INFORMATION

### special pulse-control circuit

Figure 4 shows a circuit that can be used as a pulse-generator output or in many other testing applications.

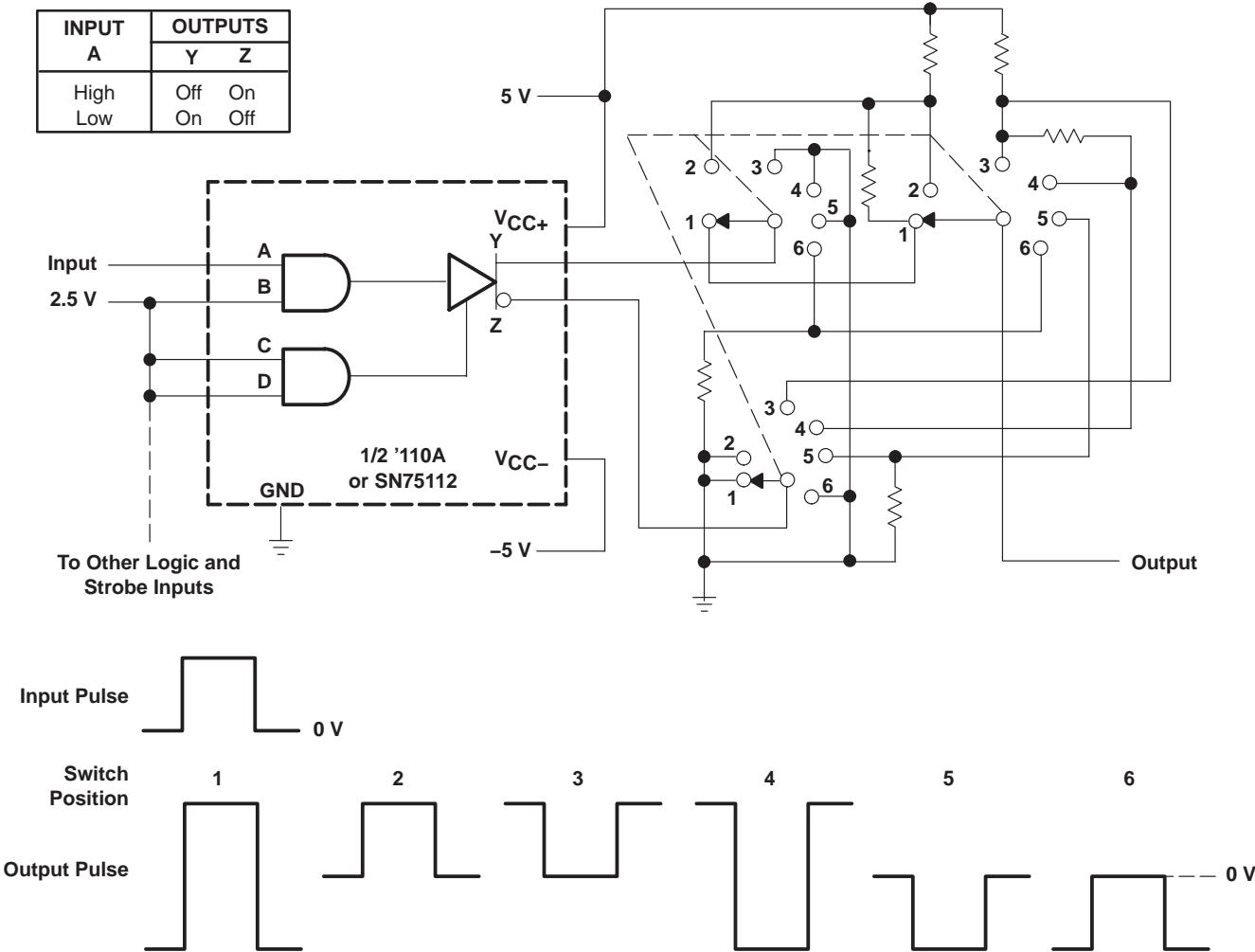


Figure 4. Pulse-Control Circuit

## APPLICATION INFORMATION

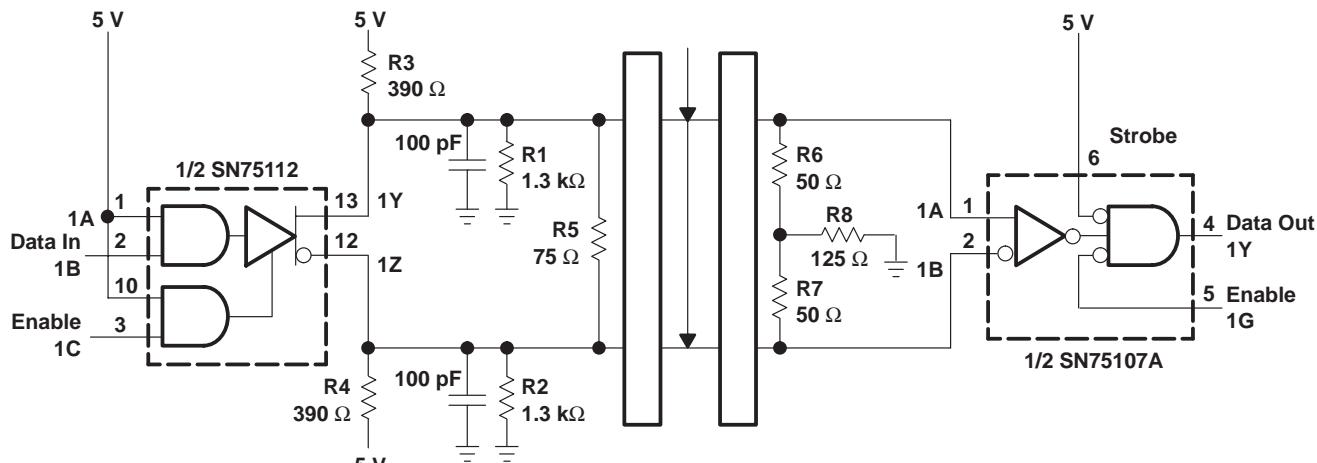
### using the SN75112 as a CCITT-recommended V.35 line driver

The SN75112 dual line driver, the SN75107A dual line receiver, and some external resistors can be used to implement the data-interchange circuit of CCITT recommendation V.35 (1976) modem specification. The circuit of one channel is shown in Figure 5 and meets the requirement of the interface as specified by Appendix 11 of CCITT V.35 and is summarized in Table 1 (V.35 has been replaced by ITU V.11).

Table 1. CCITT V.35 Electrical Requirements

| GENERATOR                                    | MIN  | MAX                       | UNIT     |
|--|------|---------------------------|----------|
| Source impedance, $Z_{\text{source}}$        | 50   | 150                       | $\Omega$ |
| Resistance to ground, $R$                    | 135  | 165                       | $\Omega$ |
| Differential output voltage, $V_{\text{OD}}$ | 440  | 660                       | mV       |
| 10% to 90% rise time, $t_r$<br>or            | 40   |                           | ns       |
|  |      | $0.01 \times u_i \dagger$ |          |
| Common-mode output voltage, $V_{\text{OC}}$  | -0.6 | 0.6                       | V        |
| LOAD (RECEIVER)                              | MIN  | MAX                       | UNIT     |
| Input impedance, $Z_I$                       | 90   | 110                       | $\Omega$ |
| Resistance to ground, $R$                    | 135  | 165                       | $\Omega$ |

$\dagger u_i$  = unit interval or minimum signal-element pulse duration



All resistors are 5%, 1/4 W.

Figure 5. CCITT-Recommended V.35 Interface Using the SN75112 and SN75107A

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)  | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)       | Samples   |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|-------------------------------|---|
| 5962-87547012A   | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-87547012A<br>SNJ55110AFK | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| 5962-8754701CA   | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-8754701CA<br>SNJ55110AJ  | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| 5962-8754701DA   | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-8754701DA<br>SNJ55110AW  | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN55110AJ        | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN55110AJ                     | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN75110AD        | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | SN75110A                      | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN75110ADR       | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | SN75110A                      | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN75110AN        | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green     | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN75110AN                     | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN75110ANSR      | ACTIVE        | SO           | NS              | 14   | 2000        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | SN75110A                      | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN75112D         | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | SN75112                       | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN75112DR        | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | SN75112                       | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SN75112N         | ACTIVE        | PDIP         | N               | 14   | 25          | RoHS & Green     | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN75112N                      | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SNJ55110AFK      | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-87547012A<br>SNJ55110AFK | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SNJ55110AJ       | ACTIVE        | CDIP         | J               | 14   | 1           | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-8754701CA<br>SNJ55110AJ  | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |
| SNJ55110AW       | ACTIVE        | CFP          | W               | 14   | 1           | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-8754701DA<br>SNJ55110AW  | <span style="background-color: red; color: white; padding: 2px;">Samples</span> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

**(2) RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3) MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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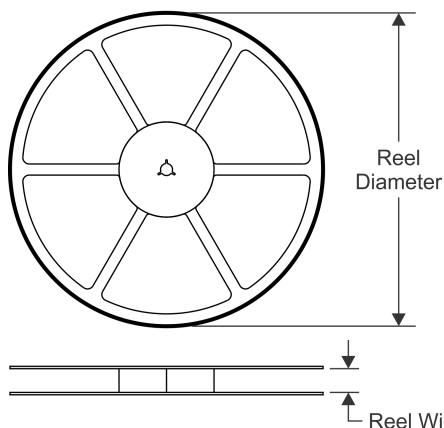
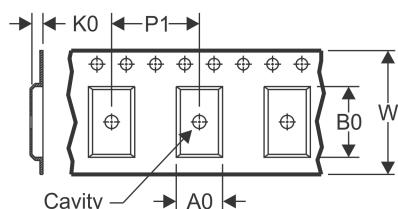
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN55110A, SN75110A :**

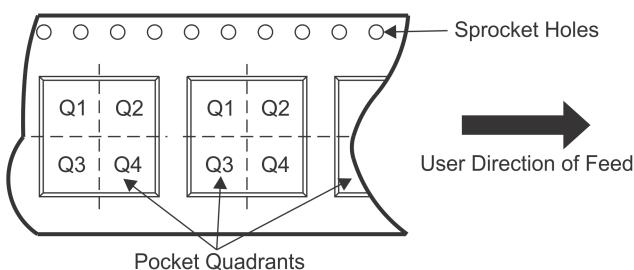
- Catalog : [SN75110A](#)
- Military : [SN55110A](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


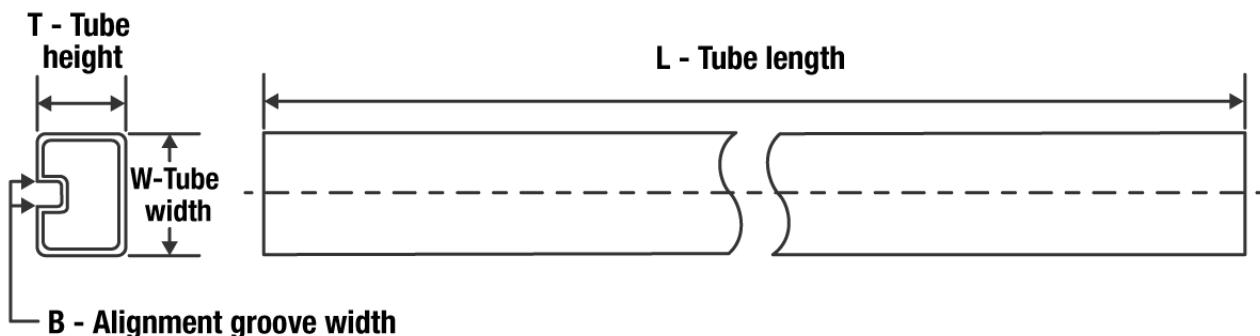
\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN75110ADR  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN75110ADR  | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN75110ANSR | SO           | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| SN75112DR   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN75110ADR  | SOIC         | D               | 14   | 2500 | 340.5       | 336.1      | 32.0        |
| SN75110ADR  | SOIC         | D               | 14   | 2500 | 853.0       | 449.0      | 35.0        |
| SN75110ANSR | SO           | NS              | 14   | 2000 | 853.0       | 449.0      | 35.0        |
| SN75112DR   | SOIC         | D               | 14   | 2500 | 853.0       | 449.0      | 35.0        |

**TUBE**


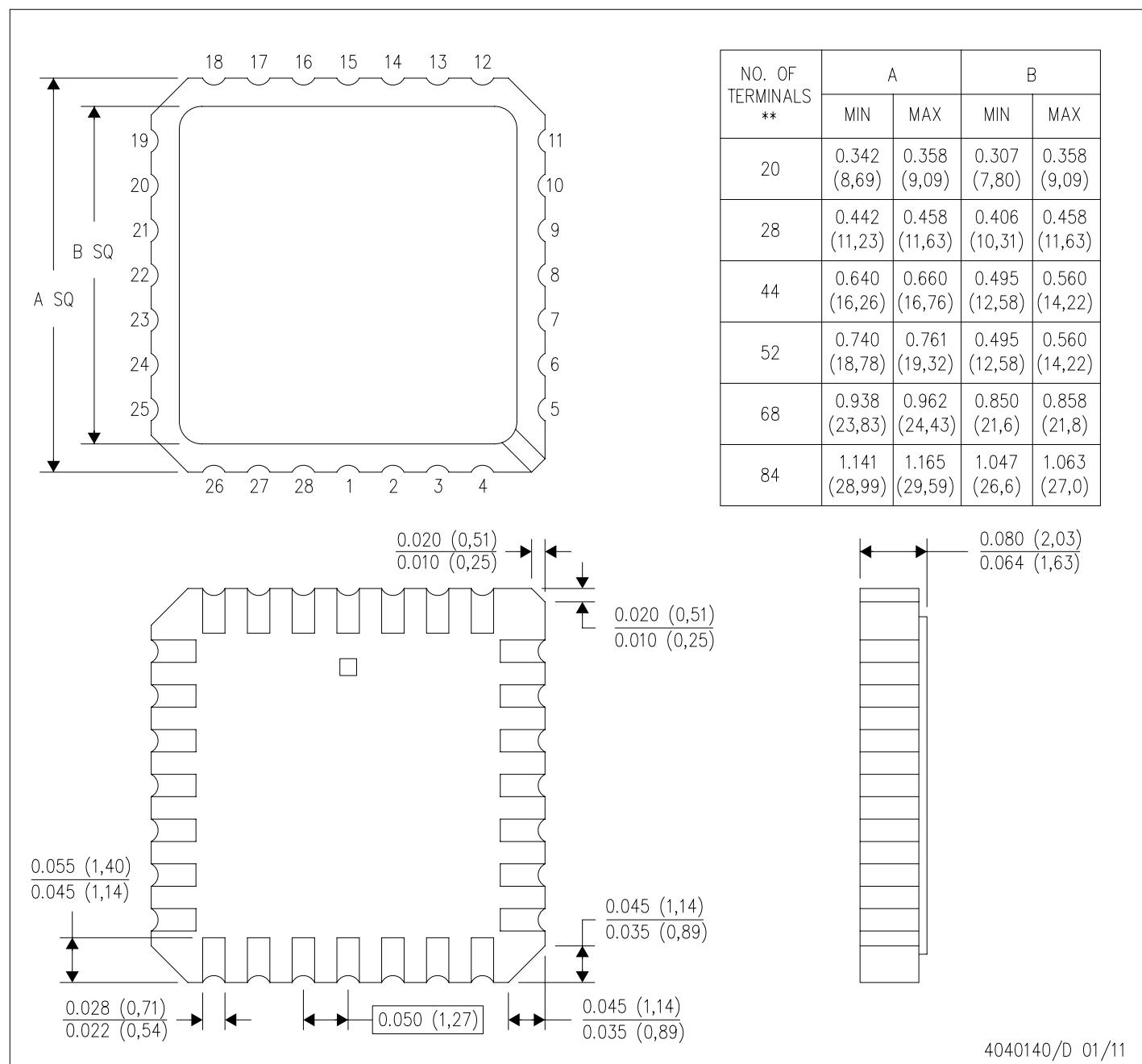
\*All dimensions are nominal

| Device         | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T ( $\mu$ m) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------------|--------|
| 5962-87547012A | FK           | LCCC         | 20   | 1   | 506.98 | 12.06  | 2030         | NA     |
| SN75110AD      | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940         | 4.32   |
| SN75110AN      | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230        | 4.32   |
| SN75110AN      | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230        | 4.32   |
| SN75112D       | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940         | 4.32   |
| SN75112N       | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230        | 4.32   |
| SNJ55110AFK    | FK           | LCCC         | 20   | 1   | 506.98 | 12.06  | 2030         | NA     |

FK (S-CQCC-N\*\*)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

4040140/D 01/11

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

## PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**

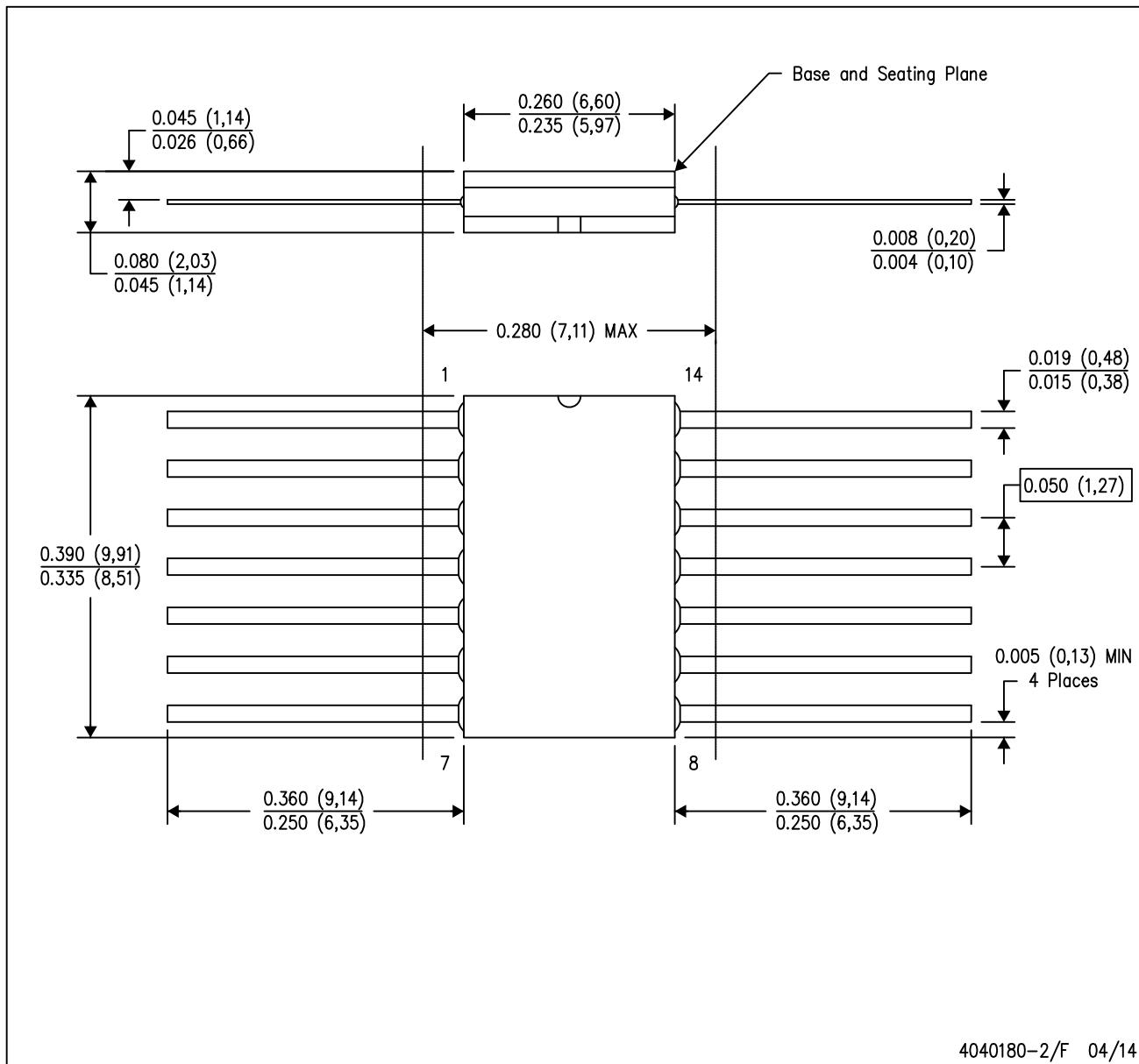


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



4040180-2/F 04/14

NOTES:

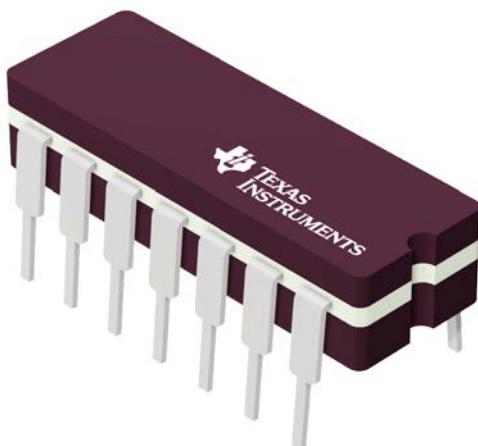
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL-STD 1835 GDFP1-F14

# GENERIC PACKAGE VIEW

**J 14**

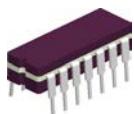
**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

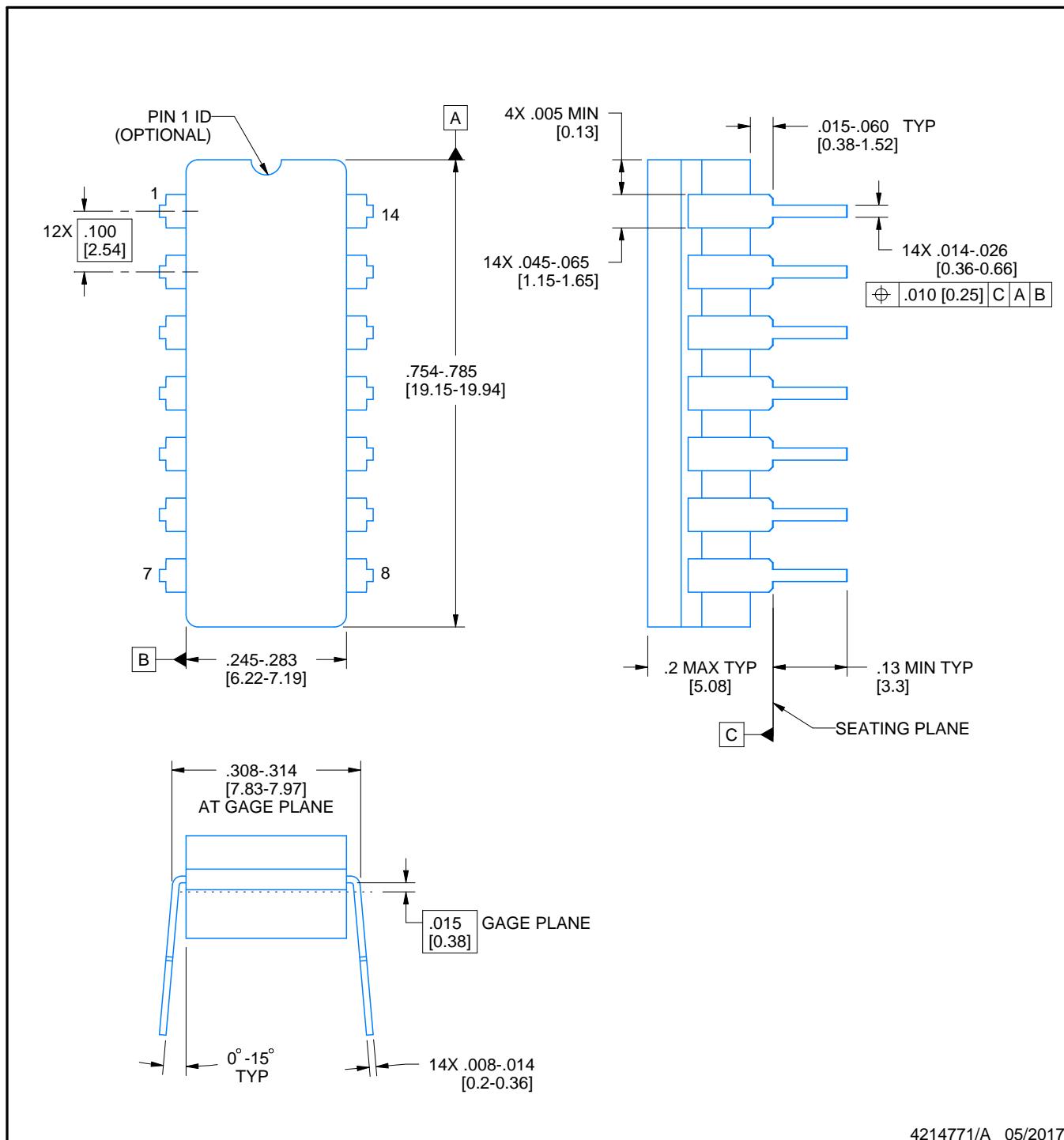


# PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

## NOTES:

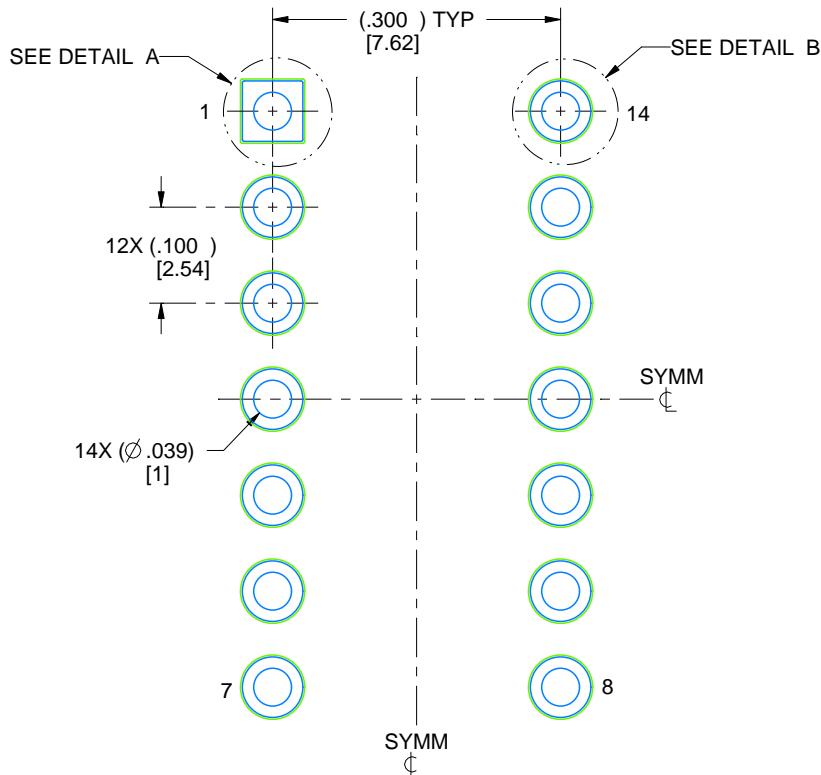
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

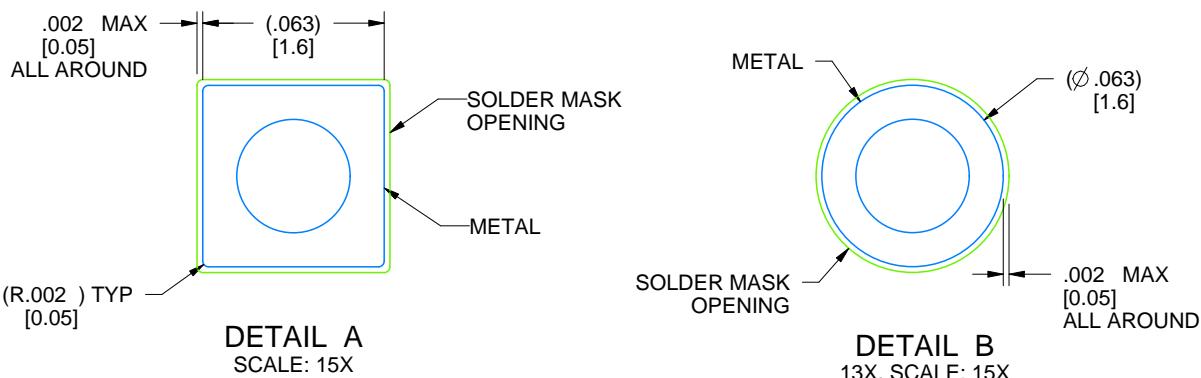
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



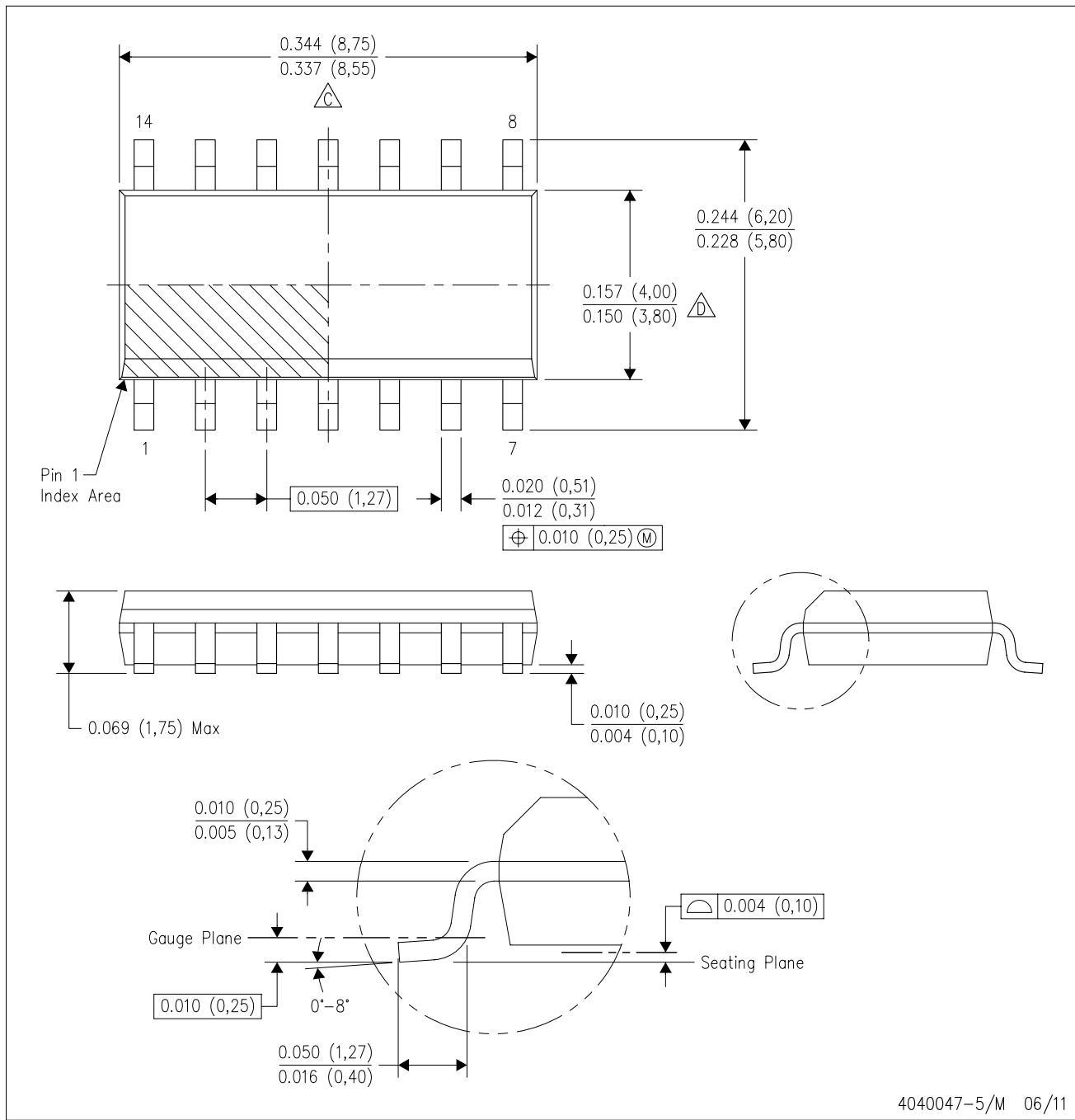
LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

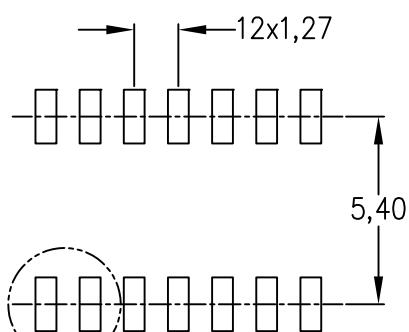
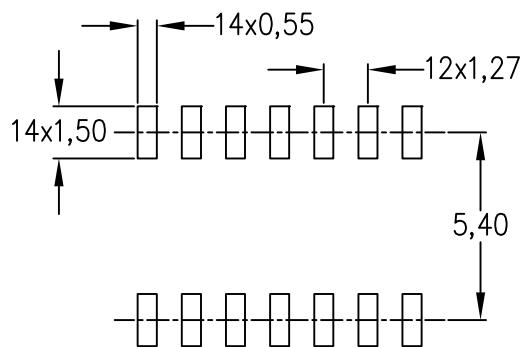
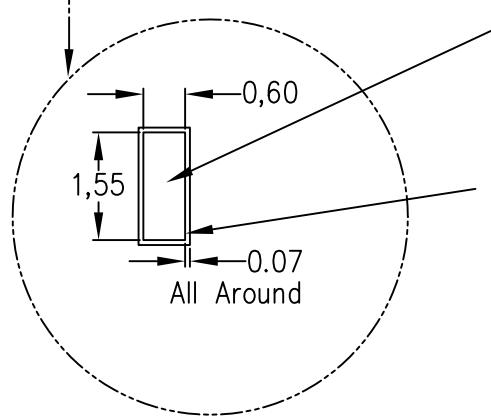
△C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

△D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)Example  
Non Soldermask Defined PadExample  
Pad Geometry  
(See Note C)Example  
Solder Mask Opening  
(See Note E)

4211283-3/E 08/12

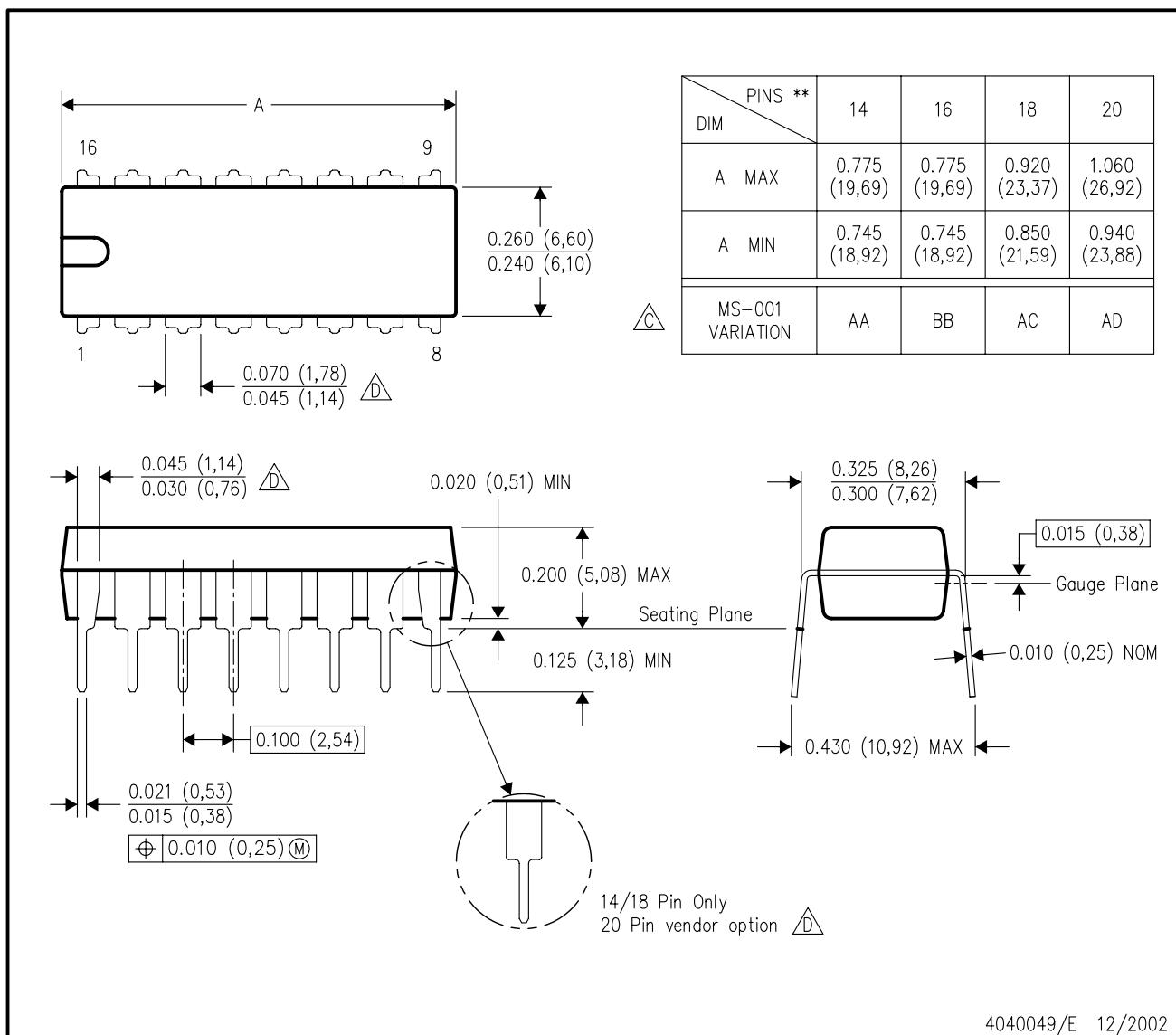
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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