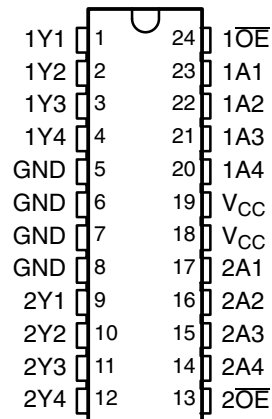


74ACT11240 OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS

SCAS210A – MAY 1987 – REVISED APRIL 1996

- Inputs Are TTL-Voltage Compatible
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, and Standard Plastic 300-mil DIPs (NT)

DB, DW, OR NT PACKAGE
(TOP VIEW)



description

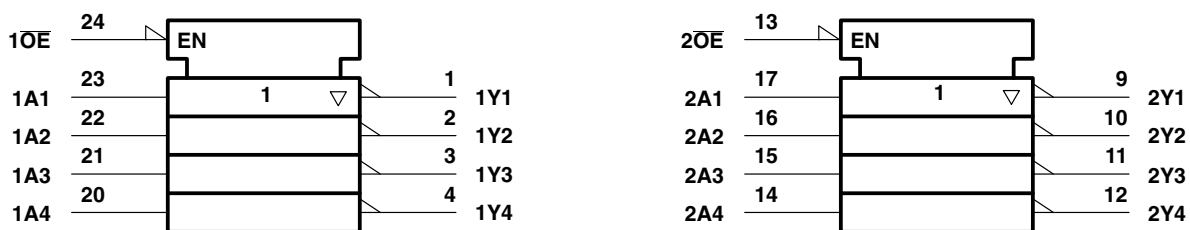
This octal buffer or line driver is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. This device provides inverting outputs and symmetrical active-low output-enable (\overline{OE}) inputs. This device features high fan-out and improved fan-in.

The 74ACT11240 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	L
L	L	H
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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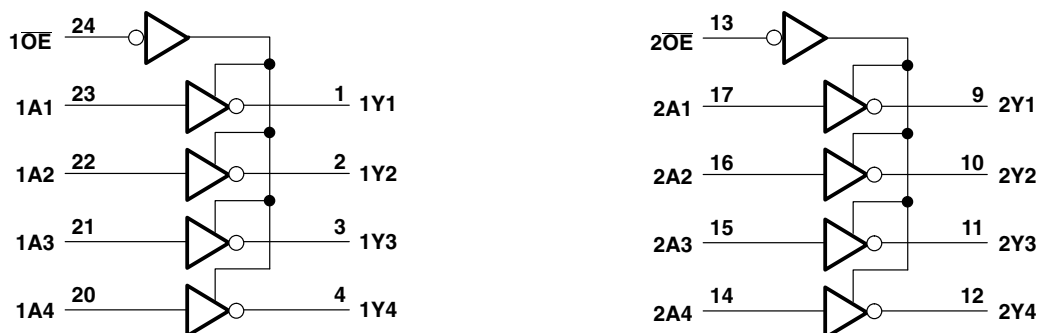
74ACT11240

OCTAL BUFFER/LINE DRIVER

WITH 3-STATE OUTPUTS

SCAS210A – MAY 1987 – REVISED APRIL 1996

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 6 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 200 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DB package	0.65 W
DW package	1.7 W
NT package	1.3 W
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has a trace length of zero.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			-24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
T_A	Operating free-air temperature	-40		85	$^\circ\text{C}$



74ACT11240
OCTAL BUFFER/LINE DRIVER
WITH 3-STATE OUTPUTS

SCAS210A – MAY 1987 – REVISED APRIL 1996

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT	
			MIN	TYP	MAX				
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4			4.4		V	
		5.5 V	5.4			5.4			
	I _{OH} = -24 mA	4.5 V	3.94			3.8			
		5.5 V	4.94			4.8			
	I _{OH} = -75 mA [†]	5.5 V				3.85			
	V _{OL}	I _{OL} = 50 μA	4.5 V				0.1		V
5.5 V						0.1			
I _{OL} = 24 mA		4.5 V				0.36			
		5.5 V				0.36			
I _{OL} = 75 mA [†]		5.5 V				1.65			
I _{OZ}		V _O = V _{CC} or GND	5.5 V				±0.5		
I _I	V _I = V _{CC} or GND	5.5 V				±0.1		μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V				8		80	μA
ΔI _{CC} [‡]	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V				0.9		1	mA
C _i	V _I = V _{CC} or GND	5 V				4			pF
C _o	V _I = V _{CC} or GND	5 V				10			pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t _{PLH}	A	Y	1.5	6.5	9.9	1.5	10.6	ns
t _{PHL}			1.5	6	8	1.5	8.7	
t _{PZH}	OE	Y	1.5	7.5	11.7	1.5	12.5	ns
t _{PZL}			1.5	7.3	11.5	1.5	12.3	
t _{PHZ}	OE	Y	1.5	7.3	9.4	1.5	10	ns
t _{PLZ}			1.5	7.9	10.3	1.5	10.8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

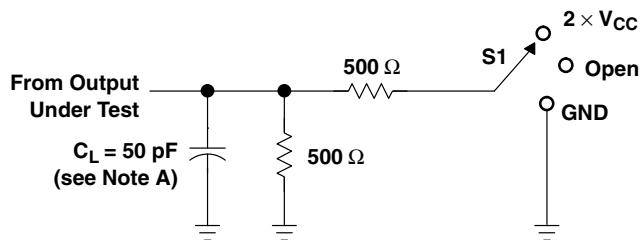
PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per buffer	C _L = 50 pF, f = 1 MHz	47	pF
			13	



74ACT11240
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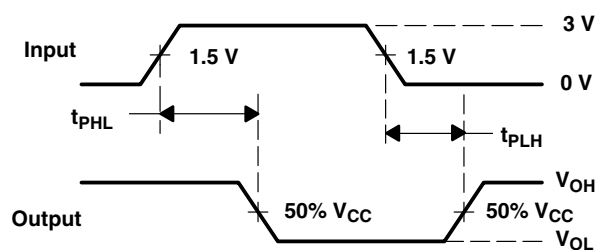
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PARAMETER MEASUREMENT INFORMATION

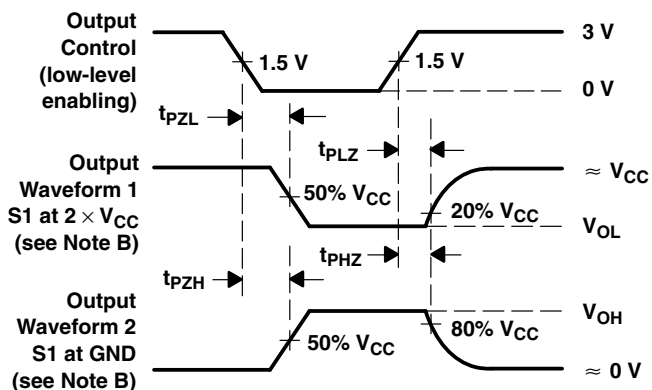


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 3$ ns, $t_f = 3$ ns.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74ACT11240DW	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT11240	Samples
74ACT11240DWR	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT11240	Samples
74ACT11240DWRG4	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT11240	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ACT11240DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74ACT11240DWR	SOIC	DW	24	2000	350.0	350.0	43.0

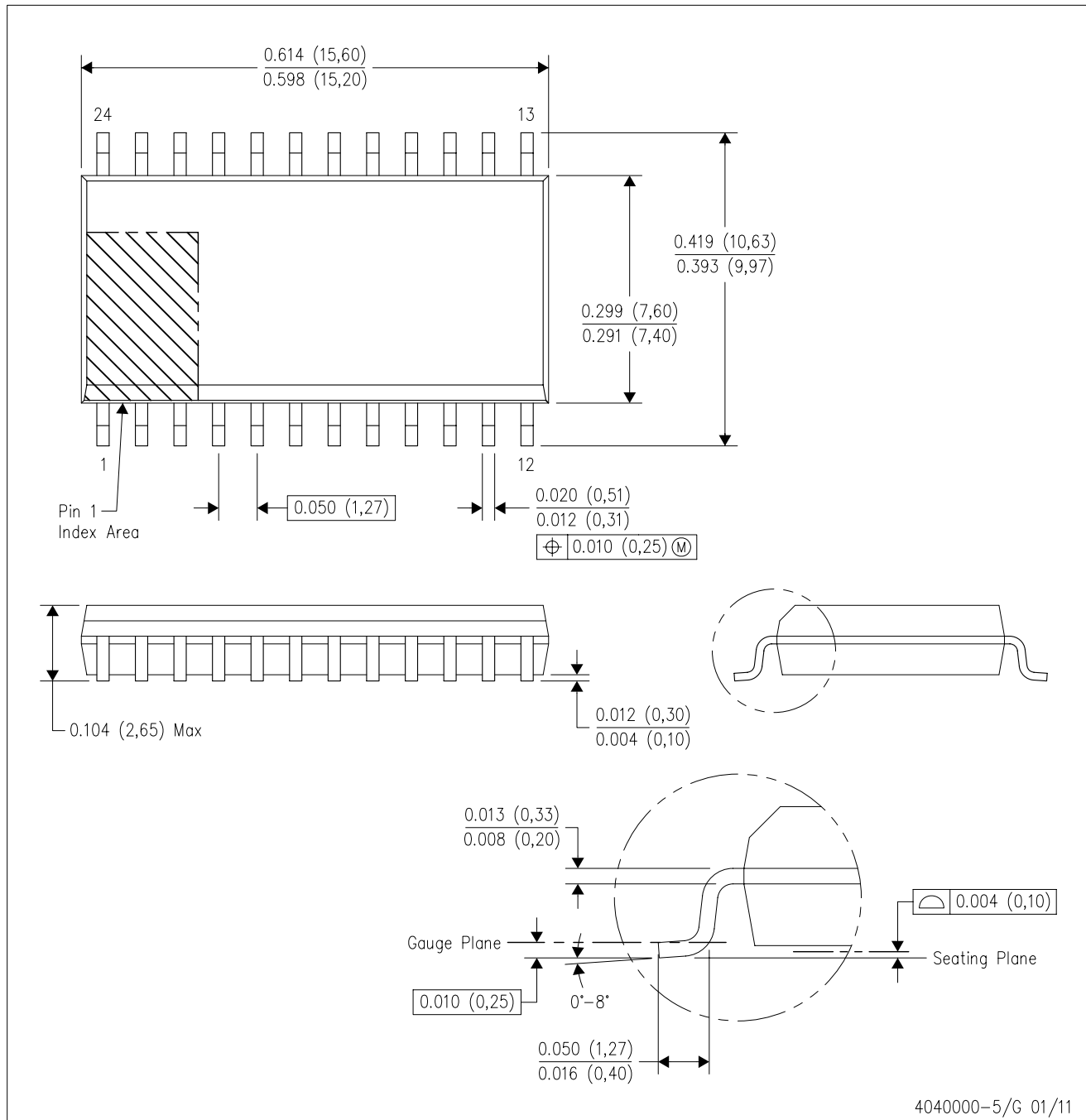
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
74ACT11240DW	DW	SOIC	24	25	506.98	12.7	4826	6.6

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



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