



# 18-Bit Analog-to-Digital Converter For Bridge Sensors

 Check for Samples: [ADS1130](#)

## FEATURES

- 18-Bit Noise-Free Resolution
- Complete Front-End for Bridge Sensor
- Onboard Gain of 64
- Onboard Oscillator
- Selectable 10SPS or 80SPS Data Rates
- Simultaneous 50Hz and 60Hz Rejection at 10SPS
- External Voltage Reference up to 5V for Ratiometric Measurements
- Simple, Pin-Driven Control
- Two-Wire Serial Digital Interface
- Tiny TSSOP-16 Package
- Supply Range: 2.7V to 5.3V

## APPLICATIONS

- Weigh Scales
- Strain Gauges

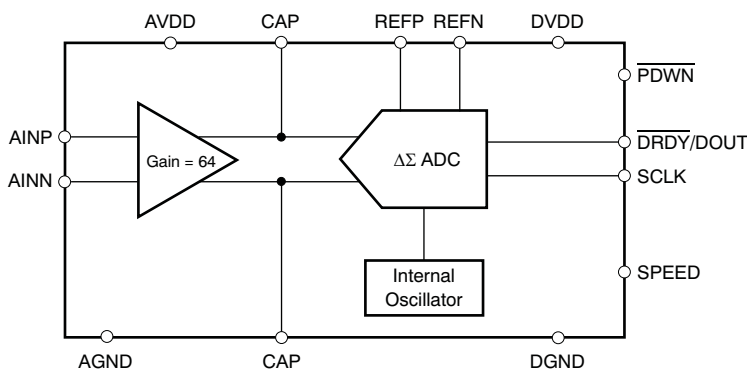
## DESCRIPTION

The ADS1130 is a precision, 18-bit analog-to-digital converter (ADC). With an onboard low-noise gain amplifier, onboard oscillator, and precision 18-bit delta-sigma ADC, the ADS1130 provides a complete front-end solution for bridge sensor applications including weigh scales and strain gauges.

The low-noise amplifier has a gain of 64, supporting a full-scale differential input of  $\pm 39\text{mV}$ . The delta-sigma ADC has 18-bit effective resolution and is comprised of a third-order modulator and fourth-order digital filter. Two data rates are supported: 10SPS (with both 50Hz and 60Hz rejection) and 80SPS. The ADS1130 can be put into a low-power standby mode or shut off completely in power-down mode.

All of the features of the ADS1130 are controlled by dedicated pins; there are no digital registers to program. Data are output over an easily-isolated serial interface that connects directly to the [MSP430](#) and other microcontrollers.

The ADS1130 is available in a TSSOP-16 package and is specified for operation from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over operating free-air temperature range, unless otherwise noted.

	ADS1130	UNIT
AVDD to AGND	-0.3 to +6	V
DVDD to DGND	-0.3 to +6	V
AGND to DGND	-0.3 to +0.3	V
Input current	100, momentary	mA
	10, continuous	mA
Analog input voltage to AGND	-0.3 to AVDD + 0.3	V
Digital input voltage to DGND	-0.3 to DVDD + 0.3	V
Maximum junction temperature	+150	°C
Operating temperature range	-40 to +85	°C
Storage temperature range	-60 to +150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

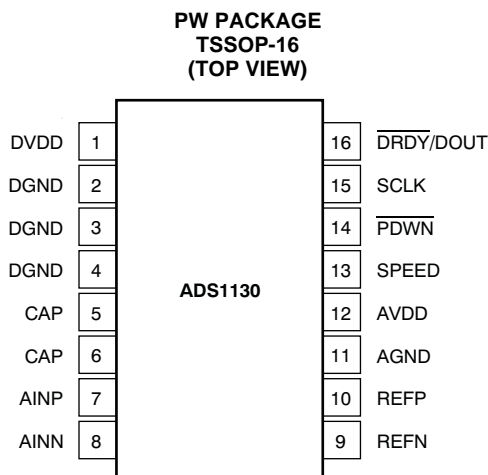
## ELECTRICAL CHARACTERISTICS

 All specifications at  $T_A = +25^\circ\text{C}$ ,  $AVDD = DVDD = REFP = +5\text{V}$ , and  $REFN = \text{AGND}$ , unless otherwise noted.

PARAMETER	CONDITIONS	ADS1130			UNIT	
		MIN	TYP	MAX		
<b>ANALOG INPUTS</b>						
Full-scale input voltage (AINP – AINN)		$\pm 0.5V_{REF}/64$			V	
Common-mode input range		AGND + 1.5V		AVDD – 1.5V	V	
Differential input current		$\pm 2$			nA	
<b>SYSTEM PERFORMANCE</b>						
Resolution	No missing codes	18			Bits	
Data rate	SPEED = high	80			SPS	
	SPEED = low	10			SPS	
Digital filter settling time	Full settling	4			Conversions	
Integral nonlinearity (INL)	Differential input, end-point fit	$\pm 20$			ppm of FSR	
Input offset error		$\pm 120$			ppm of FSR	
Input offset drift		$\pm 10$			nV/ $^\circ\text{C}$	
Gain error		$\pm 1$			%	
Gain drift		$\pm 5$			ppm/ $^\circ\text{C}$	
Normal-mode rejection	$f_{IN} = 50\text{Hz}$ or $60\text{Hz} \pm 1\text{Hz}$ , $f_{DATA} = 10\text{SPS}$	90			dB	
Common-mode rejection	at dc	100			dB	
Input-referred noise	$f_{DATA} = 10\text{SPS}$	300			nV <sub>PP</sub> <sup>(1)</sup>	
	$f_{DATA} = 80\text{SPS}$	500			nV <sub>PP</sub> <sup>(1)</sup>	
Power-supply rejection	at dc	100			dB	
<b>VOLTAGE REFERENCE INPUT</b>						
Voltage reference input ( $V_{REF}$ )	$V_{REF} = REFP - REFN$	1.5	AVDD	AVDD + 0.1V	V	
Negative reference input (REFN)		AGND – 0.1		REFP – 1.5	V	
Positive reference input (REFP)		REFN + 1.5		AVDD + 0.1	V	
Voltage reference input current		10			nA	
<b>DIGITAL</b>						
Logic levels	$V_{IH}$	0.7 DVDD			DVDD + 0.1	V
	$V_{IL}$	DGND			0.2 DVDD	V
	$V_{OH}$	$I_{OH} = 1\text{mA}$	DVDD – 0.4			V
	$V_{OL}$	$I_{OL} = 1\text{mA}$	0.2 DVDD			V
Input leakage	$0 < V_{IN} < DVDD$	$\pm 10$			$\mu\text{A}$	
Serial clock input frequency ( $f_{SCLK}$ )		5			MHz	
<b>POWER SUPPLY</b>						
Power-supply voltage (AVDD, DVDD)		2.7			5.3	V
Analog supply current	Normal mode, AVDD = 3V	900			1500	$\mu\text{A}$
	Normal mode, AVDD = 5V	900			1500	$\mu\text{A}$
	Standby mode	0.1			1	$\mu\text{A}$
	Power-down	0.1			1	$\mu\text{A}$
Digital supply current	Normal mode, DVDD = 3V	60			100	$\mu\text{A}$
	Normal mode, DVDD = 5V	95			150	$\mu\text{A}$
	Standby mode, SCLK = high, DVDD = 3V	45			70	$\mu\text{A}$
	Standby mode, SCLK = high, DVDD = 5V	65			80	$\mu\text{A}$
	Power-down	0.2				$\mu\text{A}$
Power dissipation, total	Normal mode, AVDD = DVDD = 3V	2.9				mW
	Normal mode, AVDD = DVDD = 5V	5.0				mW
	Standby mode, AVDD = DVDD = 5V	0.3				mW
<b>TEMPERATURE</b>						
Operating temperature range		–40			+85	$^\circ\text{C}$
Specified temperature range		–40			+85	$^\circ\text{C}$

(1) PP signifies peak-to-peak noise.

### PIN CONFIGURATION



### PIN DESCRIPTIONS

NAME	TERMINAL	ANALOG/DIGITAL INPUT/OUTPUT	DESCRIPTION	
DVDD	1	Digital	Digital power supply: 2.7V to 5.3V	
DGND	2-4	Digital	Digital ground	
CAP	5, 6	Analog	Gain amplifier bypass capacitor connection	
AINP	7	Analog input	Positive analog input	
AINN	8	Analog input	Negative analog input	
REFN	9	Analog input	Negative reference input	
REFP	10	Analog input	Positive reference input	
AGND	11	Analog	Analog ground	
AVDD	12	Analog	Analog power supply, 2.7V to 5.3V	
SPEED	13	Digital input	Data rate select:	
			<b>SPEED</b>	<b>DATA RATE</b>
			0	10SPS
			1	80SPS
$\overline{\text{PDWN}}$	14	Digital input	Power-down: Holding this pin low powers down the entire converter and resets the ADC.	
SCLK	15	Digital input	Serial clock: Clock out data on the rising edge. Also used to initiate Sleep mode. See the <a href="#">Standby Mode</a> section for more details.	
$\overline{\text{DRDY/DOUT}}$	16	Digital output	Dual-purpose output: Data ready: Indicates valid data by going low. Data output: Outputs data, MSB first, on the first rising edge of SCLK.	

## OVERVIEW

The ADS1130 is a precision, 18-bit ADC that includes a low-noise amplifier, internal oscillator, third-order delta-sigma ( $\Delta\Sigma$ ) modulator, and fourth-order digital filter. The ADS1130 provides a complete front-end solution for bridge sensor applications such as weigh scales, strain gauges, and pressure sensors.

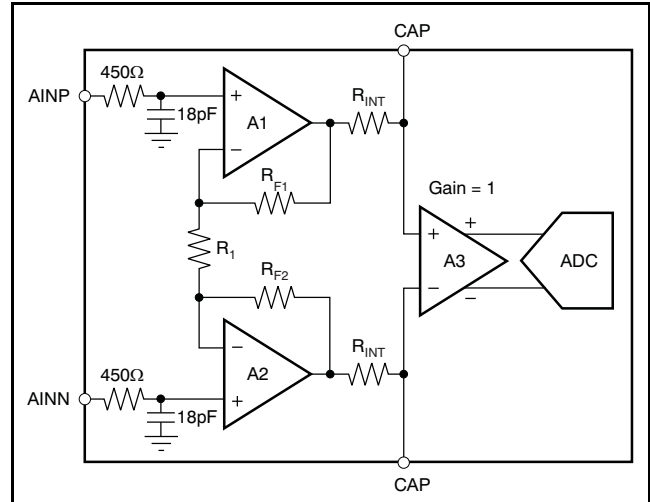
Data can be output at 10SPS for excellent 50Hz and 60Hz rejection, or at 80SPS when higher speeds are needed. The ADS1130 is easy to configure, and all digital control is accomplished through dedicated pins; there are no registers to program. A simple two-wire serial interface retrieves the data.

## ANALOG INPUTS (AINP, AINN)

The input signal to be measured is applied to the input pins AINP and AINN. The ADS1130 accepts differential input signals, but can also measure unipolar signals.

## LOW-NOISE AMPLIFIER

The ADS1130 features a low-drift, low-noise amplifier that provides a complete front-end solution for bridge sensors. A simplified diagram is shown in [Figure 1](#). It consists of two chopper-stabilized amplifiers (A1 and A2) and three accurately-matched resistors ( $R_1$ ,  $R_{F1}$ , and  $R_{F2}$ ), which construct a differential front-end stage with a gain of 64, followed by gain stage A3 (Gain = 1). The inputs are equipped with an electromagnetic interference (EMI) filter, as shown in [Figure 1](#). The cutoff frequency of the EMI filter is 19.6MHz. With a 5V reference, the bipolar input range is  $-39\text{mV}$  to  $+39\text{mV}$ . The inputs of the ADS1130 are protected with internal ESD diodes connected to the power-supply rails.



**Figure 1. Simplified Diagram of the Amplifier**

## Bypass Capacitor

Place a  $0.1\mu\text{F}$  external capacitor between the two capacitor pins (CAP). A high-quality capacitor is recommended for best performance.

## VOLTAGE REFERENCE INPUTS (REFP, REFN)

The voltage reference used by the modulator is generated from the voltage difference between REFP and REFN:  $V_{\text{REF}} = \text{REFP} - \text{REFN}$ . The reference inputs use a structure similar to that of the analog inputs. In order to increase the reference input impedance, a switching buffer circuitry is used to reduce the input equivalent capacitance. The reference drift and noise impact ADC performance. In order to achieve best results, pay close attention to the reference noise and drift specifications. A simplified diagram of the circuitry on the reference inputs is illustrated in [Figure 2](#). The switches and capacitors can be modeled approximately using an effective impedance of:

$$Z_{\text{EFF}} = \frac{1}{2f_{\text{MOD}} C_{\text{BUF}}}$$

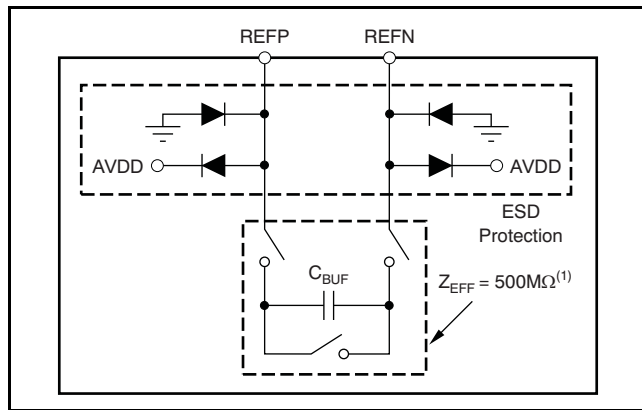
Where:

$f_{\text{MOD}}$  = modulator sampling frequency (76.8kHz)

$C_{\text{BUF}}$  = input capacitance of the buffer

For the ADS1130:

$$Z_{EFF} = \frac{1}{(2)(76.8\text{kHz})(13\text{fF})} = 500\text{M}\Omega$$



(1)  $f_{MOD} = 76.8\text{kHz}$ .

**Figure 2. Simplified Reference Input Circuitry**

ESD diodes protect the reference inputs. To prevent these diodes from turning on, make sure the voltages on the reference pins do not go below GND by more than 100mV, and likewise, do not exceed AVDD by 100mV:

$$\text{GND} - 100\text{mV} < (\text{REFP or REFN}) < \text{AVDD} + 100\text{mV}$$

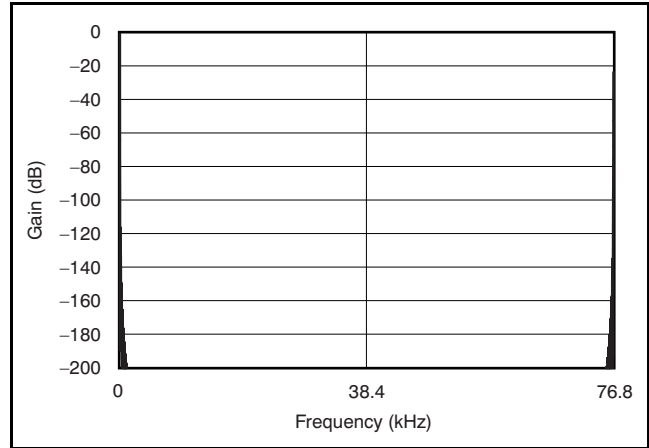
**FREQUENCY RESPONSE**

The ADS1130 uses a sinc<sup>4</sup> digital filter with the frequency response shown in Figure 3. The frequency response repeats at multiples of the modulator sampling frequency of 76.8kHz. The overall response is that of a low-pass filter with a -3dB cutoff frequency of 3.32Hz with the SPEED pin tied low (10SPS data rate) and 11.64Hz with the SPEED pin tied high (80SPS data rate).

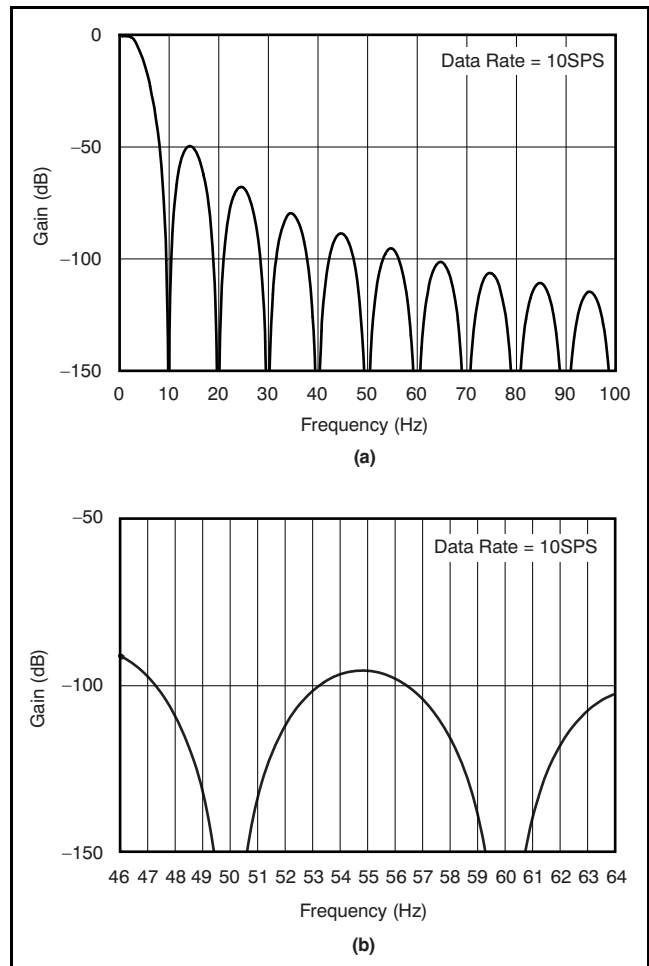
To help see the response at lower frequencies, Figure 4(a) illustrates the response out to 100Hz, when the data rate = 10SPS. Notice that signals at multiples of 10Hz are rejected, and therefore simultaneous rejection of 50Hz and 60Hz is achieved.

The benefit of using a sinc<sup>4</sup> filter is that every frequency notch has four zeros on the same location. This response, combined with the low-drift internal oscillator, provides an excellent normal-mode rejection of line-cycle interference.

Figure 4(b) shows the same plot, but enlarges the view at the 50Hz and 60Hz notches with the SPEED pin tied low (10SPS data rate).



**Figure 3. Frequency Response**



**Figure 4. Frequency Response Out To 100Hz**

## SETTLING TIME

Large changes in the input signal require settling time. For example, an external multiplexer in front of the ADS1130 can cause large changes in the input voltage when switching the multiplexer input channels. Abrupt changes in the input require four data conversion cycles to settle. When continuously converting, five readings may be necessary in order to settle the data. If the change in input occurs in the middle of the first conversion, four more full conversions of the fully-settled input are required to get fully-settled data. Discard the first four readings because they contain only partially-settled data. [Figure 5](#) illustrates the settling time for the ADS1130 in Continuous Conversion mode.

## DATA RATE

The ADS1130 data rate is set by the SPEED pin, as shown in [Table 1](#). When SPEED is low, the data rate is nominally 10SPS. This data rate provides the lowest noise, and also has excellent rejection of both 50Hz and 60Hz line-cycle interference. For applications requiring fast data rates, setting SPEED high selects a data rate of nominally 80SPS.

**Table 1. Data Rate Settings**

SPEED PIN	DATA RATE
0	10SPS
1	80SPS

## DATA FORMAT

The ADS1130 outputs 18 bits of data in binary two's complement format. The least significant bit (LSB) has a weight of  $(0.5V_{REF}/64)(2^{17} - 1)$ . The positive full-scale input produces an output code of 1FFFFh and the negative full-scale input produces an output code of 40000h. The output clips at these codes for signals exceeding full-scale. [Table 2](#) summarizes the ideal output codes for different input signals.

**Table 2. Ideal Output Code vs Input Signal<sup>(1)</sup>**

INPUT SIGNAL $V_{IN}$ (AINP – AINN)	IDEAL OUTPUT
$\geq +0.5V_{REF}/64$	1FFFFh
$(+0.5V_{REF}/64)/(2^{17} - 1)$	00001h
0	00000h
$(-0.5V_{REF}/64)/(2^{17} - 1)$	3FFFFh
$\leq -0.5V_{REF}/64$	40000h

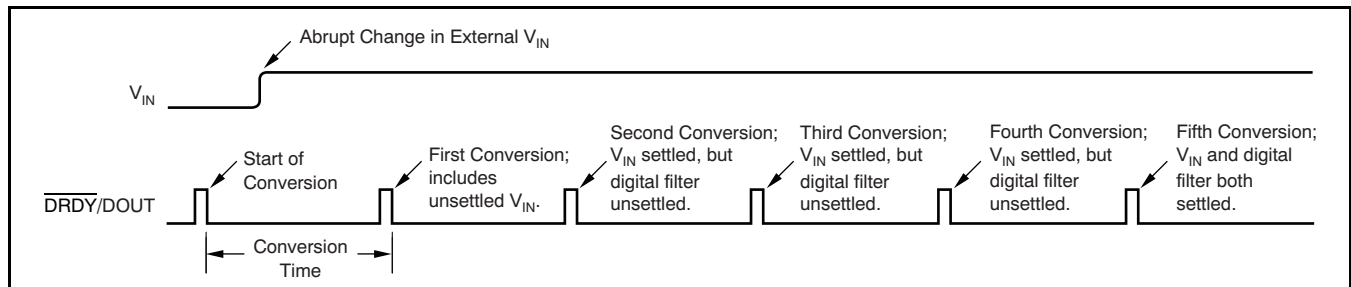
(1) Excludes effects of noise, INL, offset, and gain errors.

## DATA READY/DATA OUTPUT ( $\overline{DRDY}/DOUT$ )

This digital output pin serves two purposes. First, it indicates when new data are ready by going low. Afterwards, on the first rising edge of SCLK, the  $\overline{DRDY}/DOUT$  pin changes function and begins outputting the conversion data, most significant bit (MSB) first. Data are shifted out on each subsequent SCLK rising edge. After all 18 bits have been retrieved, the pin can be forced high with additional SCLKs. It then stays high until new data are ready. This configuration is useful when polling on the status of  $\overline{DRDY}/DOUT$  to determine when to begin data retrieval.

## SERIAL CLOCK INPUT (SCLK)

This digital input shifts serial data out with each rising edge. This input has built-in hysteresis, but care should still be taken to ensure a clean signal. Glitches or slow-rising signals can cause unwanted additional shifting. For this reason, it is best to make sure the rise and fall times of SCLK are both less than 50ns.



**Figure 5. Settling Time in Continuous Conversion Mode**

### DATA RETRIEVAL

The ADS1130 continuously converts the analog input signal. To retrieve data, wait until  $\overline{\text{DRDY}}/\text{DOUT}$  goes low, as shown in Figure 6. After  $\overline{\text{DRDY}}/\text{DOUT}$  goes low, begin shifting out the data by applying SCLKs. Data are shifted out MSB first. It is not required to shift out all 18 bits of data, but the data must be retrieved before new data are updated (within  $t_{\text{CONV}}$ )

or else the data are overwritten. Avoid data retrieval during the update period ( $t_{\text{UPDATE}}$ ). To avoid having  $\overline{\text{DRDY}}/\text{DOUT}$  remain in the state of the last bit, the 24 SCLKs may be applied to force  $\overline{\text{DRDY}}/\text{DOUT}$  high. This technique is useful when a host controlling the device is polling  $\overline{\text{DRDY}}/\text{DOUT}$  to determine when data are ready. Do not apply more than 24 SCLKs during data retrieval.

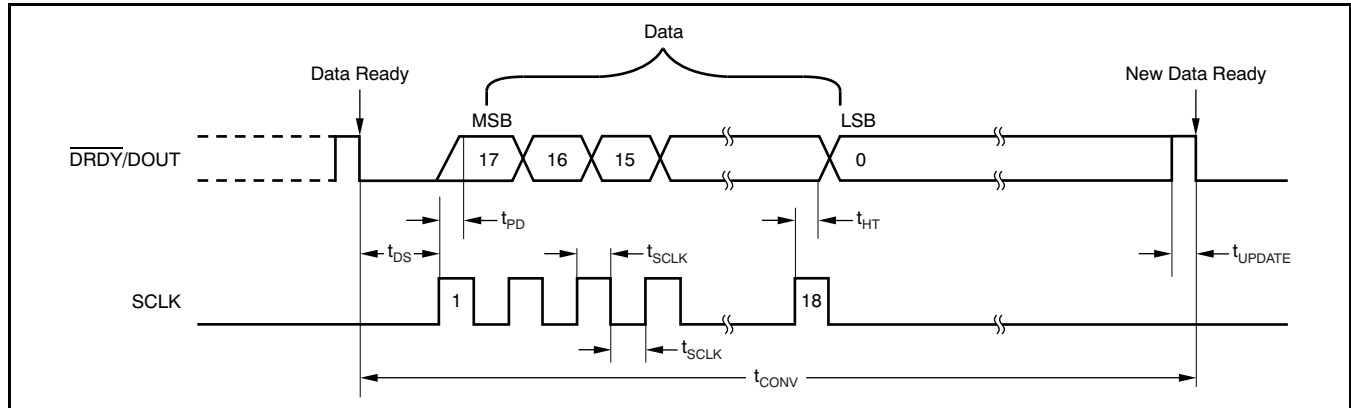


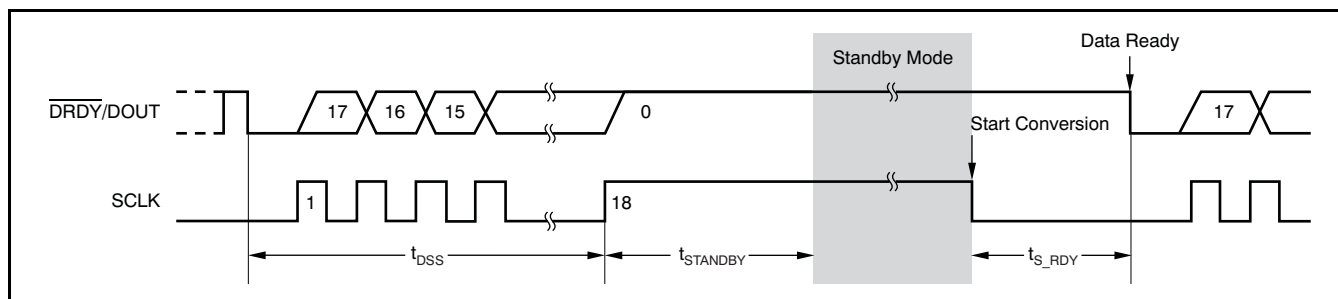
Figure 6. Data Retrieval Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
$t_{\text{DS}}$	$\overline{\text{DRDY}}/\text{DOUT}$ low to first SCLK rising edge	0			ns
$t_{\text{SCLK}}$	SCLK positive or negative pulse width	100			ns
$t_{\text{PD}}$	SCLK rising edge to new data bit valid: propagation delay			50	ns
$t_{\text{HT}}$	SCLK rising edge to old data bit valid: hold time	0			ns
$t_{\text{UPDATE}}$	Data updating: no readback allowed	39			$\mu\text{s}$
$t_{\text{CONV}}$	Conversion time (1/data rate)		SPEED = 1	12.5	ms
			SPEED = 0	100	ms

**STANDBY MODE**

Standby mode dramatically reduces power consumption by shutting down most of the circuitry. In Standby mode, the entire analog circuitry is powered down and only the clock source circuitry is awake to reduce the wake-up time from the Standby mode. To enter Standby mode, simply hold SCLK high after  $\overline{\text{DRDY}}/\text{DOUT}$  goes low; see Figure 7. Standby mode can be initiated at any time during readback.

When  $t_{\text{STANDBY}}$  has passed with SCLK held high, Standby mode activates.  $\overline{\text{DRDY}}/\text{DOUT}$  stays high when Standby mode begins. SCLK must remain high to stay in Standby mode. To exit Standby mode (wakeup), set SCLK low. The first data after exiting Standby mode is valid.



**Figure 7. Standby Mode Timing (can be used for single conversions)**

SYMBOL	DESCRIPTION		MIN	MAX	UNITS
$t_{\text{DSS}}$	SCLK high after $\overline{\text{DRDY}}/\text{DOUT}$ goes low to activate Standby mode	SPEED = 1	0	12.44	ms
		SPEED = 0	0	99.94	ms
$t_{\text{STANDBY}}$	Standby mode activation time	SPEED = 1	20		$\mu\text{s}$
		SPEED = 0	20		$\mu\text{s}$
$t_{\text{S\_RDY}}$	Data ready after exiting Standby mode	SPEED = 1	52.51	52.51	ms
		SPEED = 0	401.8	401.8	ms

### POWER-UP SEQUENCE

When powering up the ADS1130, AVDD and DVDD must be powered up before the PDWN pin goes high, as shown in Figure 8. If PDWN is not controlled by a microprocessor, a simple RC delay circuit must be implemented, as shown in Figure 9.

### POWER-DOWN MODE

Power-Down mode shuts down the entire ADC circuitry and reduces the total power consumption close to zero. To enter Power-Down mode, simply hold the PDWN pin low. Power-Down mode also resets the entire circuitry to free the ADC circuitry from locking up to an unknown state. Power-Down mode can be initiated at any time during readback; it is not necessary to retrieve all 18 bits of data beforehand. Figure 10 shows the wake-up timing from Power-Down mode.

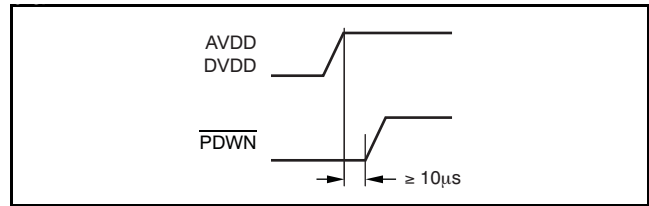
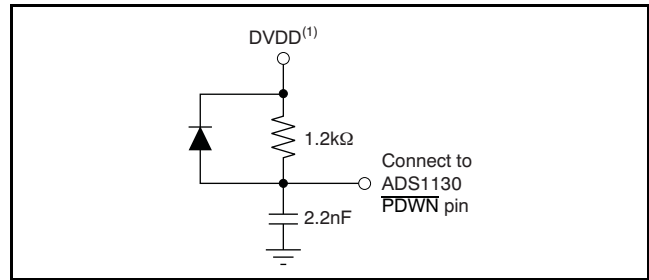


Figure 8. Power-Up Timing Sequence



(1) AVDD must be powered up at least 10µs before PDWN goes high.

Figure 9. RC Delay Circuit

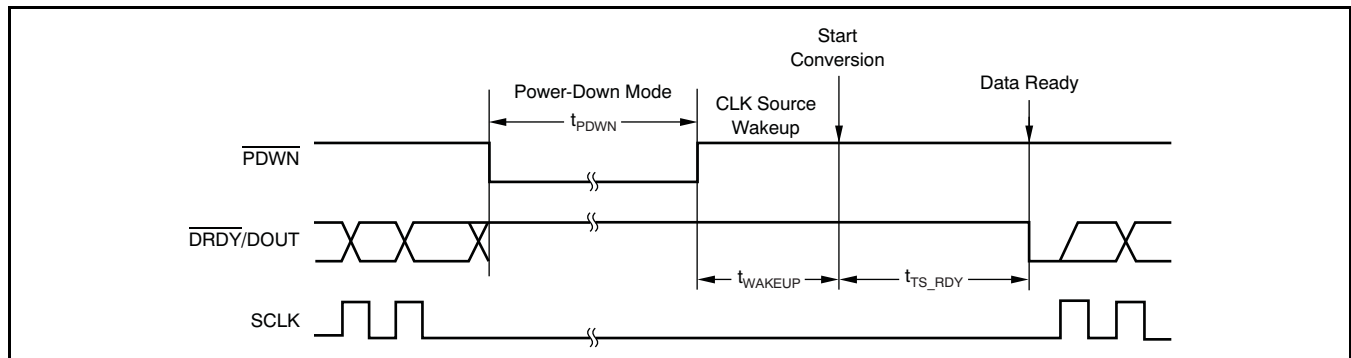


Figure 10. Wake-Up Timing from Power-Down Mode

SYMBOL	DESCRIPTION	MIN	TYP	UNITS
$t_{WAKEUP}$	Wake-up time after Power-Down mode		8	µs
$t_{PDWN}$	$\overline{PDWN}$ pulse width	30		µs

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**REVISION HISTORY**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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**Changes from Original (June 2009) to Revision A** **Page**

- 
- Deleted NRND watermark ..... 1
-

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1130IPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1130	<a href="#">Samples</a>
ADS1130IPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1130	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1130IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

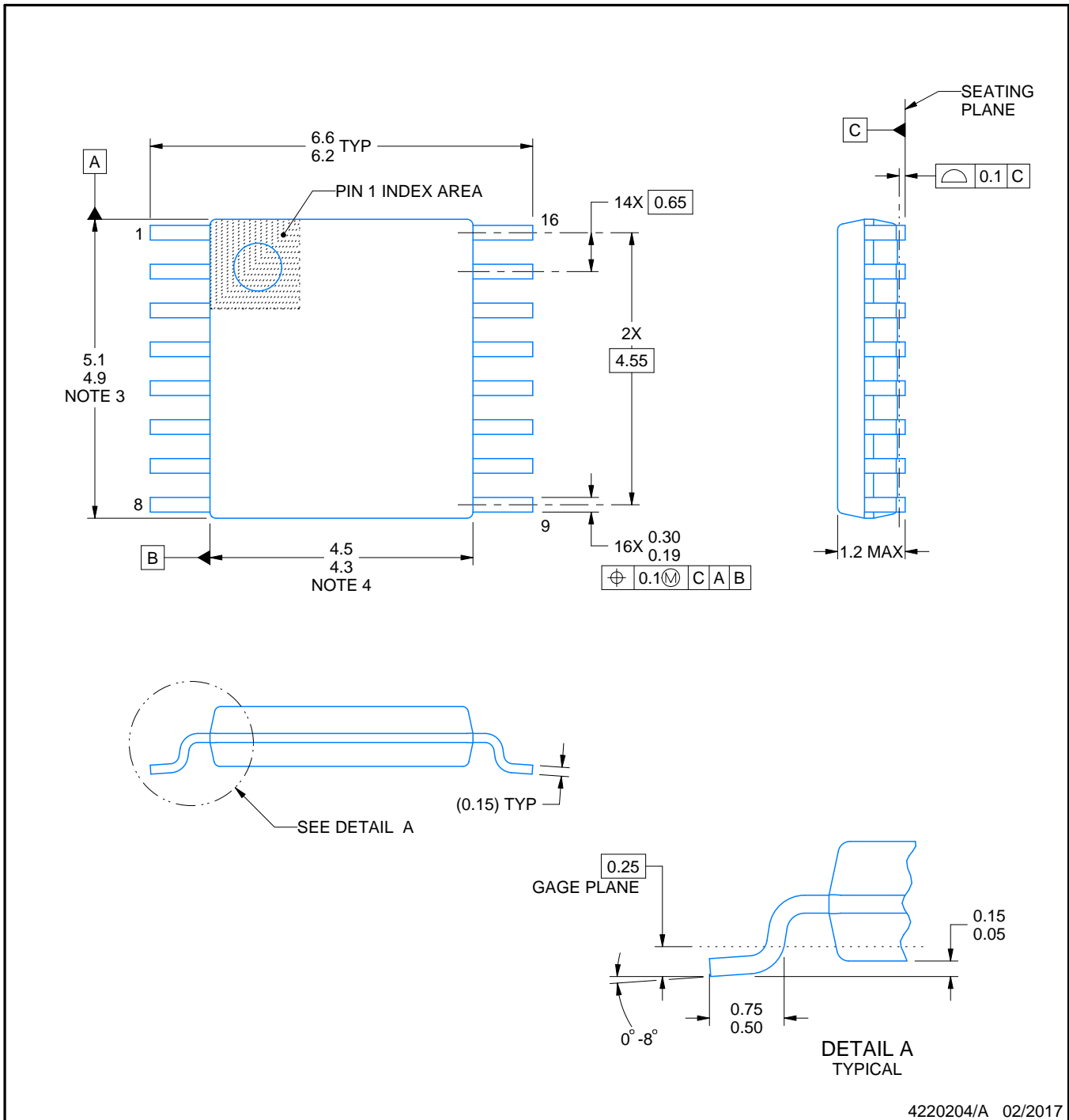

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1130IPWR	TSSOP	PW	16	2000	350.0	350.0	43.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
ADS1130IPW	PW	TSSOP	16	90	530	10.2	3600	3.5



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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