

# ADS7138 小型 8 通道 12 位 ADC, 具有 I<sup>2</sup>C 接口、GPIO 和 CRC

## 1 特性

- 小封装尺寸:
  - 3mm x 3mm WQFN
- 8 通道, 可配置为以下任意组合:
  - 最多 8 个模拟输入、数字输入或数字输出
- 用于 I/O 扩展的 GPIO:
  - 开漏、推挽数字输出
- 模拟监控:
  - 每个通道的可编程阈值
  - 用于瞬态抑制的事件计数器
- 宽工作范围:
  - AVDD: 2.35V 至 5.5V
  - DVDD: 1.65V 至 5.5V
  - 温度范围: -40°C 至 +125°C
- 用于读取/写入操作的 CRC:
  - 数据读取/写入 CRC
  - 上电配置 CRC
- I<sup>2</sup>C 接口:
  - 高达 3.4MHz (高速)
  - 8 个可配置 I<sup>2</sup>C 地址
- 可编程均值滤波器:
  - 用于求平均值的可编程样本大小
  - 利用内部转换求平均值

- 用于计算平均输出的 16 位分辨率

## 2 应用

- 监控功能
- 便携式仪表
- 电信基础设施
- 电源监控

## 3 说明

ADS7138 是一款易于使用的 8 通道多路复用 12 位逐次逼近寄存器模数转换器 (SAR ADC)。8 个通道可独立配置为模拟输入、数字输入或数字输出。该器件具有一个用于执行 ADC 转换过程的内部振荡器。

ADS7138 通过兼容 I<sup>2</sup>C 的接口进行通信, 可以在自主或单冲转换模式下运行。ADS7138 使用具有可编程高低阈值、迟滞和事件计数器的数字窗口比较器, 通过每通道事件触发的中断来实施模拟监控功能。ADS7138 具有用于数据读取/写入操作和上电配置的内置循环冗余校验 (CRC) 功能。

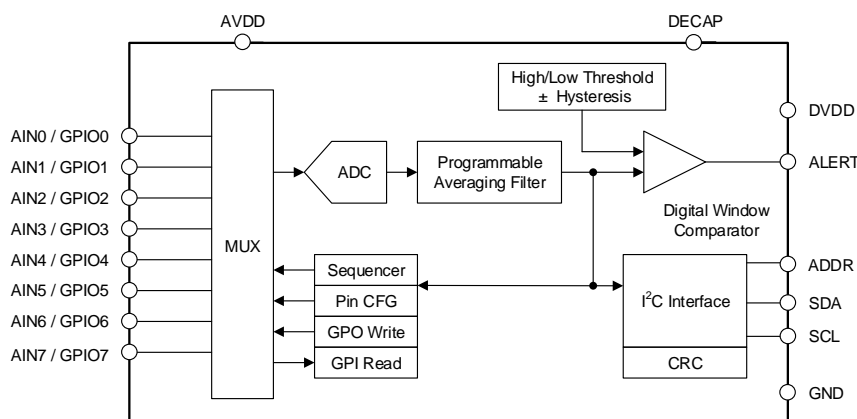
器件信息<sup>(1)</sup>

部件名称	封装	封装尺寸 (标称值)
ADS7138	WQFN (16)	3.00mm x 3.00mm

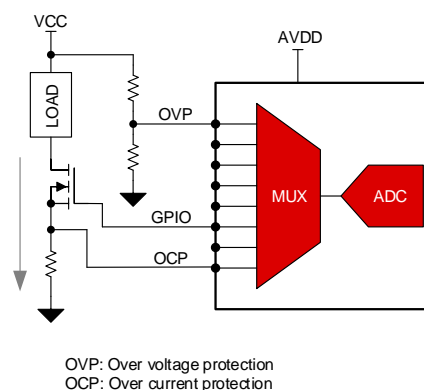
(1) 如需了解所有可用封装, 请见数据表末尾的可订购产品附录。

## ADS7138 方框图和应用

Device Block Diagram



Example System Architecture



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## 4 修订历史记录

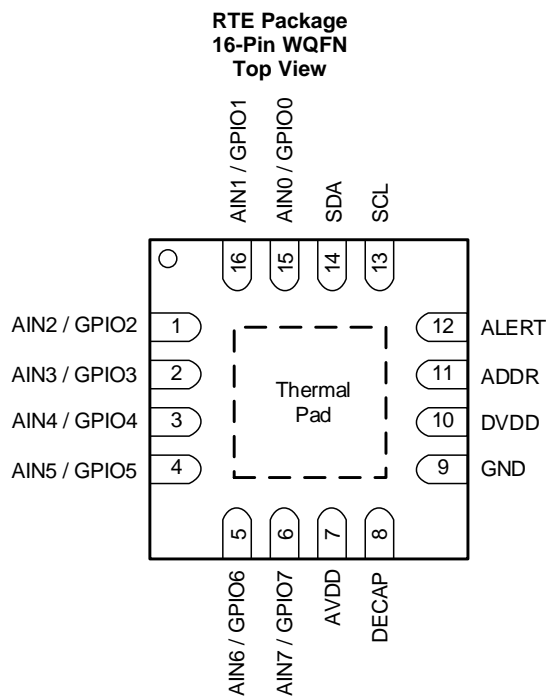
注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2019 年 5 月	*	初始发行版。

## 5 Device Comparison Table

PART NUMBER	DESCRIPTION	CRC MODULE	ZERO-CROSSING-DETECT (ZCD) MODULE	ROOT-MEAN-SQUARE (RMS) MODULE
ADS7128	8-channel, 12-bit ADC with I <sup>2</sup> C interface and GPIOs	Yes	Yes	Yes
ADS7138		Yes	No	No
ADS7138-Q1		Yes	No	No

## 6 Pin Configuration and Functions



**Pin Functions**

PIN		FUNCTION <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
AIN0/GPIO0	15	AI, DI, DO	Channel 0; configurable as either an analog input (default) or a general-purpose input/output (GPIO)
AIN1/GPIO1	16	AI, DI, DO	Channel 1; configurable as either an analog input (default) or a GPIO
AIN2/GPIO2	1	AI, DI, DO	Channel 2; configurable as either an analog input (default) or a GPIO
AIN3/GPIO3	2	AI, DI, DO	Channel 3; configurable as either an analog input (default) or a GPIO
AIN4/GPIO4	3	AI, DI, DO	Channel 4; configurable as either an analog input (default) or a GPIO
AIN5/GPIO5	4	AI, DI, DO	Channel 5; configurable as either an analog input (default) or a GPIO
AIN6/GPIO6	5	AI, DI, DO	Channel 6; configurable as either an analog input (default) or a GPIO
AIN7/GPIO7	6	AI, DI, DO	Channel 7; configurable as either an analog input (default) or a GPIO
ADDR	11	AI	Input for selecting the device I <sup>2</sup> C address. Connect a resistor to this pin from DECAP pin or GND to select one of the eight addresses.
ALERT	12	Digital output	Open-drain (default) or push-pull output for the digital comparator
AVDD	7	Supply	Analog supply input, also used as the reference voltage to the ADC; connect a 1- $\mu$ F decoupling capacitor to GND
DECAP	8	Supply	Connect a decoupling capacitor to this pin for the internal power supply
DVDD	10	Supply	Digital I/O supply voltage; connect a 1- $\mu$ F decoupling capacitor to GND
GND	9	Supply	Ground for the power supply; all analog and digital signals are referred to this pin voltage
SDA	14	DI, DO	Serial data input or output for the I <sup>2</sup> C interface
SCL	13	DI	Serial clock for the I <sup>2</sup> C interface

(1) AI = analog input, DI = digital input, and DO = digital output.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
DVDD to GND	-0.3	5.5	V
AVDD to GND	-0.3	5.5	V
AINx/GPOx <sup>(2)</sup>	GND - 0.3	AVDD + 0.3	V
ADDR	GND - 0.3	2.1	V
Digital inputs	GND - 0.3	5.5	V
Current through any pin except supply pins <sup>(3)</sup>	-10	10	mA
Junction temperature, T <sub>J</sub>	-40	125	°C
Storage temperature, T <sub>stg</sub>	-60	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) AINx/GPIOx refers to pins 1, 2, 3, 4, 5, 6, 15, and 16.
- (3) Pin current must be limited to 10mA or less.

### 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER SUPPLY</b>						
AVDD	Analog supply voltage		2.35	3.3	5.5	V
DVDD	Digital supply voltage		1.65	3.3	5.5	V
<b>ANALOG INPUTS</b>						
FSR	Full-scale input range	AIN <sub>x</sub> <sup>(1)</sup> - GND	0		AVDD	V
V <sub>IN</sub>	Absolute input voltage	AIN <sub>x</sub> - GND	-0.1		AVDD + 0.1	V
<b>TEMPERATURE RANGE</b>						
T <sub>A</sub>	Ambient temperature		-40	25	125	°C

- (1) AINx refers to AIN0, AIN1, AIN2, AIN3, AIN4, AIN5, AIN6, and AIN7.

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		ADS7138	
		RTE (WQFN)	
		16 PINS	
			UNIT
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	49.7	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	53.4	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	24.7	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.3	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	24.7	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	9.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

at AVDD = 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at TA = -40°C to +125°C; typical values at TA = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ANALOG INPUTS</b>						
C <sub>SH</sub>	Sampling capacitance			12		pF
<b>DC PERFORMANCE</b>						
	Resolution	No missing codes		12		bits
DNL	Differential nonlinearity		-0.9	±0.2	0.9	LSB
INL	Integral nonlinearity		-2	±0.5	2	LSB
V <sub>(OS)</sub>	Input offset error	Post offset calibration	-2	±0.3	2	LSB
	Input offset thermal drift	Post offset calibration		±5		ppm/°C
	Offset error match		-1	±0.5	1	LSB
G <sub>E</sub>	Gain error		-0.1	±0.05	0.1	%FSR
	Gain error thermal drift			±5		ppm/°C
	Gain error match		-0.05	±0.01	0.05	%FSR
<b>AC PERFORMANCE</b>						
SINAD	Signal-to-noise + distortion ratio	AVDD = 5 V, f <sub>IN</sub> = 2 kHz	68.5	71.5		dB
		AVDD = 3 V, f <sub>IN</sub> = 2 kHz	67.5	70.5		
SNR	Signal-to-noise ratio	AVDD = 5 V, f <sub>IN</sub> = 2 kHz	69	72		dB
		AVDD = 3 V, f <sub>IN</sub> = 2 kHz	68	71		
THD	Total harmonic distortion	f <sub>IN</sub> = 2 kHz		-85		dB
SFDR	Spurious-free dynamic range	f <sub>IN</sub> = 2 kHz		91		dB
	Crosstalk	100-kHz signal applied on any OFF channel and measured on ON the channel		-100		dB
<b>DECAP Pin</b>						
	Decoupling capacitor on DECAP pin		0.22	1		μF
<b>DIGITAL INPUT/OUTPUT (SCL, SDA)</b>						
V <sub>IH</sub>	Input high logic level	All I <sup>2</sup> C modes	0.7 x DVDD		DVDD	V
V <sub>IL</sub>	Input low logic level	All I <sup>2</sup> C modes	-0.3		0.3 x DVDD	V
V <sub>OL</sub>	Output low logic level	Sink current = 2 mA, DVDD > 2 V	0		0.4	V
		Sink current = 2 mA, DVDD ≤ 2 V	0		0.2 x DVDD	
I <sub>OL</sub>	Low-level output current (sink)	V <sub>OL</sub> = 0.4 V, standard and fast Mode			3	mA
		V <sub>OL</sub> = 0.6 V, fast mode			6	
		V <sub>OL</sub> = 0.4 V, fast mode plus			20	
<b>GPIOs</b>						
V <sub>IH</sub>	Input high logic level		0.7 x AVDD		AVDD + 0.3	V
V <sub>IL</sub>	Input low logic level		-0.3		0.3 x AVDD	V
	Input leakage current	GPIO configured as input		10	100	nA
V <sub>OH</sub>	Output high logic level	GPO_DRIVE_CFG = push-pull, I <sub>SOURCE</sub> = 2 mA	0.8 x AVDD		AVDD	V
V <sub>OL</sub>	Output low logic level	I <sub>SINK</sub> = 2 mA	0		0.2 x AVDD	V
I <sub>OH</sub>	Output high source current	V <sub>OH</sub> > 0.7 x AVDD			5	mA
I <sub>OL</sub>	Output low sink current	V <sub>OL</sub> < 0.3 x AVDD			5	mA
<b>DIGITAL OUTPUT (ALERT)</b>						
V <sub>OH</sub>	Output high logic level	GPO_DRIVE_CFG = push-pull, I <sub>SOURCE</sub> = 2 mA	0.8 x DVDD		DVDD	V
V <sub>OL</sub>	Output low logic level	I <sub>SINK</sub> = 2 mA	0		0.2 x DVDD	V

## Electrical Characteristics (continued)

at AVDD = 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T<sub>A</sub> = –40°C to +125°C; typical values at T<sub>A</sub> = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>OH</sub>	Output high sink current	V <sub>OH</sub> > 0.7 x DVDD			5	mA
I <sub>OL</sub>	Output low sink current	V <sub>OL</sub> < 0.3 x DVDD			5	mA
<b>POWER SUPPLY CURRENTS</b>						
I <sub>AVDD</sub>	Analog supply current	I <sup>2</sup> C high-speed mode, AVDD = 5 V		260	430	μA
		I <sup>2</sup> C fast mode plus, AVDD = 5 V		83	140	
		I <sup>2</sup> C fast mode, AVDD = 5 V		35	57	
		I <sup>2</sup> C standard mode, AVDD = 5 V		10	20	
		No conversion, AVDD = 5 V		5	15	

## 7.6 I<sup>2</sup>C Timing Requirements

	PARAMETER	TEST CONDITIONS	MODE				UNIT
			FAST MODE		HIGH-SPEED MODE		
			MIN	MAX	MIN	MAX	
f <sub>SCL</sub>	SCL clock frequency <sup>(1)</sup>		1		3.4	MHz	
t <sub>SUSTA</sub>	START condition setup time for repeated start		260		160	ns	
t <sub>HDSTA</sub>	Start condition hold time		260		160	ns	
t <sub>LOW</sub>	Clock low period		500		160	ns	
t <sub>HIGH</sub>	Clock high period		260		60	ns	
t <sub>SUDAT</sub>	Data in setup time		50		10	ns	
t <sub>HDDAT</sub>	Data in hold time		0		0	ns	
t <sub>R</sub>	SCL rise time			120		80	ns
t <sub>F</sub>	SCL fall time			120		80	ns
t <sub>SUSTO</sub>	STOP condition hold time		260		60	ns	
t <sub>BUF</sub>	Bus free time before new transmission		500		300	ns	

(1) Bus load (C<sub>B</sub>) consideration; C<sub>B</sub> ≤ 400 pF for f<sub>SCL</sub> ≤ 1 MHz; C<sub>B</sub> < 100 pF for f<sub>SCL</sub> = 3.4 MHz.

## 7.7 Timing Requirements

at AVDD = 2.35 V to 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T<sub>A</sub> = –40°C to +125°C; typical values at T<sub>A</sub> = 25°C.

		MIN	MAX	UNIT
t <sub>ACQ</sub>	Acquisition time	300		ns

## 7.8 I<sup>2</sup>C Switching Characteristics

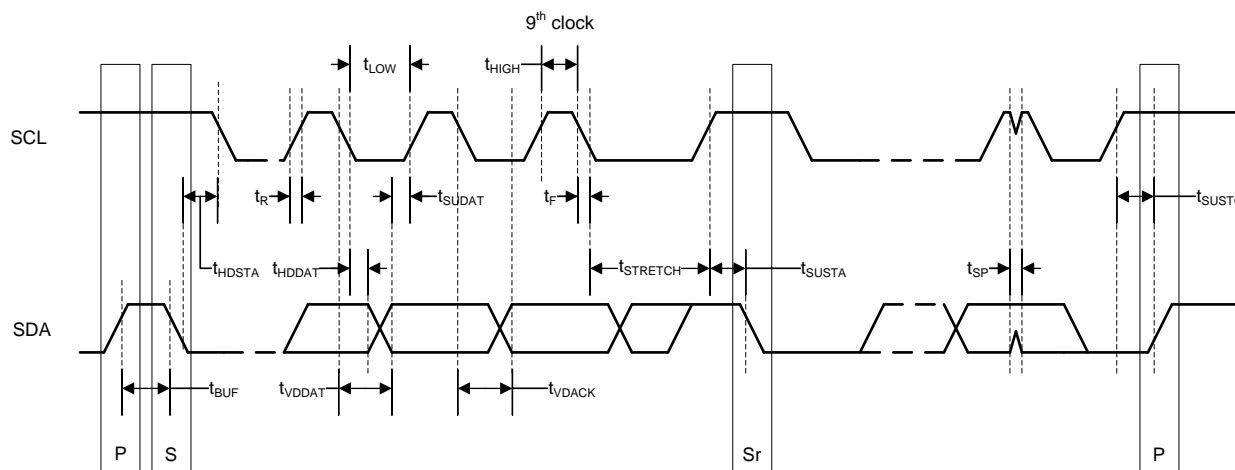
	PARAMETER	TEST CONDITIONS	MODE				UNIT
			FAST MODE		HIGH-SPEED MODE		
			MIN	MAX	MIN	MAX	
t <sub>VDDATA</sub>	SCL low to SDA data out valid		450		200	ns	
t <sub>VDACK</sub>	SCL low to SDA acknowledge time		450		200	ns	
t <sub>STRETCH</sub>	Clock stretch time in one-shot conversion mode; during ADC conversion		1200		950	ns	
t <sub>SP</sub>	Noise suppression time constant on SDA and SCL		50		10	ns	

### 7.9 Switching Characteristics

at AVDD = 2.35 V to 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at TA = -40°C to +125°C; typical values at TA = 25°C.

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT	
<b>CONVERSION CYCLE</b>					
t <sub>CONV</sub>	ADC conversion time	Manual and auto sequence modes	t <sub>STRETCH</sub>	ns	
		Autonomous mode	550	ns	
<b>RESET AND ALERT</b>					
t <sub>PU</sub>	Power-up time for device	AVDD ≥ 2.35 V	5	ms	
t <sub>RST</sub>	Delay time; RST bit = 1b to device reset complete <sup>(1)</sup>		5	ms	
t <sub>ALERT_HI</sub>	ALERT high period	ALERT_LOGIC[1:0] = 1x	85	105	ns
t <sub>ALERT_LO</sub>	ALERT low period	ALERT_LOGIC[1:0] = 1x	85	105	ns

(1) RST bit is automatically reset to 0b after t<sub>RST</sub>.



NOTE: S = start, Sr = repeated start, and P = stop.

图 1. I<sup>2</sup>C Timing Diagram

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## 8 Detailed Description

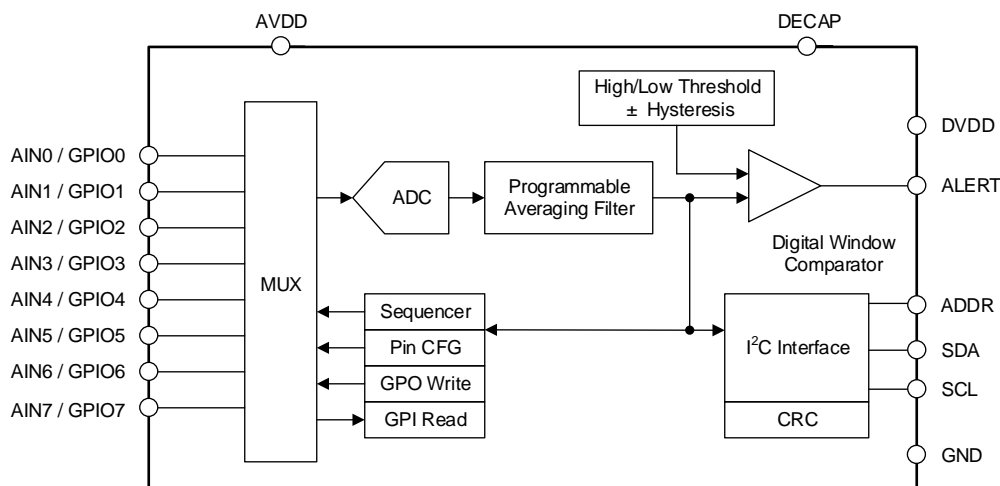
### 8.1 Overview

The ADS7138 is a small, eight-channel, multiplexed, 12-bit, analog-to-digital converter (ADC) with an I<sup>2</sup>C-compatible serial interface. The eight channels of the ADS7138 can be individually configured as either analog inputs, digital inputs, or digital outputs. The device includes a digital comparator with a dedicated alert pin that can be used to interrupt the host when a programmed high or low threshold is crossed on any input channel. The device uses an internal oscillator for conversion. The ADC can be used in the manual mode for reading ADC data over the I<sup>2</sup>C interface or in autonomous mode for monitoring the analog inputs without an active I<sup>2</sup>C interface.

The device features a programmable averaging filter that outputs a 16-bit result for enhanced resolution.

The I<sup>2</sup>C serial interface supports standard-mode, fast-mode, fast-mode plus, and high-speed mode. The device also features an 8-bit cyclic redundancy check (CRC) for the serial communication interface.

### 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Multiplexer and ADC

The eight channels of the multiplexer can be independently configured as ADC inputs or general-purpose inputs/outputs (GPIOs). 图 2 shows that each input pin has electrostatic discharge (ESD) protection diodes to AVDD and GND. On power-up or after device reset, all eight multiplexer channels are configured as analog inputs.

图 2 shows an equivalent circuit for pins configured as analog inputs. The ADC sampling switch is represented by an ideal switch (SW) in series with the resistor,  $R_{SW}$  (typically 150  $\Omega$ ), and the sampling capacitor,  $C_{SH}$  (typically 12 pF).

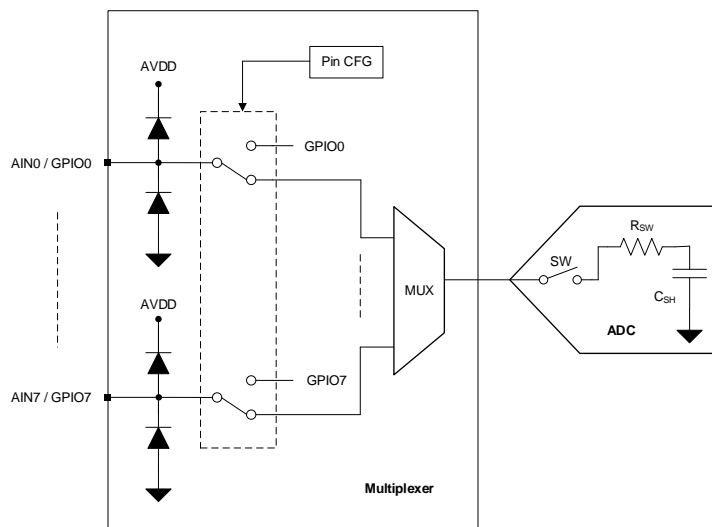


图 2. Analog Inputs, GPIOs, and ADC Connections

During acquisition, the SW switch is closed to allow the signal on the selected analog input channel to charge the internal sampling capacitor. During conversion, the SW switch is opened to disconnect the analog input channel from the sampling capacitor.

The multiplexer channels can be configured as GPIOs in the PIN\_CFG register. The direction of a GPIO (either as an input or an output) can be set in the GPIO\_CFG register. The logic level on the channels configured as digital inputs can be read from the GPI\_VALUE register. The digital outputs can be accessed by writing to the GPO\_OUTPUT\_VALUE register. The digital outputs can be configured as either open-drain or push-pull in the GPO\_DRIVE\_CFG register.

### 8.3.2 Reference

The device uses the analog supply voltage (AVDD) as a reference for the analog-to-digital conversion process. TI recommends connecting a 1- $\mu$ F, low-equivalent series resistance (ESR) ceramic decoupling capacitor between the AVDD and GND pins.

### 8.3.3 ADC Transfer Function

The ADC output is in straight binary format. 公式 1 computes the ADC resolution:

$$1 \text{ LSB} = V_{REF} / 2^N$$

where:

- $V_{REF} = AVDD$
- $N = 12$

(1)

图 3 和 表 1 detail the transfer characteristics for the device.

Feature Description (接下页)

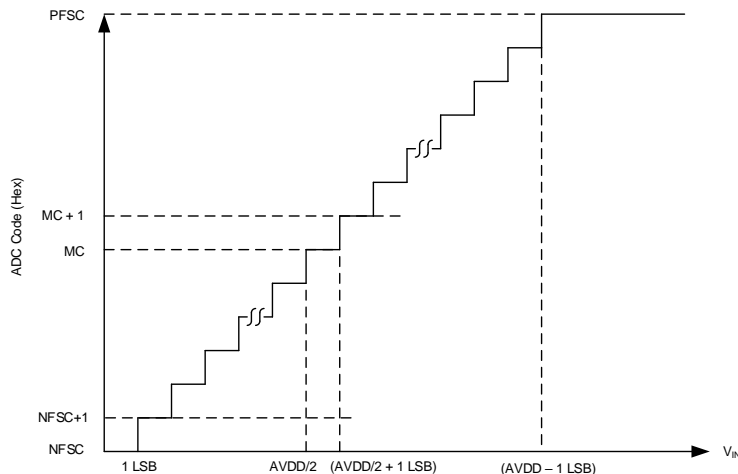


图 3. Ideal Transfer Characteristics

表 1. Transfer Characteristics

INPUT VOLTAGE	CODE	DESCRIPTION	IDEAL OUTPUT CODE
$\leq 1$ LSB	NFSC	Negative full-scale code	000
1 LSB to 2 LSBs	NFSC + 1	—	001
$(AVDD / 2)$ to $(AVDD / 2) + 1$ LSB	MC	Mid code	800
$(AVDD / 2) + 1$ LSB to $(AVDD / 2) + 2$ LSB	MC + 1	—	801
$\geq AVDD - 1$ LSB	PFSC	Positive full-scale code	FFF

8.3.4 ADC Offset Calibration

The variation in ADC offset error resulting from changes in temperature or AVDD can be calibrated by setting the CAL bit in the GENERAL\_CFG register. The CAL bit is reset to 0 after calibration. The host can poll the CAL bit to check the ADC offset calibration completion status.

8.3.5 I<sup>2</sup>C Address Selector

The I<sup>2</sup>C address for the device is determined by connecting external resistors on the ADDR pin. The device address is determined at power-up based on the resistor values. The device retains this address until the next power-up event, until the next device reset, or until the device receives a command to program its own address. 图 4 shows a connection diagram for the ADDR pin and 表 2 lists the resistor values for selecting different addresses of the device.

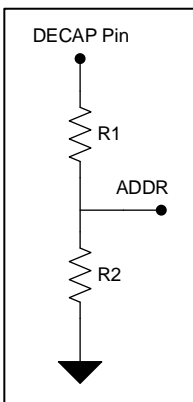


图 4. External Resistor Connection Diagram for the ADDR Pin

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表 2. I<sup>2</sup>C Address Selection

RESISTORS		ADDRESS
R1 <sup>(1)</sup>	R2 <sup>(1)</sup>	
0 Ω	DNP <sup>(2)</sup>	001 0111b (17h)
11 kΩ	DNP <sup>(2)</sup>	001 0110b (16h)
33 kΩ	DNP <sup>(2)</sup>	001 0101b (15h)
100 kΩ	DNP <sup>(2)</sup>	001 0100b (14h)
DNP <sup>(2)</sup>	0 Ω or DNP <sup>(2)</sup>	001 0000b (10h)
DNP <sup>(2)</sup>	11 kΩ	001 0001b (11h)
DNP <sup>(2)</sup>	33 kΩ	001 0010b (12h)
DNP <sup>(2)</sup>	100 kΩ	001 0011b (13h)

- (1) Tolerance for R1, R2 ≤ ±5%.
- (2) DNP = Do not populate.

### 8.3.6 Programmable Averaging Filter

The ADS7138 features a built-in oversampling (OSR) function that can be used to average several samples. The averaging filter can be enabled by programming the OSR[2:0] bits in the OSR\_CFG register. The averaging filter configuration is common to all analog input channels. 图 5 shows that the averaging filter module output is 16 bits long. In the manual conversion mode and auto-sequence mode, only the first conversion for the selected analog input channel must be initiated by the host; see the *Manual Mode* and *Auto-Sequence Mode* sections. As shown in 图 5, any remaining conversions for the selected averaging factor are generated internally. The time required to complete the averaging operation is determined by the sampling speed and number of samples to be averaged. As shown in 图 5, the 16-bit result can be read out after the averaging operation completes.

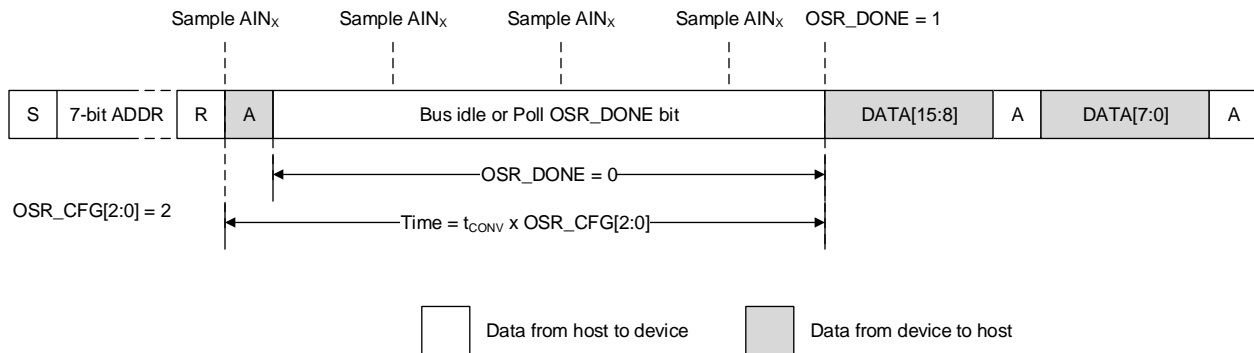


图 5. Averaging Example

In 图 5, SCL is stretched by the device after the start of conversions until the averaging operation is complete.

If SCL stretching is not required during averaging, enable the statistics registers by setting STATS\_EN to 1b and initiate conversions by writing 1b to the CNVST bit. The OSR\_DONE bit in the SYSTEM\_STATUS register can be polled to check the averaging completion status. When using the CNVST bit to initiate conversion, the result can be read in the RECENT\_CHx\_LSB and RECENT\_CHx\_MSB registers.

In the autonomous mode of operation, samples from the analog input channels that are enabled in the AUTO\_SEQ\_CH\_SEL register are averaged sequentially; see the *Autonomous Mode* section. The digital window comparator compares the top 12 bits of the 16-bit average result with the thresholds.

公式 2 provides the LSB value of the 16-bit average result.

$$1 \text{ LSB} = \frac{AVDD}{2^{16}} \tag{2}$$

### 8.3.7 CRC on Data Interface

The ADS7138 features a cyclic redundancy check (CRC) module for checking the integrity of the data bits exchanged over the I<sup>2</sup>C interface. The CRC module is bidirectional and appends an 8-bit CRC to every byte read from the device while also evaluating the CRC of every incoming byte over the I<sup>2</sup>C interface. The CRC module uses the CRC-8-CCITT polynomial ( $x^8 + x^2 + x + 1$ ) for CRC computation.

To enable the CRC module, set the CRC\_EN bit in the GENERAL\_CFG register. 表 3 shows how a CRC error can be detected when configuring the ADS7138.

**表 3. Configuration Notifications When a CRC Error is Detected**

CRC ERROR NOTIFICATION	CONFIGURATION	DESCRIPTION
ALERT pin	ALERT_CRCIN = 1b	ALERT pin is asserted if a CRC error is detected by the device.
Status flags	APPEND_STATUS = 10b	4-bit status flags are appended to the ADC data; see the <a href="#">Output Data Format</a> section for details.
Register read	—	Read the CRC_ERR_IN bit to check if a CRC error is detected.

When the ADS7138 detects a CRC error, the erroneous data are ignored and the CRC\_ERR\_IN bit is set. 表 3 describes the additional notifications that can be enabled. Further register writes are disabled until the CRC\_ERR\_IN bit is cleared by writing 1b to it. When using autonomous mode, further conversions can be disabled on the CRC error by setting CONV\_ON\_ERR to 1b; see the [Autonomous Mode](#) section.

### 8.3.8 General-Purpose I/Os (GPIOs)

The eight channels of the ADS7138 can be independently configured as analog inputs, digital inputs, or digital outputs. 表 4 describes how the PIN\_CFG and GPIO\_CFG registers can be used to configure the channels.

**表 4. Configuring Channels as Analog Inputs or GPIOs**

PIN_CFG[7:0]	GPIO_CFG[7:0]		GPO_DRIVE_CFG[7:0]	CHANNEL CONFIGURATION
0	x		x	Analog input (default)
1	0		x	Digital input
1	1		0	Digital output; open-drain driver
1	1		1	Digital output; push-pull driver

The digital outputs can be configured to logic 1 or 0 by writing to the GPO\_OUTPUT\_VALUE register. Reading the GPI\_VALUE register returns the logic level for all channels configured as digital inputs.

### 8.3.9 Oscillator and Timing Control

The device uses an internal oscillator for conversions. When using the averaging module, the host initiates the first conversion and all subsequent conversions are generated internally by the device. 表 5 shows that when the device generates the start of the conversion, the sampling rate is controlled by the OSC\_SEL and CLK\_DIV[3:0] register fields.

**表 5. Configuring Sampling Rate for Internal Conversion Start Control**

CLK_DIV[3:0]	OSC_SEL = 0		OSC_SEL = 1	
	SAMPLING FREQUENCY, $f_{\text{CYCLE}}$ (kSPS)	CYCLE TIME, $t_{\text{CYCLE}}$ ( $\mu\text{s}$ )	SAMPLING FREQUENCY, $f_{\text{CYCLE}}$ (kSPS)	CYCLE TIME, $t_{\text{CYCLE}}$ ( $\mu\text{s}$ )
0000b	1000	1	31.25	32
0001b	666.7	1.5	20.83	48
0010b	500	2	15.63	64
0011b	333.3	3	10.42	96
0100b	250	4	7.81	128
0101b	166.7	6	5.21	192
0110b	125	8	3.91	256
0111b	83	12	2.60	384
1000b	62.5	16	1.95	512
1001b	41.7	24	1.3	768
1010b	31.3	32	0.98	1024
1011b	20.8	48	0.65	1536
1100b	15.6	64	0.49	2048
1101b	10.4	96	0.33	3072

The conversion time of the device (see  $t_{\text{CONV}}$  in the [Switching Characteristics](#) table) is independent of the OSC\_SEL and CLK\_DIV[3:0] configuration.

#### 8.3.10 Output Data Format

图 6 illustrates various I<sup>2</sup>C frames for reading data.

- Read the ADC conversion result: Two 8-bit I<sup>2</sup>C packets are required (frame A).
- Read the averaged conversion result: Two 8-bit I<sup>2</sup>C packets are required (frame B).
- Read data with the channel ID appended: The 4-bit channel ID can be appended to the 12-bit ADC result by configuring the APPEND\_STATUS field in the GENERAL\_CFG register. When the channel ID appended to the 12-bit ADC data, two I<sup>2</sup>C packets are required (frame C). If the channel ID appended to the 16-bit average result, three I<sup>2</sup>C frames are required (frame D).

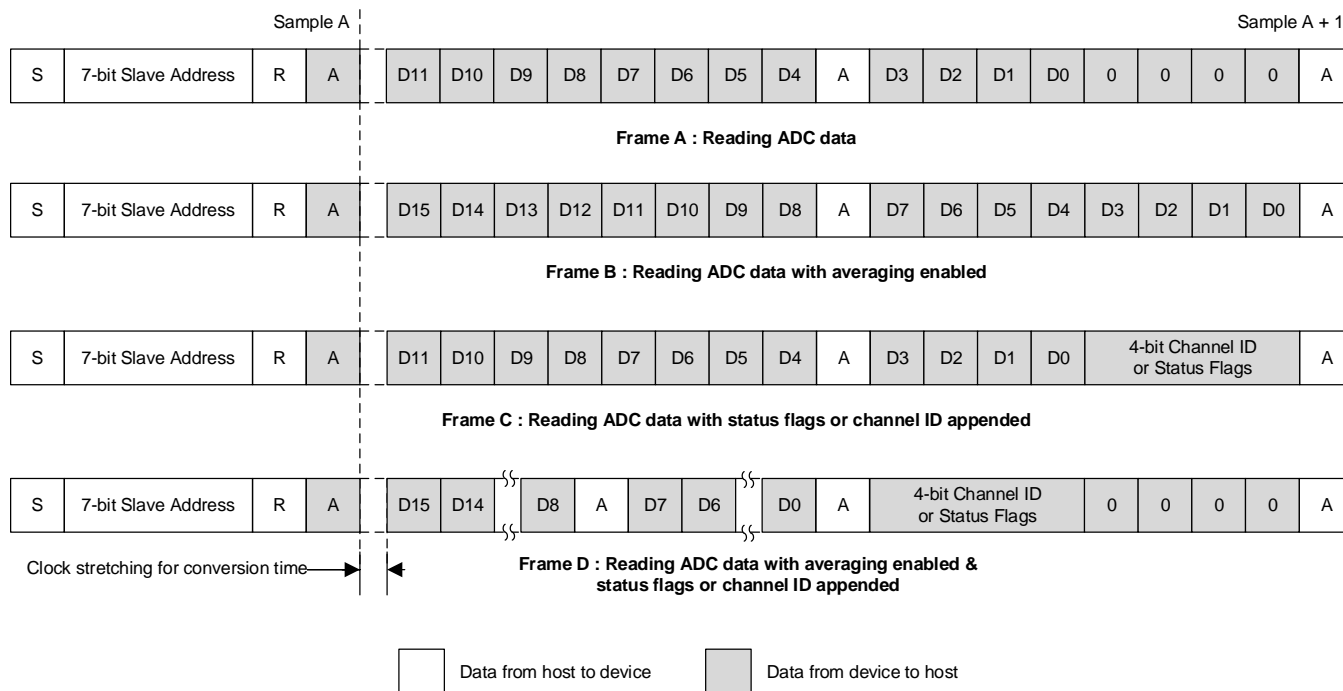


图 6. Data Frames for Reading Data

When status flags are enabled, APPEND\_STATUS is set to 10b and four bits are appended to the ADC output. The device outputs status flags in this order: {1b, 0b, CRCERR\_IN, ALERT}. The level transitions on the digital interface, resulting from the fixed 1b and 0b in the status flags, can be used to detect if the digital outputs are shorted to a fixed register voltage in the system. The CRCERR\_IN flag reflects the corresponding bit in the GENERAL\_CFG register. The ALERT flag is the output of the logical OR of the bits in the EVENT\_FLAG register.

### 8.3.11 Digital Window Comparator

The internal digital window comparator (DWC) is available in all functional modes of the device (see the [Device Functional Modes](#) section for details). The digital window comparator controls output of the ALERT pin buffer. The ALERT pin can be configured as open-drain (default) or push-pull output using the ALERT\_DRIVE bit in the ALERT\_PIN\_CFG register. 图 7 shows a block diagram for the digital window comparator.

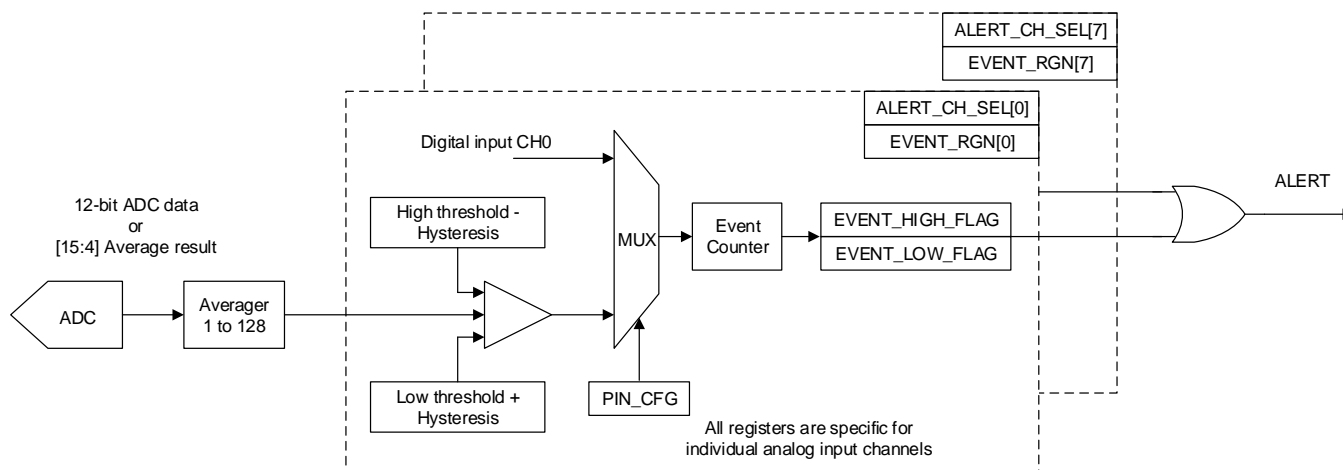
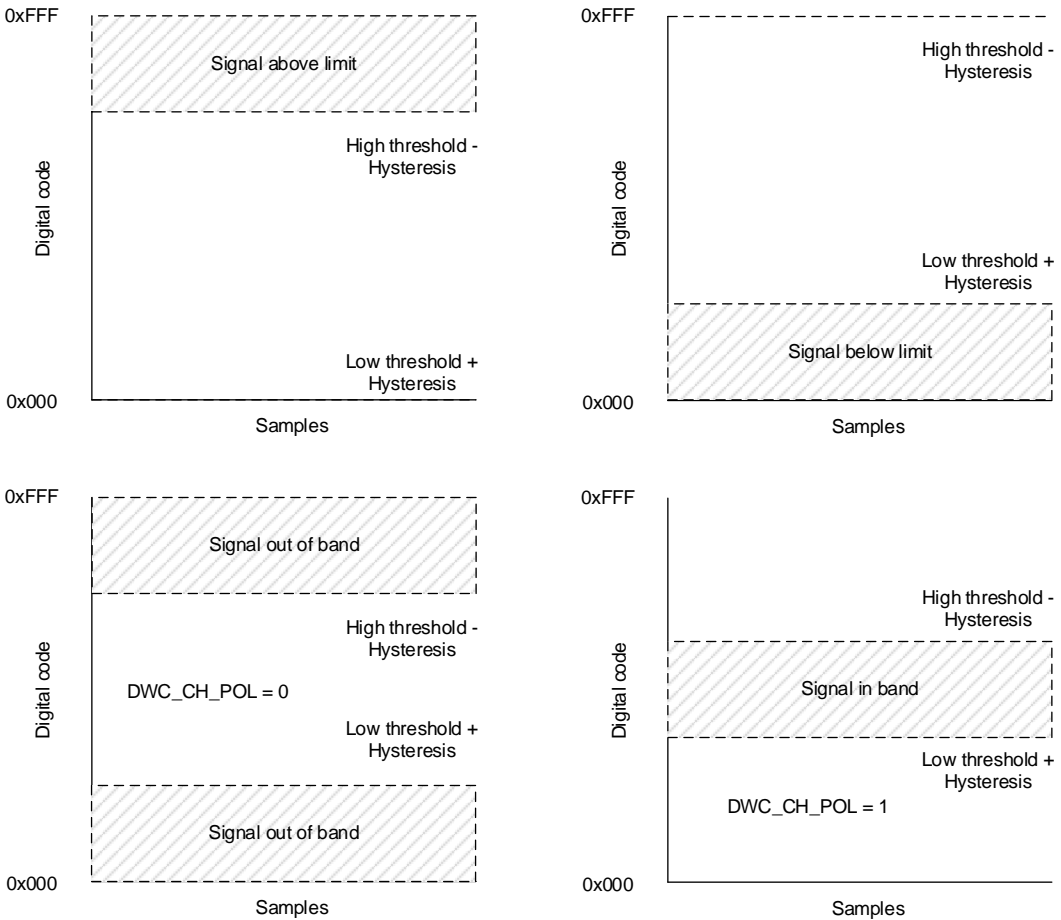
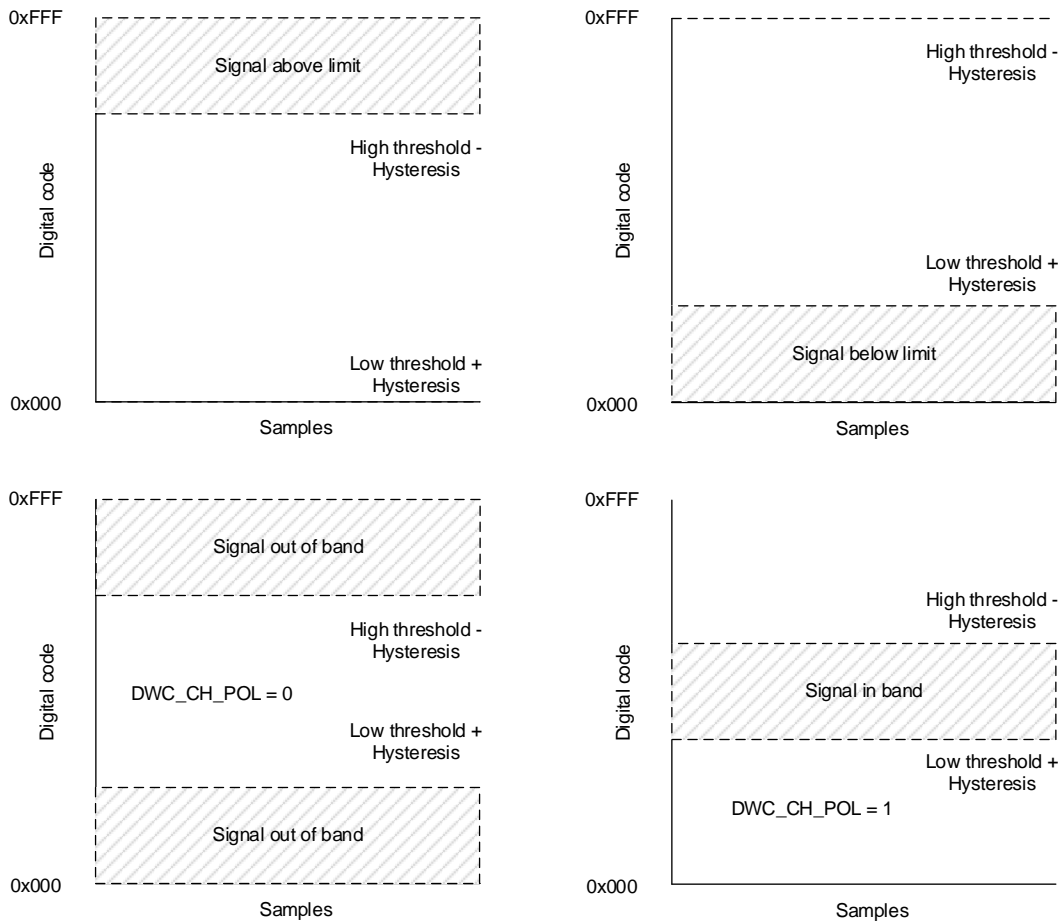
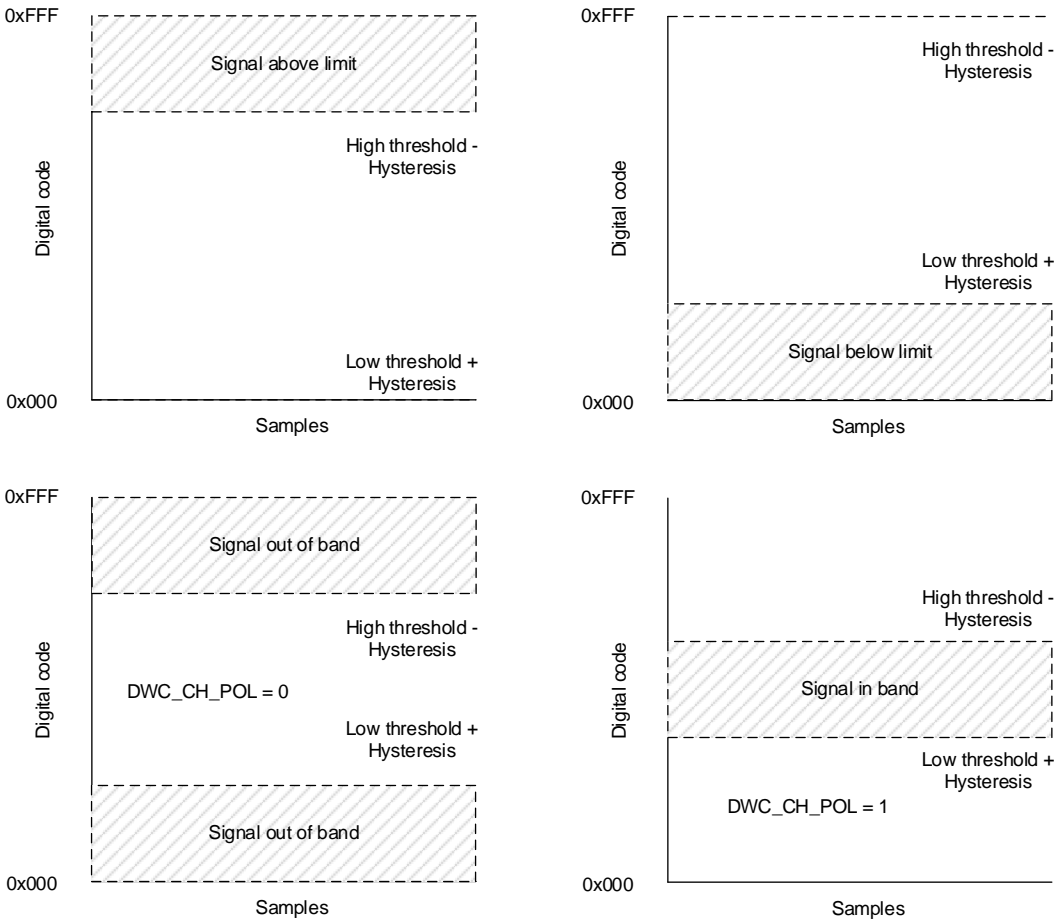
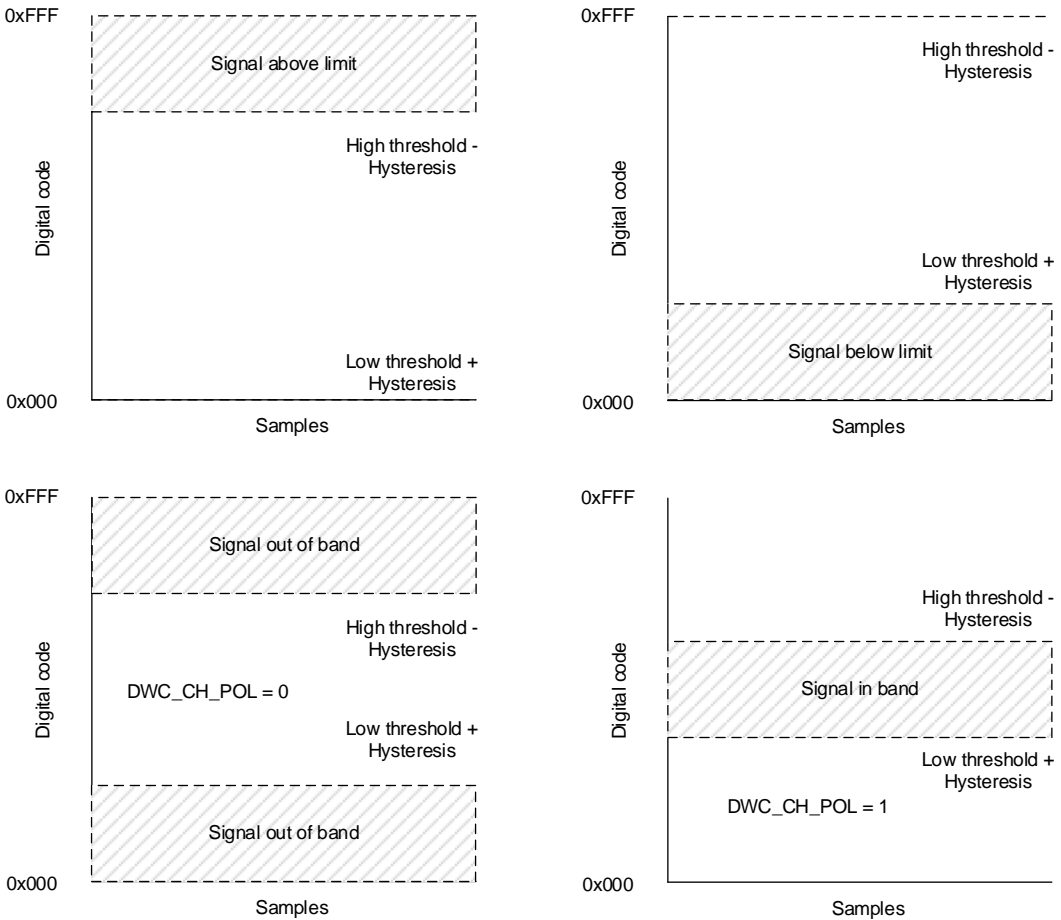


图 7. Digital Window Comparator Block Diagram

The low-side threshold, high-side threshold, event counter, and hysteresis parameters are independently programmable for each input channel.  shows the events that can be monitored for every analog input channel by the window comparator.



**图 8. Event Monitoring With the Window Comparator**

To enable the digital window comparator, set the `DWC_EN` bit in the `GENERAL_CFG` register. By default, hysteresis is 0, the high threshold is 0xFFF, and the low threshold is 0x000. A 12-bit straight binary code cannot be higher than 0xFFF or lower than 0x000, thus the thresholds have no effect unless set to different values.  shows the various types of event that can be detected by adjusting the thresholds. For detecting when a signal is in-band, the `EVENT_RGN` register must be configured. In each of the cases shown in , either or both `EVENT_HIGH_FLAG` and `EVENT_LOW_FLAG` can be set.

The programmable event counter counts consecutive thresholds violations before alert flags can be set. The event count can be set to a higher value to avoid transients in the input signal setting the alert flags.

In order to assert the `ALERT` pin when the alert flag is set for a particular analog input channel, set the corresponding bit in the `ALERT_CH_SEL` register. Alert flags are set regardless of the `ALERT_CH_SEL` configuration if `DWC_EN` is 1 and the high or low thresholds are exceeded.

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### 8.3.11.1 Interrupts From Digital Inputs

Logic 1 or logic 0 events can be detected on channels configured as digital inputs, as shown in 表 6, by enabling the corresponding ALERT\_CH\_SEL bit.

表 6. Configuring Interrupts From Digital Inputs

PIN_CFG[7:0]	GPIO_CFG[7:0]	ALERT_CH_SEL[7:0]	EVENT_RGN [7:0]	EVENT DESCRIPTION
1	0	1	0	EVENT_HIGH_FLAG is set when digital input channel is at logic 1.
1	0	1	1	EVENT_LOW_FLAG is set when digital input channel is at logic 0.

### 8.3.11.2 Changing Digital Outputs on Alert

图 9 shows how digital outputs can be updated in response to alerts from individual channels.

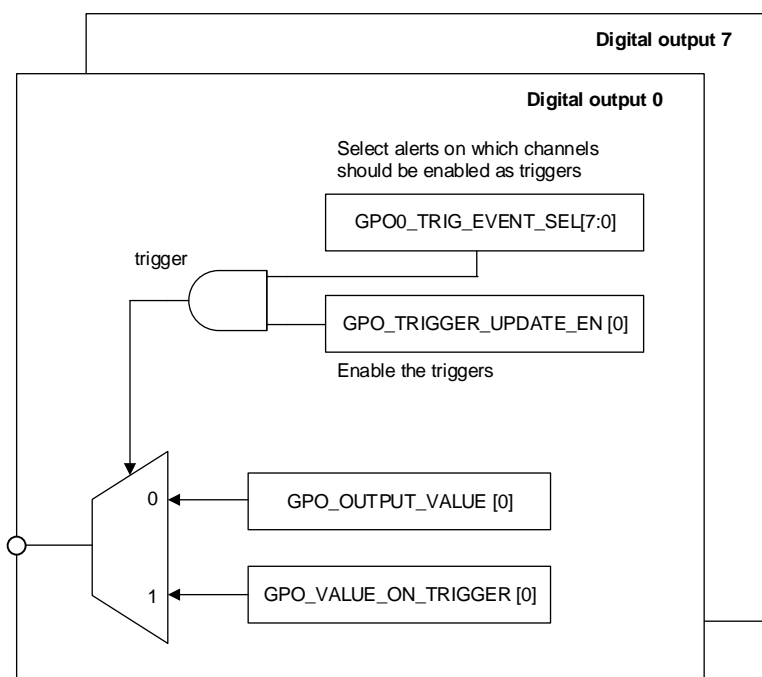


图 9. Block Diagram for the Digital Output Logic

#### 8.3.11.2.1 Changing Digital Outputs on Alerts

Any given digital output can be updated in response to an alert condition on one or more analog inputs and digital inputs. To update the digital output in response to alert conditions, the trigger must be configured and the value must be launched on the trigger.

### 8.3.11.2.1.1 Trigger

The following events can act as triggers for updating the value on the digital output:

- An alert occurs on one or more analog input channels. The digital window comparator must be enabled for these channels.
- An alert occurs on one or more digital input channels. The digital window comparator must be enabled for these channels.

Configure the GPOx\_TRIG\_EVENT\_SEL register to select which channels, analog inputs, or digital inputs can trigger an update on the digital output pin. After configuring the triggers for updating a digital output, the logic can be enabled by configuring the corresponding bit in the GPO\_TRIGGER\_UPDATE\_EN register.

### 8.3.11.2.1.2 Output Value

The digital outputs can be set to logic 1 or logic 0 in response to the triggers. The value to be updated on the digital output when a trigger event occurs can be configured in the GPO\_VALUE\_ON\_TRIGGER register.

## 8.3.12 Minimum, Maximum, and Latest Data Registers

The ADS7138 can record the minimum, maximum, and latest code (statistics registers) for every analog input channel. To enable or re-enable recording statistics, set the STATS\_EN bit in the GENERAL\_CFG register. Writing 1 to the STATS\_EN bit reinitializes the statistics module, after which results from new conversions are recorded in the statistics registers. Until a new conversion result is available, previous values can be read from the statistics registers. Before reading the statistics registers, set STATS\_EN to 0 to prevent any updates to this register block.

## 8.3.13 I<sup>2</sup>C Protocol Features

### 8.3.13.1 General Call

On receiving a general call (00h), the device provides an acknowledge (ACK).

### 8.3.13.2 General Call With Software Reset

On receiving a general call (00h) followed by a software reset (06h), the device resets itself.

### 8.3.13.3 General Call With a Software Write to the Programmable Part of the Slave Address

On receiving a general call (00h) followed by 04h, the device reevaluates its own I<sup>2</sup>C address configured by the ADDR pin. During this operation, the device does not respond to other I<sup>2</sup>C commands except the general-call command.

### 8.3.13.4 Configuring the Device for High-Speed I<sup>2</sup>C Mode

The device can be configured in high-speed I<sup>2</sup>C mode by providing an I<sup>2</sup>C frame with one of these codes: 0x09, 0x0B, 0x0D, or 0x0F.

After receiving one of these codes, the device sets the I2C\_HIGH\_SPEED bit in the SYSTEM\_STATUS register and remains in high-speed I<sup>2</sup>C mode until a STOP condition is received in an I<sup>2</sup>C frame.

## 8.4 Device Functional Modes

表 7 lists the functional modes supported by the ADS7138.

表 7. Functional Modes

FUNCTIONAL MODE	CONVERSION CONTROL	MUX CONTROL	CONV_MODE[1:0]	SEQ_MODE[1:0]
Manual	9th falling edge of SCL (ACK)	Register write to MANUAL_CHID	00b	00b
Auto-sequence	9th falling edge of SCL (ACK)	Channel sequencer	00b	01b
Autonomous	Internal to the device	Channel sequencer	01b	01b

The device powers up in manual mode (see the *Manual Mode* section) and can be configured into any mode listed in 表 7 by writing the configuration registers for the desired mode.

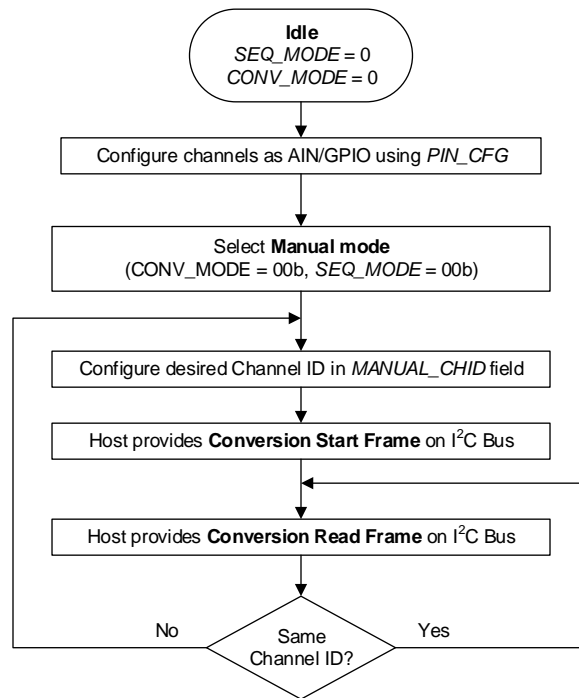
### 8.4.1 Device Power-Up and Reset

On power-up, the device calculates the address from the resistors connected on the ADDR pin and the BOR bit is set, thus indicating a power-cycle or reset event.

The device can be reset by an I<sup>2</sup>C general call (00h) followed by a software reset (06h), by setting the RST bit, or by recycling the power on the AVDD pin.

### 8.4.2 Manual Mode

Manual mode allows the external host processor to directly select the analog input channel. 图 10 lists the steps for operating the device in manual mode.



Manual mode with channel selection using register write

图 10. Device Operation in Manual Mode

Provide an I<sup>2</sup>C start or restart frame to initiate a conversion, as shown in the conversion start frame of 图 11, after configuring the device registers. ADC data can be read in subsequent I<sup>2</sup>C frames. The number of I<sup>2</sup>C frames required to read conversion data depends on the output data frame size; see the *Output Data Format* section for more details. A new conversion is initiated on the ninth falling edge of SCL (ACK bit) when the last byte of output data is read.

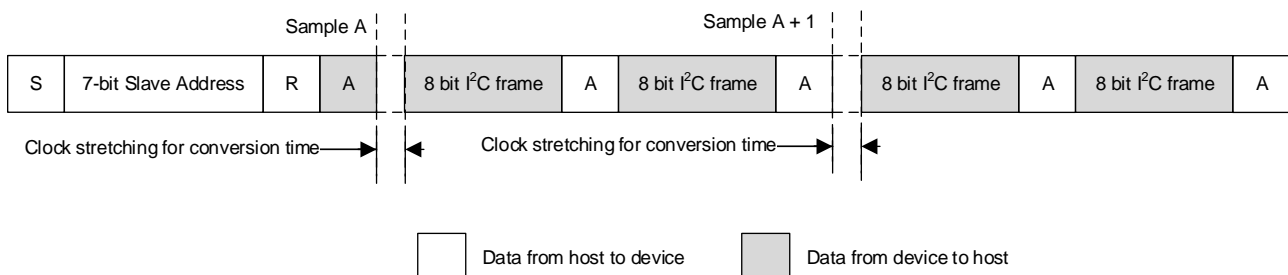


图 11. Starting a Conversion and Reading Data in Manual Mode

### 8.4.3 Auto-Sequence Mode

In auto-sequence mode, the internal channel sequencer switches the multiplexer to the next analog input channel after every conversion. The desired analog input channels can be configured for sequencing in the `AUTO_SEQ_CHSEL` register. To enable the channel sequencer, set `SEQ_START` to 1b. After every conversion, the channel sequencer switches the multiplexer to the next analog input in ascending order. To stop the channel sequencer from selecting channels, set `SEQ_START` to 0b. 图 12 lists the conversion start and read frames for auto-sequence mode.

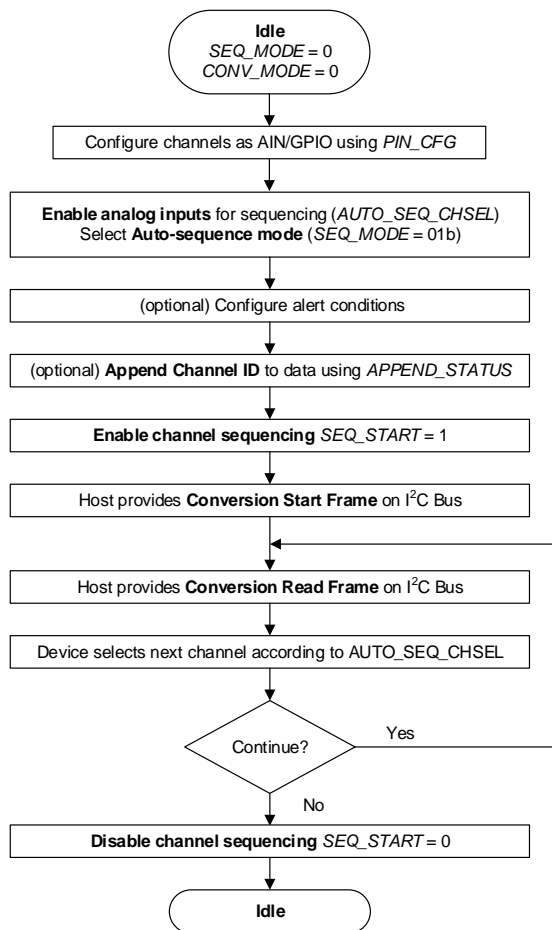
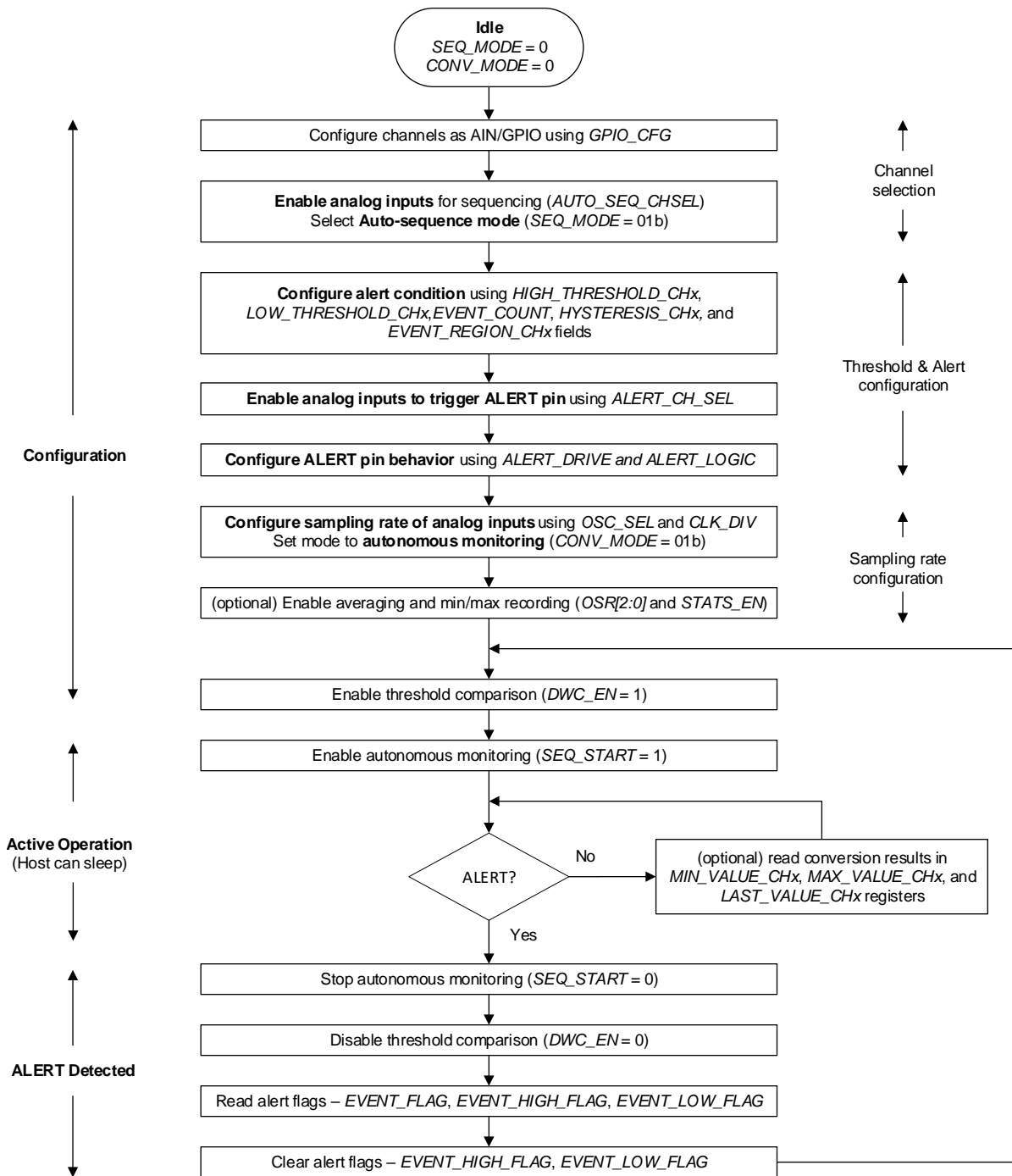


图 12. Device Operation in Auto-Sequence Mode

### 8.4.4 Autonomous Mode

In autonomous mode, the device can be programmed to monitor the voltage applied on the analog input pins of the device and generate a signal on the ALERT pin when the programmable high or low threshold values are crossed. In this mode, the device generates the start of conversion using the internal oscillator. The first start of conversion must be provided by the host and the device then generates the subsequent start of conversions.

图 13 shows the steps for configuring the operation mode to autonomous mode. Abort the ongoing sequence by setting `SEQ_START` to 0b before changing the functional mode or device configuration.



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图 13. Configuring the Device in Autonomous Mode

## 8.5 Programming

表 8 provides the acronyms for different conditions in an I<sup>2</sup>C frame. 表 9 lists the various command opcodes.

表 8. I<sup>2</sup>C Frame Acronyms

SYMBOL	DESCRIPTION
S	Start condition for the I <sup>2</sup> C frame
Sr	Restart condition for the I <sup>2</sup> C frame
P	Stop condition for the I <sup>2</sup> C frame
A	ACK (low)
N	NACK (high)
R	Read bit (high)
W	Write bit (low)

表 9. Opcodes for Commands

OPCODE	COMMAND DESCRIPTION
0001 0000b	Single register read
0000 1000b	Single register write
0001 1000b	Set bit
0010 0000b	Clear bit
0011 0000b	Reading a continuous block of registers
0010 1000b	Writing a continuous block of registers

### 8.5.1 Reading Registers

The I<sup>2</sup>C master can either read a single register or a continuous block registers from the device, as described in the [Single Register Read](#) and [Reading a Continuous Block of Registers](#) sections.

#### 8.5.1.1 Single Register Read

To read a single register from the device, the I<sup>2</sup>C master must provide an I<sup>2</sup>C command with three frames to set the register address for reading data. 表 9 lists the opcodes for different commands. After this command is provided, the I<sup>2</sup>C master must provide another I<sup>2</sup>C frame (as shown in 图 14) containing the device address and the read bit. After this frame, the device provides the register data. The device provides the same register data even if the host provides more clocks. To end the register read command, the master must provide a STOP or a RESTART condition in the I<sup>2</sup>C frame.

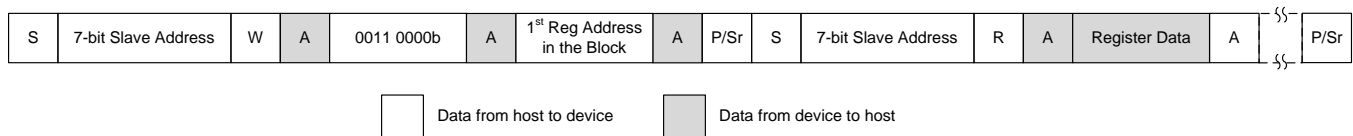


NOTE: S = start, Sr = repeated start, and P = stop.

图 14. Reading Register Data

### 8.5.1.2 Reading a Continuous Block of Registers

To read a continuous block of registers, the I<sup>2</sup>C master must provide an I<sup>2</sup>C command to set the register address. The register address is the address of the first register in the block that must be read. After this command is provided, the I<sup>2</sup>C master must provide another I<sup>2</sup>C frame, as shown in [图 15](#), containing the device address and the read bit. After this frame, the device provides the register data. The device provides data for the next register when more clocks are provided. When data are read from addresses that do not exist in the register map of the device, the device returns zeros. If the device does not have any further registers to provide data on, the device provide zeros. To end the register read command, the master must provide a STOP or a RESTART condition in the I<sup>2</sup>C frame.



NOTE: S = start, Sr = repeated start, and P = stop.

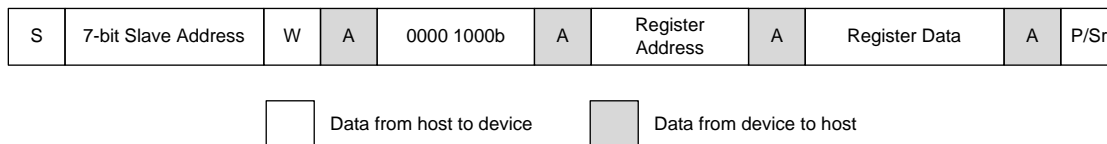
**图 15. Reading a Continuous Block of Registers**

## 8.5.2 Writing Registers

The I<sup>2</sup>C master can either write a single register or a continuous block of registers to the device, set a few bits in a register, or clear a few bits in a register.

### 8.5.2.1 Single Register Write

To write a single register from the device, as shown in [图 16](#), the I<sup>2</sup>C master must provide an I<sup>2</sup>C command with four frames. The register address is the address of the register that must be written and the register data is the value that must be written. [表 9](#) lists the opcodes for different commands. To end the register write command, the master must provide a STOP or a RESTART condition in the I<sup>2</sup>C frame.



NOTE: S = start, Sr = repeated start, and P = stop.

**图 16. Writing a Single Register**

### 8.5.2.2 Set Bit

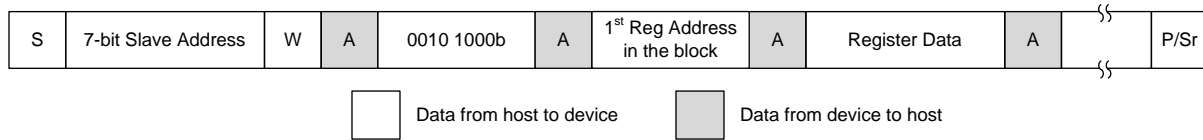
The I<sup>2</sup>C master must provide an I<sup>2</sup>C command with four frames, as shown in [图 16](#), to set bits in a register without changing the other bits. The register address is the address of the register that the bits must set and the register data is the value representing the bits that must be set. Bits with a value of 1 in the register data are set and bits with a value of 0 in the register data are not changed. [表 9](#) lists the opcodes for different commands. To end this command, the master must provide a STOP or RESTART condition in the I<sup>2</sup>C frame.

### 8.5.2.3 Clear Bit

The I<sup>2</sup>C master must provide an I<sup>2</sup>C command with four frames, as shown in [图 16](#), to clear bits in a register without changing the other bits. The register address is the address of the register that the bits must clear and the register data is the value representing the bits that must be cleared. Bits with a value of 1 in the register data are cleared and bits with a value of 0 in the register data are not changed. [表 9](#) lists the opcodes for different commands. To end this command, the master must provide a STOP or a RESTART condition in the I<sup>2</sup>C frame.

### 8.5.2.4 Writing a Continuous Block of Registers

The I<sup>2</sup>C master must provide an I<sup>2</sup>C command, as shown in 图 17, to write a continuous block of registers. The register address is the address of the first register in the block that must be written. The I<sup>2</sup>C master must provide data for registers in subsequent I<sup>2</sup>C frames in an ascending order of register addresses. Writing data to addresses that do not exist in the register map of the device have no effect. 表 9 lists the opcodes for different commands. If the data provided by the I<sup>2</sup>C master exceeds the address space of the device, the device ignores the data beyond the address space. To end the register write command, the master must provide a STOP or a RESTART condition in the I<sup>2</sup>C frame.



NOTE: S = start, Sr = repeated start, and P = stop.

图 17. Writing a Continuous Block of Registers

## 8.6 ADS7138 Registers

Table 10 lists the ADS7138 registers. All register offset addresses not listed in Table 10 should be considered as reserved locations and the register contents should not be modified.

**Table 10. ADS7138 Registers**

Address	Acronym	Register Name	Section
0x0	SYSTEM_STATUS	SYSTEM_STATUS Register (Address = 0x0) [reset = 0x81]	
0x1	GENERAL_CFG	GENERAL_CFG Register (Address = 0x1) [reset = 0x0]	
0x2	DATA_CFG	DATA_CFG Register (Address = 0x2) [reset = 0x0]	
0x3	OSR_CFG	OSR_CFG Register (Address = 0x3) [reset = 0x0]	
0x4	OPMODE_CFG	OPMODE_CFG Register (Address = 0x4) [reset = 0x0]	
0x5	PIN_CFG	PIN_CFG Register (Address = 0x5) [reset = 0x0]	
0x7	GPIO_CFG	GPIO_CFG Register (Address = 0x7) [reset = 0x0]	
0x9	GPO_DRIVE_CFG	GPO_DRIVE_CFG Register (Address = 0x9) [reset = 0x0]	
0xB	GPO_OUTPUT_VALUE	GPO_OUTPUT_VALUE Register (Address = 0xB) [reset = 0x0]	
0xD	GPI_VALUE	GPI_VALUE Register (Address = 0xD) [reset = 0x0]	
0xF	ZCD_BLANKING_CFG	ZCD_BLANKING_CFG Register (Address = 0xF) [reset = 0x0]	
0x10	SEQUENCE_CFG	SEQUENCE_CFG Register (Address = 0x10) [reset = 0x0]	
0x11	CHANNEL_SEL	CHANNEL_SEL Register (Address = 0x11) [reset = 0x0]	
0x12	AUTO_SEQ_CH_SEL	AUTO_SEQ_CH_SEL Register (Address = 0x12) [reset = 0x0]	
0x14	ALERT_CH_SEL	ALERT_CH_SEL Register (Address = 0x14) [reset = 0x0]	
0x16	ALERT_MAP	ALERT_MAP Register (Address = 0x16) [reset = 0x0]	
0x17	ALERT_PIN_CFG	ALERT_PIN_CFG Register (Address = 0x17) [reset = 0x0]	
0x18	EVENT_FLAG	EVENT_FLAG Register (Address = 0x18) [reset = 0x0]	
0x1A	EVENT_HIGH_FLAG	EVENT_HIGH_FLAG Register (Address = 0x1A) [reset = 0x0]	
0x1C	EVENT_LOW_FLAG	EVENT_LOW_FLAG Register (Address = 0x1C) [reset = 0x0]	
0x1E	EVENT_RGN	EVENT_RGN Register (Address = 0x1E) [reset = 0x0]	
0x20	HYSTERESIS_CH0	HYSTERESIS_CH0 Register (Address = 0x20) [reset = 0xF0]	
0x21	HIGH_TH_CH0	HIGH_TH_CH0 Register (Address = 0x21) [reset = 0xFF]	
0x22	EVENT_COUNT_CH0	EVENT_COUNT_CH0 Register (Address = 0x22) [reset = 0x0]	
0x23	LOW_TH_CH0	LOW_TH_CH0 Register (Address = 0x23) [reset = 0x0]	
0x24	HYSTERESIS_CH1	HYSTERESIS_CH1 Register (Address = 0x24) [reset = 0xF0]	
0x25	HIGH_TH_CH1	HIGH_TH_CH1 Register (Address = 0x25) [reset = 0xFF]	
0x26	EVENT_COUNT_CH1	EVENT_COUNT_CH1 Register (Address = 0x26) [reset = 0x0]	
0x27	LOW_TH_CH1	LOW_TH_CH1 Register (Address = 0x27) [reset = 0x0]	
0x28	HYSTERESIS_CH2	HYSTERESIS_CH2 Register (Address = 0x28) [reset = 0xF0]	
0x29	HIGH_TH_CH2	HIGH_TH_CH2 Register (Address = 0x29) [reset = 0xFF]	
0x2A	EVENT_COUNT_CH2	EVENT_COUNT_CH2 Register (Address = 0x2A) [reset = 0x0]	
0x2B	LOW_TH_CH2	LOW_TH_CH2 Register (Address = 0x2B) [reset = 0x0]	
0x2C	HYSTERESIS_CH3	HYSTERESIS_CH3 Register (Address = 0x2C) [reset = 0xF0]	
0x2D	HIGH_TH_CH3	HIGH_TH_CH3 Register (Address = 0x2D) [reset = 0xFF]	
0x2E	EVENT_COUNT_CH3	EVENT_COUNT_CH3 Register (Address = 0x2E) [reset = 0x0]	
0x2F	LOW_TH_CH3	LOW_TH_CH3 Register (Address = 0x2F) [reset = 0x0]	
0x30	HYSTERESIS_CH4	HYSTERESIS_CH4 Register (Address = 0x30) [reset = 0xF0]	
0x31	HIGH_TH_CH4	HIGH_TH_CH4 Register (Address = 0x31) [reset = 0xFF]	
0x32	EVENT_COUNT_CH4	EVENT_COUNT_CH4 Register (Address = 0x32) [reset = 0x0]	
0x33	LOW_TH_CH4	LOW_TH_CH4 Register (Address = 0x33) [reset = 0x0]	
0x34	HYSTERESIS_CH5	HYSTERESIS_CH5 Register (Address = 0x34) [reset = 0xF0]	
0x35	HIGH_TH_CH5	HIGH_TH_CH5 Register (Address = 0x35) [reset = 0xFF]	

**Table 10. ADS7138 Registers (continued)**

Address	Acronym	Register Name	Section
0x36	EVENT_COUNT_CH5	EVENT_COUNT_CH5 Register (Address = 0x36) [reset = 0x0]	
0x37	LOW_TH_CH5	LOW_TH_CH5 Register (Address = 0x37) [reset = 0x0]	
0x38	HYSTERESIS_CH6	HYSTERESIS_CH6 Register (Address = 0x38) [reset = 0xF0]	
0x39	HIGH_TH_CH6	HIGH_TH_CH6 Register (Address = 0x39) [reset = 0xFF]	
0x3A	EVENT_COUNT_CH6	EVENT_COUNT_CH6 Register (Address = 0x3A) [reset = 0x0]	
0x3B	LOW_TH_CH6	LOW_TH_CH6 Register (Address = 0x3B) [reset = 0x0]	
0x3C	HYSTERESIS_CH7	HYSTERESIS_CH7 Register (Address = 0x3C) [reset = 0xF0]	
0x3D	HIGH_TH_CH7	HIGH_TH_CH7 Register (Address = 0x3D) [reset = 0xFF]	
0x3E	EVENT_COUNT_CH7	EVENT_COUNT_CH7 Register (Address = 0x3E) [reset = 0x0]	
0x3F	LOW_TH_CH7	LOW_TH_CH7 Register (Address = 0x3F) [reset = 0x0]	
0x60	MAX_CH0_LSB	MAX_CH0_LSB Register (Address = 0x60) [reset = 0x0]	
0x61	MAX_CH0_MSB	MAX_CH0_MSB Register (Address = 0x61) [reset = 0x0]	
0x62	MAX_CH1_LSB	MAX_CH1_LSB Register (Address = 0x62) [reset = 0x0]	
0x63	MAX_CH1_MSB	MAX_CH1_MSB Register (Address = 0x63) [reset = 0x0]	
0x64	MAX_CH2_LSB	MAX_CH2_LSB Register (Address = 0x64) [reset = 0x0]	
0x65	MAX_CH2_MSB	MAX_CH2_MSB Register (Address = 0x65) [reset = 0x0]	
0x66	MAX_CH3_LSB	MAX_CH3_LSB Register (Address = 0x66) [reset = 0x0]	
0x67	MAX_CH3_MSB	MAX_CH3_MSB Register (Address = 0x67) [reset = 0x0]	
0x68	MAX_CH4_LSB	MAX_CH4_LSB Register (Address = 0x68) [reset = 0x0]	
0x69	MAX_CH4_MSB	MAX_CH4_MSB Register (Address = 0x69) [reset = 0x0]	
0x6A	MAX_CH5_LSB	MAX_CH5_LSB Register (Address = 0x6A) [reset = 0x0]	
0x6B	MAX_CH5_MSB	MAX_CH5_MSB Register (Address = 0x6B) [reset = 0x0]	
0x6C	MAX_CH6_LSB	MAX_CH6_LSB Register (Address = 0x6C) [reset = 0x0]	
0x6D	MAX_CH6_MSB	MAX_CH6_MSB Register (Address = 0x6D) [reset = 0x0]	
0x6E	MAX_CH7_LSB	MAX_CH7_LSB Register (Address = 0x6E) [reset = 0x0]	
0x6F	MAX_CH7_MSB	MAX_CH7_MSB Register (Address = 0x6F) [reset = 0x0]	
0x80	MIN_CH0_LSB	MIN_CH0_LSB Register (Address = 0x80) [reset = 0xFF]	
0x81	MIN_CH0_MSB	MIN_CH0_MSB Register (Address = 0x81) [reset = 0xFF]	
0x82	MIN_CH1_LSB	MIN_CH1_LSB Register (Address = 0x82) [reset = 0xFF]	
0x83	MIN_CH1_MSB	MIN_CH1_MSB Register (Address = 0x83) [reset = 0xFF]	
0x84	MIN_CH2_LSB	MIN_CH2_LSB Register (Address = 0x84) [reset = 0xFF]	
0x85	MIN_CH2_MSB	MIN_CH2_MSB Register (Address = 0x85) [reset = 0xFF]	
0x86	MIN_CH3_LSB	MIN_CH3_LSB Register (Address = 0x86) [reset = 0xFF]	
0x87	MIN_CH3_MSB	MIN_CH3_MSB Register (Address = 0x87) [reset = 0xFF]	
0x88	MIN_CH4_LSB	MIN_CH4_LSB Register (Address = 0x88) [reset = 0xFF]	
0x89	MIN_CH4_MSB	MIN_CH4_MSB Register (Address = 0x89) [reset = 0xFF]	
0x8A	MIN_CH5_LSB	MIN_CH5_LSB Register (Address = 0x8A) [reset = 0xFF]	
0x8B	MIN_CH5_MSB	MIN_CH5_MSB Register (Address = 0x8B) [reset = 0xFF]	
0x8C	MIN_CH6_LSB	MIN_CH6_LSB Register (Address = 0x8C) [reset = 0xFF]	
0x8D	MIN_CH6_MSB	MIN_CH6_MSB Register (Address = 0x8D) [reset = 0xFF]	
0x8E	MIN_CH7_LSB	MIN_CH7_LSB Register (Address = 0x8E) [reset = 0xFF]	
0x8F	MIN_CH7_MSB	MIN_CH7_MSB Register (Address = 0x8F) [reset = 0xFF]	
0xA0	RECENT_CH0_LSB	RECENT_CH0_LSB Register (Address = 0xA0) [reset = 0x0]	
0xA1	RECENT_CH0_MSB	RECENT_CH0_MSB Register (Address = 0xA1) [reset = 0x0]	
0xA2	RECENT_CH1_LSB	RECENT_CH1_LSB Register (Address = 0xA2) [reset = 0x0]	
0xA3	RECENT_CH1_MSB	RECENT_CH1_MSB Register (Address = 0xA3) [reset = 0x0]	
0xA4	RECENT_CH2_LSB	RECENT_CH2_LSB Register (Address = 0xA4) [reset = 0x0]	

**Table 10. ADS7138 Registers (continued)**

Address	Acronym	Register Name	Section
0xA5	RECENT_CH2_MSB	RECENT_CH2_MSB Register (Address = 0xA5) [reset = 0x0]	
0xA6	RECENT_CH3_LSB	RECENT_CH3_LSB Register (Address = 0xA6) [reset = 0x0]	
0xA7	RECENT_CH3_MSB	RECENT_CH3_MSB Register (Address = 0xA7) [reset = 0x0]	
0xA8	RECENT_CH4_LSB	RECENT_CH4_LSB Register (Address = 0xA8) [reset = 0x0]	
0xA9	RECENT_CH4_MSB	RECENT_CH4_MSB Register (Address = 0xA9) [reset = 0x0]	
0xAA	RECENT_CH5_LSB	RECENT_CH5_LSB Register (Address = 0xAA) [reset = 0x0]	
0xAB	RECENT_CH5_MSB	RECENT_CH5_MSB Register (Address = 0xAB) [reset = 0x0]	
0xAC	RECENT_CH6_LSB	RECENT_CH6_LSB Register (Address = 0xAC) [reset = 0x0]	
0xAD	RECENT_CH6_MSB	RECENT_CH6_MSB Register (Address = 0xAD) [reset = 0x0]	
0xAE	RECENT_CH7_LSB	RECENT_CH7_LSB Register (Address = 0xAE) [reset = 0x0]	
0xAF	RECENT_CH7_MSB	RECENT_CH7_MSB Register (Address = 0xAF) [reset = 0x0]	
0xC3	GPO0_TRIG_EVENT_SEL	GPO0_TRIG_EVENT_SEL Register (Address = 0xC3) [reset = 0x2]	
0xC5	GPO1_TRIG_EVENT_SEL	GPO1_TRIG_EVENT_SEL Register (Address = 0xC5) [reset = 0x2]	
0xC7	GPO2_TRIG_EVENT_SEL	GPO2_TRIG_EVENT_SEL Register (Address = 0xC7) [reset = 0x2]	
0xC9	GPO3_TRIG_EVENT_SEL	GPO3_TRIG_EVENT_SEL Register (Address = 0xC9) [reset = 0x2]	
0xCB	GPO4_TRIG_EVENT_SEL	GPO4_TRIG_EVENT_SEL Register (Address = 0xCB) [reset = 0x2]	
0xCD	GPO5_TRIG_EVENT_SEL	GPO5_TRIG_EVENT_SEL Register (Address = 0xCD) [reset = 0x2]	
0xCF	GPO6_TRIG_EVENT_SEL	GPO6_TRIG_EVENT_SEL Register (Address = 0xCF) [reset = 0x2]	
0xD1	GPO7_TRIG_EVENT_SEL	GPO7_TRIG_EVENT_SEL Register (Address = 0xD1) [reset = 0x2]	
0xE9	GPO_TRIGGER_CFG	GPO_TRIGGER_CFG Register (Address = 0xE9) [reset = 0x0]	
0xEB	GPO_VALUE_TRIG	GPO_VALUE_TRIG Register (Address = 0xEB) [reset = 0x0]	

Complex bit access types are encoded to fit into small table cells. [Table 11](#) shows the codes that are used for access types in this section.

**Table 11. ADS7138 Access Type Codes**

Access Type	Code	Description
<b>Read Type</b>		
R	R	Read
<b>Write Type</b>		
W	W	Write
<b>Reset or Default Value</b>		
-n		Value after reset or the default value
<b>Register Array Variables</b>		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

**8.6.1 SYSTEM\_STATUS Register (Address = 0x0) [reset = 0x81]**

SYSTEM\_STATUS is shown in [Figure 18](#) and described in [Table 12](#).

Return to the [Summary Table](#).

**Figure 18. SYSTEM\_STATUS Register**

7	6	5	4	3	2	1	0
RSVD	SEQ_STATUS	I <sup>2</sup> C_SPEED	RESERVED	OSR_DONE	CRC_ERR_FUSE	CRC_ERR_IN	BOR
R-1b	R-0b	R-0b	R-0b	R/W-0b	R-0b	R/W-0b	R/W-1b

**Table 12. SYSTEM\_STATUS Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	RSVD	R	1b	Reads return 1b.
6	SEQ_STATUS	R	0b	Status of the channel sequencer. 0b = Sequence stopped 1b = Sequence in progress
5	I <sup>2</sup> C_SPEED	R	0b	I <sup>2</sup> C high-speed status. 0b = I <sup>2</sup> C bus is not in high-speed mode. 1b = I <sup>2</sup> C bus is in high-speed mode.
4	RESERVED	R	0b	Reserved. Reads return 0.
3	OSR_DONE	R/W	0b	Averaging status. Clear this bit by writing 1b to this bit. 0b = Averaging in progress or not started; average result is not ready. 1b = Averaging complete; average result is ready.
2	CRC_ERR_FUSE	R	0b	Device power-up configuration CRC check status. To re-evaluate this bit, software reset the device or power cycle AVDD. 0b = No problems detected in power-up configuration. 1b = Device configuration not loaded correctly.
1	CRC_ERR_IN	R/W	0b	Status of CRC check on incoming data. Write 1b to clear this error flag. 0b = No CRC error. 1b = CRC error detected. All register writes, except to addresses 0x00 and 0x01, are blocked.
0	BOR	R/W	1b	Brown out reset indicator. This bit is set if brown out condition occurs or device is power cycled. Write 1b to this bit to clear the flag. 0b = No brown out from last time this bit was cleared. 1b = Brown out condition detected or device power cycled.

**8.6.2 GENERAL\_CFG Register (Address = 0x1) [reset = 0x0]**

GENERAL\_CFG is shown in [Figure 19](#) and described in [Table 13](#).

Return to the [Summary Table](#).

**Figure 19. GENERAL\_CFG Register**

7	6	5	4	3	2	1	0
RESERVED	CRC_EN	STATS_EN	DWC_EN	CNVST	CH_RST	CAL	RST
R-0b	R/W-0b	R/W-0b	R/W-0b	W-0b	R/W-0b	R/W-0b	W-0b

**Table 13. GENERAL\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved. Reads return 0.
6	CRC_EN	R/W	0b	Enable or disable the CRC on device interface. 0b = CRC module disabled. 1b = CRC appended to data output. CRC check is enabled on incoming data.
5	STATS_EN	R/W	0b	Enable or disable the statistics module to update minimum, maximum, and latest output code registers. 0b = Statistics registers are not updated. 1b = Clear statistics registers and continue updating with new conversion results.
4	DWC_EN	R/W	0b	Enable or disable the digital window comparator. 0b = Reset or disable the digital window comparator. 1b = Enable the digital window comparator.
3	CNVST	W	0b	Control start conversion on selected analog input. Readback of this bit returns 0b. 0b = Normal operation; conversions starts on the 9 <sup>th</sup> falling edge of I <sup>2</sup> C frame. Device stretches SCL until end of conversion or completion of averaging. 1b = Initiate start of conversion. Device does not stretch SCL until end of conversion or completion of averaging.
2	CH_RST	R/W	0b	Force all channels to be analog inputs. 0b = Normal operation. 1b = All channels are configured as analog inputs irrespective of configuration in other registers.
1	CAL	R/W	0b	Calibrate ADC offset. 0b = Normal operation. 1b = ADC offset is calibrated. After calibration is complete, this bit is set to 0b.
0	RST	W	0b	Software reset all registers to default values. 0b = Normal operation. 1b = Device is reset. After reset is complete, this bit is set to 0b and BOR bit is set to 1b.

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### 8.6.3 DATA\_CFG Register (Address = 0x2) [reset = 0x0]

DATA\_CFG is shown in [Figure 20](#) and described in [Table 14](#).

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**Figure 20. DATA\_CFG Register**

7	6	5	4	3	2	1	0
FIX_PAT	RESERVED	APPEND_STATUS[1:0]		RESERVED			
R/W-0b	R-0b	R/W-0b		R-0b			

**Table 14. DATA\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	FIX_PAT	R/W	0b	Device will output fixed data bits, which can be helpful for debugging communication with the device. 0b = Normal operation. 1b = Device outputs fixed code 0xA5A repeatedly when reading ADC data.
6	RESERVED	R	0b	Reserved. Reads return 0.

**Table 14. DATA\_CFG Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
5-4	APPEND_STATUS[1:0]	R/W	0b	Append 4-bit channel ID or status flags to output data. 0b = Channel ID and status flags are not appended to ADC data. 1b = 4-bit channel ID is appended to ADC data. 10b = 4-bit status flags are appended to ADC data. 11b = Reserved.
3-0	RESERVED	R	0b	

#### 8.6.4 OSR\_CFG Register (Address = 0x3) [reset = 0x0]

 OSR\_CFG is shown in [Figure 21](#) and described in [Table 15](#).

 Return to the [Summary Table](#).

**Figure 21. OSR\_CFG Register**

7	6	5	4	3	2	1	0
RESERVED					OSR[2:0]		
R-0b					R/W-0b		

**Table 15. OSR\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0b	Reserved. Reads return 0.
2-0	OSR[2:0]	R/W	0b	Selects the oversampling ratio for ADC conversion result. 0b = No averaging 1b = 2 samples 10b = 4 samples 11b = 8 samples 100b = 16 samples 101b = 32 samples 110b = 64 samples 111b = 128 samples

#### 8.6.5 OPMODE\_CFG Register (Address = 0x4) [reset = 0x0]

 OPMODE\_CFG is shown in [Figure 22](#) and described in [Table 16](#).

 Return to the [Summary Table](#).

**Figure 22. OPMODE\_CFG Register**

7	6	5	4	3	2	1	0
CONV_ON_ERR	CONV_MODE[1:0]		OSC_SEL	CLK_DIV[3:0]			
R/W-0b	R/W-0b		R/W-0b	R/W-0b			

**Table 16. OPMODE\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	CONV_ON_ERR	R/W	0b	Control continuation of autonomous modes if CRC error is detected on communication interface. 0b = If CRC error is detected, device continues channel sequencing and pin configuration is retained. See the CRC_ERR_IN bit for more details. 1b = If CRC error is detected, device changes all channels to analog inputs and channel sequencing will be paused until CRC_ERR_IN = 1b. After clearing CRC_ERR_IN flag, device resumes channel sequencing and pin configuration is restored.

**Table 16. OPMODE\_CFG Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
6-5	CONV_MODE[1:0]	R/W	0b	These bits set the mode of conversion of the ADC. 0b = Manual mode; conversions are initiated by host. 1b = Autonomous mode; conversions are initiated by internal state machine.
4	OSC_SEL	R/W	0b	Selects the oscillator for internal timing generation. 0b = High-speed oscillator. 1b = Low-power oscillator.
3-0	CLK_DIV[3:0]	R/W	0b	Sampling speed control in autonomous monitoring mode (CONV_MODE = 01b). See the section on oscillator and timing control for details.

**8.6.6 PIN\_CFG Register (Address = 0x5) [reset = 0x0]**

PIN\_CFG is shown in [Figure 23](#) and described in [Table 17](#).

Return to the [Summary Table](#).

**Figure 23. PIN\_CFG Register**

7	6	5	4	3	2	1	0
PIN_CFG[7:0]							
R/W-0b							

**Table 17. PIN\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	PIN_CFG[7:0]	R/W	0b	Configure device channels AIN/GPIO[7:0] as analog inputs or GPIOs. 0b = Channel is configured as analog input. 1b = Channel is configured as GPIO.

**8.6.7 GPIO\_CFG Register (Address = 0x7) [reset = 0x0]**

GPIO\_CFG is shown in [Figure 24](#) and described in [Table 18](#).

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**Figure 24. GPIO\_CFG Register**

7	6	5	4	3	2	1	0
GPIO_CFG[7:0]							
R/W-0b							

**Table 18. GPIO\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	GPIO_CFG[7:0]	R/W	0b	Configure GPIO[7:0] as either digital inputs or digital outputs. 0b = GPIO is configured as digital input. 1b = GPIO is configured as digital output.

**8.6.8 GPO\_DRIVE\_CFG Register (Address = 0x9) [reset = 0x0]**

GPO\_DRIVE\_CFG is shown in [Figure 25](#) and described in [Table 19](#).

Return to the [Summary Table](#).

**Figure 25. GPO\_DRIVE\_CFG Register**

7	6	5	4	3	2	1	0
GPO_DRIVE_CFG[7:0]							
R/W-0b							

**Table 19. GPO\_DRIVE\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	GPO_DRIVE_CFG[7:0]	R/W	0b	Configure digital outputs GPO[7:0] as either open-drain or push-pull outputs. 0b = Digital output is open-drain; connect external pullup resistor. 1b = Push-pull driver is used for digital output.

**8.6.9 GPO\_OUTPUT\_VALUE Register (Address = 0xB) [reset = 0x0]**

GPO\_OUTPUT\_VALUE is shown in [Figure 26](#) and described in [Table 20](#).

Return to the [Summary Table](#).

**Figure 26. GPO\_OUTPUT\_VALUE Register**

7	6	5	4	3	2	1	0
GPO_OUTPUT_VALUE[7:0]							
R/W-0b							

**Table 20. GPO\_OUTPUT\_VALUE Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	GPO_OUTPUT_VALUE[7:0]	R/W	0b	Logic level to be set on digital outputs GPO[7:0]. 0b = Digital output set to logic 0. 1b = Digital output set to logic 1.

**8.6.10 GPI\_VALUE Register (Address = 0xD) [reset = 0x0]**

GPI\_VALUE is shown in [Figure 27](#) and described in [Table 21](#).

Return to the [Summary Table](#).

**Figure 27. GPI\_VALUE Register**

7	6	5	4	3	2	1	0
GPI_VALUE[7:0]							
R-0b							

**Table 21. GPI\_VALUE Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	GPI_VALUE[7:0]	R	0b	Readback the logic level on GPIO[7:0]. 0b = GPIO is at logic 0. 1b = GPIO is at logic 1.

**8.6.11 ZCD\_BLANKING\_CFG Register (Address = 0xF) [reset = 0x0]**

ZCD\_BLANKING\_CFG is shown in [Figure 28](#) and described in [Table 22](#).

Return to the [Summary Table](#).

Figure 28. ZCD\_BLANKING\_CFG Register

7	6	5	4	3	2	1	0
MULT_EN		ZCD_BLANKING[6:0]					
R/W-0b		R/W-0b					

Table 22. ZCD\_BLANKING\_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MULT_EN	R/W	0b	Multiplier enable bit for the ZCD_BLANKING field. 0b = Blanking count = ZCD_BLANKING 1b = Blanking count = ZCD_BLANKING x 8
6-0	ZCD_BLANKING[6:0]	R/W	0b	This field defines the number of analog conversions, of the ZCD channel, which must be ignored for generating next ZCD event. The counting starts from ZCD event detection.

8.6.12 SEQUENCE\_CFG Register (Address = 0x10) [reset = 0x0]

SEQUENCE\_CFG is shown in Figure 29 and described in Table 23.

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Figure 29. SEQUENCE\_CFG Register

7	6	5	4	3	2	1	0
RESERVED			SEQ_START	RESERVED		SEQ_MODE[1:0]	
R-0b			R/W-0b	R-0b		R/W-0b	

Table 23. SEQUENCE\_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0b	Reserved. Reads return 0.
4	SEQ_START	R/W	0b	Control for start of channel sequence when using auto sequence mode (SEQ_MODE = 01b). 0b = Stop channel sequencing. 1b = Start channel sequencing in ascending order for channels enabled in AUTO_SEQ_CH_SEL register.
3-2	RESERVED	R	0b	Reserved. Reads return 0.
1-0	SEQ_MODE[1:0]	R/W	0b	Selects the mode of scanning of analog input channels. 0b = Manual sequence mode; channel selected by MANUAL_CHID field. 1b = Auto sequence mode; channel selected by internal channel sequencer. 10b = Reserved. 11b = Reserved.

8.6.13 CHANNEL\_SEL Register (Address = 0x11) [reset = 0x0]

CHANNEL\_SEL is shown in Figure 30 and described in Table 24.

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Figure 30. CHANNEL\_SEL Register

7	6	5	4	3	2	1	0
RESERVED				MANUAL_CHID[3:0]			
R-0b				R/W-0b			

**Table 24. CHANNEL\_SEL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0b	Reserved. Reads return 0.
3-0	MANUAL_CHID[3:0]	R/W	0b	In manual mode (SEQ_MODE = 00b), this field contains the 4-bit channel ID of the analog input channel for next ADC conversion. For valid ADC data, the selected channel must not be configured as GPIO in PIN_CFG register. 0b = AIN0 1b = AIN1 10b = AIN2 11b = AIN3 100b = AIN4 101b = AIN5 110b = AIN6 111b = AIN7 1000b = Reserved.

**8.6.14 AUTO\_SEQ\_CH\_SEL Register (Address = 0x12) [reset = 0x0]**

AUTO\_SEQ\_CH\_SEL is shown in [Figure 31](#) and described in [Table 25](#).

Return to the [Summary Table](#).

**Figure 31. AUTO\_SEQ\_CH\_SEL Register**

7	6	5	4	3	2	1	0
AUTO_SEQ_CH_SEL[7:0]							
R/W-0b							

**Table 25. AUTO\_SEQ\_CH\_SEL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	AUTO_SEQ_CH_SEL[7:0]	R/W	0b	Select analog input channels AIN[7:0] in for auto sequencing mode. 0b = Analog input channel is not enabled in scanning sequence. 1b = Analog input channel is enabled in scanning sequence.

**8.6.15 ALERT\_CH\_SEL Register (Address = 0x14) [reset = 0x0]**

ALERT\_CH\_SEL is shown in [Figure 32](#) and described in [Table 26](#).

Return to the [Summary Table](#).

**Figure 32. ALERT\_CH\_SEL Register**

7	6	5	4	3	2	1	0
ALERT_CH_SEL[7:0]							
R/W-0b							

**Table 26. ALERT\_CH\_SEL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	ALERT_CH_SEL[7:0]	R/W	0b	Select channels for which the alert flags can assert the ALERT pin. 0b = Alert flags for this channel do not assert the ALERT pin. 1b = Alert flags for this channel assert the ALERT pin.

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**8.6.16 ALERT\_MAP Register (Address = 0x16) [reset = 0x0]**

ALERT\_MAP is shown in [Figure 33](#) and described in [Table 27](#).

Return to the [Summary Table](#).

**Figure 33. ALERT\_MAP Register**

7	6	5	4	3	2	1	0
RESERVED							ALERT_CRCIN
R-0b							R/W-0b

**Table 27. ALERT\_MAP Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0b	Reserved. Reads return 0.
0	ALERT_CRCIN	R/W	0b	Enable or disable the alert notification for CRC error on input data (CRCERR_IN = 1b). 0b = ALERT pin is not asserted when CRCERR_IN = 1b. 1b = ALERT pin is asserted when CRCERR_IN = 1b. Clear CRCERR_IN for deasserting the ALERT pin.

**8.6.17 ALERT\_PIN\_CFG Register (Address = 0x17) [reset = 0x0]**

ALERT\_PIN\_CFG is shown in [Figure 34](#) and described in [Table 28](#).

Return to the [Summary Table](#).

**Figure 34. ALERT\_PIN\_CFG Register**

7	6	5	4	3	2	1	0
RESERVED					ALERT_DRIVE	ALERT_LOGIC[1:0]	
R-0b					R/W-0b	R/W-0b	

**Table 28. ALERT\_PIN\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0b	Reserved. Reads return 0.
2	ALERT_DRIVE	R/W	0b	Configure output drive of the ALERT pin. 0b = Open-drain output. Connect external pullup resistor. 1b = Push-pull output.
1-0	ALERT_LOGIC[1:0]	R/W	0b	Configure how ALERT pin is asserted. 0b = Pulsed high (one logic high pulse one time per alert flag). 1b = Active high.

**8.6.18 EVENT\_FLAG Register (Address = 0x18) [reset = 0x0]**

EVENT\_FLAG is shown in [Figure 35](#) and described in [Table 29](#).

Return to the [Summary Table](#).

**Figure 35. EVENT\_FLAG Register**

7	6	5	4	3	2	1	0
EVENT_FLAG[7:0]							
R-0b							

**Table 29. EVENT\_FLAG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	EVENT_FLAG[7:0]	R	0b	Alert flags indicating digital window comparator status for CH[7:0]. Write 0b to individual bits of high/low register to clear alert flag. 0b = Event condition not detected. 1b = Event condition detected.

**8.6.19 EVENT\_HIGH\_FLAG Register (Address = 0x1A) [reset = 0x0]**

 EVENT\_HIGH\_FLAG is shown in [Figure 36](#) and described in [Table 30](#).

 Return to the [Summary Table](#).

**Figure 36. EVENT\_HIGH\_FLAG Register**

7	6	5	4	3	2	1	0
EVENT_HIGH_FLAG[7:0]							
R/W-0b							

**Table 30. EVENT\_HIGH\_FLAG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	EVENT_HIGH_FLAG[7:0]	R/W	0b	Alert flag corresponding to high threshold of analog input or logic 1 on digital input on CH[7:0]. Write 1b to clear this flag. 0b = No alert condition detected. 1b = Either high threshold was exceeded (analog input) or logic 1 was detected (digital input).

**8.6.20 EVENT\_LOW\_FLAG Register (Address = 0x1C) [reset = 0x0]**

 EVENT\_LOW\_FLAG is shown in [Figure 37](#) and described in [Table 31](#).

 Return to the [Summary Table](#).

**Figure 37. EVENT\_LOW\_FLAG Register**

7	6	5	4	3	2	1	0
EVENT_LOW_FLAG[7:0]							
R/W-0b							

**Table 31. EVENT\_LOW\_FLAG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	EVENT_LOW_FLAG[7:0]	R/W	0b	Alert flag corresponding to low threshold of analog input or logic 0 on digital input on CH[7:0]. Write 1b to clear this flag. 0b = No Event condition detected. 1b = Either low threshold was exceeded (analog input) or logic 0 was detected (digital input).

**8.6.21 EVENT\_RGN Register (Address = 0x1E) [reset = 0x0]**

 EVENT\_RGN is shown in [Figure 38](#) and described in [Table 32](#).

 Return to the [Summary Table](#).

**Figure 38. EVENT\_RGN Register**

7	6	5	4	3	2	1	0
EVENT_RGN[7:0]							
R/W-0b							

**Table 32. EVENT\_RGN Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	EVENT_RGN[7:0]	R/W	0b	Choice of region used in monitoring analog and digital inputs CH[7:0]. 0b = Alert flag is set if: (conversion result < low threshold) or (conversion result > high threshold). For digital inputs, logic 1 sets the alert flag. 1b = Alert flag is set if: (low threshold > conversion result < high threshold). For digital inputs, logic 0 sets the alert flag.

**8.6.22 HYSTERESIS\_CH0 Register (Address = 0x20) [reset = 0xF0]**

HYSTERESIS\_CH0 is shown in [Figure 39](#) and described in [Table 33](#).

Return to the [Summary Table](#).

**Figure 39. HYSTERESIS\_CH0 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH0_LSB[3:0]				HYSTERESIS_CH0[3:0]			
R/W-1111b				R/W-0b			

**Table 33. HYSTERESIS\_CH0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH0_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH0[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteresis is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

**8.6.23 HIGH\_TH\_CH0 Register (Address = 0x21) [reset = 0xFF]**

HIGH\_TH\_CH0 is shown in [Figure 40](#) and described in [Table 34](#).

Return to the [Summary Table](#).

**Figure 40. HIGH\_TH\_CH0 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH0_MSB[7:0]							
R/W-11111111b							

**Table 34. HIGH\_TH\_CH0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH0_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

**8.6.24 EVENT\_COUNT\_CH0 Register (Address = 0x22) [reset = 0x0]**

EVENT\_COUNT\_CH0 is shown in [Figure 41](#) and described in [Table 35](#).

Return to the [Summary Table](#).

**Figure 41. EVENT\_COUNT\_CH0 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH0_LSB[3:0]				EVENT_COUNT_CH0[3:0]			
R/W-0b				R/W-0b			

**Table 35. EVENT\_COUNT\_CH0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH0_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH0[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting event flag.

**8.6.25 LOW\_TH\_CH0 Register (Address = 0x23) [reset = 0x0]**

 LOW\_TH\_CH0 is shown in [Figure 42](#) and described in [Table 36](#).

 Return to the [Summary Table](#).

**Figure 42. LOW\_TH\_CH0 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH0_MSB[7:0]							
R/W-0b							

**Table 36. LOW\_TH\_CH0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH0_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

**8.6.26 HYSTERESIS\_CH1 Register (Address = 0x24) [reset = 0xF0]**

 HYSTERESIS\_CH1 is shown in [Figure 43](#) and described in [Table 37](#).

 Return to the [Summary Table](#).

**Figure 43. HYSTERESIS\_CH1 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH1_LSB[3:0]				HYSTERESIS_CH1[3:0]			
R/W-1111b				R/W-0b			

**Table 37. HYSTERESIS\_CH1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH1_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH1[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteresis is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

**8.6.27 HIGH\_TH\_CH1 Register (Address = 0x25) [reset = 0xFF]**

 HIGH\_TH\_CH1 is shown in [Figure 44](#) and described in [Table 38](#).

 Return to the [Summary Table](#).

**Figure 44. HIGH\_TH\_CH1 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH1_MSB[7:0]							
R/W-11111111b							

**Table 38. HIGH\_TH\_CH1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH1_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

**8.6.28 EVENT\_COUNT\_CH1 Register (Address = 0x26) [reset = 0x0]**

EVENT\_COUNT\_CH1 is shown in [Figure 45](#) and described in [Table 39](#).

Return to the [Summary Table](#).

**Figure 45. EVENT\_COUNT\_CH1 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH1_LSB[3:0]				EVENT_COUNT_CH1[3:0]			
R/W-0b				R/W-0b			

**Table 39. EVENT\_COUNT\_CH1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH1_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH1[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting event flag.

**8.6.29 LOW\_TH\_CH1 Register (Address = 0x27) [reset = 0x0]**

LOW\_TH\_CH1 is shown in [Figure 46](#) and described in [Table 40](#).

Return to the [Summary Table](#).

**Figure 46. LOW\_TH\_CH1 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH1_MSB[7:0]							
R/W-0b							

**Table 40. LOW\_TH\_CH1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH1_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

**8.6.30 HYSTERESIS\_CH2 Register (Address = 0x28) [reset = 0xF0]**

HYSTERESIS\_CH2 is shown in [Figure 47](#) and described in [Table 41](#).

Return to the [Summary Table](#).

**Figure 47. HYSTERESIS\_CH2 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH2_LSB[3:0]				HYSTERESIS_CH2[3:0]			
R/W-1111b				R/W-0b			

**Table 41. HYSTERESIS\_CH2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH2_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.

**Table 41. HYSTERESIS\_CH2 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
3-0	HYSTERESIS_CH2[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteresis is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

**8.6.31 HIGH\_TH\_CH2 Register (Address = 0x29) [reset = 0xFF]**

HIGH\_TH\_CH2 is shown in [Figure 48](#) and described in [Table 42](#).

Return to the [Summary Table](#).

**Figure 48. HIGH\_TH\_CH2 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH2_MSB[7:0]							
R/W-11111111b							

**Table 42. HIGH\_TH\_CH2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH2_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

**8.6.32 EVENT\_COUNT\_CH2 Register (Address = 0x2A) [reset = 0x0]**

EVENT\_COUNT\_CH2 is shown in [Figure 49](#) and described in [Table 43](#).

Return to the [Summary Table](#).

**Figure 49. EVENT\_COUNT\_CH2 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH2_LSB[3:0]				EVENT_COUNT_CH2[3:0]			
R/W-0b				R/W-0b			

**Table 43. EVENT\_COUNT\_CH2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH2_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH2[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting event flag.

**8.6.33 LOW\_TH\_CH2 Register (Address = 0x2B) [reset = 0x0]**

LOW\_TH\_CH2 is shown in [Figure 50](#) and described in [Table 44](#).

Return to the [Summary Table](#).

**Figure 50. LOW\_TH\_CH2 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH2_MSB[7:0]							
R/W-0b							

**Table 44. LOW\_TH\_CH2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH2_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

### 8.6.34 HYSTERESIS\_CH3 Register (Address = 0x2C) [reset = 0xF0]

HYSTERESIS\_CH3 is shown in [Figure 51](#) and described in [Table 45](#).

Return to the [Summary Table](#).

**Figure 51. HYSTERESIS\_CH3 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH3_LSB[3:0]				HYSTERESIS_CH3[3:0]			
R/W-1111b				R/W-0b			

**Table 45. HYSTERESIS\_CH3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH3_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH3[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteresis is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

### 8.6.35 HIGH\_TH\_CH3 Register (Address = 0x2D) [reset = 0xFF]

HIGH\_TH\_CH3 is shown in [Figure 52](#) and described in [Table 46](#).

Return to the [Summary Table](#).

**Figure 52. HIGH\_TH\_CH3 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH3_MSB[7:0]							
R/W-11111111b							

**Table 46. HIGH\_TH\_CH3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH3_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

### 8.6.36 EVENT\_COUNT\_CH3 Register (Address = 0x2E) [reset = 0x0]

EVENT\_COUNT\_CH3 is shown in [Figure 53](#) and described in [Table 47](#).

Return to the [Summary Table](#).

**Figure 53. EVENT\_COUNT\_CH3 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH3_LSB[3:0]				EVENT_COUNT_CH3[3:0]			
R/W-0b				R/W-0b			

**Table 47. EVENT\_COUNT\_CH3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH3_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH3[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting event flag.

### 8.6.37 LOW\_TH\_CH3 Register (Address = 0x2F) [reset = 0x0]

LOW\_TH\_CH3 is shown in [Figure 54](#) and described in [Table 48](#).

Return to the [Summary Table](#).

**Figure 54. LOW\_TH\_CH3 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH3_MSB[7:0]							
R/W-0b							

**Table 48. LOW\_TH\_CH3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH3_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

**8.6.38 HYSTERESIS\_CH4 Register (Address = 0x30) [reset = 0xF0]**

HYSTERESIS\_CH4 is shown in [Figure 55](#) and described in [Table 49](#).

Return to the [Summary Table](#).

**Figure 55. HYSTERESIS\_CH4 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH4_LSB[3:0]				HYSTERESIS_CH4[3:0]			
R/W-1111b				R/W-0b			

**Table 49. HYSTERESIS\_CH4 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH4_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH4[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteresis is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

**8.6.39 HIGH\_TH\_CH4 Register (Address = 0x31) [reset = 0xFF]**

HIGH\_TH\_CH4 is shown in [Figure 56](#) and described in [Table 50](#).

Return to the [Summary Table](#).

**Figure 56. HIGH\_TH\_CH4 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH4_MSB[7:0]							
R/W-11111111b							

**Table 50. HIGH\_TH\_CH4 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH4_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

**8.6.40 EVENT\_COUNT\_CH4 Register (Address = 0x32) [reset = 0x0]**

EVENT\_COUNT\_CH4 is shown in [Figure 57](#) and described in [Table 51](#).

Return to the [Summary Table](#).

**Figure 57. EVENT\_COUNT\_CH4 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH4_LSB[3:0]				EVENT_COUNT_CH4[3:0]			
R/W-0b				R/W-0b			

**Table 51. EVENT\_COUNT\_CH4 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH4_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH4[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting event flag.

**8.6.41 LOW\_TH\_CH4 Register (Address = 0x33) [reset = 0x0]**

LOW\_TH\_CH4 is shown in [Figure 58](#) and described in [Table 52](#).

Return to the [Summary Table](#).

**Figure 58. LOW\_TH\_CH4 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH4_MSB[7:0]							
R/W-0b							

**Table 52. LOW\_TH\_CH4 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH4_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

**8.6.42 HYSTERESIS\_CH5 Register (Address = 0x34) [reset = 0xF0]**

HYSTERESIS\_CH5 is shown in [Figure 59](#) and described in [Table 53](#).

Return to the [Summary Table](#).

**Figure 59. HYSTERESIS\_CH5 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH5_LSB[3:0]				HYSTERESIS_CH5[3:0]			
R/W-1111b				R/W-0b			

**Table 53. HYSTERESIS\_CH5 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH5_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH5[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteresis is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

**8.6.43 HIGH\_TH\_CH5 Register (Address = 0x35) [reset = 0xFF]**

HIGH\_TH\_CH5 is shown in [Figure 60](#) and described in [Table 54](#).

Return to the [Summary Table](#).

**Figure 60. HIGH\_TH\_CH5 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH5_MSB[7:0]							
R/W-11111111b							

**Table 54. HIGH\_TH\_CH5 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH5_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

**8.6.44 EVENT\_COUNT\_CH5 Register (Address = 0x36) [reset = 0x0]**

 EVENT\_COUNT\_CH5 is shown in [Figure 61](#) and described in [Table 55](#).

 Return to the [Summary Table](#).

**Figure 61. EVENT\_COUNT\_CH5 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH5_LSB[3:0]				EVENT_COUNT_CH5[3:0]			
R/W-0b				R/W-0b			

**Table 55. EVENT\_COUNT\_CH5 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH5_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH5[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting event flag.

**8.6.45 LOW\_TH\_CH5 Register (Address = 0x37) [reset = 0x0]**

 LOW\_TH\_CH5 is shown in [Figure 62](#) and described in [Table 56](#).

 Return to the [Summary Table](#).

**Figure 62. LOW\_TH\_CH5 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH5_MSB[7:0]							
R/W-0b							

**Table 56. LOW\_TH\_CH5 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH5_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

**8.6.46 HYSTERESIS\_CH6 Register (Address = 0x38) [reset = 0xF0]**

 HYSTERESIS\_CH6 is shown in [Figure 63](#) and described in [Table 57](#).

 Return to the [Summary Table](#).

**Figure 63. HYSTERESIS\_CH6 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH6_LSB[3:0]				HYSTERESIS_CH6[3:0]			
R/W-1111b				R/W-0b			

**Table 57. HYSTERESIS\_CH6 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH6_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.

**Table 57. HYSTERESIS\_CH6 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
3-0	HYSTERESIS_CH6[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteresis is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

**8.6.47 HIGH\_TH\_CH6 Register (Address = 0x39) [reset = 0xFF]**

HIGH\_TH\_CH6 is shown in [Figure 64](#) and described in [Table 58](#).

Return to the [Summary Table](#).

**Figure 64. HIGH\_TH\_CH6 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH6_MSB[7:0]							
R/W-11111111b							

**Table 58. HIGH\_TH\_CH6 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH6_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

**8.6.48 EVENT\_COUNT\_CH6 Register (Address = 0x3A) [reset = 0x0]**

EVENT\_COUNT\_CH6 is shown in [Figure 65](#) and described in [Table 59](#).

Return to the [Summary Table](#).

**Figure 65. EVENT\_COUNT\_CH6 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH6_LSB[3:0]				EVENT_COUNT_CH6[3:0]			
R/W-0b				R/W-0b			

**Table 59. EVENT\_COUNT\_CH6 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH6_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH6[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting event flag.

**8.6.49 LOW\_TH\_CH6 Register (Address = 0x3B) [reset = 0x0]**

LOW\_TH\_CH6 is shown in [Figure 66](#) and described in [Table 60](#).

Return to the [Summary Table](#).

**Figure 66. LOW\_TH\_CH6 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH6_MSB[7:0]							
R/W-0b							

**Table 60. LOW\_TH\_CH6 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH6_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

**8.6.50 HYSTERESIS\_CH7 Register (Address = 0x3C) [reset = 0xF0]**

 HYSTERESIS\_CH7 is shown in [Figure 67](#) and described in [Table 61](#).

 Return to the [Summary Table](#).

**Figure 67. HYSTERESIS\_CH7 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH7_LSB[3:0]				HYSTERESIS_CH7[3:0]			
R/W-1111b				R/W-0b			

**Table 61. HYSTERESIS\_CH7 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH7_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH7[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteresis is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

**8.6.51 HIGH\_TH\_CH7 Register (Address = 0x3D) [reset = 0xFF]**

 HIGH\_TH\_CH7 is shown in [Figure 68](#) and described in [Table 62](#).

 Return to the [Summary Table](#).

**Figure 68. HIGH\_TH\_CH7 Register**

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH7_MSB[7:0]							
R/W-11111111b							

**Table 62. HIGH\_TH\_CH7 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH7_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

**8.6.52 EVENT\_COUNT\_CH7 Register (Address = 0x3E) [reset = 0x0]**

 EVENT\_COUNT\_CH7 is shown in [Figure 69](#) and described in [Table 63](#).

 Return to the [Summary Table](#).

**Figure 69. EVENT\_COUNT\_CH7 Register**

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH7_LSB[3:0]				EVENT_COUNT_CH7[3:0]			
R/W-0b				R/W-0b			

**Table 63. EVENT\_COUNT\_CH7 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH7_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH7[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting event flag.

**8.6.53 LOW\_TH\_CH7 Register (Address = 0x3F) [reset = 0x0]**

 LOW\_TH\_CH7 is shown in [Figure 70](#) and described in [Table 64](#).

 Return to the [Summary Table](#).

Figure 70. LOW\_TH\_CH7 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH7_MSB[7:0]							
R/W-0b							

Table 64. LOW\_TH\_CH7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH7_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.54 MAX\_CH0\_LSB Register (Address = 0x60) [reset = 0x0]

MAX\_CH0\_LSB is shown in Figure 71 and described in Table 65.

Return to the Summary Table.

Figure 71. MAX\_CH0\_LSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH0_LSB[7:0]							
R-0b							

Table 65. MAX\_CH0\_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH0_LSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

8.6.55 MAX\_CH0\_MSB Register (Address = 0x61) [reset = 0x0]

MAX\_CH0\_MSB is shown in Figure 72 and described in Table 66.

Return to the Summary Table.

Figure 72. MAX\_CH0\_MSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH0_MSB[7:0]							
R-0b							

Table 66. MAX\_CH0\_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH0_MSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

8.6.56 MAX\_CH1\_LSB Register (Address = 0x62) [reset = 0x0]

MAX\_CH1\_LSB is shown in Figure 73 and described in Table 67.

Return to the Summary Table.

Figure 73. MAX\_CH1\_LSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH1_LSB[7:0]							
R-0b							

**Table 67. MAX\_CH1\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH1_LSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

**8.6.57 MAX\_CH1\_MSB Register (Address = 0x63) [reset = 0x0]**

MAX\_CH1\_MSB is shown in [Figure 74](#) and described in [Table 68](#).

Return to the [Summary Table](#).

**Figure 74. MAX\_CH1\_MSB Register**

7	6	5	4	3	2	1	0
MAX_VALUE_CH1_MSB[7:0]							
R-0b							

**Table 68. MAX\_CH1\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH1_MSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

**8.6.58 MAX\_CH2\_LSB Register (Address = 0x64) [reset = 0x0]**

MAX\_CH2\_LSB is shown in [Figure 75](#) and described in [Table 69](#).

Return to the [Summary Table](#).

**Figure 75. MAX\_CH2\_LSB Register**

7	6	5	4	3	2	1	0
MAX_VALUE_CH2_LSB[7:0]							
R-0b							

**Table 69. MAX\_CH2\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH2_LSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

**8.6.59 MAX\_CH2\_MSB Register (Address = 0x65) [reset = 0x0]**

MAX\_CH2\_MSB is shown in [Figure 76](#) and described in [Table 70](#).

Return to the [Summary Table](#).

**Figure 76. MAX\_CH2\_MSB Register**

7	6	5	4	3	2	1	0
MAX_VALUE_CH2_MSB[7:0]							
R-0b							

**Table 70. MAX\_CH2\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH2_MSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

**8.6.60 MAX\_CH3\_LSB Register (Address = 0x66) [reset = 0x0]**

MAX\_CH3\_LSB is shown in [Figure 77](#) and described in [Table 71](#).

Return to the [Summary Table](#).

**Figure 77. MAX\_CH3\_LSB Register**

7	6	5	4	3	2	1	0
MAX_VALUE_CH3_LSB[7:0]							
R-0b							

**Table 71. MAX\_CH3\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH3_LSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

**8.6.61 MAX\_CH3\_MSB Register (Address = 0x67) [reset = 0x0]**

MAX\_CH3\_MSB is shown in [Figure 78](#) and described in [Table 72](#).

Return to the [Summary Table](#).

**Figure 78. MAX\_CH3\_MSB Register**

7	6	5	4	3	2	1	0
MAX_VALUE_CH3_MSB[7:0]							
R-0b							

**Table 72. MAX\_CH3\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH3_MSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

**8.6.62 MAX\_CH4\_LSB Register (Address = 0x68) [reset = 0x0]**

MAX\_CH4\_LSB is shown in [Figure 79](#) and described in [Table 73](#).

Return to the [Summary Table](#).

**Figure 79. MAX\_CH4\_LSB Register**

7	6	5	4	3	2	1	0
MAX_VALUE_CH4_LSB[7:0]							
R-0b							

**Table 73. MAX\_CH4\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH4_LSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

**8.6.63 MAX\_CH4\_MSB Register (Address = 0x69) [reset = 0x0]**

MAX\_CH4\_MSB is shown in [Figure 80](#) and described in [Table 74](#).

Return to the [Summary Table](#).

**Figure 80. MAX\_CH4\_MSB Register**

7	6	5	4	3	2	1	0
MAX_VALUE_CH4_MSB[7:0]							
R-0b							

**Table 74. MAX\_CH4\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH4_MSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

**8.6.64 MAX\_CH5\_LSB Register (Address = 0x6A) [reset = 0x0]**

MAX\_CH5\_LSB is shown in [Figure 81](#) and described in [Table 75](#).

Return to the [Summary Table](#).

**Figure 81. MAX\_CH5\_LSB Register**

7	6	5	4	3	2	1	0
MAX_VALUE_CH5_LSB[7:0]							
R-0b							

**Table 75. MAX\_CH5\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH5_LSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

**8.6.65 MAX\_CH5\_MSB Register (Address = 0x6B) [reset = 0x0]**

MAX\_CH5\_MSB is shown in [Figure 82](#) and described in [Table 76](#).

Return to the [Summary Table](#).

**Figure 82. MAX\_CH5\_MSB Register**

7	6	5	4	3	2	1	0
MAX_VALUE_CH5_MSB[7:0]							
R-0b							

**Table 76. MAX\_CH5\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH5_MSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

**8.6.66 MAX\_CH6\_LSB Register (Address = 0x6C) [reset = 0x0]**

MAX\_CH6\_LSB is shown in [Figure 83](#) and described in [Table 77](#).

Return to the [Summary Table](#).

**Figure 83. MAX\_CH6\_LSB Register**

7	6	5	4	3	2	1	0
MAX_VALUE_CH6_LSB[7:0]							
R-0b							

**Table 77. MAX\_CH6\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH6_LSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

**8.6.67 MAX\_CH6\_MSB Register (Address = 0x6D) [reset = 0x0]**

MAX\_CH6\_MSB is shown in [Figure 84](#) and described in [Table 78](#).

Return to the [Summary Table](#).

**Figure 84. MAX\_CH6\_MSB Register**

7	6	5	4	3	2	1	0
MAX_VALUE_CH6_MSB[7:0]							
R-0b							

**Table 78. MAX\_CH6\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH6_MSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

**8.6.68 MAX\_CH7\_LSB Register (Address = 0x6E) [reset = 0x0]**

MAX\_CH7\_LSB is shown in [Figure 85](#) and described in [Table 79](#).

Return to the [Summary Table](#).

**Figure 85. MAX\_CH7\_LSB Register**

7	6	5	4	3	2	1	0
MAX_VALUE_CH7_LSB[7:0]							
R-0b							

**Table 79. MAX\_CH7\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH7_LSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

**8.6.69 MAX\_CH7\_MSB Register (Address = 0x6F) [reset = 0x0]**

MAX\_CH7\_MSB is shown in [Figure 86](#) and described in [Table 80](#).

Return to the [Summary Table](#).

**Figure 86. MAX\_CH7\_MSB Register**

7	6	5	4	3	2	1	0
MAX_VALUE_CH7_MSB[7:0]							
R-0b							

**Table 80. MAX\_CH7\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH7_MSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

**8.6.70 MIN\_CH0\_LSB Register (Address = 0x80) [reset = 0xFF]**

 MIN\_CH0\_LSB is shown in [Figure 87](#) and described in [Table 81](#).

 Return to the [Summary Table](#).

**Figure 87. MIN\_CH0\_LSB Register**

7	6	5	4	3	2	1	0
MIN_VALUE_CH0_LSB[7:0]							
R-11111111b							

**Table 81. MIN\_CH0\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH0_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

**8.6.71 MIN\_CH0\_MSB Register (Address = 0x81) [reset = 0xFF]**

 MIN\_CH0\_MSB is shown in [Figure 88](#) and described in [Table 82](#).

 Return to the [Summary Table](#).

**Figure 88. MIN\_CH0\_MSB Register**

7	6	5	4	3	2	1	0
MIN_VALUE_CH0_MSB[7:0]							
R-11111111b							

**Table 82. MIN\_CH0\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH0_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

**8.6.72 MIN\_CH1\_LSB Register (Address = 0x82) [reset = 0xFF]**

 MIN\_CH1\_LSB is shown in [Figure 89](#) and described in [Table 83](#).

 Return to the [Summary Table](#).

**Figure 89. MIN\_CH1\_LSB Register**

7	6	5	4	3	2	1	0
MIN_VALUE_CH1_LSB[7:0]							
R-11111111b							

**Table 83. MIN\_CH1\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH1_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

**8.6.73 MIN\_CH1\_MSB Register (Address = 0x83) [reset = 0xFF]**

 MIN\_CH1\_MSB is shown in [Figure 90](#) and described in [Table 84](#).

 Return to the [Summary Table](#).

Figure 90. MIN\_CH1\_MSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH1_MSB[7:0]							
R-11111111b							

Table 84. MIN\_CH1\_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH1_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

8.6.74 MIN\_CH2\_LSB Register (Address = 0x84) [reset = 0xFF]

MIN\_CH2\_LSB is shown in Figure 91 and described in Table 85.

Return to the Summary Table.

Figure 91. MIN\_CH2\_LSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH2_LSB[7:0]							
R-11111111b							

Table 85. MIN\_CH2\_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH2_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

8.6.75 MIN\_CH2\_MSB Register (Address = 0x85) [reset = 0xFF]

MIN\_CH2\_MSB is shown in Figure 92 and described in Table 86.

Return to the Summary Table.

Figure 92. MIN\_CH2\_MSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH2_MSB[7:0]							
R-11111111b							

Table 86. MIN\_CH2\_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH2_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

8.6.76 MIN\_CH3\_LSB Register (Address = 0x86) [reset = 0xFF]

MIN\_CH3\_LSB is shown in Figure 93 and described in Table 87.

Return to the Summary Table.

Figure 93. MIN\_CH3\_LSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH3_LSB[7:0]							
R-11111111b							

**Table 87. MIN\_CH3\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH3_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

**8.6.77 MIN\_CH3\_MSB Register (Address = 0x87) [reset = 0xFF]**

 MIN\_CH3\_MSB is shown in [Figure 94](#) and described in [Table 88](#).

 Return to the [Summary Table](#).

**Figure 94. MIN\_CH3\_MSB Register**

7	6	5	4	3	2	1	0
MIN_VALUE_CH3_MSB[7:0]							
R-11111111b							

**Table 88. MIN\_CH3\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH3_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

**8.6.78 MIN\_CH4\_LSB Register (Address = 0x88) [reset = 0xFF]**

 MIN\_CH4\_LSB is shown in [Figure 95](#) and described in [Table 89](#).

 Return to the [Summary Table](#).

**Figure 95. MIN\_CH4\_LSB Register**

7	6	5	4	3	2	1	0
MIN_VALUE_CH4_LSB[7:0]							
R-11111111b							

**Table 89. MIN\_CH4\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH4_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

**8.6.79 MIN\_CH4\_MSB Register (Address = 0x89) [reset = 0xFF]**

 MIN\_CH4\_MSB is shown in [Figure 96](#) and described in [Table 90](#).

 Return to the [Summary Table](#).

**Figure 96. MIN\_CH4\_MSB Register**

7	6	5	4	3	2	1	0
MIN_VALUE_CH4_MSB[7:0]							
R-11111111b							

**Table 90. MIN\_CH4\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH4_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

**8.6.80 MIN\_CH5\_LSB Register (Address = 0x8A) [reset = 0xFF]**

MIN\_CH5\_LSB is shown in [Figure 97](#) and described in [Table 91](#).

Return to the [Summary Table](#).

**Figure 97. MIN\_CH5\_LSB Register**

7	6	5	4	3	2	1	0
MIN_VALUE_CH5_LSB[7:0]							
R-11111111b							

**Table 91. MIN\_CH5\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH5_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

**8.6.81 MIN\_CH5\_MSB Register (Address = 0x8B) [reset = 0xFF]**

MIN\_CH5\_MSB is shown in [Figure 98](#) and described in [Table 92](#).

Return to the [Summary Table](#).

**Figure 98. MIN\_CH5\_MSB Register**

7	6	5	4	3	2	1	0
MIN_VALUE_CH5_MSB[7:0]							
R-11111111b							

**Table 92. MIN\_CH5\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH5_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

**8.6.82 MIN\_CH6\_LSB Register (Address = 0x8C) [reset = 0xFF]**

MIN\_CH6\_LSB is shown in [Figure 99](#) and described in [Table 93](#).

Return to the [Summary Table](#).

**Figure 99. MIN\_CH6\_LSB Register**

7	6	5	4	3	2	1	0
MIN_VALUE_CH6_LSB[7:0]							
R-11111111b							

**Table 93. MIN\_CH6\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH6_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

**8.6.83 MIN\_CH6\_MSB Register (Address = 0x8D) [reset = 0xFF]**

MIN\_CH6\_MSB is shown in [Figure 100](#) and described in [Table 94](#).

Return to the [Summary Table](#).

**Figure 100. MIN\_CH6\_MSB Register**

7	6	5	4	3	2	1	0
MIN_VALUE_CH6_MSB[7:0]							
R-11111111b							

**Table 94. MIN\_CH6\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH6_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

**8.6.84 MIN\_CH7\_LSB Register (Address = 0x8E) [reset = 0xFF]**

MIN\_CH7\_LSB is shown in [Figure 101](#) and described in [Table 95](#).

Return to the [Summary Table](#).

**Figure 101. MIN\_CH7\_LSB Register**

7	6	5	4	3	2	1	0
MIN_VALUE_CH7_LSB[7:0]							
R-11111111b							

**Table 95. MIN\_CH7\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH7_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

**8.6.85 MIN\_CH7\_MSB Register (Address = 0x8F) [reset = 0xFF]**

MIN\_CH7\_MSB is shown in [Figure 102](#) and described in [Table 96](#).

Return to the [Summary Table](#).

**Figure 102. MIN\_CH7\_MSB Register**

7	6	5	4	3	2	1	0
MIN_VALUE_CH7_MSB[7:0]							
R-11111111b							

**Table 96. MIN\_CH7\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH7_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

**8.6.86 RECENT\_CH0\_LSB Register (Address = 0xA0) [reset = 0x0]**

RECENT\_CH0\_LSB is shown in [Figure 103](#) and described in [Table 97](#).

Return to the [Summary Table](#).

**Figure 103. RECENT\_CH0\_LSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH0_LSB[7:0]							
R-0b							

**Table 97. RECENT\_CH0\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH0_LSB[7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

**8.6.87 RECENT\_CH0\_MSB Register (Address = 0xA1) [reset = 0x0]**

RECENT\_CH0\_MSB is shown in [Figure 104](#) and described in [Table 98](#).

Return to the [Summary Table](#).

**Figure 104. RECENT\_CH0\_MSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH0_MSB[7:0]							
R-0b							

**Table 98. RECENT\_CH0\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH0_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

**8.6.88 RECENT\_CH1\_LSB Register (Address = 0xA2) [reset = 0x0]**

RECENT\_CH1\_LSB is shown in [Figure 105](#) and described in [Table 99](#).

Return to the [Summary Table](#).

**Figure 105. RECENT\_CH1\_LSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH1_LSB[7:0]							
R-0b							

**Table 99. RECENT\_CH1\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH1_LSB[7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

**8.6.89 RECENT\_CH1\_MSB Register (Address = 0xA3) [reset = 0x0]**

RECENT\_CH1\_MSB is shown in [Figure 106](#) and described in [Table 100](#).

Return to the [Summary Table](#).

**Figure 106. RECENT\_CH1\_MSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH1_MSB[7:0]							
R-0b							

**Table 100. RECENT\_CH1\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH1_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

**8.6.90 RECENT\_CH2\_LSB Register (Address = 0xA4) [reset = 0x0]**

 RECENT\_CH2\_LSB is shown in [Figure 107](#) and described in [Table 101](#).

 Return to the [Summary Table](#).

**Figure 107. RECENT\_CH2\_LSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH2_LSB[7:0]							
R-0b							

**Table 101. RECENT\_CH2\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH2_LSB[7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

**8.6.91 RECENT\_CH2\_MSB Register (Address = 0xA5) [reset = 0x0]**

 RECENT\_CH2\_MSB is shown in [Figure 108](#) and described in [Table 102](#).

 Return to the [Summary Table](#).

**Figure 108. RECENT\_CH2\_MSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH2_MSB[7:0]							
R-0b							

**Table 102. RECENT\_CH2\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH2_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

**8.6.92 RECENT\_CH3\_LSB Register (Address = 0xA6) [reset = 0x0]**

 RECENT\_CH3\_LSB is shown in [Figure 109](#) and described in [Table 103](#).

 Return to the [Summary Table](#).

**Figure 109. RECENT\_CH3\_LSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH3_LSB[7:0]							
R-0b							

**Table 103. RECENT\_CH3\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH3_LSB[7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

**8.6.93 RECENT\_CH3\_MSB Register (Address = 0xA7) [reset = 0x0]**

 RECENT\_CH3\_MSB is shown in [Figure 110](#) and described in [Table 104](#).

 Return to the [Summary Table](#).

**Figure 110. RECENT\_CH3\_MSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH3_MSB[7:0]							
R-0b							

**Table 104. RECENT\_CH3\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH3_MSB [7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

**8.6.94 RECENT\_CH4\_LSB Register (Address = 0xA8) [reset = 0x0]**

RECENT\_CH4\_LSB is shown in [Figure 111](#) and described in [Table 105](#).

Return to the [Summary Table](#).

**Figure 111. RECENT\_CH4\_LSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH4_LSB[7:0]							
R-0b							

**Table 105. RECENT\_CH4\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH4_LSB [7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

**8.6.95 RECENT\_CH4\_MSB Register (Address = 0xA9) [reset = 0x0]**

RECENT\_CH4\_MSB is shown in [Figure 112](#) and described in [Table 106](#).

Return to the [Summary Table](#).

**Figure 112. RECENT\_CH4\_MSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH4_MSB[7:0]							
R-0b							

**Table 106. RECENT\_CH4\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH4_MSB [7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

**8.6.96 RECENT\_CH5\_LSB Register (Address = 0xAA) [reset = 0x0]**

RECENT\_CH5\_LSB is shown in [Figure 113](#) and described in [Table 107](#).

Return to the [Summary Table](#).

**Figure 113. RECENT\_CH5\_LSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH5_LSB[7:0]							
R-0b							

**Table 107. RECENT\_CH5\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH5_LSB[7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

**8.6.97 RECENT\_CH5\_MSB Register (Address = 0xAB) [reset = 0x0]**

 RECENT\_CH5\_MSB is shown in [Figure 114](#) and described in [Table 108](#).

 Return to the [Summary Table](#).

**Figure 114. RECENT\_CH5\_MSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH5_MSB[7:0]							
R-0b							

**Table 108. RECENT\_CH5\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH5_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

**8.6.98 RECENT\_CH6\_LSB Register (Address = 0xAC) [reset = 0x0]**

 RECENT\_CH6\_LSB is shown in [Figure 115](#) and described in [Table 109](#).

 Return to the [Summary Table](#).

**Figure 115. RECENT\_CH6\_LSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH6_LSB[7:0]							
R-0b							

**Table 109. RECENT\_CH6\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH6_LSB[7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

**8.6.99 RECENT\_CH6\_MSB Register (Address = 0xAD) [reset = 0x0]**

 RECENT\_CH6\_MSB is shown in [Figure 116](#) and described in [Table 110](#).

 Return to the [Summary Table](#).

**Figure 116. RECENT\_CH6\_MSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH6_MSB[7:0]							
R-0b							

**Table 110. RECENT\_CH6\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH6_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

**8.6.100 RECENT\_CH7\_LSB Register (Address = 0xAE) [reset = 0x0]**

RECENT\_CH7\_LSB is shown in [Figure 117](#) and described in [Table 111](#).

Return to the [Summary Table](#).

**Figure 117. RECENT\_CH7\_LSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH7_LSB[7:0]							
R-0b							

**Table 111. RECENT\_CH7\_LSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH7_LSB[7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

**8.6.101 RECENT\_CH7\_MSB Register (Address = 0xAF) [reset = 0x0]**

RECENT\_CH7\_MSB is shown in [Figure 118](#) and described in [Table 112](#).

Return to the [Summary Table](#).

**Figure 118. RECENT\_CH7\_MSB Register**

7	6	5	4	3	2	1	0
LAST_VALUE_CH7_MSB[7:0]							
R-0b							

**Table 112. RECENT\_CH7\_MSB Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH7_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

**8.6.102 GPO0\_TRIG\_EVENT\_SEL Register (Address = 0xC3) [reset = 0x2]**

GPO0\_TRIG\_EVENT\_SEL is shown in [Figure 119](#) and described in [Table 113](#).

Return to the [Summary Table](#).

**Figure 119. GPO0\_TRIG\_EVENT\_SEL Register**

7	6	5	4	3	2	1	0
GPO0_TRIG_EVENT_SEL[7:0]							
R/W-10b							

**Table 113. GPO0\_TRIG\_EVENT\_SEL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	GPO0_TRIG_EVENT_SEL[7:0]	R/W	10b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO0. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO0 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit trigger GPO0 output.

**8.6.103 GPO1\_TRIG\_EVENT\_SEL Register (Address = 0xC5) [reset = 0x2]**

GPO1\_TRIG\_EVENT\_SEL is shown in [Figure 120](#) and described in [Table 114](#).

Return to the [Summary Table](#).

**Figure 120. GPO1\_TRIG\_EVENT\_SEL Register**

7	6	5	4	3	2	1	0
GPO1_TRIG_EVENT_SEL[7:0]							
R/W-10b							

**Table 114. GPO1\_TRIG\_EVENT\_SEL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	GPO1_TRIG_EVENT_SEL[7:0]	R/W	10b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO1. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO1 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit trigger GPO1 output.

**8.6.104 GPO2\_TRIG\_EVENT\_SEL Register (Address = 0xC7) [reset = 0x2]**

 GPO2\_TRIG\_EVENT\_SEL is shown in [Figure 121](#) and described in [Table 115](#).

 Return to the [Summary Table](#).

**Figure 121. GPO2\_TRIG\_EVENT\_SEL Register**

7	6	5	4	3	2	1	0
GPO2_TRIG_EVENT_SEL[7:0]							
R/W-10b							

**Table 115. GPO2\_TRIG\_EVENT\_SEL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	GPO2_TRIG_EVENT_SEL[7:0]	R/W	10b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO2. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO2 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit trigger GPO2 output.

**8.6.105 GPO3\_TRIG\_EVENT\_SEL Register (Address = 0xC9) [reset = 0x2]**

 GPO3\_TRIG\_EVENT\_SEL is shown in [Figure 122](#) and described in [Table 116](#).

 Return to the [Summary Table](#).

**Figure 122. GPO3\_TRIG\_EVENT\_SEL Register**

7	6	5	4	3	2	1	0
GPO3_TRIG_EVENT_SEL[7:0]							
R/W-10b							

**Table 116. GPO3\_TRIG\_EVENT\_SEL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	GPO3_TRIG_EVENT_SEL[7:0]	R/W	10b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO3. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO3 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit trigger GPO3 output.

**8.6.106 GPO4\_TRIG\_EVENT\_SEL Register (Address = 0xCB) [reset = 0x2]**

GPO4\_TRIG\_EVENT\_SEL is shown in [Figure 123](#) and described in [Table 117](#).

Return to the [Summary Table](#).

**Figure 123. GPO4\_TRIG\_EVENT\_SEL Register**

7	6	5	4	3	2	1	0
GPO4_TRIG_EVENT_SEL[7:0]							
R/W-10b							

**Table 117. GPO4\_TRIG\_EVENT\_SEL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	GPO4_TRIG_EVENT_SEL[7:0]	R/W	10b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO4. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO4 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit trigger GPO4 output.

**8.6.107 GPO5\_TRIG\_EVENT\_SEL Register (Address = 0xCD) [reset = 0x2]**

GPO5\_TRIG\_EVENT\_SEL is shown in [Figure 124](#) and described in [Table 118](#).

Return to the [Summary Table](#).

**Figure 124. GPO5\_TRIG\_EVENT\_SEL Register**

7	6	5	4	3	2	1	0
GPO5_TRIG_EVENT_SEL[7:0]							
R/W-10b							

**Table 118. GPO5\_TRIG\_EVENT\_SEL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	GPO5_TRIG_EVENT_SEL[7:0]	R/W	10b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO5. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO5 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit trigger GPO5 output.

**8.6.108 GPO6\_TRIG\_EVENT\_SEL Register (Address = 0xCF) [reset = 0x2]**

GPO6\_TRIG\_EVENT\_SEL is shown in [Figure 125](#) and described in [Table 119](#).

Return to the [Summary Table](#).

**Figure 125. GPO6\_TRIG\_EVENT\_SEL Register**

7	6	5	4	3	2	1	0
GPO6_TRIG_EVENT_SEL[7:0]							
R/W-10b							

**Table 119. GPO6\_TRIG\_EVENT\_SEL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	GPO6_TRIG_EVENT_SEL[7:0]	R/W	10b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO6. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO6 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit trigger GPO6 output.

**8.6.109 GPO7\_TRIG\_EVENT\_SEL Register (Address = 0xD1) [reset = 0x2]**

 GPO7\_TRIG\_EVENT\_SEL is shown in [Figure 126](#) and described in [Table 120](#).

 Return to the [Summary Table](#).

**Figure 126. GPO7\_TRIG\_EVENT\_SEL Register**

7	6	5	4	3	2	1	0
GPO7_TRIG_EVENT_SEL[7:0]							
R/W-10b							

**Table 120. GPO7\_TRIG\_EVENT\_SEL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	GPO7_TRIG_EVENT_SEL[7:0]	R/W	10b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO7. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO7 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit trigger GPO7 output.

**8.6.110 GPO\_TRIGGER\_CFG Register (Address = 0xE9) [reset = 0x0]**

 GPO\_TRIGGER\_CFG is shown in [Figure 127](#) and described in [Table 121](#).

 Return to the [Summary Table](#).

**Figure 127. GPO\_TRIGGER\_CFG Register**

7	6	5	4	3	2	1	0
GPO_TRIGGER_UPDATE_EN[7:0]							
R/W-0b							

**Table 121. GPO\_TRIGGER\_CFG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	GPO_TRIGGER_UPDATE_EN[7:0]	R/W	0b	Update digital outputs GPO[7:0] when corresponding trigger is set. 0b = Digital output is not updated in response to alert flags. 1b = Digital output is updated when corresponding alert flags are set. Configure GPOx_TRIG_EVENT_SEL register to select which alert flags can trigger an update on the desired GPO.

**8.6.111 GPO\_VALUE\_TRIG Register (Address = 0xEB) [reset = 0x0]**

 GPO\_VALUE\_TRIG is shown in [Figure 128](#) and described in [Table 122](#).

 Return to the [Summary Table](#).

**Figure 128. GPO\_VALUE\_TRIG Register**

7	6	5	4	3	2	1	0
GPO_VALUE_ON_TRIGGER[7:0]							
R/W-0b							

**Table 122. GPO\_VALUE\_TRIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	GPO_VALUE_ON_TRIGGER[7:0]	R/W	0b	Value to be set on digital outputs GPO[7:0] when corresponding trigger occurs. GPO update on alert flags must be enabled in corresponding bit in GPO_TRIGGER_CFG register. 0b = Digital output set to logic 0. 1b = Digital output set to logic 1.

## 9 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The two primary circuits required to maximize the performance of a high-precision, successive approximation register (SAR), analog-to-digital converter (ADC) are the input driver and the reference driver circuits. This section details some general principles for designing the input driver circuit, reference driver circuit, and provides some application circuits designed for the ADS7138.

### 9.2 Typical Applications

#### 9.2.1 Mixed-Channel Configuration

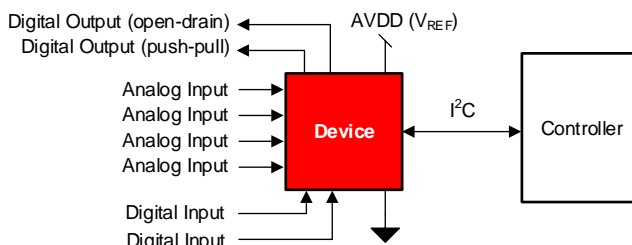


图 129. DAQ Circuit: Single-Supply DAQ

##### 9.2.1.1 Design Requirements

The goal of this application is to configure some channels of the ADS7138 as digital inputs, open-drain digital outputs, and push-pull digital outputs.

##### 9.2.1.2 Detailed Design Procedure

The ADS7138 can support GPIO functionality at each input pin. Any analog input pin can be independently configured as a digital input, a digital open-drain output, or a digital push-pull output through the PIN\_CFG and GPIO\_CFG registers; see 表 4.

##### 9.2.1.2.1 Digital Input

The digital input functionality can be used to monitor a signal within the system. 图 130 illustrates that the state of the digital input can be read from the GPI\_VALUE register.

Typical Applications (接下页)

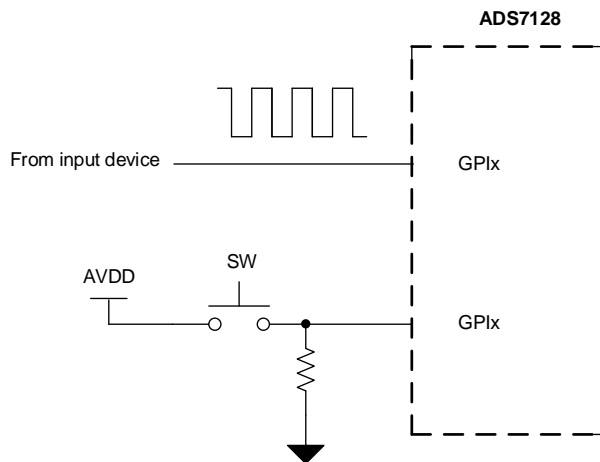


图 130. Digital Input

9.2.1.2.2 Digital Open-Drain Output

The channels of the ADS7138 can be configured as digital open-drain outputs supporting an output voltage up to 5.5 V. An open-drain output, as shown in 图 131, consists of an internal FET (Q) connected to ground. The output is idle when not driven by the device, which means Q is off and the pull-up resistor,  $R_{PULL\_UP}$ , connects the GPOx node to the desired output voltage. The output voltage can range anywhere up to 5.5 V, depending on the external voltage that the GPIOx is pulled up to. When the device is driving the output, Q turns on, thus connecting the pull-up resistor to ground and bringing the node voltage at GPOx low.

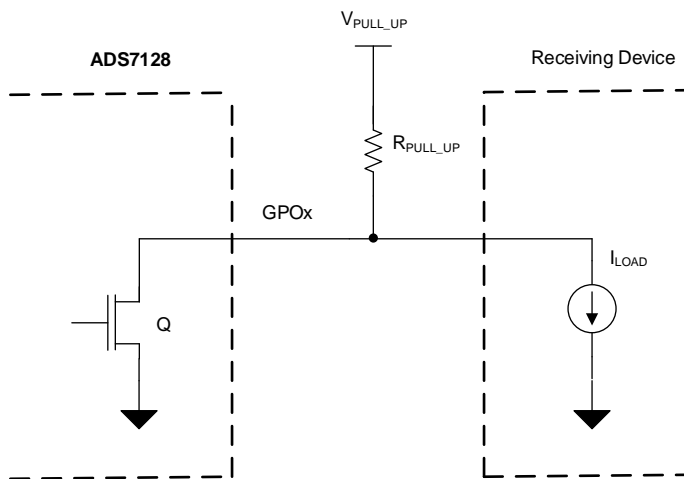


图 131. Digital Open-Drain Output

The minimum value of the pullup resistor, as calculated in 公式 3, is given by the ratio of  $V_{PULL\_UP}$  and the maximum current supported by the device digital output (5 mA).

$$R_{MIN} = (V_{PULL\_UP} / 5 \text{ mA}) \tag{3}$$

The maximum value of the pullup resistor, as calculated in 公式 4, depends on the minimum input current requirement,  $I_{LOAD}$ , of the receiving device driven by this GPIO.

$$R_{MAX} = (V_{PULL\_UP} / I_{LOAD}) \tag{4}$$

Select  $R_{PULL\_UP}$  such that  $R_{MIN} < R_{PULL\_UP} < R_{MAX}$ .

ADVANCE INFORMATION

Typical Applications (接下页)

9.2.1.3 Digital Push-Pull Output

The channels of the ADS7138 can be configured as digital push-pull outputs supporting an output voltage up to AVDD. As shown in 图 132, a push-pull output consists of two mirrored opposite bipolar transistors, Q1 and Q2. The device can both source and sink current because only one transistor is on at a time (either Q2 is on and pulls the output low, or Q1 is on and sets the output high). A push-pull configuration always drives the line opposed to an open-drain output where the line is left floating.

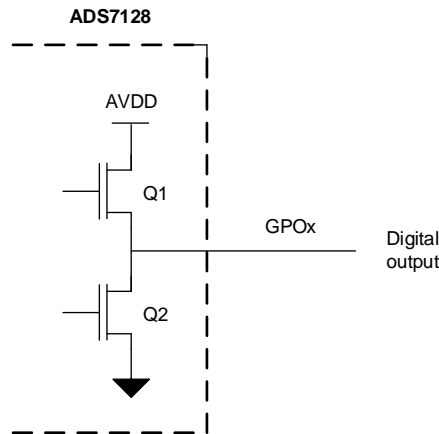


图 132. Digital Push-Pull Output

10 Power Supply Recommendations

10.1 AVDD and DVDD Supply Recommendations

The ADS7138 has two separate power supplies: AVDD and DVDD. The device operates on AVDD; DVDD is used for the interface circuits. For supplies greater than 2.35 V, AVDD and DVDD can be shorted externally if single-supply operation is desired. The AVDD supply also defines the full-scale input range of the device. Decouple the AVDD and DVDD pins individually, as shown in 图 133, with 1-μF ceramic decoupling capacitors. The minimum capacitor value required for AVDD and DVDD is 200 nF and 20 nF, respectively. If both supplies are powered from the same source, a minimum capacitor value of 220 nF is required for decoupling.

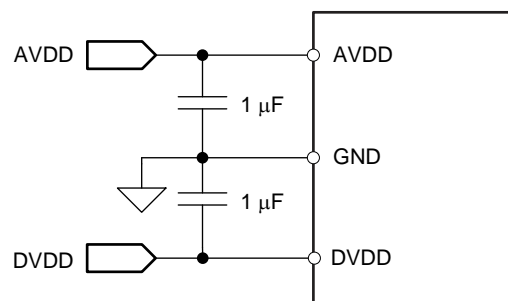


图 133. Power-Supply Decoupling

## 11 Layout

### 11.1 Layout Guidelines

图 134 shows a board layout example for the ADS7138. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the AVDD supply away from noise sources.

Use 1- $\mu$ F ceramic bypass capacitors in close proximity to the analog (AVDD) and digital (DVDD) power-supply pins. Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors. Connect the GND pin to the ground plane using short, low-impedance paths. The AVDD supply voltage also functions as the reference voltage for the ADS7138. Place the decoupling capacitor ( $C_{REF}$ ) for AVDD close to the device AVDD and GND pins and connect  $C_{REF}$  to the device pins with thick copper tracks.

### 11.2 Layout Example

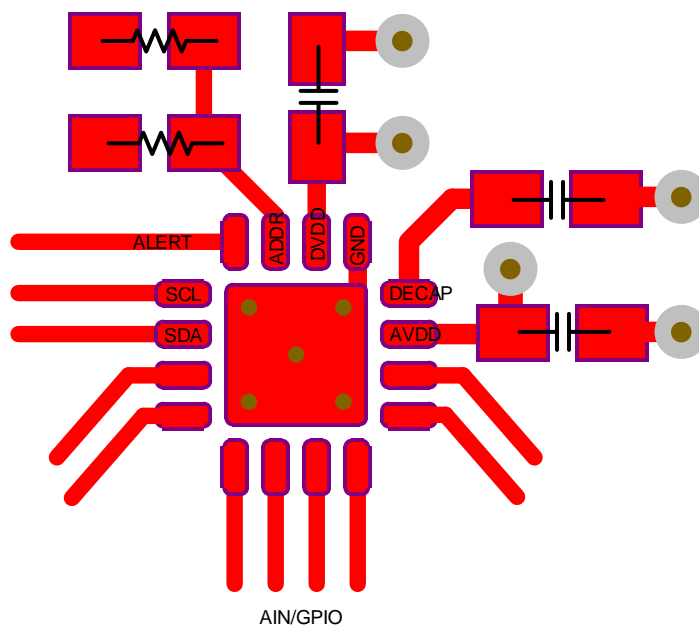


图 134. Example Layout

## 12 器件和文档支持

### 12.1 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](http://TI.com.cn) 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 12.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.3 商标

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### 12.4 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7138IRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7138	<a href="#">Samples</a>
ADS7138IRTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7138	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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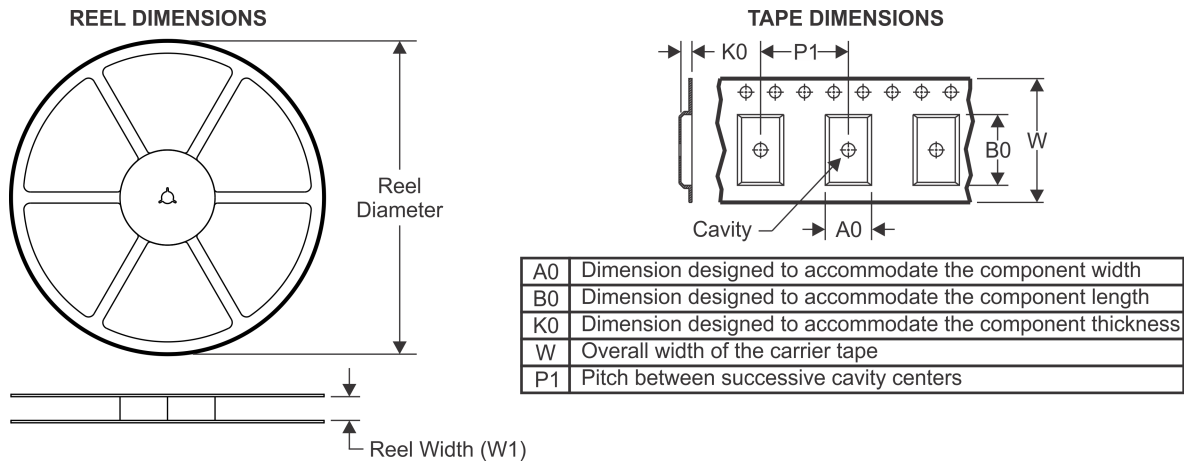
**OTHER QUALIFIED VERSIONS OF ADS7138 :**

- Automotive : [ADS7138-Q1](#)

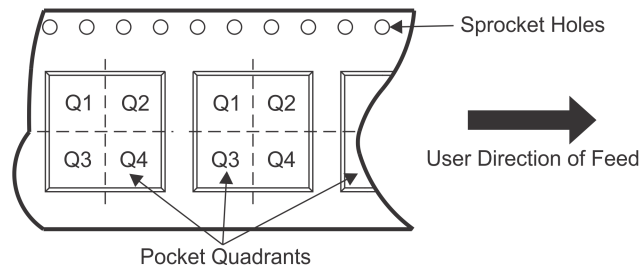
## NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

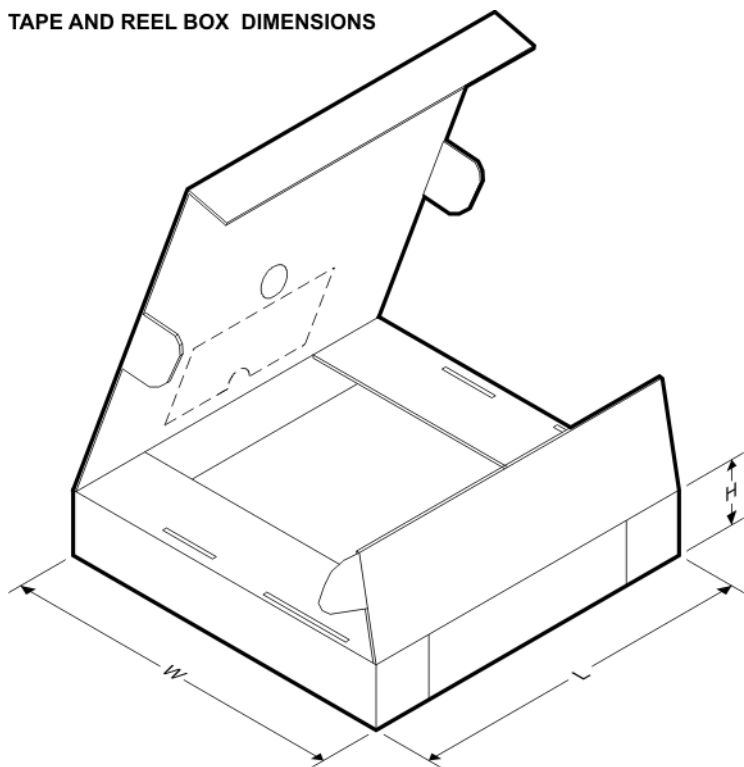


### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7138IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7138IRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7138IRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
ADS7138IRTET	WQFN	RTE	16	250	210.0	185.0	35.0

## GENERIC PACKAGE VIEW

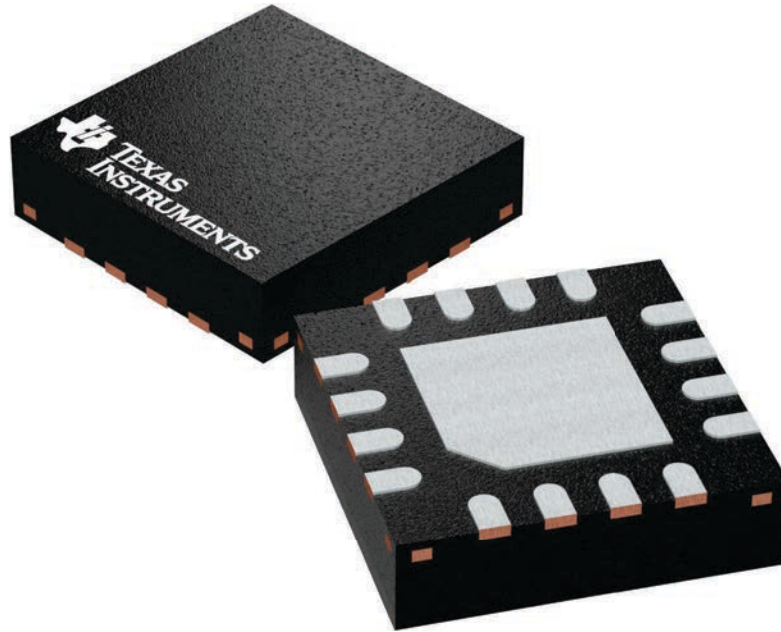
**RTE 16**

**WQFN - 0.8 mm max height**

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225944/A

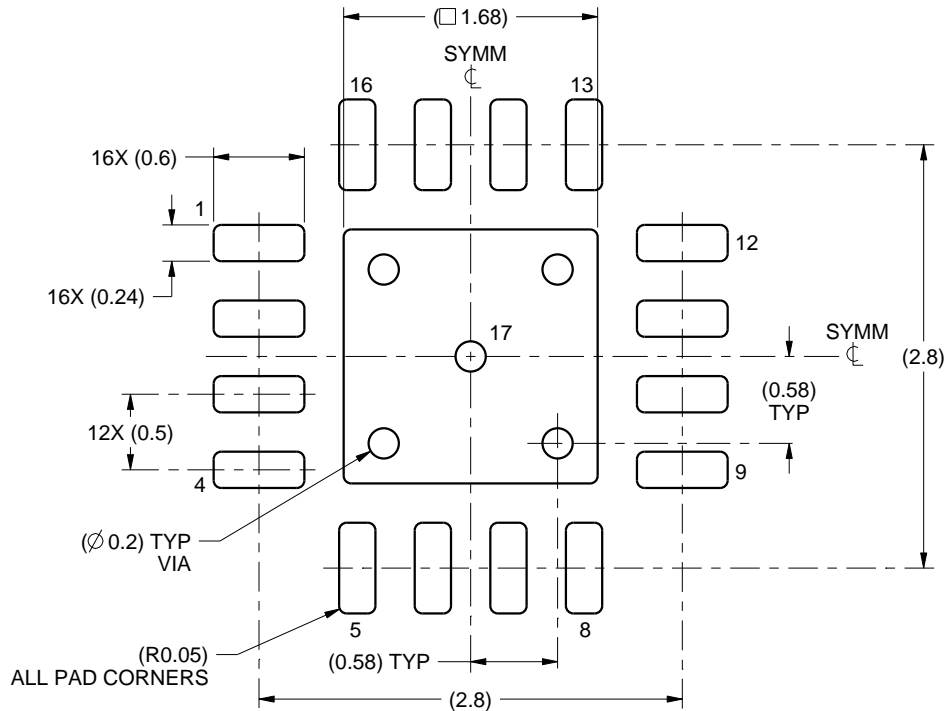


# EXAMPLE BOARD LAYOUT

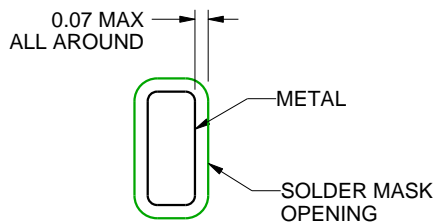
RTE0016C

WQFN - 0.8 mm max height

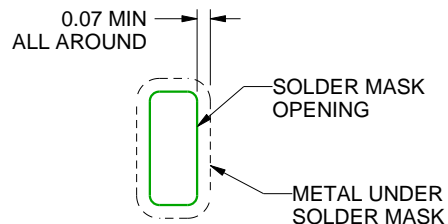
PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



NON SOLDER MASK  
DEFINED  
(PREFERRED)



SOLDER MASK  
DEFINED

## SOLDER MASK DETAILS

4219117/A 09/2016

NOTES: (continued)

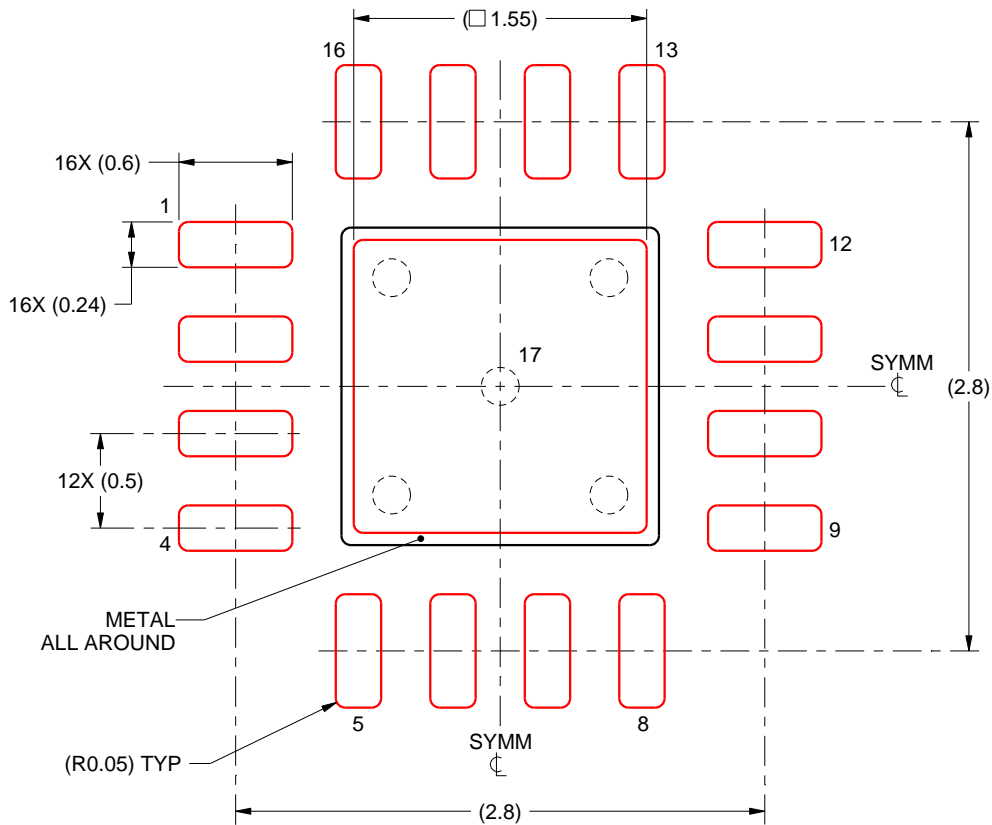
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:  
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

4219117/A 09/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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