Burr-Brown Products from Texas Instruments

ADS8364

SBAS219C – JUNE 2002 – REVISED AUGUST 2006

250kSPS, 16-Bit, 6-Channel Simultaneous Sampling ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- 6 INPUT CHANNELS
- FULLY DIFFERENTIAL INPUTS
- 6 INDEPENDENT 16-BIT ADC
- 4µs TOTAL THROUGHPUT PER CHANNEL
- TESTED NO MISSING CODES TO 14 BITS
- BUFFERED REFERENCE INPUTS
- LOW POWER: 450mW
- TQFP-64 PACKAGE

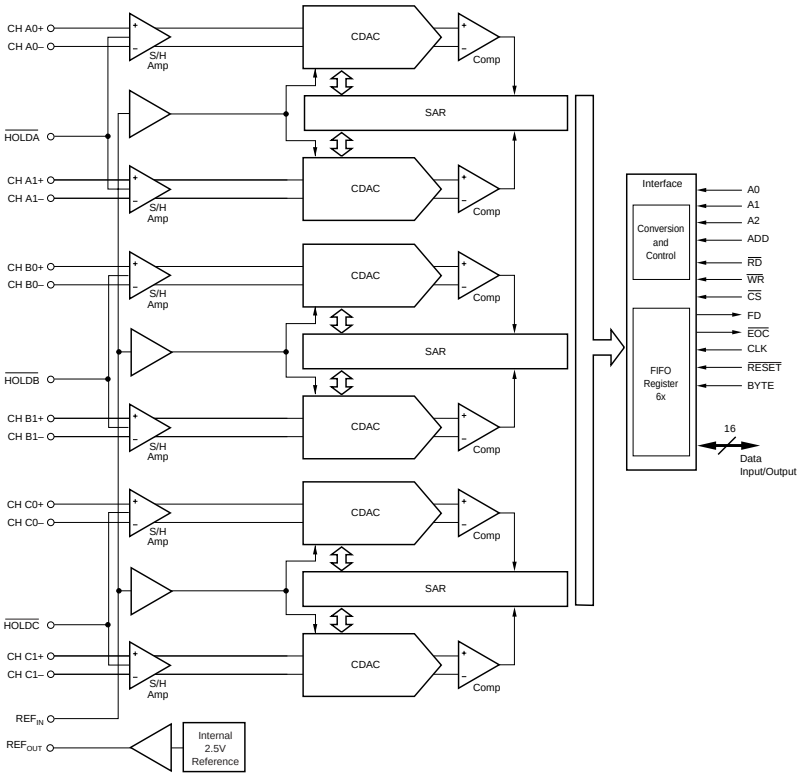
APPLICATIONS

- MOTOR CONTROL
- MULTI-AXIS POSITIONING SYSTEMS
- 3-PHASE POWER CONTROL

DESCRIPTION

The ADS8364 includes six, 16-bit, 250kSPS ADCs (Analog-to- Digital converters) with 6 fully differential input channels grouped into two pairs for high-speed simultaneous signal acquisition. Inputs to the sample-and-hold amplifiers are fully differential and are maintained differential to the input of the ADC. This provides excellent common-mode rejection of 80dB at 50KHz that is important in high-noise environments.

The ADS8364 offers a flexible high-speed parallel interface with a direct address mode, a cycle, and a FIFO mode. The output data for each channel is available as a 16-bit word.



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ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings over operating free-air temperature (unless otherwise noted)[1]

Supply Voltage, AGND to AV_{DD}	–0.3V to 6V
Supply Voltage, BGND to BV_{DD}	–0.3V to 6V
Supply Voltage, DGND to DV_{DD}	–0.3V to 6V
Analog Input Voltage Range	AGND – 0.3V to AV_{DD} + 0.3V
Reference Input Voltage	AGND – 0.3V to AV_{DD} + 0.3V
Digital Input Voltage Range	BGND – 0.3V to BV_{DD} + 0.3V
Ground Voltage Differences, AGND to BGND/DGND	±0.3V
Voltage Differences, BV_{DD}, DV_{DD} to AGND	–0.3V to 6V
Input Current ot Any Pin Except Supply	–20mA to 20mA
Power Dissipation	See Dissipation Rating Table
Operating Virtual Junction Temperature Range, T_J	–40°C to 150°C
Operating Free-Air Temperature Range, T_A	–40°C to 85°C
Storage Temperature Range, T_{STG}	–65°C to 150°C
Lead Temperature 1.6mm (1/16 inch) from Case for 10sec	260°C

NOTE: (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions of extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION[1]

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	NO MISSING CODES ERROR (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS8364Y	±8	14	TQFP-64	PAG	–40°C to +85°C	ADS8364Y/250	Tape and Reel, 250
"	"	"	"	"	"	ADS8364Y/2K	Tape and Reel, 2000

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI web site at www.ti.com.

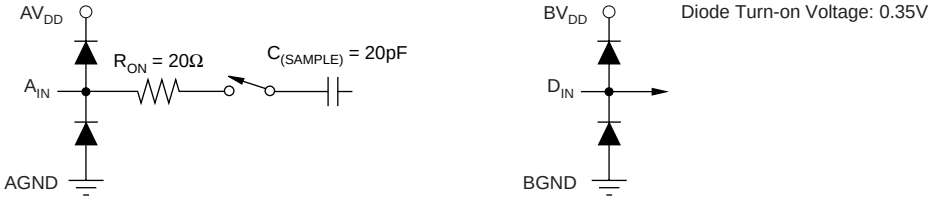
PACKAGE DISSIPATION RATING TABLE

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = +25°C	$T_A \leq$ +25°C POWER RATING	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING
Low-K[1]	PAG	8.6°C/W	68.5°C/W	14.598mW/°C	1824mW	1168mW	949mW
High-K[2]	PAG	8.6°C/W	42.8°C/W	23.364mw/°C	2920mW	1869mW	1519mW

NOTES: (1) The JEDEC Low K (1s) board design used to derive this data was a 3-inch x 3-inch, two-layer board with 2-ounce copper traces on top of the board. (2) The JEDEC High K (2s2p) board design used to derive this data was a 3-inch x 3-inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on the top and bottom of the board.

RECOMMENDED OPERATING CONDITIONS		MIN	NOM	MAX	UNIT
Supply Voltage, AGND to AV_{DD}		4.75	5	5.25	V
Supply Voltage, BGND to BV_{DD}	Low-Voltage Levels	2.7		3.6	V
	5V Logic Levels	4.5	5	5.5	V
Supply Voltage, DGND to DV_{DD}		4.75	5	5.25	V
Difference AV_{DD} to DV_{DD}		–0.3	0	0.3	V
Reference Input Voltage		1.5	2.5	2.6	V
Operating Common-Mode Signal	–IN	2.2	2.5	2.8	V
Analog Inputs	+IN – (–IN)	0		$\pm V_{REF}$	V
Operating Junction Temperature Range, T_J		–40		125	°C

EQUIVALENT INPUT CIRCUIT



Equivalent Analog Input Circuit

Equivalent Digital Input Circuit

ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at –40°C to +85°C, AV_{DD} = DV_{DD} = 5V, BV_{DD} = 3V, V_{REF} = internal +2.5V, f_{CLK} = 5MHz, f_{SAMPLE} = 250kSPS, unless otherwise noted.

PARAMETER		CONDITIONS	ADS8364Y MIN	ADS8364Y TYP(1)	ADS8364Y MAX	UNITS
ANALOG INPUT						
Full-Scale Range	(FSR)	+IN – (–IN)			$\pm V_{REF}$	V
Operating Common-Mode Signal			2.2		2.8	V
Input Resistance		–IN = V_{REF}		20		Ω
Input Capacitance		–IN = V_{REF}		25		pF
Input Leakage Current		–IN = V_{REF}		±1		nA
Differential Input Resistance		–IN = V_{REF}		40		Ω
Differential Input Capacitance		–IN = V_{REF}		50		pF
Common-Mode Rejection Ratio	(CMRR)	At DC		84		dB
		V_{IN} = ±1.25V_{PP} at 50kHz		80		dB
Bandwith	(BW)	FS Sinewave, –3dB		300		MHz
DC ACCURACY						
Resolution			16			Bits
No Missing Codes	(NMC)		14			Bits
Integral Linearity Error	(INL)			±3	±8	LSB
Integral Linearity Match		Only pair wise matching		1.5		LSB
Differential Nonlinearity	(DNL)	Specified only for 14-Bit		±1.5		LSB
Bipolar Offset Error	(V_{OS})			±0.05	±2	mV
Bipolar Offset Error Match		Only pair wise matching		0.2	1	mV
Bipolar Offset Error Drift	(TCV_{OS})			0.8		ppm/°C
Gain Error	(G_{ERR})	Referenced to V_{REF}		±0.05	±0.25	%FSR
Gain Error Match		Only pair wise matching		0.005	0.05	%FSR
Gain Error Drift	(TCG_{ERR})			2		ppm/°C
Noise				120		μV_{RMS}
Power-Supply Rejection Ratio	(PSRR)	4.75V < AV_{DD} < 5.25V		–87		dB
SAMPLING DYNAMICS						
Conversion Time per ADC	(t_{CONV})	50kHz ≤ f_{CLK} ≤ 5MHz	3.2		320	µs
Acquisition Time	(t_{AQ})	f_{CLK} = 5MHz	800			ns
Throughput Rate					250	kSPS
Aperture Delay					5	ns
Aperture Delay Matching				100		ps
Aperture Jitter				50		ps
Clock Frequncy			0.05		5	MHz
AC ACCURACY						
Total Harmonic Distortion	(THD)	V_{IN} = ±2.5V_{PP} at 100kHz		–92		dB
Spurous-Free Dynamic Range	(SFDR)	V_{IN} = ±2.5V_{PP} at 100kHz		93.5		dB
Signal-to-Noise Ratio	(SNR)	V_{IN} = ±2.5V_{PP} at 100kHz		83.2		dB
Signal-to-Noise Ratio + Distortion	(SINAD)	V_{IN} = ±2.5V_{PP} at 100kHz		82.5		dB
Channel-to-Channel Isolation		V_{IN} = ±2.5V_{PP} at 50kHz		95		dB
Effective Number of Bits	(ENOB)			13.3		Bits
VOLTAGE REFERENCE OUTPUT						
Reference Voltage Output	(V_{OUT})		2.475	2.5	2.525	V
Initial Accuracy					±1	%
Output Voltage Temperature Drift	(dV_{OUT}/dT)			±20		ppm/°C
Output Voltage Noise		f = 0.1Hz to 10Hz, C_L = 10µF		40		μV_{PP}
		f = 10Hz to 10kHz, C_L = 10µF		8		µVRMS
Power-Supply Refection Ratio	(PSRR)			60		dB
Output Current	(I_{OUT})			10		µA
Short-Circuit Current	(I_{SC})			0.5		mA
Turn-On Settling Time		to 0.1% at C_L = 0		100		µs
VOLTAGE REFERENCE INPUT						
Reference Voltage Input	(V_{IN})		1.5	2.5	2.6	V
Reference Input Resistance			100			MΩ
Reference Input Capacitance				5		pF
Reference Input Current					1	µA

NOTE: (1) All values are at T_A = +25°C.

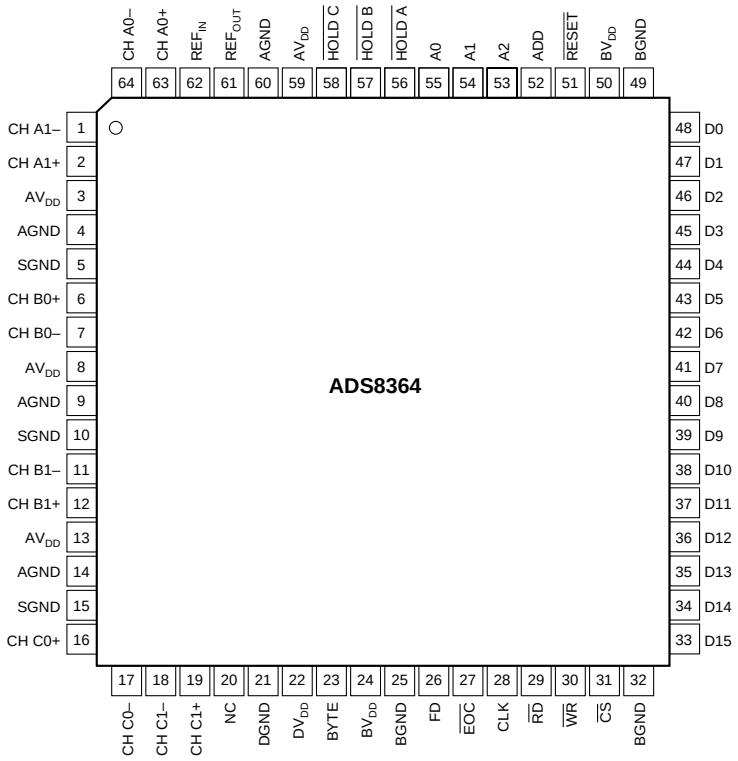
ELECTRICAL CHARACTERISTICS (Cont.)

Over recommended operating free-air temperature range at –40°C to +85°C, $AV_{DD} = DV_{DD} = 5V$, V_{REF} = internal +2.5V, f_{CLK} = 5MHz, f_{SAMPLE} = 250kSPS, unless otherwise noted.

PARAMETER		CONDITIONS	ADS8364Y MIN	ADS8364Y TYP[1]	ADS8364Y MAX	UNITS
DIGITAL INPUTS[2]						
Logic Family				CMOS		
High-Level Input Voltage	(V_{IH})		0.7 • BV_{DD}		BV_{DD} + 0.3	V
Low-Level Input Voltage	(V_{IL})		–0.3		0.3 • BV_{DD}	V
Input Current	(I_{IN})	$V_I = BV_{DD}$ or GND			±50	nA
Input Capacitance	(C_I)			5		pF
DIGITAL OUTPUTS[2]						
Logic Family				CMOS		
High-Level Output Voltage	(V_{OH})	BV_{DD} = 4.5V, I_{OH} = –100µA	4.44			V
Low-Level Output Voltage	(V_{OL})	BV_{DD} = 4.5V, I_{OL} = 100µA			0.5	V
High-Impedance-State Output Current	(I_{OZ})	$\overline{CS}$ = BV_{DD}, $V_I = BV_{DD}$ or GND			±50	nA
Output Capacitance	(C_O)			5		pF
Load Capacitance	(C_L)				30	pF
Data Format				Binary Two's Complement		
DIGITAL INPUTS[3]						
Logic Family				LVCMOS		
High-Level Input Voltage	(V_{IH})	BV_{DD} = 3.6V	2		BV_{DD} + 0.3	V
Low-Level Input Voltage	(V_{IL})	BV_{DD} = 2.7V	–0.3		0.8	V
Input Current	(I_{IN})	$V_I = BV_{DD}$ or GND			±50	nA
Input Capacitance	(C_I)			5		pF
DIGITAL OUTPUTS[3]						
Logic Family				LVCMOS		
High-Level Output Voltage	(V_{OH})	BV_{DD} = 2.7V, I_{OH} = –100µA	BV_{DD} – 0.2			V
Low-Level Output Voltage	(V_{OL})	BV_{DD} = 2.7V, I_{OL} = 100µA			0.2	V
High-Impedance-State Output Current	(I_{OZ})	$\overline{CS}$ = BV_{DD}, VI = BV_{DD} or GND			±50	nA
Output Capacitance	(C_O)			5		pF
Load Capacitance	(C_L)				30	pF
Data Format				Binary Two's Complement		
POWER SUPPLY						
Analog Supply Voltage	(AV_{DD})		4.75		5.25	V
Buffer I/O Supply Voltage	(BV_{DD})	Low-Voltage Levels	2.7		3.6	V
		5V Logic Levels	4.5		5.5	V
Digital Supply Voltage	(DV_{DD})		4.75		5.25	V
Analog Operating Supply Current	(AI_{DD})			80	90	mA
Buffer I/O Operating Supply Current	(BI_{DD})	BV_{DD} = 3V			300	µA
		BV_{DD} = 5V		200	300	µA
Digital Operating Supply Current	(DI_{DD})			2.5	4	mA
Power Dissipation		BV_{DD} = 3V		413.1	470.9	mW
		BV_{DD} = 5V		413.5	471.5	mW

NOTES: (1) All values are at T_A = +25°C.
(2) Applies for 5.0V nominal Supply: BV_{DD} (min) = 4.5V and BV_{DD} (max) = 5.5V.
(3) Applies for 3.0V nominal Supply: BV_{DD} (min) = 2.7V and BV_{DD} (max) = 3.6V.

PIN CONFIGURATION

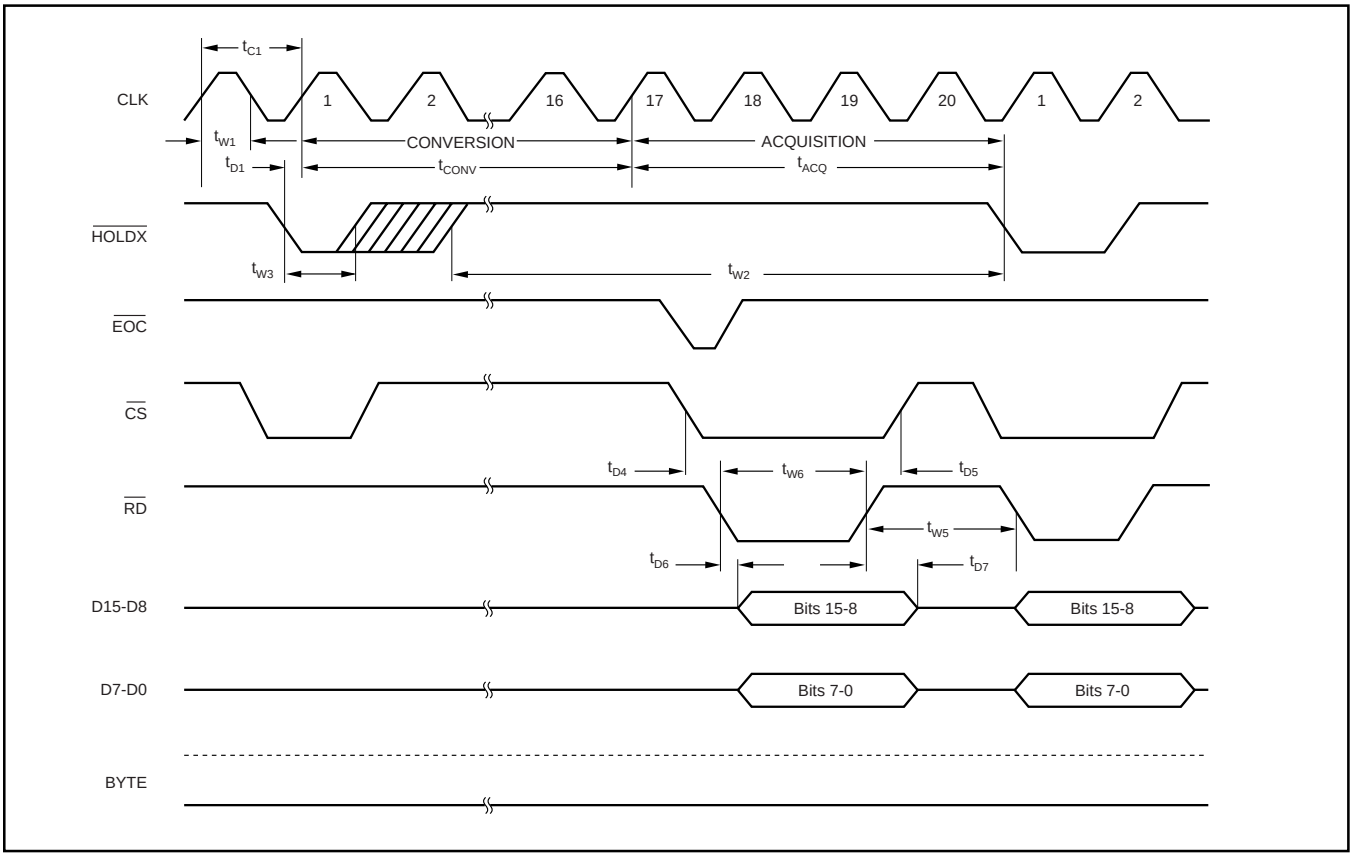


PIN DESCRIPTIONS

PIN	NAME	I/O	DESCRIPTION	PIN	NAME	I/O	DESCRIPTION
1	CH A1–	AI	Inverting Input Channel A1	32	BGND	P	Buffer Digital Ground
2	CH A1+	AI	Noninverting Input channel A1	33	DB15	DO	Data Bit 15-MSB
3	AV_{DD}	P	Analog Power Supply	34	DB14	DO	Data Bit 14
4	AGND	P	Analog Ground	35	DB13	DO	Data Bit 13
5	SGND	P	Signal Ground	36	DB12	DO	Data Bit 12
6	CH B0+	AI	Noninverting Input Channel B0	37	DB11	DO	Data Bit 11
7	CH B0–	AI	Inverting Input Channel B0	38	DB10	DO	Data Bit 10
8	AV_{DD}	P	Analog Power Supply	39	DB9	DO	Data Bit 9
9	AGND	P	Analog Ground	40	DB8	DO	Data Bit 8
10	SGND	P	Signal Ground	41	DB7	DIO	Data Bit 7, Software Input 7
11	CH B1–	AI	Inverting Input Channel B1	42	DB6	DIO	Data Bit 6, Software Input 6
12	CH B1+	AI	Noninverting Input Channel B1	43	DB5	DIO	Data Bit 5, Software Input 5
13	AV_{DD}	P	Analog Power Supply	44	DB4	DIO	Data Bit 4, Software Input 4
14	AGND	P	Analog Ground	45	DB3	DIO	Data Bit 3, Software Input 3
15	SGND	P	Signal Ground	46	DB2	DIO	Data Bit 2, Software Input 2
16	CH C0+	AI	Noninverting Input Channel C0	47	DB1	DIO	Data Bit 1, Software Input 1
17	CH C0–	AI	Inverting Input Channel C0	48	DB0	DIO	Data Bit 0, Software Input 0
18	CH C1–	AI	Inverting Input Channel C1	49	BGND	P	Buffer Digital Ground
19	CH C1+	AI	Noninverting Input Channel C1	50	BV_{DD}	P	Power Supply for Digital Interface from 3V to 5V
20	NC	–	No Connection	51	$\overline{RESET}$	DI	Global Reset, Active LOW
21	DGND	P	Digital ground connected to AGND.	52	ADD	DI	Address Mode Select
22	DV_{DD}	P	+5V Power Supply for Digital Logic Connected to AV_{DD}.	53	A2	DI	Address Line 3
23	BYTE	DI	2 x 8 Output Capability. Active HIGH.	54	A1	DI	Address Line 2
24	BV_{DD}	P	Power supply for digital interface from 3V to 5V.	55	A0	DI	Address Line 1
25	BGND	P	Buffer Digital Ground	56	$\overline{HOLDA}$	DI	Hold Command A
26	FD	DO	First Data, A0 Data	57	$\overline{HOLDB}$	DI	Hold Command B
27	$\overline{EOC}$	DO	End of Conversion, Active LOW	58	$\overline{HOLDC}$	DI	Hold Command C
28	CLK	DI	An external CMOS compatible clock can be applied to the CLK input to synchronize the conversion process to an external source.	59	AV_{DD}	P	Analog Power Supply
				60	AGND	P	Analog Ground
				61	REF_{OUT}	AO	Reference Output, attach 0.1µF and 10µF capacitors.
29	$\overline{RD}$	DI	Read, Active LOW	62	REF_{IN}	AI	Reference Input
30	$\overline{WR}$	DI	Write, Active LOW	63	CH A0+	AI	Noninverting Input Channel A0
31	$\overline{CS}$	DI	Chip Select, Active LOW	64	CH A0–	AI	Inverting Input Channel A0

NOTE: AI is Analog Input, AO is Analog Output, DI is Digital Input, DO is Digital Output, DIO is Digital Input/Output, P is Power Supply Connection.

TIMING CHARACTERISTICS



TIMING CHARACTERISTICS TABLE

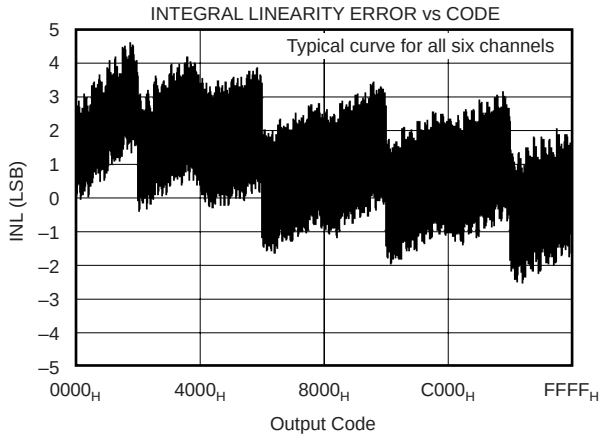
Timing Characteristics over recommended operating free-air temperature range T_{MIN} to T_{MAX}, $AV_{DD} = DV_{DD} = 5V$, $REF_{IN} = REF_{OUT}$ internal reference +2.5V, $f_{CLK} = 5MHz$, $f_{SAMPLE} = 250kSPS$, $BV_{DD} = 2.7 \div 5V$ (unless otherwise noted).

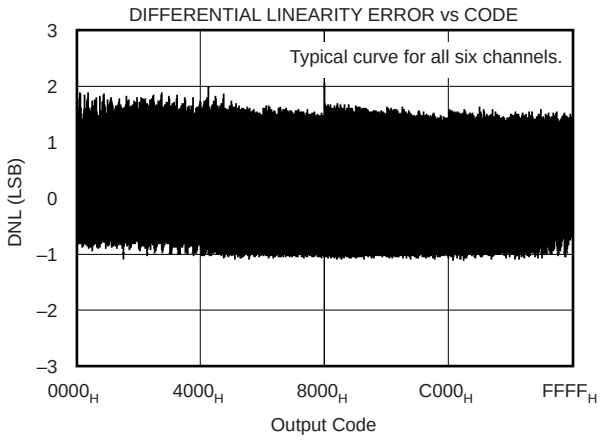
SPEC	DESCRIPTION		MIN	TYP(1)	MAX	UNITS
t_{CONV}	Conversion Time				3.2	µs
t_{ACQ}	Acquistion Time				0.8	µs
t_{C1}	Cycle Time of CLK		200			ns
t_{W1}	Pulse Width CLK HIGH Time or LOW Time.		60			ns
t_{D1}(5)	Delay Time of Rising Edge of Clock After Falling Edge of $\overline{HOLD}$ (A,B,C)		10			ns
t_{W2}	Pulse Width of $\overline{HOLDX}$ HIGH Time to be Recognized again	BV_{DD} = 5V	15			ns
		BV_{DD} = 3V	30			ns
t_{W3}	Pulse Width of $\overline{HOLDX}$ LOW Time	BV_{DD} = 5V	20			ns
		BV_{DD} = 3V	30			ns
t_{W4}	Pulse Width of $\overline{RESET}$	BV_{DD} = 5V	20			ns
		BV_{DD} = 3V	40			ns
t_{W5}	Pulse Width of $\overline{RD}$ HIGH Time	BV_{DD} = 5V	30			ns
		BV_{DD} = 3V	40			ns
t_{D2}	Delay Time of First Hold After $\overline{RESET}$	BV_{DD} = 5V	20			ns
		BV_{DD} = 3V	40			ns
t_{D4}	Delay Time of Falling Edge of $\overline{RD}$ After Falling Edge of $\overline{CS}$		0			ns
t_{D5}	Delay Time of Rising Edge of $\overline{CS}$ After Rising Edge of $\overline{RD}$		0			ns
t_{W6}	Pulse Width of $\overline{RD}$ and $\overline{CS}$ Both LOW Time	BV_{DD} = 5V	50			ns
		BV_{DD} = 3V	70			ns
t_{W7}	Pulse Width of $\overline{RD}$ HIGH Time	BV_{DD} = 5V	20			ns
		BV_{DD} = 3V	40			ns
t_{D6}	Delay Time of Data Valid After Falling Edge $\overline{RD}$	BV_{DD} = 5V	40			ns
		BV_{DD} = 3V	60			ns
t_{D7}	Delay Time of Data Hold From Rising Edge of $\overline{RD}$	BV_{DD} = 5V	5			ns
		BV_{DD} = 3V	10			ns
t_{D8}	Delay Time of $\overline{RD}$ HIGH After $\overline{CS}$ LOW	BV_{DD} = 5V	50			ns
		BV_{DD} = 3V	60			ns
t_{D9}	Delay Time of $\overline{RD}$ Low After Address Setup	BV_{DD} = 5V	10			ns
		BV_{DD} = 3V	20			ns

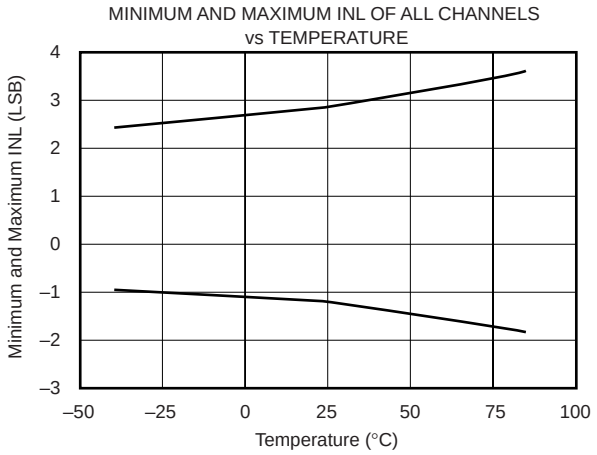
NOTES: (1) Assured by design. (2) All input signals are specified with tr = tf = 5ns (10% to 90% of BV_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. (3) See timing diagram above. (4) BYTE is asynchronous; when BYTE is 0, bits 15 through 0 appear at DB15-DB0. When BYTE is 1, bits 15 through 8 appear on DB7-DB0. $\overline{RD}$ may remain LOW between changes in BYTE. (5) Only important when synchronization to clock is important.

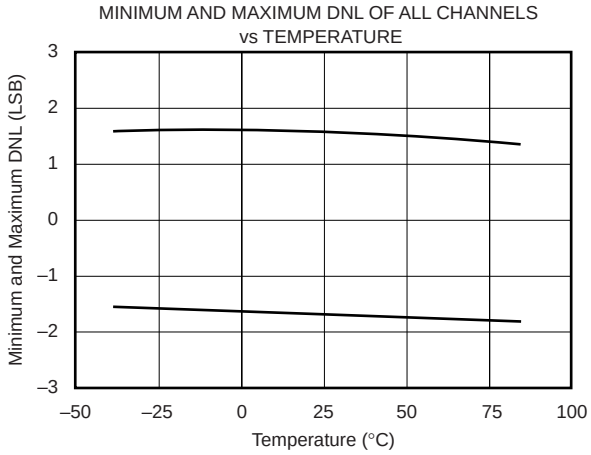
TYPICAL CHARACTERISTICS

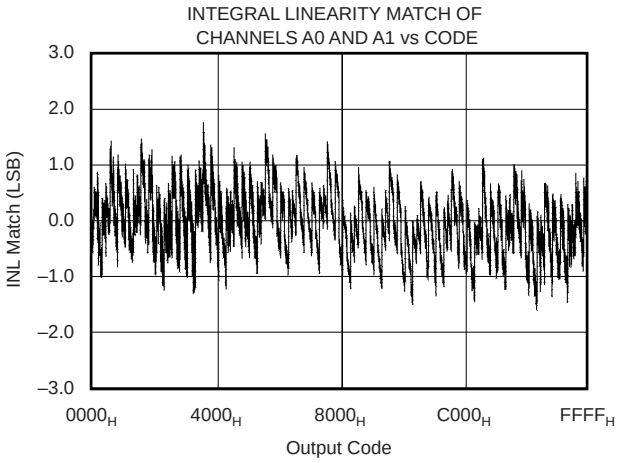
At T_A = +25°C, AV_{DD} = DV_{DD} = +5V, BV_{DD} = 3V V_{REF} = internal +2.5V and f_{CLK} = 5MHz, f_{SAMPLE} = 250kSPS, unless otherwise noted.

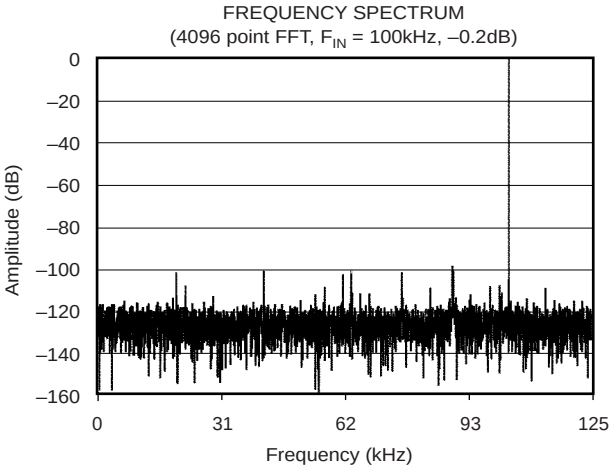






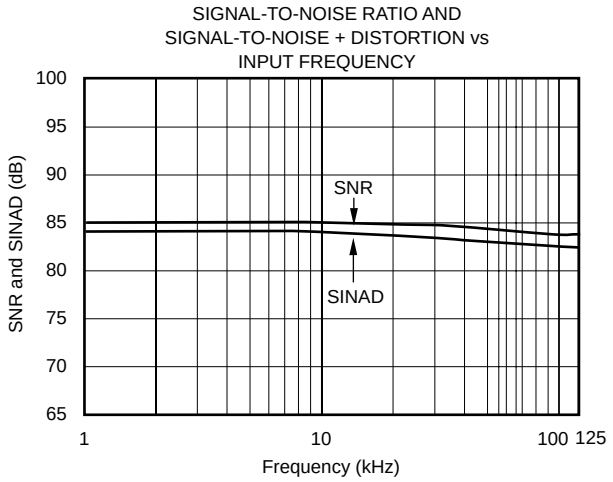


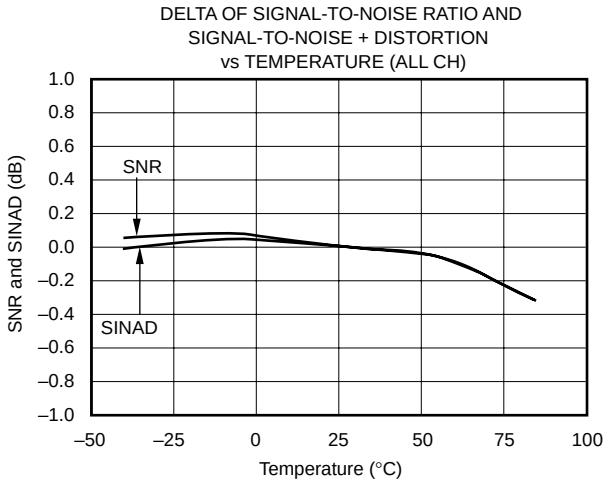


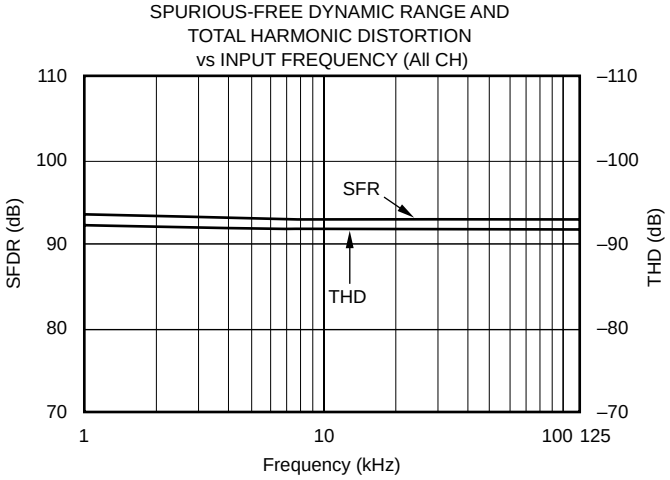


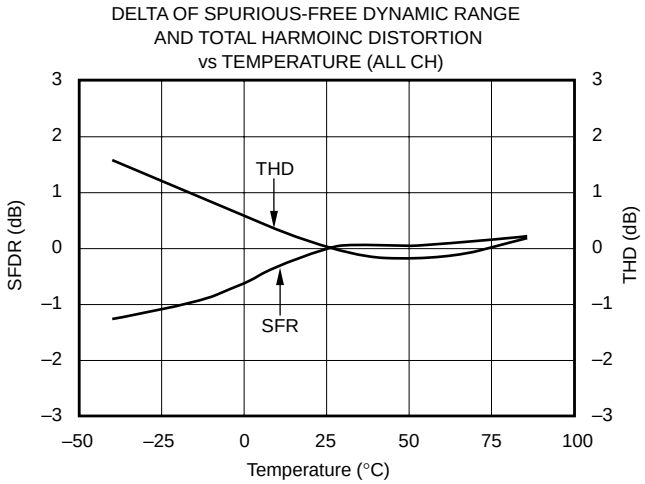
TYPICAL CHARACTERISTICS (Cont.)

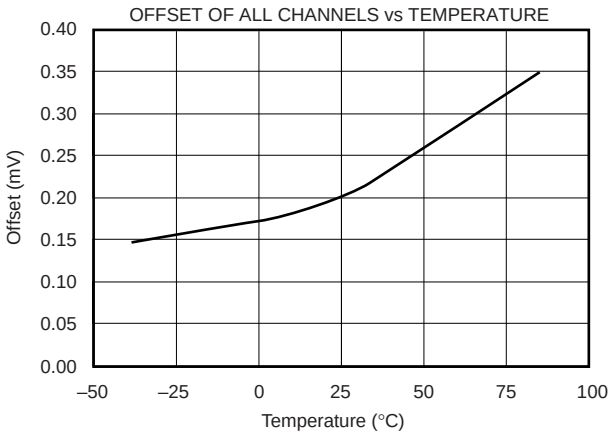
At T_A = +25°C, AV_{DD} = DV_{DD} = +5V, BV_{DD} = 3V V_{REF} = internal +2.5V and f_{CLK} = 5MHz, f_{SAMPLE} = 250kSPS, unless otherwise noted.

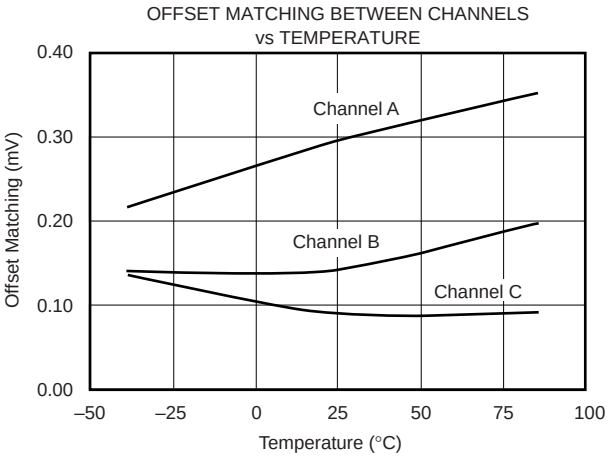






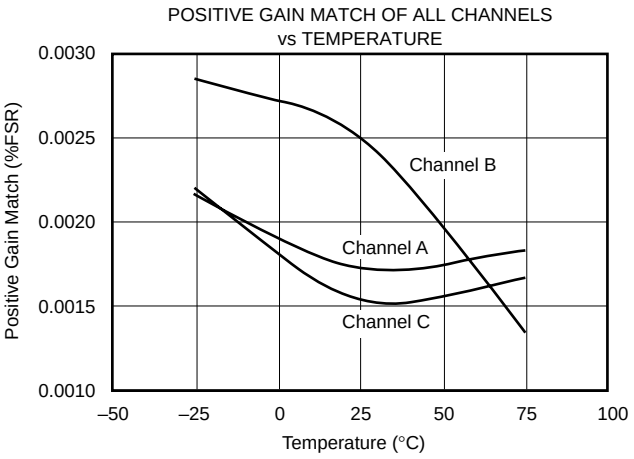


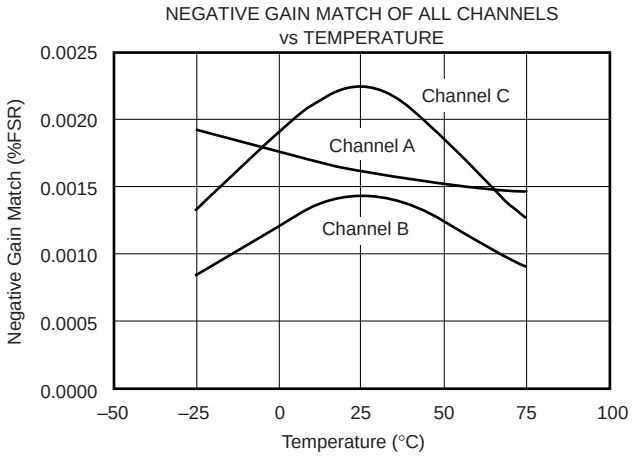


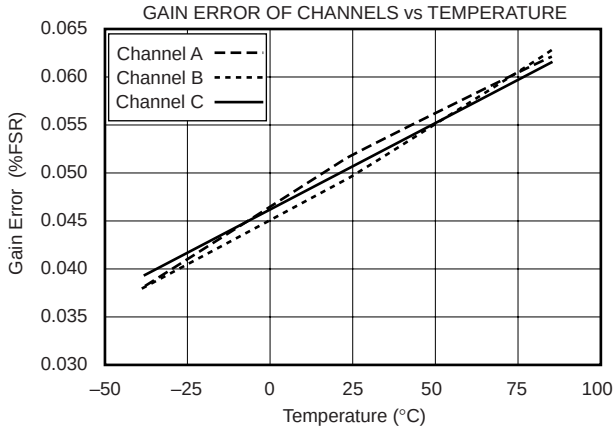


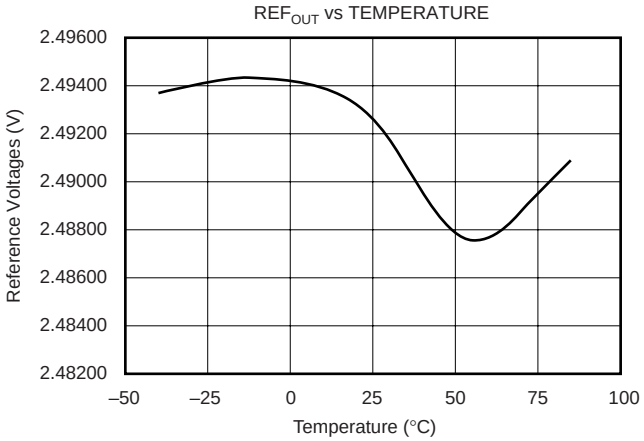
TYPICAL CHARACTERISTICS (Cont.)

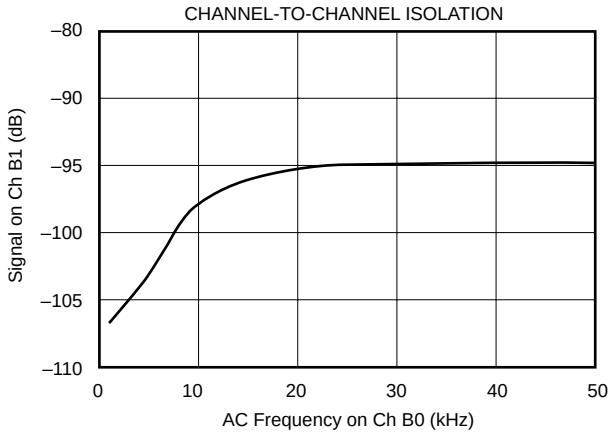
At T_A = +25°C, AV_{DD} = DV_{DD} = +5V, BV_{DD} = 3V V_{REF} = internal +2.5V and f_{CLK} = 5MHz, f_{SAMPLE} = 250kSPS, unless otherwise noted.

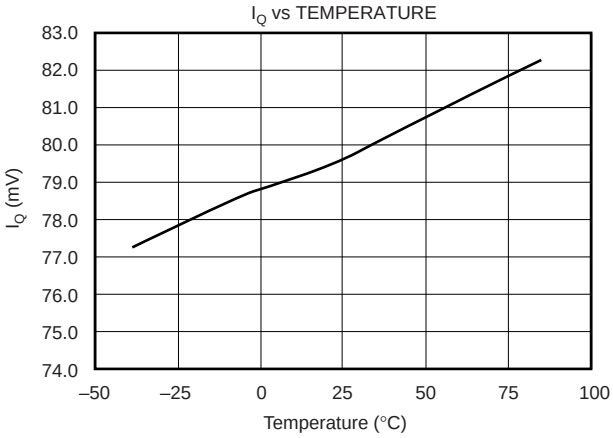












INTRODUCTION

The ADS8364 is a high-speed, low-power, 6-channel simultaneous sampling and converting, 16-bit ADC that operates from a single +5V supply. The input channels are fully differential with a typical common-mode rejection of 80dB. The part contains six 4µs successive approximation ADCs, six differential sample-and-hold amplifiers, an internal +2.5V reference with REF_{IN} and REF_{OUT} pins and a high-speed parallel interface. There are six analog inputs that are grouped into three channel pairs (A, B, and C). There are six ADCs, one for each input that can be sampled and converted simultaneously, thus preserving the relative phase information of the signals on both analog inputs. Each pair of channels has a hold signal ($\overline{HOLDA}$, $\overline{HOLDB}$, and $\overline{HOLDC}$) to allow simultaneous sampling on each channel pair, on four or on all six channels. The part accepts a differential analog input voltage in the range of $-V_{REF}$ to $+V_{REF}$, centered on the common-mode voltage (see the Analog Input Section). The part will also accept bipolar input ranges when a level shift circuit is used at the front end (see Figure 6).

A conversion is initiated on the ADS8364 by bringing the $\overline{HOLDX}$ pin LOW for a minimum of 20ns. $\overline{HOLDX}$ LOW places the sample-and-hold amplifiers of the X channels in the hold state simultaneously and the conversion process is started on each channel. The $\overline{EOC}$ output will go LOW for half a clock cycle when the conversion is latched into the output register. The data can be read from the parallel output bus following the conversion by bringing both $\overline{RD}$ and $\overline{CS}$ LOW.

Conversion time for the ADS8364 is 3.2µs when a 5MHz external clock is used. The corresponding acquisition time is 0.8µs. To achieve the maximum output data rate (250kSPS), the read function can be performed during the next conversion. Note: This mode of operation is described in more detail in the Timing and Control section of this data sheet.

SAMPLE-AND-HOLD SECTION

The sample-and-hold amplifiers on the ADS8364 allow the ADCs to accurately convert an input sine wave of full-scale amplitude to 16-bit resolution. The input bandwidth of the sample-and-hold is greater than the Nyquist rate (Nyquist equals one-half of the sampling rate) of the ADC even when the ADC is operated at its maximum throughput rate of 250kSPS. The typical small-signal bandwidth of the sample-and-hold amplifiers is 300MHz.

Typical aperture delay time or the time it takes for the ADS8364 to switch from the sample to the hold mode following the negative edge of $\overline{HOLDX}$ signal is 5ns. The average delta of repeated aperture delay values is typically 50ps (also known as aperture jitter). These specifications reflect the ability of the ADS8364 to capture AC input signals accurately at the exact same moment in time.

REFERENCE

Under normal operation, the REF_{OUT} (pin 61) can directly be connected to the REF_{IN} pin (pin 62) to provide an internal +2.5V reference to the ADS8364. The ADS8364 can operate, however, with an external reference in the range of 1.5V to 2.6V, for a corresponding full-scale range of 3.0V to 5.2V, as long as the input does not exceed the AV_{DD} + 0.3V value.

The reference of the ADS8364 is double-buffered. If the internal reference is used to drive an external load, a buffer is provided between the reference and the load applied to pin 61 (the internal reference can typically source 10µA of current—load capacitance should be 0.1µF and 10µF to minimize noise). If an external reference is used, the three-second buffers provide isolation between the external reference and the CDACs. These buffers are also used to recharge all of the capacitors of all CDACs during conversion.

ANALOG INPUT

The analog input is bipolar and fully differential. There are two general methods of driving the analog input of the ADS8364: single-ended or differential, as shown in Figure 1 and Figure 2. When the input is single-ended, the –IN input is held at the common-mode voltage. The +IN input swings around the same common voltage and the peak-to-peak amplitude is the (common-mode + V_{REF}) and the (common-mode – V_{REF}). The value of V_{REF} determines the range over which the common-mode voltage may vary (see Figure 3).

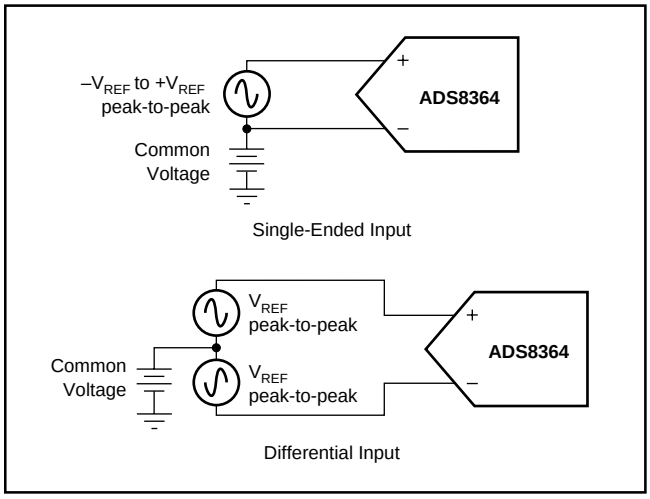
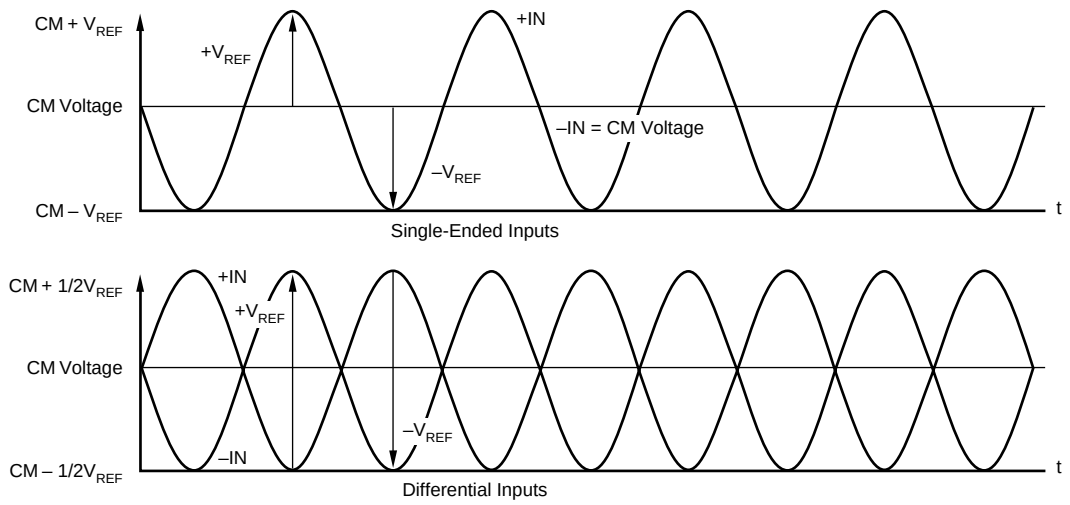


FIGURE 1. Methods of Driving the ADS8364 Single-Ended or Differential.



NOTES: Common-Mode Voltage (Differential Mode) = $\frac{(+IN) + (-IN)}{2}$, Common-Mode Voltage (Single-Ended Mode) = IN–.

The maximum differential voltage between +IN and –IN of the ADS8364 is V_{REF}. See Figures 3 and 4 for a further explanation of the common voltage range for single-ended and differential inputs.

FIGURE 2. Using the ADS8364 in the Single-Ended and Differential Input Modes.

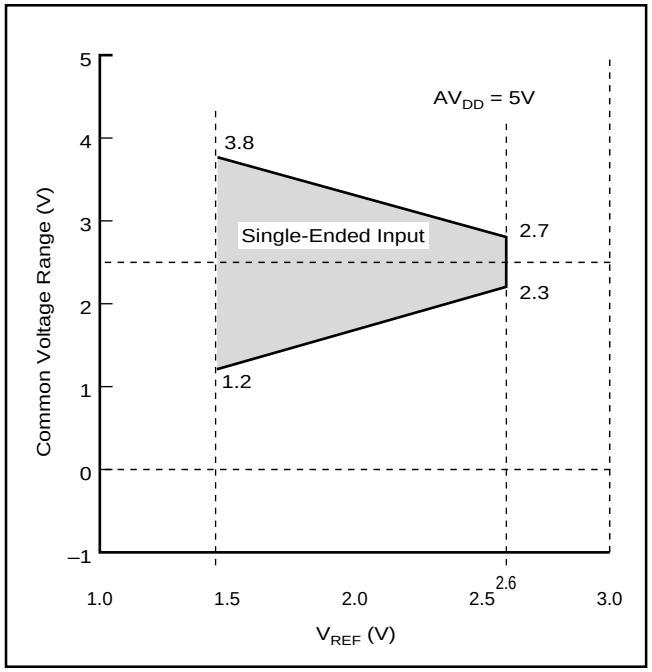


FIGURE 3. Single-Ended Input: Common-Mode Voltage Range vs V_{REF}.

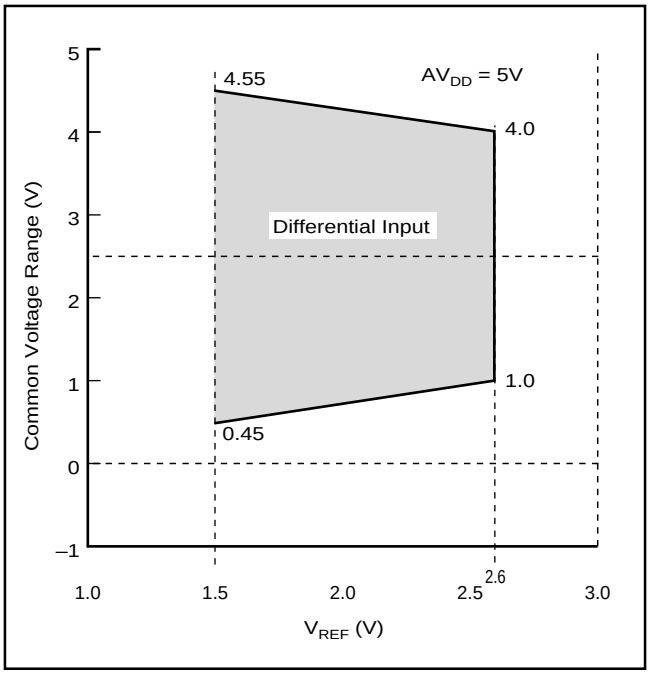


FIGURE 4. Differential Input: Common-Mode Voltage Range vs V_{REF}.

When the input is differential, the amplitude of the input is the difference between the +IN and –IN input, or: (+IN) – (–IN). The peak-to-peak amplitude of each input is $\pm 1/2V_{REF}$ around this common voltage. However, since the inputs are 180° out-of-phase, the peak-to-peak amplitude of the differential voltage is $+V_{REF}$ to $-V_{REF}$. The value of V_{REF} also determines the range of the voltage that may be common to both inputs, as shown in Figure 4.

In each case, care should be taken to ensure that the output impedance of the sources driving the +IN and –IN inputs are matched. Often, a small capacitor (20pF) between the positive and negative input helps to match their impedance. Otherwise, this may result in offset error, which will change with both temperature and input voltage.

The input current on the analog inputs depends on a number of factors as sample rate or input voltage. Essentially, the

current into the ADS8364 charges the internal capacitor array during the sampling period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (25pF) to a 16-bit settling level within 3 clock cycles if the minimum acquisition time is used. When the converter goes into the hold mode, the input impedance is greater than 1GΩ.

Care must be taken regarding the absolute analog input voltage. The +IN and –IN inputs should always remain within the range of AGND – 0.3V to AV_{DD} + 0.3V.

TRANSITION NOISE

The transition noise of the ADS8364 itself is low, as shown in Figure 5. These histograms were generated by applying a low-noise DC input and initiating 8000 conversions. The digital output of the ADC will vary in output code due to the internal noise of the ADS8364. This is true for all 16-bit, SAR-type ADCs. Using a histogram to plot the output codes, the distribution should appear bell-shaped with the peak of the bell curve representing the nominal code for the input value. The ±1σ, ±2σ, and ±3σ distributions will represent the 68.3%, 95.5%, and 99.7%, respectively, of all codes. The transition noise can be calculated by dividing the number of codes measured by 6 and this will yield the ±3σ distribution, or 99.7%, of all codes. Statistically, up to three codes could fall outside the distribution when executing 1000 conversions. Remember, to achieve this low-noise performance, the peak-to-peak noise of the input signal and reference must be < 50µV.

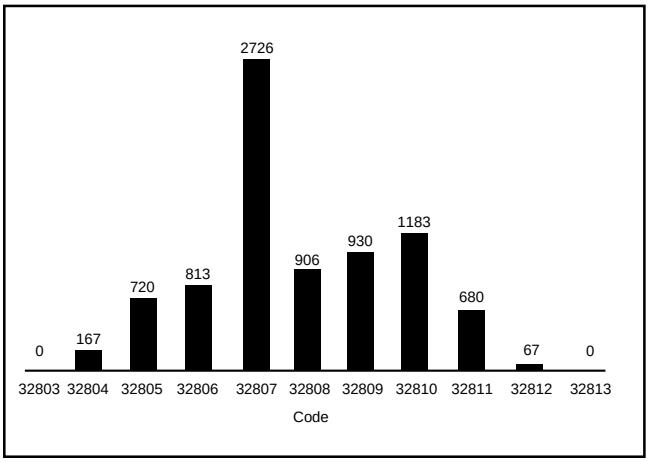
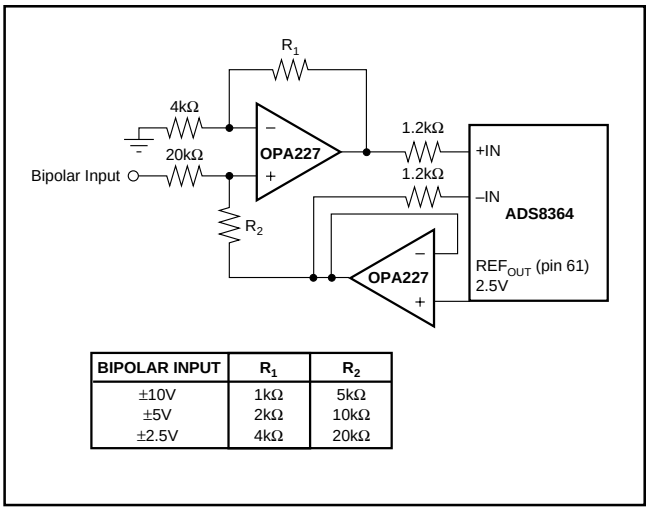


FIGURE 5. 8000 Conversion Histogram of a DC Input.

BIPOLAR INPUTS

The differential inputs of the ADS8364 were designed to accept bipolar inputs ($-V_{REF}$ and $+V_{REF}$) around the common-mode voltage (2.5V), which corresponds to a 0V to 5V input range with a 2.5V reference. By using a simple op amp circuit featuring four, high-precision external resistors, the ADS8364 can be configured to accept bipolar inputs. The conventional ±2.5V, ±5V, and ±10V input ranges could be interfaced to the ADS8364 using the resistor values shown in Figure 6.



BIPOLAR INPUT	R_1	R_2
±10V	1kΩ	5kΩ
±5V	2kΩ	10kΩ
±2.5V	4kΩ	20kΩ

FIGURE 6. Level Shift Circuit for Bipolar Input Ranges.

TIMING AND CONTROL

The ADS8364 uses an external clock (CLK, pin 28) which controls the conversion rate of the CDAC. With a 5MHz external clock, the ADC sampling rate is 250kSPS which corresponds to a 4µs maximum throughput time. Acquistion and conversion takes a total of 20 clock cycles.

THEORY OF OPERATION

The ADS8364 contains six 16-bit ADCs that can operate simultaneously in pairs. The three hold signals ($\overline{HOLDA}$, $\overline{HOLDB}$, and $\overline{HOLDC}$) initiate the conversion on the specific channels. A simultaneous hold on all six channels can occur with all three hold signals strobe together. The converted values are saved in six registers. For each read operation, the ADS8364 outputs 16 bits of information (16 Data or 3 Channel Address, Data Valid, and some synchronization information). The Address/Mode signals (A0, A1, and A2) select how the data is read from the ADS8364. These Address/Mode signals can define a selection of a single channel, a cycle mode that cycles through all channels, or a FIFO mode that sequences the data determined by the order of the hold signals. The FIFO mode will allow the six registers to be used by a single-channel pair and, therefore, three locations for CH X0 and three locations for CH X1 can be updated before they are read from the part.

EXPLANATION OF CLOCK, $\overline{RESET}$, FD, AND $\overline{EOC}$ PINS

Clock—An external clock has to be provided for the ADS8364. The maximum clock frequency is 5MHz. The minimum clock cycle is 200ns (Timing Diagram, t_{C1}), and the clock has to remain HIGH (Timing Diagram, t_{W1}) or LOW for at least 60ns.

$\overline{RESET}$—Bringing reset signal LOW will reset the ADS8364. It will clear all the output registers, stop any actual conversions, and will close the sampling switches. The reset signal has to stay LOW for at least 20ns (see Figure 7, t_{W4}). The reset signal should be back HIGH for at least 20ns (see Figure 7, t_{D2}), before starting the next conversion (negative hold edge).

$\overline{EOC}$—End of conversion goes low when new data of the internal ADC is latched into the output registers, which usually happens 16.5 clock cycles after hold initiated the conversion. It remains low for half a clock cycle. If more than one channel pair is converted simultaneously, the A-channels get stored to the registers first (16.5 clock cycles after hold), followed by the B-channels one clock cycle later, and finally the C-channels at another clock cycle later. If a reading ($\overline{RD}$ and $\overline{CS}$ are LOW) is in process, then the latch process is delayed until the read operation is finished.

FD—First data or A0 data is HIGH if channel A0 is chosen to be read next. In the FIFO mode whatever channel X0 is written to the FIFO first is latched into the A0 register. So, for example, when the FIFO is empty, FD is 0. Then the first result is latched into the FIFO register A0 is, therefore, chosen to be read next, and FD rises. After the first channel is read (1-3 read cycles depending on BYTE and ADD) FD goes LOW again.

START OF A CONVERSION AND READING DATA

By bringing one, two, or all of the $\overline{HOLDX}$ signals LOW, the input data of the corresponding channel X is immediately placed in the hold mode (5ns). The conversion of this channel X follows with the next rising edge of clock. If it is important to detect a hold command during a certain clock-cycle, then the falling edge of the hold signal has to occur at least 10ns before the rising edge of clock, as shown in Figure 7, t_{D1}. The hold signal can remain LOW without initiating a new conversion. The hold signal has to be HIGH for at least 15ns (as shown in Figure 7, t_{W2}) before it is brought LOW again and hold has to stay LOW for at least 20ns (Figure 7, t_{W3}).

Once a particular hold signal goes low, further impulses of this hold signal are ignored until the conversion is finished or the part is reset. When the conversion is finished (after 16 clock cycles) the sampling switches will close and sample the selected channel. The start of the next conversion must be delayed to allow the input capacitor of the ADS8364 to be fully charged. This delay time depends on the driving amplifier, but should be at least 800ns.

The ADS8364 can also convert one channel continuously (see Figure 8). Therefore, $\overline{HOLDA}$ and $\overline{HOLDC}$ are kept HIGH all the time. To gain acquisition time, the falling edge of $\overline{HOLDB}$ takes place just before the rising edge of clock. One conversion requires 20 clock cycles. Here, data is read after the next conversion is initiated by $\overline{HOLDB}$. To read data from channel B, A1 is set HIGH and A2 is LOW. As A0 is LOW during the first reading (A2 A1 A0 = 010) data B0 is put to the output. Before the second $\overline{RD}$, A0 switches HIGH (A2 A1 A0 = 011) so data from channel B1 is read, as shown in Table II. However, reading data during the conversion or on a falling hold edge might cause a loss in performance.

A2	A1	A0	CHANNEL TO BE READ
0	0	0	CHA0
0	0	1	CHA1
0	1	0	CHB0
0	1	1	CHB1
1	0	0	CHC0
1	0	1	CHC1
1	1	0	Cycle mode reads registers CHA0 through CHC1 on successive transitions of the read line.
1	1	1	FIFO Mode

TABLE II. Address Control for $\overline{RD}$ Functions.

Reading data ($\overline{RD}$, $\overline{CS}$)—In general, the channel/data outputs are in tri-state. Both $\overline{CS}$ and $\overline{RD}$ have to be LOW to enable these outputs. $\overline{RD}$ and $\overline{CS}$ have to stay LOW together for at least 40ns (see Timing Characteristics, t_{D6}) before the output data is valid. $\overline{RD}$ has to remain HIGH for at least 30ns (see Timing Diagram, t_{W5}) before bringing it back LOW for a subsequent read command.

16.5 clock-cycles after the start of a conversion (next rising edge of clock after the falling edge of $\overline{HOLDX}$), the new data is latched into its output register. Even if the ADS8364 is forced to wait until the read process is finished ($\overline{RD}$ signal going HIGH) before the new data gets latched into its output

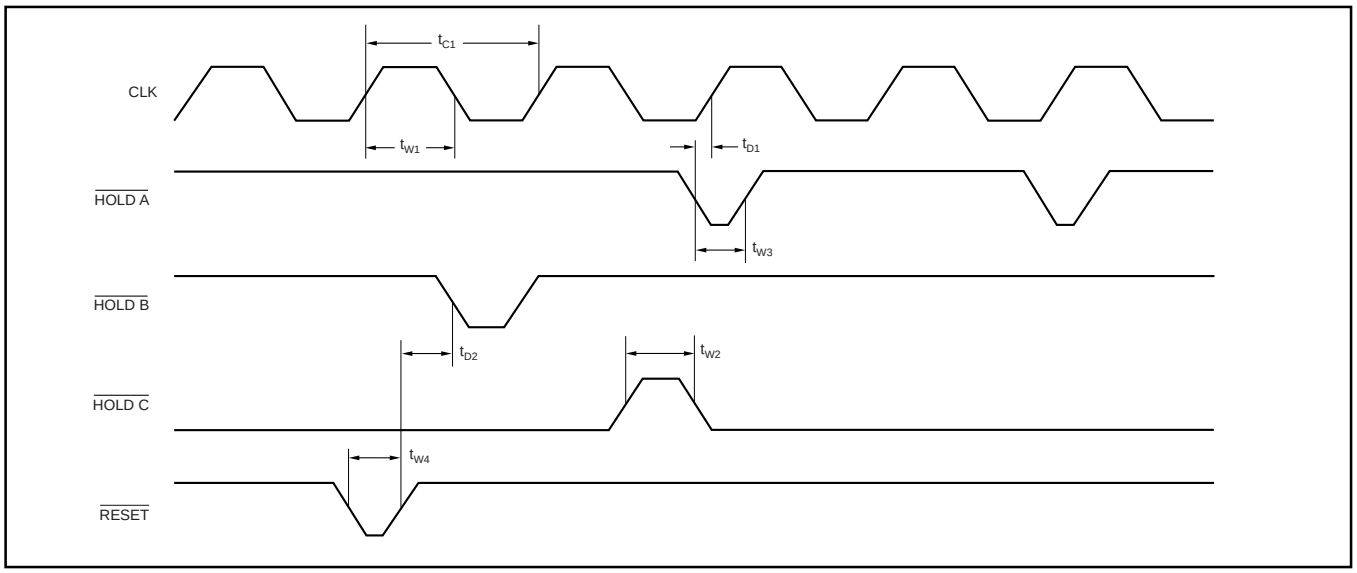


FIGURE 7. Start of the Conversion.

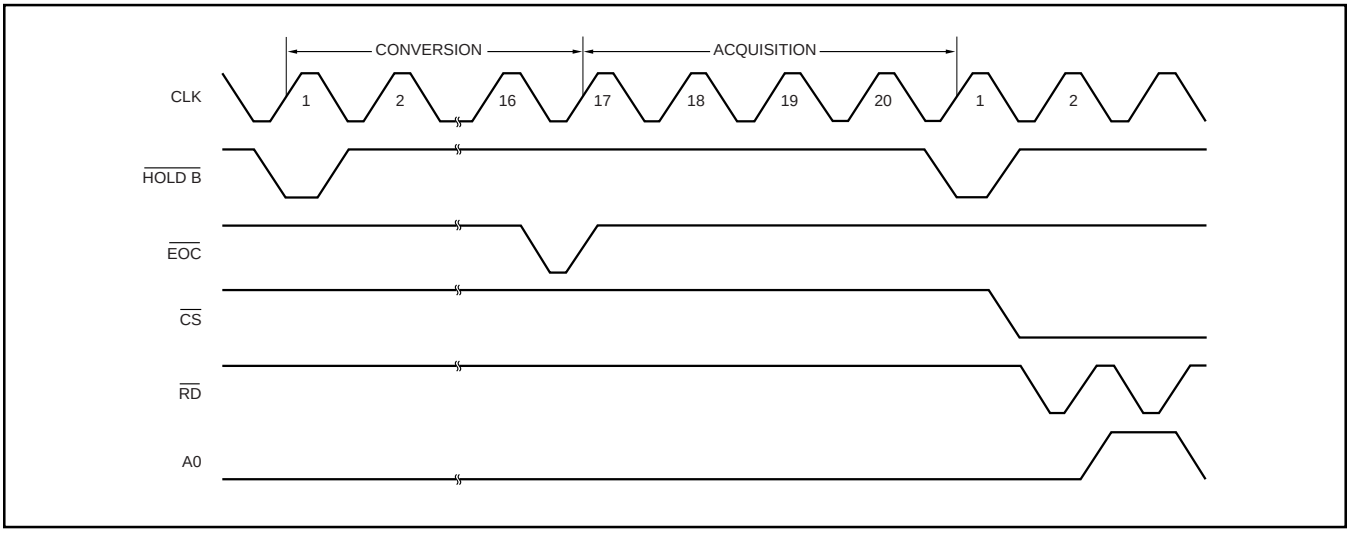


FIGURE 8. Timing of one Conversion Cycle.

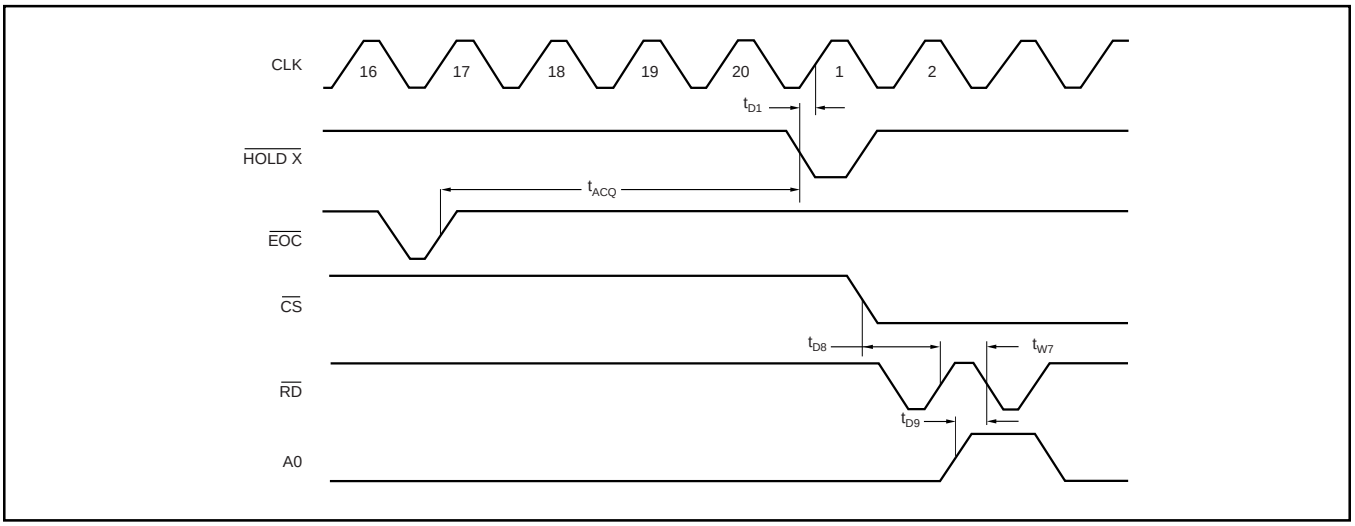


FIGURE 9. Timing for Reading Data.

register, the possibility still exists that the new data was latched to the output register just before the falling edge of $\overline{RD}$. If a read process is initiated around 16.5 clock cycles after the conversion started, $\overline{RD}$ and $\overline{CS}$ should stay LOW for at least 50ns (see Timing Diagram, t_{W6}) to get the new data stored to its register and switched to the output.

$\overline{CS}$ being LOW tells the ADS8364 that the bus on the board is assigned to the ADS8364. If an ADC shares a bus with digital gates, there is a possibility that digital (high-frequency) noise will be coupled into the ADC. If the bus is just used by the ADS8364, $\overline{CS}$ can be hardwired to ground. Reading data at the falling edge of one of the $\overline{HOLDX}$ signals might cause noise.

BYTE—If there is only an 8-bit bus available on a board, then BYTE can be set HIGH. (see Figure 11) In this case, the lower 8 bits can be read at the output pins D15 to D8 or D7 to D0 at the first $\overline{RD}$ signal and the higher bits after the second $\overline{RD}$ signal. If the ADS8364 is used in the cycle or the FIFO mode, then the address and a data valid information is added to the data if ADD is HIGH. In this case, the address will be read first, then the lower 8 bits, and finally the higher 8 bits.

If BYTE is LOW, then the ADS8364 operates in the 16-bit output mode. Here, data is read between the pins DB15 and DB0. As long as ADD is LOW, with every $\overline{RD}$-impulse, data from a new channel is brought to the output. If ADD is HIGH, and the cycle or the FIFO mode is chosen; the first output word will contain the address, while the second output word contains the 16-bit data.

ADD-Signal–In the cycle and the FIFO mode, it might be desirable to have address information with the 16-bit output data. Therefore, ADD can be set HIGH. In this case, two (or three readings if the part is operated with byte being HIGH) $\overline{RD}$-signals are necessary to read data of one channel, while the ADS8364 provides channel information on the first $\overline{RD}$ signal (see Table III and Table IV).

The signals ADD, A0, A1, A2, $\overline{RESET}$, $\overline{HOLDA}$, $\overline{HOLDB}$, and $\overline{HOLDC}$ are accessible through the data bus and control word. All these pins are in OR configuration with hardware pins. When software configuration is used, the corresponding pins must be connected to ground or the power supply. When the MSB is HIGH, the device is in the configuration mode. MSB LOW will start conversion or reset the part.

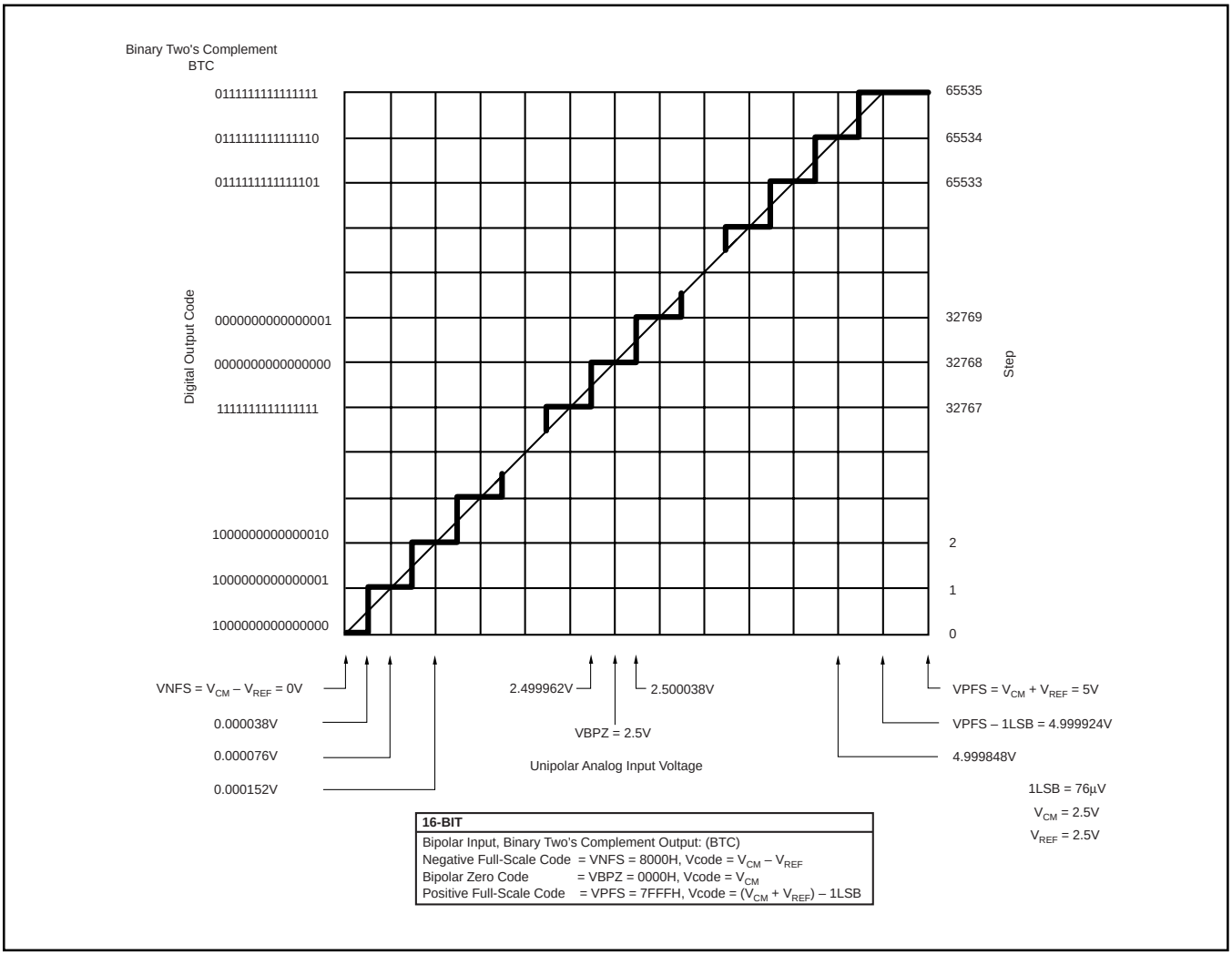


FIGURE 10. Ideal Conversion Characteristics (Condition: Single-Ended, VCM = chXX– = 2.5V, V_{REF} = 2.5V)

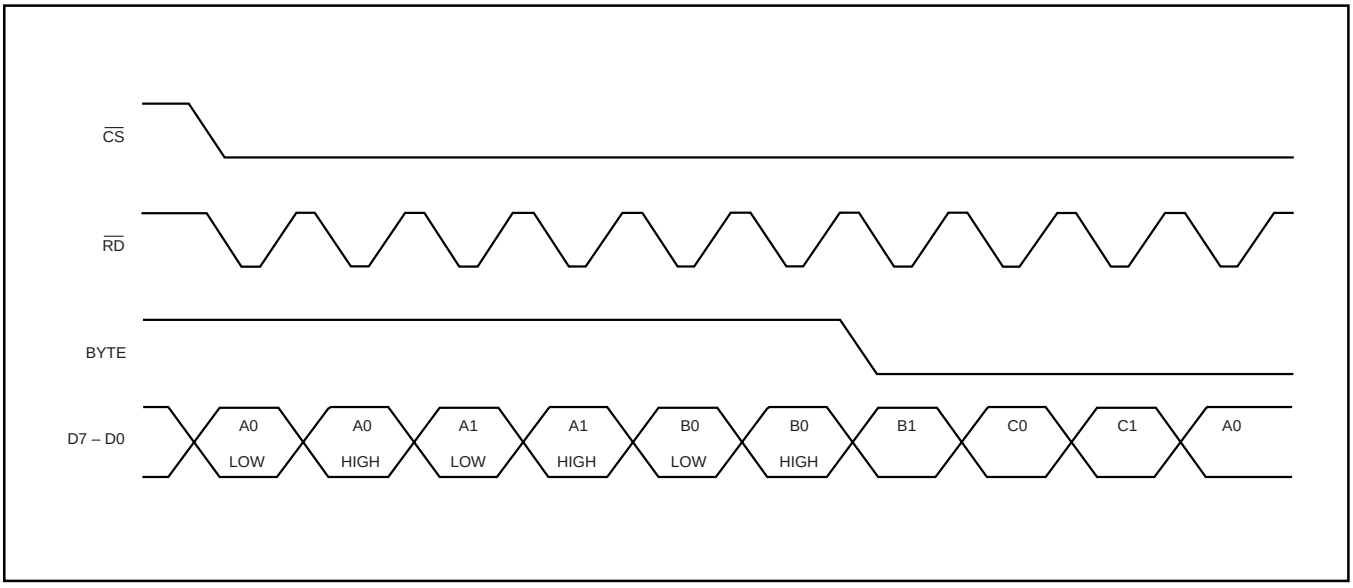


FIGURE 11. Reading Data in Cycling Mode.

ADD = 0	BYTE = 0		BYTE = 1		
A2 A1 A0	1st RD	2nd RD	1st RD	2nd RD	3rd RD
000	db15...db0	no 2nd RD	db7...db0	db15...db8	no 3rd RD
001	db15...db0	no 2nd RD	db7...db0	db15...db8	no 3rd RD
010	db15...db0	no 2nd RD	db7...db0	db15...db8	no 3rd RD
011	db15...db0	no 2nd RD	db7...db0	db15...db8	no 3rd RD
100	db15...db0	no 2nd RD	db7...db0	db15...db8	no 3rd RD
101	db15...db0	no 2nd RD	db7...db0	db15...db8	no 3rd RD
110	db15...db0	no 2nd RD	db7...db0	db15...db8	no 3rd RD
111	db15...db0	no 2nd RD	db7...db0	db15...db8	no 3rd RD

TABLE III. Overview of the Output Formats Depending on the Mode (Case ADD = 0).

The HOLD signals will start conversion automatically on the next clock cycle. The format of the two words that can be writing to ADS8364 are shown in Table V.

GETTING DATA

Flexible output modes: (**A0, A1, A2**)

The ADS8364 has three different output modes that are selected with A2, A1, and A0.

With (A2 A1 A0) = 000 to 101, a particular channel can directly be addressed (see Table II and Figure 9). The channel address should be set at least 10ns (see Figure 9, t_{D9}) before the falling edge of $\overline{RD}$ and should not change as long as $\overline{RD}$ is LOW. In this standard address mode, ADD will be ignored, but should be connected to either ground or supply.

With (A2 A1 A0) = 110, the interface is running in a cycle mode (see Figure 11). Here, data 7 down to 0 of channel A0 is read on the first $\overline{RD}$-signal and 15 down to 8 on the second as BYTE is HIGH. Then A1 on the second, followed by B0, B1, C0, and finally, C1 before reading A0 again. Data from channel A0 is brought to the output first after a reset-signal or after powering the part up. The third mode is a FIFO mode that is addressed with (A2 A1 A0 = 111). Data of the channel that is converted first will be read first. So, if a particular channel pair is most interesting and is converted more frequently (e.g., to get a history of a particular channel pair) then there are three output registers per channel available to store data.

If all the output registers are filled up with unread data and new data from an additional conversion has to get latched in, then the oldest data gets thrown away. If a read process is going on ($\overline{RD}$-signal LOW) and new data has to be stored, then the ADS8364 will wait until the read process is finished ($\overline{RD}$-signal going HIGH) before the new data gets latched into its output register. Again, with the ADD signal, it can be chosen if the address should be added to the output data.

New data is always written into the next available register. At t_0 (see Figure 12), the reset deletes all the existing data. At t_1, the new data of the channels A0 and A1 are put into registers 0 and 1. At t_2, the read process of channel A0 data is finished. Therefore, this data is dumped and A1 data is shifted to register 0. At t_3, new data is available, this time from channels B0, B1, C0 and C1. This data is written into the next available registers (registers 1, 2, 3, and 4).

On t_4, the new read process of channel A1 data is finished. The new data of channel C0 and C1 at t_5 is put on top (registers 4 and 5).

In Cycle mode and in FIFO mode, the ADS8364 offers the ability to add the address of the channel to the output data. As there is just a 16-bit bus available (or 8-bit bus in the case byte is HIGH), an additional ($\overline{RD}$-signal is necessary to get the information (see Table III and Table IV).

The Output Code (DB15…DB0)–In the standard address mode (A2 A1 A0 = 000…101), the ADS8364 has a 16-bit output word on pins DB15…DB0 if BYTE = 0. If BYTE = 1 then two $\overline{RD}$-impulses are necessary to first read the lower bits then the higher bits on either DB7…DB0 or DB15...DB8.

The address of the channel (a2a1a0) and a data valid (dv) bit is added to the data if the ADS8364 is operated in the cycle or in the FIFO-mode and ADD is set HIGH. If BYTE = 0, then the data valid and the address of the channel is active during the first ($\overline{RD}$-impulse (1000 0000 0000 dv a2 a1 a0). During the second ($\overline{RD}$, the 16-bit data word can be read (db15…db0). If BYTE = 1, then three ($\overline{RD}$-impulses are needed. On the first one, data valid, the three address bits and the data bits db3…db0 (dv, a2, a1, a0, db3, db2, db1, db0) are read, followed by the eight lower bits of the 16-bit data word

ADD = 1	BYTE = 0		BYTE = 1		
A2A1A0	1st RD	2nd RD	1st RD	2nd RD	3rd RD
000	db15...db0	no 2nd RD	db7...db0	db15...db8	no 3rd RD
001	db15...db0	no 2nd RD	db7...db0	db15...db8	no 3rd RD
010	db15...db0	no 2nd RD	db7...db0	db15...db8	no 3rd RD
011	db15...db0	no 2nd RD	db7...db0	db15...db8	no 3rd RD
100	db15...db0	no 2nd RD	db7...db0	db15...db8	no 3rd RD
101	db15...db0	no 2nd RD	db7...db0	db15...db8	no 3rd RD
110	1000 0000 0000 dv a2 a1 a0	db15...db0	dv a2 a1 a0 db3 db2 db0	db7...db0	db15...db8
111	1000 0000 0000 dv a2 a1 a0	db15...db0	dv a2 a1 a0 db3 db2 db0	db7...db0	db15...db8

TABLE IV. Overview Over the Output formats Depending on the Mode in Case ADD = 1

DB7 (MSB)	DB6	DB5	DB4	DB3	DB2	DB1	DB0 (LSB)
1	X	X	X	ADD	A2	A1	A0
0	X	X	X	RESET	HOLDA	HOLDB	HOLDC

TABLE V. Data Register Bits.

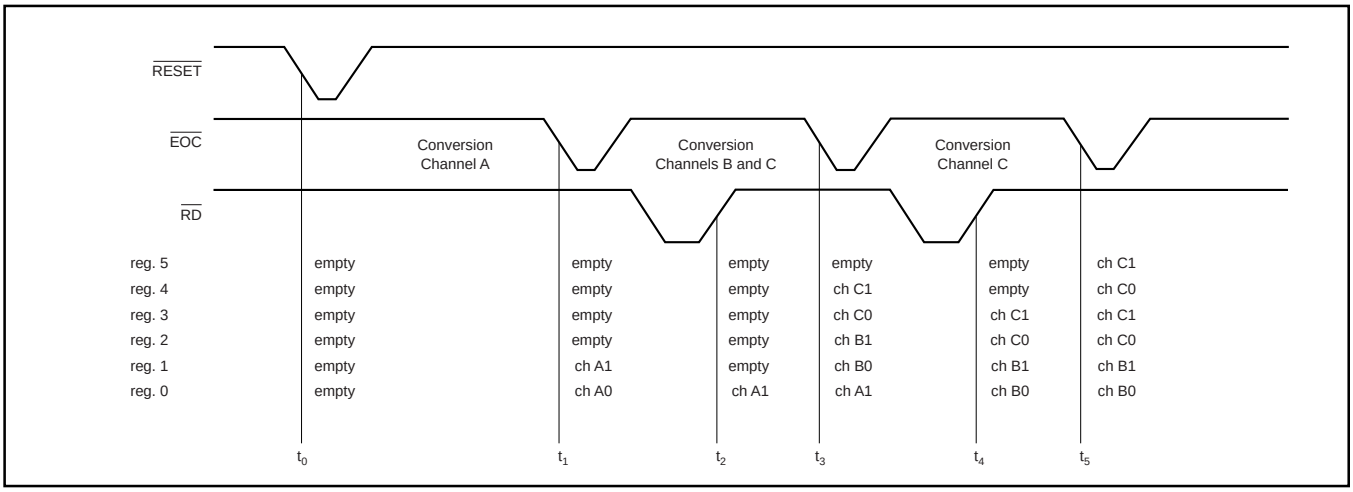


FIGURE 12. Functionality Diagram of FIFO Registers.

(db7…db0) and finally the higher eight data bits (db15…db8). 1000 0000 0000 is added before the address in case BYTE = 0 and db3…db0 after the address if BYTE = 1. This provides the possibility to check if the counting of the $\overline{RD}$ signals inside the ADS8364 are still tracking with the external interface (see Table III and Table IV).

The data valid bit is useful for the FIFO mode. Valid data can simply get read until dv turns 0. The three address bits are listed in Table VI. If the FIFO is empty, 16 zeroes are put to the output.

	a2	a1	a0
Data From Channel A0	0	0	0
Data From Channel A1	0	0	1
Data From Channel B0	0	1	0
Data From Channel B1	0	1	1
Data From Channel C0	1	0	0
Data From Channel C1	1	0	1

TABLE VI. Address Bit in the Output Data.

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS8364 circuitry. This is particularly true if the CLK input is approaching the maximum throughput rate.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Thus, driving any single conversion for an n-bit SAR converter, there are n *windows* in which large external transient voltages can affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, or high-power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. Their error can change if the external event changes in time with respect to the CLK input.

With this in mind, power to the ADS8364 should be clean and well-bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1µF to 10µF capacitor is recommended. If needed, an even larger capacitor and a 5Ω or 10Ω series resistor may be used to low-pass filter a noisy supply. On average, the ADS8364 draws very little current from an external reference as the reference voltage is internally buffered. A bypass capacitor of 0.1µF and 10µF are suggested when using the internal reference (tie pin 61 directly to pin 62).

GROUNDING

The AGND and DGND pins should be connected to a clean ground point. In all cases, this should be the analog ground. Avoid connections that are too close to the grounding point of a microcontroller or digital signal processor. If required, run a ground trace directly from the converter to the power-supply entry point. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry. Three signal ground pins, SGND, are the input signal grounds which are on the same potential as analog ground.

APPLICATION INFORMATION

In Figures 13 through 18, different connection diagrams to DSPs or micro-controllers are shown.

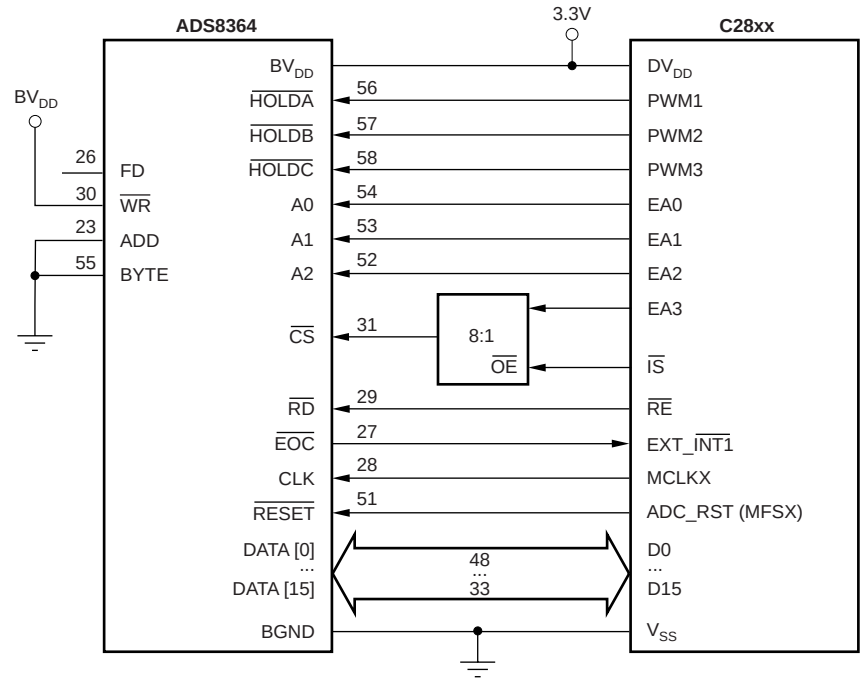


FIGURE 13. Typical C28xx Connection (Hardware Control).

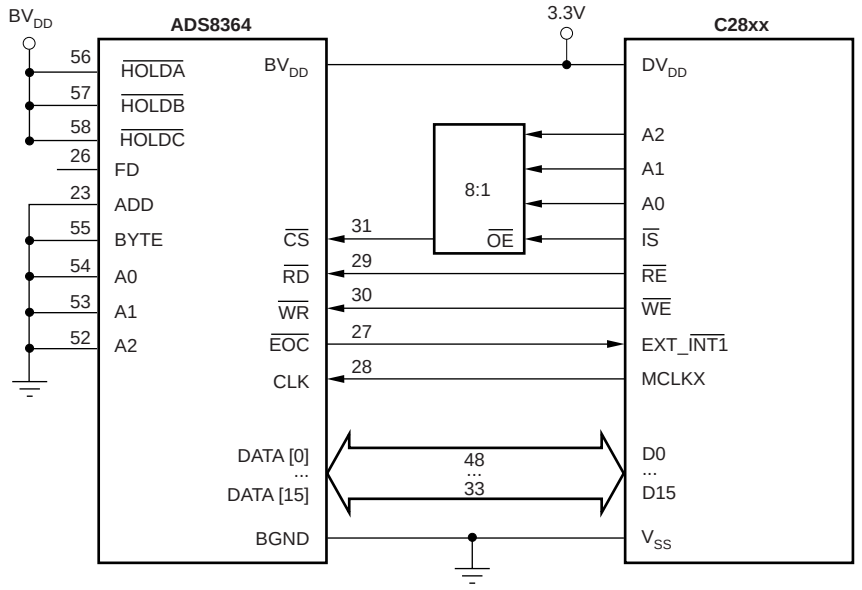


FIGURE 14. Typical C28xx Connection (Software Control).

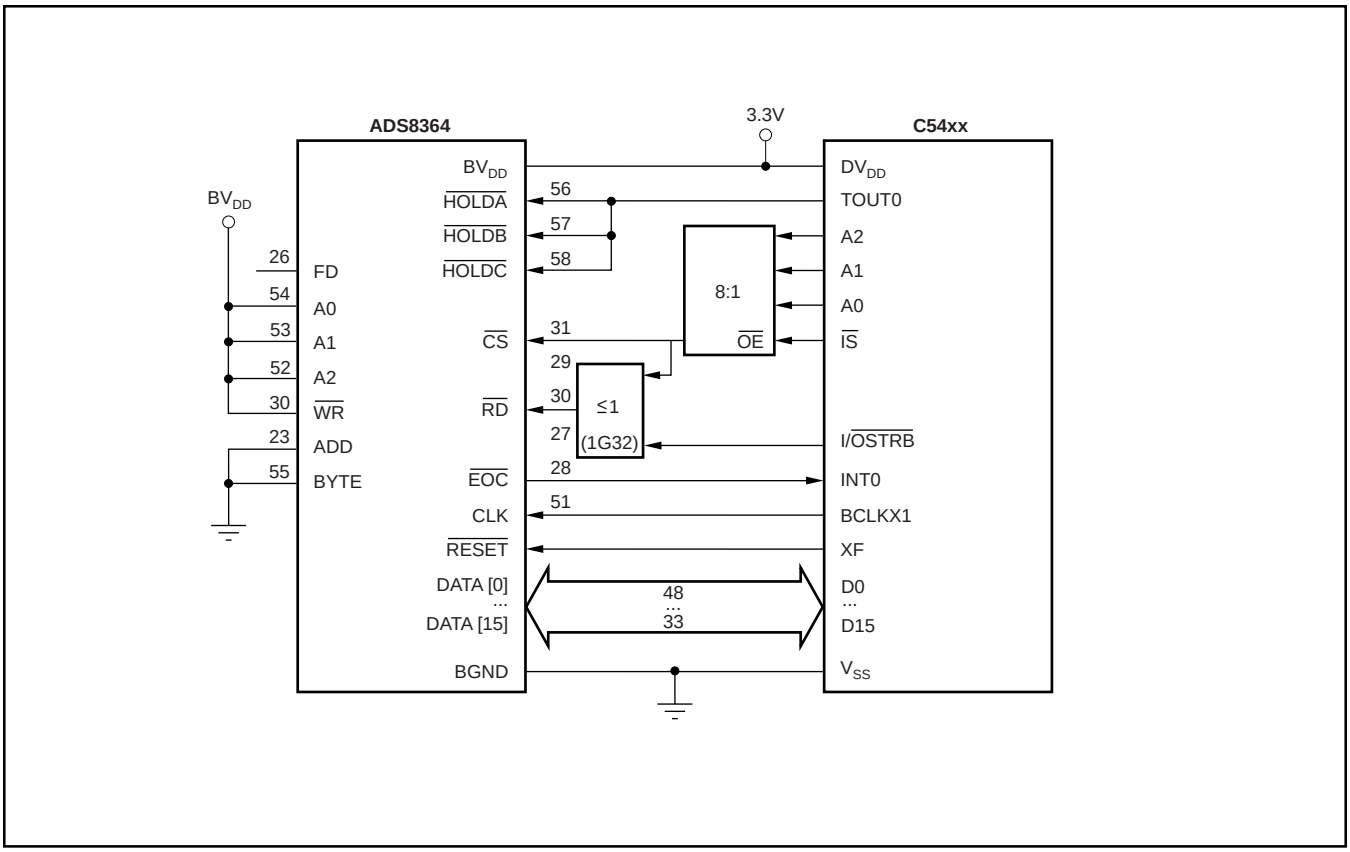


FIGURE 15. Typical C54xx Connection (FIFO with Hardware Control).

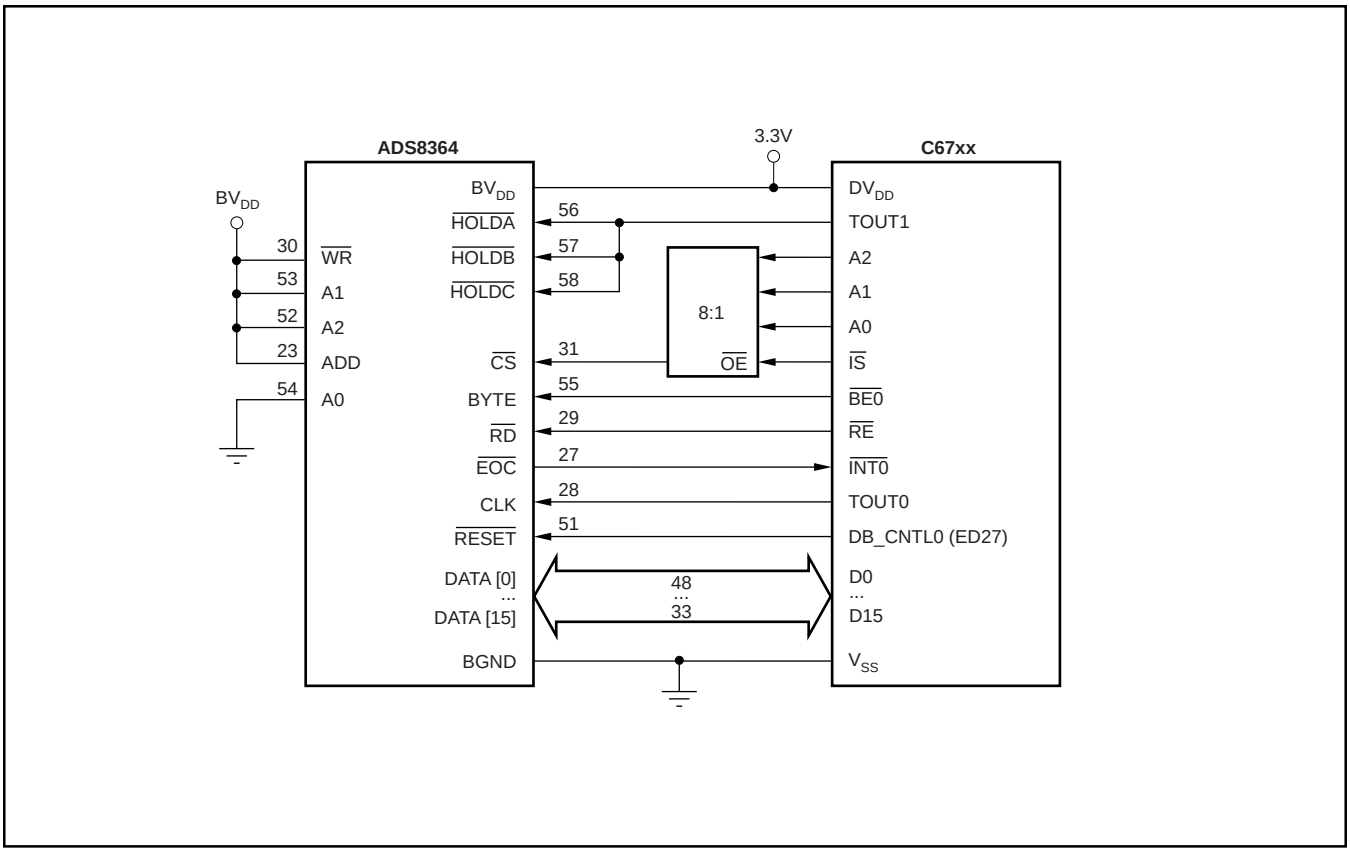


FIGURE 16. Typical C67xx Connection (Cycle Mode – Hardware Control).

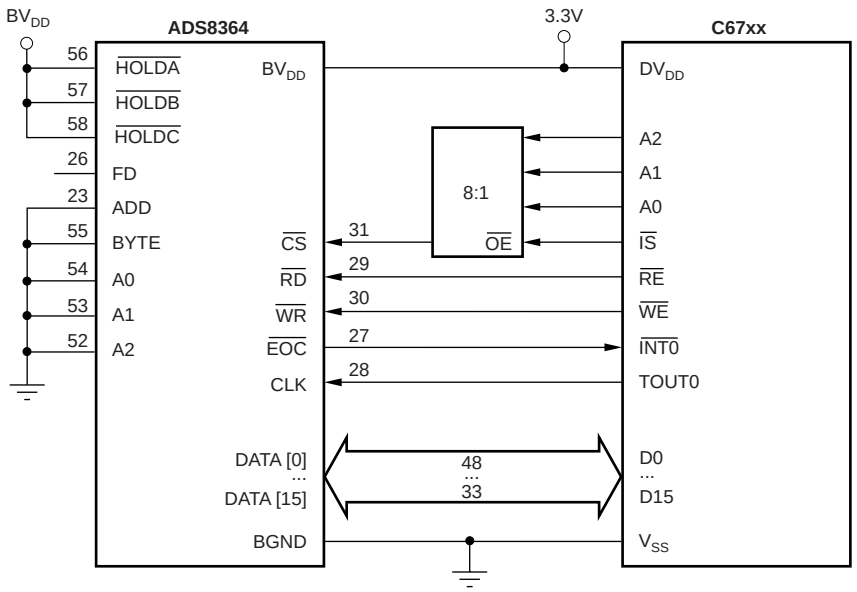


FIGURE 17. Typical C67xx Connection (Software Control).

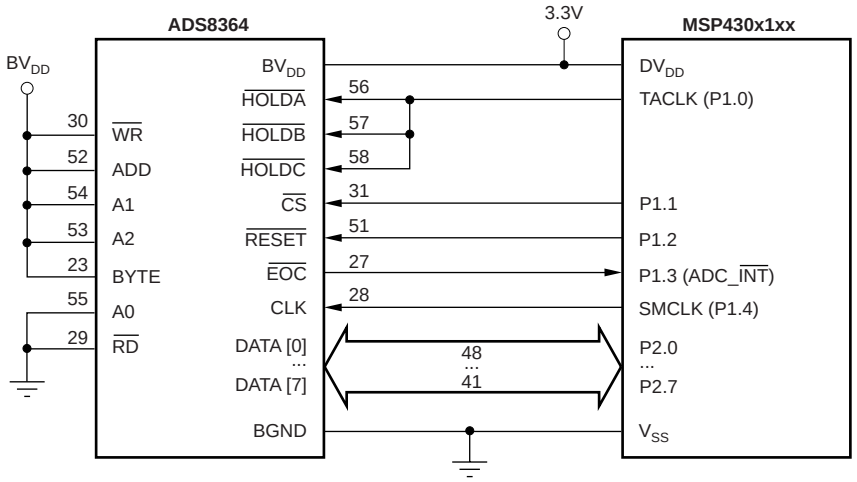


FIGURE 18. Typical MSP430x1xx Connection (Cycle Mode – Hardware Control).

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
8/06	C	1	—	Changed Throughput Rate from 250kHz to 250kSPS throughout document.
		2	Dissipation Ratings Table	Changed package from DGK to PAG.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8364Y/250	ACTIVE	TQFP	PAG	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS8364Y	Samples
ADS8364Y/2K	ACTIVE	TQFP	PAG	64	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS8364Y	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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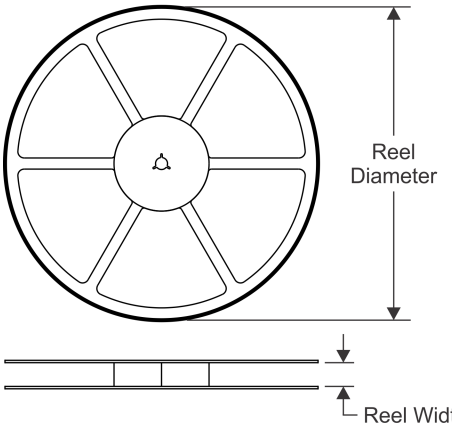
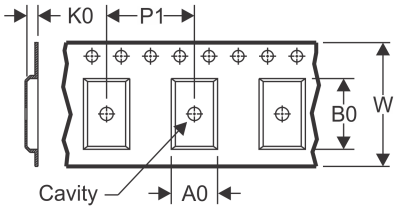
TAPE AND REEL INFORMATION

REEL DIMENSIONS

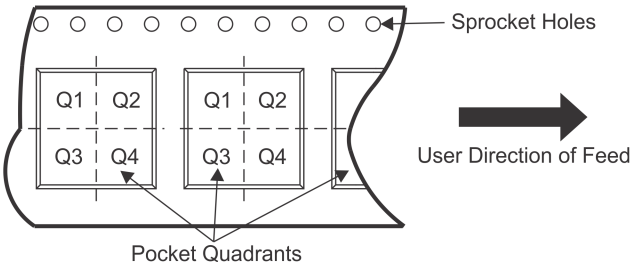


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

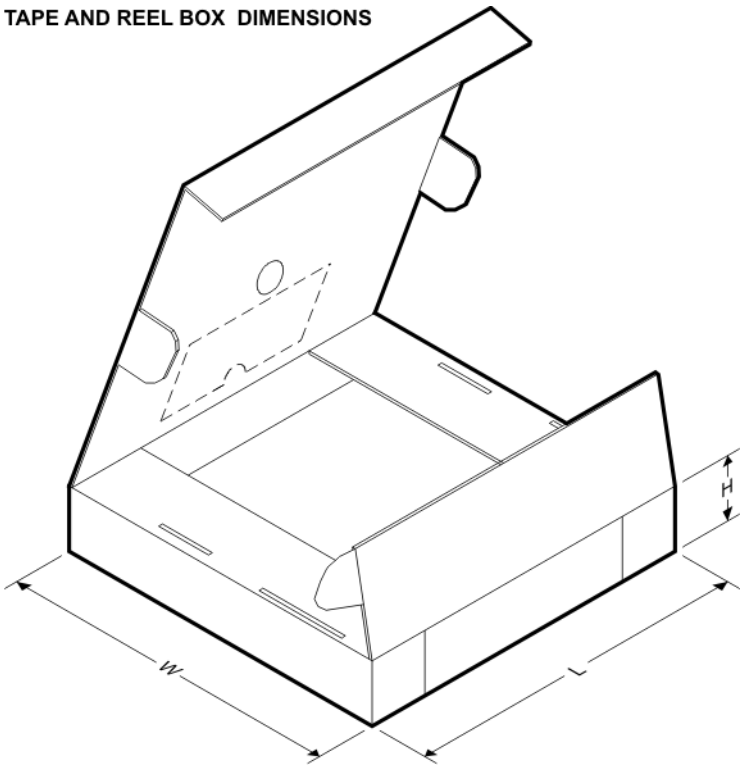
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8364Y/2K	TQFP	PAG	64	2000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

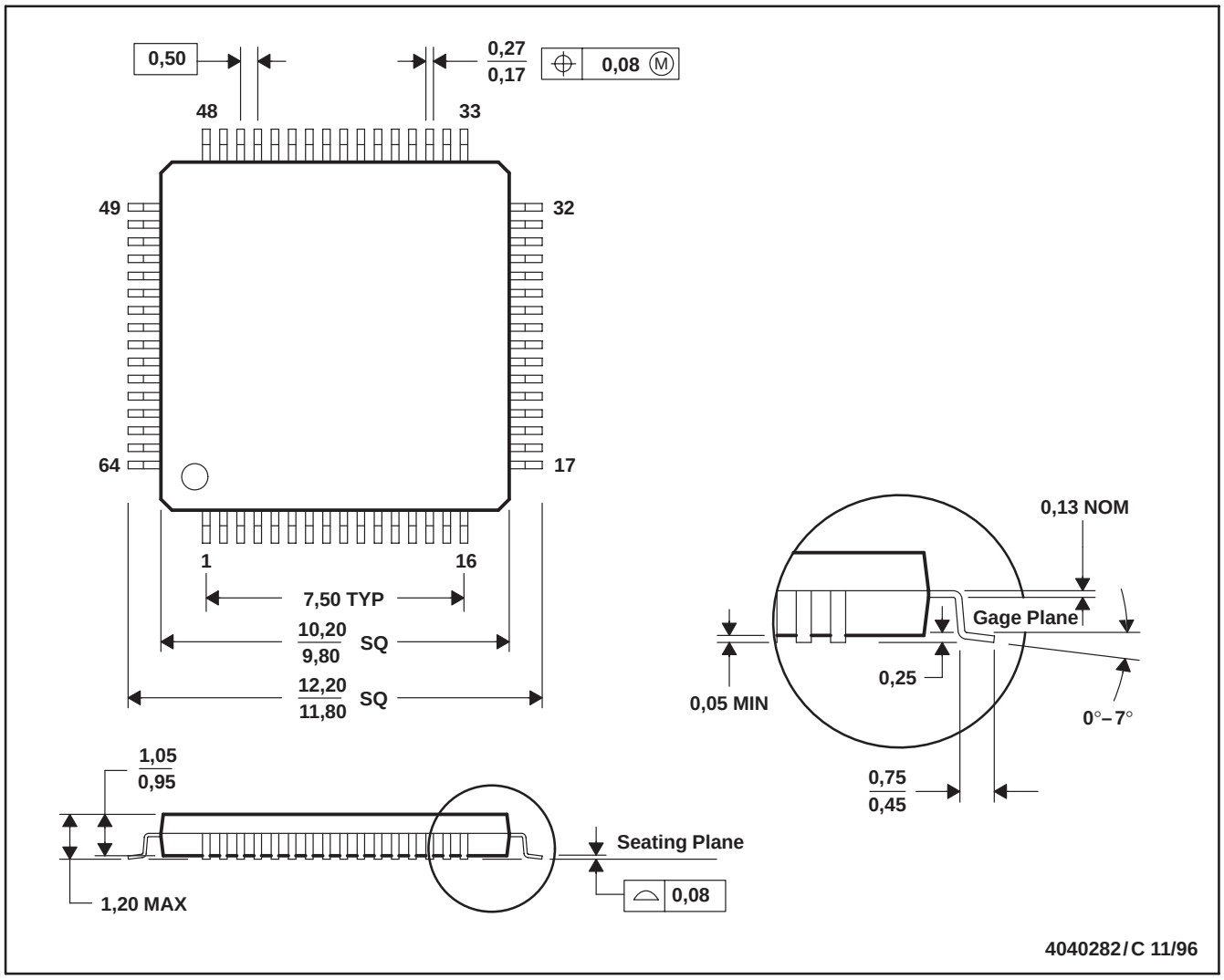
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

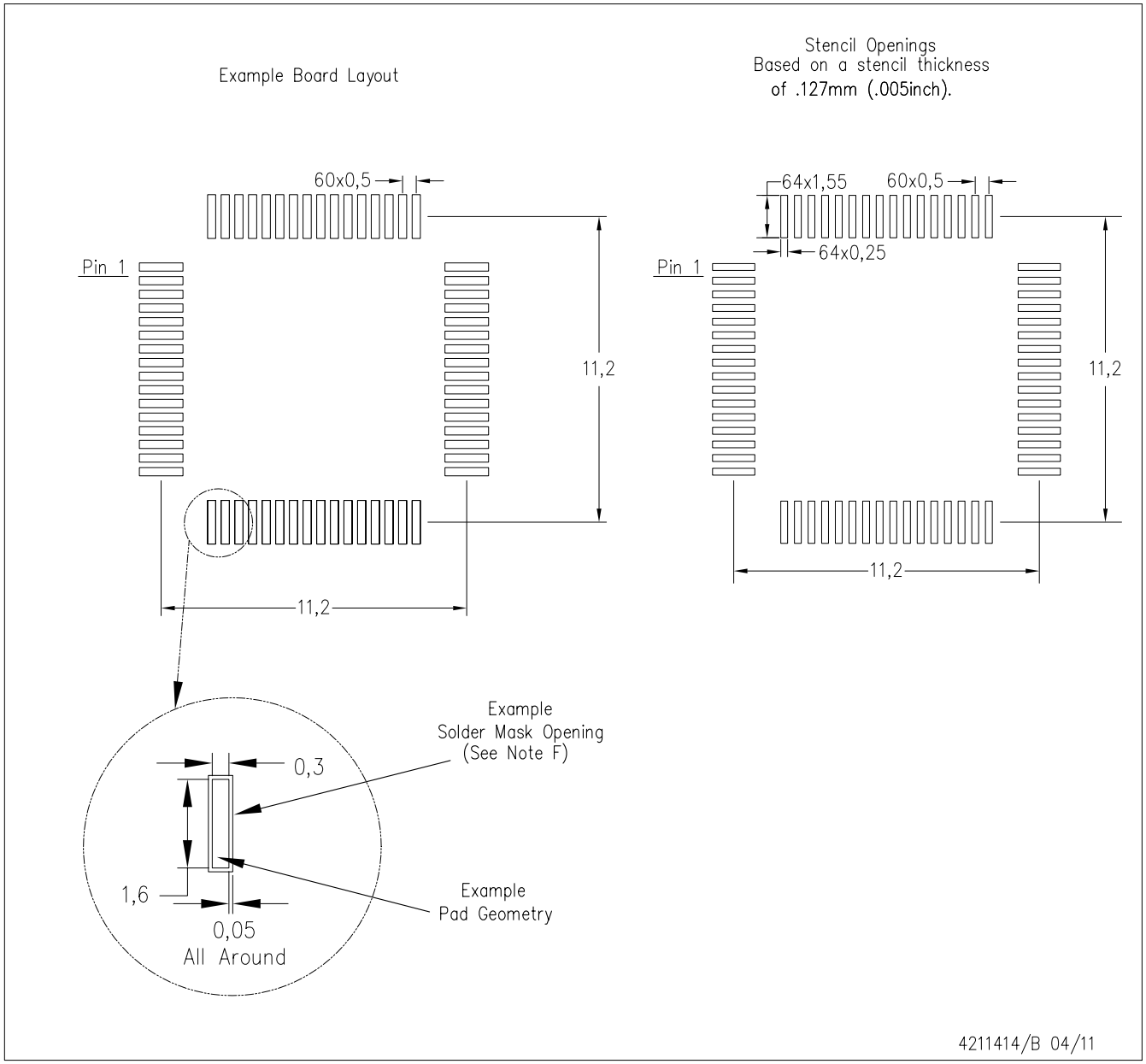
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8364Y/2K	TQFP	PAG	64	2000	350.0	350.0	43.0

PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



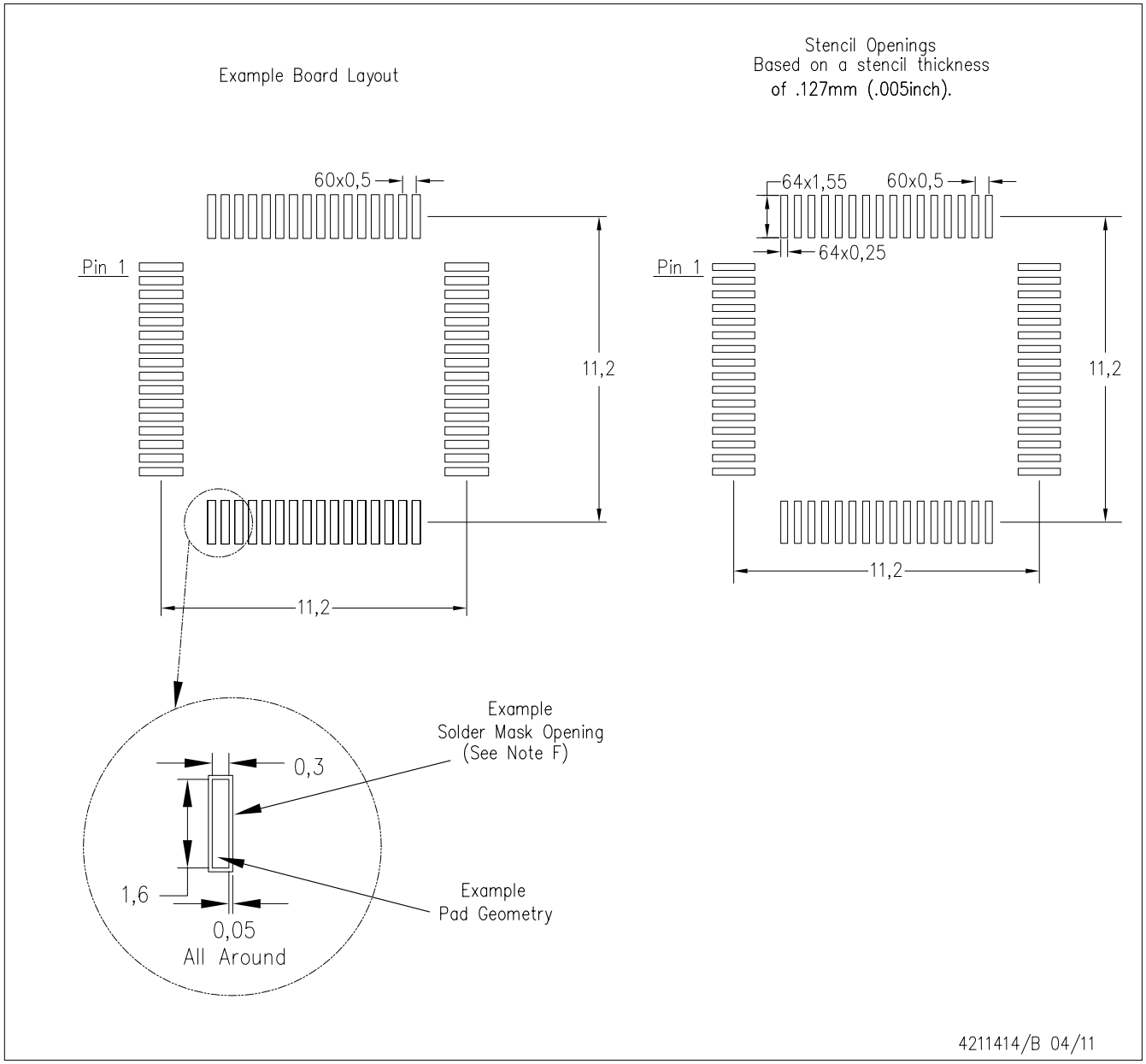
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PAG (S–PQFP–G64) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PAG (S–PQFP–G64) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
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