16 CHANNEL VARIABLE GAIN AMPLIFIER (VGA) WITH OCTAL HIGH SPEED ADC

Check for Samples: AFE5851

FEATURES

- **16 Variable Gain Amplifiers (VGA)**
  - **16 Single-Ended Buffered Inputs With $1V_{PP}$ Maximum Swing**
  - **5.5nV/$\sqrt{Hz}$ VCA Input Noise (31dB Gain).**
  - **Variable Gain –5dB to 31dB With 0.125dB Steps**
  - **Digital Gain Control**
- **3rd Order Anti-Aliasing Filter With Programmable Cut-Off Frequency (7.5, 10 and 14MHz).**
- **Clamping**
- **Analog-to-Digital Converter (ADC)**
  - **Octal channel 12-bit, 65 MSPS**
  - **32.5 MSPS Maximum per Input Channel**
  - **2 VGA Outputs Alternately Sampled by Each ADC**
  - **Internal and External Reference Support**
  - **No External Decoupling Required for References**
  - **Serial LVDS Outputs**
- **1.8V and 3.3V Supply**
- **39 mW Total Power per Channel at 32.5 MSPS**
- **64-QFN Package (9mm × 9mm)**

APPLICATIONS

- **Imaging: Ultrasound, PET**

RELATED DEVICES

- **AFE5801: Octal VGA+ADC, 65 MSPS/channel**

DESCRIPTION

The AFE5851 is an analog front-end targeting applications where the power and level of integration are critical. The device contains 16 variable gain amplifiers (VGA), followed by an octal high speed (up to 65 MSPS) analog to digital converter (ADC).

Each of the 16 single ended inputs is buffered, accepts up to $1V_{PP}$ maximum input swing and it is followed by a VGA with a gain range from –5dB to 31dB. The VGA gain is digitally controlled and the gain curves versus time can be stored in memory, integrated within the device using the serial interface.

A selectable clamping and anti-alias low pass filter (with 3dB attenuation at 7.5, 10 or 14MHz) is also integrated between the VGA and ADC for every channel. The VGA/anti-alias filter outputs are differential (limited to 2 V_{PP}) and drive the on-board 12-bit 65MSPS ADC that is shared between two VGAs to optimize the power dissipation. Each VGA output is sampled at alternate clock cycles, making the effective sampling frequency half the input clock rate. The ADC also scales down its power consumption should a lower sampling rate be selected.

The ADC outputs are serialized in LVDS streams further minimizing power and board area. The AFE5851 is available in a 64-pin QFN package ($9x9mm^2$) and is specified over the full industrial temperature range (–40°C to 85°C).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

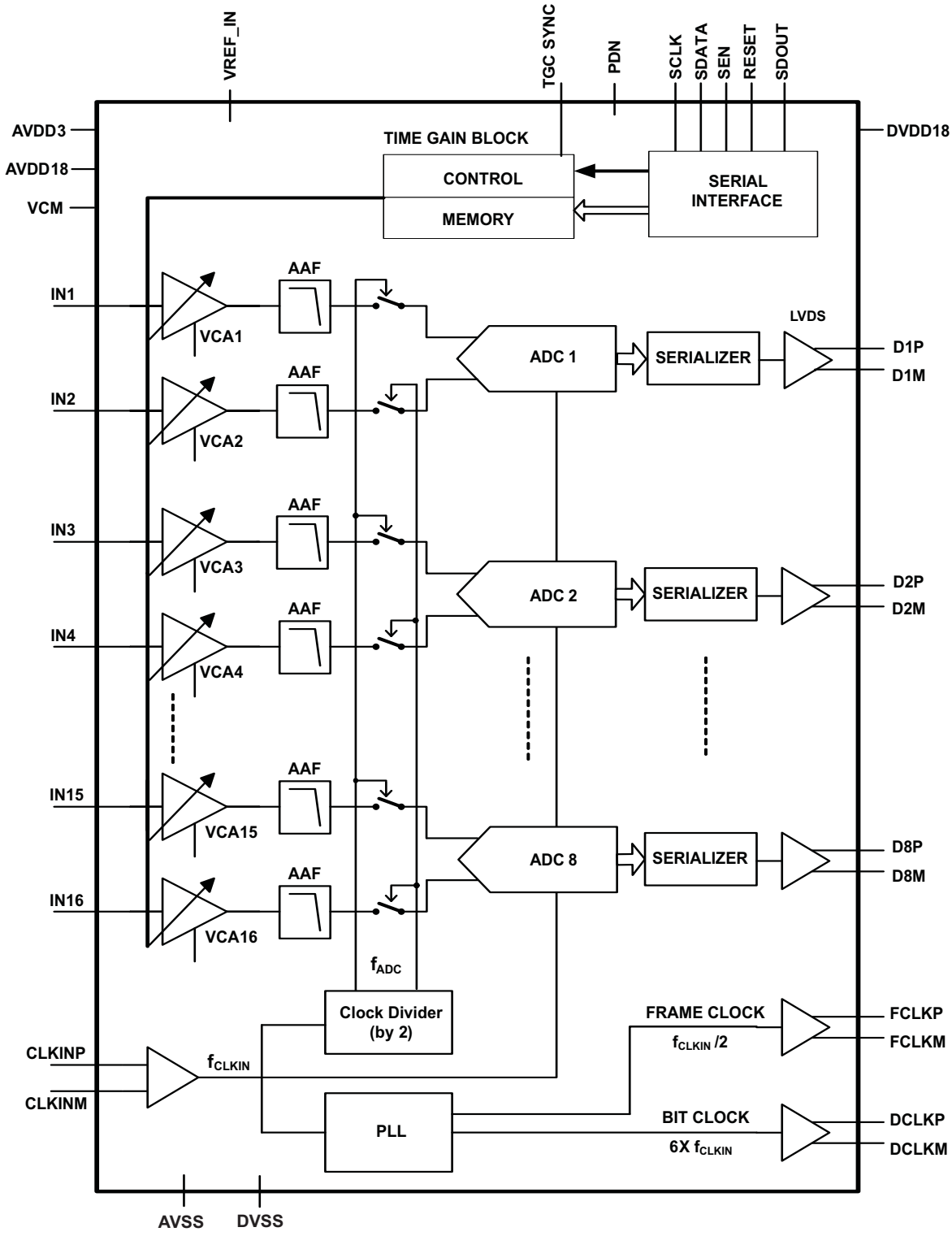
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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

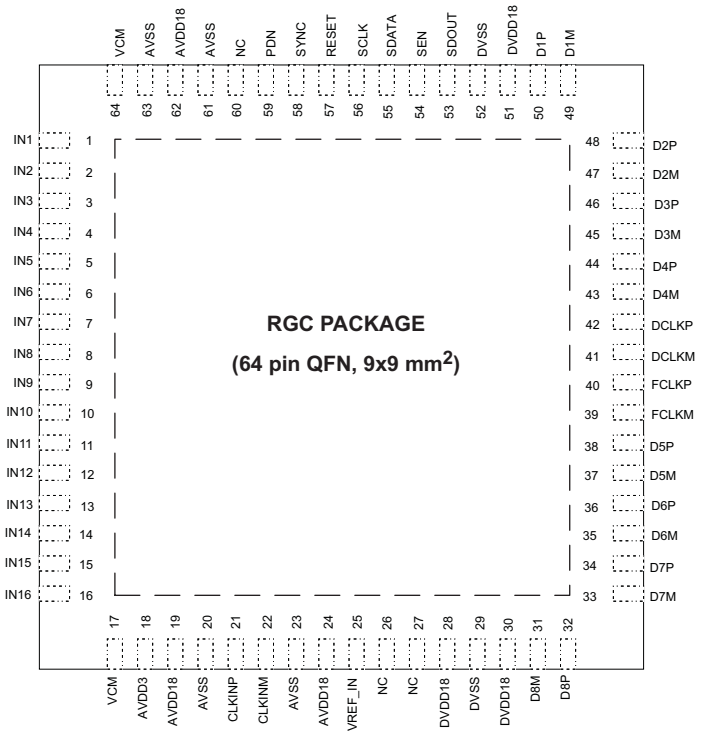
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BLOCK DIAGRAM



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PINOUT



PIN FUNCTIONS

NAME	NUMBER	DESCRIPTION
IN1–IN16	1–16	Single-ended analog input pins for channel 1 to 16.
CLKINP, CLKINM	21, 22	Differential clock input pins. Single-ended clock also supported (See Clock Inputs Section).
VCM	17, 64	Common-mode output pins for possible bias of the analog input signals.
VREF_IN	25	Reference input in the external reference mode.
RESET	57	Hardware reset pin (active high).
SCLK	56	Serial interface clock input.
SDATA	55	Serial interface data input.
$\overline{\text{SEN}}$	54	Serial interface enable.
SDOUT	53	Serial interface data readout.
PDN	59	Global power down control input (active high).
SYNC	58	TGC/VGA synchronization signal input
D1P/M... D4P/M D5P/M... D8P/M	50... 43 38... 31	LVDS output for channels 1 and 2, 3 and 4, 5 and 6.... to 15 and 16.
FCLKM, FCLKP	39, 40	LVDS frame clock output.
DCLKM,DCLP	41, 42	LVDS bit clock output.
AVDD3	18	3.3V Analog supply voltage.
AVDD18	19, 24, 62	1.8V Analog supply voltage.
DVDD18	28, 30, 51	1.8V LVDS buffer supply voltage.
AVSS	20, 23, 61, 63	Analog ground.
DVSS	29, 52	Digital ground.
NC	26, 27, 60	Do not connect.
Thermal Pad	Bottom of the package	Connect to AVSS.

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PACKAGING/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
AFE5851	QFN-64(2)	RGC	–40°C to 85°C	AFE5851	AFE5851IRGCT	Tape/Reel, 250
				AFE5851	AFE5851IRGCR	Tape/Reel, 2000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) For the thermal pad size on the package, see the mechanical drawings at the end of this document

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		RANGE	UNIT
	AVDD3 to AVSS	–0.3 to 3.8	V
	AVDD18 to AVSS	–0.3 to 2.2	V
	DVDD18 to DVSS	–0.3 to 2.2	V
	Voltage between AVSS and DVSS	–0.3 to 0.3	V
	Analog input pins (IN_i) to AVSS	–0.3V to Minimum (3.6, AVDD3+0.3)	V
	VREF_IN to AVSS	–0.3 to 2.2	V
	V_{CLKP}, V_{CLKM} to AVSS	–0.3 to 2.2	V
	Digital control pins to DVSS	–0.3 to 2.2	V
ESD	Human body model	2	kV
T_J	Maximum operating junction temperature	125	°C
T_{stg}	Storage temperature range	–60 to 150	°C

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied Exposure to absolute maximum rated conditions for extended periods may degrade device reliability

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

		TYP	UNIT
θ_{JA}	0LFM air flow	23.17	°C/W
θ_{JC}	2 oz. copper trace and pad soldered directly to a JEDEC standard 4-layer 3inch × 3inch PCB	22.1	°C/W

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	TYP	MAX	UNIT
T_A	Ambient Temperature	–40		85	°C
SUPPLIES					
AVDD3	Analog Supply Voltage (VGA)	3.0	3.3	3.6	V
AVDD18	Analog Supply Voltage (ADC)	1.7	1.8	1.9	V
DVDD18	Digital Supply Voltage (ADC, LVDS)	1.7	1.8	1.9	V
ANALOG INPUTS					
IN_i	Input voltage	VCM–0.5		VCM+0.5	V
VREF_IN in external reference mode		1.35	1.4	1.45	V
VCM load			3		mA
CLOCK INPUT					
f_{CLKIN}	Input clock frequency	5		65	MHz
$f_{Channel}$	Channel sampling frequency (f_{CLKIN}/2)	2.5		32.5	MSPS
Input Clock Duty Cycle		40%	50%	60%	

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RECOMMENDED OPERATING CONDITIONS (continued)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{CLKP-CLKM}$	Sine wave, AC-coupled	0.5			V_{PP}
	LVPECL, AC-coupled		1.6		V_{PP}
	LVDS, AC-coupled		0.7		V_{PP}
V_{CLKP}	LVCMOS, single-ended, V_{CLKM} connected to AVSS		1.8		V_{PP}
DIGITAL OUTPUT					
C_{LOAD}	External load capacitance from each output pin to DVSS		5		pF
R_{LOAD}	Differential load resistance (external) between the LVDS output pairs		100		Ω

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, typical values are at 25°C, min and max values are across full temperature range T_{min}= –40°C to T_{max}=85°C, AVDD3=3.3V, AVDD18=1.8V, DVDD18=1.8V, –1dBFS analog input AC coupled with 0.1μF, internal reference mode, maximum rated channel sampling frequency (32.5 MSPS), LVCMOS (single-ended) clock, 50% duty cycle, anti-aliasing filter set at 14MHz (3dB corner), output clamp disabled and analog high-pass filter enabled.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
VARIABLE GAIN AMPLIFIER (VGA)							
	Max input voltage swing	Linear operation			1		Vpp
VCM	Common-mode voltage	DC level at the input			1.6		V
	Gain range	Maximum gain – minimum gain			36		dB
	Maximum Gain			29.5	31	32.5	dB
	Gain resolution				0.125 or 1		dB
	Input resistance	From input to dc bias level			5		kΩ
	Input capacitance	From input to AVSS			2		pF
ANTIALIAS FILTER (AAF)							
	AAF cutoff frequency	7.5 MHz filter selected	–3 dB		7.5		MHz
		10 MHz filter selected			10		
		14 MHz filter selected			14		
	AAF stop-band attenuation	7.5 MHz filter selected	–6 dB		10		MHz
		10 MHz filter selected			14		
		14 MHz filter selected			20		
		7.5 MHz filter selected	–12 dB		18		MHz
		10 MHz filter selected			24		
		14 MHz filter selected			30		
	In-band attenuation	7.5 MHz filter selected	At 3.2 MHz		1.2		dB
		10 MHz filter selected			0.5		
		14 MHz filter selected			0.2		
FULL-CHANNEL CHARACTERISTICS							
	Gain matching	Across channels and parts			+0.1	+0.6	dB
	Gain error	–5 to 28dB gain		–1.2	±0.3	1.2	dB
		Gain > 28dB gain		–1.8	±0.5	1.8	
	Offset error	31dB gain		–50		50	LSB
	Input-referred noise voltage	5 MHz, 31dB VGA gain, low-noise mode			5	6.5	nV/√Hz
		5 MHz, 31dB VGA gain, default-noise mode			5.5		
SNR	Signal-to-noise ratio	–1dBFS ADC input, 6dB gain			66		dBFS
HD2	Second-harmonic distortion	–1dBFS ADC input, 17dB VGA gain, f_{in} = 2MHz		–48	–55		dBc
		–1dBFS ADC input, 31dB VGA gain, f_{in} = 2MHz		–55	–65		
HD3	Third-harmonic distortion	–1dBFS ADC input, 17dB VGA gain, f_{in} = 2MHz		–52	–63		dBc
		–1dBFS ADC input, 31dB VGA gain, f_{in} = 2MHz		–48	–58		

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ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise noted, typical values are at 25°C, min and max values are across full temperature range T_{min}= –40°C to T_{max}=85°C, AVDD3=3.3V, AVDD18=1.8V, DVDD18=1.8V, –1dBFS analog input AC coupled with 0.1µF, internal reference mode, maximum rated channel sampling frequency (32.5 MSPS), LVCMOS (single-ended) clock, 50% duty cycle, anti-aliasing filter set at 14MHz (3dB corner), output clamp disabled and analog high-pass filter enabled.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SFDR	Spurious free dynamic range	–1dBFS ADC input, 17dB VGA gain, f_{in} = 2MHz		55		dBc
THD	Total harmonic distortion	–1dBFS ADC input, 17dB VGA gain, f_{in} = 2MHz		54		dBc
IMD	Intermodulation distortion	f_{in1}=1MHz, f_{in2}=2MHz, $A_{in1,\ in2}$ = –7dBFS, 30dB VGA gain		–70		dBFS
	Group delay variation	f_{in} from 100kHz to 14MHz, across gain settings and channels		±3.5		ns
		f_{in} from 100kHz to 14MHz, across channels		±1.5		
	Input overload recovery	≤6dB overload to within 1%		1		Input clock cycles
	Clamp level	After amplification. Clamp enabled by default		3		dB
	ADC number of bits			12		
	Crosstalk	Aggressor: f_{in} = 2MHz, 1dB below ADC full-scale Victims (channel sharing same ADC): 50Ω to AVSS		65		dB
POWER						
	Total power dissipation	Default-noise mode		633	723	mW
		Low-noise mode		715	831	
I_{AVDD3}	AVDD3 Current consumption			4.7	7	mA
I_{AVDD18}	AVDD18 Current consumption	Default-noise mode		259	290	mA
		Low-noise mode		310	350	
I_{DVDD18}	DVDD18 Current consumption			81	100	mA
	Power down	Standby mode		64		mW
		Full power down mode		5	30	mW
AC PSRR	Power-supply rejection ratio			30		dBc

DIGITAL CHARACTERISTICS(1)

The DC specifications refer to the condition where the digital outputs are not switching, but permanently at a valid logic level 0 or 1. Unless otherwise noted, typical values are at 25°C, min and max values are across full temperature range T_{min}= –40°C to T_{max}=85°C, AVDD3=3.3V, AVDD18=1.8V, DVDD18=1.8V, external differential load resistance between the LVDS output pair R_{load}=100Ω.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS					
High-level input voltage		1.4		3.6	V
Low-level input voltage				0.8	V
High-level input current			10		µA
Low-level input current			10		µA
Input Capacitance			4		pF
DIGITAL OUTPUTS					
High-level output voltage			1375		mV
Low-level output voltage			1025		
Output differential voltage $\|V_{OD}\|$		270	380	490	
Output offset voltage V_{OS}	Common-mode voltage of D_iP and D_iM	0.9	1.15	1.5	V
Output capacitance	Output capacitance inside the device, from either output to DVSS		2		pF

(1) Note: All LVDS specifications have been characterized but not production tested.

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OUTPUT INTERFACE TIMING(1)

Typical values are at 25°C, AVDD3 = 3.3V, AVDD18 = DVDD = 1.8V, LVCMOS (single ended) clock, C_{LOAD} = 5pF, R_{LOAD} = 100Ω, I_O = 3.5mA, unless otherwise noted. Minimum and maximum values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C.

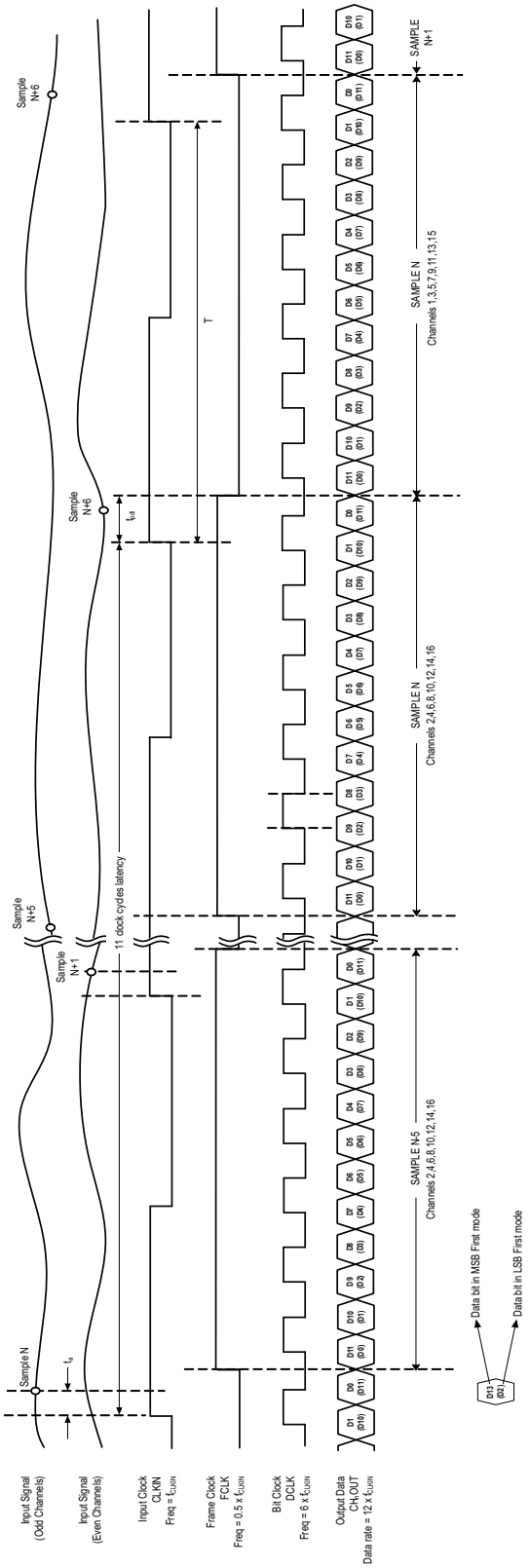
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_a	Aperture delay	The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs	0.7	3		ns
	Aperture delay matching	Across channels within the same device		±150		ps
t_j	Aperture jitter			450		fs rms
	Wake-up time	Time to valid data after coming out of STANDBY mode		10	50	µs
		Time to valid data after coming out of PDN GLOBAL mode		50	200	
		Time to valid data after stopping and restarting the input clock		30	200	
	ADC latency	Default, after reset		11		Input clock cycles
t_{delay}		Input clock rising edge (zero cross) to frame clock rising edge (zero cross) minus half the input clock period (T).	3	4.7	6.4	ns
t_{delay}	Variation	At fixed supply and 20°C T difference	–1		1	ns
t_{RISE} t_{FALL}	Data rise time Data fall time	Rise time measured from –100mV to 100mV Fall time measured from 100mV to –100mV 10 MHz < f_{CLKIN} < 65MHz	0.1	0.25	0.4	ns
$t_{FCLKRISE}$ $t_{FCLKFALL}$	Frame clock rise time Frame clock fall time	Rise time measured from –100mV to 100mV Fall time measured from 100mV to –100mV 10MHz < f_{CLKIN} < 65MHz	0.1	0.25	0.4	ns
	Frame clock duty cycle	Zero crossing of the rising edge to zero crossing of the falling edge	48	50	52	ns
$t_{DCLKRISE}$ $t_{DCLKFALL}$	Bit clock rise time Bit clock fall time	Rise time measured from –100mV to 100mV Fall time measured from 100mV to –100mV 10MHz < f_{CLKIN} < 65MHz	0.1	0.2	0.35	ns
	Bit clock duty cycle	Zero crossing of the rising edge to zero crossing of the falling edge 10MHz < f_{CLKIN} < 65MHz	44%	50%	56%	

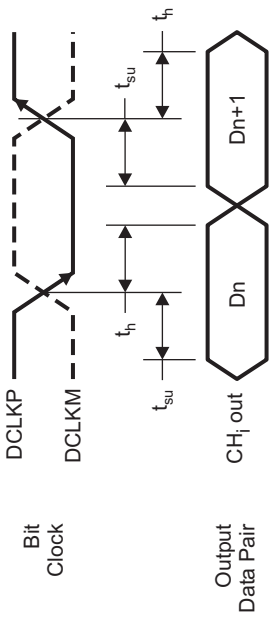
Table 1. Output Interface Timing(1)

fCLKIN, Input Clock Frequency [2x Channel Sampling frequency]	Period (T)	Setup Time (tsu), ns			Hold Time (th), ns			tpdi = 0.5 × Ts + tdelay, ns		
MHz	ns	Zero-Cross Data to Zero-Cross Clock (both edges)			Zero-Cross Clock to Zero-Cross Data (both edges)			Input Clock Zero-Cross (rise edge) to Frame Clock Zero-Cross (rise-edge)		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
65	15	0.35	0.65		0.3	0.6			12.35	
50	20	0.5	0.8		0.5	0.8			14.6	
40	25	0.75	1.05		0.75	1.05			17.04	
30	33	1	1.4		1	1.4			21.19	
20	50	1.7	2.1		1.7	2.1			29.52	
10	100	3.8	4.2		3.8	4.2			54.71	

(1) See timing diagrams on the following page.

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TYPICAL CHARACTERISTICS

All graphs are at 25°C, AVDD3 = 3.3V, AVDD18 = DVDD18 = 1.8V, –1dBFS analog input AC coupled with 0.1μF, internal reference mode, maximum rated channel sampling frequency (32.5 MSPS), LVCMOS (single-ended) clock, 50% duty cycle, f_{IN} = 2MHz, anti-aliasing filter set at 14MHz (3dB corner), output clamp disable and analog high-pass filter enabled.

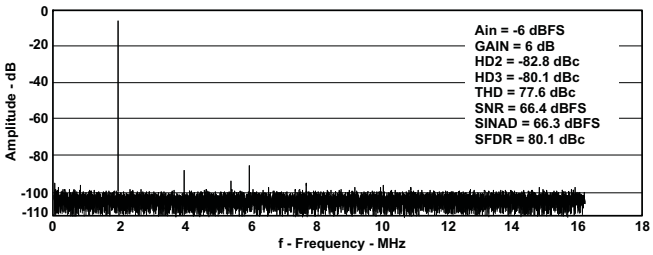


Figure 1. FFT for 2MHz Input Signal and 6dB Gain

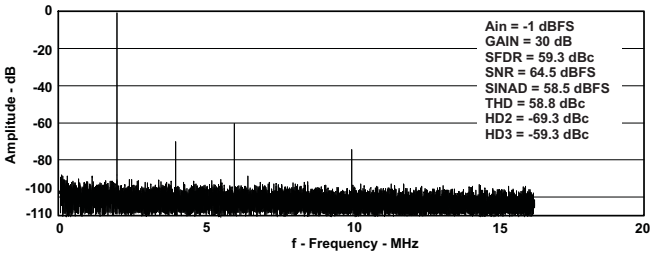


Figure 2. FFT for 2MHz Input Signal and 30dB Gain

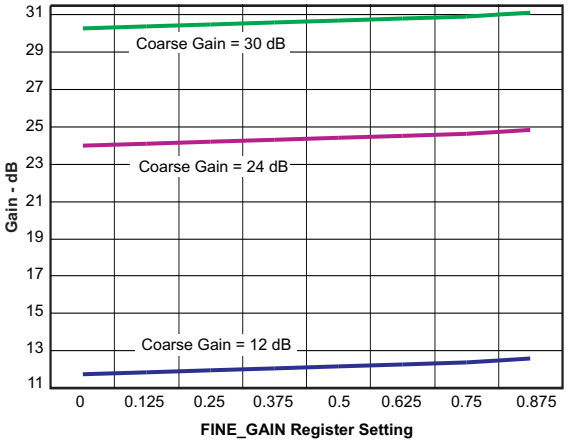


Figure 3. Fine Gain versus Gain Code

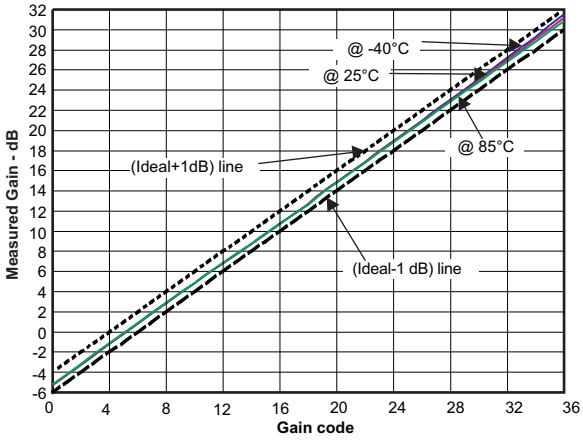


Figure 4. Measured Gain versus Gain Code and Temperature

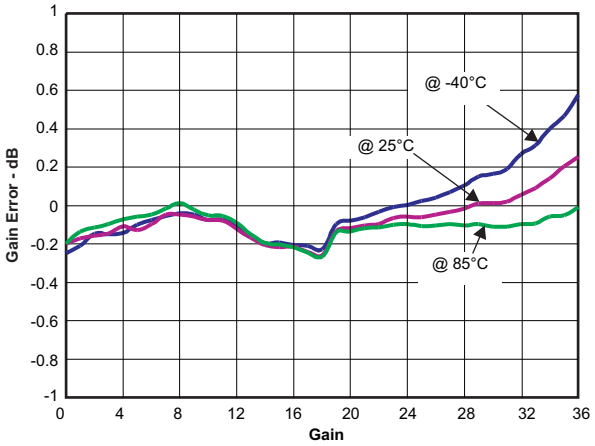


Figure 5. Gain Error versus Gain Code and Temperature

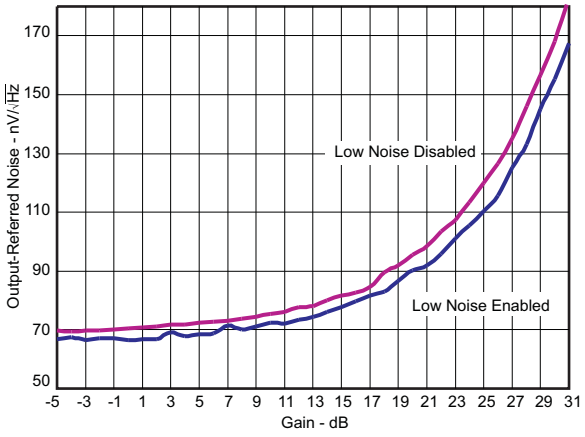


Figure 6. Output-Referred Noise versus Gain

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TYPICAL CHARACTERISTICS (continued)

All graphs are at 25°C, AVDD3 = 3.3V, AVDD18 = DVDD18 = 1.8V, –1dBFS analog input AC coupled with 0.1μF, internal reference mode, maximum rated channel sampling frequency (32.5 MSPS), LVCMOS (single-ended) clock, 50% duty cycle, f_{IN} = 2MHz, anti-aliasing filter set at 14MHz (3dB corner), output clamp disable and analog high-pass filter enabled.

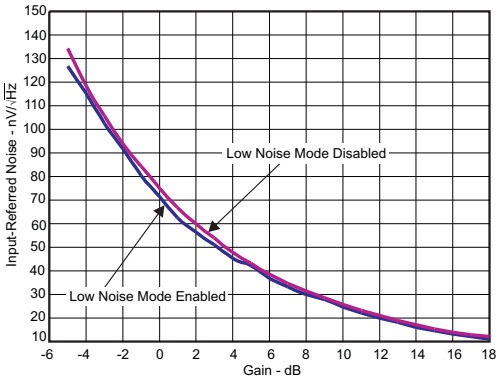


Figure 7. Input-Referred Noise for Low Gains

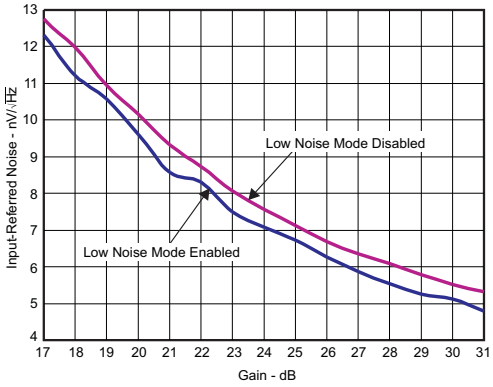


Figure 8. Input-Referred Noise for High Gains

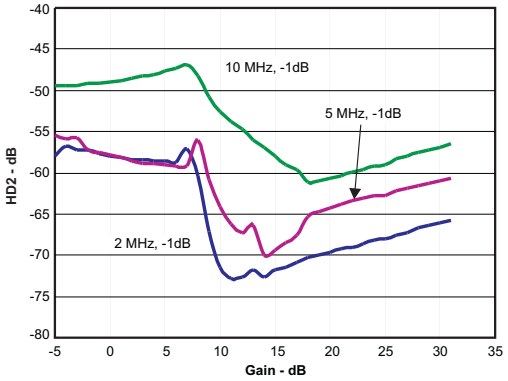


Figure 9. HD2 Across Coarse Gain and 3 Fin (–1dBFS)(1)

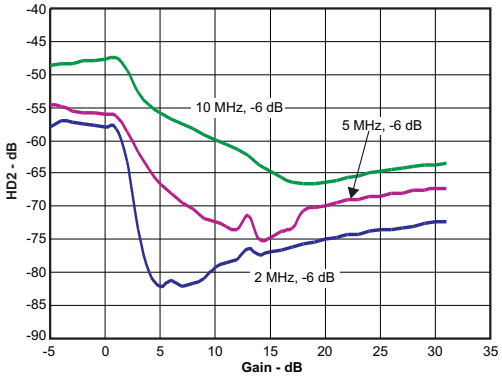


Figure 10. HD2 Across Coarse Gain and 3 Fin (–6dBFS)(2)

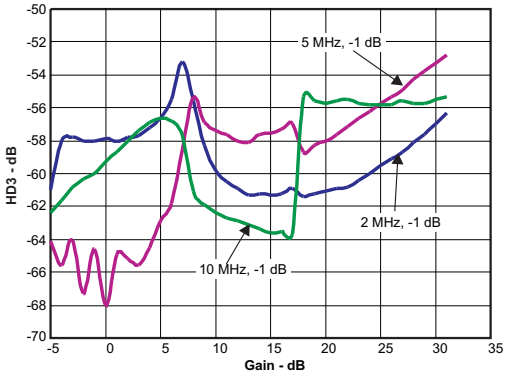


Figure 11. HD3 Across Coarse Gain and 3 Fin (–1dBFS)(1)

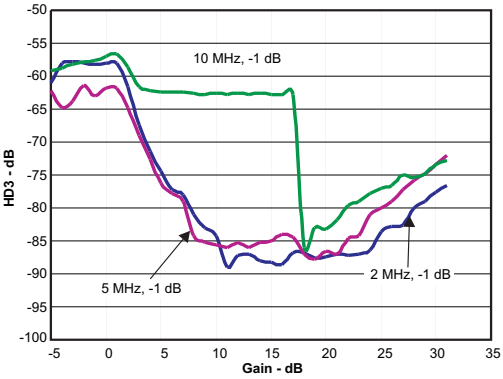


Figure 12. HD3 Across Coarse Gain and 3 Fin (–6dBFS)(2)

(1) For gains ≥5dB, the input amplitude is adjusted to give –1dBFS. At 5dB gain, input amplitude is 4dBm (corresponding to –1dBFS). For gains less than 5dB, the input is kept constant at 4dBm.

(2) For gains ≥0dB, the input amplitude is adjusted to give –6dBFS. At 0dB gain, input amplitude is 4dBm (corresponding to –6dBFS). For gains less than 0dB, the input is kept constant at 4dBm.

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TYPICAL CHARACTERISTICS (continued)

All graphs are at 25°C, AVDD3 = 3.3V, AVDD18 = DVDD18 = 1.8V, –1dBFS analog input AC coupled with 0.1μF, internal reference mode, maximum rated channel sampling frequency (32.5 MSPS), LVCMOS (single-ended) clock, 50% duty cycle, f_{IN} = 2MHz, anti-aliasing filter set at 14MHz (3dB corner), output clamp disable and analog high-pass filter enabled.

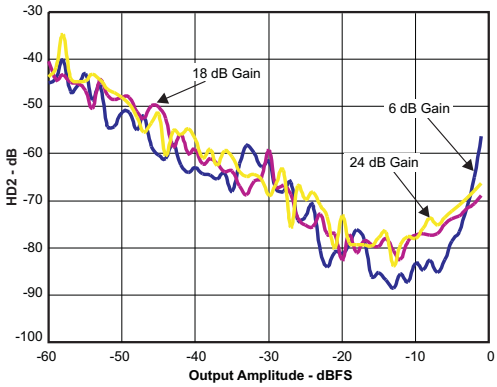


Figure 13. HD2 versus Output Amplitude

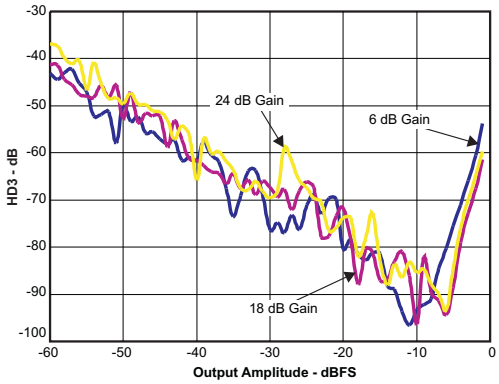


Figure 14. HD3 versus Output Amplitude

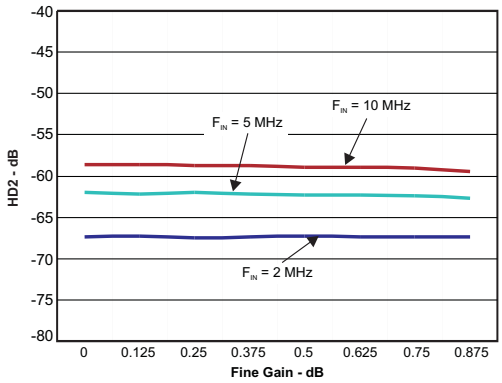


Figure 15. HD2 (at 24 dB Gain) Across Fine Gain

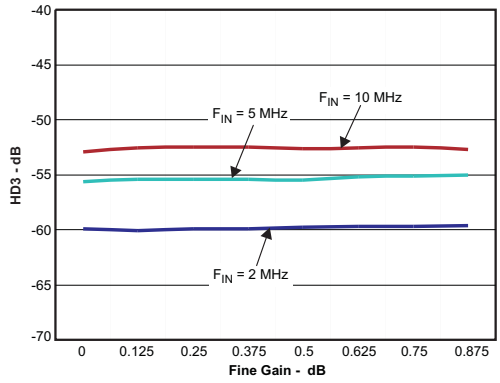


Figure 16. HD3 (at 24 dB Gain) Across Fine Gain

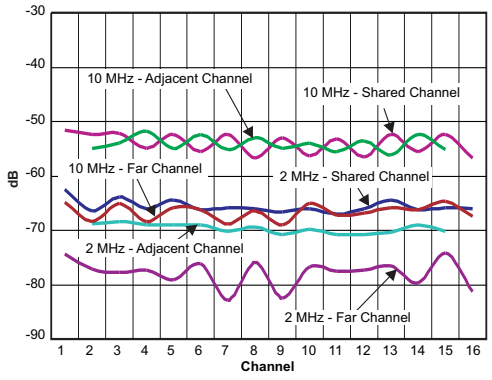


Figure 17. Crosstalk(3)

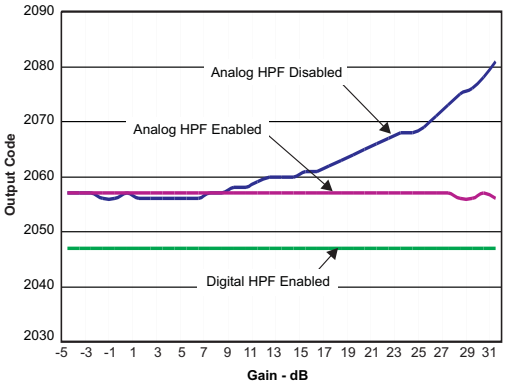


Figure 18. Output Offset Across TGC Gain

(3) -1dB signal applied on one channel at a time and output is observed on:
1. Shared channel - second channel in the pair having a common ADC
2. Adjacent channel - channel next to the aggressor channel, but not a shared channel
3. Far channel - all other channels (neither shared or adjacent)

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TYPICAL CHARACTERISTICS (continued)

All graphs are at 25°C, AVDD3 = 3.3V, AVDD18 = DVDD18 = 1.8V, –1dBFS analog input AC coupled with 0.1μF, internal reference mode, maximum rated channel sampling frequency (32.5 MSPS), LVCMOS (single-ended) clock, 50% duty cycle, f_{IN} = 2MHz, anti-aliasing filter set at 14MHz (3dB corner), output clamp disable and analog high-pass filter enabled.

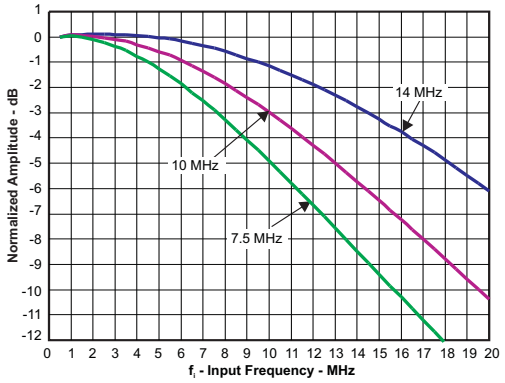


Figure 19. Antialiasing Filter Frequency Response

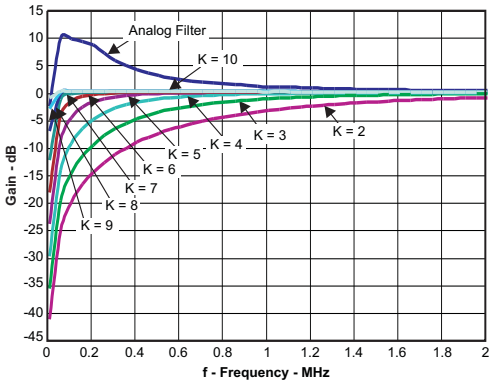


Figure 20. Highpass Filter Options

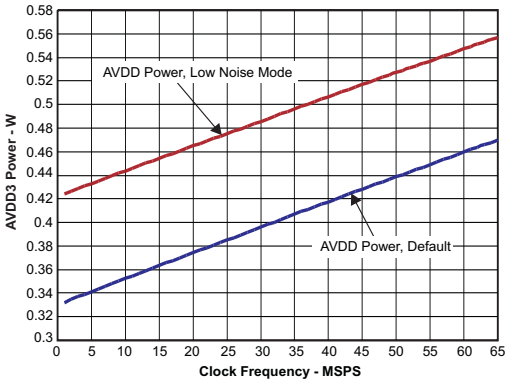


Figure 21. Analog Power versus Input Clock Frequency

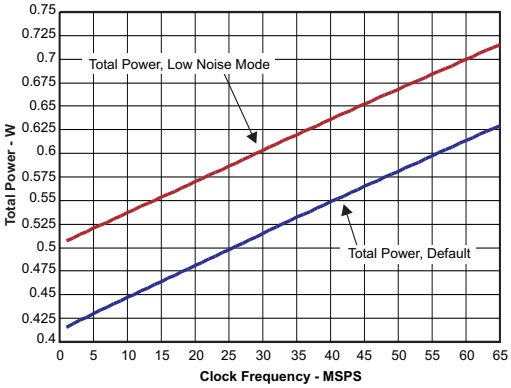


Figure 22. Total Power versus Input Clock Frequency

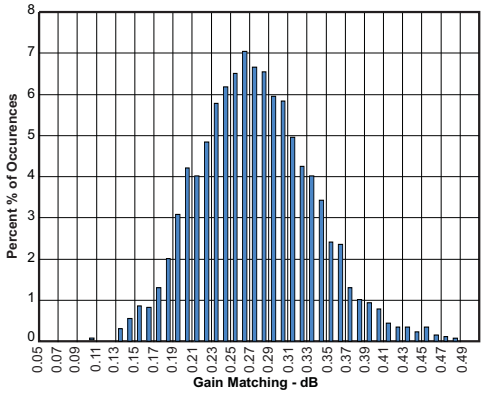


Figure 23. Gain Matching Measured at a Single Gain (30 dB) as Peak-to-Peak Variation of Gain Across Channels on Every Device and Measured at 3 Temperatures. Every Device at Each Temperature is Counted as One Event.

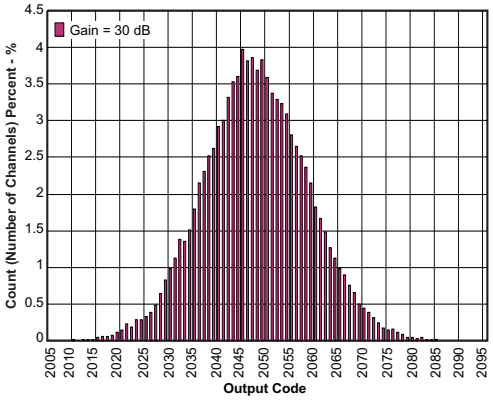


Figure 24. Offset (Average Code) with Signal. Every Channel Counted as One Event.

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TYPICAL CHARACTERISTICS (continued)

All graphs are at 25°C, AVDD3 = 3.3V, AVDD18 = DVDD18 = 1.8V, –1dBFS analog input AC coupled with 0.1μF, internal reference mode, maximum rated channel sampling frequency (32.5 MSPS), LVCMOS (single-ended) clock, 50% duty cycle, f_{IN} = 2MHz, anti-aliasing filter set at 14MHz (3dB corner), output clamp disable and analog high-pass filter enabled.

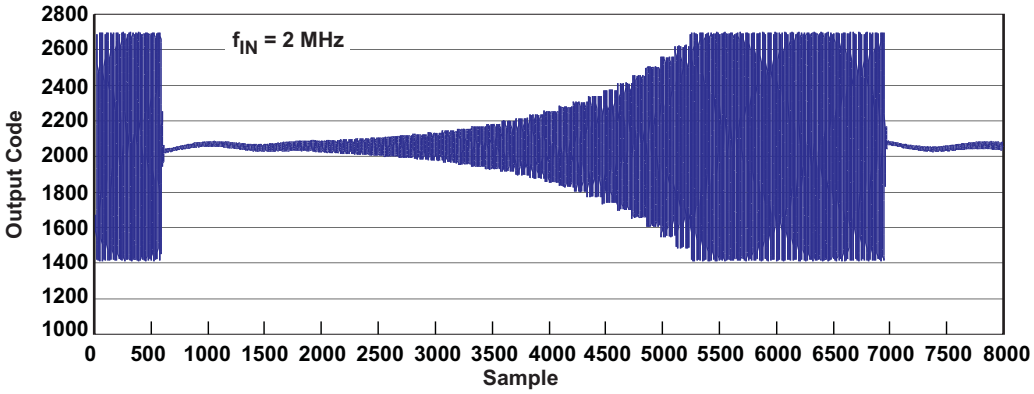


Figure 25. TGC Sweep with Interpolation Disabled and High-Pass Filter Enabled

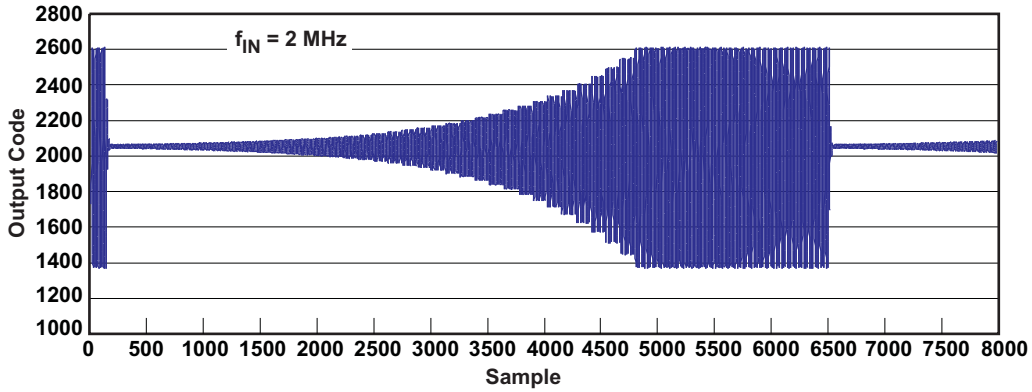


Figure 26. TGC Sweep with Interpolation Disabled and High-Pass Filter Disabled

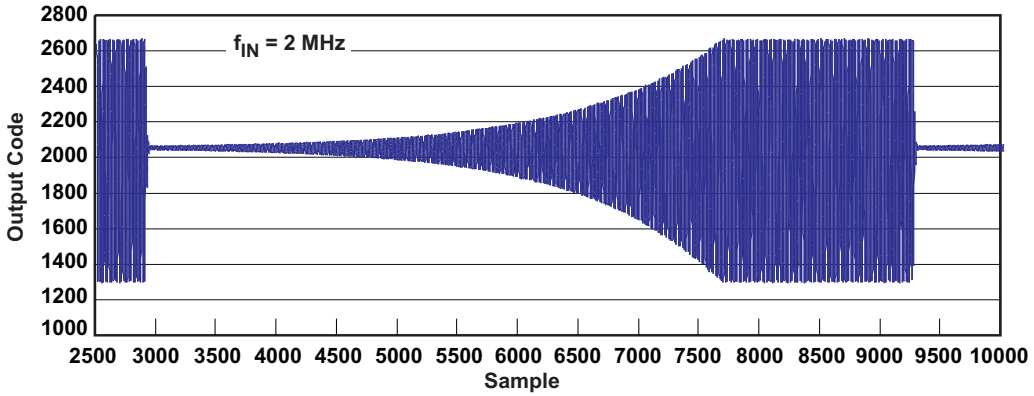


Figure 27. TGC Sweep with Interpolation Enabled and High-Pass Filter Disabled

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TYPICAL CHARACTERISTICS (continued)

All graphs are at 25°C, AVDD3 = 3.3V, AVDD18 = DVDD18 = 1.8V, –1dBFS analog input AC coupled with 0.1μF, internal reference mode, maximum rated channel sampling frequency (32.5 MSPS), LVCMOS (single-ended) clock, 50% duty cycle, f_{IN} = 2MHz, anti-aliasing filter set at 14MHz (3dB corner), output clamp disable and analog high-pass filter enabled.

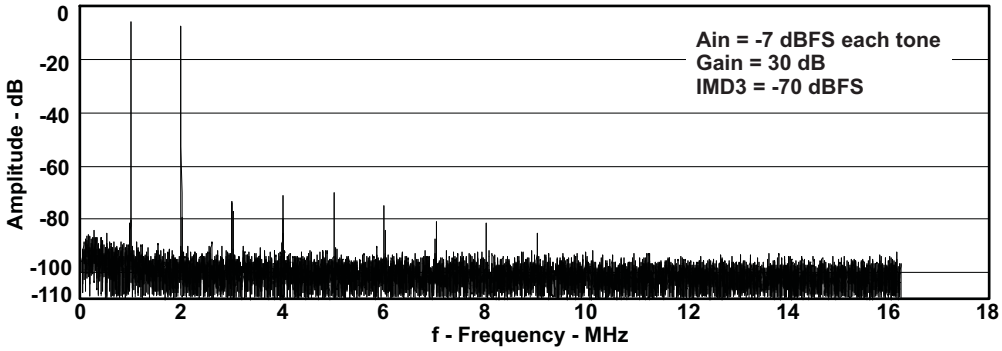


Figure 28. Intermodulation Distortion

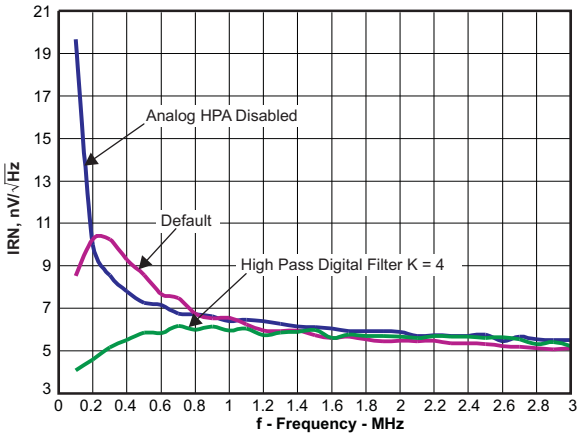


Figure 29. IRN versus Frequency (Gain = 31dB)

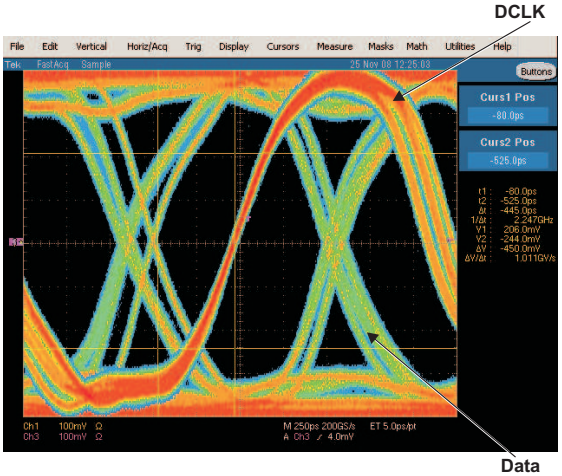


Figure 30. LVDS Eye Pattern

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APPLICATION INFORMATION

THEORY OF OPERATION

The AFE5851 is a low power CMOS monolithic analog front end that includes a 16-channel variable gain amplifier (VGA) followed by an 8-channel 12-bit high speed pipeline analog to digital converter (ADC) based on switched capacitor architecture.

Each of the 16 VGA single ended inputs is buffered and accepts a maximum swing of $1V_{PP}$ centered at a DC level (VCM) of about 1.6V.

Each VGA has a gain range from –5dB to 31dB and it is digitally controlled, with a resolution of 0.125 dB. The gain curves (common to all VGAs) versus time can be stored in memory integrated within the device using the serial interface.

A hardware sync input pin is available (SYNC). When a pulse is applied to this pin, all the VGAs in the device start stepping through the selected time-gain curve at the same clock cycle. This sync can also be initiated by software using the serial interface.

A selectable anti-alias low pass filter (AAF) with 6 dB attenuation at 7.5MHz, 10MHz or 14MHz, is also integrated, together with clamping (which can be disabled).

The VGA/AAF can output $2V_{PP}$ differential swing without degradation in the specified linearity, and drive an on-board 12-bit ADC shared between two VGAs to optimize power dissipation. Each VGA output is sampled at the rising edge of alternating clock cycles, making the effective sampling frequency half the input clock rate. For instance, in order to sample each analog channel at 30 MSPS, the input clock frequency needs to be 60 MHz. This effectively introduces a half (sampling) clock delay between the sampling instants of the two analog channels.

After the input signals are captured by the sample and hold circuit, the samples are sequentially converted by a series of low resolution stages. The stage outputs are combined in a digital correction logic block to form the final 12-bit word with a latency of 11 clock cycles (without taking into account the delays introduced by the optional digital signal processing functions). The 12-bit words of each channel are serialized and output as LVDS levels in straight offset binary format. In addition to the data streams, a bit clock and frame clock are also output. The frame clock is aligned with the 12-bit word boundary.

Notice that for the correct operation of the device (see Serial Interface Section) a positive pulse must be applied to the Reset pin. This sets the internal control registers to zero. There is, nevertheless, no need for any type of power-up sequencing.

INPUT CONFIGURATION

The analog input for the AFE5851 (Figure 31) consists of an analog buffer input gate biased to a value of 1.6V (usually referred as voltage common mode, VCM). The biasing is done with an internal resistor of 5kΩ. For proper operation, the input signal should be in the recommended input range. The maximum input swing is limited to $1V_{PP}$ before distortion/saturation of the input stage occurs. As the input DC level (VCM) is about 1.6V, the input of the VGA should stay between 1.1V and 2.1V. If the information in the low frequencies of the signal is irrelevant AC coupling can be used. As the input capacitor forms a high-pass filter with the internal bias resistor (5kΩ), the value of the capacitor should allow the lowest frequency of interest to pass with minimum attenuation. For the typical frequencies used in ultrasound (>1MHz) a value of 10nF or greater is recommended. If DC coupling is preferred, the user can tap the VCM output pins to set the DC level of the input signal. VCM output should be connected to high input impedance circuits as its driving capability is limited. Regardless of the chosen input configuration, a capacitor of 100nF should be connected on each VCM input to AVSS.

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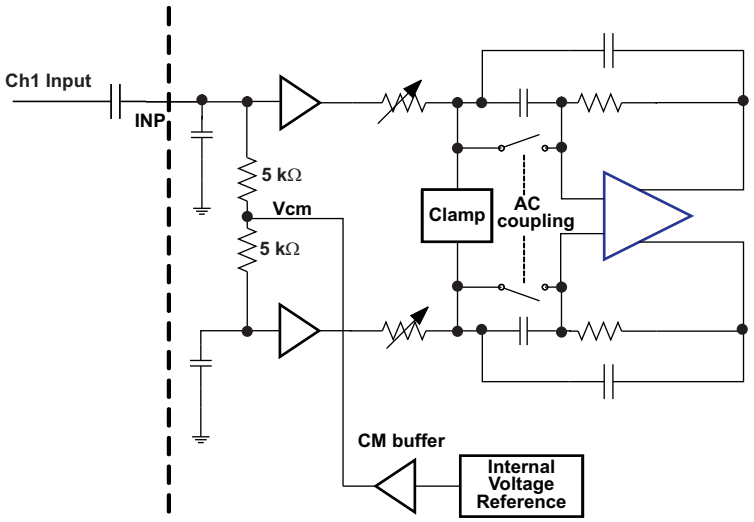


Figure 31. Input Equivalent Circuit

SERIAL INTERFACE

Register Initialization

After power-up, the internal registers must be initialized to the default value (zero). Initialization can be done in one of two ways:

1. Through a hardware reset, by applying a positive pulse in the RESET pin
2. Through a software reset, using the serial interface, by setting the SOFTWARE RESET bit to high. Setting this bit initializes the internal registers to the respective default values (all zeros) and then self-resets the SOFTWARE RESET bit to low. In this case, the RESET pin can stay low (inactive).

Reset Timing

Typical values at 25°C, min and max values across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD3 = 3.3V, AVDD18 = DVDD18 = 1.8V unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay time	Delay from power-up of AVDD and LVDD to RESET pulse active	5			ms
t_2	Reset pulse width	Pulse width of active RESET signal	10			ns
t_3	Register write delay time	Delay from RESET disable to SEN active	25			ns
t_{PO}	Power-up delay time	Delay from power-up of AVDD and LVDD to output stable		6.5		ms

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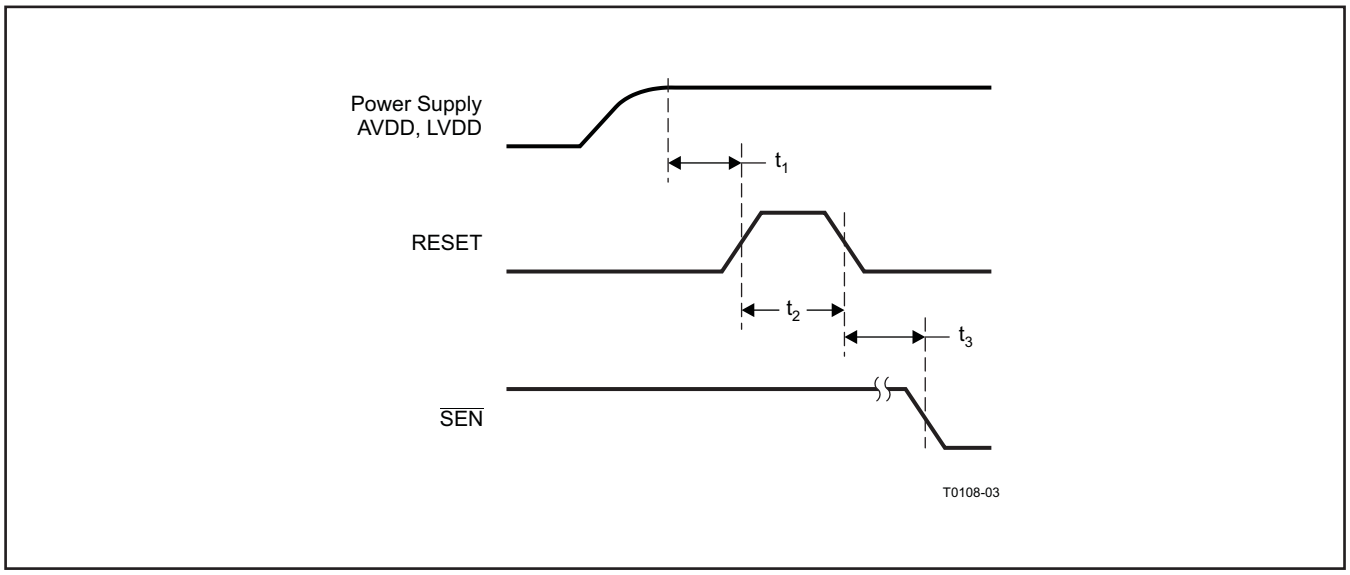


Figure 32. Reset Timing Diagram

Programming of different modes can be done through the serial interface formed by pins SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data) and RESET. SCLK and SDATA have a pull-down resistor to GND of 100kΩ and SEN has a 100kΩ pullup resistor to DVDD18. Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA is latched at every rising edge of SCLK when SEN is active (low). The serial data is loaded into the register at every 24th SCLK rising edge when SEN is low. If the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiple of 24-bit words within a single active SEN pulse (there is an internal counter that counts groups of 24 clocks after the falling edge of SEN). The interface can work with the SCLK frequency from 20 MHz down to low speeds (few Hertz) and even with non-50% duty cycle SCLK.

The data is divided into two main portions: a register address (8 bits) and the data itself, to load on the addressed register (16bits). When writing to a register with unused bits, these should be set to 0. The following timing diagram illustrates this process:

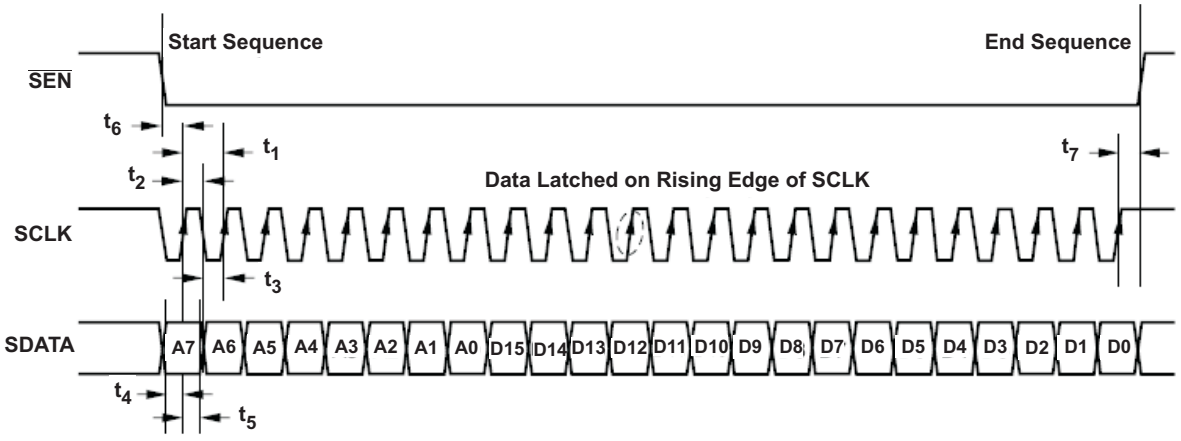


Figure 33. Serial Interface Register Write

Minimum values across the full temperature range, T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD3 = 3.3V, AVDD18 = DVDD18 = 1.8V.

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_1	SCLK period	50			ns
t_2	SCLK high time	20			ns
t_3	SCLK low time	20			ns
t_4	Data setup time	5			ns
t_5	Data hold time	5			ns
t_6	SEN fall to SCLK rise	8			ns
t_7	Time between last SCLK rising edge to SEN rising edge	8			ns

General Purpose Register Map

The internal registers can be divided into two groups. A group of registers to control all the general functions and settings of the device, and a bank of registers to control the TGC/gain curves operation. Those two sets of registers overlap in all the address space, except for the address 0 which holds the control of the register bank. One of the bits of this register, TGC_REG_WREN (see table below) is used to access one set of registers or the other. Its default value is zero and gives access to the general purpose registers. The TGC control registers (described after the general purpose registers) can be accessed by writing '1' to TGC_REG_WREN.

The following table describes the function of the general purpose registers (when TGC_REGISTER_WREN is zero, default). The address format is "address[bit of the register]":

ADDRESS	FUNCTION	DESCRIPTION
0[2]	TGC_REGISTER_WREN	0: Access to general-purpose registers. 1: Access to TGC registers
0[1]	REGISTER_READOUT_ENABLE	1: Enables readout of the registers
0[0]	SOFTWARE_RESET	1: Resets the device and self-resets the bit to zero
1[13]	EXTERNAL_REFERENCE	0: Internal reference. 1: External reference
1[11]	LOW_FREQUENCY_NOISE_SUPRESSION	0: No suppression. 1: Suppresses noise at low frequencies and pushes it to $f_{channel}/2$
1[10]	STDBY	0: Power up. 1: Standby (fast power-up mode)
1[9:2]	PDN CHANNEL<7:0>	PDN for each individual channel (VCA+ADC). LVDS outputs logic 0.
1[1]	OUTPUT_DISABLE	0: Output enabled. 1: Output disabled
1[0]	GLOBAL_PDN	0: Power up. 1: Global power down (slow power-up mode)
2[15:13]	PATTERN_MODE	Pattern modes for serial LVDS. 000: No pattern. 001: Sync. 010: Deskew. 011: Custom reg. 100: All 1s. 101: toggle. 110: All 0s. 111: Ramp
2[11]	AVERAGING_ENABLE	0: Default (no averaging). 1: Average two channels to increase SNR.
2[10:3]	PDN_LVDS	Power down the eight data-output LVDS pairs.
3[14:13]	SERIALIZED_DATA_RATE	Serialization factor. 00: 12×. 01: 10×. 10: 16×. 11: 14×
3[12]	DIGITAL_GAIN_ENABLE	0: Default (no gain). 1: Apply digital gain set by the following registers.
3[8]	REGISTER_OFFSET_SUBTRACTION_ENABLE	0: Default (no subtraction). 1: Subtract offset value set in the corresponding registers.
4[3]	DFS	Data format select. 0: 2s complement. 1: Offset binary
5[13:0]	CUSTOM_PATTERN	Custom pattern data for LVDS (PATTERN_MODE = 011)
7[10]	VCA_LOW_NOISE_MODE_(INCREASE_POWER)	0: Low power. 1: Low noise, at the expense of increased power (5mW per channel)
7[8:7]	SELF_TEST	00, 10: No self-test. 01: Self-test enabled. 100 mV DC applied to the input of the channels. 11: Self-test enabled. 150 mV DC applied to the input of the channels.
7[3:2]	FILTER_BW	00: 14MHz. 01: 10MHz. 10: 7.5MHz. 11: Not used.
7[1]	INTERNAL_AC_COUPLING	VGA coupling. 0: AC-coupled. 1: DC-coupled
13[15:11]	DIG_GAIN1	0dB to 6dB in steps of 0.2dB
13[9:2]	OFFSET_CH1	Value to be subtracted from channel 1
14[15:11]	DIG_GAIN2	0dB to 6dB in steps of 0.2dB

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ADDRESS	FUNCTION	DESCRIPTION
14[9:2]	OFFSET_CH2	Value to be subtracted from channel 2
15[15:11]	DIG_GAIN3	0dB to 6dB in steps of 0.2dB
15[9:2]	OFFSET_CH3	Value to be subtracted from channel 3
16[15:11]	DIG_GAIN4	0dB to 6dB in steps of 0.2dB
16[9:2]	OFFSET_CH4	Value to be subtracted from channel 4
17[15:11]	DIG_GAIN5	0dB to 6dB in steps of 0.2dB
17[9:2]	OFFSET_CH5	Value to be subtracted from channel 5
18[15:11]	DIG_GAIN6	0dB to 6dB in steps of 0.2dB
18[9:2]	OFFSET_CH6	Value to be subtracted from channel 6
19[15:11]	DIG_GAIN7	0dB to 6dB in steps of 0.2dB
19[9:2]	OFFSET_CH7	Value to be subtracted from channel 7
20[15:11]	DIG_GAIN8	0dB to 6dB in steps of 0.2dB
20[9:2]	OFFSET_CH8	Value to be subtracted from channel 8
21[4:1]	DIGITAL_HIGH_PASS_FILTER_CORNER_FREQ_FOR_CHANNELS-1–4	Sets k for the high-pass filter as described in *General-Purpose Register Description* (k from 2 to 10).
21[0]	DIGITAL_HIGH_PASS_FILTER_ENABLE_FOR_CHANNELS_1–4	0: No high-pass filter. 1: High-pass filter enabled
25[15:11]	DIG_GAIN15	0dB to 6dB in steps of 0.2dB
25[9:2]	OFFSET_CH15	Value to be subtracted from channel 16
26[15:11]	DIG_GAIN16	0dB to 6dB in steps of 0.2dB
26[9:2]	OFFSET_CH16	Value to be subtracted from channel 15
27[15:11]	DIG_GAIN13	0dB to 6dB in steps of 0.2dB
27[9:2]	OFFSET_CH13	Value to be subtracted from channel 14
28[15:11]	DIG_GAIN14	0dB to 6dB in steps of 0.2dB
28[9:2]	OFFSET_CH14	Value to be subtracted from channel 13
29[15:11]	DIG_GAIN11	0dB to 6dB in steps of 0.2dB
29[9:2]	OFFSET_CH11	Value to be subtracted from channel 12
30[15:11]	DIG_GAIN12	0dB to 6dB in steps of 0.2dB
30[9:2]	OFFSET_CH12	Value to be subtracted from channel 11
31[15:11]	DIG_GAIN9	0dB to 6dB in steps of 0.2dB
31[9:2]	OFFSET_CH9	Value to be subtracted from channel 10
32[15:11]	DIG_GAIN10	0dB to 6dB in steps of 0.2dB
32[9:2]	OFFSET_CH10	Value to be subtracted from channel 9
33[4:1]	DIGITAL_HIGH_PASS_FILTER_CORNER_FREQ_FOR_CHANNELS_5–8	Sets k for the high-pass filter as described in *General-Purpose Register Description* (k from 2 to 10).
33[0]	DIGITAL_HIGH_PASS_FILTER_ENABLE_FOR_CHANNELS_5–8	0: No high-pass filter. 1: High-pass filter enabled
70[14]	CLAMP_DISABLE	0: Enabled. 1: Disabled

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General Purpose Register Description

AVERAGING_ENABLE

Address: 2[11]

When set to one, two samples, corresponding to two different channels on the same pair, are averaged (channel 1 with 3, 2 with 4, 5 with 7, 6 with 8, 9 with 11, 10 with 12, 13 with 15 and 14 with 16). If both channels receive the same input, the net effect is an improvement on SNR. The averaging is performed as:

1. Channel 1 with channel 3 comes out on channel 3 LVDS pair, followed by the average of channels 2 and 4 (on the same pair).
2. Channel 5 with channel 7 comes out on channel 4 LVDS pair, followed by the average of channels 6 and 8 (on the same pair).
3. Channel 9 with channel 11 comes out on channel 5 LVDS pair, followed by the average of channels 10 and 12 (on the same pair).
4. Channel 13 with channel 15 comes out on channel 6 LVDS pair, followed by the average of channels 14 and 16 (on the same pair).

CUSTOM_PATTERN

Address: 5[13:0]

This register stores the code that will be output when PATTERN_MODE equal to '011'. See PATTERN_MODE for more details.

DFS

Address: 4[3]

DFS stands for Data Format Select. The ADC output, by default, is in 2s complement mode. Programming the DFS bit to '1' inverts the MSB, and the output becomes straight offset binary mode.

DIGITAL_GAIN_ENABLE

Address: 3[12]

Setting this bit to ‘1’ applies to each channel I the corresponding gain given by DIG_GAIN_i<15:11>. The gain is given as 0dB+0.2dB*DIG_GAIN_i<15:11>. For instance, if DIG_GAIN_5<15:11>=3, channel 5 is increased by 0.6dB gain. DIG_GAIN_i<15:11>=31 produces the same effect as DIG_GAIN_i<15:11>=30 setting the gain of channel i to 6dB.

DIGITAL_HIGH_PASS_FILTER and DIGITAL_HIGH_PASS_FILTER_CORNER_FREQ

Address: 21[0]

Address: 33[0]

Address: 21[4:1]

Address: 33[4:1]

This group of 4 registers controls the characteristics of a digital high pass transfer function applied to the output data, following the formula: y(n)= 2^k/(2^k +1) [x(n) –x(n–1) + y(n–1)]. K is set as described by the DIGITAL_HIGH_PASS_FILTER_CORNER_FREQ registers (one for the first 8 channels and one for the second group of 8 channels).

EXTERNAL_REFERENCE

Address: 1[13]

Internal reference mode (default) uses approximately 3mW more power on AVDD (already included in all the specification tables). The AFE5851 can operate in external reference mode by programming EXTERNAL_REFERENCE to '1'. In this mode, drive the VREF_IN pin with 1.4V. Due to the high input impedance of this pin, no special drive capabilities are required. The advantage of using the external reference mode is that multiple AFE5851 units can be made to operate with the same external reference, thereby improving parameters such as gain matching across devices.

FILTER_BW

Address: 7[3:2]

This bit sets the 3dB attenuation frequency for the anti-aliasing filter (AAF).

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GLOBAL_PDN

Address: 1[0]

The Global PDN bit is ORed with the signal in the external PDN pin (59). Hereby, a '1' on this bit shuts down the device completely.

INTERNAL_AC_COUPLING

Address: 7[1]

This bit controls an internal high pass filter, Figure 31, set between the input buffer and the VCA. This filter removes the input offset to avoid its amplification by the TGC. An alternative method is to remove the offset effect on the digital domain, either on the device following the ADC or at the ADC output, by using the DIGITAL HIGH PASS FILTER registers (see above).

LOW_FREQUENCY_NOISE_SUPRESSION

Address: 0[11]

low-frequency noise suppression mode is specifically useful in applications where good noise performance is desired in the frequency band of 0MHz to 1MHz (around DC). Setting this mode shifts the low-frequency noise of the ADC in the AFE5851 to approximately fchannel/2, thereby reducing the noise floor around DC to a much lower value.

OUTPUT_DISABLE

Address: 1[1]

A '1' on this bit sets the outputs into high-impedance state.

PATTERN_MODE

Address: 2[15:13]

AFE5851 can output a variety of test patterns on the LVDS outputs. These test patterns replace the normal ADC data output and help on debugging and synchronization with the device reading the output of the ADC:

1. PATTERN_MODE equal to ‘000’ is the default and disables this test mode, i.e., the output data is the same as the ADC data.
2. PATTERN_MODE equal to ‘001’ (SYNC mode) replaces the normal ADC word by a fixed 111111000000 word.
3. PATTERN_MODE equal to ‘010’ sets the DESKEW mode, where the 12-bit ADC output D<11:0> is replaced with the ‘101010101010’ word, creating a continuous stream of ones and zeros in the data line. The exact sequence (first a zero or a one) depends on power-up. This mode only ensures alternating ones and zeros at the output.
4. PATTERN_MODE equal to ‘011’ will output a constant code set by the bits in CUSTOM_PATTERN<13:0>. Depending on the value of SERIALIZED_DATA_RATE (see below) the output bits follow these rules:
   (a) On the default case, where SERIALIZED_DATA_RATE is ‘00’, for a 12-bit ADC data at the output, CUSTOM_PATTERN<13:2> would be used, replacing the sampled data. These would still be controlled by LSB-first and MSB-first modes in the same way as normal ADC data are.
   (b) For SERIALIZED_DATA_RATE= ’01’, 10-bit output mode is selected, and bits CUSTOM_PATTERN<13:4> are used.
   (c) For SERIALIZED_DATA_RATE= ’10’, 16-bit output mode is selected. On this case, CUSTOM_PATTERN<13:0> are used for the first 14 most significant bits, and two zeros take the place of the LSBs.
   (d) For SERIALIZED_DATA_RATE= ’11’, 14-bit mode is selected, and CUSTOM_PATTERN<13:0> takes the place of the output word.
5. PATTERN_MODE equal to '100’ makes it always ‘1’, while setting it to ‘110’ makes the output always ‘0’.
6. PATTERN_MODE equal to ‘101’ makes the output of the device toggle between all zeros and all ones. On the nth sample clock, the data would be ‘000000000000’ and on the following one (nth+1) it would be ‘111111111111’.
7. PATTERN_MODE equal to ‘111’ causes all the channels to output a repeating full-scale ramp pattern. The ramp increments from zero code to full-scale code in steps of 1LSB every clock cycle. After hitting the full-scale code, it returns back to zero code and ramps again.

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PDN_Channel<7:0>

Address: 1[9:2]

Each bit controls the power down of a pair of consecutive channels (that share the same ADC). For example: PDN_Channel<0> powers down channels 1 and 2 and the corresponding LVDS pair become high impedance. DCLK and FCLK are not powered down; they will be active if terminated with 100Ω.

PDN_LVDS

Address: 2[10:3]

PDN_LVDS<7..0> selects which LVDS pairs become inactive (zero output). The frame and clock LVDS streams get powerdown only when OUTPUT_DISABLE or GLOBAL_PDN are set.

REGISTER_OFFSET_SUBSTRACTION_ENABLE

Address: 3[8]

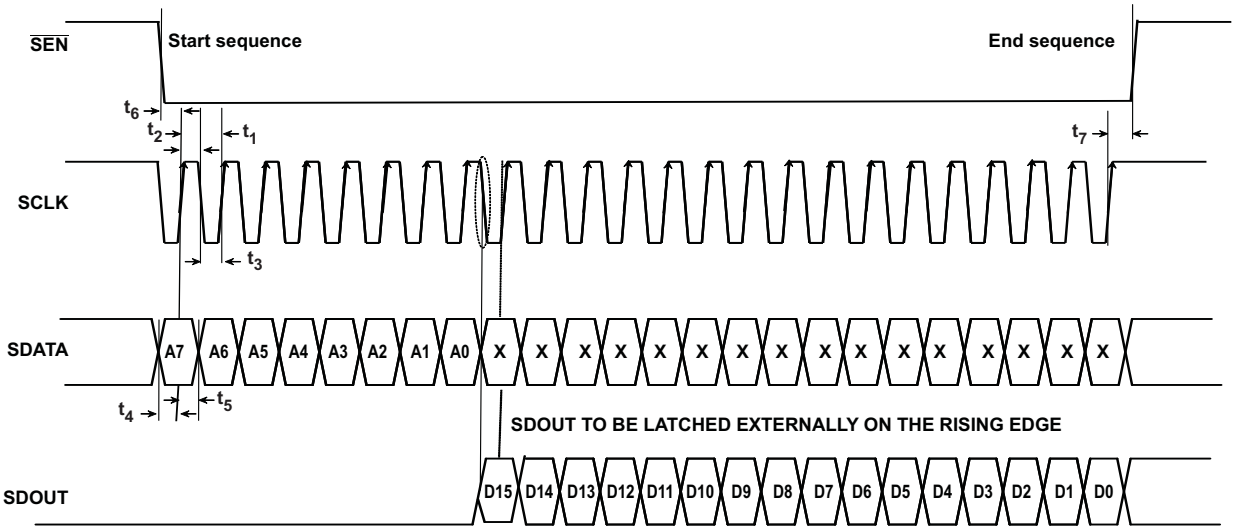
Setting this bit to '1' enables the subtraction of the value on the corresponding $OFFSET_CHANNEL_i$<9:2> from the ADC output. The number is specified in 2s complement format. For example, $OFFSET_CHANNEL_i$<9:2>='1000000' means "subtract –128". For $OFFSET_CHANNEL_i$<9:2>='01111111' the effect will be to subtract 127. Hereby, both addition and subtraction can be done.

Notice that the offset is applied before the digital gain (see next). In fact, digital gain is the last step and the whole data path is 2s complement through out internally. Only when DFS='1' (straight binary output format), the 2s complement word is translated into offset binary right at the end.

REGISTER_READOUT_ENABLE

Address:0[1]

The device includes an option where the contents of the internal registers can be read back. This may be useful as a diagnostic to verify the serial interface communication between the external controller and the AFE. First, the <REGISTER READOUT ENABLE> bit needs to be set to '1'. Then the user should initiate a serial interface cycle specifying the address of the register (A7-A0) whose content has to be read. The data bits are "don't care". The device will output the contents (D15-D0) of the selected register on the SDOUT pin. The external controller can latch the contents at the rising edge of SCLK. To enable serial register writes, set the <REGISTER READOUT ENABLE> bit back to '0'. The following timing diagram shows this operation (the time specifications follow the same information provided on the table for a serial interface register write):



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SERIALIZED_DATA_RATE

Address: 3[14:13]

These two bits control the length of the data word, i.e., the number of DCLK per FCLK periods. It is possible, for instance, to output 16bit data stream, even with a 12bit ADC. In this case, the last 4 LSBs are padded with zeros. The pass from higher resolution to lower serialization is not supported though; i.e, it is not possible to select a 10bit stream with a 12bit ADC.

TGC_REGISTER_WREN

Address: 0[2]

Set this bit to '1' to access the TGC table and '0' (default after reset) to access the general purpose register table. As explained before, the same address may point to one bank of registers or to the other. Nevertheless, observe that register 0 of the general purpose registers is always accessible, regardless of the value of TGC_REGISTER_WREN. The TGC table starts at address 1.

VCA_LOW_NOISE_MODE

Address: 7[10]

Setting this bit to '1' reduces the equivalent input noise of the channel to 5nV/√Hz (for a 31dB gain) at the expense of an increase in power consumption (5mW/channel).

TGC CONTROL REGISTER MAP

The TGC operation is described in the VGA/TGC Operation section below. This section describes the TGC control registers which can be accessed by writing '1' to TGC_REG_WREN bit. The following table describes the register map for all the registers involved in the TGC operation.

ADDRESS	D[15:7]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x01...0x94		REG_VALUES								
0x95	NOT USED	START_ INDEX								
0x96		STOP_INDEX								
0x97		INTERP ENABLE	0	START _GAIN						
0x98		HOLD_ GAIN _TIME								
0x99		0	0	SOFT SYNC	UNIFORM GAIN MODE	STATIC PGA	FINE_GAIN			
0x9A		0	0	COARSE_GAIN						
0x9B		UNIFORM_GAIN_SLOPE								

REG_VALUE

Address: 0x01[8:0] to 0x94[8:0]

Each of these 9 bit registers (148 of them) stores the time to stay at a given gain setting, during the gain ramp. The most significant bit of each register (REG_VALUE<8>) denotes either increment or decrement gain from current gain value. The other 8 bits (REG_VALUE<7:0>) denote the time (a multiple of 8 × Tclk; Tclk being the channel sampling clock, i.e., double the period of the device input clock) for the change of the gain from the CURRENT_GAIN to CURRENT_GAIN ±1dB (depending on the REG_VALUE<8>). The fastest ramp (shortest time) for this 1dB gain change is set by REG_VALUE<7:0> equal to 0x00 and it is 8 × Tclk. The slowest ramp (longest time) for this 1dB gain change is set by REG_VALUE<7:0> equal to 0xFF and it is 255 × 8 × Tclk (see VGA operation – described later).

START_INDEX

Address: 0x95[7:0]

This 8 bit register specifies/points to the first REG_VALUE register of the TGC curve (i.e., where the curve starts) and can have values ranging from 1 to 148 (in decimal).

STOP_INDEX

Address: 0x96[7:0]

This 8 bit register specifies/points to the last REG_VALUE register of the TGC curve (i.e., where the curve finishes) and can have values ranging from 1 to 148 (in decimal).

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START_GAIN

Address: 0x97[5:0]

This 6 bit register specifies the start gain value from –5dB to 31dB.

START_GAIN = [–5 + REG_VALUE] dB

REG_VALUE	GAIN
0x0	–5 dB
0x1	–4 dB
0x24	31 dB

STOP_GAIN **(Not a programmable register, it is an internally computed value)**

Case 1:

INTERP_ENABLE=1,

STOP_GAIN = START_GAIN + (STOP_INDEX -START_INDEX) – (2 * Number of decrements) + 0.875dB.

Case 2:

INTERP_ENABLE='0',

STOP_GAIN = START_GAIN + (STOP_INDEX-START_INDEX) – (2 * Number of Decrements).

HOLD_GAIN_TIME

Address: 0x98[7:0]

This 8 bit register specifies the time for holding of the STOP_GAIN, after reaching either the STOP_GAIN value as computed earlier or the maximum/minimum gain. After this time, the TGC starts stepping down to the START_GAIN value in 1dB steps every Tclk. The STOP_GAIN value is held for the following number of clocks:

HOLD_GAIN_TIME = [33 * REG_VALUE] Tclks

where Tclk is the channel sampling clock.

REG_VALUE	HOLD_GAIN_TIME
0x0	0 Tclks
0x1	33 Tclks
0xFF	8415 Tclks

INTERP_ENABLE

Address: 0x97[7]

This 8 bit register sets the ramp rate. When INTERP_ENABLE='1' the ramp rate is 0.125dB for every number of clocks stored in REG_VALUE:

REG_VALUE	SLOPE
0x0	0.125dB per Tclk
0x1	0.125dB per Tclk
0x2	0.125dB per 2*Tclk
0xFF	0.125dB per 255*Tclk

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When INTERP_ENABLE='0' the ramp rate is 1dB for every 8 times the number of clocks stored in REG_VALUE:

REG_VALUE	SLOPE
0x0	1dB per 8 × Tclk
0x1	1dB per 8 × Tclk
0x2	1dB per 16 × Tclk
0xFF	1dB per 255× 8 × Tclk

SOFT_SYNC

Address 0x99[5]

Setting SOFT_SYNC bit to '1' enables the TGC engine to run periodically following a given TGC curve, without the need for a high pulse signal in the SYNC pin (see more details below).

UNIFORM_GAIN_MODE

Address 0x99[4]

Setting this bit to '0' (default) directs the TGC engine to follow an arbitrary gain versus time curve. If this bit to '1' the gain is ramped up with a slope set by the UNIFORM_GAIN_SLOPE register. (See more details below)

UNIFORM_GAIN_SLOPE

Address 0x9B[7:0]

See Uniform Gain Increment Mode section below.

STATIC_PGA

Address 0x99[3]

Setting this bit to '1' disables the TGC engine. COARSE_GAIN and FINE_GAIN will control the gain value, which will be independent of time.

COARSE_GAIN

Address 0x9A[5:0]

This 6 bit register specifies the coarse gain from –5 to 31dB, in 1dB steps. Observe that only values from 0x00 to 0x24, both included, are valid. Setting a value bigger than 0x24 on the COARSE_GAIN register is the same as setting 0x24. COARSE_GAIN = [–5 + REG_VALUE] dB

REG_VALUE	GAIN
0x0	–5dB
0x1	–4dB
0x24	31dB

FINE_GAIN

Address 0x99[2:0]

This 3 bit register specifies the fine gain in steps of 0.125dB resolution, from 0dB to 0.875dB. FINE_GAIN = [0.125 × REG_VALUE] dB

REG_VALUE	GAIN
0x0	0dB
0x1	0.125dB
0x7	0.875dB

VGA/TGC OPERATION

The gain variation of the variable gain amplifier (VGA) versus time is called TGC function and on the AFE5851 is controlled digitally. The gain is implemented by a switched network where the switches controlling the gain are synchronized with the ADC sampling instant to minimize glitches on the output data. The gain setting depends on the mode of operation selected by the user. There are 3 possible modes of operation: non-uniform gain, uniform gain, and static mode. The following sections describe each in detail.

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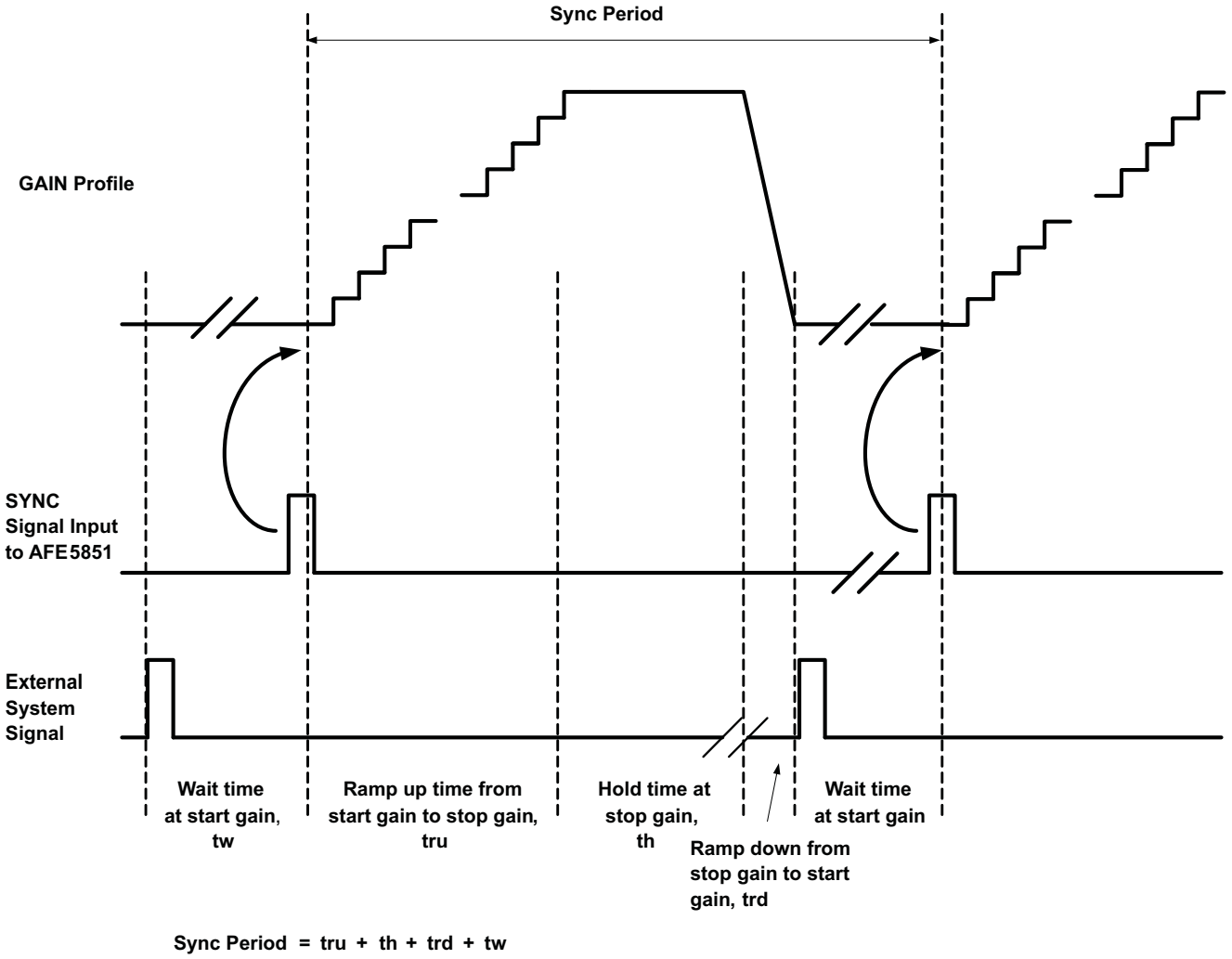


Figure 34. SYNC Period

Non-Uniform Gain Increment Mode

In the non-uniform gain increment mode, the user sets an arbitrary shape for the gain versus time curve. For a given time/sampling instant, the digital gain setting is obtained from an internal memory of 148 positions/registers (named REG_VALUEs), each 9 bits wide, loaded by the user through the serial port (see Serial Interface section). Addresses 1 to 148 can be used to access these registers, while TGC_REGISTER_WREN='1'.

As explained above, the most significant bit of each register (REG_VALUE<8>) denotes either increment or decrement gain from current gain value. The other 8 bits (REG_VALUE<7:0>) denote the time (a multiple of 8*Tclk, being Tclk the sampling clock) for the change of the gain from the CURRENT_GAIN to CURRENT_GAIN ±1dB (depending on the REG_VALUE<8>). The fastest ramp (shortest time) for this 1dB gain change is set by REG_VALUE<7:0> equal to 0x00 and it is 8 × Tclk. The slowest ramp (longest time) for this 1dB gain change is set by REG_VALUE<7:0> equal to 0xFF and it is 255 × 8 × Tclk.

INTERP_ENABLE sets the way the gain is increased/decreased. By default the gain ramp is implemented in steps of 1dB (INTERP_ENABLE equal to 0). If INTERP_ENABLE is equal to 1, the actual 1dB gain step is implemented in 8 steps of 0.125dB.

The 148 REG_VALUE registers can be used to store either a single curve or multiple TGC curves. The START_INDEX register points to the REG_VALUE register where the TGC curve starts and the STOP_INDEX register points to the REG_VALUE register where the TGC curve stops. Using the START_INDEX and STOP_INDEX registers the desired TGC curves can be chosen.

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As shown in Figure 34, a pulse high signal on the SYNC pin will set the starting gain value of the TGC curve to the START_GAIN register value, and it will initiate the progression through the different REG_VALUEs, starting at START_INDEX. Observe that there is no option to delay the start of gain stepping after the SYNC pulse is received. Then, the progression continues until either the STOP_INDEX is reached or maximum/minimum gain is exceeded. After that, the last valid value of gain is held for an extra given number of clocks set by the register HOLD_GAIN_TIME.

After the elapsing of clocks mentioned by the HOLD_GAIN_TIME register, the TGC starts to step down (or up) to the START_GAIN in steps of 1dB every Tclk (channel sampling clock) in preparation for the next TGC profile. The TGC will start updating/following the REG_VALUEs again after a new high pulse on the SYNC pin is given.

The SYNC signal is latched by the rising edge of the channel sampling clock. In other words, the gain increments at the rising edge of the channel sampling clock. Setup time with rising edge is 7ns, and hold time 4ns.

SOFT_SYNC

The TGC can run periodically following a given TGC curve but without the need for a high pulse signal in the SYNC pin. This is done by setting SOFT_SYNC bit to '1'. Once this bit is set, the sequence of events is the same as with the hardwired SYNC pulse. The TGC curve updates from START_INDEX to STOP_INDEX. After reaching STOP_INDEX or the maximum/minimum gain, the STOP_GAIN value is held for HOLD_VALUE_TIME and then the gain ramps up or down to START_GAIN. After this the TGC update starts again automatically and repeats all these steps periodically till the SOFT_SYNC bit becomes zero.

The SYNC process through register write occurs at the serial clock edge where the register is written. If serial clock and sample clock (channel sampling clock) are synchronous then the described relation in the hardwired SYNC section will hold and the SYNC bit is latched by the rising edge of the channel sampling clock, respecting a setup time with rising edge of 7ns and hold time of 4ns. If sample clock and serial clock are not synchronous then this relationship does not apply and a clock uncertainty of ±1 sample will apply in respect to the nearest sample clock rising edge.

Example 1: In the following example of non-uniform gain mode, all the 148 registers are loaded. Nevertheless, the start address for the TGC is set in START_INDEX to 2 and the stop address (STOP_INDEX) to 7. The START_GAIN is set to 6 and HOLD_GAIN_TIME is 4.

With a high pulse on the SYNC pin the gain starts from 1dB (START_GAIN=0x06). 1dB to 2dB ramp is done in 120Tclks, using eight 0.125dB steps (as INTERP_ENABLE is set to 1), each 15Tclks long. The ramp from 2dB to 3dB is done in 64Tclks, also in 0.125dB steps. The ramp from 3dB to 4dB is done in 40 Tclks. Decrement from 4dB to 3dB in 64Tclks. Gain increment from 3dB to 4dB in 56 Tclks and from 4dB to 4.875dB in 80 Tclks.

Observe that in the case where INTERP_ENABLE=1, STOP_GAIN = START_GAIN + (STOP_INDEX -START_INDEX) – (2 × Number of decrements) + 0.875dB. In the case where INTERP_ENABLE='0', STOP_GAIN = START_GAIN + (STOP_INDEX-START_INDEX) – (2 × Number of Decrements). This is due to the fact that the interpolation engine keeps the gain increasing or decreasing when INTERP_ENABLE=1, while the gain is frozen when INTERP_ENABLE=0.

TGC REG INDEX	REG_VALUE[8:0]	Number of Tclks	Direction of Gain Change
1	0x004	4 × 8 = 32	Increment
2	0x00F	15 × 8 = 120	Increment
3	0x008	8 × 8 = 64	Increment
4	0x005	5 × 8 40	Increment
5	0x108	8 × 8 = 64	Decrement
6	0x007	7 × 8 = 56	Increment
7	0x00A	10 × 8 = 80	Increment
...	...	...	...
147	0x00F	15 × 8 = 120	Increment
148	0x00F	15 × 8 = 120	Increment

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NAME	VALUE
START_INDEX	0x02
STOP_INDEX	0x07
START_GAIN	0x06
HOLD_GAIN_TIME	0x04
INTERP_ENABLE	1
UNIFORM_GAIN_MODE	0

Uniform Gain Increment Mode

By setting UNIFORM_GAIN_MODE to '1', the TGC engine can also be configured for a uniform increment gain ramp mode where the gain is ramped up from the START_GAIN value to the STOP_GAIN with a slope set by the UNIFORM_GAIN_SLOPE register. Note: STOP_GAIN is not a programmable register, but just an internally computed value from START_GAIN, UNIFORM_GAIN_SLOPE, START_INDEX and STOP_INDEX.

If INTERP_ENABLE=1, UNIFORM_GAIN_SLOPE sets the number of Tclk (channel sampling clock) at a given gain before incrementing or decrementing 0.125dB. If INTERP_ENABLE=0, this register sets the number of 8*Tclk (eight sampling periods) at a given gain before incrementing or decrementing 1dB. Observe that in both cases the time it takes to step by 1dB is the same. In INTERP_ENABLE=0 the gain is stationary at the same setting for the given time, while in the other case the gain increments in fine gain steps of 0.125dB to cover that 1dB step

When INTERP_ENABLE is zero, the STOP_GAIN is computed as START_GAIN + (STOP_INDEX-START_INDEX). Nevertheless, when INTERP_ENABLE = '1', the STOP_GAIN is equal to START_GAIN + (STOP_INDEX - START_INDEX) + 0.875dB. This is basically due to the fact that the interpolation engine keeps the gain increasing on the second case, while, as explained above, is frozen on the first case. Observe that START_INDEX and STOP_INDEX are not used in this case as pointers to the REG_VALUEs table. Instead, only the difference between the two is important to compute STOP_GAIN. As such, START_INDEX can be set to zero and STOP_INDEX will store STOP_GAIN – START_GAIN. Observe that only positive slope ramps are possible.

Example 1: setting START_GAIN=0x2 (–3dB), START_INDEX=0x00, STOP_INDEX=0x06, INTERP_ENABLE=0 and UNIFORM_GAIN_SLOPE=0x8, will set the gain at –3dB for 8 × 8 × Tclk, then to –2dB for another 64 Tclk, and so on, through –1, 0, 1, 2 and 3. After spending 64 × Tclk in 3dB, the gain will stay at that gain setting for HOLD_GAIN_TIME and start stepping down back to START_GAIN, with 1dB per Tclk.

Example 2: for the same settings, START_GAIN=0x2 (–3dB), START_INDEX=0x00, STOP_INDEX=0x06, and UNIFORM_GAIN_SLOPE=0x8, if we set INTERP_ENABLE=1, the gain will start at –3dB for 8Tclk, then –2.875dB for another 8Tclk, then –2.750dB and so on, till 3dB. At this point, while in example 1, with INTERP_ENABLE=0 the gain would be frozen for another 64 Tclk, in this example, the gain will continue to increase with 0.125dB steps every 8Tclk till 3.875dB is reached. There will stay for another 8Tclk before starting to wait for HOLD_GAIN_TIME and start stepping down.

Example 3: for START_GAIN=0x2(–3dB) , START_INDEX=0x00, STOP_INDEX=0x00, INTERP_ENABLE=1 and UNIFORM_GAIN_SLOPE=0x1, the gain will step through –3dB, –2.875, –2.75, –2.625, –2.5, –2.375, –2.25 and –2.125, staying at each of these 8 values 1 clock cycle (8 total). Then it will wait for HOLD_GAIN_TIME in –2.125dB and then it will start stepping down back to –3dB.

Example 4: same settings as example 3, but with INTERP_ENABLE=0, would simply set the VGA gain to –3dB for 8 clock cycles and then the logic would wait for HOLD_GAIN_TIME.

Static PGA Mode

The 3rd mode of operation is actually a mode where the TGC engine is disabled by writing '1' into the STATIC_PGA bit. This enables the use of a fixed gain mode where the gain is obtained by the sum of a coarse and a fine gain. Coarse gain can be set from –5 to 31dB, in 1dB steps, by the register COARSE_GAIN (6 bit word from 0x00 to 0x24). Setting a value bigger than 0x24 on the COARSE_GAIN register is the same as setting 0x24. The fine gain can be set in steps of 0.125dB resolution, from 0dB to 0.875dB by the FINE_GAIN register (3 bit word with range from 0x00 to 0x07). Observe that the maximum gain, when both registers are set to their maximum gains, is actually 31.875dB.

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ANTI ALIAS FILTER (AAF)

The AFE5851 integrates a selectable 3 order low pass filter for each of the 16 channels. The cutoff frequency can be set for all the channels simultaneously through the serial interface (see FILTER_BW register, in the General Purpose Register table) between 3 possible settings: 7.5, 10 and 14MHz. Figure 19 shows the frequency response for each of these settings. The filter characteristics are set by passive components which are subject to variations over process and temperature. A typical variation of ±5% on the frequency characteristics is expected.

CLAMPING CIRCUIT AND OVERLOAD RECOVERY

The AFE5851 is designed in particular for ultrasound applications where the front-end device is required to recover very quickly from an overload condition. Such overload can either be the result of a transmit pulse feed-through or a strong echo, which can cause overload of the VGA and ADC.

Enabled by default, the AFE5851 includes a clamping circuit to further optimize the overload recovery behavior of the complete channel (see Figure 31). The circuit can be disabled by writing a '1' in the bit 14 of the address 70 (decimal) of the General Purpose Register Map. The clamp is set to limit the signal at 3dB above the full scale of the ADC (2Vpp).

CLOCK INPUTS

The 16 channels on the device operate from a single clock input. To ensure that the aperture delay and jitter are the same for all channels, the AFE5851 uses a clock tree network to generate individual sampling clocks to each channel. The clock channels for all the channels are matched from the source point to the sampling circuit of each of the eight internal ADCs. The variation on this delay is described in the Aperture Delay parameter of the Output Interface Timing. Its variation over time is described in the Aperture Jitter number of the same table. Observe that the rising edges of the input clock are used to sample the even channels in one input clock period and the odd channels in the next. Using an input clock double the speed of the channel sampling clock ensures that the sampling instant between even and odd channels is exactly an input clock period apart and does not depend on its duty cycle..

The AFE5851 clock input can be driven differentially (sinewave, LVPECL or LVDS) or single-ended (LVCMOS). The clock input of the device has an internal buffer/clock amplifier (see Figure 35) which is enabled or disabled automatically depending on the type of clock provided (autodetect feature). When enabled, the device will consume 6mW more power from the AVDD18 supply rail, but it will also accept differential or single ended inputs of smaller swing.

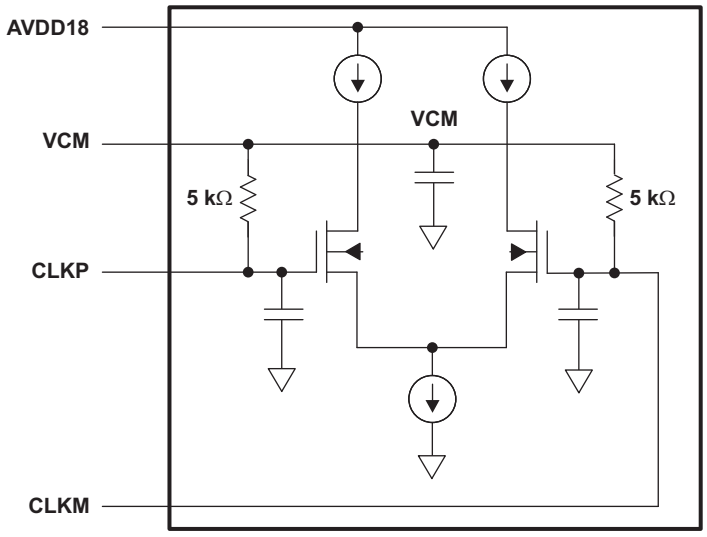


Figure 35. Internal Clock Buffer for Differential Clock Mode

If the preferred clocking scheme for the device is single-ended, CLKINM pin should be connected to ground, i.e., shorted directly to AVSS (see Figure 37). In this case, the autodetect feature will shut down the internal clock buffer and the device will go into single-ended clock input automatically. The user should connect the single-ended clock source directly (no decoupling) to CLKINP pin, which would be the only device clock input. In that case, it is recommended the use of low jitter square signals (LVCMOS levels, 1.8V amplitude) to drive the ADC (see SLYT075 for further details on the theory).

For single ended sinusoidal clocks or for differential clocks (differential sinewave, LVPECL, LVDS…), the clock amplifier should be enabled. For that, the connection scheme of Figure 36 should be used. The common-mode voltage of the clock source should match one of the clock inputs of the AFE5851 (VCM) which is set internally using 5kΩ resistors, as shown in Figure 35. The easiest way to ensure this is to AC couple the inputs as shown in Figure 36. The same scheme applies to the case where the clock is single ended but its amplitude is small or its edges are not sharp (for instance, with a sinusoidal single-ended clock). In this case, the input clock signal can be connected with a capacitor to CLKINP (as in Figure 36) and the CLKINM should be connected to ground also through a capacitor, i.e., AC coupled to AVSS.

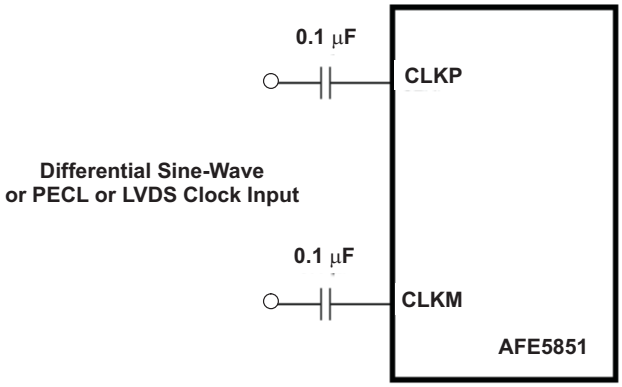


Figure 36. Differential Clock Driving Circuit

If a transformer is used with the secondary floating (for instance, to pass from single-ended to differential) , it can then obviously be connected directly to the clock inputs, without the need of the 100nF series capacitors.

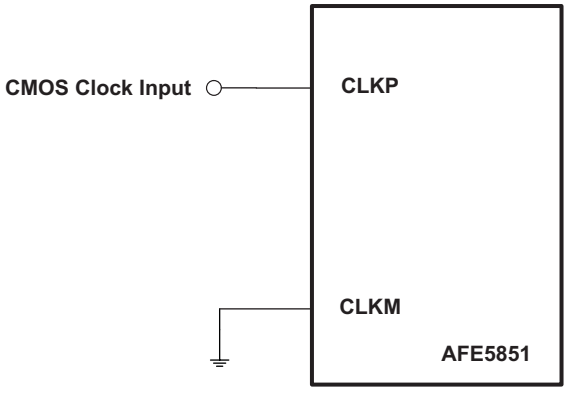


Figure 37. Single-Ended Clock Driving Circuit

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Finally, on the differential clock configurations, Figure 38 shows the use of the CDCM7005 to generate the AFE5851 clock signals.

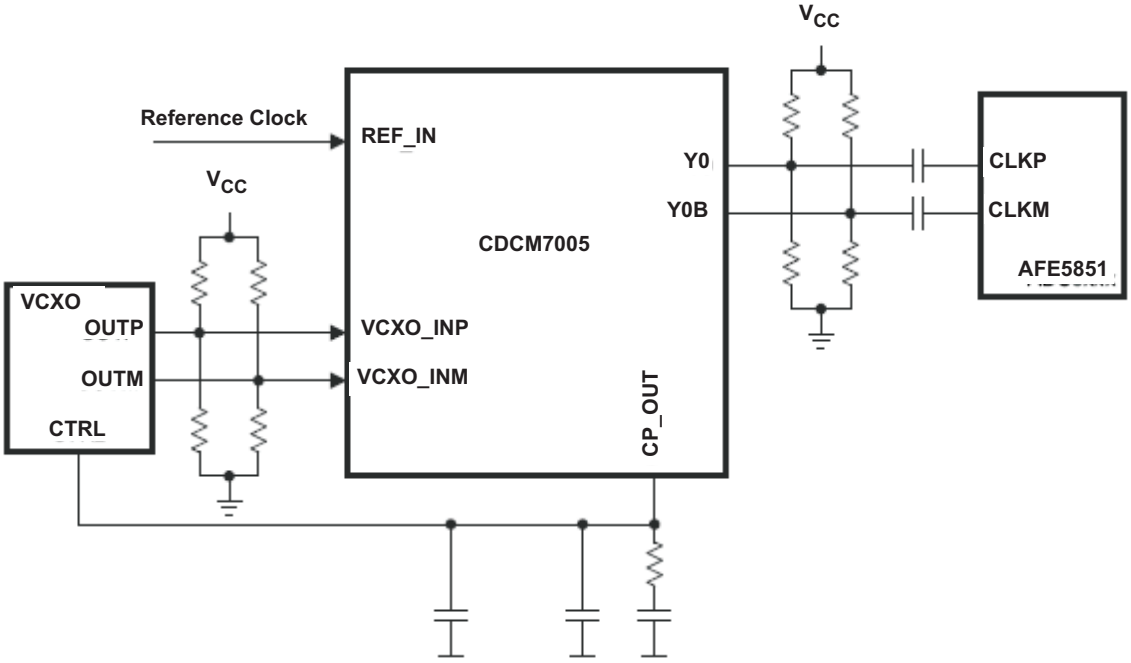


Figure 38. PECL Clock Drive Using CDCM7005

DIGITAL OUTPUTS

The conversion results from all 8 ADCs are serialized and output using one LVDS data pair per ADC, at 12 times the device input clock rate. Besides that, two more LVDS pairs are used to facilitate the interface to the circuit reading the ADC output. For one side, a reference frame LVDS signal running at the channel rate (half the input clock rate) indicates the beginning and end of the sample word. On top of that, the device outputs a reference clock running at 6 times the input clock rate, with rise and fall times aligned with the individual bits. See the Output Interface Timing section for a description of the timing diagram as well as details on the timing margins.

Figure 39 represents the device LVDS output circuit. Observe that for an LVDS output high (OUTP=1.375V, OUTM=1.025V) the "high" switches would be closed and the “low” switches would be open. For LVDS output low (OUTP=1.025V, OUTM=1.375V) the “low” switches would be closed and the “high” left open. As the “high” and “low” switches have a nominal R_{ON} of 50Ω ±10%, notice that the output impedance will be nominally 100Ω in any of those two configurations (“high” or “low” switches closed).

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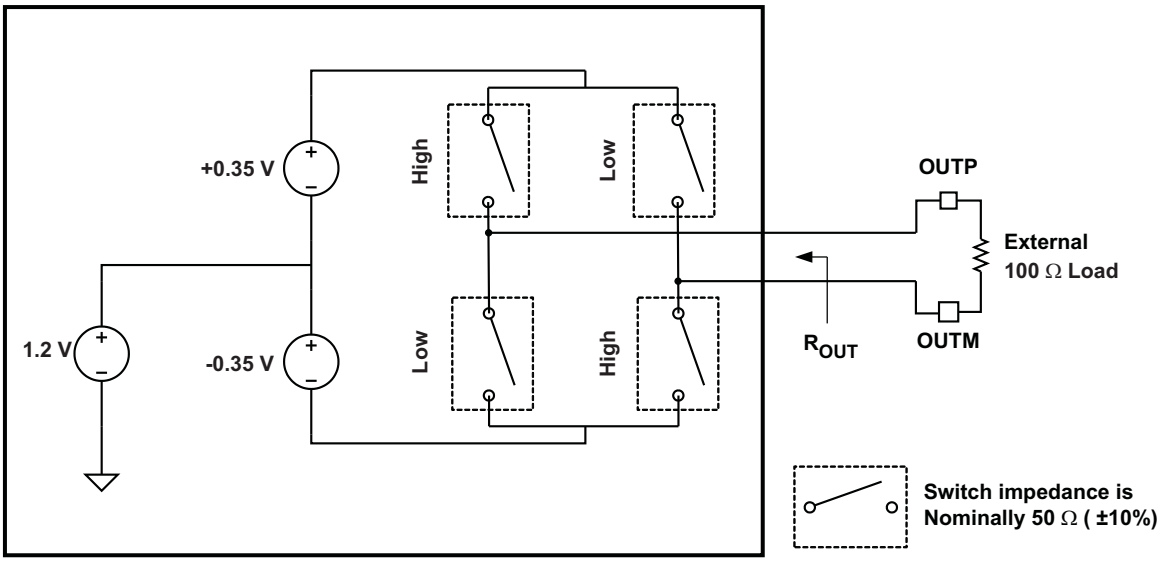


Figure 39. LVDS Output Circuit

EXTERNAL/INTERNAL REFERENCE

See EXTERNAL_REFERENCE register description in the General Purpose Register Description Section.

POWER SUPPLIES

The use of low noise power supplies with adequate decoupling is recommended, being the linear supplies the first choice vs switched ones, which tend to generate more noise components that can be coupled to the AFE5851.

There is no need of any type of power-up sequencing, although a positive pulse must be applied to the Reset pin once the power supplies are considered stable (see Serial Interface Section)

There are several types of powerdown modes. On the standby mode all circuits but the reference generator are powered-down. This enables for a fast recovery from power down to full operation. On the full power down mode, all the blocks are powered down (except some digital circuits). The power savings are bigger but the power-up will also be slower (see specification tables for more details). The device includes also the possibility of powering down pairs of channels (corresponding to the same ADC) through the use of PDN_Channel<7:0> and powering down the LVDS outputs by using PDN_LVDS.

Finally, notice that the metallic heat sink under the package is also connected to analog ground.

LAYOUT INFORMATION

The evaluation board represents a good guideline of how to layout the board to obtain the maximum performance out of the AFE5851. General design rules as the use of multilayer boards, single ground plane for both, analog and digital ADC ground connections, and local decoupling ceramic chip capacitors should be applied. The input traces should be isolated from any external source of interference or noise, including the digital outputs as well as the clock traces. Clock should also be isolated from other signals although the low frequencies of the input signal relaxes the jitter requirements.

In order to maintain proper LVDS timing, all LVDS traces should follow a controlled impedance design (for example, 100Ω differential). In addition, all LVDS trace lengths should be equal and symmetrical. It is recommended to keep trace length variations less than 150mil (0.150in or 3.81mm).

It is necessary to solder the exposed pad at the bottom of the package to a ground plane for best thermal performance. For detailed information, see application notes QFN Layout Guidelines (SLOA122A) and QFN/SON PCB Attachment (SLUA271A).

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DEFINITION OF SPECIFICATIONS

Analog Bandwidth – The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low frequency value.

Aperture Delay –The delay in time between the rising or the falling edge of the input sampling clock (depending on the channel) and the actual time at which the sampling occurs. This delay will be different across channels. The maximum variation is specified as aperture delay variation (channel-channel).

Aperture Uncertainty (Jitter) – The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle – The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Conversion Rate – The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate – The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL) – An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL) – The INL is the deviation of the ADC's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error – The difference between the actual gain of a channel & its ideal (theoretical) gain, i.e., the error in the absolute gain of the channel.

Gain Matching – The gain difference between two channels with same theoretical gain setting. For perfect matching, the difference should be zero. On the context of this device, the gain matching is obtained in two different ways:

1. The values on the specification table represent the expected gain matching between any two channels on the system. The gain is measured on every channel of every device, for a given gain setting, at any temperature. The difference between the maximum recorded gain and the minimum recorded gain represents the gain matching at that given gain setting. The same is done for every gain setting and the maximum difference for any gain setting is presented on the table.
2. The gain matching histogram represents the channel to channel matching inside the same device, i.e., the maximum expected gain difference between any two channels of the same device, or in other words, the peak-to-peak variation of absolute gains across all channels in the device. At a given gain setting for all the channels of a given device (at one temperature assumed common to the whole device), the difference between the channel with maximum gain and the channel with minimum gain represents one count. The same thing is done for all the devices and for 3 temperatures (–40C, 25C and 85C). Every measurement of a device at one given temperature represents one count.

Offset Error – The offset error is the difference, given in mV, between the ADC's actual average idle channel output code and the ideal average idle channel output code.

Temperature Drift – The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. It is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference $T_{MAX}–T_{MIN}$.

Signal-to-Noise Ratio – SNR is the ratio of the power of the fundamental (PS) to the noise floor power (PN), excluding the power at DC and the first nine harmonics.

$$SNR = 10Log10\frac{P_S}{P_N} \quad (1)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Signal-to-Noise and Distortion (SINAD) – SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

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$$SINAD = 10 \log 10 \frac{P_S}{P_N + P_D} \quad (2)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Effective Number of Bits (ENOB) – The ENOB is a measure of a converter's performance as compared to the theoretical limit based on quantization noise.

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (3)$$

Spurious Free Dynamic Range (SFDR) – SFDR is the ratio of the power of the fundamental (PS) to the highest FFT bin, harmonic or not, excluding DC. SFDR is typically given in units of dBc (dB to carrier).

Second Harmonic Distortion (HD2) – HD2 is the ratio of the power of the fundamental (PS) to the second harmonic, typically given in units of dBc (dB to carrier).

Third Harmonic Distortion (HD3) –HD3 is the ratio of the power of the fundamental (PS) to the third harmonic, typically given in units of dBc (dB to carrier).

Total Harmonic Distortion (THD) – THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics (PD).

$$THD = 10 \log 10 \frac{P_S}{P_D} \quad (4)$$

THD is typically given in units of dBc (dB to carrier).

AC Power Supply Rejection Ratio (AC PSRR) – A measure of the device immunity to variations in its supply voltage. In this datasheet, if ΔVSUP represents the change in supply voltage and ΔVOUT is the resultant change of the ADC output code (referred to the input), then:

$$PSRR = 20 \log \left(\frac{\Delta Vout}{\Delta Vsup} \right) \quad (5)$$

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REVISION HISTORY

NOTE: Page numbers of current version may differ from previou versions.

Changes from Original (September 2008) to Revision A **Page**

- Changed document status from Product Preview to Production Data 1

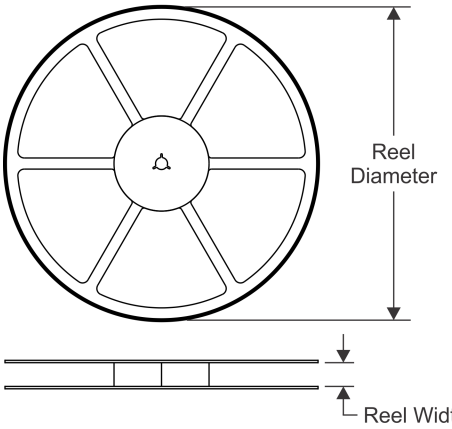
Changes from Revision A (March 2009) to Revision B **Page**

- Deleted Registers 3[7:0] INVERT CHANNEL and 4[4] MSB_FIRST from General Purpose Register Map 18
- Deleted description for Registers 3[7:0] INVERT_CHANNEL; and, 4[4] MSB_FIRST 21

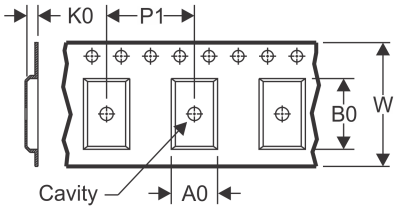
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

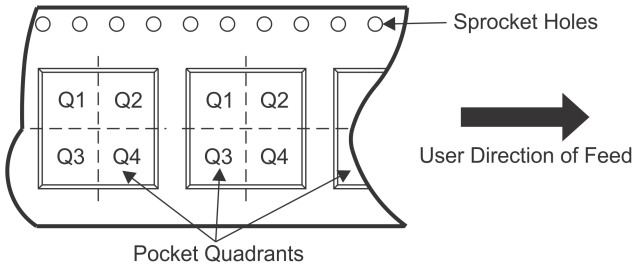


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

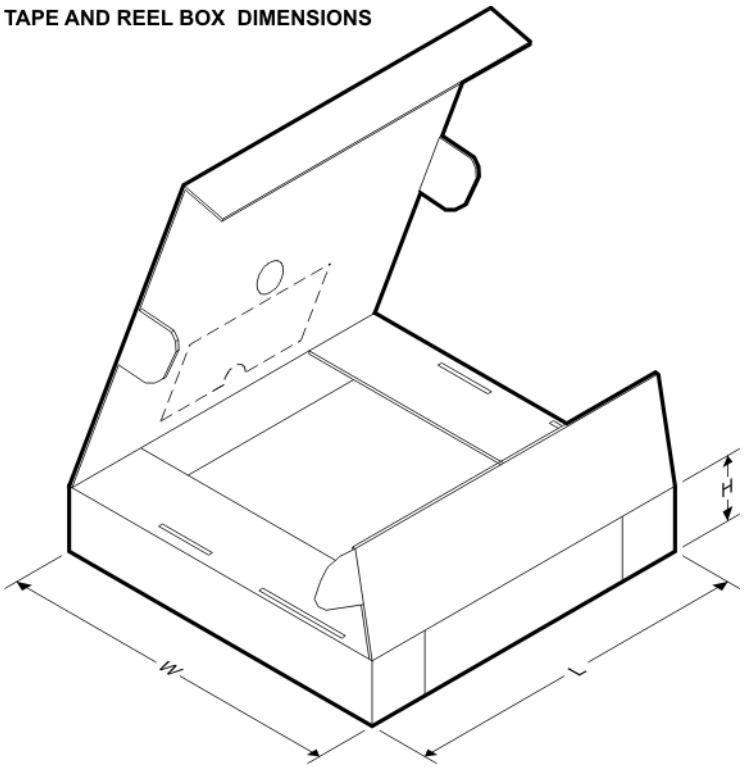
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AFE5851IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AFE5851IRGCR	VQFN	RGC	64	2000	350.0	350.0	43.0

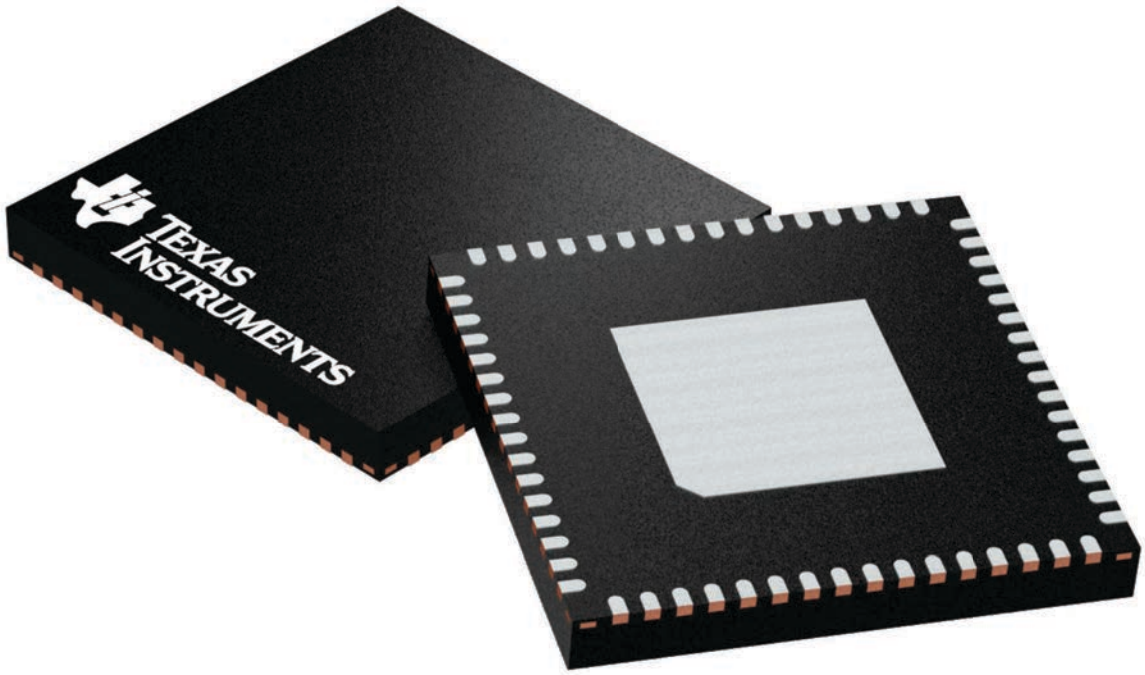
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

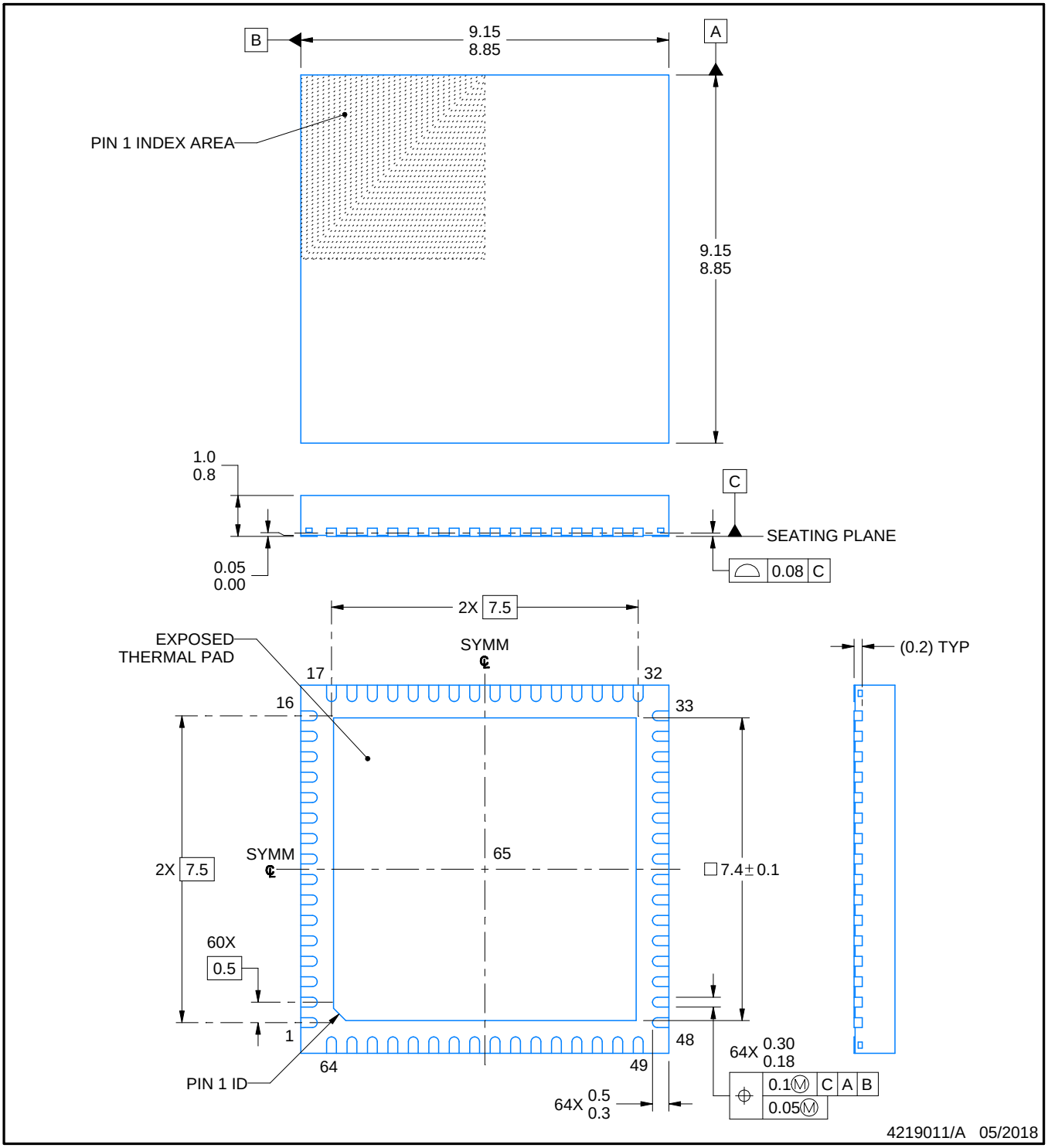
4224597/A

RGC0064H

PACKAGE OUTLINE

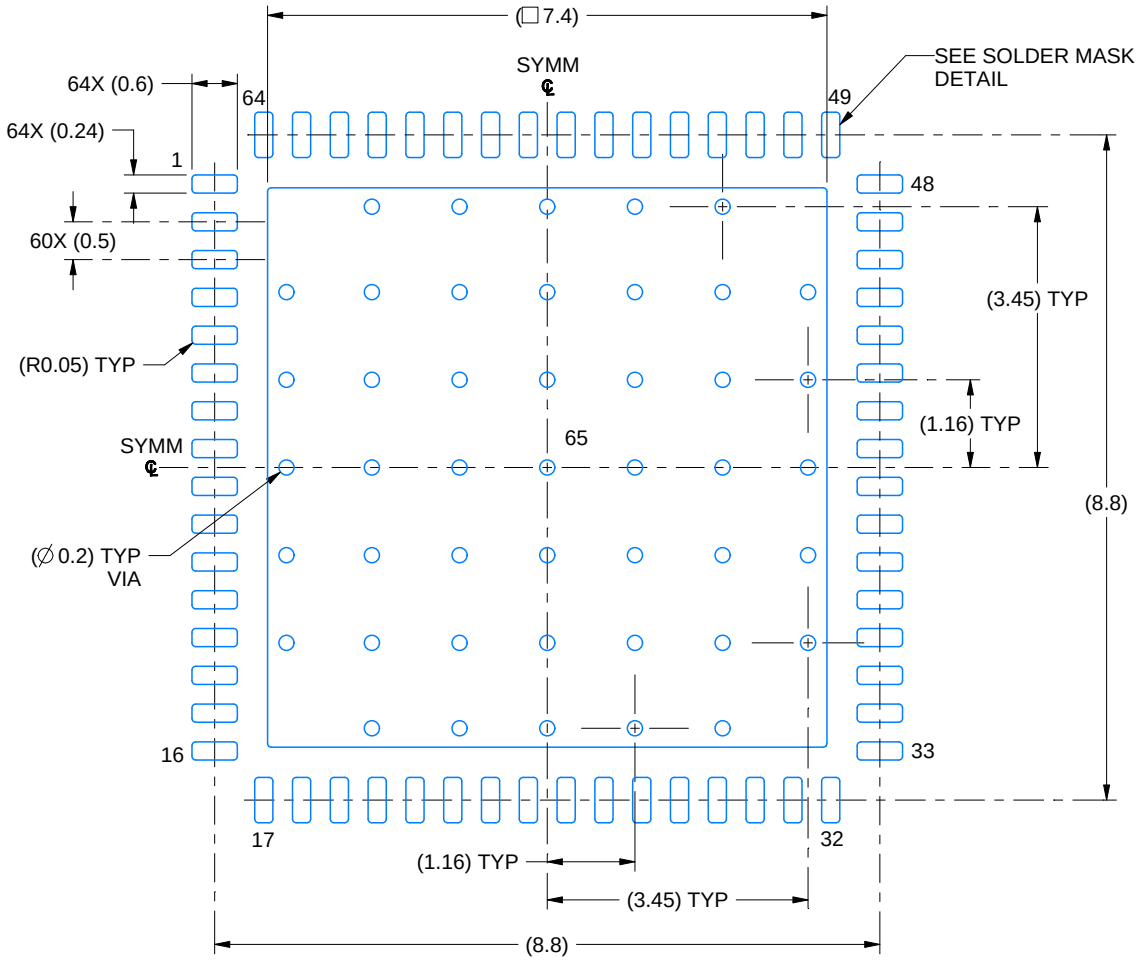
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

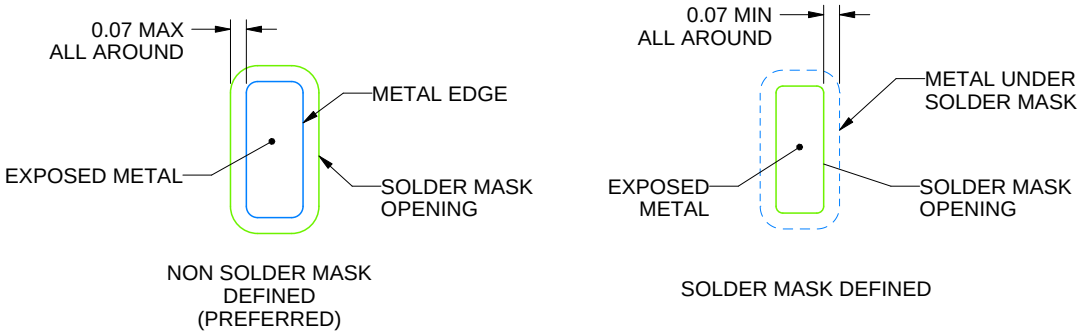


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

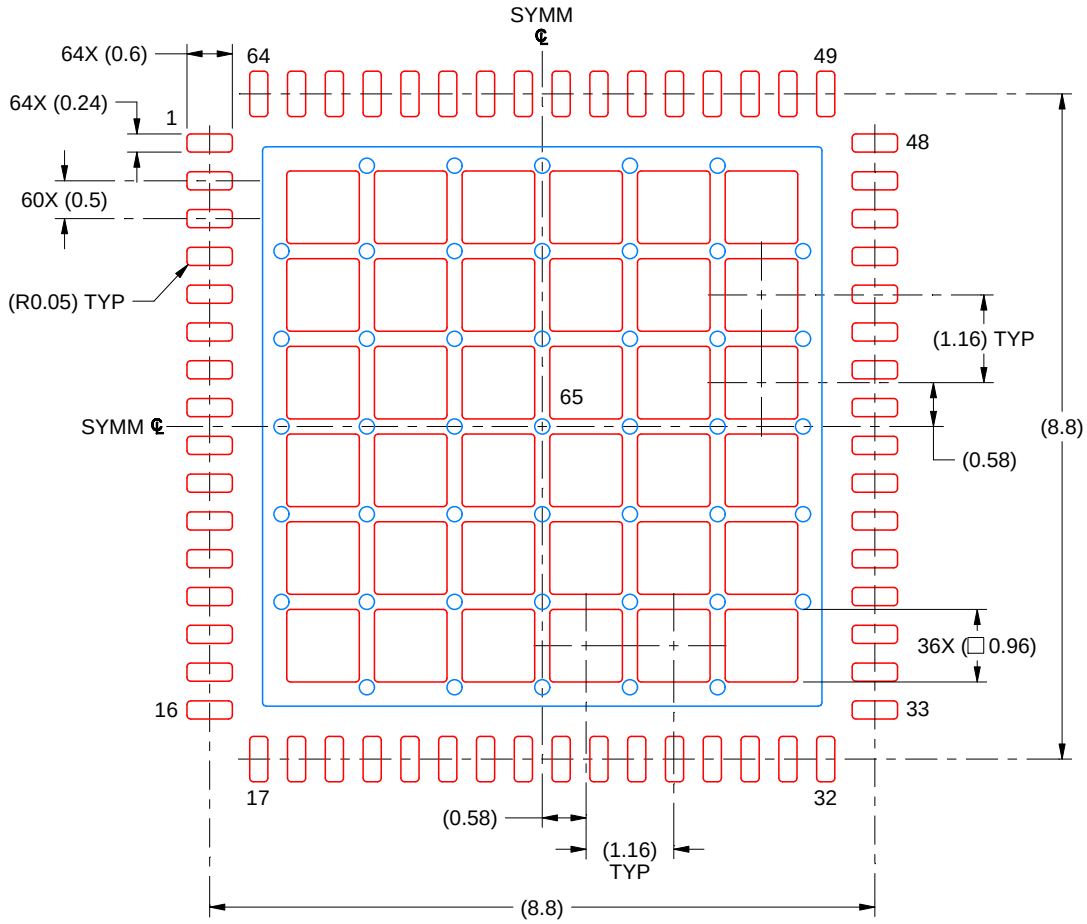


SOLDER MASK DETAILS

4219011/A 05/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
61% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219011/A 05/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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