带有
集成感测元件的 2.5A，单输入，单节开关模式锂离子电池充电器

查询样品: bq24273

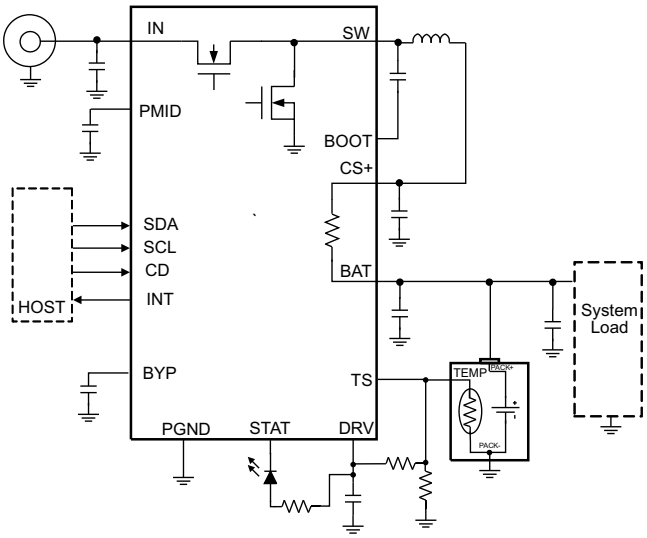
特性

- 带有集成电流感测元件的高效开关模式充电器
- 单输入充电器
  - 额定 **20V** 输入，带有 **10.5V** 过压保护 **(OVP)**
  - 集成场效应晶体管 **(FET)** 可使充电率高达 **2.5A**
- 集成充电电流感测元件可减少物料清单 **(BOM)** 数量并节省电路板空间
- 安全且准确的电池管理功能
  - 电池调节精度 **0.5%**
  - 充电电流精度 **10%**
- 基于电压的，负温度系数热敏电阻 **(NTC)** 监控输入**(TS)**
  - 与 **JEITA** 标准兼容
- 针对输出电流控制的热调节保护
- 电池 **(BAT)** 短路保护
- 降低涌入电流的软启动特性
- 热关断和保护
- 采用小型 **49** 焊球晶圆级芯片封装 **(WCSP)** 或者四方扁平无引线 **(QFN)-24** 封装

应用范围

- 手持产品
- 便携式媒体播放器
- 便携式设备
- 平板电脑和便携式互联网器件

应用电路原理图



说明

bq24273 是一款高度集成的单节锂离子电池充电器，针对空间有限且带有高容量电池的便携式应用，此充电器集成了充电电流感测元件。 单节充电器可由一个专用电源供电运行，例如墙式充电器或者针对多用途解决方案的无线电源。 集成的电流感测元件免除了对于外部感测电阻器的需要，从而减少了总体解决方案尺寸和外部组件数量。

电池充电有三个阶段：预充电、快速充电恒定电流和恒定电压。 在所有的充电阶段，一个内部控制环路监测 IC 结温并且在超过内部温度阀值的情况下减少充电电流。 根据用户可选最小电流水平，充电可被终止。 在一个安全定时器防止对已损坏电池持续充电的同时，一个软件安全装置为 I2C 接口提供了一个安全备份。 正常运行期间，如果电池电压下降至低于一个内部阀值，bq24273 自动重新启动充电周期；并且当输入电源被移除后，自动进入睡眠模式或者高阻抗模式。 可使用 I2C 接口将充电状态报告给主机。 此外，还包括一个基于电压的电池组热敏电阻器监控输入 (TS) 来监控电池温度以实现安全充电。 bq24273 的 TS 功能与 JEITA 标准兼容。

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PART NUMBER	OVP	NTC MONITORING (TS)	JEITA COMPATIBLE	PACKAGE
bq24273YFFR	10.5 V	Yes	Yes	WCSP
bq24273YFFT	10.5 V	Yes	Yes	WCSP

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Pin voltage range (with respect to VSS)	IN	–2	20	V
	BYP, PMID, BOOT	–0.3	20	V
	SW	–0.7	12	V
	CS+, BAT, BGATE, DRV, STAT, INT, SDA, SCL, CD,TS	–0.3	7	V
BOOT to SW		–0.3	7	V
Output Current (Continuous)	SW		4.5	A
Input Current (Continuous)	IN		2.75	A
Output Sink Current	STAT, INT		10	mA
Operating free-air temperature range		–40	85	°C
Junction temperature, T_J		–40	125	°C
Storage temperature, T_{STG}		–65	150	°C
Lead temperature (soldering, 10 s)			300	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

THERMAL INFORMATION

THERMAL METRIC(1)		bq24273	UNITS
		49 PINS (YFF)	
θ_{JA}	Junction-to-ambient thermal resistance	49.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	0.2	
θ_{JB}	Junction-to-board thermal resistance	1.1	
ψ_{JT}	Junction-to-top characterization parameter	1.1	
ψ_{JB}	Junction-to-board characterization parameter	6.6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) 有关传统和全新热度量的更多信息，请参阅 *IC 封装热度量* 应用报告 （文献号：SPRA953）。

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RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNITS
V_{IN}	IN voltage range	4.2	18(1)	V
	IN operating range	4.2	10	
I_{IN}	Input current IN input		2.5	A
I_{BAT}	Charging		2.5	A
T_J	Operating junction temperature range	0	125	°C

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either the BOOT or SW pins. A tight layout minimizes switching noise.

ELECTRICAL CHARACTERISTICS

Circuit of Figure 1, $V_{UVLO} < V_{IN} < V_{OVP}$ AND $V_{IN}>V_{BAT}+V_{SLP}$, T_J = 0°C – 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{IN}	Input quiescent current	$V_{UVLO} < V_{IN} < V_{OVP}$ AND $V_{IN} > V_{BAT}+V_{SLP}$, PWM switching			15		mA
		$V_{UVLO} < V_{IN} < V_{OVP}$ AND $V_{IN} > V_{BAT}+V_{SLP}$, PWM NOT switching				5	
		0°C< T_J < 85°C, High-Z Mode				175	µA
$I_{BATLEAK}$	Leakage current from BAT to the supply	0°C< T_J < 85°C, V_{BAT} = 4.2V, V_{IN} = 0V				5	µA
I_{BAT_HIZ}	Battery discharge current in high impedance mode, (BAT, SW)	0°C< T_J < 85°C, V_{BAT} = 4.2 V, V_{IN} = 0 V or 5 V, High-Z mode				55	µA
BATTERY CHARGER							
$R_{ON(BAT-CS+)}$	Internal battery charger MOSFET on-resistance	Measured from BAT to CS+, V_{BAT} = 4.2V	YFF pkg		37	57	mΩ
			RGE pkg		50	70	
V_{BATREG}	Battery regulation voltage			3.5		4.44	V
	Battery regulation voltage accuracy	T_A = 25°C		–0.5%		0.5%	
		Over temperature		–1%		1%	
I_{CHARGE}	Charge current programmable range	$V_{BATSHRT} < V_{BAT} < V_{BATREG}$		550		2500	mA
	Fast charge current accuracy	0°C to 125°C		–10%		10%	
$V_{BATSHRT}$	Battery short threshold	V_{BAT} Rising, 100 mV Hysteresis		2.9	3.0	3.1	V
$I_{BATSHRT}$	Battery short current	$V_{BAT} < V_{BATSHRT}$			50.0		mA
$t_{DGL(BATSHRT)}$	Deglitch time for battery short to fast charge transition				32		ms
I_{TERM}	Termination charge current accuracy	I_{CHARGE} = 50 mA		–35%		35%	
		I_{CHARGE} > 50 mA		–15%		15%	
$t_{DGL(TERM)}$	Deglitch time for charge termination	Both rising and falling, 2-mV over-drive, t_{RISE}, t_{FALL} = 100 ns			32		ms
V_{RCH}	Recharge threshold voltage	Below V_{BATREG}			120		mV
$t_{DGL(RCH)}$	Deglitch time	V_{BAT} falling below V_{RCH}, t_{FALL} = 100ns			32		ms
V_{DETECT}	Battery detection voltage threshold	During battery detection source cycle			3.3		V
		During battery detection sink cycle			3.0		
I_{DETECT}	Battery detection current before charge done (sink current)				2.5		mA
t_{DETECT}	Battery detection time				250		ms
$V_{IH(CD)}$	CD input high logic level			1.3			V
$V_{IL(CD)}$	CD input low logic level				0.4		V
INPUT PROTECTION							
I_{INLIM}	Input current limit	VIN=5V, DC current pulled from SW	I_{INLIM} = 1.5 A	1.35	1.5	1.65	A
			I_{INLIM} = 2.5 A	2.3	2.5	2.8	
V_{IN_DPM}	Input DPM threshold			4.2		4.76	V
	Input DPM accuracy			–2%		2%	
V_{DRV}	Internal bias regulator voltage			5	5.2	5.45	V
I_{DRV}	DRV Output current			10			mA
V_{DO_DRV}	DRV Dropout voltage (V_{IN} – V_{DRV})	I_{IN} = 1A, V_{IN} = 5V, I_{DRV} = 10mA				450	mV
V_{UVLO}	IC active threshold voltage	V_{IN} rising, 150 mV hysteresis		3.6	3.8	4.0	V
V_{SLP}	Sleep-mode entry threshold, V_{IN}-V_{BAT}	2.0 V ≤ V_{BAT} ≤ V_{OREG}, V_{IN} falling		0	40	100	mV
V_{SLP_EXIT}	Sleep-mode exit hysteresis	2.0 V ≤ V_{BAT} ≤ V_{OREG}		40	100	160	mV

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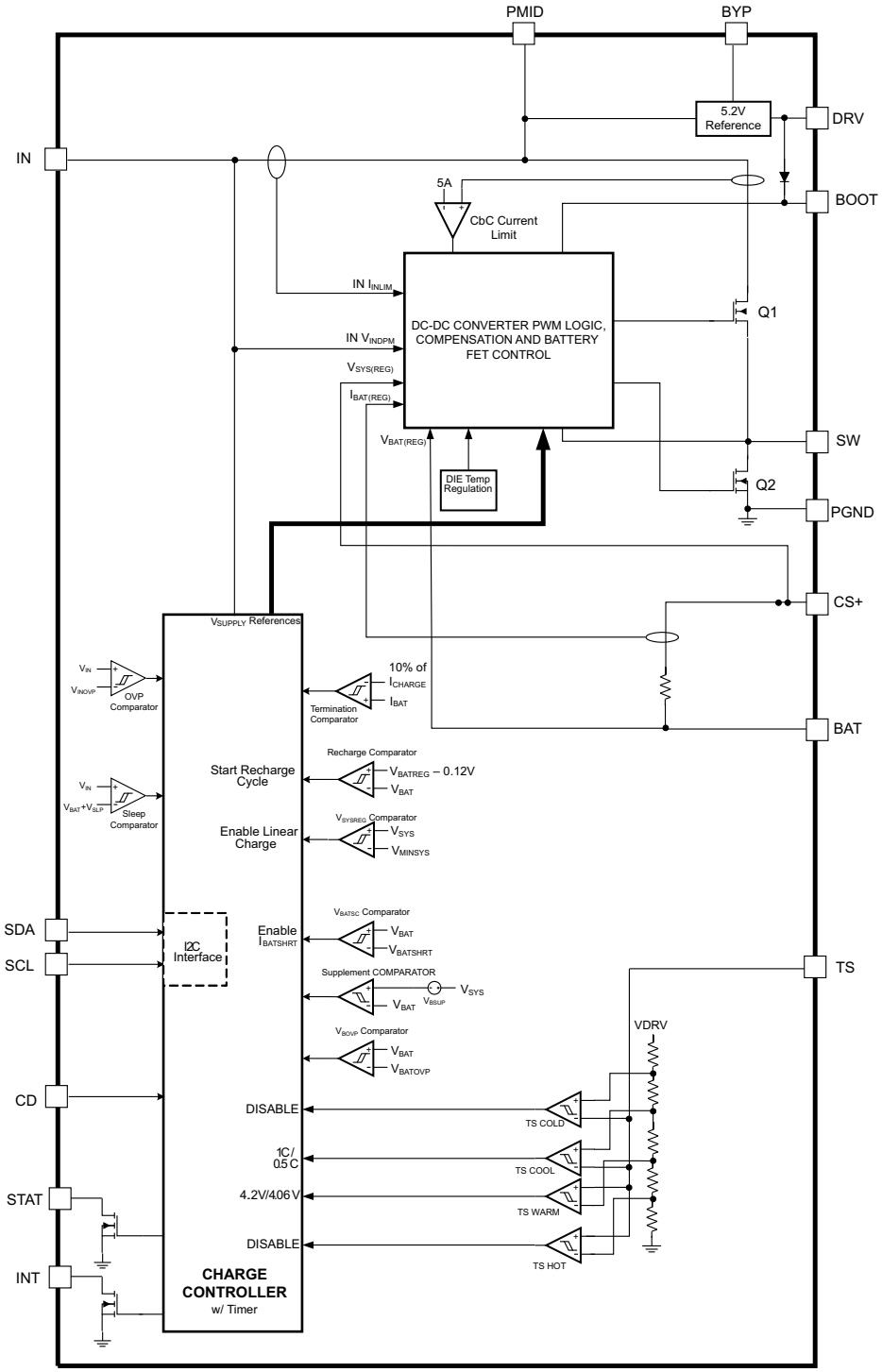
ELECTRICAL CHARACTERISTICS (continued)

Circuit of , $V_{UVLO} < V_{IN} < V_{OVP}$ AND $V_{IN}>V_{BAT}+V_{SLP}$, T_J = 0°C – 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
	Deglitch time for supply rising above VSLP+VSLP_EXIT	Rising voltage, 2-mV over drive, t_{RISE}=100ns		30		ms
V_{OVP}	Input supply OVP threshold voltage	IN, V_{IN} Rising, 100 mV hysteresis	10.3	10.5	10.7	V
V_{BOVP}	Battery OVP threshold voltage	V_{BAT} threshold over V_{OREG} to turn off charger during charge	1.025 × V_{BATREG}	1.05 × V_{BATREG}	1.075 × V_{BATREG}	V
	V_{BOVP} hysteresis	Lower limit for V_{BAT} falling from above V_{BOVP}		1		% of V_{BATREG}
$V_{BATUVLO}$	Battery UVLO threshold voltage			2.5		V
V_{BAT_SOURCE}	Bad source detection threshold			V_{IN_DPM} – 80mV		V
	Bad source detection deglitch			32		ms
I_{LIMIT}	Cycle by cycle current limit		4.1	4.9	5.6	A
$T_{SHUTDWN}$	Thermal shutdown	10°C Hysteresis		165		C
T_{REG}	Thermal regulation threshold			120		C
	Safety timer accuracy		–20%		20%	
STAT, INT						
I_{IH}	High-level leakage current	$V_{/CHG}$ = $V_{/PG}$ = 5 V			1	µA
V_{OL}	Low-level output saturation voltage	IO = 10 mA, sink current			0.4	V
PWM CONVERTER						
	Internal top reverse blocking MOSFET on-resistance	I_{IN_LIMIT} = 1.5 A, Measured from $_{VIN}$ to PMIDU		45	80	mΩ
	Internal top N-channel Switching MOSFET on-resistance	Measured from PMID to SW		65	110	mΩ
	Internal bottom N-channel MOSFET on-resistance	Measured from SW to PGND		65	115	mΩ
f_{OSC}	Oscillator frequency		1.35	1.50	1.65	MHz
D_{MAX}	Maximum duty cycle			95%		
D_{MIN}	Minimum duty cycle		0			
BATTERY-PACK NTC MONITOR						
V_{HOT}	High temperature threshold	V_{TS} falling, 1%V_{DRV} Hysteresis	29.7	30	30.5	%VDRV
V_{WARM}			37.9	38.3	39.6	%VDRV
V_{COOL}	Low temperature threshold	V_{TS} rising, 1%V_{DRV} Hysteresis	56.0	56.5	56.9	%VDRV
V_{COLD}			59.5	60	60.4	%VDRV
V_{TSOFF}	TS Disable threshold	V_{TS} rising, 2%V_{DRV} Hysteresis	70		73	%VDRV
$t_{DGL(TS)}$	Deglitch time on TS change			50		ms
V_{IH}	Input high threshold	V_{PULLUP} = 1.8 V, SDA and SCL	1.3			V
V_{IL}	Input low threshold	V_{PULLUP} = 1.8 V, SDA and SCL			0.4	V
V_{OL}	Output low threshold	I_{SDA} = 10 mA, sink current			0.4	V
I_{IH}	Input high leakage current	V_{PULLUP} = 1.8 V, SDA and SCL		1		µA
$t_{WATCHDOG}$	Watchdog timer timeout		30			s

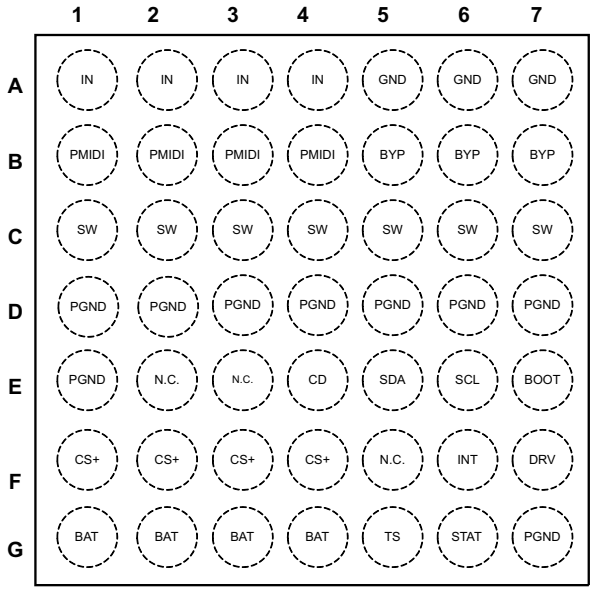
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BLOCK DIAGRAM



PIN CONFIGURATION

49-Ball WCSP (Top View)



PIN FUNCTIONS

PIN			
NAME	**bq24273 (YFF)**	**I/O**	**DESCRIPTION**
IN	A1-A4	I	Input Power Supply. IN is connected to the external DC supply (AC adapter). Bypass IN to PGND with at least a 1µF ceramic capacitor.
GND	A5-A7	I	Ground. Connect to ground plane.
PMID	B1-B4	O	Reverse Blocking MOSFET and High Side MOSFET Connection Point for the input. Bypass PMID to GND with at least a 4.7µF ceramic capacitor. Use caution when connecting an external load to PMID. The PMID output is not current limited. Any short on PMID will result in damage to the IC.
BYP	B5-B7	O	Bypass for internal circuits. Bypass BYP to GND with at least 0.1µF of capacitance. Do not connect any external load to BYP.
SW	C1-C7	O	Inductor Connection. Connect to the switched side of the external inductor.
PGND	D1-D7, E1, G7	--	Ground terminal. Connect to the thermal pad (for QFN only) and the ground plane of the circuit.
N.C.	E2-E3, F5		No Connection. Leave N.C. unconnected.
CD	E4		IC Hardware Disable Input – Drive CD high to place the bq24273 in high-z mode. Drive CD low for normal operation. Do not leave CD unconnected.
SDA	E5		I^2C Interface Data – Connect SDA to the logic rail through a 10kΩ resistor.
SCL	E6		I^2C Interface Clock – Connect SCL to the logic rail through a 10kΩ resistor.
BOOT	E7	I	High Side MOSFET Gate Driver Supply. Connect a 0.01µF ceramic capacitor (voltage rating > 10V) from BOOT to SW to supply the gate drive for the high side MOSFETs.
CS+	F1-F4	I	Current Sense Input. High side connection to internal current sense element. Bypass CS+ locally with at least 10µF of ceramic capacitance for stability.
INT	F6		Status Output – INT is an open-drain output that signals charging status and fault interrupts. INT pulls low during charging. INT is high impedance when charging is complete or the charger is disabled. When a fault occurs, a 128µs pulse is sent out as an interrupt for the host. INT is enabled/disabled using the EN_STAT bit in the control register. Connect INT to a logic rail through a 100kΩ resistor to communicate with the host processor
DRV	F7	O	Gate Drive Supply. DRV is the bias supply for the gate drive of the internal MOSFETs. bypass DRV to PGND with a 1µF ceramic capacitor. DRV may be used to drive external loads up to 10mA. DRV is active whenever the input is connected and $_{VIN}$ > V_{UVLO} and V_{IN} > (V_{BAT} + V_{SLP})
BAT	G1-G4	I/O	Battery Connection. Connect to the positive terminal of the battery. Additionally, bypass BAT to GND with a 1µF capacitor.

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PIN FUNCTIONS (continued)

PIN			
NAME	**bq24273 (YFF)**	**I/O**	**DESCRIPTION**
TS	G5		Battery Pack NTC Monitor. Connect TS to the center tap of a resistor divider from DRV to GND. The NTC is connected from TS to GND. The TS function in the bq24276 provides 2 thresholds for Hot/ Cold shutoff, while the bq24277 has 2 additional thresholds for JEITA compliance. See the *NTC Monitor* section for more details on operation and selecting the resistor values.
STAT	G6		Status Output – STAT is an open-drain output that signals charging status and fault interrupts. STAT pulls low during charging. STAT is high impedance when charging is complete or the charger is disabled. When a fault occurs, a 128µs pulse is sent out as an interrupt for the host. STAT is enabled/ disabled using the EN_STAT bit in the control register. Pull STAT up to a logic rail through an LED for visual indication or through a 10kΩ resistor to communicate with the host processor.
Thermal Pad	–	–	There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times.

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TYPICAL APPLICATION CIRCUIT

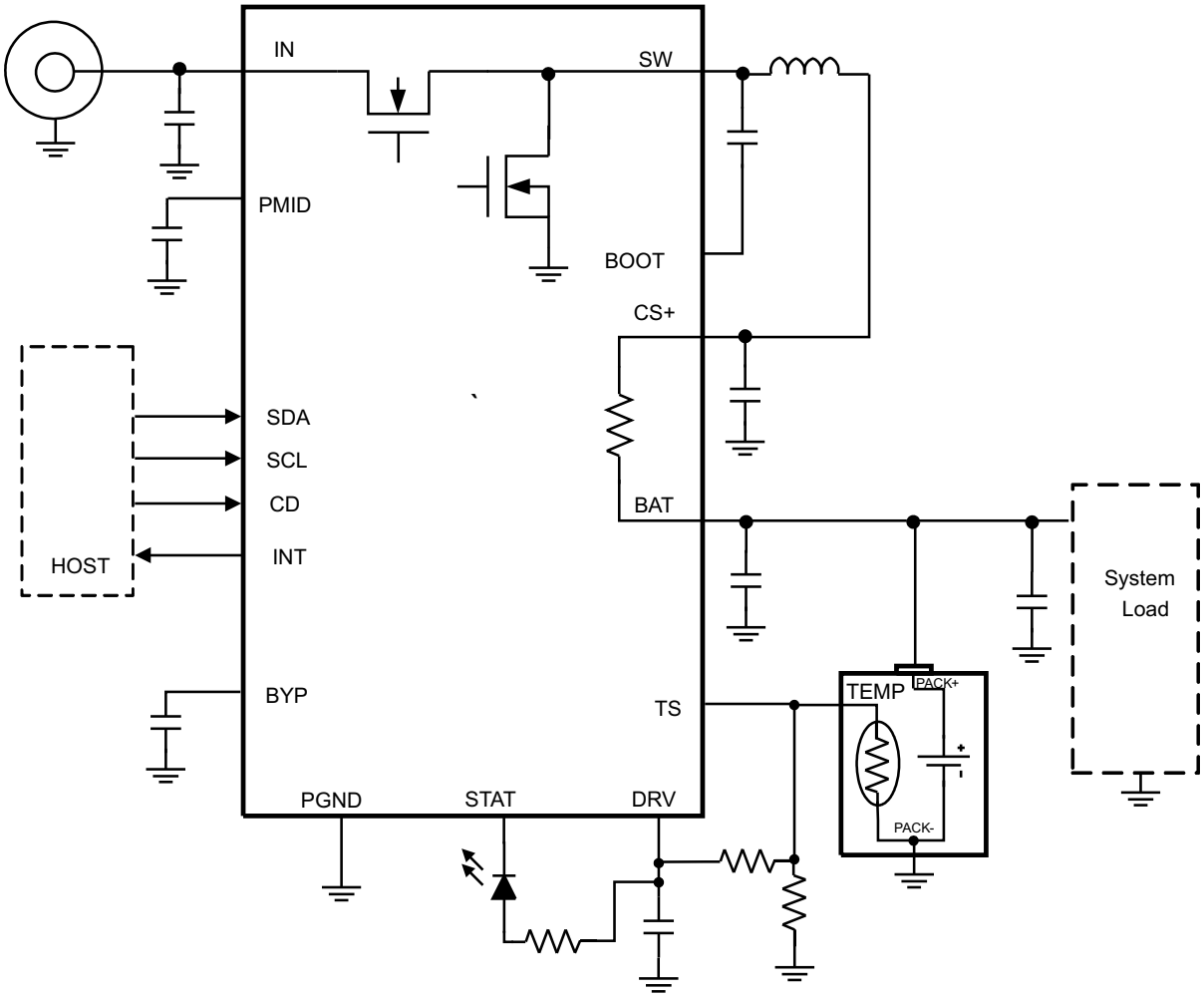


Figure 1. bq24273 Application Circuit

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DETAILED DESCRIPTION

The bq24273 is a highly integrated synchronous switch-mode charger featuring integrated MOSFETs and current sense element reducing the count of external components. It is targeted at portable applications with higher capacity batterires powered by 1-cell Li-Ion, LiFePO4 or Li-polymer battery pack. Due to the high efficiency in a wide range of the input voltage and battery voltage, the switching mode charger is a good choice for high speed charging with less power loss and better thermal management.

The bq24273 has two operation states: charge state and high impedance state. In the charge state, the bq24273 supports a precision Li-ion, LiFePO4 or Li-polymer charging system for single-cell applications. In the high impedance state, the bq24273 stops charging and operates in a mode with very low current from IN and battery, to effectively reduce the power consumption when the portable device is in standby mode.

The bq24273 includes an integrated 35mΩ sense resistor that is used to measure the charge current into the battery. As resistors are expected to have a temperature coefficient, the bq24273 includes a compensation mechanism that maintains the accuracy of the charge current as the temperature changes. This allows for a smaller BOM solution allowing the removal of an external high accuracy sense resistor that are typically needed for non-power path charger solutions.

Charge Mode Operation

Charge Profile

There are 5 loops that influence the charge current; constant current loop (CC), constant voltage loop (CV), thermal regulation loop, input current sense loop and input voltage dynamic power management loop (VIN-DPM). During the charging process, all five loops are enabled and the one that is dominate takes control. The bq24273 supports a precision LiFePO4, Li-Ion or Li-Polymer charging systems for single-cell applications. Figure 2 shows a typical charge profile.

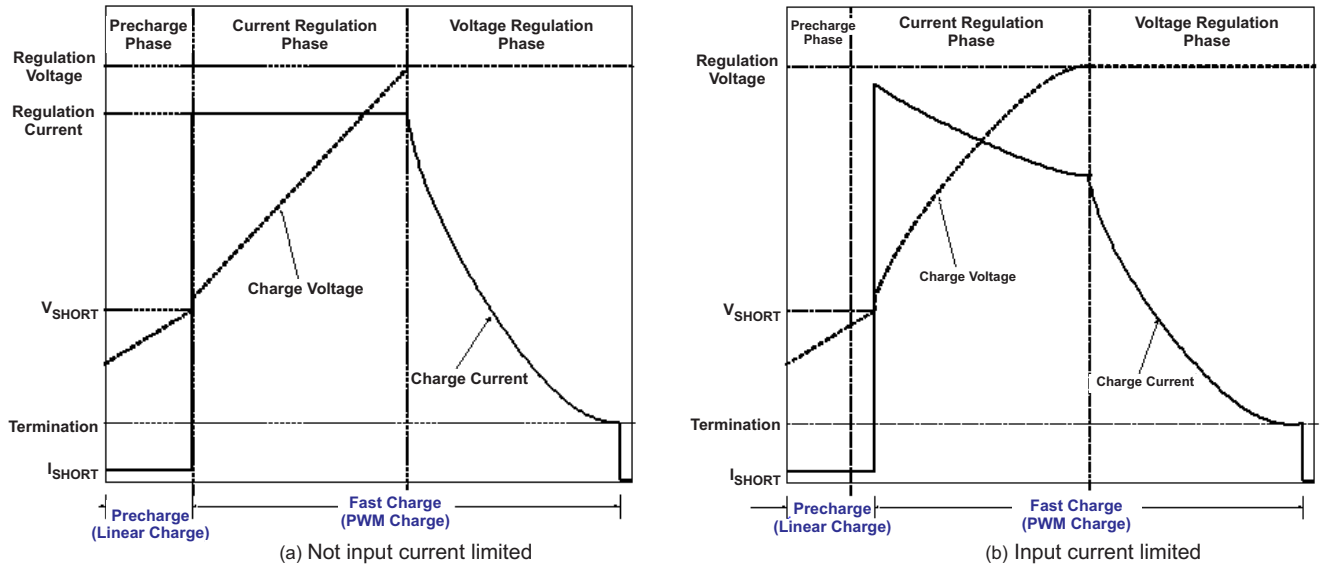


Figure 2. Typical Charging Profile of bq24273

PWM Controller in Charge Mode

The bq24273 provides an integrated, fixed-frequency 1.5MHz voltage-mode controller to supply the charge current. The voltage loop is internally compensated and provides enough phase margin for stable operation, allowing the use of small ceramic capacitors with very low ESR.

The input is protected from short circuit by a cycle-by-cycle current limit that is sensed through the high-side MOSFET. The threshold is set to a nominal 5-A peak current. The input also utilizes an input current limit that limits the current from the power source.

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Battery Charging Process

When the battery is deeply discharged or shorted (V_{BAT}<$V_{BATSHRT}$), the bq24273 applies a 50mA current to close the pack protector switch and bring the battery voltage up to acceptable charging levels. Once the battery rises above $V_{BATSHRT}$, the charge current is regulated to the value set in the I^2C register. If the die temperature does heat up, the thermal regulation circuit reduces the charge current to maintain a die temperature less than 125°C. The slew rate for fast charge current is controlled to minimize the current and voltage over-shoot during transient. The charge current is regulated to $I_{OCHARGE}$ until the battery is charged to the regulation voltage. Once the battery voltage is close to the regulation voltage, V_{BATREG}, the charge current is tapered down as shown in Figure 2. The voltage regulation feedback occurs by monitoring the battery-pack voltage between the BAT and PGND pins. The bq24273 is a fixed single-cell voltage version, with adjustable regulation voltage (3.5V to 4.44V) programmed using the I^2C interface.

The bq24273 monitors the charging current during the voltage regulation phase. Once the termination threshold, I_{TERM}, is detected and the battery voltage is above the recharge threshold, the bq24273 terminates the charge cycle and enters battery detection. The termination current level is programmable. To disable the charge current termination, the host sets the charge termination bit (TE) of charge control register to 0, refer to I^2C section for details.

A new charge cycle is initiated when one of the following conditions is detected:

1. The battery voltage falls below the V_{BATREG}-V_{RCH} threshold.
2. CE bit toggle or RESET bit is set
3. HI-Z bit toggle

Battery Detection

When termination conditions are met, a battery detection cycle is started. During battery detection, I_{DETECT} is pulled from V_{BAT} for t_{DETECT} to verify there is a battery. If the battery voltage remains above V_{DETECT} for the full duration of t_{DETECT}, a battery is determined to present and the IC enters “Charge Done”. If V_{BAT} falls below V_{DETECT}, a “Battery Not Present” fault is signaled and battery detection continues. The next cycle of battery detection, the bq2427x turns on $I_{BATSHORT}$ for t_{DETECT}. If V_{BAT} rises to V_{DETECT}, the current source is turned off and after t_{DETECT}, the battery detection continues through another current sink cycle. Battery detection continues until charge is disabled or a battery is detected. Once a battery is detected, the fault status clears and a new charge cycle begins. Battery detection is not run when termination is disabled.

DEFAULT Mode

DEFAULT mode is used when I^2C communication is not available. DEFAULT mode is entered in the following situations:

1. When the charger is enabled and V_{BAT}<3.6V before I^2C communication is established
2. When the watchdog timer expires without a reset from the I^2C interface and the safety timer has not expired.
3. When the device comes out of any fault condition (sleep mode, OVP, faulty adapter mode, etc.) before I^2C communication is established

In default mode, the I^2C registers are reset to the default values. The 27 min safety timer is reset and starts when DEFAULT mode is entered. The default value for V_{BATREG} is 3.6V, and the default value for I_{CHARGE} is 1A. The input current limit for the IN input is set to 1.5A. Default mode is exited by programming the I^2C interface. Note that if termination is enabled and charging has terminated, a new charge cycle is NOT initiated when entering DEFAULT mode.

Safety Timer and Watchdog Timer

At the beginning of charging process, the bq24273 starts the safety timer. This timer is active during the entire charging process. If charging has not terminated before the safety timer expires, charging is halted and the $\overline{CE}$ bit is written to a “1”. The length of the safety timer is selectable using the I^2C interface. A single 128µs pulse is sent on the STAT and INT outputs and the STATx bits of the status registers are updated in the I^2C. The /CE bit must be toggled in order to clear the safety timer fault. The safety timer duration is selectable using the TMR_X bits in the Safety Timer Register/ NTC Monitor register. Changing the safety timer duration resets the safety timer. If the safety timer expires, charging is disabled ($\overline{CE}$ changed to a “1”). This function prevents continuous charging of a defective battery if the host fails to reset the safety timer.

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In addition to the safety timer, the bq24273 contains a watchdog timer that monitors the host through the I^2C interface. Once a read/write is performed on the I^2C interface, a 30-second timer ($t_{WATCHDOG}$) is started. The 30-second timer is reset by the host using the I2C interface. This is done by writing a "1" to the reset bit (TMR_RST) in the control register. The TMR_RST bit is automatically set to "0" when the 30-second timer is reset. This process continues until battery is fully charged or the safety timer expires. If the 30-second timer expires, the IC enters DEFAULT mode where the default register values are loaded, the safety timer restarts at 27minutes and charging continues. The I^2C may be accessed again to reinitialize the desired values and restart the watchdog timer as long as the 27 minute safety timer has not expired. The watchdog timer flow chart is shown in Figure 3.

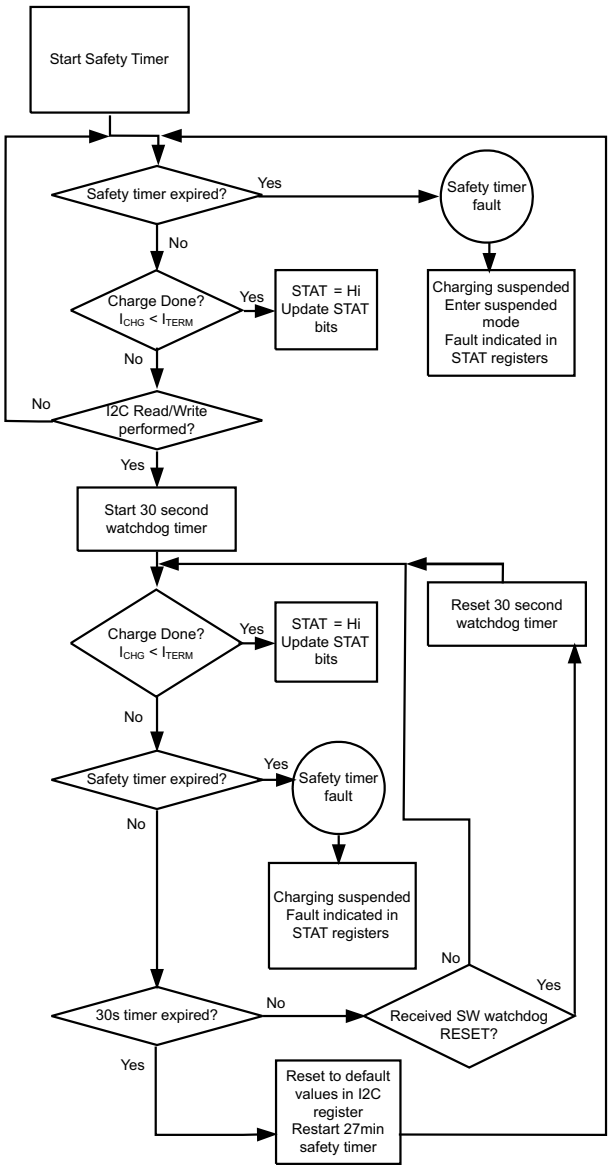


Figure 3. The Watchdog Timer Flow Chart for bq24273

Hardware Chip Disable Input (CD)

The bq24273 contains a CD input that is used to disable the IC and place the bq24273 into high-impedance mode. Drive CD low to enable charge and enter normal operation. Drive CD high to disable charge and place the bq24273 into high-impedance mode. Driving CD high during DEFAULT mode resets the safety timer. Driving CD high during HOST mode resets the safety timer.

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LDO Output (DRV)

The bq24273 contains a linear regulator (DRV) that is used to supply the internal MOSFET drivers and other circuitry. Additionally, DRV supplies up to 10mA external loads to power the STAT. The maximum value of the DRV output is 5.45V. The LDO is on whenever a supply is connected to the IN input of the bq24273. The DRV is disabled under the following conditions:

1. V_{SUPPLY} < UVLO
2. V_{SUPPLY} < V_{SLP}
3. Thermal Shutdown

External NTC Monitoring (TS)

The I^2C interface allows the user to easily implement the JEITA standard for systems where the battery pack thermistor is monitored by the host. Additionally, the bq24273 provides a flexible, voltage based TS input for monitoring the battery pack NTC thermistor. The voltage at TS is monitored to determine that the battery is at a safe temperature during charging. The bq24273 enable the user to easily implement the JEITA standard for charging temperature. The JEITA specification is shown in Figure 4.

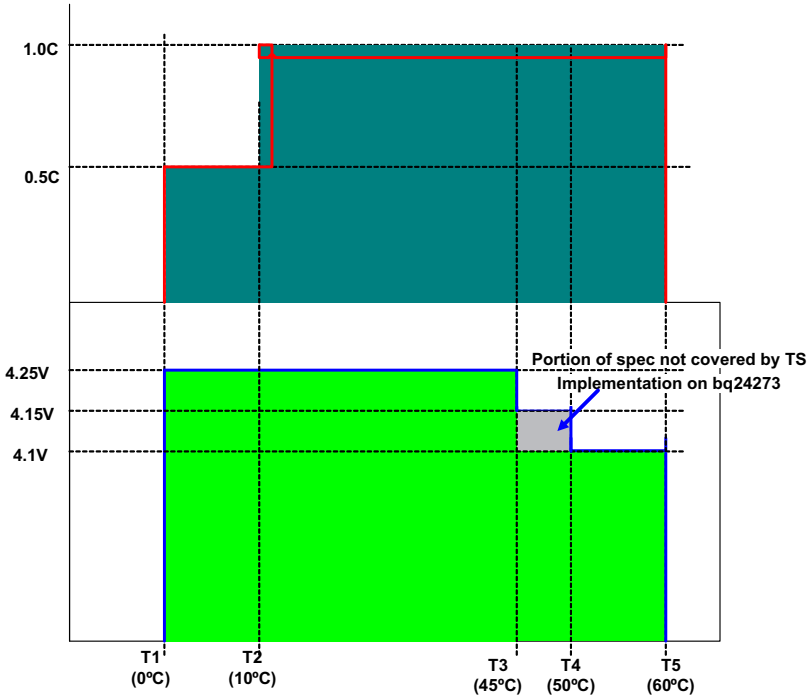


Figure 4. Charge Current During TS Conditions

To satisfy the JEITA requirements, four temperature thresholds are monitored; the cold battery threshold (T_{NTC} < 0°C), the cool battery threshold (0°C < T_{NTC} < 10°C), the warm battery threshold (45°C < TNTC < 60°C) and the hot battery threshold (TNTC > 60°C). These temperatures correspond to the V_{COLD}, V_{COOL}, V_{WARM}, and V_{HOT} thresholds. Charging is suspended and timers are suspended when V_{TS} < V_{HOT} or V_{TS} > V_{COLD}. When V_{HOT} < V_{TS} < V_{WARM}, the battery regulation voltage is reduced by 140mV from the programmed regulation threshold. When V_{COOL} < V_{TS} < V_{COLD}, the charging current is reduced to half of the programmed charge current.

The TS function is voltage based for maximum flexibility. Connect a resistor divider from DRV to GND with TS connected to the center tap to set the threshold. The connections are shown in Figure 5. The resistor values are calculated using the following equations:

$$RLO = \frac{V_{DRV} \times RCOLD \times RHOT \times \left[\frac{1}{V_{COLD}} - \frac{1}{V_{HOT}}\right]}{RHOT \times \left[\frac{V_{DRV}}{V_{HOT}} - 1\right] - RCOLD \times \left[\frac{V_{DRV}}{V_{COLD}} - 1\right]} \quad (1)$$

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$$RHI = \frac{\frac{V_{DRV}}{V_{COLD}} - 1}{\frac{1}{RLO} + \frac{1}{RCOLD}} \quad (2)$$

Where:

$V_{COLD} = 0.60 \times V_{DRV}$
$V_{HOT} = 0.30 \times V_{DRV}$

Where RHOT is the NTC resistance at the hot temperature and RCOLD is the NTC resistance at cold temperature.

The WARM and COOL thresholds are not independently programmable. The COOL and WARM NTC resistances for a selected resistor divider are calculated using the following equations:

$$RCOOL = \frac{RLO \times 0.564 \times RHI}{RLO - RLO \times 0.564 - RHI \times 0.564} \quad (3)$$

$$RWARM = \frac{RLO \times 0.383 \times RHI}{RLO - RLO \times 0.383 - RHI \times 0.383} \quad (4)$$

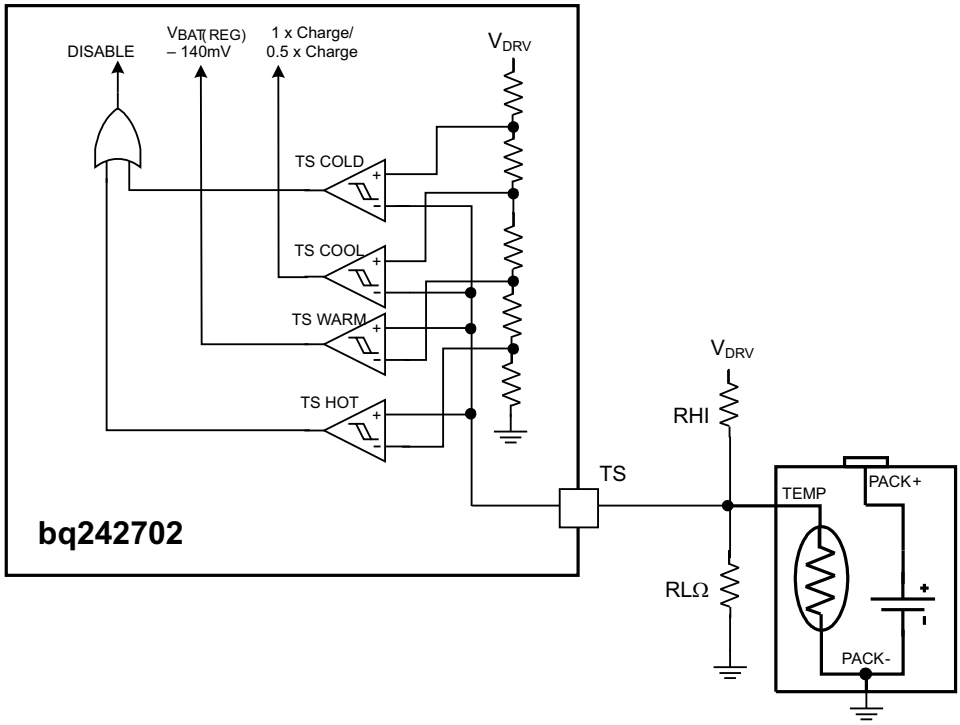


Figure 5. TS Circuit

Thermal Regulation and Protection

During the charging process, to prevent chip overheating, bq24273 monitors the junction temperature, T_J, of the die and begins to taper down the charge current once T_J reaches the thermal regulation threshold, T_{REG}. The charge current is reduced to zero when the junction temperature increases about 10°C above T_{REG}. Once the charge current is reduced, the system current is reduced while the battery supplements the load to supply the system. This may cause a thermal shutdown of the bq24273 if the die temperature rises too high. At any state, if T_J exceeds T_{SHTDWN}, bq24273 suspends charging and disables the buck converter. During thermal shutdown mode, the PWM is turned off, all timers are suspended, and a single 128µs pulse is sent on the STAT and INT outputs and the STATx and FAULT_x bits of the status registers are updated in the I^2C. A new charging cycle begins when T_J falls below T_{SHTDWN} by approximately 10°C.

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Input Voltage Protection in Charge Mode

Sleep Mode

The bq24273 enters the low-power sleep mode if the voltage on V_{SUPPLY} falls below sleep-mode entry threshold, V_{BAT}+V_{SLP}, and V_{VBUS} is higher than the undervoltage lockout threshold, V_{UVLO}. This feature prevents draining the battery during the absence of V_{SUPPLY}. When V_{SUPPLY} < V_{BAT}+ V_{SLP}, the bq24273 turns off the PWM converter and sends a single 128µs pulse on the STAT and INT outputs and updates the STATx and FAULT_x bits in the status registers. Once V_{SUPPLY} > V_{BAT}+ V_{SLP}, the STATx and FAULT_x bits are cleared and the device initiates a new charge cycle.

Input Voltage Based DPM

During normal charging process, if the input power source is not able to support the programmed or default charging current, the supply voltage will decease. Once the supply drops to V_{IN_DPM} (default 4.76V), the input current limit is reduced down to prevent further supply droop. When the IC enters this mode, the charge current is lower than the set value and the DPM_STATUS bit is set (Bit 5 in Register 05H). This feature ensures IC compatibility with adapters with different current capabilities without a hardware change.

Bad Source Detection

When a source is connected to IN, the bq24273 runs a Bad Source Detection procedure to determine if the source is strong enough to provide some current to charge the battery. A current sink is turned on (75mA) for 32ms. If the source is valid after the 32ms ($V_{BADSOURCE}$ < V_{SUPPLY} < V_{OVP}), the buck converter starts up and normal operation continues. If the supply voltage falls below V_{BAD_SOURCE} during the detection, the current sink shuts off for 2s and then retries, a single 128µs pulse is sent on the STAT and INT outputs and the STATx and FAULT_x bits of the status registers and the battery/supply status registers are updated in the I^2C. The detection circuits retries continuously until a valid source is detected after the detection time. If during normal operation the source falls to V_{BAD_SOURCE}, the bq24273 turns off the PWM converter and sends a single 128µs pulse is sent on the STAT and INT outputs and the STATx and FAULT_x bits of the status registers and the battery/supply status registers are updated in the I2C. Once a good source is detected, the STATx and FAULT_x bits are cleared and the device returns to normal operation.

Input Over-Voltage Protection

The bq24273 provides over-voltage protection on the input that protects downstream circuitry. The built-in input over-voltage protection to protect the device and other components against damage from overvoltage on the input supply (Voltage from V_{IN} to PGND). During normal operation, if V_{SUPPLY} > V_{OVP}, the bq24273 turns off the PWM converter and sends a single 128µs pulse is sent on the STAT and INT outputs and the STATx and FAULT_x bits of the status registers and the battery/supply status registers are updated in the I2C. Once the OVP fault is removed, the STATx and FAULT_x bits are cleared and the device returns to normal operation.

To allow operation with some unregulated adapters, the OVP circuit is not active during Bad Source Detection. This provides some time for the current sink to pull the unregulated adapter down into an acceptable range. If the adapter voltage is high at the end of the detection, the startup of the PWM converter does not occur. The OVP circuit is active during normal operation, so if the system standby current plus the charge current is not enough to pull down the source, operation is suspended.

Charge Status Outputs (STAT, INT)

The STAT output is used to indicate operation conditions for bq24273. STAT is pulled low during charging when EN_STAT bit in the control register (0x02h) is set to “1”. When charge is complete or disabled, STAT is high impedance. When a fault occurs, a 128-µs pulse (interrupt) is sent out to notify the host. The status of STAT during different operation conditions is summarized in Table 1. STAT drives an LED for visual indication or can be connected to the logic rail for host communication. The EN_STAT bit in the control register (00H) is used to enable/disable the charge status for STAT. The interrupt pulses are unaffected by EN_STAT and will always be shown. The INT output is identical to STAT and is used to interface with a low voltage host processor.

Table 1. STAT Pin Summary

Charge State	STAT and INT behavior
Charge in progress and EN_STAT=1	Low
Other normal conditions	High-Impedance
Status Changes: Supply Status Change (plug in or removal), safety timer fault, watchdog expiration, sleep mode, battery temperature fault (TS), battery fault (OVP or absent), thermal shutdown	128-µs pulse, then High Impedance

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SERIAL INTERFACE DESCRIPTION

The bq24273 uses an I^{2}C compatible interface to program charge parameters. I^{2}C™ is a 2-wire serial interface developed by Philips Semiconductor (see I2C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I2C compatible devices connect to the I^{2}C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The bq24273 device works as a slave and supports the following data transfer modes, as defined in the I^{2}C Bus™ Specification: standard mode (100 kbps) and fast mode (400 kbps). The interface adds flexibility to the battery charging solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as battery voltage remains above 2.5 V (typical). The I^{2}C circuitry is powered from IN when a supply is connected. If the IN supply is not connected, the I2C circuitry is powered from the battery through BAT. The battery voltage must stay above 2.5V with no input connected in order to maintain proper operation.

The data transfer protocol for standard and fast modes is exactly the same; therefore, they are referred to as the F/S-mode in this document. The bq24273 devices only support 7-bit addressing. The device 7-bit address is defined as ‘1101011’ (6Bh).

F/S Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 6. All I^{2}C -compatible devices should recognize a start condition.

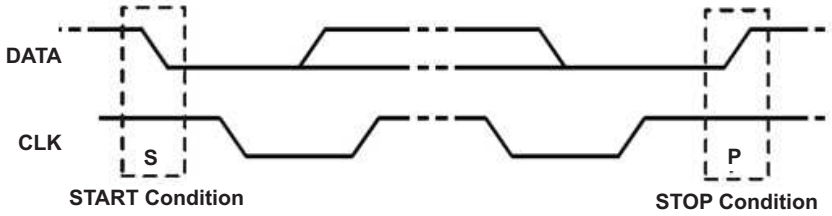


Figure 6. START and STOP Condition

The master then generates the SCL pulses, and transmits the 8-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 7). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 8) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

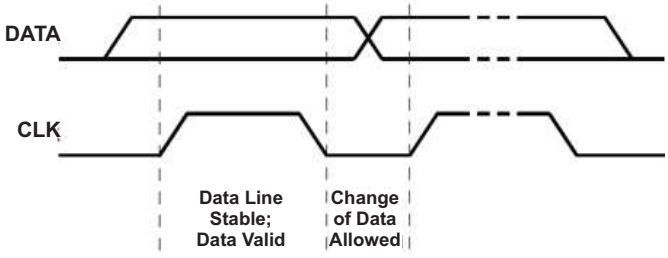


Figure 7. Bit Transfer on the Serial Interface

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The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary. To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 9). This releases the bus and stops the communication link with the addressed slave. All I^2C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and wait for a start condition followed by a matching address. If a transaction is terminated prematurely, the master needs sending a STOP condition to prevent the slave I2C logic from remaining in an incorrect state. Attempting to read data from register addresses not listed in this section result in FFh being read out.

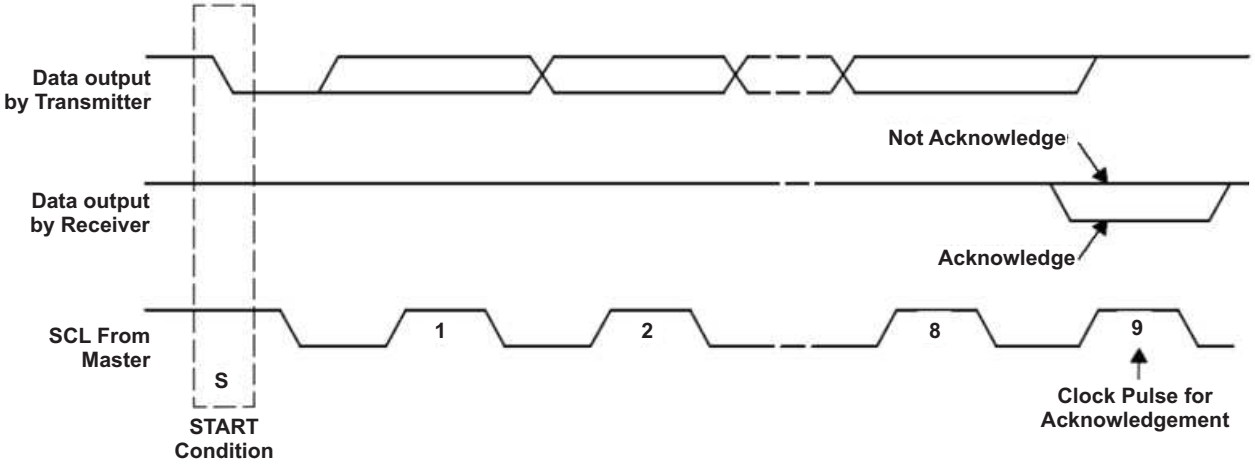


Figure 8. Acknowledge on the I2C Bus

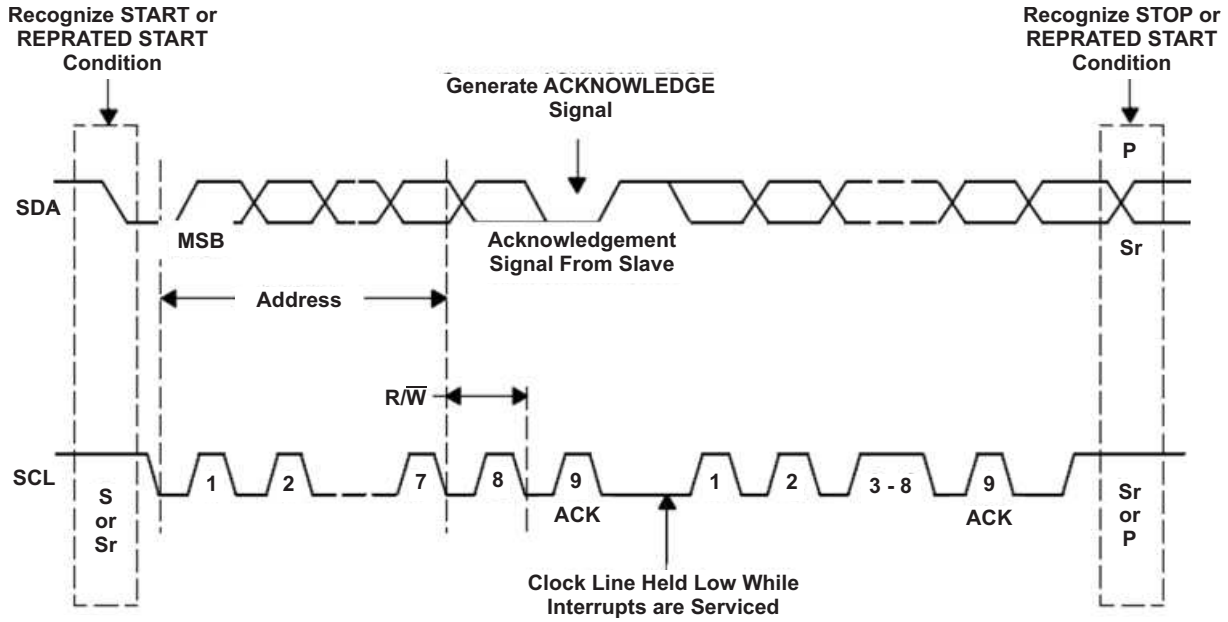


Figure 9. Bus Protocol

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REGISTER DESCRIPTION

Status/Control Register (READ/WRITE)
Memory location: 00, Reset state: 0xxx 0xxx

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	TMR_RST	Read/Write	Write: TMR_RST function, write “1” to reset the watchdog timer (auto clear) Read: Always 0
B6	STAT_2	Read only	000- No Valid Source Detected 001- IN Ready 010- NA 011- Charging 100- NA 101- Charge Done 110- NA 111- Fault
B5	STAT_1	Read only	
B4	STAT_0	Read only	
B3	NA	Read/Write	0-Set always to 0
B2	FAULT_2	Read only	000-Normal 001- Thermal Shutdown 010- Battery Temperature Fault 011- Watchdog Timer Expired 100- Safety Timer Expired 101- Supply Fault 110- NA 111- Battery Fault
B1	FAULT_1	Read only	
B0(LSB)	FAULT_0	Read only	

Battery/ Supply Status Register (READ/WRITE)
Memory location: 01, Reset state: xxxx 0xxx

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	INSTAT1	Read Only	00-Normal 01-Supply OVP 10-Weak Source Connected (No Charging) 11- VIN<VUVLO
B6	INSTAT0	Read Only	
B5	NA	Read Only	NA
B4	NA	Read Only	NA
B3	NA	Read/Write	NA
B2	BATSTAT1	Read Only	00-Battery Present and Normal 01-Battery OVP 10-Battery Not Present 11- NA
B1	BATSTAT0	Read Only	
B0 (LSB)	EN_NOBATOP	Read/ Write	0-Normal Operation 1-Enables No Battery Operation when termination is disabled (default 0)

EN_NOBATOP (No Battery Operation with Termination Disabled)

The EN_NOBATOP bit is used to enable operation when termination is disabled and no battery is connected. This is useful for factory mode cases where it is desired to do a GSM calibration in the factory. For this application, the TE bit (Bit 2 in Register 0x02h) should be set to a “0” to disable termination and the EN_NOBATOP should be set to a “1”. This feature should not be used during normal operation as it disables the BATOVP and the reverse boost protection circuits.

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Control Register (READ/WRITE)
Memory location: 02, Reset state: 1000 1100

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	RESET	Write Only	Write: 1-Reset all registers to default values 0-No effect Read: always get “1”
B6	NA	Read/Write	NA
B5	NA	Read/Write	NA
B4	NA	Read/Write	NA
B3	EN_STAT	Read/Write	1-Enable STAT output to show charge status, 0-Disable STAT output for charge status. Fault interrupts are still show even when EN_STAT = 0. (default 1)
B2	TE	Read/Write	1-Enable charge current termination, 0-Disable charge current termination (default 1)
B1	$\overline{CE}$	Read/Write	1-Charger is disabled 0-Charger enabled (default 0)
B0 (LSB)	HZ_MODE	Read/Write	1-High impedance mode 0-Not high impedance mode (default 0)

RESET Bit
The RESET bit in the control register (0x02h) is used to reset all the charge parameters. Write “1” to RESET bit to reset all the registers to default values and place the bq24273 into DEFAULT mode and turn off the watchdog timer. The RESET bit is automatically cleared to zero once the bq24273 enters DEFAULT mode.

$\overline{CE}$ Bit (Charge Enable)
The $\overline{CE}$ bit in the control register (0x02h) is used to disable or enable the charge process. A low logic level (0) on this bit enables the charge and a high logic level (1) disables the charge. When charge is disabled, the battery is disconnected from the CS+.

HZ_MODE Bit (High Impedance Mode Enable)
The HZ_MODE bit in the control register (0x02h) is used to disable or enable the high impedance mode. A low logic level (0) on this bit enables the IC and a high logic level (1) puts the IC in a low quiescent current state called high impedance mode.

Control/Battery Voltage Register (READ/WRITE)
Memory location: 03, Reset state: 0001 0100

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	V_{BREG5}	Read/Write	Battery Regulation Voltage: 640mV (default 0)
B6	V_{BREG4}	Read/Write	Battery Regulation Voltage: 320mV (default 0)
B5	V_{BREG3}	Read/Write	Battery Regulation Voltage: 160mV (default 0)
B4	V_{BREG2}	Read/Write	Battery Regulation Voltage: 80mV (default 1)
B3	V_{BREG1}	Read/Write	Battery Regulation Voltage: 40mV (default 0)
B2	V_{BREG0}	Read/Write	Battery Regulation Voltage: 20mV (default 1)
B1	$I_{INLIMIT_IN}$	Read/Write	Input Limit for IN input 0 – 1.5A 1 – 2.5A (default 0)
B0(LSB)	NA	Read/Write	NA

- Charge voltage range is 3.5V–4.44V with the offset of 3.5V and step of 20mV (default 3.6V).

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Vender/Part/Revision Register (READ only)
Memory location: 04, Reset state: 0100 0000

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	Vender2	Read only	Vender Code: bit 2 (default 0)
B6	Vender1	Read only	Vender Code: bit 1 (default 1)
B5	Vender0	Read only	Vender Code: bit 0 (default 0)
B4	PN1	Read only	For I2C Address 6Bh: 00: bq24273 01 – 11: Future product spins
B3	PN0	Read only	
B2	Revision2	Read only	000: Revision 1.0 001:Revision 1.1 010: Revision 2.0 100: Revision 2.2 101: Revision 2.3 110-111: Future Revisions
B1	Revision1	Read only	
B0(LSB)	Revision0	Read only	

Battery Termination/Fast Charge Current Register (READ/WRITE)
Memory location: 05, Reset state: 0011 1110

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	I_{CHRG4}	Read/Write	Charge current: 1200 mA – (default 0)
B6	I_{CHRG3}	Read/Write	Charge current: 600 mA— (default 0)
B5	I_{CHRG2}	Read/Write	Charge current: 300 mA—(default 1)
B4	I_{CHRG1}	Read/Write	Charge current: 150 mA— (default 1)
B3	I_{CHRG0}	Read/Write	Charge current: 75 mA (default 0)
B2	I_{TERM2}	Read/Write	Termination current sense voltage: 200 mA (default 0)
B1	I_{TERM1}	Read/Write	Termination current sense voltage: 100 mA (default 1)
B0(LSB)	I_{TERM0}	Read/Write	Termination current sense voltage: 50 mA (default 0)

- Charge current sense offset is 550mA and default charge current is 1000mA
- Termination threshold offset is 50mA and default termination current is 150mA

V_{IN-DPM} Voltage/ DPPM Status Register
Memory location: 06, Reset state: xx00 0000

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	NA	Read Only	NA
B6	DPM_STATUS	Read Only	1 – V_{IN}-DPM mode is active 0 – V_{IN}-DPM mode is not active
B5	NA	Read/Write	NA
B4	NA	Read/Write	NA
B3	NA	Read/Write	NA
B2	$V_{INDPM2(IN)}$	Read/Write	IN input V_{IN-DPM} voltage: 320 mV (default 0)
B1	$V_{INDPM1(IN)}$	Read/Write	IN input V_{IN-DPM} voltage: 160 mV (default 0)
B0(LSB)	$V_{INDPM0(IN)}$	Read/Write	IN input V_{IN-DPM} voltage: 80 mV (default 0)

- V_{IN-DPM} voltage offset is 4.20 V and default V_{IN-DPM} threshold is 4.20 V.

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Safety Timer/ NTC Monitor Register (READ/WRITE)
Memory location: 07, Reset state: 1001 1xxx

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	2XTMR_EN	Read/Write	1 – Timer slowed by 2x when in thermal regulation, input current limit, V_{IN_DPM} or DPPM 0 – Timer not slowed at any time (default 0)
B6	TMR_1	Read/Write	Safety Timer Time Limit 00 – 27 minute fast charge 01 – 6 hour fast charge 10 – 9 hour fast charge 11 – Disable safety timers (default 00)
B5	TMR_2	Read/Write	
B4	NA	Read/Write	NA
B3	TS_EN	Read/Write	0 – TS function disabled 1 – TS function enabled (default 1)
B2	TS_FAULT1	Read Only	TS Fault Mode: 00— Normal, No TS fault 01— TS temp < T_{COLD} or TS temp > T_{HOT}(Charging suspended) 10— T_{COOL} > TS temp > T_{COLD} (Charge current reduced by half, bq24273 only) 11— T_{WARM} < TS temp < T_{HOT} (Charge voltage reduced by 140mV, bq24273 only)
B1	TS_FAULT0	Read Only	
B0(LSB)	LOW_CHG	Read/Write	0 – Charge current as programmed in Register 0x05 1 – Charge current half programmed value in Register 0x05 (default 0)

LOW_CHG Bit (Low Charge Mode Enable)

The LOW_CHG bit is used to reduce the charge current to half of the programmed value. This feature is used by systems where battery NTC is monitored by the host and requires a reduced charge current setting or by systems that need a “preconditioning” current for low battery voltages. Write a “1” to this bit to charge at half of the programmed charge current. Write a “0” to this bit to charge at the programmed charge current.

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APPLICATION INFORMATION

OUTPUT INDUCTOR AND CAPACITOR SELECTION GUIDELINES

When selecting an inductor, several attributes must be examined to find the right part for the application. First, the inductance value should be selected. The bq24273 is designed to work with 1.5µH to 2.2µH inductors. The chosen value will have an effect on efficiency and package size. Due to the smaller current ripple, some efficiency gain is reached using the 2.2µH inductor, however, due to the physical size of the inductor, this may not be a viable option. The 1.5µH inductor provides a good tradeoff between size and efficiency.

Once the inductance has been selected, the peak current must be calculated in order to choose the current rating of the inductor. Use equation 2 to calculate the peak current.

$$I_{PEAK} = I_{LOAD(MAX)} \times \left(1 + \frac{\%_{RIPPPLE}}{2}\right) \quad (5)$$

The inductor selected must have a saturation current rating less than or equal to the calculated I_{PEAK}. Due to the high currents possible with the bq24273, a thermal analysis must also be done for the inductor. Many inductors have 40°C temperature rise rating. This is the DC current that will cause a 40°C temperature rise above the ambient temperature in the inductor. For this analysis, the typical load current may be used adjusted for the duty cycle of the load transients. For example, if the application requires a 1.5A DC load with peaks at 2.5A 20% of the time, a Δ40°C temperature rise current must be greater than 1.7A:

$$I_{TEMPRISE} = I_{LOAD} + D \times I\left(_{PEAK} - I_{LOAD}\right) = 1.5A + 0.2 \times \left(2.5A - 1.5A\right) = 1.7A \quad (6)$$

The bq24273 provides internal loop compensation. Using this scheme, the bq24273 is stable with 10µF to 200µF of local capacitance. The capacitance on the BAT rail can be higher if distributed amongst the rail. To reduce the output voltage ripple, a ceramic capacitor with the capacitance between 10µF and 47µF is recommended for local bypass to CS+.

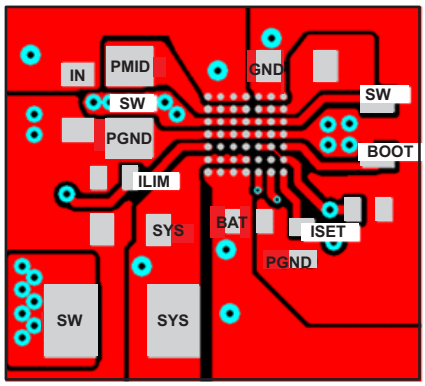
PCB LAYOUT GUIDELINES

It is important to pay special attention to the PCB layout. The following provides some guidelines:

- To obtain optimal performance, the power input capacitors, connected from the PMID input to PGND, must be placed as close as possible to the bq24273
- Place 4.7µF input capacitor as close to PMID pin and PGND pin as possible to make high frequency current loop area as small as possible. Place 1µF input capacitor GNDs as close to the respective PMID cap GND and PGND pins as possible to minimize the ground difference between the input and PMID_.
- The local bypass capacitor from CS+ to GND should be connected between the CS+ pin and PGND of the IC. The intent is to minimize the current path loop area from the SW pin through the LC filter and back to the PGND pin.
- Place all decoupling capacitor close to their respective IC pin and as close as to PGND (do not place components such that routing interrupts power stage currents). All small control signals should be routed away from the high current paths.
- The PCB should have a ground plane (return) connected directly to the return of all components through vias (two vias per capacitor for power-stage capacitors, one via per capacitor for small-signal components). It is also recommended to put vias inside the PGND pads for the IC, if possible. A star ground design approach is typically used to keep circuit block currents isolated (high-power/low-power small-signal) which reduces noise-coupling and ground-bounce issues. A single ground plane for this design gives good results. With this small layout and a single ground plane, there is no ground-bounce issue, and having the components segregated minimizes coupling between signals.
- The high-current charge paths into IN, BAT, CS+ and from the SW pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces. The PGND pins should be connected to the ground plane to return current through the internal low-side FET.
- For high-current applications, the balls for the power paths should be connected to as much copper in the board as possible. This allows better thermal performance as the board pulls heat away from the IC.

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Sample Layout



(YFF Package)

Figure 10. PCB Layout Example

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24273YFFR	ACTIVE	DSBGA	YFF	49	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24273	Samples
BQ24273YFFT	ACTIVE	DSBGA	YFF	49	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24273	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

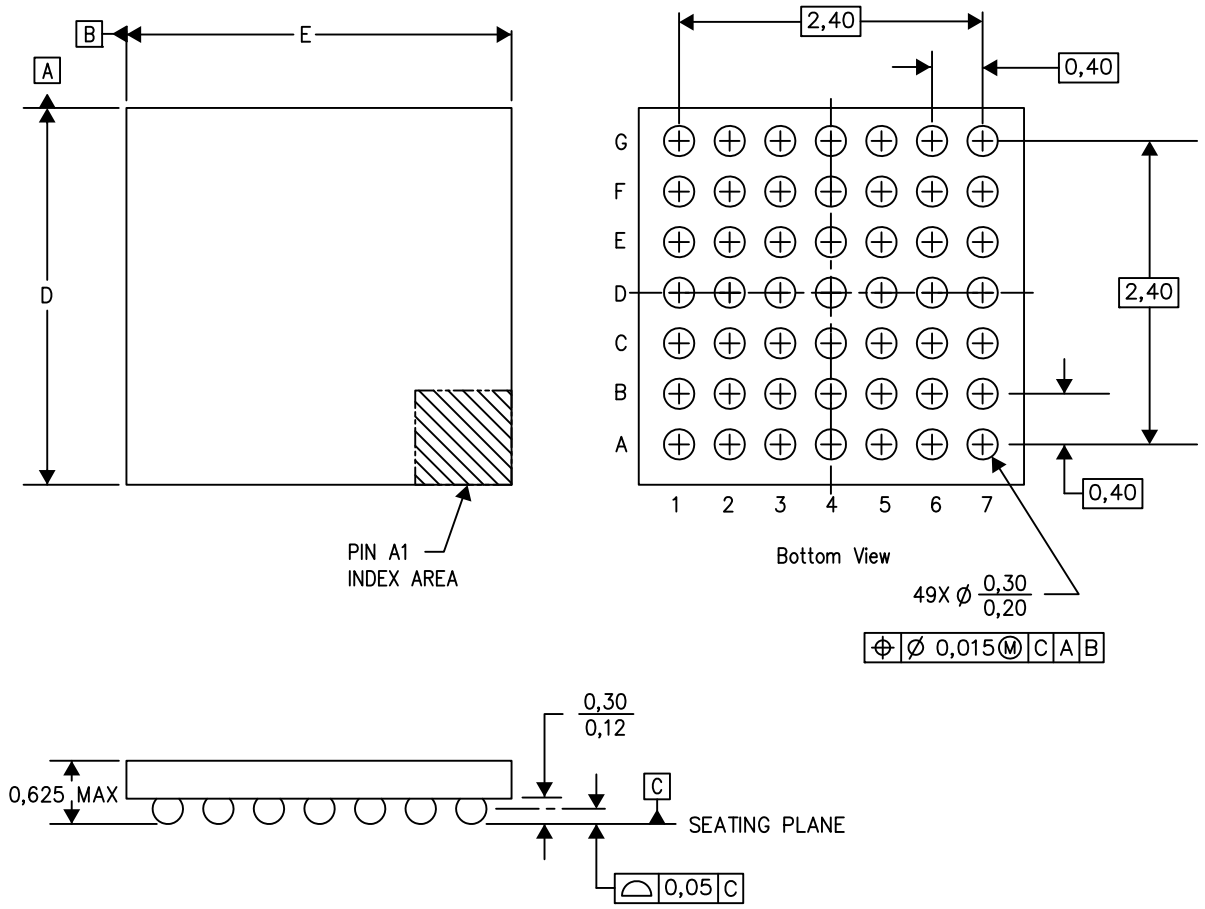
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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YFF (R–XBGA–N49) DIE–SIZE BALL GRID ARRAY



4207625–16/AO 12/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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