1.1A, Single-Input 5-V Power Supply IC for Wireless Power Applications

Check for Samples: bq25046

FEATURES

- **30V Input Rating, with 15V Over-Voltage Protection (OVP) Threshold**
- **Integrated Charge Current Sense for Wireless Power Transfer Efficiency Monitoring**
- **3.3V, 15mA integrated Low Dropout Linear Regulator (VDD3.3) Supplies Power to MSP430BQ1010 Directly**
- **2% Output Voltage Regulation**
- **Pin Selectable 100mA and 400mA Current Limit Enables Robust Communication in Wireless Power Systems at any Output Current Level**
- **Soft-Start Feature to Reduce Inrush Current**
- **Status Indication – Power Good ($\overline{PG}$) and Output Enabled ($\overline{CHG}$)**
- **Available in Small 2mm × 3mm DFN-10 Package**

APPLICATIONS

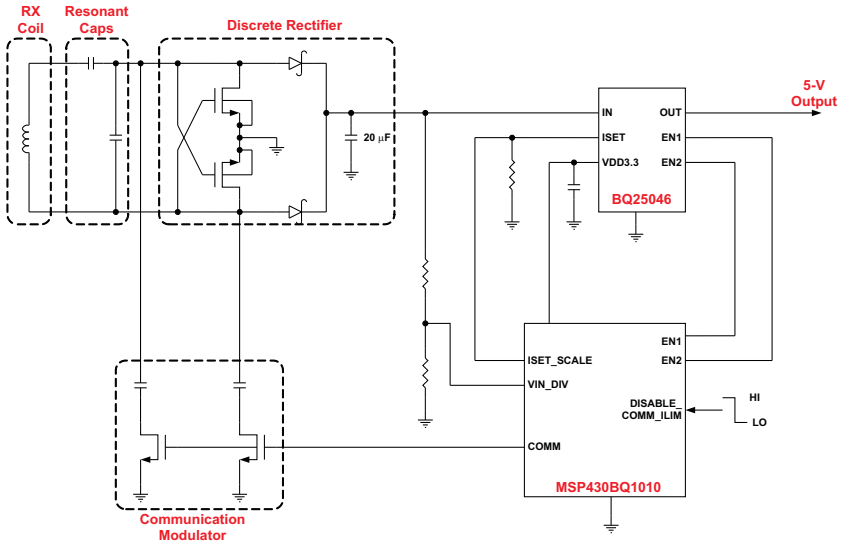
- **Wireless Power Applications**
- **Smart Phones**
- **PDAs**
- **MP3 Players**
- **Low-Power Handheld Devices**

DESCRIPTION

The bq25046 is a highly integrated linear power supply IC targeted at both wired and wireless power applications. With an accurate 5-V regulated output and integrated 3.3-V LDO, the bq25046 is an ideal solution for wireless power supply solutions up to 5 W.

The bq25046 integrates several functions which enable a wireless charging solution within a small area and low component count. These include a 3.3-V LDO which drives an MSP430BQ1010 wireless controller, high-accuracy current sense for calculating receiver-side power usage, 100mA/400mA current limits enable robust communication at all load current levels, and integrated pass FET acts as load disconnect switch and 5-V regulator to protect downstream circuitry. In addition, the bq25046 has an absolute maximum input voltage of 30 V and an OVP threshold of 15 V, which enables safe and robust operation in inductive power transfer systems that use either resistive or capacitive load modulation.

APPLICATION SCHEMATIC



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2010, Texas Instruments Incorporated

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PART NUMBER(1)	$V_{OUT(REG)}$	V_{OVP}	$V_{VDD3.3}$	MARKING
bq25046DQCR	5.0 V	15 V	3.3 V	OFS
bq25046DQCT	5.0 V	15 V	3.3 V	OFS

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX
Input Voltage	IN (with respect to VSS)	–0.3 V	30 V
Output Voltage	OUT, VDD3.3, $\overline{CHG}$, $\overline{PG}$ (with respect to VSS)	–0.3 V	7 V
Input voltage	EN1, EN2, ISET (with respect to VSS)	–0.3 V	7 V
Input Current	IN	1.5 A	
Output Current (Continuous)	OUT	1.5 A	
	VDD3.3	100 mA	
Output Sink Current	$\overline{CHG}$, $\overline{PG}$	15 mA	
Junction temperature, T_J		–40 °C	150 °C
Storage temperature, T_{STG}		–65 °C	150 °C
ESD protection	HBM		2 kV
	CDM		500 V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

THERMAL INFORMATION

THERMAL METRIC(1)		bq25046 DFN 10 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	71.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	65.2	
θ_{JB}	Junction-to-board thermal resistance	85.2	
ψ_{JT}	Junction-to-top characterization parameter	0.6	
ψ_{JB}	Junction-to-board characterization parameter	29.6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	5.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{IN}	IN voltage range	3.3	26	V
	IN operating voltage range	3.3	9	
I_{IN}	Input current, IN pin		1.5	A
I_{OUT}	Current, OUT pin		1.5	A
T_J	Junction Temperature	–40	125	ºC
R_{ISET}	Current limit programming resistor	470	5360	Ω

Copyright © 2010, Texas Instruments Incorporated

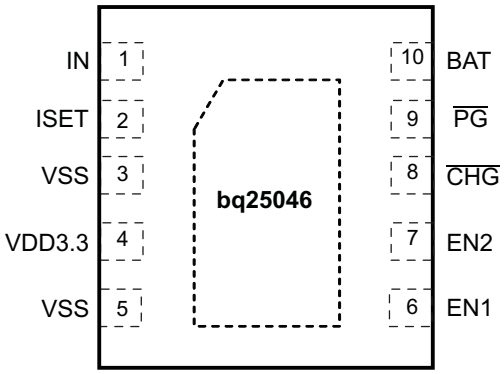
ELECTRICAL CHARACTERISTICS

Over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{UVLO}	Under-voltage lock-out	V_{IN}: 0V → 4 V	3.15	3.30	3.45	V
$V_{HYS-UVLO}$	Hysteresis on UVLO	V_{IN}: 4V → 0 V	200	260	320	mV
V_{OVP}	Input over-voltage protection threshold	V_{IN}: 13V → 17 V	14.5	15.0	15.5	V
$V_{HYS-OVP}$	Hysteresis on OVP	V_{IN}: 17V → 13 V		150		mV
$t_{BLK(OVP)}$	Input over-voltage blanking time			115		µs
$t_{REC(OVP)}$	Input over-voltage recovery time	Time measured from V_{IN}: 17V → 13V 1µs fall-time to $\overline{CHG}$ = LO, V_{OUT} = 3.5 V		500		µs
$I_{IN-USB-CL}$	USB input I-Limit 100mA	USB100 programmed by EN1/EN2, R_{ISET} < 1.1 kΩ	85	91	96	mA
	USB input I-Limit 400mA	USB500 programmed by EN1/EN2, R_{ISET} < 1.1 kΩ	360	400	440	mA
ISET SHORT CIRCUIT TEST						
RISET	Continuous Monitor	R_{ISET}: 500 ≥ 200, IC latches off after $t_{DGL-SHORT}$	300		460	Ω
$t_{DGL-SHORT}$	Deglitch time transition from ISET to IC latched off			1.5		ms
$I_{LIM-ISET-SHRT}$	Current limit with ISET shorted	ISET = 0V, IC latches off after $t_{DGL-SHORT}$	1.5	1.9	2.2	A
QUIESCENT CURRENT						
$I_{OUT(PDWN)}$	Quiescent current into OUT	V_{IN} = 0V			1	µA
$I_{IN(STDBY)}$	Standby current into IN pin	V_{IN} ≤ 10V, EN1=EN2=Hi			400	µA
		V_{IN} < 16V, EN1=EN2=Hi			800	µA
I_{CC}	Active supply current, IN pin	V_{IN} = 6V, no load on OUT pin, V_{OUT} > $V_{OUT(REG)}$, IC enabled			3	mA
OUT						
$V_{OUT(REG)}$	Output voltage		4.9	5.0	5.1	V
I_{OUT}	Programmed Output current limit range	$V_{OUT(REG)}$ > V_{OUT} > V_{LOWV}, V_{IN} = 5V, R_{ISET} = 470 to 7.5 kΩ, User Programmable set by EN1/EN2	100		1100	mA
$V_{DO(IN-OUT)}$	V_{IN} – V_{OUT}	V_{IN} = 4.9V and I_{OUT} = 1 A		280	512	mV
I_{OUT}	Output current limit formula	$V_{OUT(REG)}$ > V_{OUT} > V_{LOWV}, V_{IN} = 5V, User Programmable set by EN1/EN2	KISET/RI SET			A
K_{ISET}	Current limit factor		480	530	580	AΩ
VDD3.3						
$V_{VDD3.3}$	VDD3.3 Output Voltage		3.2	3.3	3.4	V
$I_{VDD3.3(Max)}$	VDD3.3 Maximum Output Current		15			mA
THERMAL REGULATION						
$T_{J(REG)}$	Temperature Regulation Limit		115	125	135	°C
$T_{J(OFF)}$	Thermal shutdown temperature			155		°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis			20		°C
LOGIC LEVELS ON EN1, EN2						
V_{IL}	Logic LOW input voltage				0.4	V
V_{IH}	Logic HIGH input voltage		1.4			V
$R_{PULLDOWN}$	Pulldown resistor for EN1 and EN2			260		kΩ
LOGIC LEVELS ON $\overline{CHG}$ AND $\overline{PG}$						
V_{OL}	Output LOW voltage	I_{SINK} = 5 mA			0.4	V
I_{IH}	Leakage current	$V_{/CHG}$ = $V_{/PG}$ =5 V		5		µA

Copyright © 2010, Texas Instruments Incorporated

PIN CONFIGURATION



10-pin 3mm x 3mm DFN

PIN FUNCTIONS

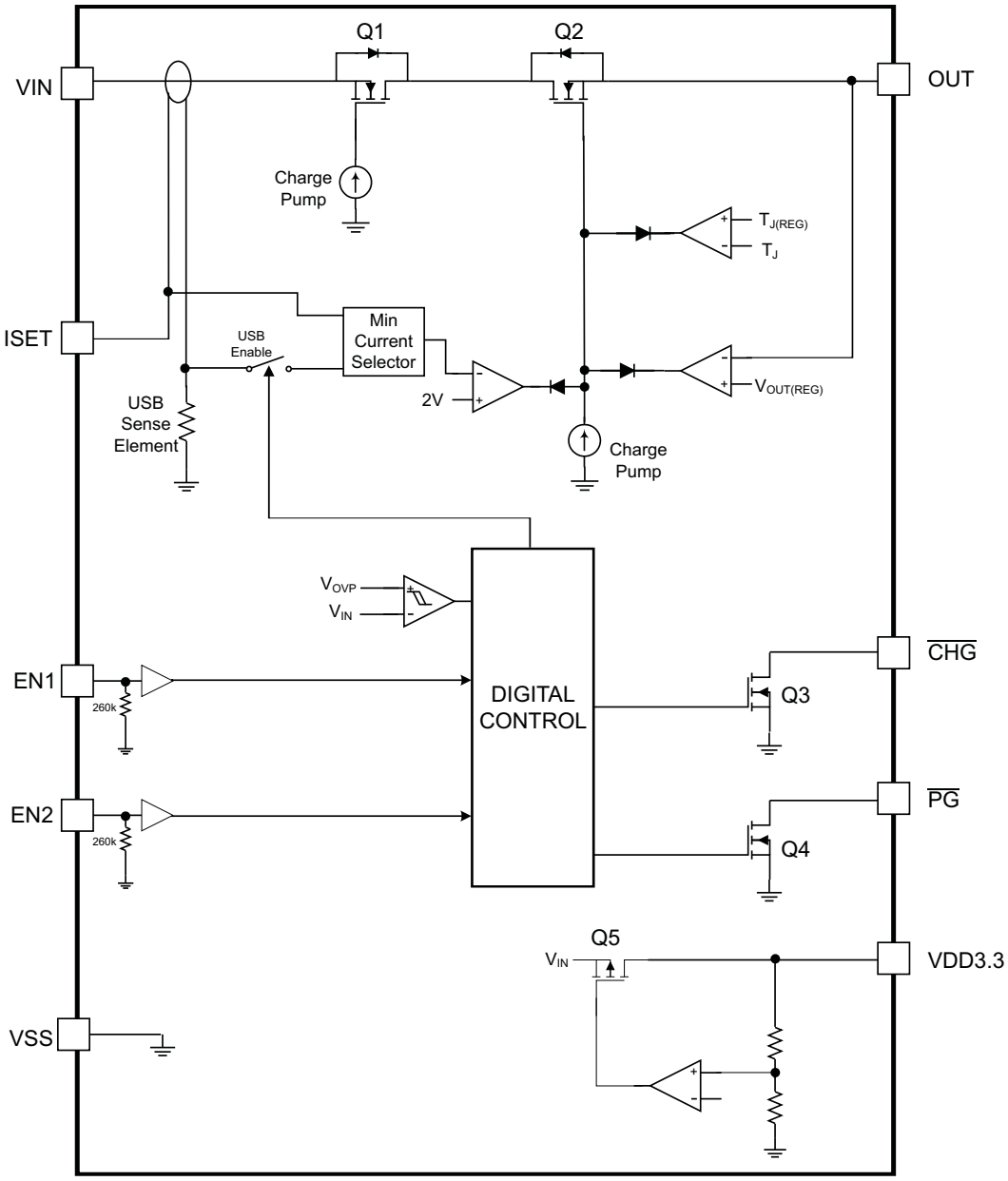
PIN		I/O	DESCRIPTION
NAME	NO.		
IN	1	I	Input power supply. IN is connected to the external DC supply (AC adapter or USB port) or wireless rectifier. Bypass IN to VSS with at least a 1μF ceramic capacitor for wired applications and 10 μF typical for wireless power applications.
ISET	2	I	Current programming input. Connect a resistor from ISET to VSS to program the current limit when the user programmable mode is selected by EN1 and EN2. The resistor range is between 470Ω and 5360Ω to set the current between 100mA and 1.1A.
VSS	3, 5	–	Ground terminal. Connect to the thermal pad and the ground plane of the circuit.
VDD3.3	4	O	3.3V output. VDD3.3 is regulated to 3.3V and drives up to 15mA. Bypass VDD3.3 to VSS with at least a 0.1μF ceramic capacitor. VDD3.3 is enabled when VIN is above the UVLO voltage.
EN1	6	I	Current Limit Selection inputs. EN1 and EN2 are used to select the current limit and enable/disable the device. See Table 1 for current limit settings.
EN2	7	I	
$\overline{CHG}$	8	O	IC Enabled output. $\overline{CHG}$ is pulled to VSS when the bq25046 is enabled. $\overline{CHG}$ is high impedance when the IC is disabled.
$\overline{PG}$	9	O	Power good output. $\overline{PG}$ is an open-drain output that pulls to VSS when the input power is above the UVLO and below the OVP threshold. $\overline{PG}$ is high impedance when outside this range.
OUT	10	O	5V LDO output. Connect OUT to the system input. OUT regulates to 5.0V. Bypass OUT to VSS with at least a 1μF ceramic capacitor.
Thermal Pad		–	There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times.

Table 1. EN1 and EN2 Input Table

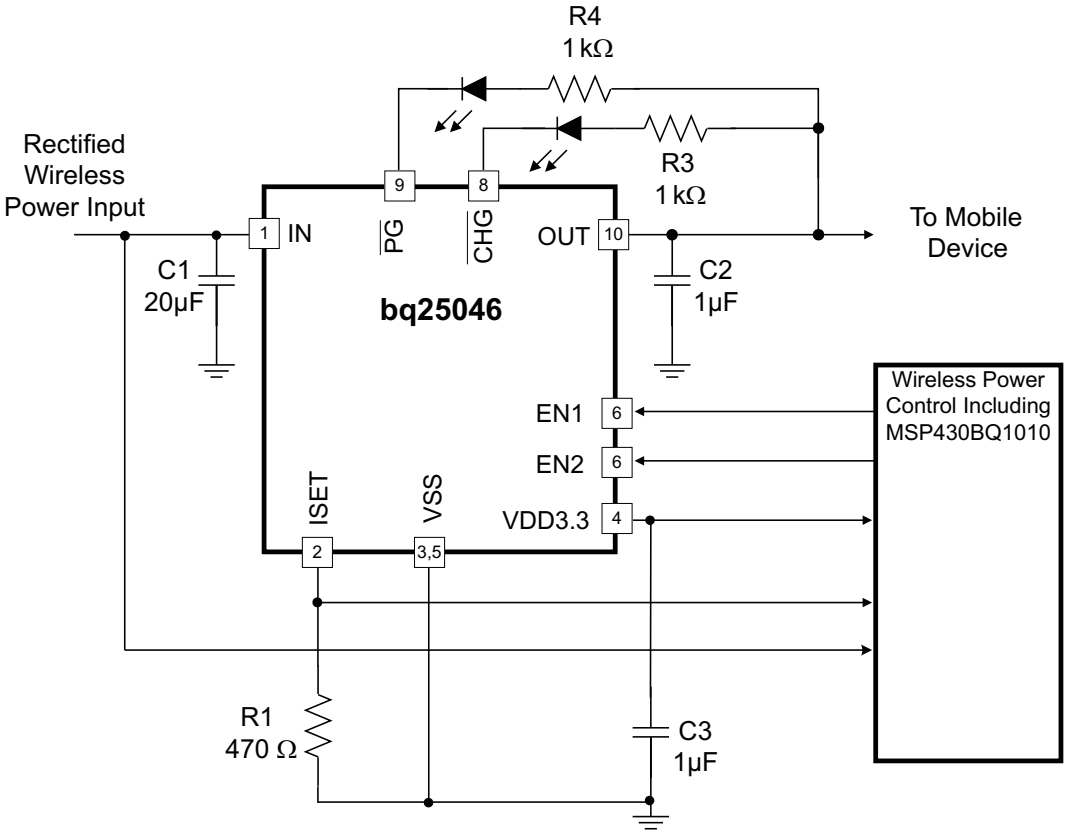
EN1	EN2	CURRENT LIMIT
Low	Low	100 mA
Low	High	400 mA
High	Low	ISET
High	High	IC Off

Copyright © 2010, Texas Instruments Incorporated

BLOCK DIAGRAM



TYPICAL APPLICATION CIRCUIT



DETAILED FUNCTIONAL DESCRIPTION

INPUT OVER VOLTAGE PROTECTION

The bq25046 contains an input over voltage protection circuit that disables the OUT output when the input voltage rises above V_{OVP}. This prevents damage from faulty adapters or open loop rectifiers. The OVP circuitry contains a 150 µs deglitch that prevents ringing on the input from line transients from tripping the OVP circuitry falsely. If an adapter with an output greater than V_{OVP} is plugged in, the IC completes powers up and but does not enable the output. The VDD3.3 output remains on to maintain power and protect the MSP430BQ1010 circuit. The OUT LDO remains disabled until the input voltage falls below V_{OVP}.

CURRENT LIMIT (ISET, EN1, EN2)

The current limit is programmed using the EN1, EN2 and ISET inputs. The EN1 and EN2 inputs allow the user to select USB100 mode, USB400 mode, or the user programmable current limit set by ISET. The user programmable current is set by connecting a resistor from ISET to VSS. The value of the resistor is determined by:

$$R_{ISET1} = \frac{K_{ISET}}{I_{LIMIT}} \quad (1)$$

Where K_{ISET} = 375 and the current limit (I_{LIMIT}) must be programmed between 100mA and 1.1A.

15mA LDO (VDD3.3)

The VDD3.3 output of the bq25046 is a low dropout linear regulator (VDD3.3) that supplies up to 15mA while regulating to $V_{VDD3.3}$. The VDD3.3 is active whenever the input voltage is above V_{UVLO}. It is not affected by the EN1 and EN2 inputs or OVP. The VDD3.3 output is used to power circuitry such as MSP430BQ1010.

Copyright © 2010, Texas Instruments Incorporated

OUT STATUS (/CHG)

The bq25046 contains an open drain $\overline{CHG}$ output that indicates when the bq25046 device in enabled. $\overline{CHG}$ output is pulled to ground when the input voltage is above UVLO and less than OVP and the device is enabled. $\overline{CHG}$ goes high impedance to signal that the OUT output is not available.

Connect $\overline{CHG}$ to the required logic level voltage through a 1kΩ to 100kΩ resistor to use the signal with a microprocessor. Additionally, $\overline{CHG}$ may be used to drive an LED for a visual charging status signal. $I_{/CHG}$ must be below 15mA.

UNDER VOLTAGE LOCKOUT

The bq25046 remains in power down mode when the input voltage is below the undervoltage lockout threshold (VUVLO). During this mode, the control inputs (EN1 and EN2) are ignored. The FET connected between IN and OUT is off, VDD3.3 is off and the status outputs ($\overline{CHG}$ and $\overline{PG}$) are high impedance. Once the input voltage rises above V_{UVLO}, the internal circuitry is turned on and the normal operating procedures are followed.

Power Good (/PG)

The bq25046 contains a $\overline{PG}$ signal that indicates when a valid input source is connected. The $\overline{PG}$ output goes low when an input source between V_{UVLO} and V_{OVP} is connected. $\overline{PG}$ transitions after the deglitch times out. The deglitch depends on the state of the bq25046 and the condition. Table 2 shows the deglitch for different conditions.

Table 2. Deglitch for Different Conditions

CONDITION	$\overline{PG}$ Deglitch (Measured from Event to $\overline{PG}$ High or Low)	
	bq25046 ENABLED	bq25046 DISABLED (EN1=EN2=0)
Entering OVP (VIN = 5.5 V→11 V)	100 µs	0
Leaving OVP (VIN = 11 V→5.5 V)	450 µs	500 µs
Entering UVLO (VIN = 5.5 V→2.5 V)	0	0
Leaving UVLO (VIN = 2.5 V→5.5 V)	230 µs	230 µs

$\overline{PG}$ may be pulled up to any voltage rail less than the maximum rating on the $\overline{PG}$ output. Another option is to pull up $\overline{PG}$ to the LDO output.

THERMAL REGULATION AND THERMAL SHUTDOWN

The bq25046 contains a thermal regulation loop that monitors the die temperature continuously. If the temperature exceeds $T_{J(REG)}$, the device automatically reduces the input current limit to prevent the die temperature from increasing further. In some cases, the die temperature continues to rise despite the operation of the thermal loop, particularly under high V_{IN} conditions. If the die temperature increases to $T_{J(OFF)}$, the IC is turned off. Once the device die temperature cools by $T_{J(OFF-HYS)}$, the device turns on and returns to thermal regulation. Continuous over-temperature conditions result in the pulsing of the load current. If the junction temperature of the device exceeds $T_{J(OFF)}$, the FET is turned off. The FET is turned back on when the junction temperature falls below $T_{J(OFF)} – T_{J(OFF-HYS)}$.

Note that these features monitor the die temperature of the bq25046. This is not synonymous with ambient temperature. Self heating exists due to the power dissipated in the IC because of the linear nature of the regulation algorithm.

Copyright © 2010, Texas Instruments Incorporated

APPLICATION INFORMATION

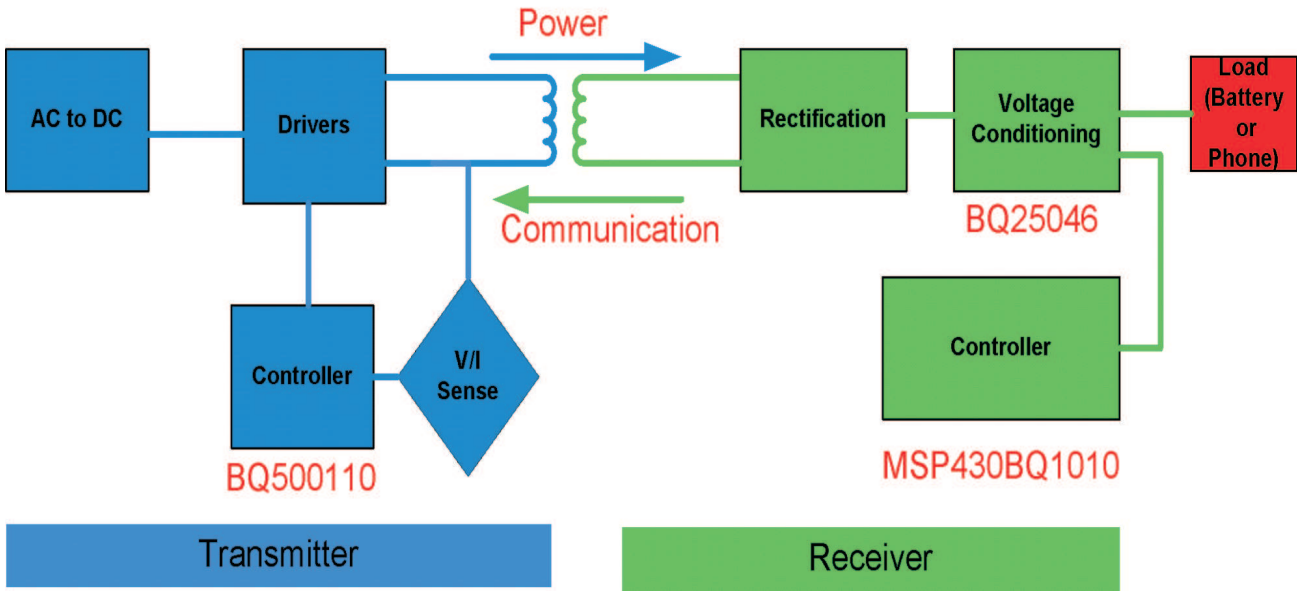


Figure 1. Wireless Power System

GENERAL OVERVIEW OF A WIRELESS POWER SYSTEM

Figure 1 presents a block diagram of a wireless power system, which consists of a transmitter and receiver. The transmitter consists of an AC-DC power stage, followed by a transmitter coil driver, coil voltage and coil current sensing block, and a wireless power controller (BQ500110). The receiver consists of a receiver coil, rectifier, BQ25046 voltage regulation circuit, and MSP430BQ1010 wireless power controller. The output of the system is the BQ25046 5-V regulated output voltage which is used as a power supply to the charger in a cellular phone or other mobile device. The system shown in Figure 2 implements wireless power transfer via inductive coupling between the transmitter and receiver. In this system the transmitter drives a transmit coil with a frequency between 100 and 200 kHz and the receiver coil, which is in close proximity to the transmitter coil, rectifies the received voltage to power the BQ25046. In addition, the receiver continuously monitors its operating point (coil voltage and coil current) and communicates correction packets to the transmitter via backscatter modulation.

Utilizing BQ25046 in a Wireless Power System

Figure 2 shows the BQ25046 used in a wireless power receiver solution. In this application a receiver coil connects to a half-synchronous rectifier which includes a rectifier filter capacitor. The rectifier voltage is connected directly to the IN pin of the BQ25046 and the BQ25046 generates a 3.3 V LDO output that is used to power an MSP430BQ1010 wireless power supply controller. The MSP430BQ1010 monitors the rectifier voltage and output current and communicates to the transmitter via the communication modulator to optimize the power delivered to a mobile device. The OUT pin of the BQ25046 delivers 5-V to a mobile device at power levels up to 5W.

Copyright © 2010, Texas Instruments Incorporated

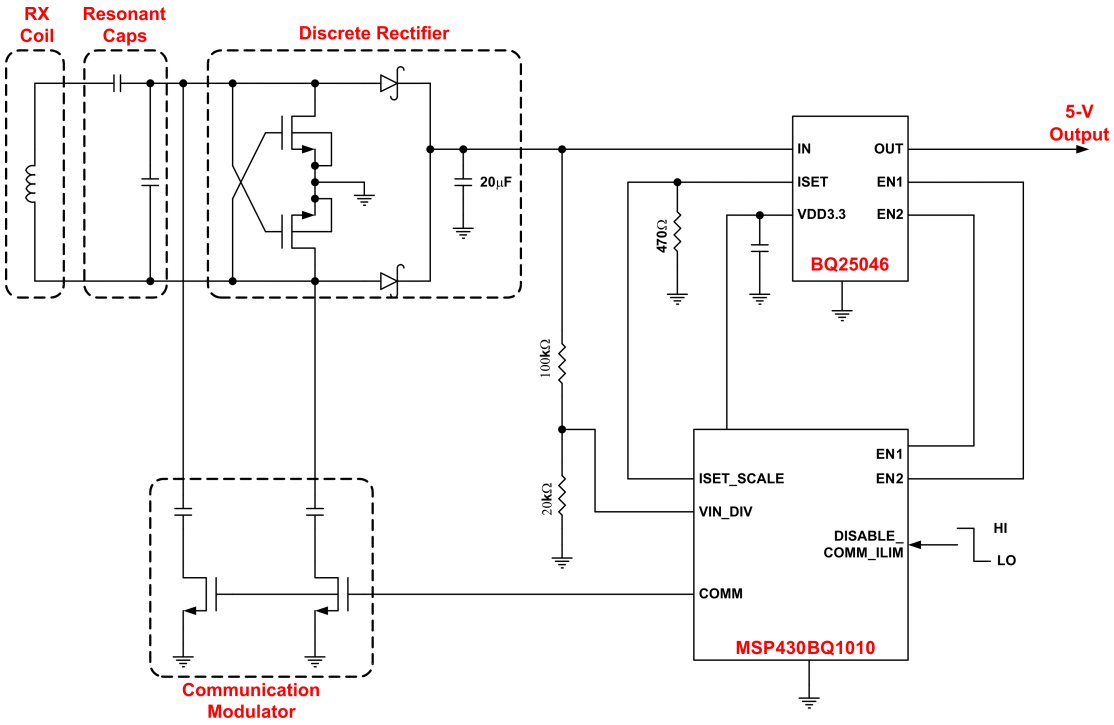


Figure 2. bq25046 Used in a Contactless Power Receiver

When used in conjunction with the MSP430BQ1010 wireless power controller, the BQ25046 is an ideal solution for wireless power systems. The key features of the BQ25046 for wireless power include 30-V input protection and 15-V OVP to enable safe operation in the case of a load dump or parasitic magnetic field, 3.3-V LDO that can be connected directly to the MSP430BQ1010, 5-V output regulation voltage can interface to a wide array of mobile devices, integrated current sensing can be used to monitor power usage, and EN1/EN2 control interface provides a simple means to enable and disable BQ25046 and also implement current limiting.

Copyright © 2010, Texas Instruments Incorporated

Figure 3 shows typical waveforms for BQ25046 used in the wireless power system shown in Figure 2. In this plot the BQ25046 IN voltage is blue, OUT voltage is red, $\overline{PG}$ voltage is green, and $\overline{CHG}$ voltage is magenta. As you can see at the initial ping (i.e., beginning of power transfer) the IN voltage rises to 5 V and then the MSP430BQ1010 begins to communicate to the transmitter via load modulation. After sending several messages to establish communication with the transmitter, the BQ25046 OUT voltage is enabled and then the $\overline{CHG}$ pin is pulled low. From this point forward the MSP430BQ1010 periodically communicates with the transmitter, and a 5-V regulated DC output voltage is present at the BQ25046 OUT pin.

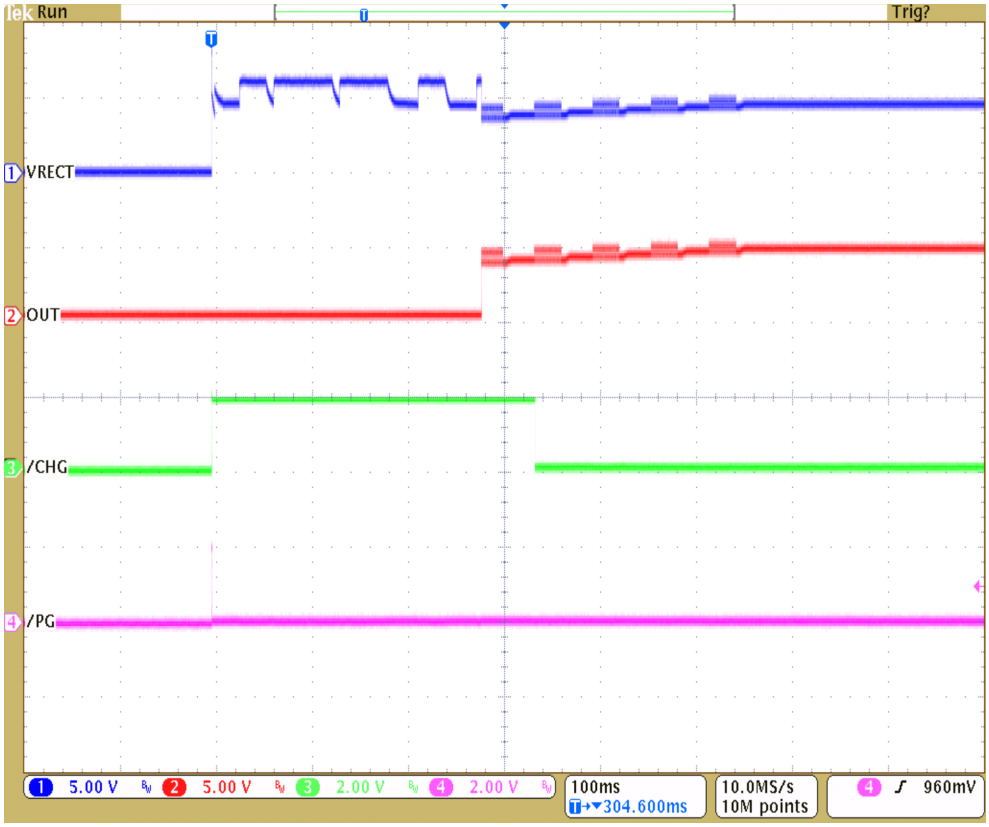


Figure 3. Power-Up In a Wireless Power Application

Copyright © 2010, Texas Instruments Incorporated

Figure 4 shows how the internal current limits on BQ25046 can be used in a wireless power application. If the Disable_Comm_Ilimit pin on the MSP430BQ1010 is pulled low, then the USB current limit on the BQ25046 will be enabled during communication. In Figure 4 it can be seen that during every communication packet the BQ25046 EN1 pin is pulled low, which will limit the BQ25046 OUT current to 100mA during communication. In some applications this will improve the robustness of the communication by limiting load modulation due to dynamic loading.

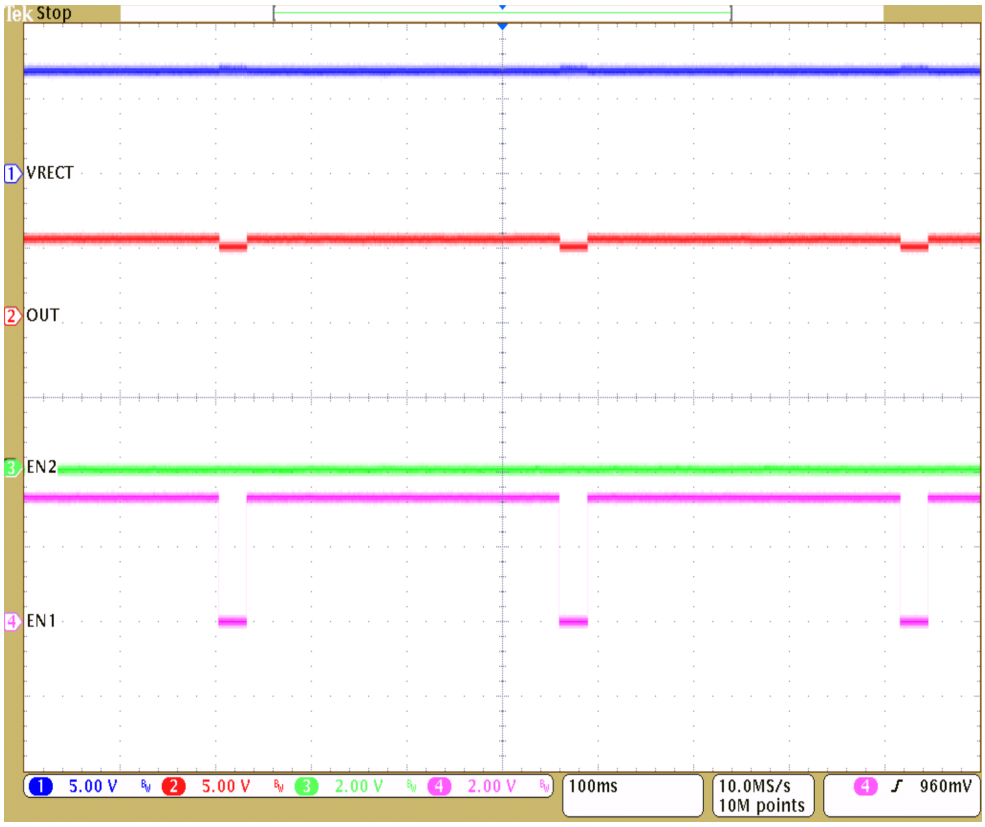


Figure 4. Utilizing Internal bq25046 Current Limit In a Wireless Power Application

If load modulation during communication is not a concern then Disable_Comm_Ilim can be pulled high and the BQ25046 will always deliver full rated current based on the ISET programming resistor. Figure 5 presents an example of a wireless power application where EN1 is always high so that the ISET current limit is always used.

Copyright © 2010, Texas Instruments Incorporated

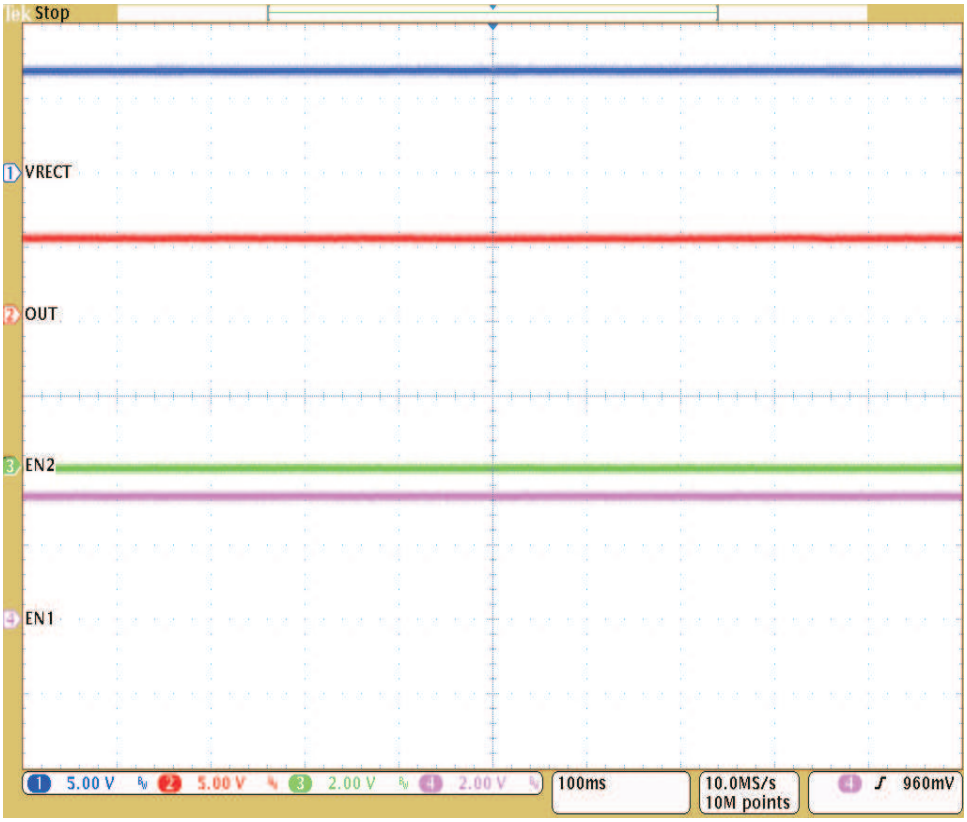


Figure 5. Wireless Power Application in ISET Mode

SELECTION OF INPUT/OUTPUT CAPACITORS

For wireless power applications a rectifier filter capacitor is required between the IN pin and ground to minimize ripple at the BQ25046 input. For applications with output current greater than 500 mA, a ceramic capacitor of at least 20 μF is required to minimize ripple. In addition, board trace resistance between the IN pin, rectifier capacitor, and ground should be minimized. For wired applications a 1μF capacitor placed in close proximity between the IN pin and GND is generally sufficient

The linear regulator in the bq25046 requires a capacitor from OUT to GND for loop stability. Connect a 1μF ceramic capacitor from OUT to GND close to the pins for best results. More output capacitance may be required to minimize the output droop during large load transients.

The VDD3.3 also requires an output capacitor for loop stability. Connect at least a 1μF ceramic capacitor from VDD3.3 to GND close to the pins. For improved transient response, this capacitor may be increased.

THERMAL CONSIDERATIONS

The bq25046 is packaged in a thermally enhanced QFN package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application note entitled: *QFN/SON PCB Attachment Application Note* (SLUA271).

Copyright © 2010, Texas Instruments Incorporated

The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

$$\vartheta_{JA} = \frac{T_J - T_A}{P_D} \quad (2)$$

Where:

T_J = chip junction temperature
T_A = ambient temperature
P_D = device power dissipation

Factors that can greatly influence the measurement and calculation of θ_{JA} include:

- Whether or not the device is board mounted
- Trace size, composition, thickness, and geometry
- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test and airflow
- Whether other surfaces are in close proximity to the device being tested

The device power dissipation, P_D, is a function of the current and the voltage drop across the internal PowerFET. It can be calculated from Equation 3:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (3)$$

If the board thermal design is not adequate the programmed current limit may not be achieved under maximum input voltage, as the thermal loop can be active, effectively reducing the current limit to avoid excessive IC junction temperature

PCB LAYOUT CONSIDERATIONS

It is important to pay special attention to the PCB layout. The following provides some guidelines:

- To obtain optimal performance, the decoupling capacitor from IN to GND (thermal pad) and the output filter capacitors from OUT to GND (thermal pad) should be placed as close as possible to the bq25046, with short trace runs to both IN, OUT and GND (thermal pad).
- All low-current GND connections should be kept separate from the high-current paths.
- Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The high current paths into IN pin and from the OUT pin must be sized appropriately for the maximum current in order to avoid voltage drops in these traces.
- The bq25046 is packaged in a thermally enhanced QFN package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB); this thermal pad is also the main ground connection for the device. Connect the thermal pad to the PCB ground connection. Full PCB design guidelines for this package are provided in the application note entitled: *QFN/SON PCB Attachment Application Note* (SLUA271).

Copyright © 2010, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ25046DQCR	ACTIVE	WSON	DQC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OFS	Samples
BQ25046DQCT	ACTIVE	WSON	DQC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OFS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

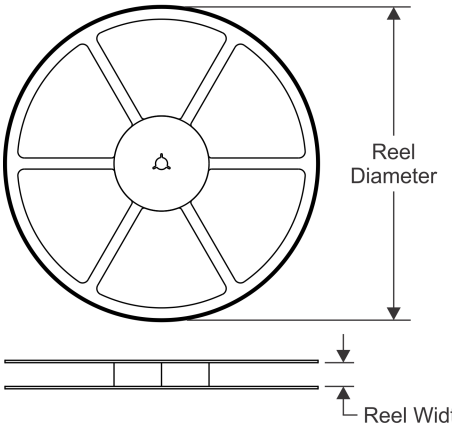
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

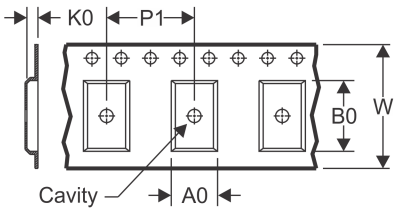
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

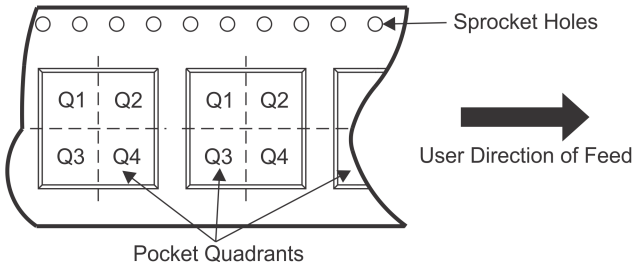


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

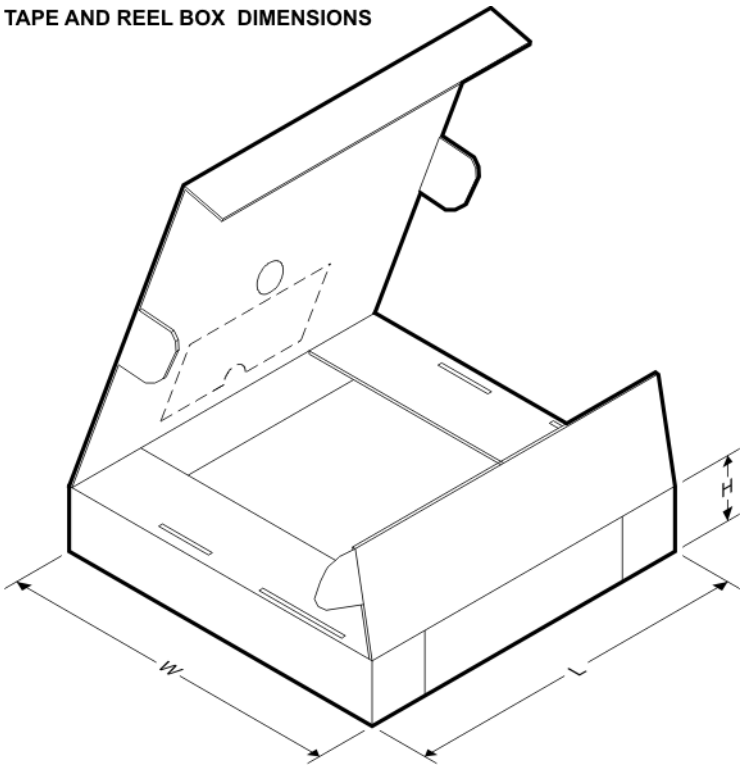
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25046DQCR	WSON	DQC	10	3000	179.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1
BQ25046DQCT	WSON	DQC	10	250	179.0	8.4	2.3	3.2	1.0	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



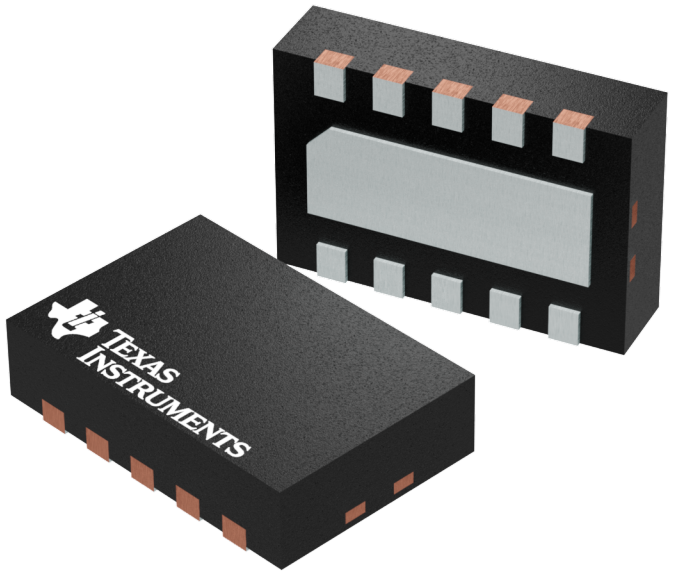
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25046DQCR	WSON	DQC	10	3000	213.0	191.0	35.0
BQ25046DQCT	WSON	DQC	10	250	195.0	200.0	45.0

GENERIC PACKAGE VIEW

DQC 10 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

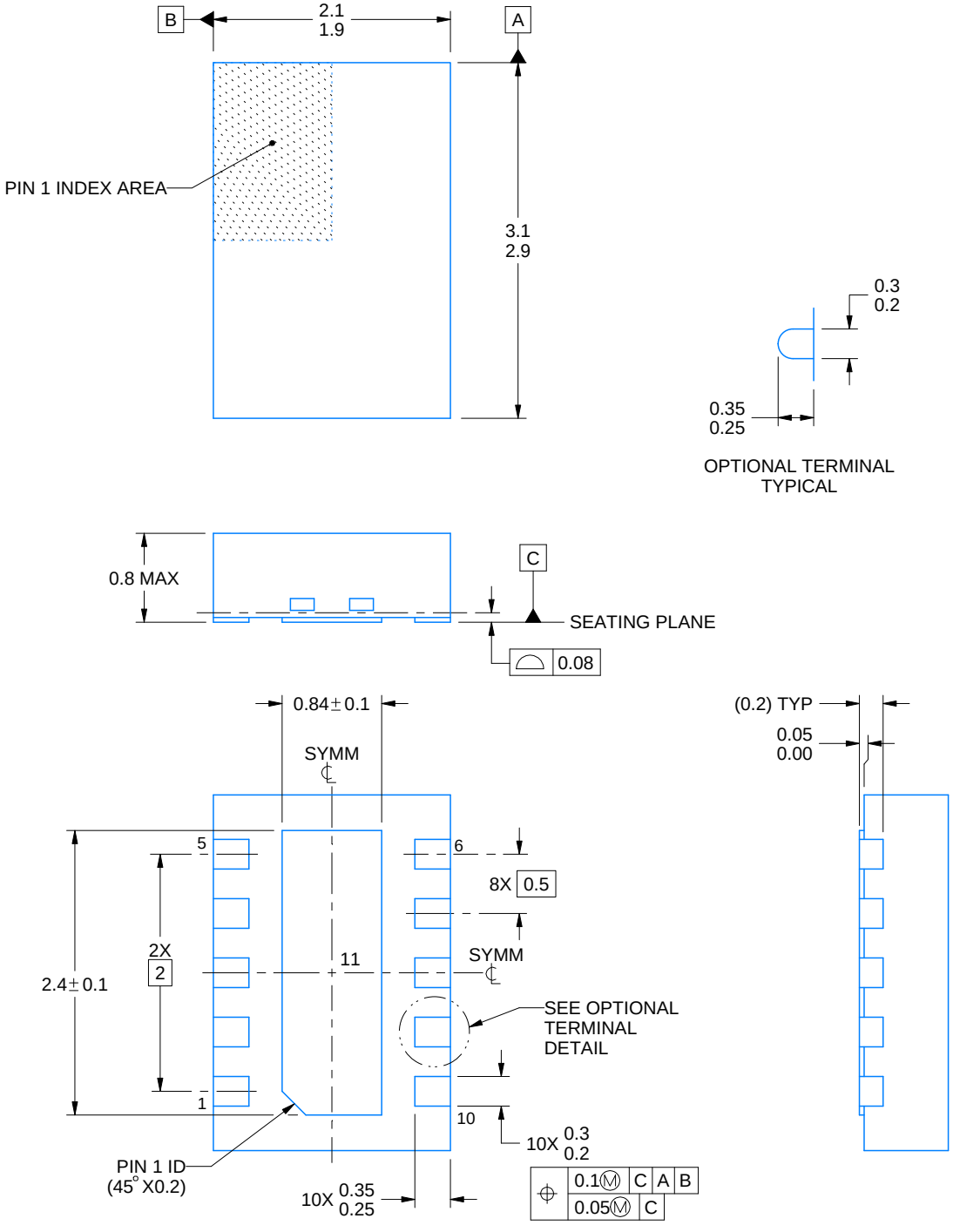
4209674/B

PACKAGE OUTLINE

DQC0010A

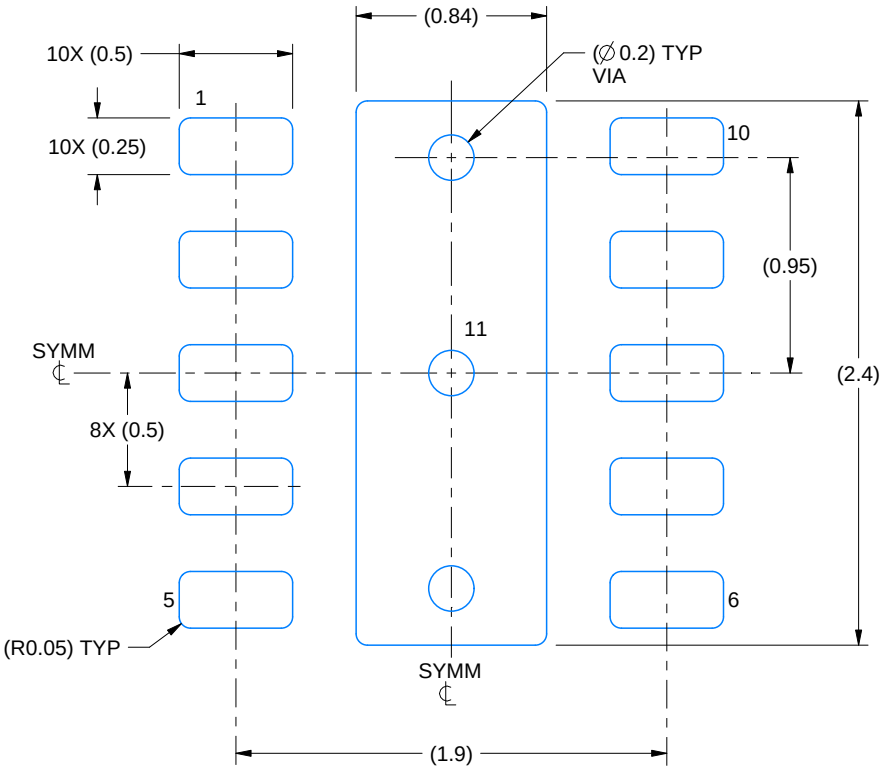
WSON - 0.8mm max height

PLASTIC SMALL OUTLINE - NO LEAD

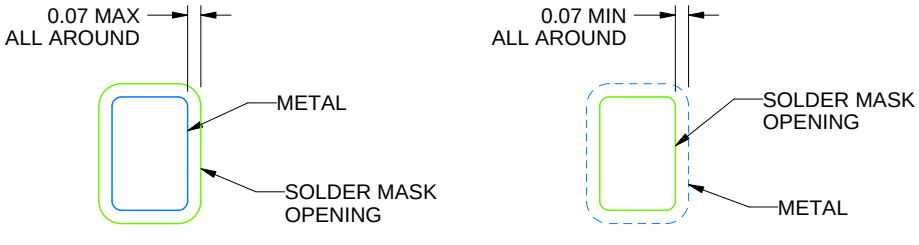


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 30X



SOLDER MASK DETAILS

4218281/B 11/2016

NOTES: (continued)

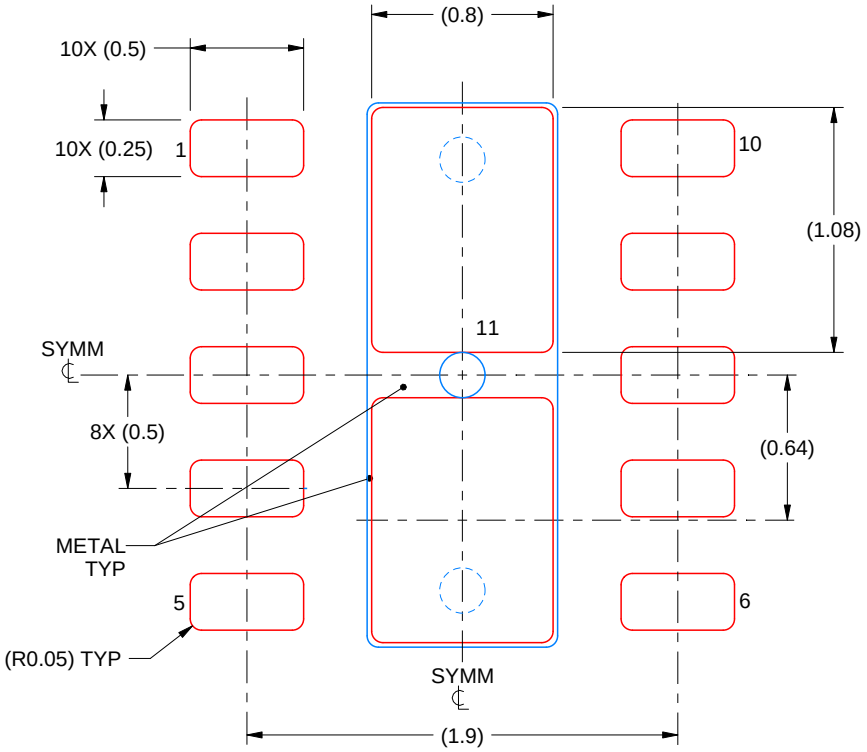
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DQC0010A

WSON - 0.8mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 30X

4218281/B 11/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (https:www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021, Texas Instruments Incorporated