BQ2947 具有外部延迟电容器且适用于 2 节至 4 节串联锂离子电池的过压保护器件

1 特性

- 2、3 和 4 节串联电池过压保护
- 外部电容器编程的延迟计时器
- 出厂编程的 OVP 阈值（阈值范围为 3.85V 至 4.6V）
- 输出选项：高电平有效或开漏低电平有效
- 高精度过压保护：±10mV
- 低功耗 $I_{CC} \approx 1\mu A$ ($V_{CELL(ALL)} < V_{PROTECT}$)
- 每节电池输入具有小于 100nA 的低泄漏电流
- 小型封装尺寸
  - 8 引脚 WSON (2.00mm x 2.00mm)

2 应用

- 笔记本电脑
- UPS 备用电池

3 说明

BQ2947 系列是用于锂离子电池组系统的过压监视器和保护器。独立监控每节电池是否具有过压状态。

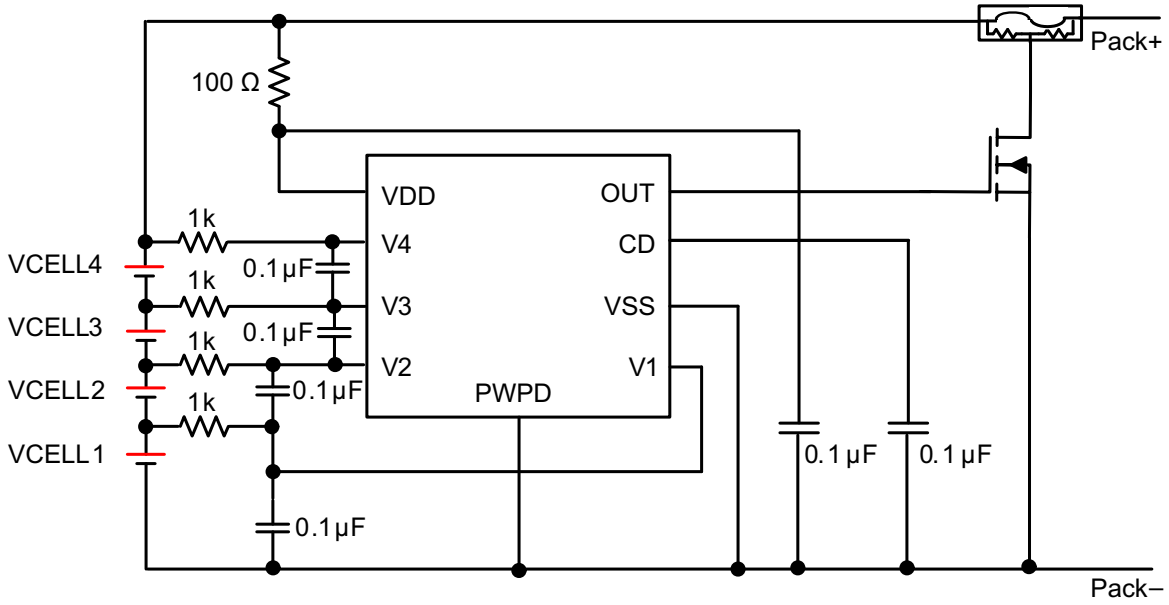
在 BQ2947 器件中，当检测到任意电池上存在过压状态时，即会启动外部延迟计时器。在延迟计时器超时时，输出被触发进入其工作状态（根据配置的不同为高电平或低电平）。外部延迟计时器的特性还包括检测 CD 引脚上开路或者短路延迟电容器（这也将在过压条件下以类似方式触发输出驱动器）的功能。

为了实现更快速的产品线测试，BQ2947 器件提供具有较短延迟时间的客户测试模式。

器件信息

器件型号(1)	封装	封装尺寸（标称值）
BQ294700	WSON (8)	2.00mm × 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



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简化版原理图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。
English Data Sheet: SLUSB15

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4 Revision History

Changes from Revision I (June 2018) to Revision J (May 2021)	Page
• Updated the BQ294712 and BQ294713 devices in the *Device Options table*	3

Changes from Revision H (February 2018) to Revision I (June 2018)	Page
• Added BQ294713 to the *Device Options table*	3
• Added BQ294713 to the *Electrical Characteristics*	6

Changes from Revision G (November 2017) to Revision H (February 2018)	Page
• Changed BQ294712 to Production Data in the *Device Options table*	3

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5 Device Comparison Table

PART NUMBER	OVP (V)	OV HYSTERESIS	OUTPUT DRIVE
BQ294700	4.350	0.300	CMOS Active High
BQ294701	4.250	0.300	CMOS Active High
BQ294702	4.300	0.300	CMOS Active High
BQ294703	4.325	0.300	CMOS Active High
BQ294704	4.400	0.300	CMOS Active High
BQ294705	4.450	0.300	CMOS Active High
BQ294706	4.550	0.300	CMOS Active High
BQ294707	4.225	0.050	NCH Open Drain Active Low
BQ294708	4.500	0.300	CMOS Active High
BQ294711	4.220	0.300	CMOS Active High
BQ294712	4.125	0.300	CMOS Active High
BQ294713	4.600	0.300	CMOS Active High
BQ2947	3.850 – 4.60	0 – 0.300	CMOS Active High or Open Drain Active Low

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6 Pin Configuration and Functions

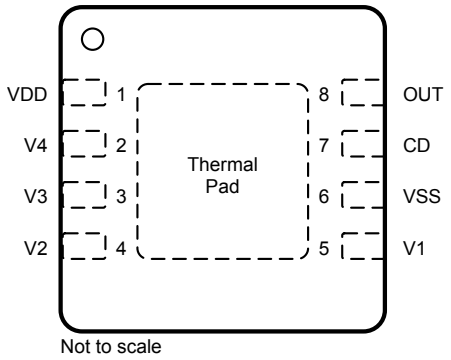

图 6-1. DSG Package 8-Pin WSON Top View

表 6-1. Pin Functions

NUMBER	NAME	TYPE(1)	DESCRIPTION
1	VDD	P	Power supply input
2	V4	IA	Sense input for positive voltage of the fourth cell from the bottom of the stack
3	V3	IA	Sense input for positive voltage of the third cell from the bottom of the stack
4	V2	IA	Sense input for positive voltage of the second cell from the bottom of the stack
5	V1	IA	Sense input for positive voltage of the lowest cell in the stack
6	VSS	P	Electrically connected to IC ground and negative terminal of the lowest cell in the stack
7	CD	OA	External capacitor connection for delay timer
8	OUT	OA	Analog Output drive for overvoltage fault signal. Active High or Open Drain Active Low
PowerPAD™		P	TI recommends connecting the exposed pad to VSS on the PCB.

(1) IA = Input Analog, OA = Output Analog, P = Power Connection

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage	VDD – VSS	– 0.3	30	V
Input voltage	V4 – V3, V3 – V2, V2 – V1, V1 – VSS, or CD – VSS	– 0.3	30	V
Output voltage	OUT – VSS	– 0.3	30	V
Continuous total power dissipation, P_{TOT}		See 节 7.4		
Lead temperature (soldering, 10 s), T_{SOLDER}			300	°C
Storage temperature, T_{stg}		– 65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over-operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V_{DD}		3	20	V
Input voltage range	V4 – V3, V3 – V2, V2 – V1, V1 – VSS, or CD – VSS	0	5	V
Operating ambient temperature range, T_A		– 40	110	°C

7.4 Thermal Information

THERMAL METRIC[1]		BQ2947 WSON 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	62	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	72	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	10	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Typical values stated where T_A = 25°C and VDD = 14.4V, MIN/MAX values stated where T_A = –40°C to +110°C and V_{DD} = 3 V to 20 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE PROTECTION THRESHOLDS						
V_{OV}	$V_{(PROTECT)}$ Overvoltage Detection	BQ294700, R_{IN} = 1 kΩ		4.350		V
		BQ294701, R_{IN} = 1 kΩ		4.250		V
		BQ294702, R_{IN} = 1 kΩ		4.300		V
		BQ294703, R_{IN} = 1 kΩ		4.325		V
		BQ294704, R_{IN} = 1 kΩ		4.400		V
		BQ294705, R_{IN} = 1 kΩ		4.450		V
		BQ294706, R_{IN} = 1 kΩ		4.550		V
		BQ294707, R_{IN} = 1 kΩ		4.225		V
		BQ294708, R_{IN} = 1 kΩ		4.500		V
		BQ294711, R_{IN} = 1 kΩ		4.220		V
		BQ294712, R_{IN} = 1 kΩ		4.125		V
		BQ294713, R_{IN} = 1 kΩ		4.600		V
V_{HYS}	OV Detection Hysteresis	BQ2947[(1)]	250	300	400	mV
V_{OA}	OV Detection Accuracy	T_A = 25°C	–10		10	mV
$V_{OADRIFT}$	OV Detection Accuracy Across Temperature	T_A = –40°C	–40		40	mV
		T_A = 0°C	–20		20	mV
		T_A = 60°C	–24		24	mV
		T_A = 110°C	–54		54	mV
SUPPLY AND LEAKAGE CURRENT						
I_{DD}	Supply Current	(V4 – V3) = (V3 – V2) = (V2 – V1) = (V1 – VSS) = 4.0 V at T_A = 25°C (See 图 8-4.)		1	2	μA
I_{IN}	Input Current at Vx Pins	(V4 – V3) = (V3 – V2) = (V2 – V1) = (V1 – VSS) = 4.0 V at T_A = 25°C (See 图 8-4.)	–0.1		0.1	μA
I_{CELL}	Input Current (ALL Vx and VDD Input Pins)	Current Consumption at Power down, (V4 – V3) = (V3 – V2) = (V2 – V1) = (V1 – VSS) = 2.30 V at T_A = 25°C		1.1		μA
OUTPUT DRIVE OUT, CMOS ACTIVE HIGH VERSIONS ONLY						
V_{OUT}	Output Drive Voltage, Active High	(V4 – V3), (V3 – V2), (V2 – V1), or (V1 – VSS) > V_{OV}, VDD = 14.4 V, I_{OH} = 100 μA	6			V
		If three of four cells are short circuited, only one cell remains powered and > V_{OV}, VDD = Vx (cell voltage), I_{OH} = 100 μA		VDD – 0.3		V
		(V4 – V3), (V3 – V2), (V2 – V1), and (V1 – VSS) < V_{OV}, VDD = 14.4 V, I_{OL} = 100 μA measured into OUT pin.		250	400	mV
I_{OUTH}	OUT Source Current (during OV)	(V4 – V3), (V3 – V2), (V2 – V1), or (V1 – VSS) > V_{OV}, VDD = 14.4 V, OUT = 0 V, measured out of OUT pin.			4.5	mA
I_{OUTL}	OUT Sink Current (no OV)	(V4 – V3), (V3 – V2), (V2 – V1), and (V1 – VSS) < V_{OV}, VDD = 14.4 V, OUT = VDD, measured into OUT pin .Pull resistor R_{PU} = 5 kΩ to VDD = 14.4 V	0.5		14	mA
OUTPUT DRIVE OUT, CMOS OPEN DRAIN ACTIVE LOW VERSIONS ONLY						

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7.5 Electrical Characteristics (continued)

Typical values stated where T_A = 25°C and VDD = 14.4V, MIN/MAX values stated where T_A = –40°C to +110°C and V_{DD} = 3 V to 20 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output Drive Voltage, Active High	(V4 – V3), (V3 – V2), (V2 – V1), and (V1 – VSS) < V_{OV}, VDD = 14.4 V, I_{OL} = 100 µA measured into OUT pin.		250	400	mV
I_{OUTL}	OUT Sink Current (no OV)	(V4 – V3), (V3 – V2), (V2 – V1), and (V1 – VSS) < V_{OV}, VDD = 14.4 V, OUT = VDD, measured into OUT pin. Pull resistor R_{PU} = 5 kΩ to VDD = 14.4 V	0.5		14	mA
I_{OUTLK}	OUT pin leakage	(V4 – V3), (V3 – V2), (V2 – V1), and (V1 – VSS) < V_{OV}, VDD = 14.4 V, OUT = VDD, measured into OUT pin.			100	nA
DELAY TIMER						
t_{CD}	OV Delay Time	C_{CD} = 0.1 µF (see External Delay Capacitor, CD)	1	1.5	2	s
t_{CD_GND}	OV Delay Time with CD pin = 0 V	Delay due to C_{CD} capacitor shorted to ground for Customer Test Mode	20		170	ms

(1) Future option, contact TI.

7.6 Typical Characteristics

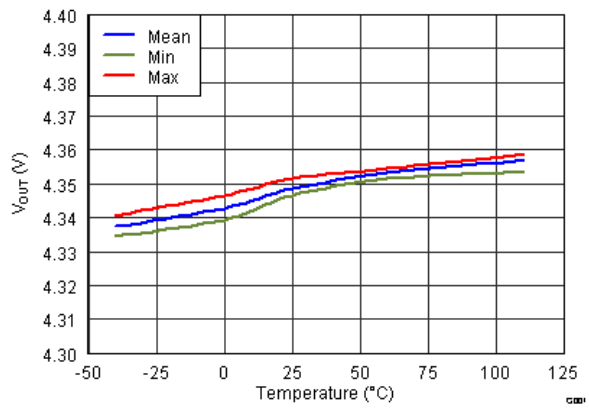

图 7-1. Overvoltage Threshold (Nominal = 4.35 V) vs. Temperature

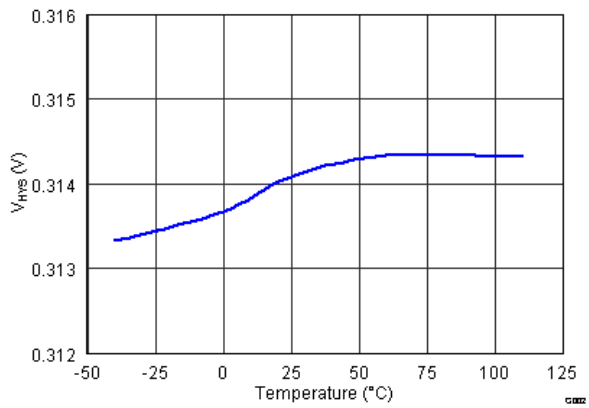

图 7-2. Hysteresis V_{HYS} vs. Temperature

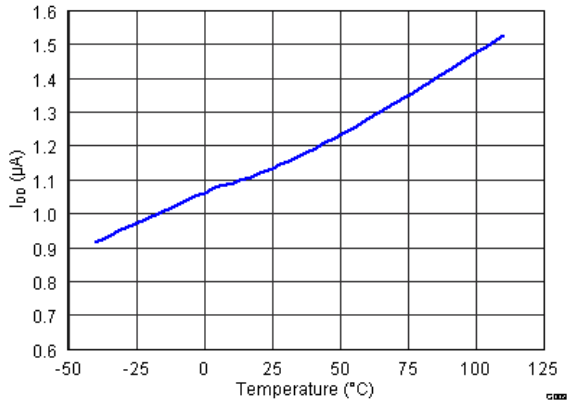

图 7-3. I_{DD} Current Consumption vs. Temperature at VDD = 16 V

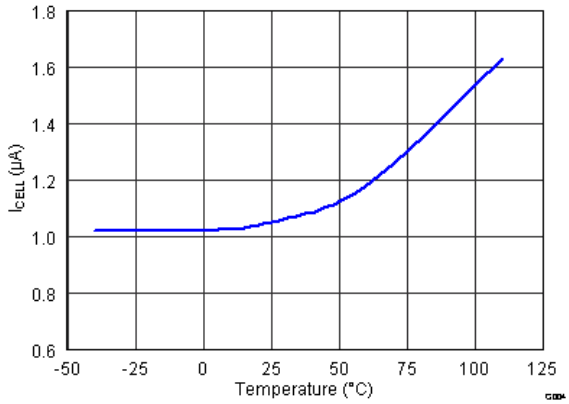

图 7-4. I_{CELL} vs. Temperature at V_{CELL}= 9.2 V

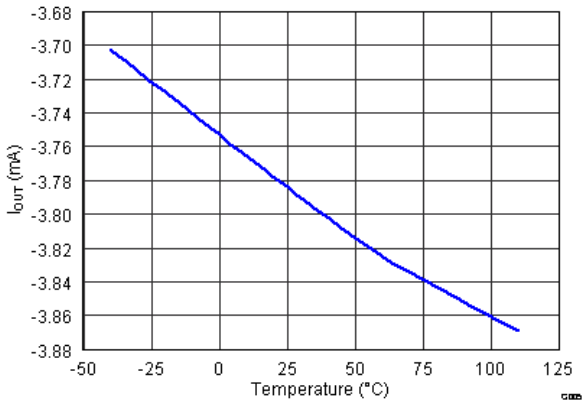

图 7-5. Output Current I_{OUT} vs. Temperature

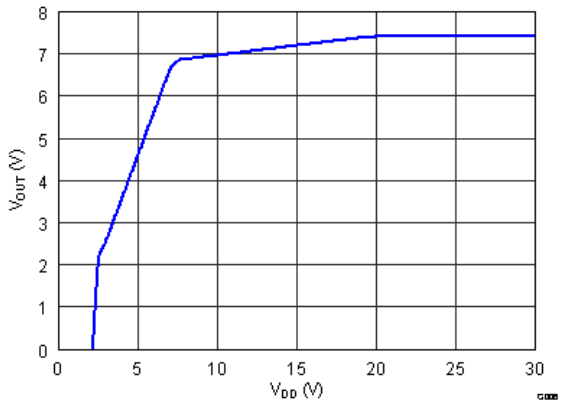

图 7-6. V_{OUT} vs. V_{DD}

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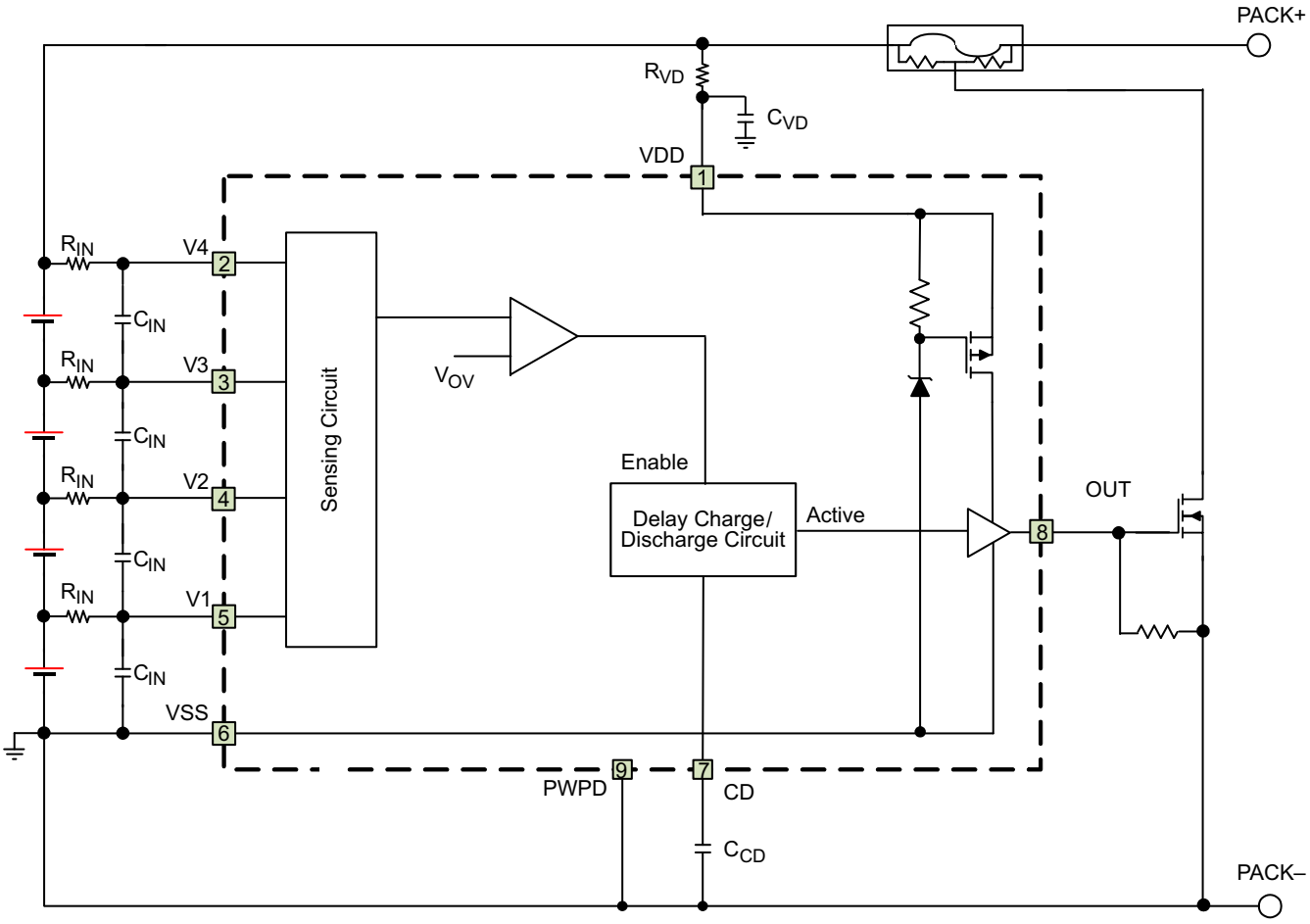
8 Detailed Description

8.1 Overview

The BQ2947 is a second level overvoltage (OV) protector. Each cell is monitored independently by comparing the actual cell voltage to a protection voltage threshold, V_{OV}. The protection threshold is preprogrammed at the factory with a range between 3.85 V and 4.65 V.

8.2 Functional Block Diagram

The Functional Block Diagram shows a CMOS Active High configuration.



Note

In the case of an Open Drain Active Low configuration, an external pull-up resistor is required on the OUT terminal.

8.3 Feature Description

In the BQ2947 family of devices, if any cell voltage exceeds the programmed OV value, a timer circuit is activated. This timer circuit charges the CD pin to a nominal value, then slowly discharges it with a fixed current back down to VSS. When the CD pin falls below a nominal threshold near VSS, the OUT terminal goes from inactive to active state. Additionally, a timeout detection circuit checks to ensure that the CD pin successfully begins charging to above VSS and subsequently drops back down to VSS, and if a timeout error is detected in either direction, it will similarly trigger the OUT pin to become active. See 图 8-2 for details on CD and OUT pin behavior during an overvoltage event.

For an NCH Open Drain Active Low configuration, the OUT pin pulls down to VSS when active (OV present) and is high impedance when inactive (no OV).

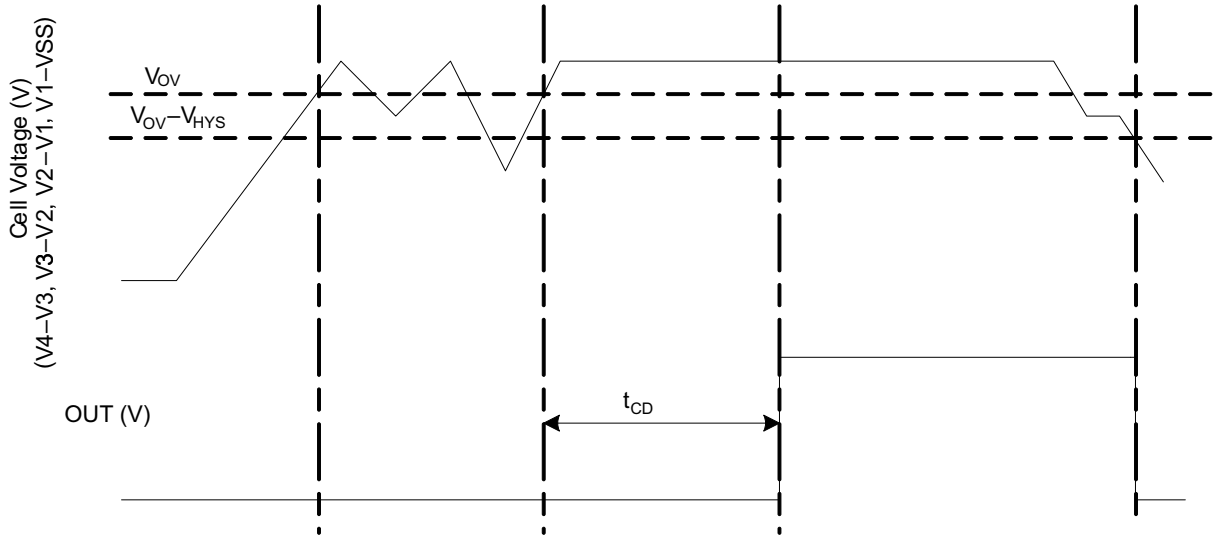


图 8-1. Timing for Overvoltage Sensing (OUT Pin Is Active High)

图 8-2 shows the behavior of CD pin during an OV sequence.

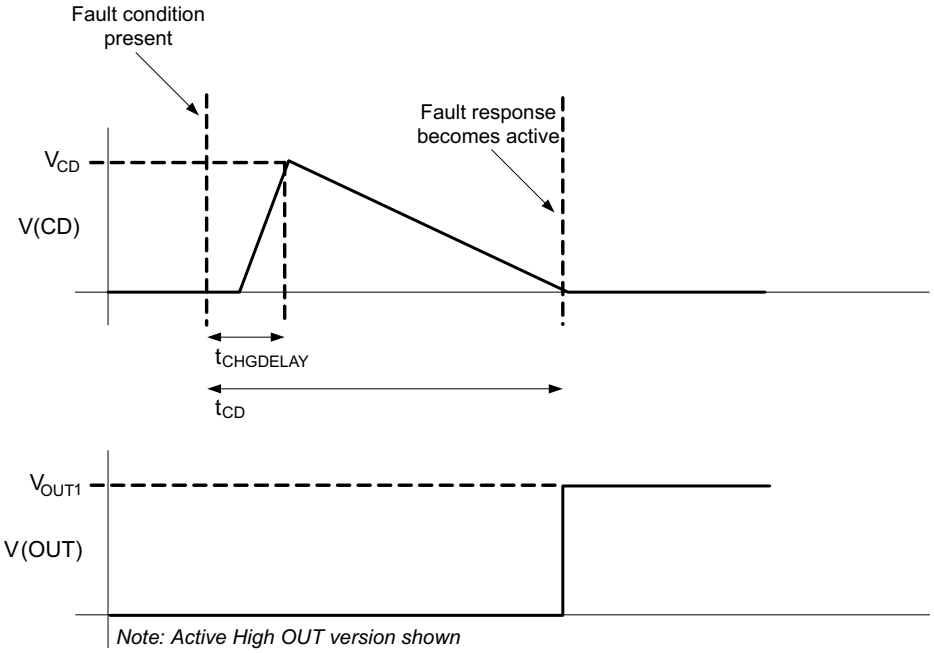


图 8-2. CD Pin Mechanism (OUT Pin Is Active High)

Note

In the case of an Open Drain Active Low version, the V_{OUT} signal will be high and transition to low state when the voltage on the V_{CD} capacitor discharges to the set level based on the t_{CD} timer.

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8.3.1 Pin Details

8.3.1.1 Input Sense Voltage, Vx

These inputs sense each battery cell voltage. A series resistor and a capacitor across the cell for each input is required for noise filtering and stable voltage monitoring.

8.3.1.2 Output Drive, OUT

This terminal serves as the fault signal output, and may be ordered in either Active High or Open Drain Active Low options.

8.3.1.3 Supply Input, VDD

This terminal is the unregulated input power source for the IC. A series resistor is connected to limit the current, and a capacitor is connected to ground for noise filtering.

8.3.1.4 External Delay Capacitor, CD

This terminal is connected to an external capacitor that sets the delay timer during an overvoltage fault event.

The CD pin includes a timeout detection circuit to ensure that the output drives active even with a shorted or open capacitor during an overvoltage event.

The capacitor connected on the CD pin rapidly charges to a voltage if any one of the cell inputs exceeds the OV threshold. Then the delay circuit gradually discharges the capacitor on the CD pin. Once this capacitor discharges below a set voltage, the OUT transitions from an inactive to active state.

To calculate the delay, use the following equation:

$$t_{CD}\ (\text{sec}) = K \times C_{CD}\ (\mu\text{F}),\ \text{where } K = 10 \text{ to } 20 \text{ range.} \quad (1)$$

Example: If C_{CD}= 0.1 µF (typical), then the delay timer range is

t_{CD} (s) = 10 × 0.1 = 1 s (Minimum)

t_{CD} (s) = 20 × 0.1 = 2 s (Maximum)

Note

The tolerance on the capacitor used for C_{CD} increases the range of the t_{CD} timer.

8.4 Device Functional Modes

8.4.1 NORMAL Mode

When all of the cell voltages are below the overvoltage threshold, V_{OV}, the device operates in NORMAL mode. The device monitors the differential cell voltages connected across (V1 – VSS), (V2 – V1), (V3 – V2), and (V4 – V3). The OUT pin is inactive, and is low if configured active high, or, if configured active low, is an open drain being externally pulled up.

8.4.2 OVERVOLTAGE Mode

OVERVOLTAGE mode is detected if any of the cell voltage exceeds the overvoltage threshold, V_{OV} for configured OV delay time. The OUT pin is activated after a delay time set by the capacitance in the CD pin. The OUT pin will either pull high internally, if configured as active high, or will be pulled low internally if configured as active low. An external FET is then turned on, shorting the fuse to ground, which allows the battery and/or charger power to blow the fuse. When all of the cell voltages fall below the (V_{OV} – V_{HYS}), the device returns to NORMAL mode.

8.4.3 Customer Test Mode

It is possible to reduce test time for checking the overvoltage function by simply shorting the external CD capacitor to VSS. In this case, the OV delay would be reduced to the $t_{(CD_GND)}$ value, which has a maximum of 170 ms.

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图 8-3 shows the timing for the Customer Test Mode.

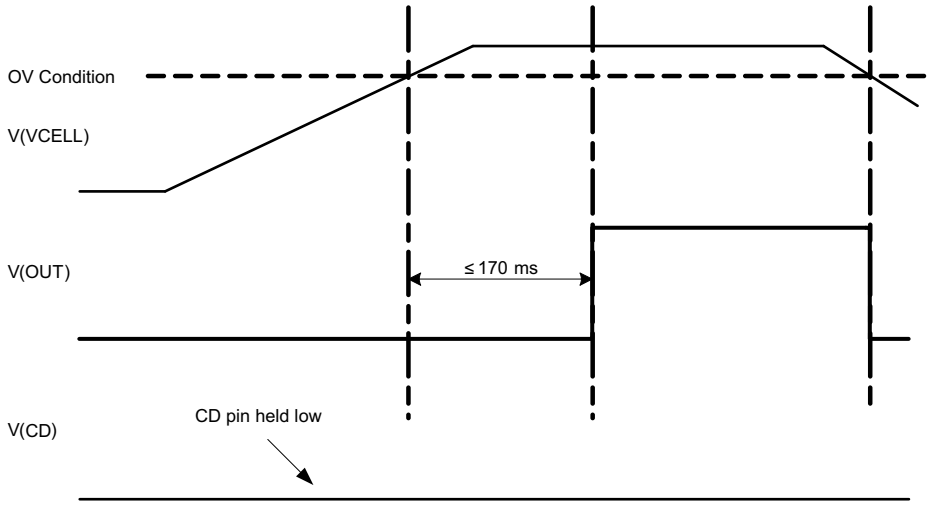
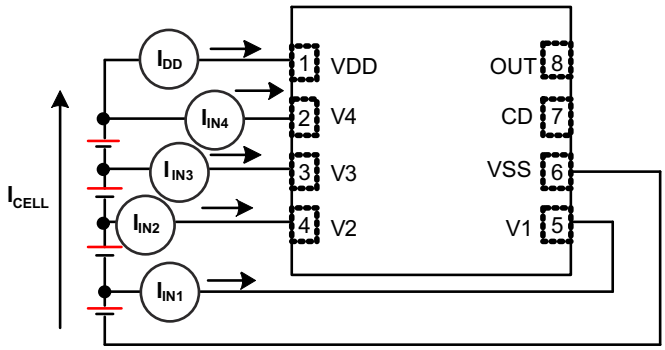


图 8-3. Timing for Customer Test Mode

图 8-4 shows the measurement for current consumption of the product for both VDD and Vx.



$I_{CELL} = I_{DD} + I_{IN1} + I_{IN2} + I_{IN3} + I_{IN4}$

图 8-4. Configuration for IC Current Consumption Test

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The BQ2947 devices are a family of second-level protectors used for overvoltage protection of the battery pack in the application. The device, when configuring the OUT pin with active high, drives a NMOS FET that connects the fuse to ground in the event of a fault condition. This provides a shorted path to use the battery and/or charger power to blow the fuse and cut the power path. The OUT pin, when configured as active low, can be used to drive a PMOS FET to connect the fuse to ground instead.

9.2 Typical Applications

9.2.1 Application Configuration for Active High

图 9-1 shows the recommended reference design components.

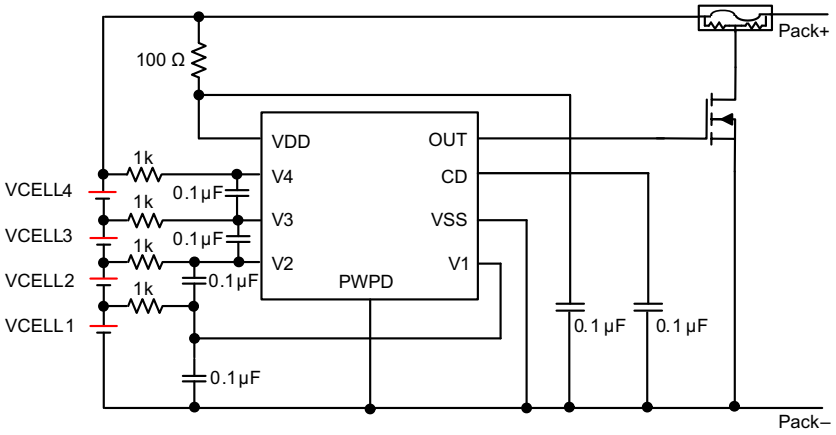

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图 9-1. Application Configuration for Active High

9.2.1.1 Design Requirements

Note

In the case of an Open Drain Active Low configuration, an external pull-up resistor is required on the OUT terminal.

Changes to the ranges stated in 表 9-1 will impact the accuracy of the cell measurements.

表 9-1. Parameters

PARAMETER	EXTERNAL COMPONENT	MIN	NOM	MAX	UNIT
Voltage monitor filter resistance	R_{IN}	900	1000	4700	Ω
Voltage monitor filter capacitance	C_{IN}	0.01	0.1	1.0	µF
Supply voltage filter resistance	R_{VD}	100		1000	Ω
Supply voltage filter capacitance	C_{VD}		0.1	1.0	µF
CD external delay capacitance	C_{CD}		0.1	1.0	µF

Note

The device is calibrated using an R_{IN} value = 1 kΩ. Using a value other than this recommended value changes the accuracy of the cell voltage measurements and V_{OV} trigger level.

9.2.1.2 Detailed Design Procedure

1. Determine the number of cell in series.

   The device supports 2-S to 4-S cell configuration. For 2S and 3S, the top unused pin(s) should be shorted as shown in 图 9-2 and 图 9-3.
2. Determine the overvoltage protection delay.

   Follow the calculation example described in CD pin description. Select the right capacitor to connect to the CD pin.
3. Follow the application schematic to connect the device. If the OUT pin is configured to open drain, an external pull up resistor should be used.

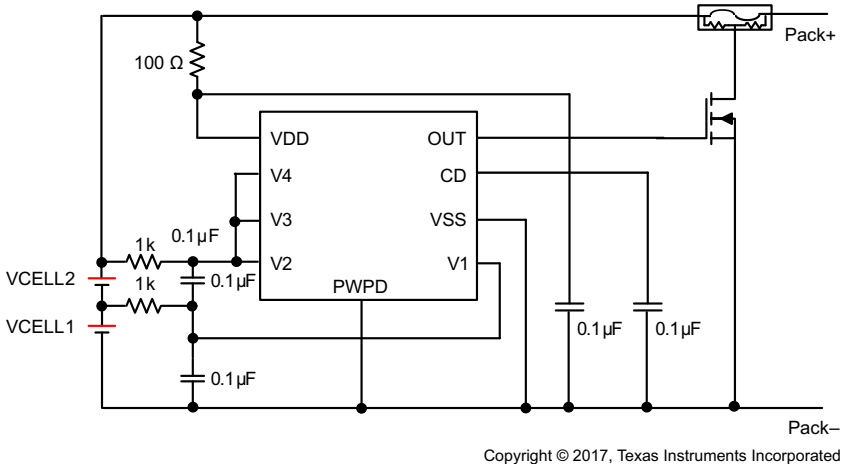

图 9-2. 2-Series Cell Configuration

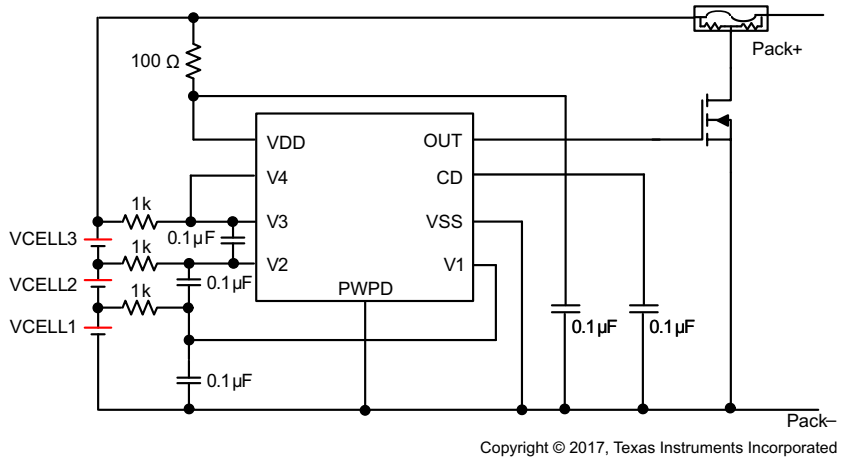

图 9-3. 3-Series Cell Configuration

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9.2.1.3 Application Curves

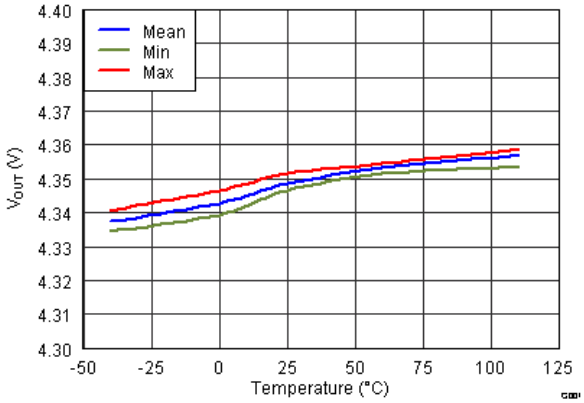

图 9-4. Overvoltage Threshold (OVT) vs. Temperature

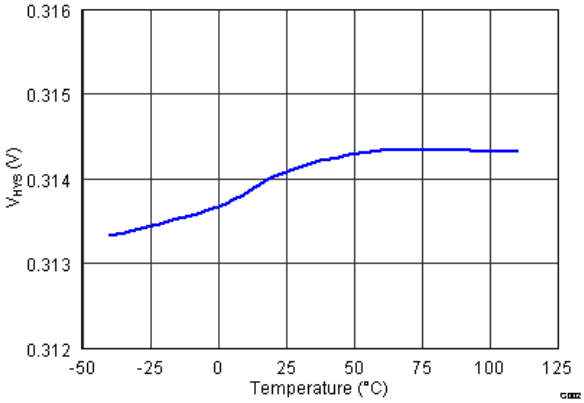

图 9-5. Hysteresis V_{HYS} vs. Temperature

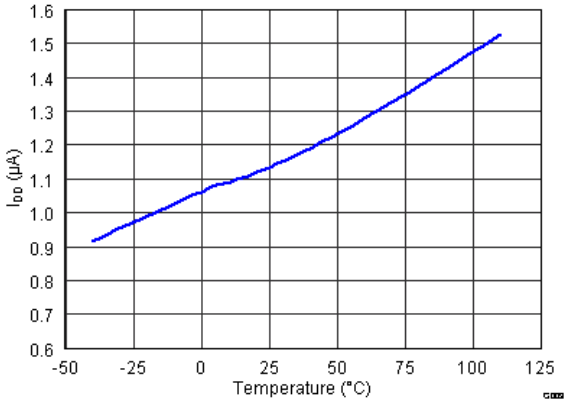

图 9-6. I_{DD} Current Consumption vs. Temperature at VDD = 16 V

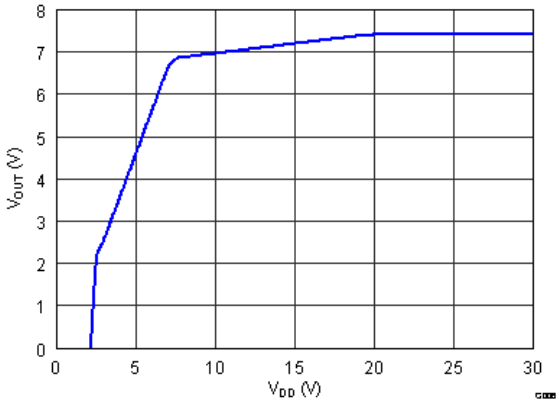

图 9-7. V_{OUT} vs. V_{DD}

10 Power Supply Recommendations

The maximum power of this device is 20 V on V_{DD}.

11 Layout

11.1 Layout Guidelines

1. Ensure the RC filters for the Vx pins and VDD pin are placed as close as possible to the target terminal, reducing the tracing loop area.
2. The capacitor for CD should be placed close to the IC terminals.
3. Ensure the trace connecting the fuse to the gate, source of the NFET to the Pack – is sufficient to withstand the current during fuse blown event.

11.2 Layout Example

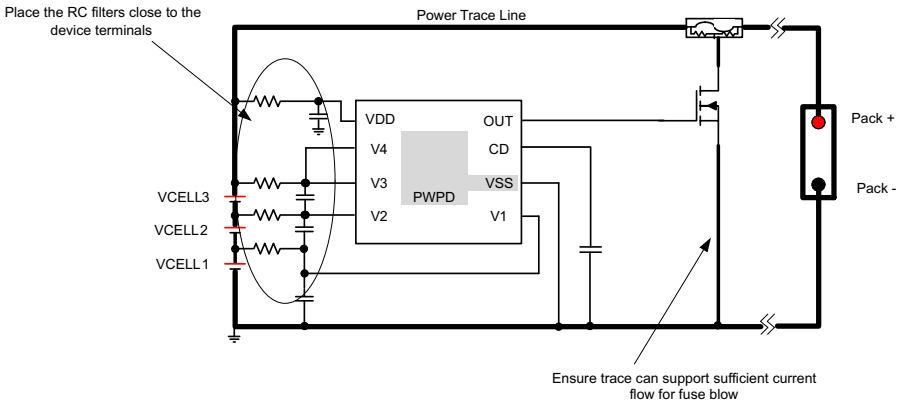

图 11-1. Layout Example

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12 Device and Documentation Support

12.1 第三方产品免责声明

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12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see *BQ2945xy and BQ2947xy Cascade Voltage Monitoring* (SLUA662).

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 支持资源

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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ294700DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	700	Samples
BQ294700DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	700	Samples
BQ294701DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	701	Samples
BQ294701DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	701	Samples
BQ294702DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	702	Samples
BQ294702DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	702	Samples
BQ294703DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	703	Samples
BQ294703DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	703	Samples
BQ294704DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	704	Samples
BQ294704DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	704	Samples
BQ294705DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	705	Samples
BQ294705DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	705	Samples
BQ294706DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	706	Samples
BQ294706DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	706	Samples
BQ294707DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	707	Samples
BQ294707DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	707	Samples
BQ294708DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	Call TI | NIPDAU	Level-2-260C-1 YEAR	-40 to 85	708	Samples
BQ294708DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	Call TI | NIPDAU	Level-2-260C-1 YEAR	-40 to 85	708	Samples
BQ294711DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	711	Samples
BQ294711DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	711	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ294712DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	712	Samples
BQ294712DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	712	Samples
BQ294713DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	713	Samples
BQ294713DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	713	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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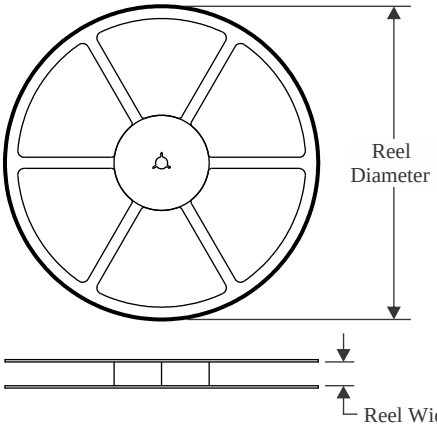
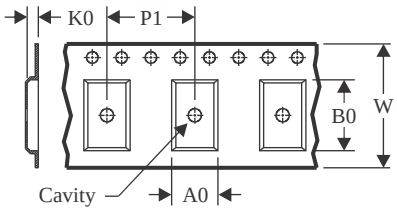
TAPE AND REEL INFORMATION

REEL DIMENSIONS

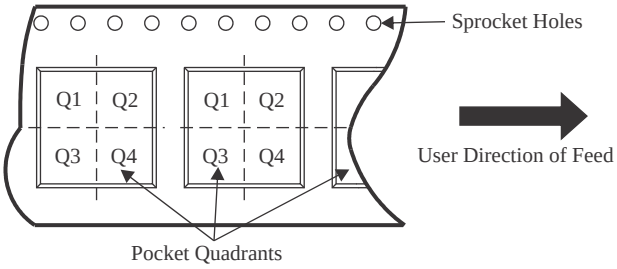


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

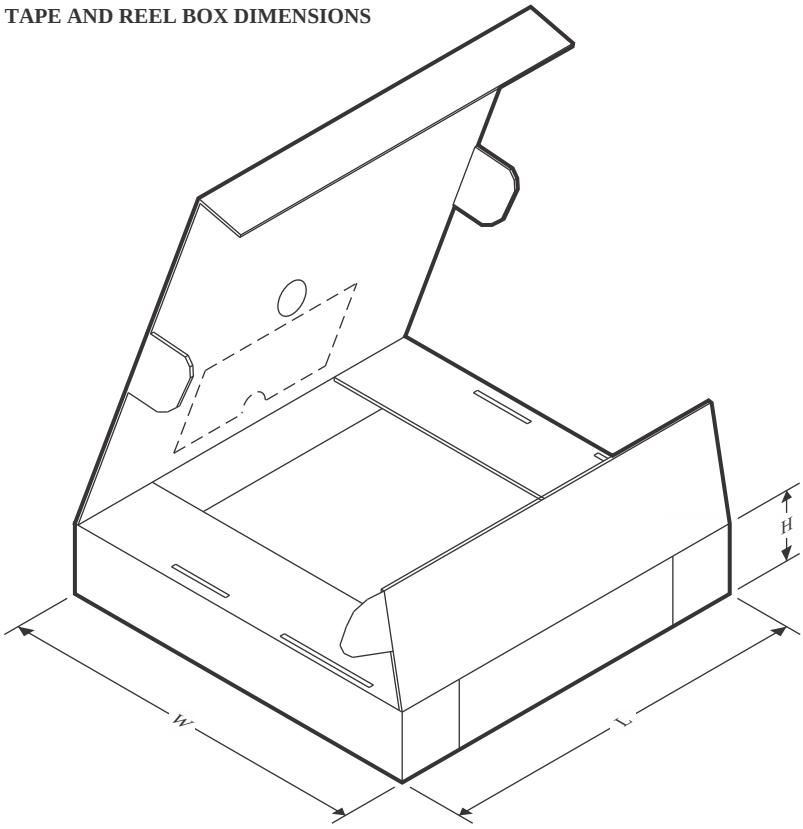


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ294700DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294700DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294700DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294700DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294701DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294701DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294701DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294701DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294702DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294702DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294702DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294702DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294703DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294703DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294704DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294704DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ294704DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294704DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294705DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294705DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294705DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294705DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294706DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294706DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294707DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294707DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294708DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294708DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294711DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294711DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294711DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294711DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294712DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294712DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294712DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294712DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294713DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294713DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294713DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294713DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ294700DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ294700DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ294700DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ294700DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ294701DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ294701DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ294701DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ294701DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ294702DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ294702DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ294702DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ294702DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ294703DSGR	WSON	DSG	8	3000	182.0	182.0	20.0
BQ294703DSGT	WSON	DSG	8	250	182.0	182.0	20.0
BQ294704DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ294704DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ294704DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ294704DSGT	WSON	DSG	8	250	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ294705DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ294705DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ294705DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ294705DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ294706DSGR	WSON	DSG	8	3000	182.0	182.0	20.0
BQ294706DSGT	WSON	DSG	8	250	182.0	182.0	20.0
BQ294707DSGR	WSON	DSG	8	3000	182.0	182.0	20.0
BQ294707DSGT	WSON	DSG	8	250	182.0	182.0	20.0
BQ294708DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ294708DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ294711DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ294711DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ294711DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ294711DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ294712DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ294712DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ294712DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ294712DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ294713DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ294713DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ294713DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ294713DSGT	WSON	DSG	8	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

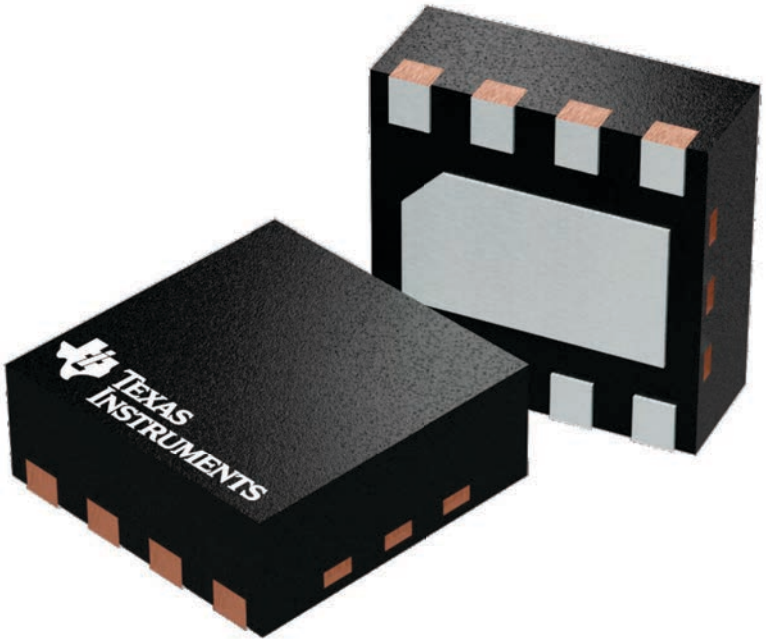
DSG 8

WSON - 0.8 mm max height

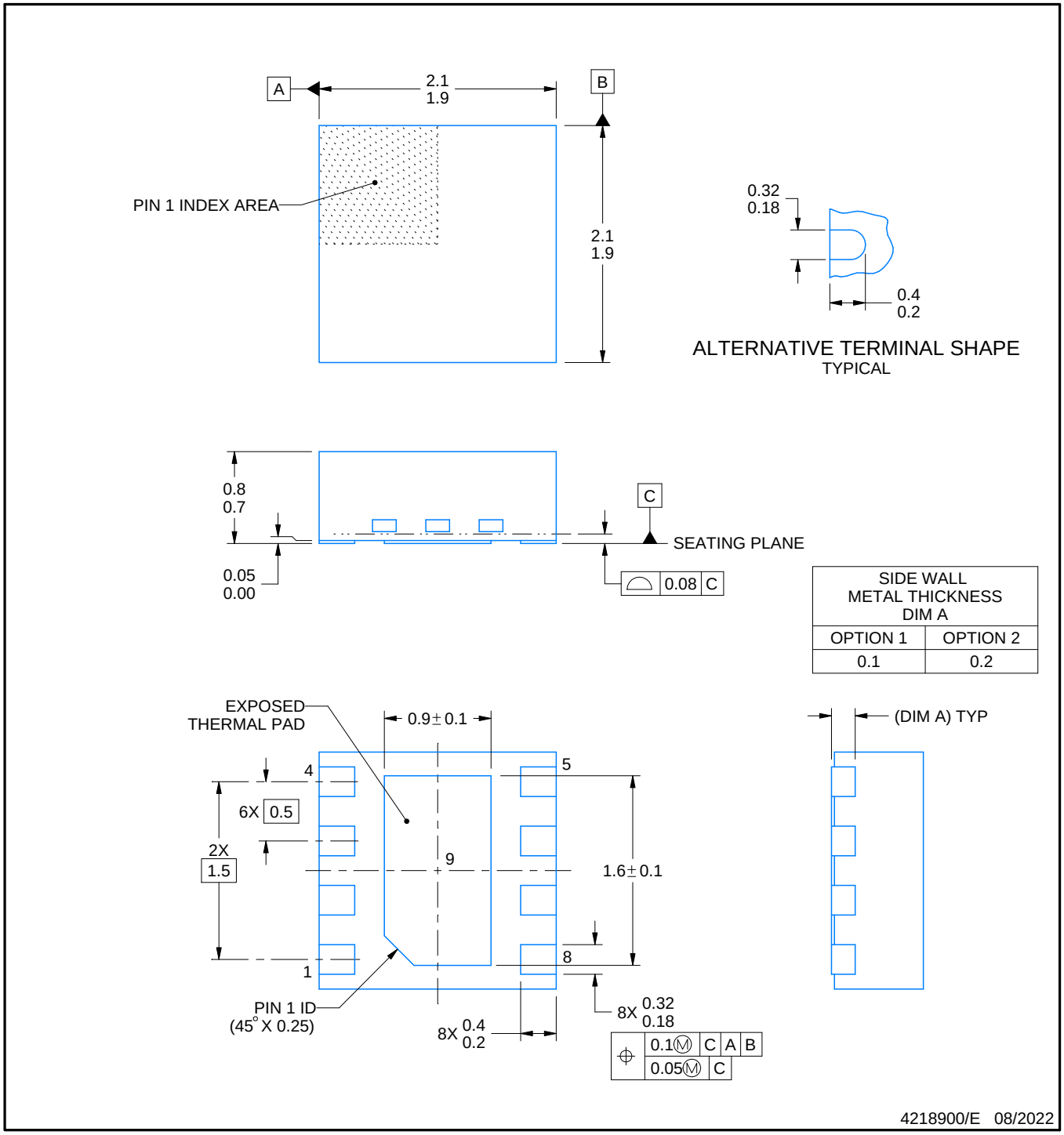
2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

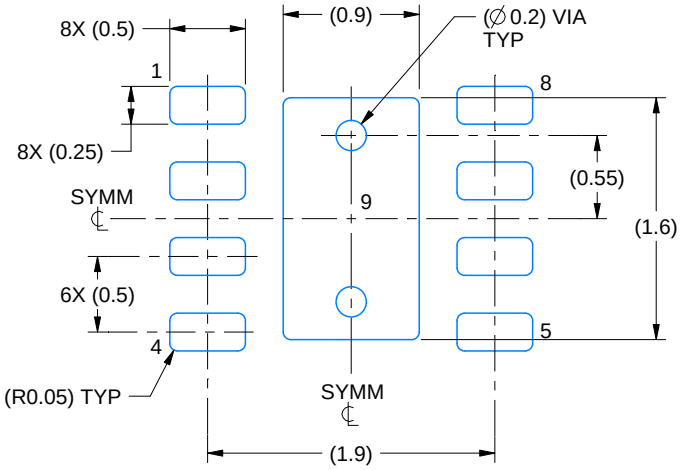


4224783/A

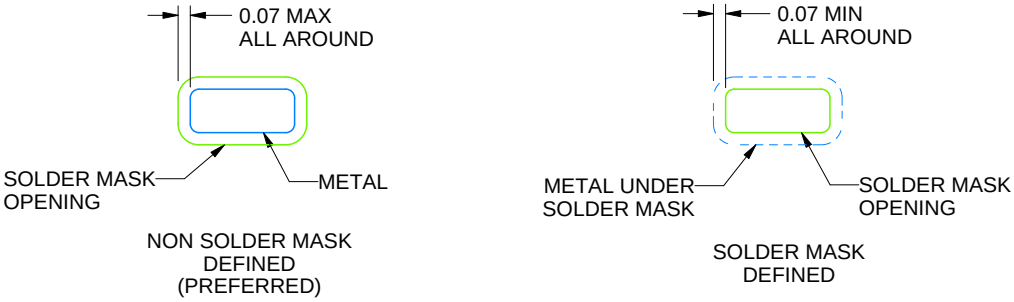


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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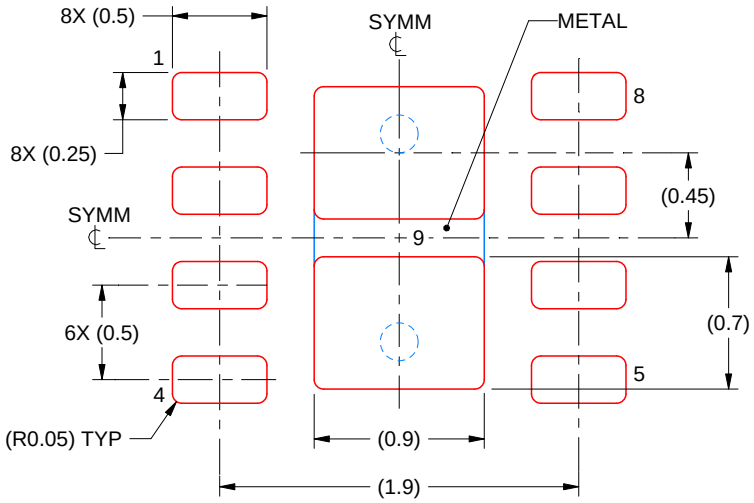
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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