

BQ77216 具有内部延迟计时器、适用于 3 节至 16 节串联锂离子电池的电压和温度保护器

1 特性

- 3 节至 16 节串联电池保护
- 高精度过压保护
 - 25°C 时为 $\pm 10\text{mV}$
 - 0°C 至 60°C 时为 $\pm 20\text{mV}$
- 3.55V 至 5.1V 的过压保护选项
- 1.0V 至 3.5V 的欠压保护选项
- 开路连接检测
- 过热保护
- 支持电池随机连接
- 提供功能安全
- 固定内部延迟计时器
- 固定检测阈值
- 固定输出驱动类型，适用于每个 COUT 和 DOUT
 - 高电平有效或低电平有效
 - 高电平有效驱动达 6V
 - 漏极开路，可从外部上拉至 VDD
- 低功耗 $I_{CC} \approx 1\mu\text{A}$
($V_{\text{CELL(ALL)}} < V_{\text{OV}}$)
- 每节电池输入具有小于 100nA 的低泄漏电流，且禁用开路检测
- 封装尺寸选项：
 - 24 引脚引线式 TSSOP，引线间距为 0.65mm

2 应用

- 锂离子电池组保护，可应用于：
 - 手持园艺工具
 - 手持电动工具
 - 无线真空吸尘器
 - UPS 备用电池
 - 轻型电动车辆（电动自行车、电动踏板车、踏板辅助自行车）

3 说明

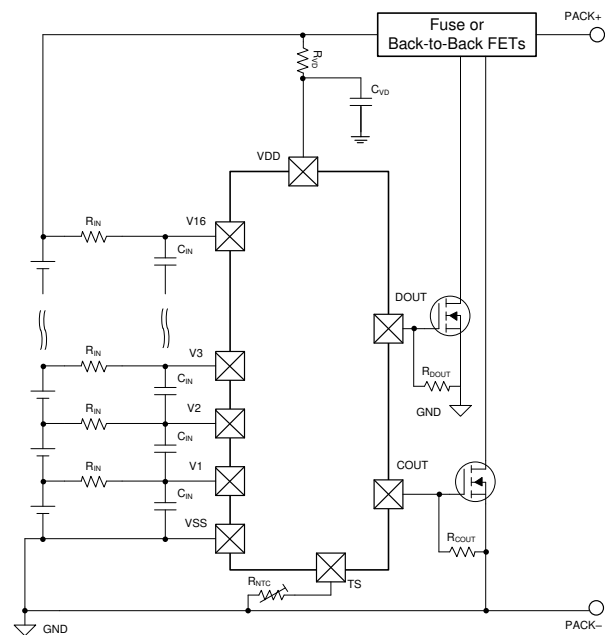
BQ77216 产品系列提供了多种电压和温度监控功能，包括适用于锂离子电池组系统的过压 (OVP)、欠压 (UVP)、开路 (OW)、过热 (OT) 保护。可独立监控每节电池是否具有过压、欠压和开路情况。通过增加外部 NTC 热敏电阻，该器件可以检测到过热情况。

当检测到存在过压、欠压、开路或过热情况时，BQ77216 器件即启动内部延迟计时器。延迟计时器过期时，将触发相应的输出进入其工作状态（根据配置的不同，为高电平或低电平状态）。

器件信息表

器件型号	封装	封装尺寸 (标称值)
BQ7721600 ⁽¹⁾	TSSOP (24)	4.40mm x 7.80mm (6.40mm x 7.80mm, 含引线)

(1) 如需了解可用封装，请参阅数据表末尾的可订购产品附录和 [Device Comparison Table](#)。



简化版原理图



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (April 2022) to Revision F (June 2022)	Page
• Changed the UVP entry for the BQ7721609 device in the Device Comparison Table	3
Changes from Revision D (January 2022) to Revision E (April 2022)	Page
• Moved the BQ7721609 and BQ7721610 devices from PRODUCT PREVIEW to Production Data in the Device Comparison Table	3
Changes from Revision C (September 2021) to Revision D (January 2022)	Page
• Added the BQ7721609 and BQ7721610 devices to the Device Comparison Table	3
Changes from Revision B (July 2021) to Revision C (September 2021)	Page
• Added the BQ7721607 device to the Device Comparison Table	3
• Updated the charged device model (CDM) to the ANSI/ESDA/JEDEC JS-002 standard.....	5

5 说明 (续)

如果检测到过压故障，将触发 COUT 引脚。如果检测到欠压故障，将触发 DOUT 引脚。如果检测到过热或开路故障，则同时触发 DOUT 和 COUT 引脚。为了实现更快速的产品线测试，BQ77216 器件可提供延迟时间大幅减少的客户测试模式 (CTM)。

6 Device Comparison Table

表 6-1. BQ77216 Device Comparison

PART NUMBER	T _A	PACKAGE	PACKAGE DESIGNATOR	OVP (V)	OV HYSTERISIS (V)	OVP DELAY	UVP (V)	UVP DELAY
BQ7721600	-40°C to 110°C	24-Pin TSSOP	PW	4.325	0.100	1 s	2.25	1 s
BQ7721602	-40°C to 110°C	24-Pin TSSOP	PW	4.325	0.100	1 s	2.25	1 s
BQ7721603	-40°C to 110°C	24-Pin TSSOP	PW	4.3	0.100	2 s	2	2 s
BQ7721605	-40°C to 110°C	24-Pin TSSOP	PW	4.225	0.100	1 s	2.6	1 s
BQ7721606	-40°C to 110°C	24-Pin TSSOP	PW	4.275	0.100	1 s	2.5	1 s
BQ7721607	-40°C to 110°C	24-Pin TSSOP	PW	4.25	0.100	4 s	2.5	2 s
BQ7721609	-40°C to 110°C	24-Pin TSSOP	PW	4.35	0.200	4 s	Disabled	
BQ7721610	-40°C to 110°C	24-Pin TSSOP	PW	4.25	0.100	4 s	2.5	2 s

表 6-2. BQ77216 Device Comparison (continued)

PART NUMBER	UV HYSTERISIS (V)	OTC (°C)	UTC (°C)	OW	LATCH	OUTPUT DRIVE	TAPE AND REEL
BQ7721600	0.100	70	NA	Enabled	Disabled	Active Low	BQ7721600PWR
BQ7721602	0.100	70	NA	Enabled	Disabled	Active High, 6-V Drive	BQ7721602PWR
BQ7721603	0.100	75	NA	Enabled	Disabled	Active High, 6-V Drive	BQ7721603PWR
BQ7721605	0.200	75	-10	Disabled	Disabled	Active High, 6-V Drive	BQ7721605PWR
BQ7721606	0.200	75	-10	Disabled	Disabled	Active High, 6-V Drive	BQ7721606PWR
BQ7721607	0.100	83	-30	Enabled	Disabled	Active High, 6-V Drive	BQ7721607PWR
BQ7721609	Disabled	83	NA	Enabled	Disabled	Active High, 6-V Drive	BQ7721609PWR
BQ7721610	0.100	83	NA	Enabled	Disabled	Active High, 6-V Drive (COUT) Active Low (DOUT)	BQ7721610PWR

7 Pin Configuration and Functions

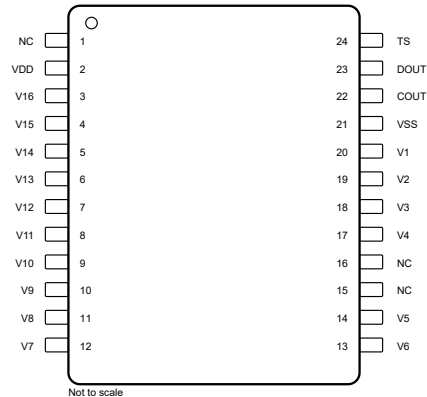


表 7-1. 24-Lead Pin Functions

NO.	NAME	TYPE	DESCRIPTION
1	NC	—	Not electrically connected and can be left floating
2	VDD	P	Power supply
3	V16	I	Sense input for positive voltage of the sixteenth cell from the bottom of the stack
4	V15	I	Sense input for positive voltage of the fifteenth cell from the bottom of the stack
5	V14	I	Sense input for positive voltage of the fourteenth cell from the bottom of the stack
6	V13	I	Sense input for positive voltage of the thirteenth cell from the bottom of the stack
7	V12	I	Sense input for positive voltage of the twelfth cell from the bottom of the stack
8	V11	I	Sense input for positive voltage of the eleventh cell from the bottom of the stack
9	V10	I	Sense input for positive voltage of the tenth cell from the bottom of the stack
10	V9	I	Sense input for positive voltage of the ninth cell from the bottom of the stack
11	V8	I	Sense input for positive voltage of the eighth cell from the bottom of the stack
12	V7	I	Sense input for positive voltage of the seventh cell from the bottom of the stack
13	V6	I	Sense input for positive voltage of the sixth cell from the bottom of the stack
14	V5	I	Sense input for positive voltage of the fifth cell from the bottom of the stack
15	NC	—	Not electrically connected and can be left floating
16	NC	—	Not electrically connected and can be left floating
17	V4	I	Sense input for positive voltage of the fourth cell from the bottom of the stack
18	V3	I	Sense input for positive voltage of the third cell from the bottom of the stack
19	V2	I	Sense input for positive voltage of the second cell from the bottom of the stack
20	V1	I	Sense input for positive voltage of the lowest cell in the stack
21	VSS	P	Electrically connected to IC ground and negative terminal of the lowest cell in the stack
22	COUT	O	Output drive for overvoltage, open wire, and overtemperature. It can be left floating if not used.
23	DOUT	O	Output drive for undervoltage, open wire, and overtemperature. It can be left floating if not used.
24	TS	I	Temperature sensor input. If not used, leave it NC.

I = Input, O = Output, P = Power Connection

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage range	VDD - VSS	- 0.3	85	V

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input voltage range	V _n - VSS where n = 1 to 16	- 0.3	85	V
	TS	- 0.3	1.5	V
Output voltage range	CO _{UT} - VSS, DO _{UT} - VSS	- 0.3	85	V
Functional temperature, T _{FUNC}		- 40	110	°C
Storage temperature, T _{STG}		- 65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

8.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002, all pins	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{DD}	Supply voltage ⁽¹⁾	5		75	V
V _{IN}	Input voltage range of V _n - V _{n-1} where n = 2 to 16 and V ₁ - VSS	0		5	V
	TS	0		1.5	V
V _{CTM}	Customer Test Mode Entry V _{DD} > V ₁₆ + V _{CTM}	12		13	V
C _{TS}	Total capacitance on the TS Pin			200	pF
T _A	Ambient temperature	- 40		85	°C
T _J	Junction temperature	- 65		150	°C

- (1) V_{DD} is equal to top of stack voltage

8.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DEVICE	UNIT
		PW (TSSOP)	
		24 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	97.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	40.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	53.1	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	4.3	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	52.7	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	NA	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

8.5 DC Characteristics

Typical values stated where $T_A = 25^\circ\text{C}$ and $V_{DD} = 58\text{ V}$, MIN/MAX values stated where $T_A = -40^\circ\text{C}$ to 85°C and $V_{DD} = 5\text{ V}$ to 75 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVER VOLTAGE PROTECTION (OV)						
V_{OV}	OV Detection Range		3.55		5.1	V
V_{OV_STEP}	OV Detection Steps			25		mV
V_{OV_HYS}	OV Detection Hysteresis	Selected OV Hysteresis depends on part number. See device selection table for details.		$V_{OV} - 100$		mV
		Selected OV Hysteresis depends on part number. See device selection table for details.		$V_{OV} - 200$		mV
V_{OV_ACC}	OV Detection Accuracy	$T_A = 25^\circ\text{C}$	-10		10	mV
	OV Detection Accuracy	$0^\circ\text{C} \leq T_A \leq 60^\circ\text{C}$	-20		20	mV
	OV Detection Accuracy	$-40^\circ\text{C} \leq T_A \leq 110^\circ\text{C}$	-50		50	mV
UNDER VOLTAGE PROTECTION (UV)						
V_{UV}	UV Detection Range		1.0		3.5	V
V_{UV_STEP}	UV Detection Steps			50		mV
V_{UV_HYS}	UV Detection Hysteresis	Selected UV Hysteresis depends on part number. See device selection table for details.		$V_{UV} + 100$		mV
		Selected UV Hysteresis depends on part number. See device selection table for details.		$V_{UV} + 200$		mV
V_{UV_ACC}	UV Detection Accuracy	$T_A = 25^\circ\text{C}$	-30		30	mV
	UV Detection Accuracy	$-40 \leq T_A \leq 110^\circ\text{C}$	-50		50	mV
V_{UV_MIN}	UV Detection Disabled Threshold	$V_n - V_{n-1}$ where $n = 2$ to 16 and $V_1 - V_{SS}$	450	500	550	mV
OVER TEMPERATURE PROTECTION (OT)						
T_{OT}	OT Detection Range	Available options: 62°C , 65°C , 70°C , 75°C , 80°C , 83°C	62.0		83.0	$^\circ\text{C}$
R_{OT_EXT}	OT Detection External Resistance	62°C		2850		Ω
		65°C		2570		
		70°C		2195		
		75°C		1915		
		80°C		1651		
		83°C		1525		
$T_{OT_ACC}^{(1)}$	OT Detection Accuracy		-5		5	$^\circ\text{C}$
$T_{OT_HYS}^{(2)}$	OT Detection Hysteresis			-10		$^\circ\text{C}$
				4186		Ω
				3530		Ω
R_{NTC}	Internal Pull Up Resistor	After TI Factory Trim	19.5	20	20.6	k Ω
OPEN WIRE PROTECTION (OW)						
V_{OW}	OW Detection Threshold	$V_n < V_{n-1}$ where $n = 2$ to 16		-200		mV
		$V_1 - V_{SS}$		500		mV
V_{OW_HYS}	OW Detection Hysteresis	$V_n < V_{n-1}$ where $n = 1$ to 16		$V_{OW} + 100$		mV

8.5 DC Characteristics (continued)

Typical values stated where $T_A = 25^\circ\text{C}$ and $V_{DD} = 58\text{ V}$, MIN/MAX values stated where $T_A = -40^\circ\text{C}$ to 85°C and $V_{DD} = 5\text{ V}$ to 75 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OW_ACC}	OW Detection Accuracy	$-40^\circ\text{C} \leq T_A \leq 110^\circ\text{C}$	-25		25	mV
SUPPLY AND LEAKAGE CURRENT						
I_{CC}	Supply Current	No fault detected.		2	3.5	μA
$I_{IN}^{(2)}$	Input Current at V_x Pins	$V_n - V_{n-1}$ and $V1 - V_{SS} = 4\text{V}$, where $n = 2$ to 16 , Open Wire Enabled	-0.3		0.3	μA
		$V_n - V_{n-1}$ and $V1 - V_{SS} = 4\text{V}$, where $n = 2$ to 16 , Open Wire Disabled	-0.1		0.1	μA
OUTPUT DRIVE, COUT and DOUT, CMOS ACTIVE HIGH VERSIONS ONLY						
V_{OUT_AH}	Output Drive Voltage for COUT and DOUT, Active High 6V	$V_n - V_{n-1}$ or $V1 - V_{SS} > V_{OV}$, where $n = 2$ to 16 , $V_{DD} = 58\text{ V}$, $I_{OH} = 100\ \mu\text{A}$ measured out of COUT, DOUT pin.	6			V
	Output Drive Voltage for COUT and DOUT, Active High VDD	$V_{DD} - V_{COUT}$ or V_{DOUT} , $V_n - V_{n-1}$ or $V1 - V_{SS} > V_{OV}$, where $n = 2$ to 16 , $I_{OH} = 10\ \mu\text{A}$ measured out of COUT, DOUT pin.	0	1	1.5	V
	Output Drive Voltage for COUT and DOUT, Active High 6V	$V_{DD} - V_{COUT}$ or V_{DOUT} . If 15 of 16 cells are short circuited and only one cell remains powered and $> V_{OV}$, $V_{DD} = V_x$ (cell voltage), $I_{OH} = 100\ \mu\text{A}$.	0	1	1.5	V
	Output Drive Voltage for COUT and DOUT, Active High 6V and VDD	$V_n - V_{n-1}$ and $V1 - V_{SS} < V_{OV}$, where $n = 2$ to 16 , $V_{DD} = 58\text{ V}$, $I_{OH} = 100\ \mu\text{A}$ measured into pin		250	400	mV
R_{OUT_AH}	Internal Pull Up Resistor		80	100	120	$\text{k}\Omega$
$I_{OUT_AH_H}$	OUT Source Current (during OV)	$V_n - V_{n-1}$ or $V1 - V_{SS} > V_{OV}$, where $n = 2$ to 16 , $V_{DD} = 58\text{ V}$, $OUT = 0\text{V}$. Measured out of COUT, DOUT pin			4.5	mA
$I_{OUT_AH_L}$	OUT Sink Current (no OV)	$V_n - V_{n-1}$ and $V1 - V_{SS} < V_{OV}$, where $n = 2$ to 16 , $V_{DD} = 58\text{ V}$, $OUT = V_{DD}$. Measured into COUT, DOUT pin	0.3		3	mA
OUTPUT DRIVE, COUT and DOUT, NCH OPEN DRAIN ACTIVE LOW VERSIONS ONLY						
V_{OUT_AL}	Output Drive Voltage for COUT and DOUT, Active Low	$V_n - V_{n-1}$ or $V1 - V_{SS} > V_{OV}$, where $n = 2$ to 16 , $V_{DD} = 58\text{ V}$, $I_{OH} = 100\ \mu\text{A}$ measured into COUT, DOUT pin.		250	400	mV
$I_{OUT_AL_L}$	OUT Source Current (during OV)	$V_n - V_{n-1}$ or $V1 - V_{SS} > V_{OV}$, where $n = 2$ to 16 , $V_{DD} = 58\text{ V}$, $OUT = V_{DD}$. Measured into COUT, DOUT pin.	0.3		3	mA
$I_{OUT_AL_H}$	OUT Sink Current (no OV)	$V_n - V_{n-1}$ and $V1 - V_{SS} < V_{OV}$, where $n = 2$ to 16 , $V_{DD} = 58\text{ V}$, $OUT = V_{DD}$. Measured out of COUT, DOUT pin.			100	nA

- (1) Assured by Design. This accuracy assumes the external resistance is within +/- 2% of the R_{OT_EXT} values for the corresponding temperature threshold.
- (2) Assured by Design.

8.6 Timing Requirements

Typical values stated where $T_A = 25^\circ\text{C}$ and $V_{DD} = 58\text{ V}$, MIN/MAX values stated where $T_A = -40^\circ\text{C}$ to 85°C and $V_{DD} = 5\text{ V}$ to 85 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{\text{OV_DELAY}}$	OV Delay Time			0.25		s
				0.5		s
				1		s
				2		s
				4		s
$t_{\text{UV_DELAY}}$	UV Delay Time			0.25		s
				0.5		s
				1		s
				2		s
$t_{\text{OT_DELAY}}$	OT Delay Time			4		s
$t_{\text{OW_DELAY}}$	OW Delay Time			4		s
$t_{\text{DELAY_ACC}}$	Delay Time Accuracy	For 0.25s, 0.5s delays	- 128		128	ms
$t_{\text{DELAY_ACC}}$	Delay Time Accuracy	For 1s delays	- 150		150	ms
$t_{\text{DELAY_DR}}$	Delay time drift across operating temp	For all delays other than 0.25s, 0.5s, 1s delays	- 10%		10%	
$t_{\text{CTM_DELAY}}$	Fault Detection Delay Time during Customer Test Mode	See Customer Test Mode.		50		ms

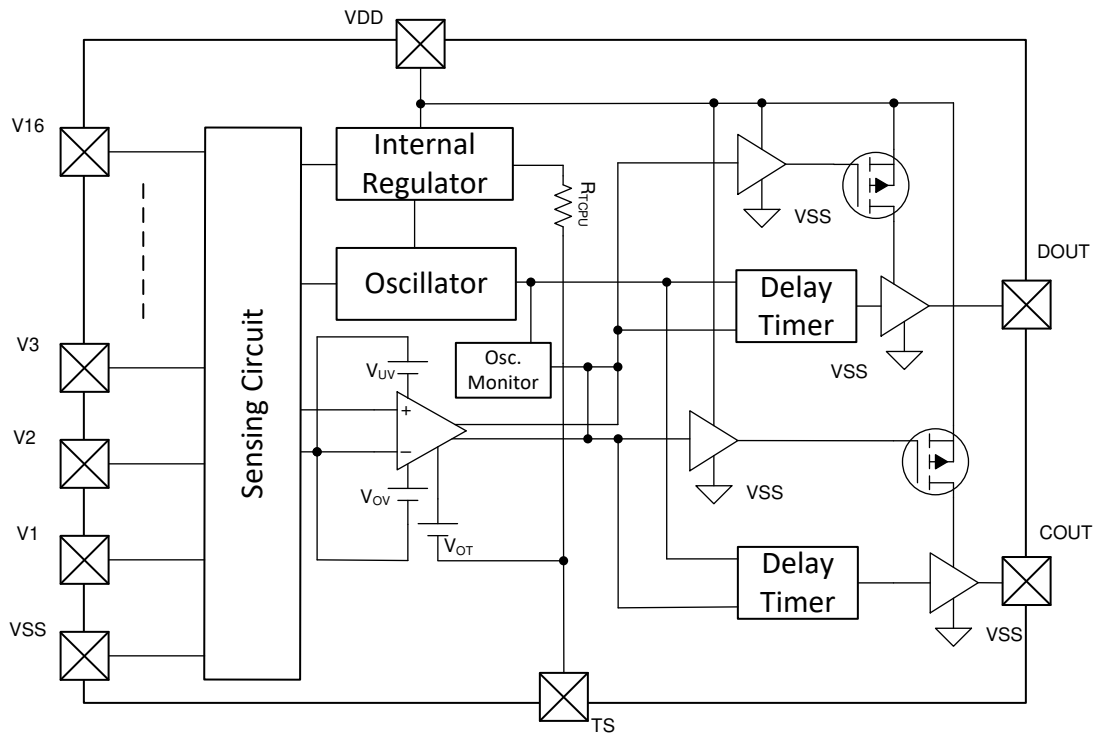
9 Detailed Description

9.1 Overview

The BQ77216 family of devices provides a range of voltage and temperature monitoring including overvoltage (OVP), undervoltage (UVP), open wire (OW), and overtemperature (OT) protection for Li-ion battery pack systems. Each cell is monitored independently for overvoltage, undervoltage, and open-wire conditions. With the addition of an external NTC thermistor, the device can detect overtemperature conditions. An internal delay timer is initiated upon detection of an overvoltage, undervoltage, open-wire, or overtemperature condition. Upon expiration of the delay timer, the respective output is triggered into its active state (either high or low depending on the configuration). The overvoltage triggers the COUT pin if a fault is detected, and undervoltage triggers the DOUT pin if a fault is detected. If an undertemperature, overtemperature, or open-wire fault is detected, then both the DOUT and COUT are triggered.

For quicker production-line testing, the BQ77216 device provides a Customer Test Mode (CTM) with greatly reduced delay time.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Voltage Fault Detection

In the BQ77216 device, each cell is monitored independently. Overvoltage is detected by comparing the actual cell voltage to a protection voltage reference, V_{OV} . If any cell voltage exceeds the programmed OV value, a timer circuit is activated. When the timer expires, the COUT pin goes from inactive to active state. The timer is reset if the cell voltage falls below the recovery threshold ($V_{OV} - V_{OV_HYS}$). Undervoltage is detected by comparing the actual cell voltage to a protection voltage reference, V_{UV} . If any cell voltage falls below the programmed UV value, a timer circuit is activated. When the timer expires, the DOUT pin goes from inactive to active state. The timer is reset if the cell voltage rises below the recovery threshold ($V_{UV} + V_{UV_HYS}$).

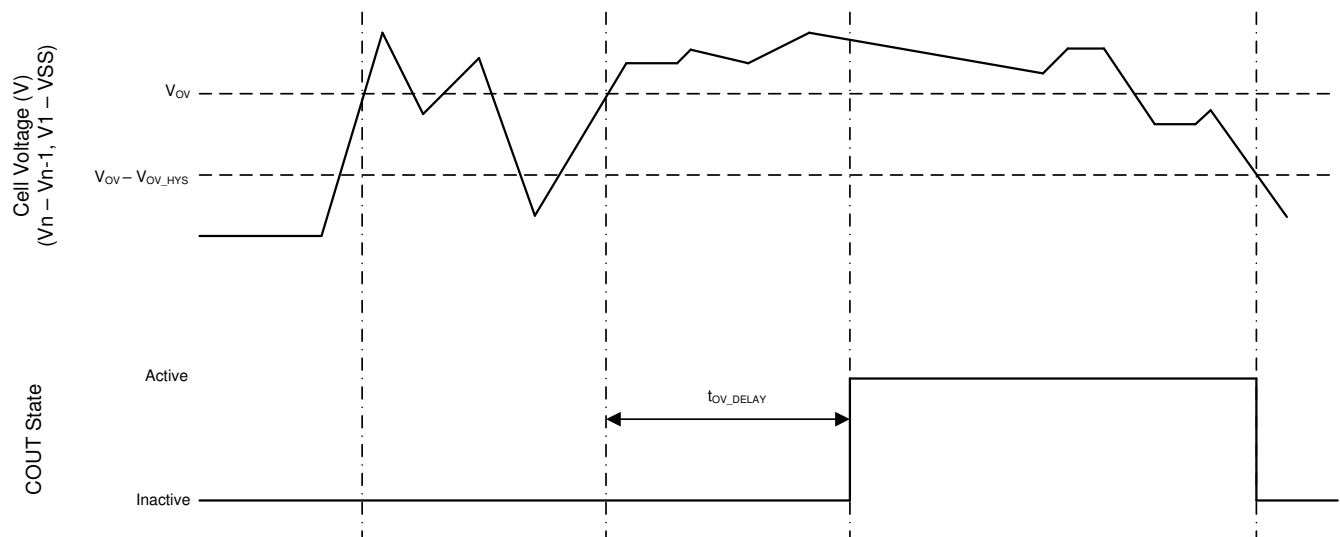


图 9-1. Timing for Overvoltage Sensing

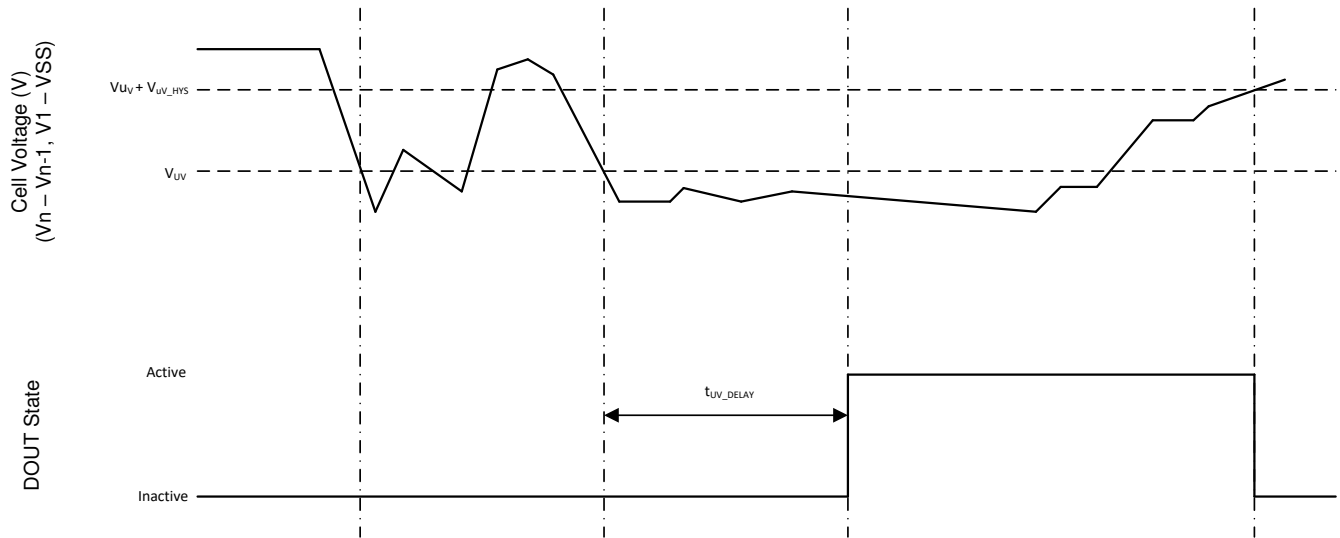


图 9-2. Timing for Undervoltage Sensing

9.3.2 Open Wire Fault Detection

In the BQ77216 device, each cell input is monitored independently to determine if the input is connected to a cell or not by applying a 50- μ A pull down current to ground that is activated for 128 μ s every 128 ms. If the device detects that $V_n < V_{n-1} - V_{OW}$ V, then a timer is activated. When the timer expires, the COUT and DOUT pins go from an inactive to active state. The timer is reset if the cell input rises above below the recovery threshold ($V_{OW} + V_{OW_HYS}$).

9.3.3 Temperature Fault Detection

In the BQ77216 device, the TS pin is ratiometrically monitored with an internal pull up resistance R_{NTC} . Overtemperature is detected by evaluating the TS input voltage to determine the external resistance falls below a protection resistance, R_{OT_EXT} . If the resistance falls below the programmed OT value, a timer circuit is activated. When the timer expires, the COUT and DOUT pins go from inactive to active state. The timer is reset if the resistance rises above the recovery threshold ($R_{OT} + R_{OT_HYS}$). If external capacitance is added to the TS pin, it needs to be within the spec limit shown in recommended operating conditions.

备注

Texas Instruments does not recommend adding an external capacitor to the TS pin. The capacitance on this pin will affect the TS measurement accuracy if greater than C_{TS} .

9.3.4 Oscillator Health Check

The device can detect if the internal oscillator slows down below the f_{OSC_FAULT} threshold. When this occurs then the COUT and DOUT go from inactive to active state. If the oscillator returns to normal then the fault recovers.

9.3.5 Sense Positive Input for Vx

This is an input to sense each single battery cell voltage. A series resistor and a capacitor across the cell for each input is required for noise filtering and stable voltage monitoring.

9.3.6 Output Drive, COUT and DOUT

These pins serve as the fault signal outputs, and may be ordered in either active HIGH with drive to 6V or active LOW options configured through internal OTP.

The COUT and DOUT will respond per the following table when a fault is detected, if the specific fault is enabled.

表 9-1. Fault Detection vs COUT and DOUT Action

FAULT Detected	COUT	DOUT
Overvoltage	Active	Inactive
Undervoltage	Inactive	Active
Open Wire	Active	Active
Over Temperature	Active	Active
Oscillator Health	Active	Active

9.3.7 The LATCH Function

The device can be enabled to latch the fault signal, which effectively disables the recovery functions of all fault detections. The only way to recover from a fault state when the latch is enabled is a POR of the device.

9.3.8 Supply Input, VDD

This pin is the unregulated input power source for the IC. A series resistor is connected to limit the current, and a capacitor is connected to ground for noise filtering.

9.4 Device Functional Modes

9.4.1 NORMAL Mode

When COUT and DOUT are inactive (no fault detected) the device operates in NORMAL mode and device is monitoring for voltage, open wire and temperature faults.

The COUT and DOUT pins are inactive and if configured:

- Active high is low.
- Active low is being externally pulled up and is an open drain.

9.4.2 FAULT Mode

FAULT mode is entered if the COUT or DOUT pins are activated. The OUT pin will either pull high internally, if configured as active high, or will be pulled low internally, if configured as active low. When COUT and DOUT are deactivated the device returns to NORMAL mode.

9.4.3 Customer Test Mode

Customer Test Mode (CTM) helps to reduce test time for checking the delay timer parameter once the circuit is implemented in the battery pack. To enter CTM, VDD should be set to at least V_{CTM} higher than V16 (see [图 9-3](#)). The delay timer is greater than 10 ms, but considerably shorter than the timer delay in normal operation. To exit Customer Test Mode, remove the VDD to a V16 voltage differential of 10 V so that the decrease in this value automatically causes an exit.

CAUTION

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into Customer Test Mode. Also avoid exceeding Absolute Maximum Voltages for the individual cell voltages ($V_{Cn} - V_{Cn-1}$) and ($V1 - VSS$). Stressing the pins beyond the rated limits may cause permanent damage to the device.

[图 9-3](#) shows the timing for the Customer Test Mode.

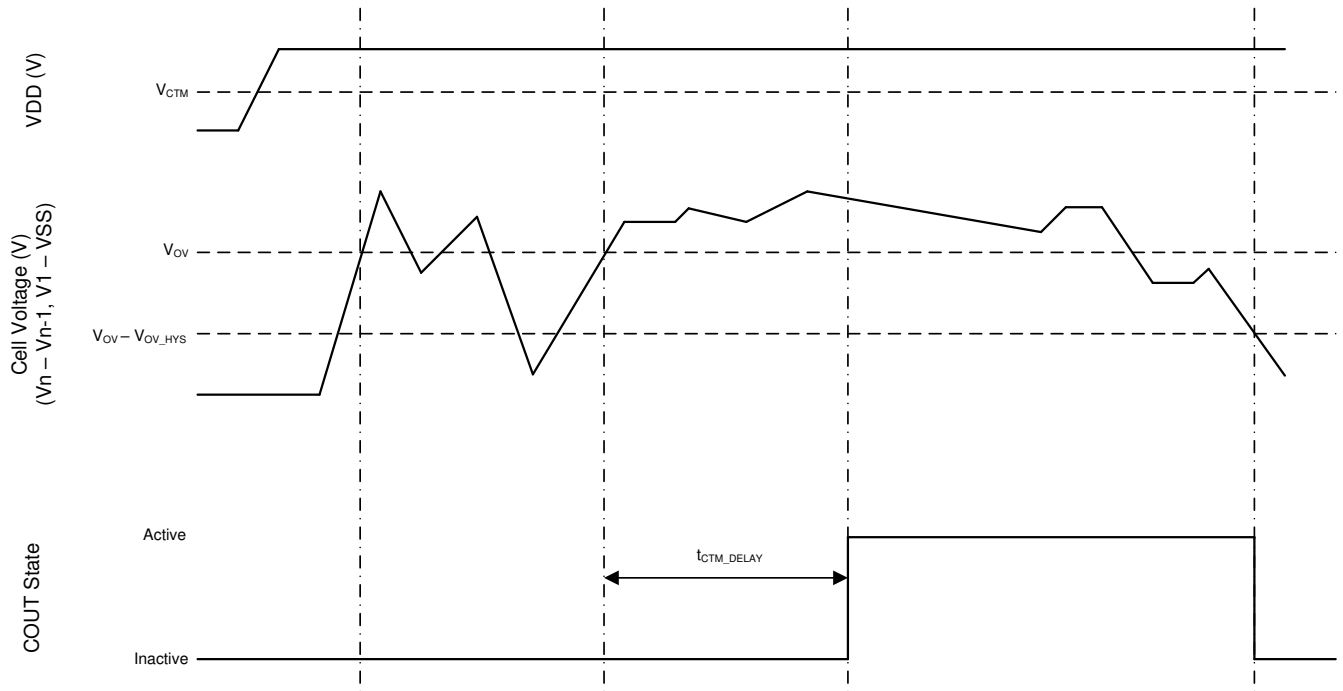


图 9-3. Timing for Customer Test Mode

10 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

Changes to the ranges stated in 表 10-1 will impact the accuracy of the cell measurements.

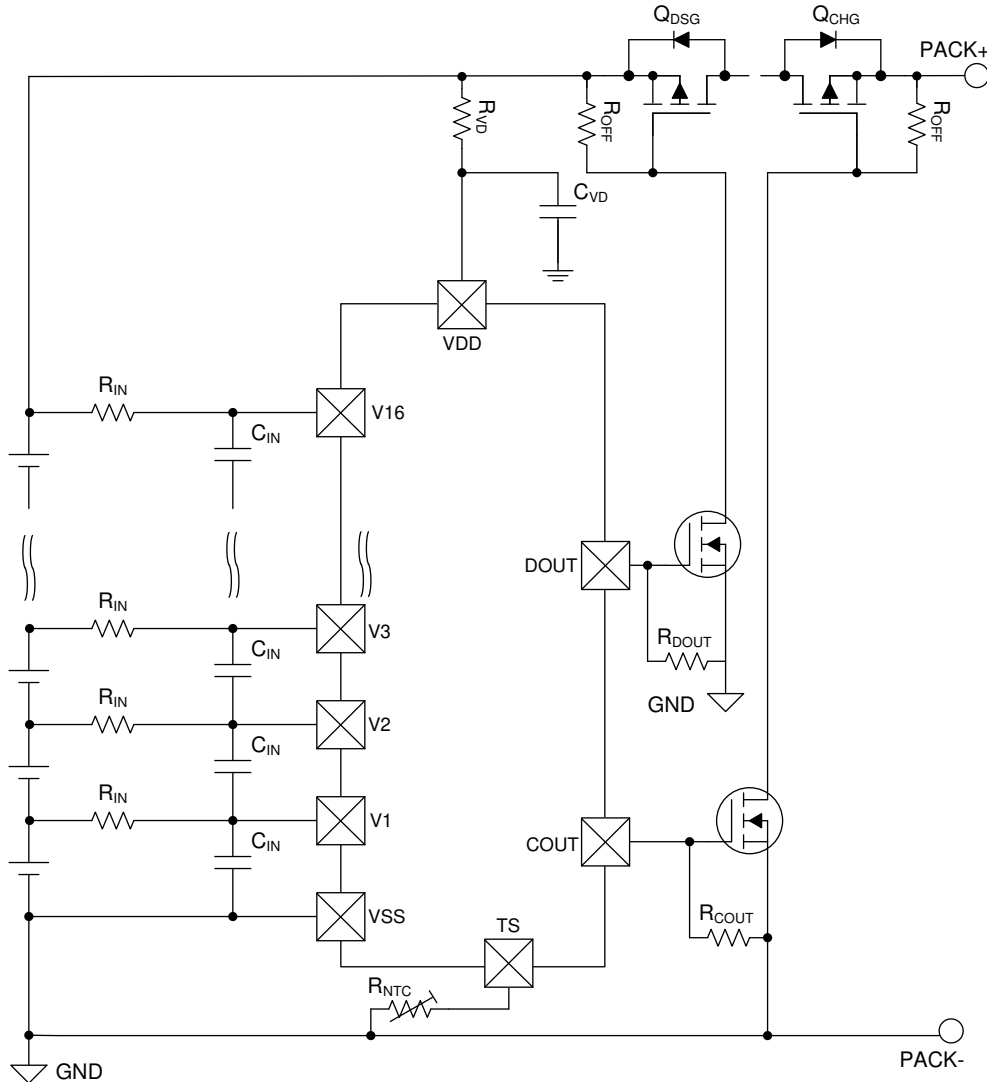


图 10-1. Application Configuration

10.1.1 Design Requirements

Changes to the ranges stated in 表 10-1 will impact the accuracy of the cell measurements. 图 10-1 shows each external component.

表 10-1. Parameters

PARAMETER	EXTERNAL COMPONENT	MIN	NOM	MAX	UNIT
Voltage monitor filter resistance	R_{IN}	900	1000	1100	Ω
Voltage monitor filter capacitance	C_{IN}	0.01		0.1	μF
Supply voltage filter resistance	R_{VD}	100	300	1K	Ω
Supply voltage filter capacitance	C_{VD}	0.05	0.1	1	μF

备注

The device is calibrated using an R_{IN} value = 1 k Ω . Using a value other than this recommended value changes the accuracy of the cell voltage measurements and V_{OV} trigger level.

10.1.2 Detailed Design Procedure

图 10-2 shows the measurement for current consumption for the product for both VDD and V_x .

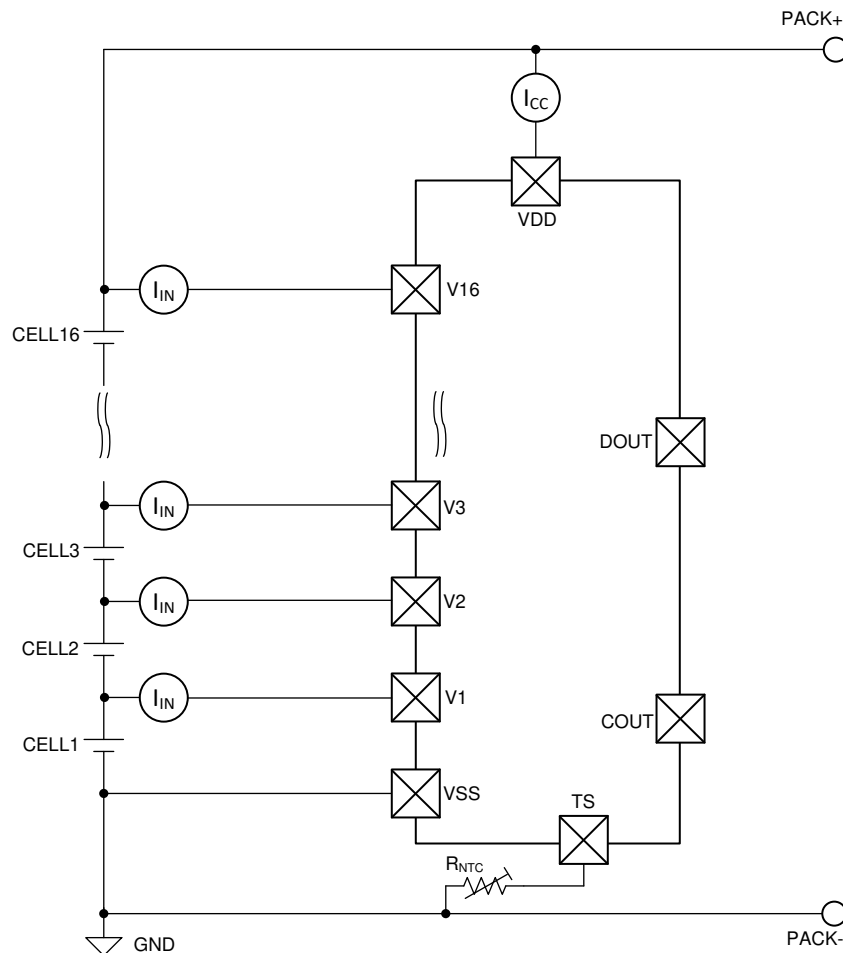


图 10-2. Configuration for IC Current Consumption Test

10.1.2.1 Cell Connection Sequence

The BQ77216 device can be connected to the array of cells in any order without damaging the device.

During cell attachment, the device could detect a fault if the cells are not connected within a fault detection delay period. If this occurs, then COUT and/or DOUT could transition from inactive to active. Both COUT and DOUT can be tied to VSS or VDD to prevent any change in output state during cell attach.

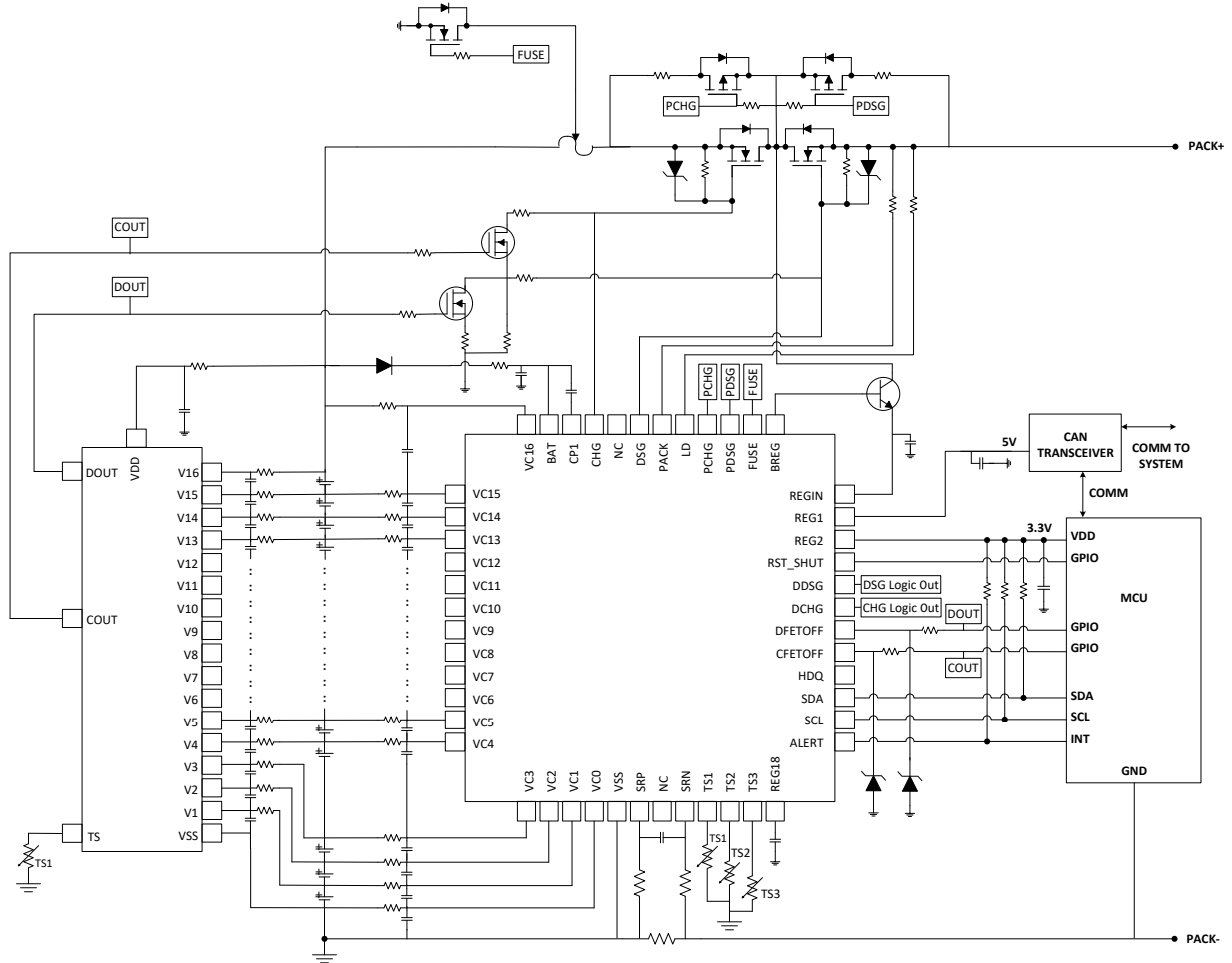


图 10-4. BQ77216 with BQ76952

11 Power Supply Recommendations

The maximum power supply of this device is 85 V on VDD.

12 Layout

12.1 Layout Guidelines

- Ensure the RC filters for the Vn and VDD pins are placed as close as possible to the target terminal.
- The VSS pin should be routed to the CELL - terminal.

12.2 Layout Example

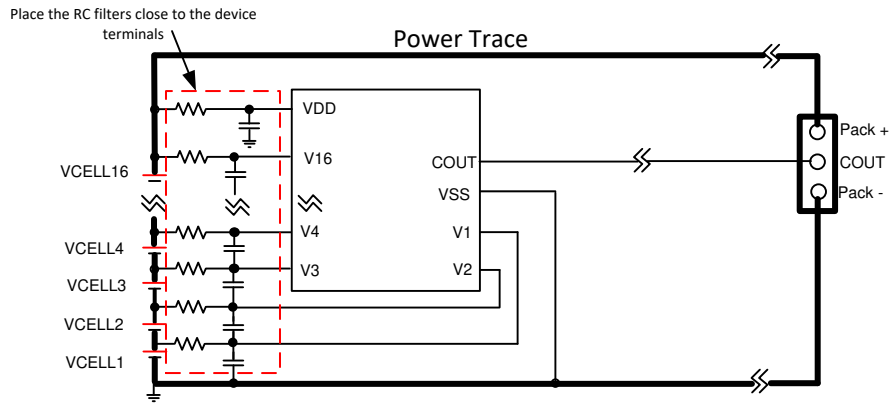


图 12-1. Example Layout

13 Device and Documentation Support

13.1 第三方产品免责声明

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13.3 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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13.4 Trademarks

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13.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ7721600PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7721600	Samples
BQ7721602PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7721602	Samples
BQ7721603PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7721603	Samples
BQ7721605PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	BQ7721605	Samples
BQ7721606PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	BQ7721606	Samples
BQ7721607PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	BQ7721607	Samples
BQ7721609PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	BQ7721609	Samples
BQ7721610PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	BQ7721610	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ7721600PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
BQ7721602PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
BQ7721603PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
BQ7721605PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
BQ7721606PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
BQ7721607PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
BQ7721609PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
BQ7721610PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

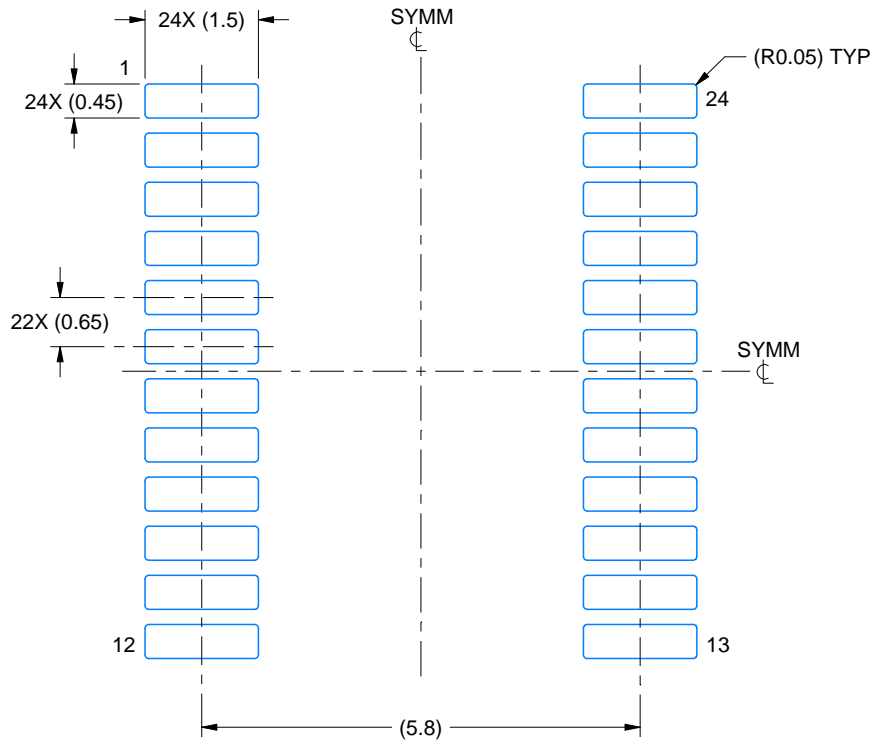
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ7721600PWR	TSSOP	PW	24	2000	356.0	356.0	35.0
BQ7721602PWR	TSSOP	PW	24	2000	356.0	356.0	35.0
BQ7721603PWR	TSSOP	PW	24	2000	356.0	356.0	35.0
BQ7721605PWR	TSSOP	PW	24	2000	356.0	356.0	35.0
BQ7721606PWR	TSSOP	PW	24	2000	356.0	356.0	35.0
BQ7721607PWR	TSSOP	PW	24	2000	356.0	356.0	35.0
BQ7721609PWR	TSSOP	PW	24	2000	356.0	356.0	35.0
BQ7721610PWR	TSSOP	PW	24	2000	356.0	356.0	35.0

EXAMPLE BOARD LAYOUT

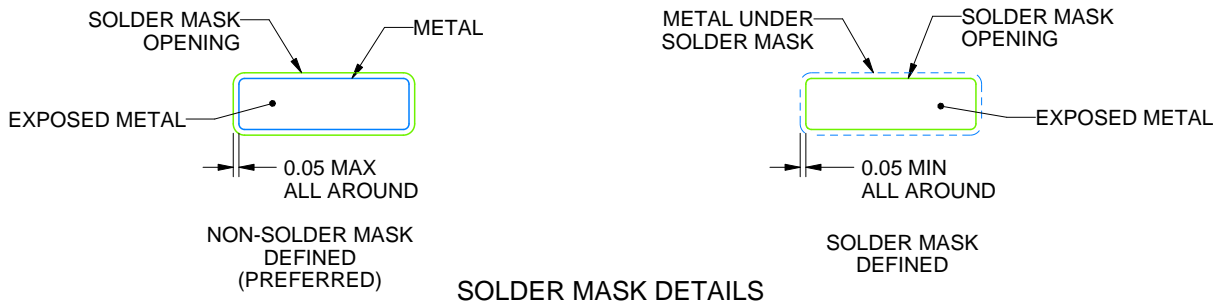
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

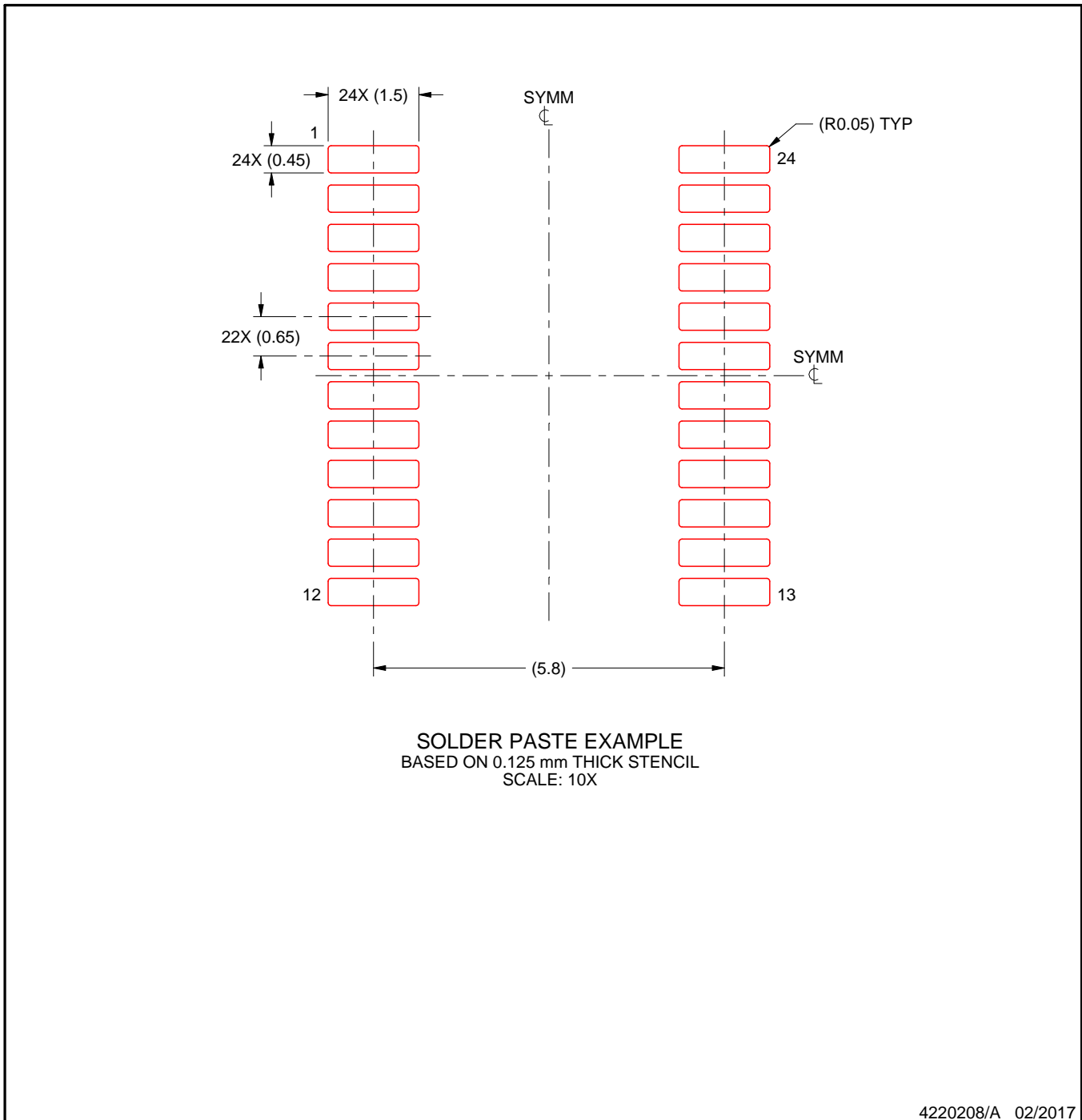
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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