PowerLAN™ Master Gateway Battery Management Controller With PowerPump™ Cell Balancing Technology

Check for Samples: bq78PL116

FEATURES

- **bq78PL116 Designed for Managing 3- to 16-Series-Cell Battery Systems**
  - **Support for LCD and Electronic Paper Displays or EPDs**
  - **Configurable for 11-A, 26-A, or 110-A Operating Currents**
- **Systems With More Than Four Series Cells Require External bq76PL102 Dual-Cell Monitors**
- **SmartSafety Features:**
  - **Prevention: Optimal Cell Management**
  - **Diagnosis: Improved Sensing of Cell Problems**
  - **Fail Safe: Detection of Event Precursors**
- **Rate-of-Change Detection of All Important Cell Characteristics:**
  - **Impedance**
  - **Cell Temperature**
- **PowerPump Technology Transfers Charge Efficiently From Cell to Cell During All Operating Conditions, Resulting in Longer Run Time and Cell Life**
  - **Includes User-Configurable PowerPump Cell-Balancing Modes**
- **High-Resolution 18-Bit Integrating Delta-Sigma Coulomb Counter for Precise Charge-Flow Measurements and Gas Gauging**
- **Multiple Independent Δ-Σ ADCs: One-per-Cell Voltage, Plus Separate Temperature, Current, and Safety**
- **Simultaneous, Synchronous Measurement of Pack Current and Individual Cell Voltages**
- **Very Low Power Consumption**
  - **< 400 µA Active, < 185 µA Standby, < 85 µA Ship, and < 1 µA Undervoltage Shutdown**
- **Accurate, Advanced Temperature Monitoring of Cells and MOSFETs With up to 4 Sensors**
- **Fail-Safe Operation of Pack Protection Circuits: Up to Three Power MOSFETs and One Secondary Safety Output (Fuse)**
- **Fully Programmable Voltage, Current, Balance, and Temperature-Protection Features**
- **External Inputs for Auxiliary MOSFET Control**
- **Smart Battery System 1.1 Compliant via SMBus**

APPLICATIONS

- **Portable Medical Instruments and Test Equipment**
- **Mobility Devices (E-Bike)**
- **Uninterruptible Power Supplies and Hand-Held Tools**

DESCRIPTION

The bq78PL116 master gateway battery controller is part of a complete Li-Ion control, monitoring, and safety solution designed for large series cell strings.

The bq78PL116 along with bq76PL102 PowerLAN™ dual-cell monitors provide complete battery-system control, communications, and safety functions for a structure of three up to 16 series cells. This PowerLAN system provides simultaneous, synchronized voltage and current measurements using one A/D per-cell technology. This eliminates system-induced noise from measurements and allows the precise, continuous, real-time calculation of cell impedance under all operating conditions, even during widely fluctuating load conditions.

PowerPump technology transfers charge between cells to balance their voltage and capacity. Balancing is possible during all battery modes: charge, discharge, and rest. Highly efficient charge-transfer circuitry nearly eliminates energy loss while providing true real-time balance between cells, resulting in longer run-time and improved cycle life.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

Temperature is sensed by up to 4 external sensors and one on-chip sensor. This permits accurate temperature monitoring of each cell individually. Firmware is then able to compensate for the temperature-induced effects on capacity, impedance, and OCV on a cell-by-cell basis, resulting in superior charge/ discharge and balancing control.

External MOSFET control inputs provide user- definable direct hardware control over MOSFET states. Smart control prevents excessive current through MOSFET body diodes. Auxiliary inputs can be used for enhanced safety and control in large multicell arrays.

The bq78PL116 is completely user-configurable, with parametric tables in flash memory to suit a variety of cell chemistries, operating conditions, safety controls, and data reporting needs. It is easily configured using the supplied bqWizard™ graphical user interface (GUI). The device is fully programmed and requires no algorithm or firmware development.

The bq78PL116 pin functions of LED1/SEG1–LED5/SEG5, PSH/BP/TP, and FIELD support LED, LCD, and electronic paper displays (EPDs). The user can configure the bq78PL116 for the desired display type.

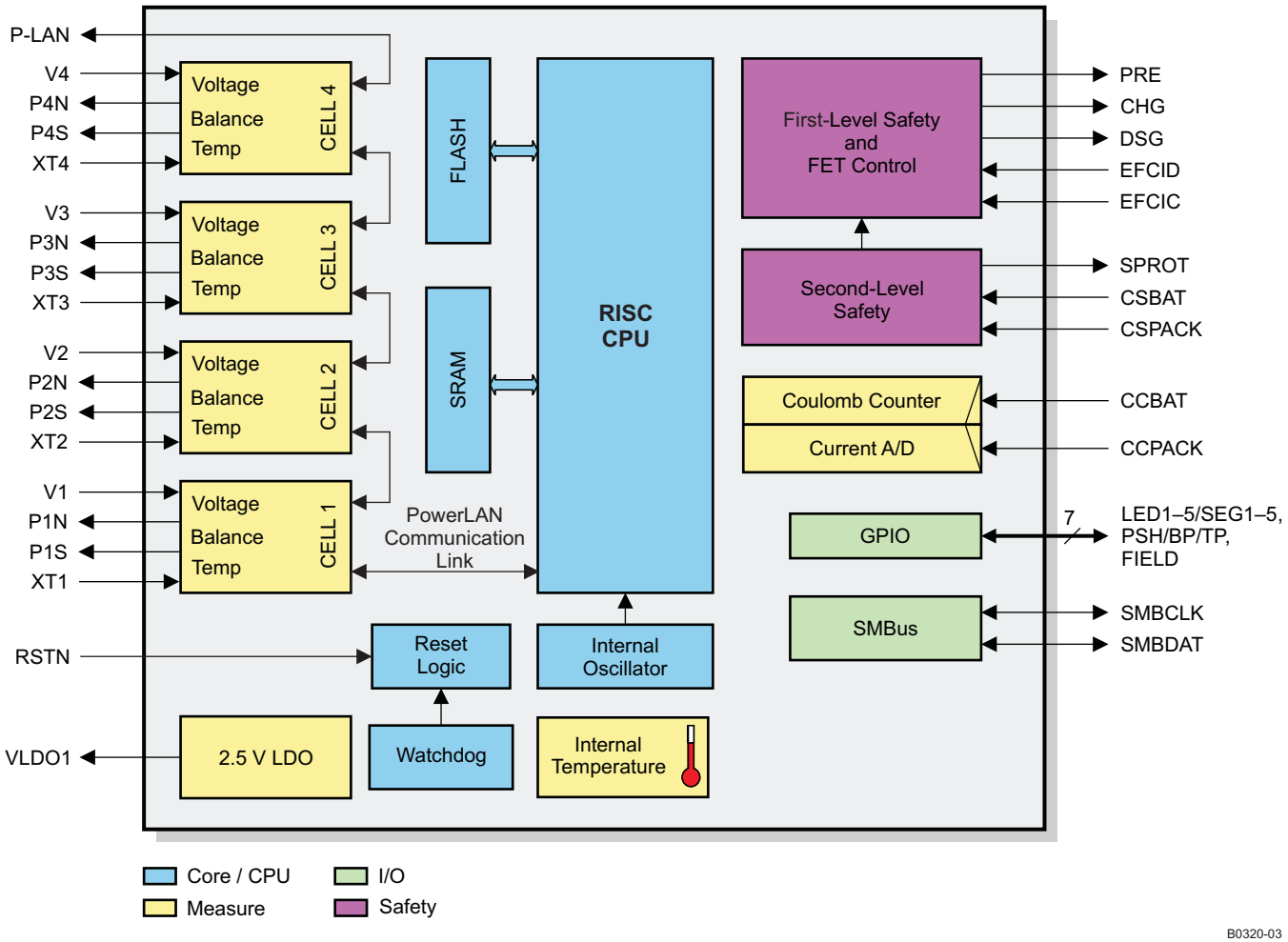


Figure 1. BQ78PL116 Internal Block Diagram

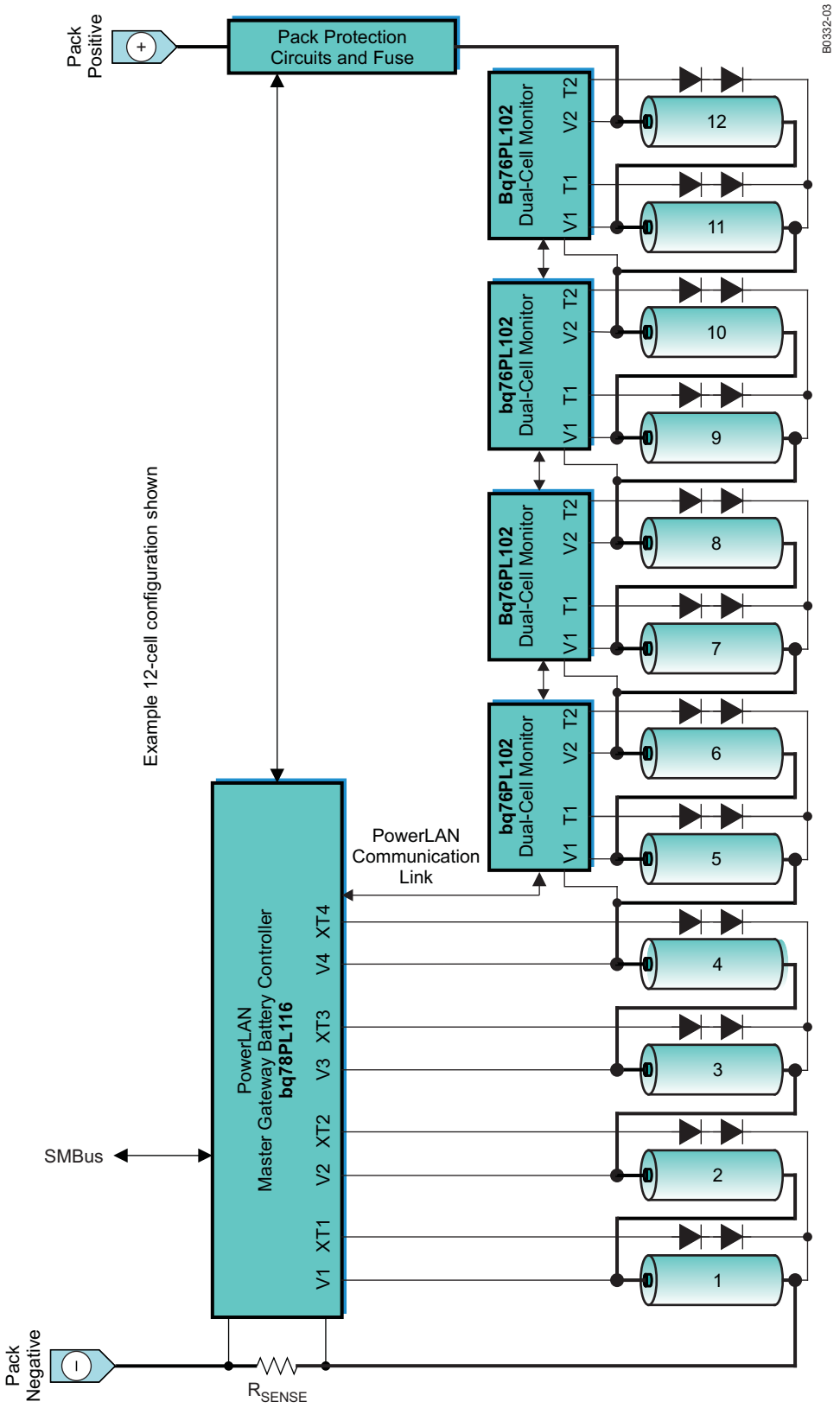


Figure 2. Example bq78PL116 System Implementation (12 Cells)

Table 1. ORDERING INFORMATION

Product	Cell Configuration(1)	Package	Package Designator	Temperature Range	Ordering Number	Quantity, Transport Media
bq78PL116	3 to 16 series cells	QFN-48, 7-mm × 7-mm	RGZ	–40°C to 85°C	bq78PL116RGZT	250, tape and reel
					bq78PL116RGZR	2500, tape and reel

(1) For configurations consisting of more than four series cells, additional bq76PL102 parts must be used.

AVAILABLE OPTIONS

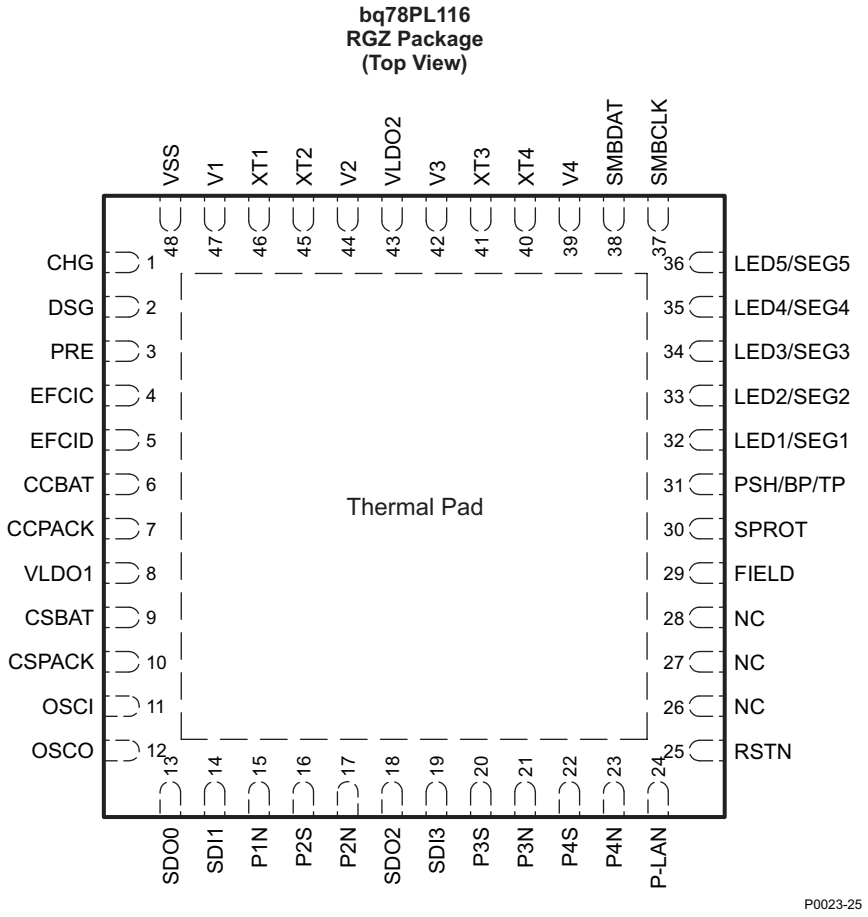


Figure 3. bq78PL116 Pinout

bq78PL116 TERMINAL FUNCTIONS

NAME	NO.	TYPE(1)	DESCRIPTION
CCBAT	6	IA	Coulomb counter input (sense resistor), connect to battery negative
CCPACK	7	IA	Coulomb counter input (sense resistor), connect to pack negative
CHG	1	O	Charge MOSFET control (active-high, low opens MOSFET)
CSBAT	9	IA	Current sense input (safety), connect to battery negative
CSPACK	10	IA	Current sense input (safety), connect to pack negative
DSG	2	O	Discharge MOSFET control (active-high, low opens MOSFET)
EFCIC	4	I	External charge MOSFET control input
EFCID	5	I	External discharge MOSFET control input

(1) Types: I = Input, IA = Analog input, IO = Input/Output, O = Output, P = Power

bq78PL116 TERMINAL FUNCTIONS (continued)

NAME	NO.	TYPE(1)	DESCRIPTION
FIELD	29	O	EPD field segment
LED1/SEG1	32	O	LED1 – open-drain, active-low, LCD and EPD segment 1
LED2/SEG2	33	O	LED2 – open-drain, active-low, LCD and EPD segment 2
LED3/SEG3	34	O	LED3 – open-drain, active-low, LCD and EPD segment 3
LED4/SEG4	35	O	LED4 – open-drain, active-low, LCD and EPD segment 4
LED5/SEG5	36	O	LED5 – open-drain, active-low, LCD and EPD segment 5
N/C	26, 27	IO	Connect 1-MΩ resistor to VSS
N/C	28	O	No connect
OSCI	11	I	External oscillator input (no connect, internal oscillator used)
OSCO	12	O	External oscillator output (no connect, internal oscillator used)
P1N	15	O	Charge-balance gate drive, cell 1 north
P2N	17	O	Charge-balance gate drive, cell 2 north
P2S	16	O	Charge-balance gate drive, cell 2 south
P3N	21	O	Charge-balance gate drive, cell 3 north
P3S	20	O	Charge-balance gate drive, cell 3 south
P4N	23	O	Charge-balance gate drive, cell 4 north
P4S	22	O	Charge-balance gate drive, cell 4 south
P-LAN	24	IO	PowerLAN I/O to external bq76PL102 nodes
PRE	3	O	Precharge MOSFET control (active-high)
PSH/BP/TP	31	IO	Pushbutton detect for LED display, LCD backplane, EPD top plane and charge pump
RSTN	25	I	Device reset, active-low
SDI1	14	I	Connect to SDO0 via a capacitor
SDI3	19	I	Internal PowerLAN connection – connect to SDO2 through a 0.01-µF capacitor
SDO0	13	O	Requires 100-kΩ pullup resistor to VLDO1
SDO2	18	O	Internal PowerLAN connection – connect to SDI3 through a 0.01-µF capacitor
SMBCLK	37	IO	SMBus clock signal
SMBDAT	38	IO	SMBus data signal
SPROT	30	O	Secondary protection output, active-high (FUSE)
V1	47	IA	Cell-1 positive input
V2	44	IA	Cell-2 positive input
V3	42	IA	Cell-3 positive input
V4	39	IA	Cell-4 positive input
VLDO1	8	P	Internal LDO-1 output, bypass with 10-µF capacitor to VSS
VLDO2	43	P	Internal LDO-2 output, bypass with 10-µF capacitor to V2
VSS	48	IA	Cell-1 negative input
XT1	46	IA	External temperature-sensor-1 input
XT2	45	IA	External temperature-sensor-2 input
XT3	41	IA	External temperature-sensor-3 input
XT4	40	IA	External temperature-sensor-4 input
–	–	P	Thermal pad. Connect to VSS

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		RANGE	UNITS
T_A	Operating free-air temperature (ambient)	–40 to 85	°C
T_{stg}	Storage temperature	–65 to 150	°C
V4	Voltage range with respect to V3	–0.5 to 5.0	V
V3	Voltage range with respect to V2	–0.5 to 5.0	V
V2	Voltage range with respect to V1	–0.5 to 5.0	V
V1	Voltage range with respect to VSS	–0.5 to 5.0	V
EFCIC, EFCID	Voltage range with respect to VSS	–0.5 to 5.0	V
LED1/SEG1—LED5/SEG5	Voltage on I/O pin with respect to VSS	–0.5 to 5.0	V
SMBCLK, SMBDAT	Voltage range with respect to VSS	–0.5 to 6.0	V
VLDO1	Voltage with respect to VSS	3.0	V
VLDO2	Voltage range with respect to V2	3.0	V
RSTN	Voltage range with respect to VSS	–0.5 to VLDO1 + 0.5	V
FIELD, SPROT, PSH/BP/TP	Voltage range with respect to VSS	–0.5 to VLDO1 + 0.5	V
CCBAT, CCPACK, CSBAT, CSPACK	Voltage range with respect to VSS	–0.5 to VLDO1 + 0.5	V
CHG, DSG, PRE	Voltage range with respect to VSS	–0.5 to VLDO1 + 0.5	V
OSCI, OSCO	Voltage with respect to VSS	–0.5 to VLDO1 + 0.5	V
XT1, XT2	Voltage with respect to VSS	–0.5 to VLDO1 + 0.5	V
SDO0	Voltage range with respect to VSS	–0.5 to VLDO1 + 0.5	V
XT3, XT4	Voltage range with respect to V2	–0.5 to VLDO2 + 0.5	V
SDO2, SDI3, P-LAN	Voltage range with respect to V2	–0.5 to VLDO2 + 0.5	V
SDO0, SDI1	Voltage range with respect to VSS	–0.5 to V1 + 0.5	V
P1N, P2S, P2N	Voltage range with respect to VSS	–0.5 to V1 + 0.5	V
P3S, P3N, P4S, P4N	Voltage range with respect to V2	–0.5 to V3 + 0.5	V
PRE, CHG, DSG, SPROT, FIELD, PSH/BP/TP	Current source/sink	20	mA
LED1/SEG1–LED5/SEG5	Current source/sink	20	mA
VLDO1, VLDO2	Current source/sink	20	mA
ESD tolerance	JEDEC, JESD22-A114 human-body model, R = 1500 Ω, C = 100 pF	2	kV
Lead temperature, sodlering	Total time < 3 seconds	300	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{SUP}	Supply voltage—V1, V2, V3, V4	All cell voltages equal, four-cell operation	2.5	3.6	4.5	V
		All cell voltages equal, three-cell operation (V3 = V4)	2.8	3.6	4.5	
$V_{Startup}$	Minimum startup voltage—V1, V2, V3, V4	All cell voltages equal	2.9			V
V_{IN}	Input cell voltage range—V(n+1) – V(n), n = 1, 2, 3, 4		0		4.5	V
C_{VLDO1}	VLDO 1 capacitor—VLDO1		2.2	10	47	µF
C_{VLDO2}	VLDO 2 capacitor—VLDO2		2.2	10	47	µF
C_{Vn}	Cell-voltage capacitor—Vn		1			µF

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C (unless otherwise noted)

DC Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Operating-mode current (at V2)	Acrtive mode, cells = 3.6 V		400		µA
I_{STBY}	Standby-mode current (at V2)	SMBCLK = SMBDAT = VSS, I_{BAT} = 0, cells = 3.6 V		185		µA
I_{SHIP}	Ship-mode current (at V2)	SMBCLK = SMBDAT = VSS, I_{BAT} = 0, cells = 3.6 V		85		µA
I_{ECUV}	Extreme cell undervoltage shutdown current	All cells < 2.7 V and any cell < ECUV set point			1	µA
V_{OL}	SPROT, LEDEN, PSH/BP/TP(bq78PL116), FIELD(bq78PL116)	I_{OL} < 4 mA	0		0.5	V
V_{OH} (1)	SPROT, LEDEN, PSH/BP/TP(bq78PL116), FIELD(bq78PL116)	I_{OH} < –4 mA	V_{LDO1} – 0.1			V
V_{IL}	SPROT, LEDEN, PSH/BP/TP(bq78PL116), FIELD(bq78PL116)				0.25 V_{LDO1}	V
V_{IH}	SPROT, LEDEN, PSH/BP/TP(bq78PL116), FIELD(bq78PL116)		0.75 V_{LDO1}			V

(1) Does not apply to SMBus pins.

Voltage-Measurement Characteristics

T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Measurement range		2.75		4.5	V
Resolution			<1		mV
Accuracy(1)	25°C		±3	±7	mV
	0°C to 60°C		±10		
Measurement temperature coefficient		160	180	200	µV/°C

(1) Voltage measurement calibrated at factory

Current-Sense Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Measurement range	Hardware gain = 9	–0.112		0.1	V
Measurement range (SENSE1)	10-mΩ sense resistor(1)	–11.2		10	A
Measurement range (SENSE2)	3-mΩ sense resistor (hardware gain = 13)	–25.8		25.8	A
Measurement range (SENSE3)	1-mΩ sense resistor(2)	–112		100	A
Input offset	T_A = 25°C		±50		µV
Offset drift	T_A = 0°C to 60°C		0.5		µV/°C
Resolution	Hardware gain = 9		10		µV
Full-scale error(3)	T_A = 25°C	±0.1%			
Full-scale error drift	T_A = 0°C to 60°C	50			PPM/°C

(1) Default setting
(2) Measurement range beyond ±32,768 mA requires the use of an SBData IPScale Factor.
(3) After calibration. Accuracy is dependent on system calibration and temperature coefficient of sense resistor.

Coulomb-Count Characteristics(1) (2)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			5		nVh
Intergral nonlinearity			0.008%		
Snap-to-zero (deadband)			±100(3)		µV

(1) Shares common input with current-sense section (CCBAT, CCPACK)
(2) After calibration. Accuracy is dependent on system calibration and temperature.
(3) Corresponds to ±10 mA with 10-mΩ sense resistor

Current-Sense (Safety) Characteristics(1)

over free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Measurement range		–0.312		0.312	V
Minimum threshold setting			25	42	mV
Accuracy(1)	Short-circuit detection	–20		20	mV
	Overcurrent detection, charge and discharge	–4		4	
Resolution	Short-circuit detection		10		mV
	Overcurrent detection, charge and discharge		1.25		
Duration	Short-circuit detection	0.1		3.2	ms
	Overcurrent detection, charge and discharge	0.9		106	

(1) After calibration. Accuracy is dependent on system calibration and temperature coefficient of sense resistor.

Internal Temperature-Sensor Characteristics(1)

over free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Measurement range		–30		85	°C
Resolution			0.1		°C
Accuracy(1)	0° to 85°		±2		°C

(1) After calibration. Accuracy is dependent on system calibration.

LDO Voltage Characteristics(1)

over free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{LDO1}	LDO1 operating voltage, referenced to VSS	Load = –200 µA	2.425	2.5	2.575	V
V_{LDO2}	LDO2 operating voltage, referenced to V2	Load = –2 mA	2.425	2.5	2.575	V

(1) After calibration. Accuracy is dependent on system calibration.

External Temperature-Sensor Characteristics

over free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Measurement range		–40		90	°C
Resolution			0.2		°C
Accuracy(1)	25°		±2		°C
	0° to 85°		±2		
Source current		30	50	70	µA

(1) After calibration. Accuracy is dependent on system calibration.

SMBus Characteristics(1)

over free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input low voltage		0		0.8	V
V_{IH}	Input high voltage		2.1		5.5	V
V_{OL}	Output low voltage	350-µA sink current	0		0.4	V
C_L	Capacitance, each I/O pin				10	pF
f_{SCL}	SCLK nominal clock frequency	T_A = 25°C	10	100	100	kHz
R_{PU}(2)	Pullup resistors for SCLK, SDATA	V_{BUS} 5 V nominal	13.3		45.3	kΩ
		V_{BUS} 3 V nominal	2.4		6.8	

(1) SMBus timing and signals meet the SMBus 2.0 specification requirements under normal operating conditions. All signals are measured with respect to PACK-negative.
(2) Pullups are typically implemented external to the battery pack and are selected to meet SMBus requirements.

PowerLAN Characteristics(1)(2)(3)

over free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_L	Load capacitance	SDI1, SDI3, SDO0, SDO2, P-LAN			100	pF
V_{IH}	Input logic high	SDI1	0.8 VLDO1			V
		SDI3	0.8 VLDO2			
V_{OH}	Output logic high	SDO0, SDO2	0.9 VLDO1			V
		P-LAN	0.9 VLDO2			
V_{IL}	Input logic low	SDI1			0.2 VLDO1	V
		SDI3			0.2 VLDO2	
V_{OL}	Output logic low	SDO0, SDO2			0.1 VLDO1	V
		P-LAN			0.1 VLDO2	
$t_{r(I)}$	Input rise time	SDI1, SDI3			500	ns
$t_{f(I)}$	Input fall time	SDI1, SDI3			500	ns
$t_{r(O)}$	Output rise time	SDO0, SDO2, P-LAN		30	50	ns
$t_{f(O)}$	Output fall time	SDO0, SDO2, P-LAN		30	50	ns

(1) Values specified by design and are over the full input voltage range and the maximum load capacitance.
(2) The SDI and SDO pins are ac-coupled from the cell circuits downstream and upstream, respectively. The limits specified here are the voltage transitions which must occur within the SDI and SDO rise-and fall-time specifications.
(3) Coupling capacitor between PowerLAN pins is 1000 pF. This value is specified by design.

PowerPump Characteristics(1)

over free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High drive, P2S	I_{OUT} = –10 µA	0.9 V1			V
V_{OL}	Low drive, P2S	I_{OUT} = 200 µA			0.1 V1	V
V_{OH}	High drive, P1N, P2N	I_{OUT} = –200 µA	0.9 V1			V
V_{OL}	Low drive, P1N, P2N	I_{OUT} = 10 µA			0.1 V1	V
V_{OH}	High drive, P3S, P4S	I_{OUT} = –10 µA	0.9 V1			V
V_{OL}	Low drive, P3S, P4S	I_{OUT} = 200 µA			0.1 V1	V
V_{OH}	High drive, P3N, P4N	I_{OUT} = –200 µA	0.9 V1			V
V_{OL}	Low drive, P1N, P2N	I_{OUT} = 10 µA			0.1 V1	V
I_{OH}	Source current, P2S, P3S, P4S	V_{OH} = V1 – 0.8 V	250			µA
I_{OL}	Sink current, P1N, P2N, P3N, P4N	VOH = V1 + 0.2 V	–250			µA
t_r	Signal rise time	C_{Load} = 300 pF			100	ns
t_f	Signal FET fall time	C_{Load} = 300 pF			100	ns
f_P	Frequency			204.8		kHz
D	PWM duty cycle	P1N, P2N, P3N, P4N		33%		
		P2S, P3S, P4S		67%(2)		

(1) All parameters representative of a typical cell voltage of 3.6 V.
(2) Effective duty cycle is 33%. PxS pins are P-channel drives and MOSFET on-time is (1 – D).

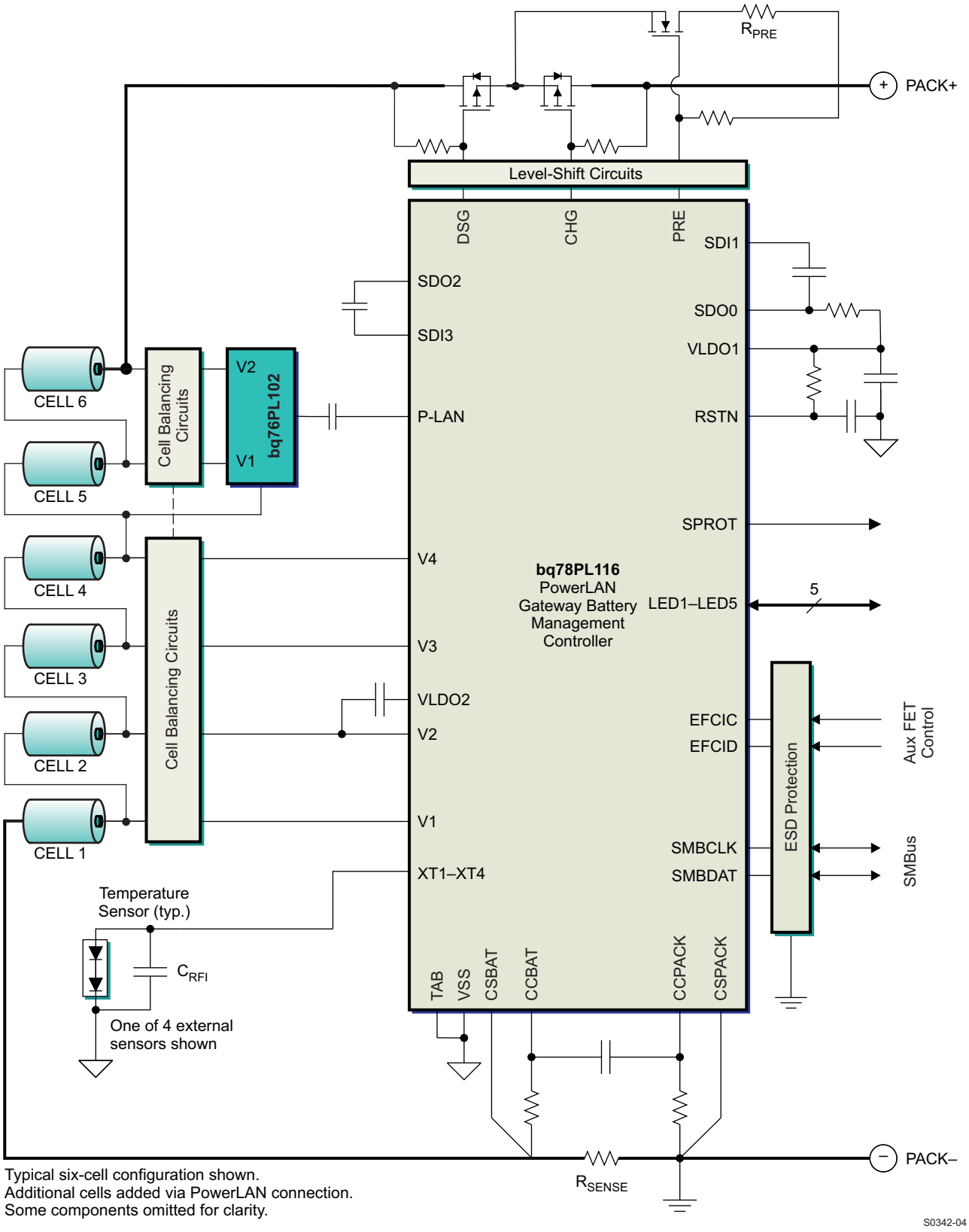


Figure 4. bq78PL116 Simplified Example Circuit Diagram

FEATURE SET

Primary (First-Level) Safety Features

The bq78PL116 implements a breadth of system protection features which are easily configured by the customer. First-level protections work by controlling the MOSFET switches. These include:

- Battery cell over/undervoltage protection
- Pack over/undervoltage protection
- Charge and discharge overcurrent protection
- Short-circuit protection
- External MOSFET control inputs (EFCIx) with programmable polarity
- Up to four external temperature inputs for accurate cell and MOSFET monitoring
- Watchdog timer protection
- Brownout detection and protection against extreme pack undervoltage

Secondary (Second-Level) Safety Features

The bq78PL116 can detect more serious system faults and activate the SPROT pin, which can be used to open an in-line chemical fuse to permanently disable the pack. Secondary optional features include

- Fully independent of first-level protections
- SmartSafety algorithms for early detection of potential faults
  - Temperature abnormalities (extremes, rate of change)
  - Cell imbalance exceeds safety limits
  - Impedance rise due to cell or weld strap fault
- MOSFET failure or loss of MOSFET control
- Safety overvoltage, pack and cell
- Safety overtemperature, limits for both charge and discharge
- Safety overcurrent, charge and discharge
- Failed current measurement, voltage measurement, or temperature measurement

Charge Control Features

- Meets SMBus 1.1 and Smart Battery System (SBS) Specification 1.1 requirements
- Active cell balancing using patented PowerPump technology, which eliminates unrecoverable capacity loss due to normal cell imbalance
- Simultaneous, synchronous measurement of all cell voltages in a pack
- Simultaneous, synchronous measurement of pack current with cell voltages
- Reports target charging current and/or voltage to an SBS Smart Charger
- Reports the chemical state-of-charge for each cell and pack
- Supports precharging and zero-volt charging with separate MOSFET control
- Programmable, Chemistry-specific parameters
- Fault reporting

Gas Gauging

- The bq78PL116 accurately reports battery cell and pack state-of-charge (SOC). No full charge/discharge cycle is required for accurate reporting.
- State-of-charge is reported via SMBus and optional display.
- 18-bit integrating delta-sigma ADC coulomb counter

Display Types

- The bq78PL116 drives a three- to five-segment LED display in response to a pushbutton (LEDEN) input signal. Each LED pin can sink up to 10 mA.
- The bq78PL116 drives a three- to five-segment static liquid-crystal display.
- The bq78PL116 drives a three- to five-segment electronic paper display. An external 15-V voltage source is required. E Ink Corporation supplies this type of display.

The display type is selected via the parameter set.

Lifetime Logging (Readable via SMBus)

- Lifetime delivered ampere-hours
- Last discharge average
- Lifetime maximum power
- Maximum/minimum temperature
- Maximum/minimum pack voltage
- Maximum/minimum cell voltage in a pack
- Maximum charge and discharge currents

Power Modes

- **Normal Mode:** The bq78PL116 performs measurements and calculations, makes decisions, and updates internal data approximately once per second. *All safety circuitry is fully functional in this mode.*
- **Standby Mode:** The bq78PL116 performs as in normal mode, but at a dramatically reduced rate to lower power consumption at times when the host computer is inactive or the battery system is not being used. *All safety circuitry remains fully functional in this mode.*
- **Ship Mode:** The bq78PL116 disables (opens) all the protection MOSFETs, and continues to monitor temperature and voltage, but at a reduced measurement rate to dramatically lower power consumption. Environmental data is saved in flash as a part of the historical record. *Safety circuitry is disabled in this mode*. The device does not enter this power state as a part of normal operation; it is intended for use after factory programming and test. Entry occurs only after a unique SMBus command is issued. Exit occurs when the SMBus lines return to an active state.
- **Extreme Cell Undervoltage (ECUV) Shutdown Mode:** In this mode, the bq78PL116 draws minimal current and the charge and discharge protection MOSFETs are disabled (opened). The precharge MOSFET remains enabled when a charge voltage is present. *Safety circuitry is disabled in this mode*. The device does not enter this mode as a part of normal operation; it enters this state during extreme cell undervoltage conditions (ECUV). The ECUV threshold is programmable between 2.5 V and 2.8 V for even series cell applications and 2.7 V to 2.8 V for odd series cell applications.

STATE	OVERCURRENT PROTECTION	ENTRY CONDITION	EXIT CONDITION
Active	Fully active	Normal operation as determined by firmware	Firmware directed to the following operating modes
Standby	Fully active	No load current flowing for predetermined time	Load activity
Ship	Not active	Protected SMBus command	SMBus becomes active
Extreme cell undervoltage	Not active (precharge enabled)	Enabled when Vcell < ECUV	Vcell charge above ECUV recovery threshold (2.9 V/cell typical)

OPERATION

The bq78PL116 battery-management controller serves as a master controller for a Li-Ion battery system consisting of up to 16 cells in series. Any number of cells may be connected in parallel; other system or safety issues limit the number of parallel cells. The bq78PL116 provides extraordinarily precise state-of-charge gas gauging along with first- and second-level pack safety functions. Voltage and current measurements are performed synchronously and simultaneously for all cells in the system, allowing a level of precision not previously possible in battery management. Temperature is measured by up to four additional external temperature sensors. Coulomb counting is captured continuously by a dedicated 18-bit integrating delta-sigma ADC in the bq78PL116. The CPU in the bq78PL116 is also responsible for system data calculations and communicating parameters via the SMBus interface.

PowerLAN Communication Link

PowerLAN technology is Texas Instruments' patented serial network and protocol designed specifically for battery management in a multicell system environment. The PowerLAN link is used to initiate and report measurements of cell voltage and temperature, and control cell balancing. The bq78PL116 serves as the master controller of the PowerLAN link and can interface to multiple bq76PL102 dual-cell battery monitors, which measure and balance additional cells. The bq78PL116 monitors the first three or four cells, and bq76PL102s can be added to monitor more series cells.

The PowerLAN link isolates voltages from adjacent bq76PL102 devices to permit high-voltage stack assembly without compromising precision and accuracy. The PowerLAN link is expandable to support up to 16 cells in series. Each bq76PL102 handles voltage and temperature measurements, as well as balancing for two cells. The PowerLAN link provides high ESD tolerance and high immunity to noise generated by nearby digital circuitry or switching currents. Each bq76PL102 has both a PowerLAN input and PowerLAN output: Received data is buffered and retransmitted, permitting high numbers of nodes without loss of signal fidelity. Signals are capacitor-coupled between nodes, providing dc isolation.

Safety

Unique in the battery-management controller market, the bq78PL116 simultaneously measures voltage and current using independent and highly accurate delta-sigma ADCs. This technique removes virtually all systemic noise from measurements, which are made during all modes of battery operation: charge, discharge, and rest. The bq78PL116 also directs all connected bq76PL102 dual-cell battery monitors to measure each cell voltage simultaneously with the bq78PL116 measurements. Battery impedance and self-discharge characteristics are thus measured with an unprecedented level of accuracy in real time. The bq78PL116 applies this precise information to SmartSafety algorithms to detect certain anomalies and conditions which may be indicative of internal cell faults, before they become serious problems.

The bq78PL116 uses its enhanced measurement system to detect system faults including cell under- and overvoltage, cell under- and overtemperature, system overvoltage, and system overcurrent. First-level safety algorithms first attempt to open the MOSFET safety switches. If this fails, second-level safety algorithms activate the SPROT output, normally used to open a fuse and provide permanent, hard protection for the systems. External MOSFET control inputs with programmable polarity can also be used to operate the safety MOSFETs under control of user supplied circuitry. The bq78PL116 continuously monitors these inputs. If any MOSFET fails to open when commanded; the 2^{nd} level safety algorithms also activate the SPROT output. All first- and second-level safety algorithms have fully programmable time delays to prevent false triggering.

Cell Balancing

Patented PowerPump cell balancing technology drastically increases the useful life of battery packs by eliminating the cycle life fade of multi-cell packs due to cell imbalance. PowerPump technology efficiently transfers charge from cell to cell, rather than simply bleeding off charging energy as heat as is typically done with resistive-bleed balancing circuits. Balancing is configurable and may be performed during any battery operational modes: charge, discharge, or rest. Compared to resistive bleed balancing, virtually no energy is lost as heat. The actual balance current is externally scalable and can range from 10 mA to 1 A (100 mA typical) depending on component selection and system or cell requirements.

A variety of techniques, such as simple terminal voltage, terminal voltage corrected for impedance and temperature effects, or state-of-charge balancing, is easily implemented by the bq78PL116. By tracking the balancing required by individual cells, overall battery safety is enhanced, often allowing early detection of soft shorts or other cell failures. Balancing is achieved between all cells within the pack as dynamically determined by the bq78PL116.

The bq78PL116 supports the following configurable cell-balancing features:

- Turbo-pump mode. When enabled, this allows 60%–70% pump availability when there are no active safety events and current is not flowing. While in turbo-pump mode, temperature rate-of-rise features are not available.
- Option to disable cell balancing during discharge
- Option to disable cell balancing during charge
- Test mode operation that allows for convenient production-line testing of PowerPump circuitry

Outputs

Charge Control

The CHG and PRE outputs are ordinarily used to drive MOSFET transistors controlling charge to the cell stack. Charge or precharge mode is selected based on the present cell voltage compared to the user-definable cell precharge, undervoltage, and temperature thresholds. When below these limits, the PRE signal is active and the CHG signal is inactive. This turns on the precharge MOSFET and is used to charge a depleted system through a current-limiting series resistor. When all cell voltages are above the limit and the temperature is above the charge temperature minimum, then the CHG output also becomes active and enables the charge MOSFET to turn on, providing a high-current path between charger and battery cells.

The CHG and PRE MOSFET control outputs are both disabled (low) when any cell reaches the safety cutoff limit or temperature threshold. During active charging modes (and above cell voltage thresholds), the discharge MOSFET is also enabled to avoid excessive heating of the body diode. Similarly, the charge MOSFET is active during discharge, provided current flow is in the correct direction and no safety violations are present.

The CHG and PRE outputs are intended to drive buffer transistors acting as inverting level shifters.

Discharge Control

The DSG output operates similarly to control-system discharging. It is enabled (high) by default. If a cell voltage falls below a programmable threshold, or excessive current or other safety related fault is sensed, the DSG output is disabled (low) to prevent damage to the cells.

All facets of safely charging and discharging the cell stack are controlled by user-definable parameters which provide precise control over MOSFET states. Both system and cell over- and undervoltage limits are provided, as well as programmable hysteresis to prevent oscillation. Temperature and current thresholds are also provided, each with independent timers to prevent nuisance activations.

The DSG output is intended to drive a buffer transistor acting as an inverting level-shifter.

Display

The bq78PL116 shows state-of-charge indication on LED, static liquid crystal, and electronic paper displays or EPDs in a bar-graph-type format. The parameter set allows selection of display type and configuration. PSH/BP/TP is a multifunction pin. In LED display mode, PSH serves as an input that monitors for closure of a state-of-charge indicator (SOCi) push-button switch. In LCD mode, this pin is used to drive the LCD backplane. In EPD mode, this pin drives the top plane common signal of the display.

In LED display mode, the signals LED1/SEG1–LED5/SEG5 are current-sinking outputs designed to drive low-current LEDs.

In LCD and EPD modes, the LED1/SEG1–LED5/SEG5 pins drive the active segments through external buffer transistors. In EPD mode, the FIELD pin drives the display background field.

Electronic paper displays require an external power supply, typically 15 V, to power the display. In EPD, mode the bq78PL116 strobes the display outputs for a user- programmable period of milliseconds to drive an external voltage multiplier or charge pump to the required display supply voltage. The display segments are then updated in a manner that ensures the required 0-Vdc segment voltage offset is maintained and keeps the external power supply at its nominal voltage.

Inputs

Current Measurement

Current is monitored by four separate ADCs. All use the same very low-value sense resistor, typically 10, 3, or 1 milliohms in series with the pack negative connection. CCBAT and CCPACK connections to the sense resistor use an R/C filter for noise reduction. (CSBAT and CSPACK are direct connections used for secondary safety). When configured to use a 1-milliohm sense resistor, the maximum available pack capacity increases to 327 Ah from 32.7 Ah.

A 14-bit delta-sigma ADC is used to measure current flow accurately in both directions. The measurements are taken simultaneously and synchronously with all the cell voltage measurements, even those cells measured by bq76PL102 dual-cell battery monitors.

Coulomb Counting

A dedicated coulomb counter is used to measure charge flow with 18-bit precision in both directions by a calibrated, integrating delta-sigma ADC. This allows the bq78PL116 to keep very accurate state-of-charge (SOC) information and battery statistics. A small deadband is applied to further reduce noise effects. The coulomb counter is unique in that it continues to accumulate (integrate) current flow in either direction even as the rest of the internal microcontroller is placed in a very low power state, further lowering power consumption without compromising system accuracy.

Safety Current

Two additional ADCs are used to directly monitor for overcurrent or short-circuit current conditions, independently of the internal function. This provides a direct and rapid response to insure pack integrity and safe operation by opening the appropriate MOSFETs. These functions are implemented in hardware, and do not require firmware for functionality.

Voltage Measurement

Voltage measurement is performed by four independent delta-sigma ADCs which operate simultaneously and are triggered synchronously so that all voltages are read at precisely the same moment. The bq78PL116 coordinates the attached bq76PL102 dual-cell battery monitors so they also perform their cell voltage measurements in sync with the bq78PL116 voltage and current measurements. Voltage measurements are converted with better than 1 mV of resolution, providing superior accuracy. One-ADC-per-cell technology means that voltage is also measured simultaneously with current, permitting accurate, real-time cell impedance calculation during all operating conditions. This technique also provides greatly enhanced noise immunity and filtering of the input signal without signal loss.

Temperature Measurement

XT1–XT4 are dedicated temperature-sensor inputs. Each external sensor consists of a low-cost silicon diode (dual diode in one package is recommended) and capacitor combination. The bq78PL116 can report all four of these temperatures individually. The bq78PL116 firmware uses the internal temperature sensor of the device for board temperature measurements.

EFCIx

The external MOSFET control inputs are for user control of MOSFETs based on external circuitry and conditions. The polarity of the input signal is user-programmable. These pins can be used to force the protection MOSFETs to an OFF state.

COMMUNICATIONS

SMBus

The bq78PL116 uses the industry-standard Smart Battery System's two-wire System Management Bus (SMBus) communications protocol for all external communication. SMBus version 1.1 is supported by the bq78PL116, and includes clock stretching, bus fault time-out detection, and optional packet error checking (PEC). For additional information, see the www.smbus.org and www.sbs-forum.org Web sites.

Smart Battery Data (SBData)

The bq78PL116 supports Smart Battery System's (SBS) Smart Battery Data Specification 1.1. See the SBS/SMBus site at www.sbs-forum.org for further information regarding these specifications.

This SBS Data (SBData) specification defines read/write commands for accessing data commonly required in laptop computer applications. The commands are generic enough to be useful in most applications.

The bq78PL116 provides a wealth of data beyond the standard set of SBData (0x00 - 0x23) through Extended SBData Commands. See the following table for a listing of the SBData commands and the default set of Extended SBData (0x3C - 0x58). SBData command locations 0x80 and 0x81 are used to implement some of the features unique to the bq78PL116. Refer to the bq78PL116 Technical Reference Manual Document for additional details on compliance to SBData and how to take advantage of the data and controls specific to bq78PL116.

THERMAL PAD

The large pad on the bottom of the package is square, located in the center, and is 5.3 ±0.05 mm per side.

SBS Standard Data Parameter List (Abridged)(1)

Command	Data Type	Description
00	R/W word (unsigned)	Manufacturer Access
01	R/W word (unsigned)	Remaining Capacity Alarm Level
02	R/W word (unsigned)	Remaining Time Alarm Level
03	R/W word (unsigned)	Battery Mode
04	R/W word (unsigned)	At Rate value used in AtRate calculations – NOT SUPPORTED
05	Read word (unsigned)	At Rate Time to Full – NOT SUPPORTED
06	Read word (unsigned)	At Rate Time to Empty – NOT SUPPORTED
07	Read word (Boolean)	At Rate OK – NOT SUPPORTED
08	Read word (unsigned)	Pack Temperature (maximum of all individual cells)
09	Read word (unsigned)	Pack Voltage (sum of individual cell readings)
0A	Read word (unsigned)	Pack Current
0B	Read word (unsigned)	Average Pack Current
0C	Read word (unsigned)	Max Error
0D	Read word (unsigned)	Relative State of Charge
0E	Read word (unsigned)	Absolute State of Charge
0F	Read word (unsigned)	Remaining Pack Capacity
10	Read word (unsigned)	Full Charge Capacity
11	Read word (unsigned)	Run Time to Empty
12	Read word (unsigned)	Average Time to Empty
13	Read word (unsigned)	Average Time to Full
14	Read word (unsigned)	Charging Current
15	Read word (unsigned)	Charging Voltage
16	Read word (unsigned)	Battery Status
17	Read word (unsigned)	Cycle Count
18	Read word (unsigned)	Design Capacity
19	Read word (unsigned)	Design Voltage
1A	Read word (unsigned)	Specification Information
1B	Read word (unsigned)	Manufacture Date
1C	Read word (unsigned)	Serial Number
1D–1F	Reserved	
20	Read block (string)	Pack Manufacturer Name (31 characters maximum)
21	Read block (string)	Pack Device Name (31 characters maximum)
22	Read block (string)	Pack Chemistry
23	Read block (string)	Manufacturer Data
24–2E	Reserved	
2F	R/W Block	Optional Manufacturer Function 5
30–3B	Reserved	
3C	R/W word (unsigned)	Optional Manufacturer Option 4 (Vcell 1)
3D	R/W word (unsigned)	Optional Manufacturer Option 3 (Vcell 2)
3E	R/W word (unsigned)	Optional Manufacturer Option 2 (Vcell 3)
3F	R/W word (unsigned)	Optional Manufacturer Option 1 (Vcell 4)
40	R/W word (unsigned)	Extended Data (Vcell 5)
41	R/W word (unsigned)	Extended Data (Vcell 6)
42	R/W word (unsigned)	Extended Data (Vcell 7)
43	R/W word (unsigned)	Extended Data (Vcell 8)
44	R/W word (unsigned)	Extended Data (Vcell 9)

(1) Parameters 0x00–0x3F are compatible with the SBDATA specification.

Command	Data Type	Description
45	R/W word (unsigned)	Extended Data (Vcell 10)
46	R/W word (unsigned)	Extended Data (Vcell 11)
47	R/W word (unsigned)	Extended Data (Vcell 12)
48	R/W word (unsigned)	Extended Data (Vcell 13)
49	R/W word (unsigned)	Extended Data (Vcell 14)
4A	R/W word (unsigned)	Extended Data (Vcell 15)
4B	R/W word (unsigned)	Extended Data (Vcell 16)
4C	R/W word (unsigned)	Extended Data (Temp 0 – Intenal)
4D	R/W word (unsigned)	Extended Data (Temp 1 – Extenal)
4E	R/W word (unsigned)	Extended Data (Temp 2 – Extenal)
4F	R/W word (unsigned)	Extended Data (Temp 3 – Extenal)
50	R/W word (unsigned)	Extended Data (Temp 4 – Extenal)
51	R/W word (unsigned)	Extended Data (Safety Status)
52	R/W word (unsigned)	Extended Data (Permanent Fail Status)
53	R/W word (unsigned)	Extended Data (Charge Status)
54	R/W word (unsigned)	Extended Data (Lifetime Maximum Pack Voltage)
55	R/W word (unsigned)	Extended Data (Lifetime Maximum Cell Voltage)
56	R/W word (unsigned)	Extended Data (Lifetime Maximum Charge Current)
57	R/W word (unsigned)	Extended Data (Lifetime Maximum Discharge Current)
58	R/W word (unsigned)	Extended Data (Lifetime Maximum Temperature)
80	R/W word (unsigned)	Extended Command (Device Status)
81	R/W word (unsigned)	Extended Command (Device Command)

REFERENCE SCHEMATICS

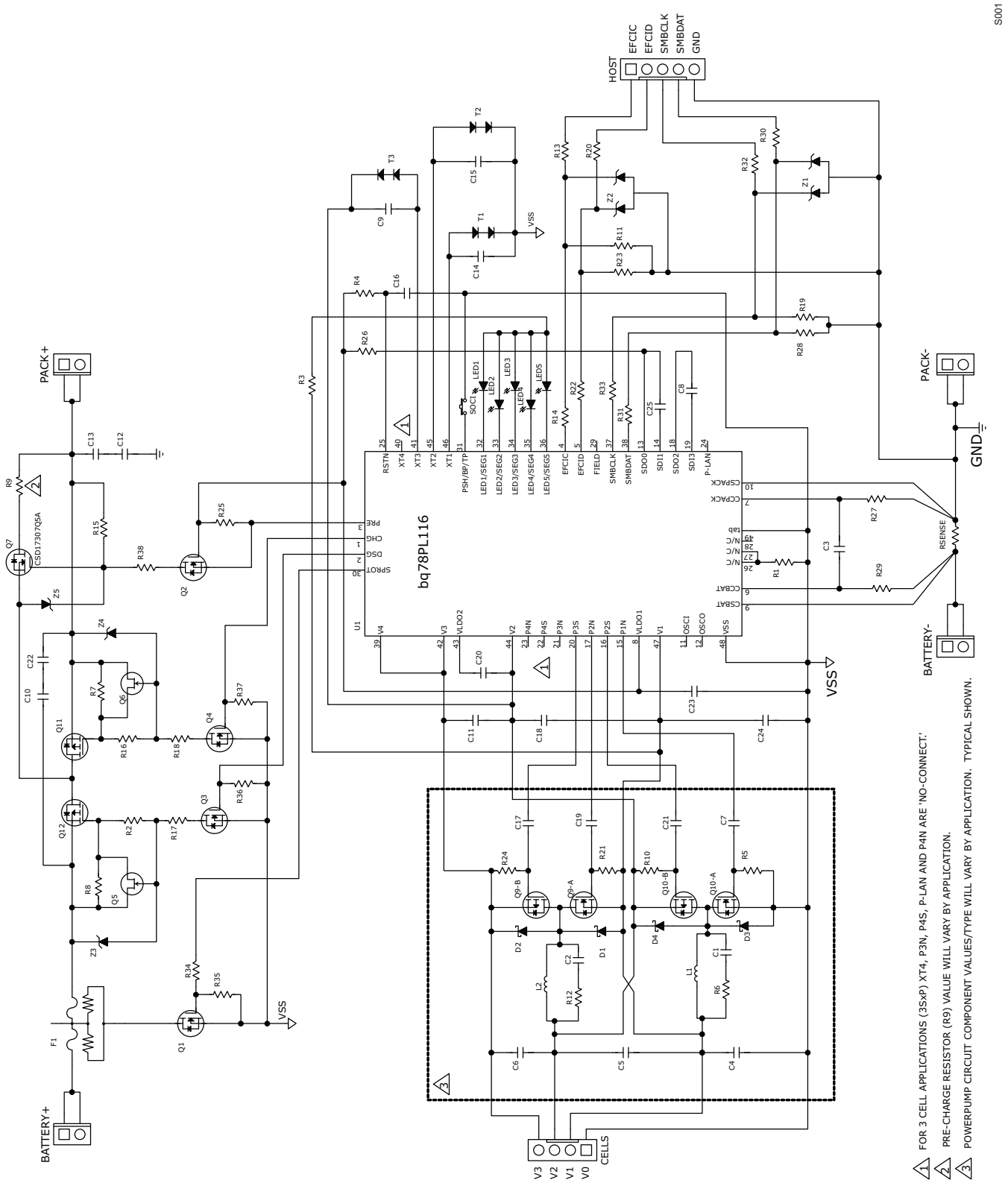


Figure 5. Typical 3S Application Schematic

Table 2. Bill of Materials for 3S Application

Qty	Reference	Value	Description	Size	Manufacturer	Mfg Part No.
5	C10 C12-13 C16 C22	0.1uF	Capacitor SMT Ceramic X7R +/-10% 50V	603	Standard	Standard
5	C11 C18 C20 C23-24	10uF	Capacitor SMT Ceramic X5R +/-10% 6.3V	603	Standard	Standard
3	C1-3	0.01uF	Capacitor SMT Ceramic X7R +/-10% 25V	603	Standard	Standard
3	C4-6	22uF	Capacitor SMT Ceramic Y5V +/-20% 10V	805	Standard	Standard
4	C7 C17 C19 C21	3300pF	Capacitor SMT Ceramic X7R +/-10% 50V	603	Standard	Standard
5	C8-9 C14-15 C25	1000pF	Capacitor SMT Ceramic X7R +/-10% 50V	603	Standard	Standard
12	R1 R7-8 R11 R15 R19 R23 R25 R28 R36-38	1.0M	Resistor SMT 1/10W +/-5%	603	Standard	Standard
2	R17-18	30K	Resistor SMT 1/10W +/-5%	603	Standard	Standard
2	R2 R16	200K	Resistor SMT 1/10W +/-5%	603	Standard	Standard
2	R26 R35	100K	Resistor SMT 1/10W +/-5%	603	Standard	Standard
2	R27 R29	4.7K	Resistor SMT 1/10W +/-5%	603	Standard	Standard
11	R3 R6 R12-14 R20 R22 R30-33	100	Resistor SMT 1/10W +/-5%	603	Standard	Standard
2	R4 R34	10K	Resistor SMT 1/10W +/-5%	603	Standard	Standard
4	R5 R10 R21 R24	20K	Resistor SMT 1/10W +/-5%	603	Standard	Standard
1	R9	100	Resistor SMT +/-5% 1W	603	Standard	Standard
1	RSENSE	0.01	Resistor SMT +/-1% 1W +/-100ppm/°C	2512	Standard	Standard
4	D1-4	Vf=385mV	Schottky Rectifier Diode 20V IFSM>2A	SOD-123	Standard	Standard
2	L1-2	4.7uH	Inductor SMT Shielded Isat=2.0A	4.9mm x 4.9mm x 2.0mm	Taiyo Yuden	NRS5020T4R7MMGJ
5	LED1-5		Green LED	603	Standard	Standard
1	SOCI	50mA	Momentary Pushbutton		Standard	Standard
3	T1-3		Dual Diode (Series Arrangement)	SOT-23	Fairchild	MMBD4148SE
4	Q1-4		N-Channel MOSFET 2.5Vgs rated, Vds>30V	SOT-23	Infineon	BSS138N
2	Q5-6	Vdg = -40V	N-Channel JFET Idss>0.2mA, Vgs<-1.5V	SOT-23	Fairchild	MMBFJ201
1	Q7	9.7 mOhm RDSon	MOSFET N-Channel SMT 30Vds	SON 5mm x 6mm	Texas Instruments	CSD17307Q5A
2	Q9-10		MOSFET N/P Complementary Pair	6-TSOP	Alpha & Omega	AO6604

Table 2. Bill of Materials for 3S Application (continued)

Qty	Reference	Value	Description	Size	Manufacturer	Mfg Part No.
2	Q11-12		MOSFET P-Channel SMT -30VDS	SOIC-8	Fairchild	FDS6673
1	U1		PowerLAN Master Gateway Battery Management Controller	QFN48	Texas Instruments	bq78PL116RGZR
3	Z1-2 Z5	5.6V	Common Anode Zener Diode Pair 300mW	SOT-23	Standard	Standard
2	Z3-4	12V	Zener Diode 500mW	SOD-123	Diodes, Inc	BZT52C12-13-F
1	F1	12 Amp	Chemical Fuse For 2-3 Cells In Series		Sony	SFH-1212A
4	BATTERY+ BATTERY- PACK+ PACK-		2 Pin Connector		Standard	Standard
1	CELLS		4 Pin Connector		Standard	Standard
1	HOST		5 Pin Connector		Standard	Standard

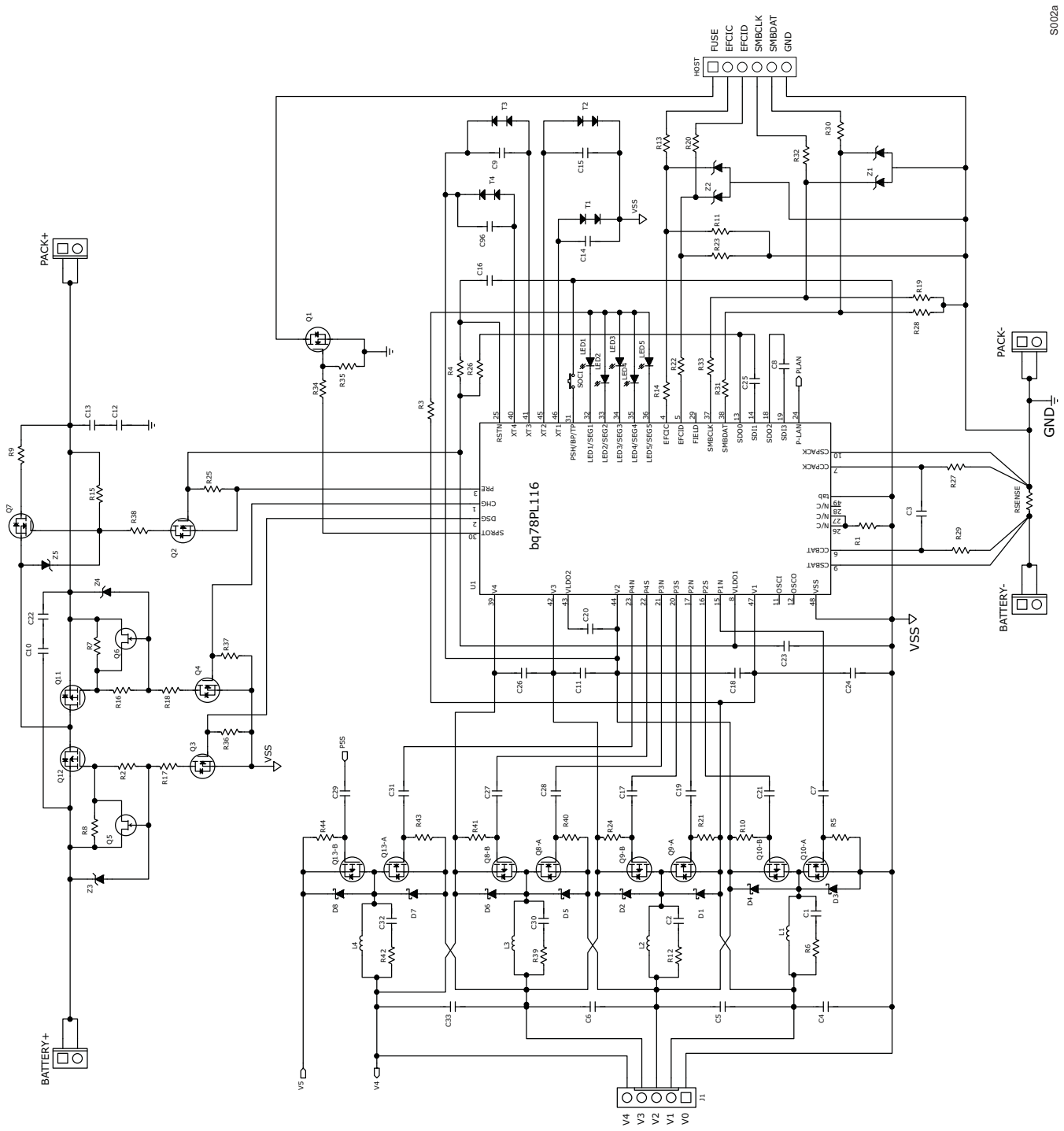


Figure 6. Typical 16S Application Circuit – bq78PL116 and FETs (Sheet 1 of 4)

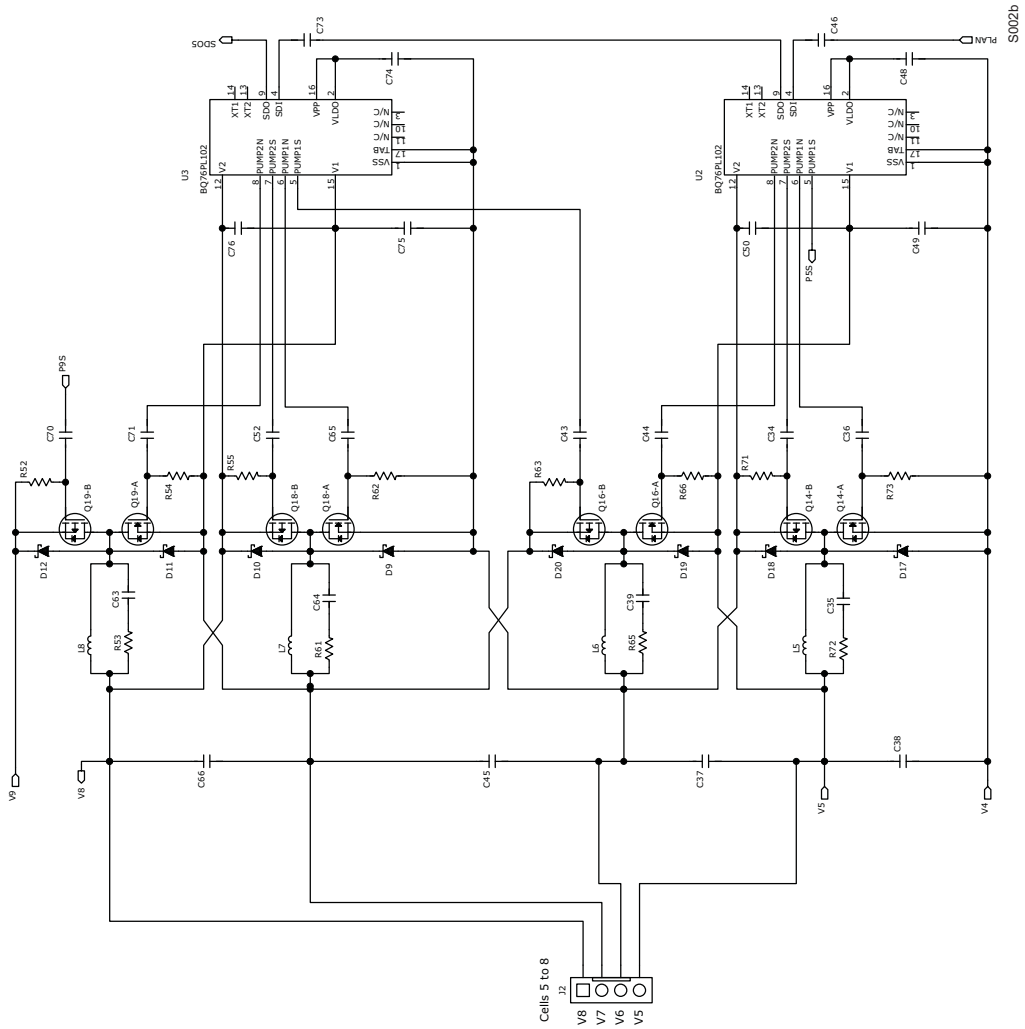


Figure 7. Typical 16S Application Circuit – bq76PL102 for Cells 5–8 (Sheet 2 of 4)

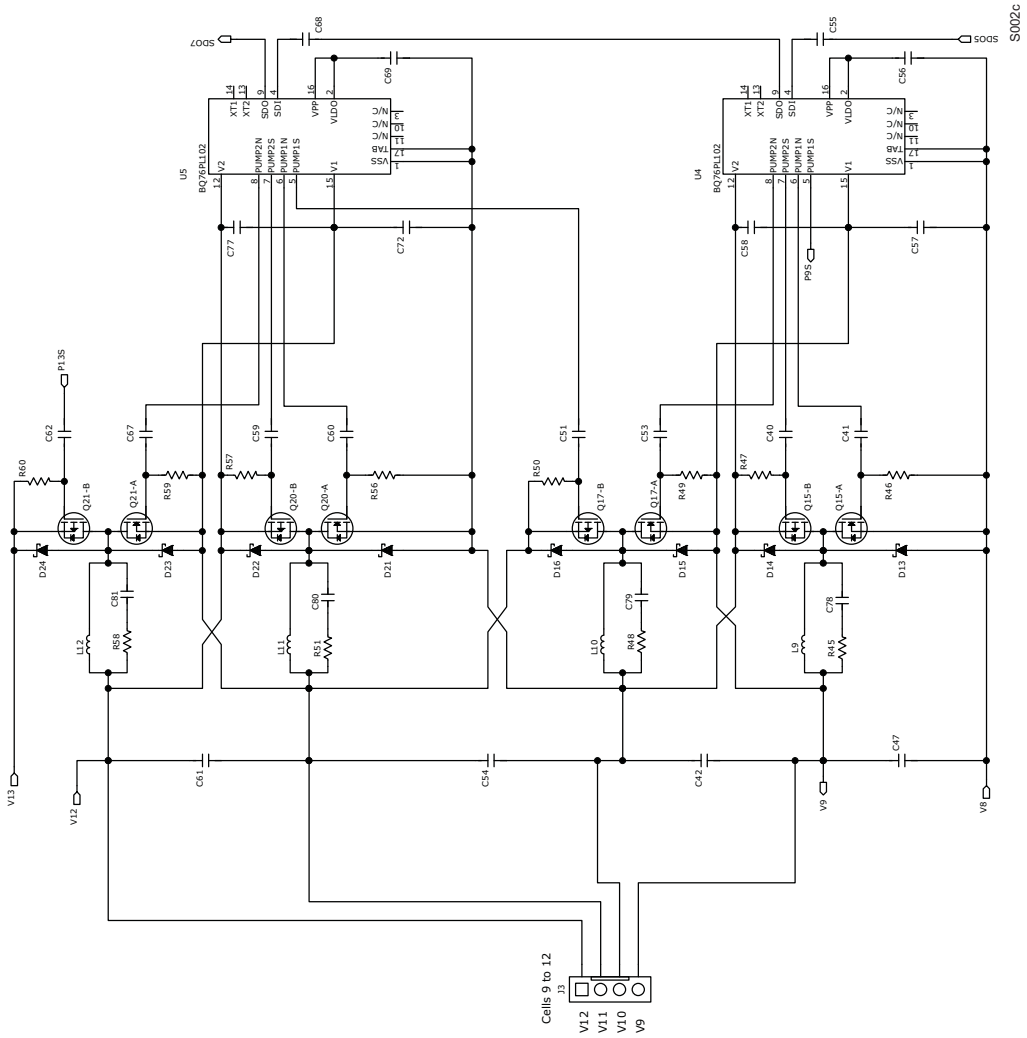


Figure 8. Typical 16S Application Circuit – bq76PL102 for Cells 9–12 (Sheet 3 of 4)

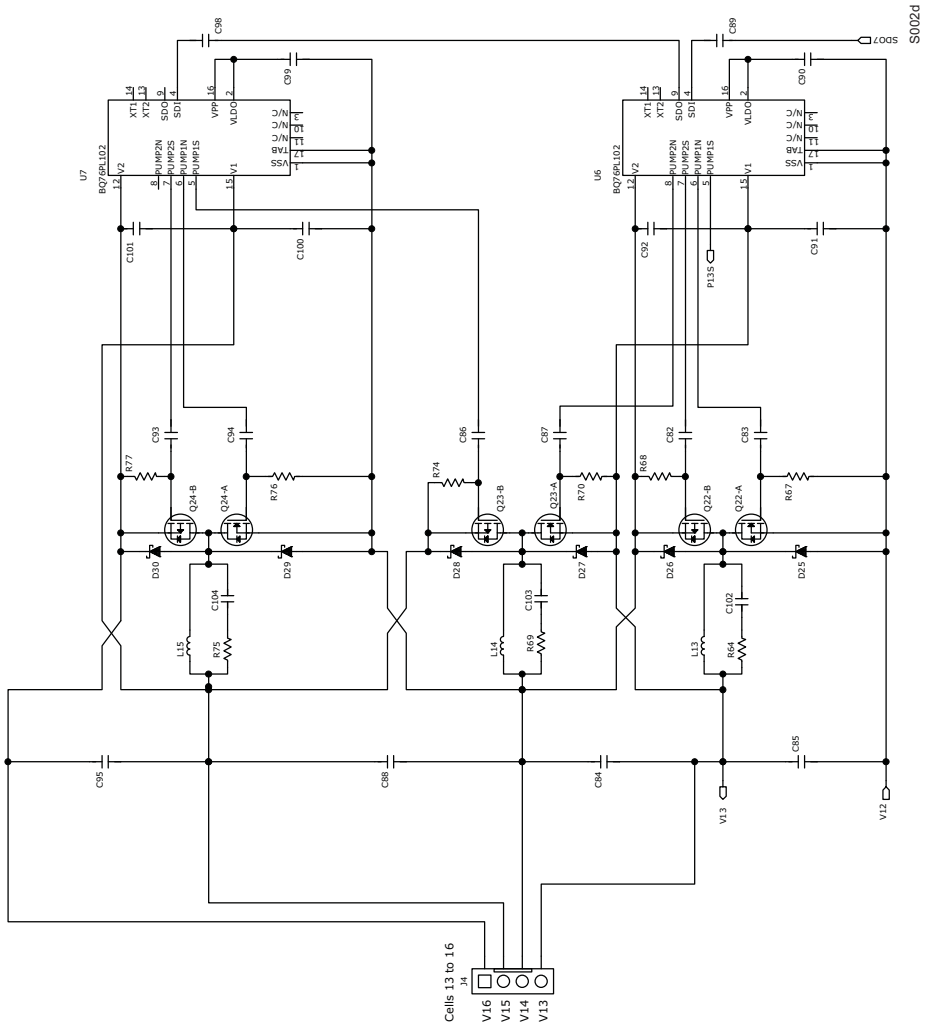


Figure 9. Typical 16S Application Circuit – bq76PL102 for Cells 13–16 (Sheet 4 of 4)

Table 3. Bill of Materials for 16S Application

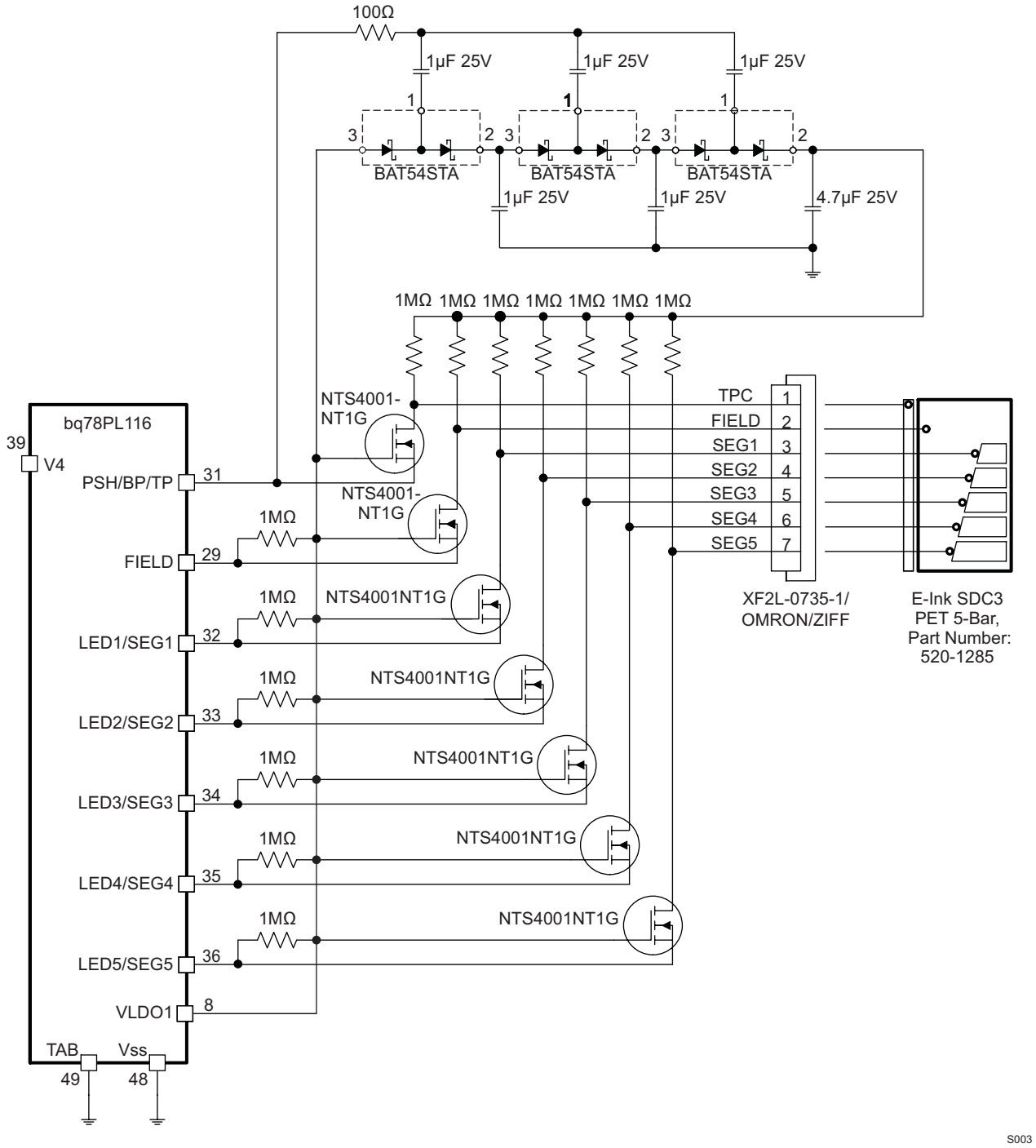
Qty	Reference	Value	Description	Size	Manufacturer	Mfg Part No.
6	U2-7	QFN-16	PowerLAN Dual Cell Monitor	QFN16	Texas Instruments	bq76PL102RGTT
1	U1	QFN-48	PowerLAN Master Gateway Battery Management Controller	QFN48	Texas Instruments	bq78PL116RGZR
24	C11 C18 C20 C23-24 C26 C48-50 C56-58 C69 C72 C74-77 C90-92 C99-101	10uF	Capacitor SMT Ceramic X5R +/-10% 6.3V	603	Standard	Standard
16	C1-3 C30 C32 C35 C39 C63-64 C78-81 C102-104	0.01uF	Capacitor SMT Ceramic X7R +/-10% 25V	603	Standard	Standard
12	C8-9 C14-15 C25 C46 C55 C68 C73 C89 C96 C98	1000pF	Capacitor SMT Ceramic X7R +/-10% 50V	603	Standard	Standard
5	C10 C12-13 C16 C22	0.1uF	Capacitor SMT Ceramic X7R +/-10% 50V	603	Standard	Standard

Table 3. Bill of Materials for 16S Application (continued)

Qty	Reference	Value	Description	Size	Manufacturer	Mfg Part No.
30	C7 C17 C19 C21 C27-29 C31 C34 C36 C40-41 C43-44 C51-53 C59-60 C62 C65 C67 C70-71 C82-83 C86-87 C93-94	3300pF	Capacitor SMT Ceramic X7R +/-10% 50V	603	Standard	Standard
16	C4-6 C33 C37-38 C42 C45 C47 C54 C61 C66 C84-85 C88 C95	22uF	Capacitor Ceramic SMT Y5V +/-20% 10V	805	Standard	Standard
24	R3 R6 R12-14 R20 R22 R30-33 R39 R42 R45 R48 R51 R53 R58 R61 R64-65 R69 R72 R75	100	Resistor SMT 1/10W +/-5%	603	Standard	Standard
2	R4 R34	10K	Resistor SMT 1/10W +/-5%	603	Standard	Standard
2	R26 R35	100K	Resistor SMT 1/10W +/-5%	603	Standard	Standard
12	R1 R7-8 R11 R15 R19 R23 R25 R28 R36- 38	1.0M	Resistor SMT 1/10W +/-5%	603	Standard	Standard
30	R5 R10 R21 R24 R40-41 R43-44 R46-47 R49-50 R52 R54-57 R59-60 R62-63 R66- 68 R70-71 R73-74 R76-77	20K	Resistor SMT 1/10W +/-5%	603	Standard	Standard
2	R2 R16	200K	Resistor SMT 1/10W +/-5%	603	Standard	Standard
2	R17-18	30K	Resistor SMT 1/10W +/-5%	603	Standard	Standard
1	R9	3K	Resistor SMT +/-5% 1W	603	Standard	Standard
2	R27 R29	4.7K	Resistor SMT 1/10W +/-5%	603	Standard	Standard
1	RSENSE	0.01	Resistor SMT +/-1% 1W +/-100ppm/°C	2512	Standard	Standard
15	L1-15	4.7uH	Inductor SMD Shielded Isat=2.0A	4.9mm x 4.9mm x 2.0mm	Taiyo Yuden	NRS5020T4R7MMGJ
4	Q1-4	Vds > 80V	N-Channel MOSFET, 2.5Vgs Rated	SOT-23	Standard	Standard
2	Q5-6	Idss=0.2 to 1.0mA	General Purpose N-Channel JFET Amplifier	SOT-23	Fairchild	MMBFJ201
1	Q7	100 Vds	MOSFET N-Channel 20Vgs	D2PAK	Standard	Standard
15	Q8-10 Q13-24	+/-8Vgs	MOSFET N/P Complementary Pair	6-TSOP	Alpha & Omega	AO6604
2	Q11-12	-100 Vds	MOSFET P-Channel 20Vgs	D2PAK	Standard	Standard
30	D1-30	500mA	Schottky Rectifier Diode 20V	SOD-123	Fairchild	MBR0520L
4	T1-4		Dual Diode	SOT-23	Fairchild	MMBD4148SE
5	LED1-5	Green/25 mA	Green Diffused LED 1.6mm x 0.8mm SMT	603	Standard	Standard

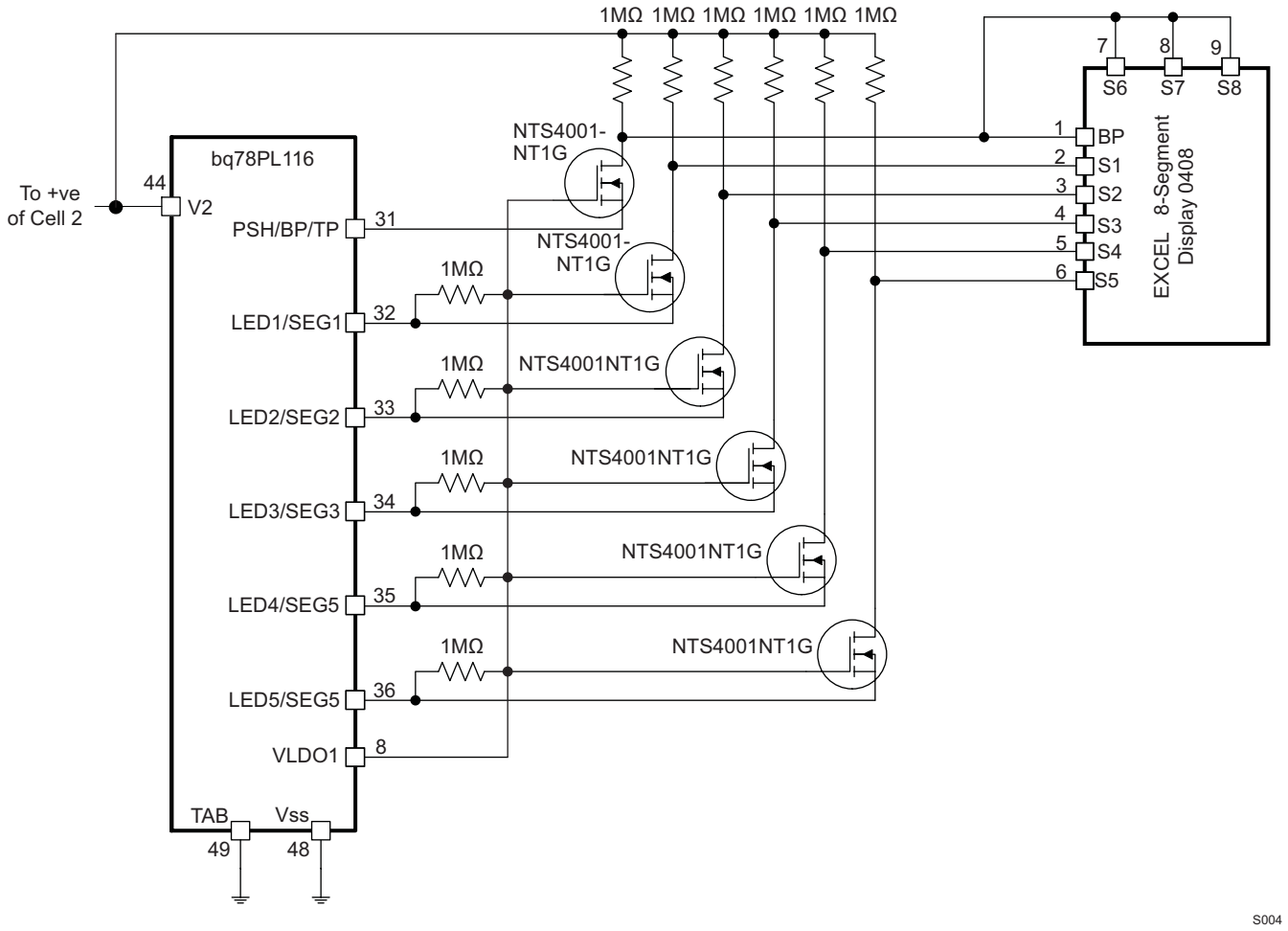
Table 3. Bill of Materials for 16S Application (continued)

Qty	Reference	Value	Description	Size	Manufacturer	Mfg Part No.
2	Z1 Z2	5.6VDC	Common Anode Zener Diode Pair 300mW	SOT-23	Standard	Standard
3	Z3-5	500mW	Zener Diode 500mW 12V	SOD-123	Standard	Standard
1	SOCI	50mA	Tactile Momentary Pushbutton Thru-Hole		Standard	Standard
1	HOST		Header	6 Position	Standard	Standard
1	J1	1.0 Amp	Header	5 Position	Standard	Standard
3	J2-4	3.0A	Header	4 Position	Standard	Standard
4	BATTERY+ BATTERY- PACK+ PACK-	30 Amps	Header	2 Position	Standard	Standard



NOTE: For reference only. Actual display used may require different operating voltage. Consult with display vendor.

Figure 10. Reference Schematic (Electronic-Paper Display Connections)



NOTE: For reference only. Actual display used may require different operating voltage. Consult with display vendor.

Figure 11. Reference Schematic (LCD Connections)

REVISION HISTORY

Changes from Revision A (October 2010) to Revision B **Page**

- Revised PowerLAN Characteristics table 9
- Changed Ah values in Current Measurement paragraph 16

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ78PL116RGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	78PL116 BQ	Samples
BQ78PL116RGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	78PL116 BQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

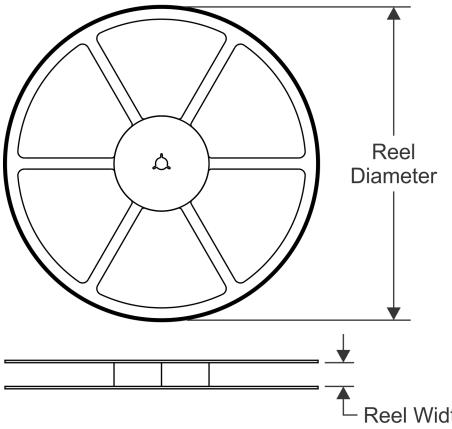
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

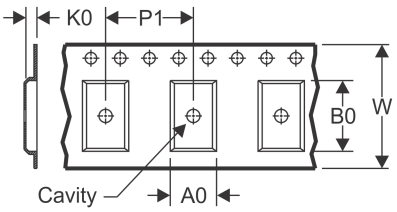
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

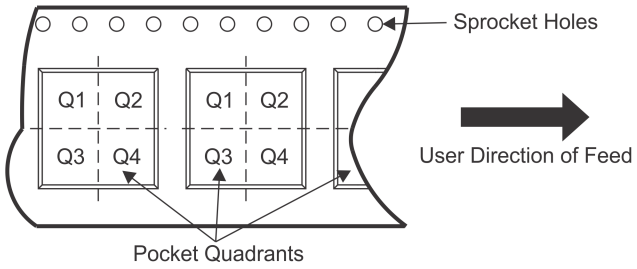


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

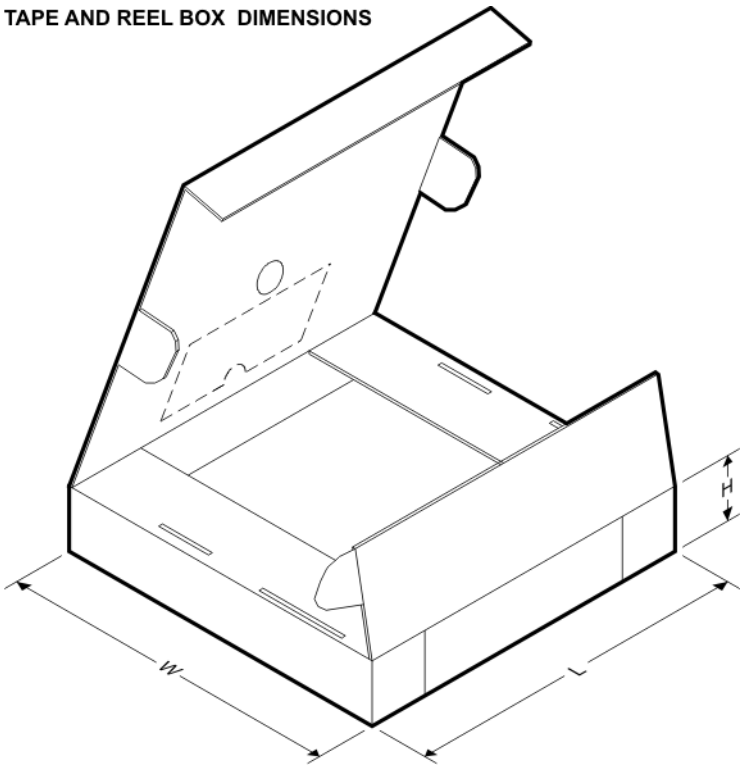
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ78PL116RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
BQ78PL116RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ78PL116RGZR	VQFN	RGZ	48	2500	853.0	449.0	35.0
BQ78PL116RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0

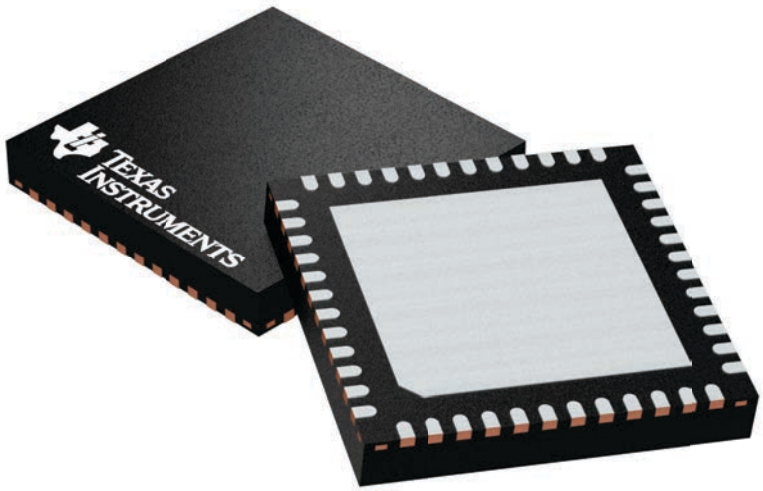
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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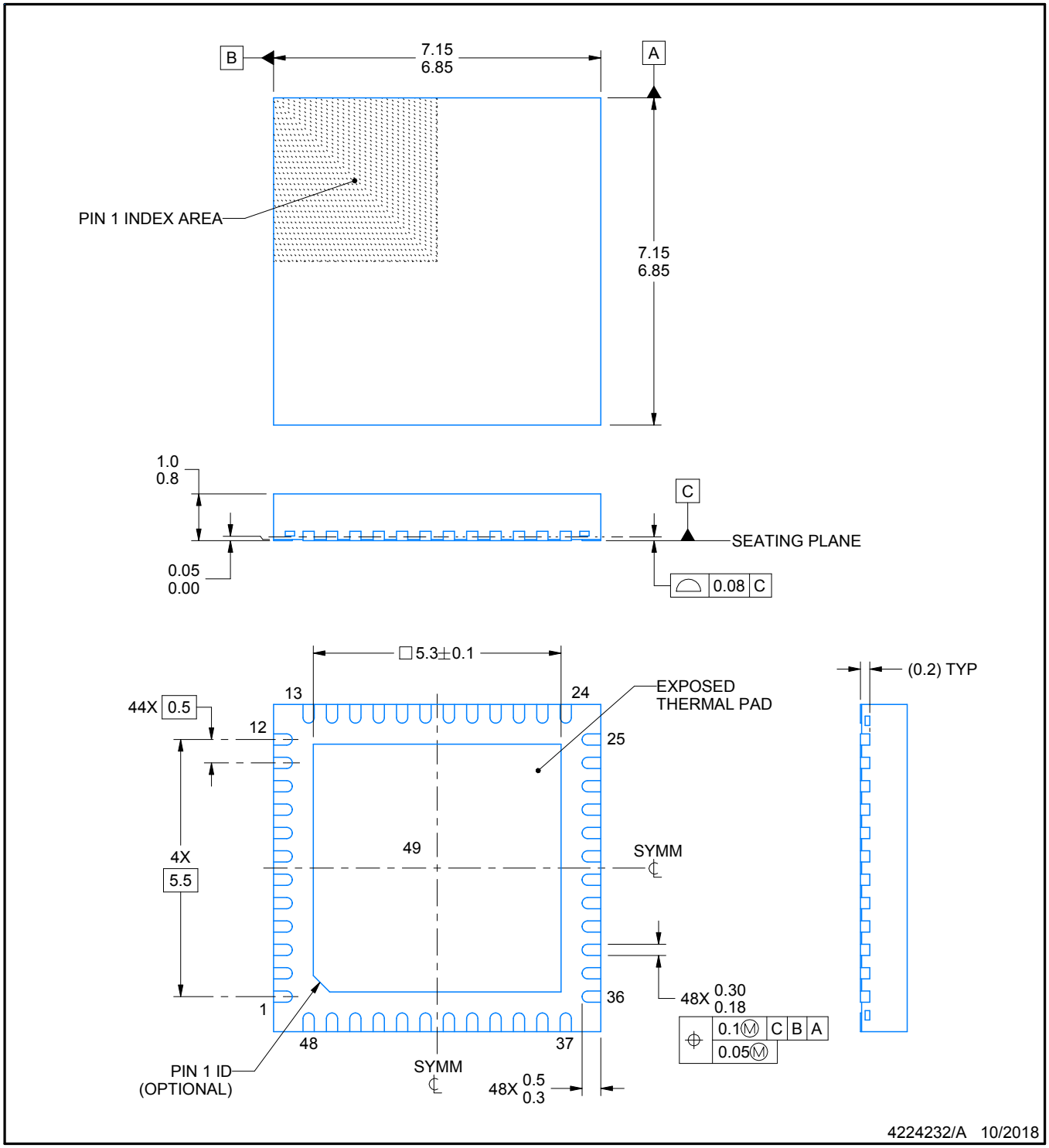
RGZ0048H

PACKAGE OUTLINE

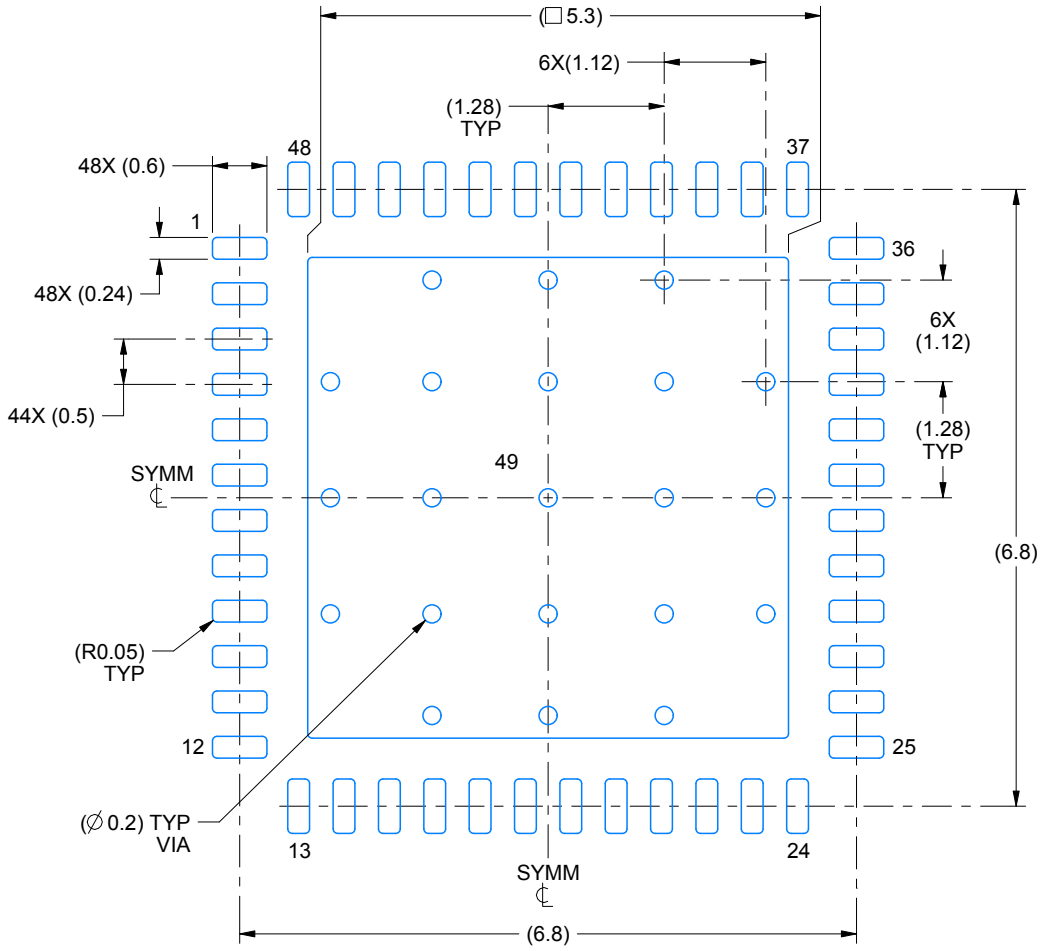
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

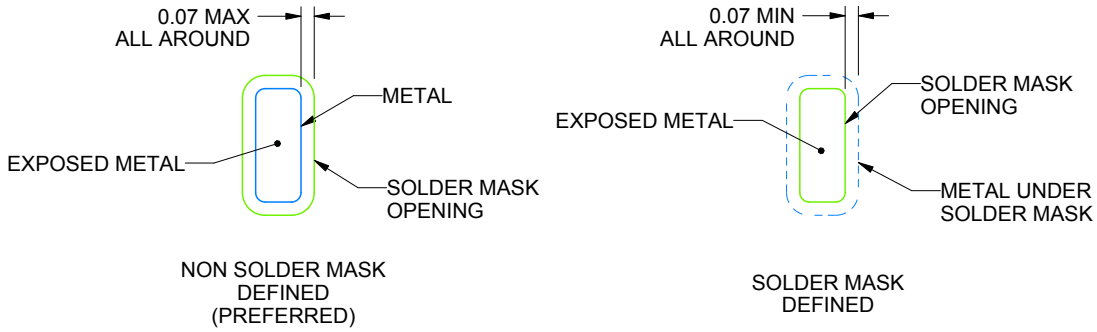


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

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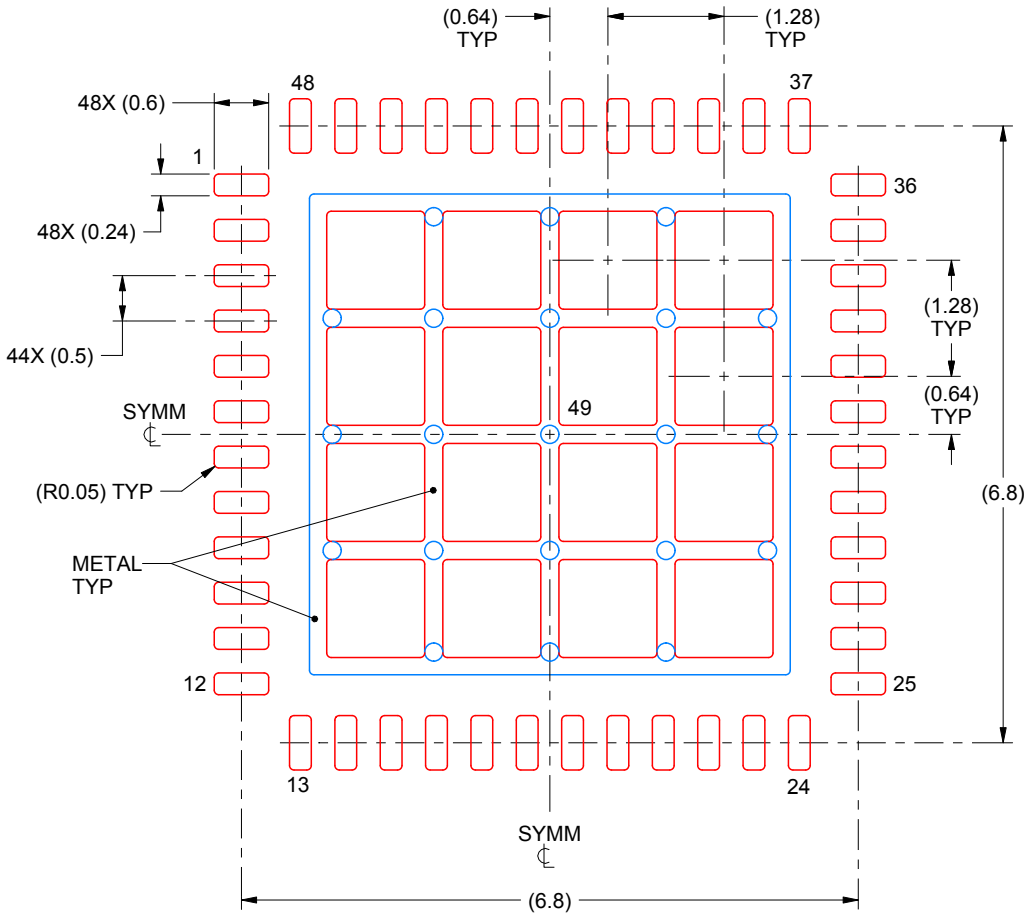
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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