CD4066B CMOS 四路双向开关

1 特性

- 15V 数字或 ±7.5V 峰峰值开关
- 工作电压为 15V 时典型导通状态电阻为 125Ω
- 在 15V 信号输入范围内匹配的开关导通电阻不超过 5Ω
- 在整个峰峰值信号范围内具有平缓的导通状态电阻
- 高开关输出电压比：f_{is} = 10kHz、R_L = 1kΩ 时典型值为 80dB
- 高度线性：f_{is} = 1kHz、V_{is} = $5V_{p-p}$、$V_{DD} – V_{SS}$ ≥ 10V、R_L = 10kΩ 时失真典型值小于 0.5%
- 极低的关闭状态开关泄漏，从而产生极低的失调电流和高有效关闭状态电阻：$V_{DD} – V_{SS}$ = 10V、T_A = 25°C 时典型值为 10pA
- 极高的控制输入阻抗（控制电路与信号电路相隔离）：典型值为 10^{12}Ω
- 低开关间串扰：f_{is} = 8MHz、R_L = 1kΩ 时典型值为 –50dB
- 匹配的控制输入到信号输出电容：可减少输出信号瞬态
- 频率响应，开启 = 40MHz（典型值）
- 针对 20V 下的静态电流进行了 100% 测试
- 5V、10V 和 15V 参数额定值

2 应用

- 模拟信号开关和多路复用：信号门控、调制器、静噪控制、解调器、斩波器、换向开关
- 数字信号开关和多路复用
- 传输门逻辑实施
- 模数转换和数模转换
- 频率、阻抗、相位和模拟信号增益的数字控制
- 楼宇自动化

3 说明

CD4066B 器件是一款用于模拟或数字信号传输或多路复用的四路双向开关。该器件与 CD4016B 器件引脚对引脚兼容，但导通状态电阻低得多。此外，导通状态电阻在整个信号输入范围内相对恒定。

CD4066B 器件包含四个双向开关，每个开关都具有独立的控件。控制信号同时偏置打开或关闭给定开关中的 p 和 n 器件。如图 17 所示，每个开关上 n 沟道器件的阱都与输入（当开关打开时）或 V_{SS}（当开关关闭时）相连。该配置使开关晶体管阈值电压不再随输入信号的变化而变化，从而使导通状态电阻在整个工作信号范围内都很低。

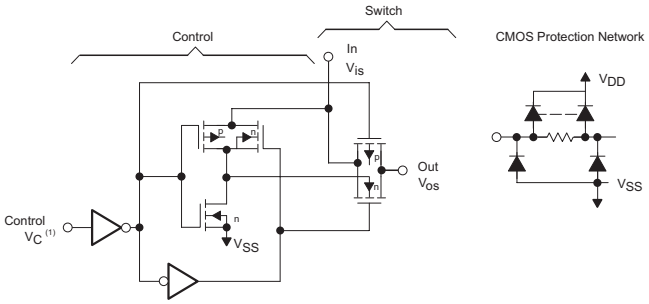
与单通道开关相比，优点包括峰值输入信号电压摆幅等于最大电源电压以及在输入信号范围内具有更恒定的导通状态阻抗。不过，对于采样保持 应用，建议使用 CD4016B 器件。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
CD4066B	PDIP (14)	19.30mm x 6.35mm
	CDIP (14)	19.50mm × 6.92mm
	SOIC (14)	8.65mm × 3.91mm
	SOP (14)	10.30mm × 5.30mm
	TSSOP (14)	5.00mm x 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

通过数字控制逻辑进行双向信号传输



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目录

1 特性 ... 1
2 应用 ... 1
3 说明 ... 1
4 修订历史记录 ... 2
5 **Pin Configuration and Functions** ... 3
6 **Specifications** ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Switching Characteristics ... 8
6.7 Typical Characteristics ... 9
7 **Parameter Measurement Information** ... 10
8 **Detailed Description** ... 14
8.1 Overview ... 14
8.2 Functional Block Diagram ... 14
8.3 Feature Description ... 14
8.4 Device Functional Modes ... 14
9 **Application and Implementation** ... 15
9.1 Application Information ... 15
9.2 Typical Application ... 15
10 **Power Supply Recommendations** ... 17
11 **Layout** ... 17
11.1 Layout Guidelines ... 17
11.2 Layout Example ... 17
12 器件和文档支持 ... 18
12.1 接收文档更新通知 ... 18
12.2 社区资源 ... 18
12.3 商标 ... 18
12.4 静电放电警告 ... 18
12.5 Glossary ... 18
13 机械、封装和可订购信息 ... 18

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision G (June 2017) to Revision H — **Page**

- Added Junction Temperature details to the *Absolute Maximum Ratings* table ... 4

Changes from Revision F (March 2017) to Revision G — **Page**

- Changed From: V_{SS} To: Hi-Z in the SIG OUT/IN column of ... 14

Changes from Revision E (September 2016) to Revision F — **Page**

- Corrected the r_{on} V_{DD} = 10 V values in the *Electrical Characteristics* table. ... 7
- Corrected the y axis scale in Figure 6 ... 9

Changes from Revision D (September 2003) to Revision E — **Page**

- 已添加 添加了 *ESD 额定值* 表、*特性 说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 ... 1
- 已删除 删除了*订购信息* 表，请参阅数据表末尾的 POA ... 1
- Changed values in the *Thermal Information* table to align with JEDEC standards ... 4

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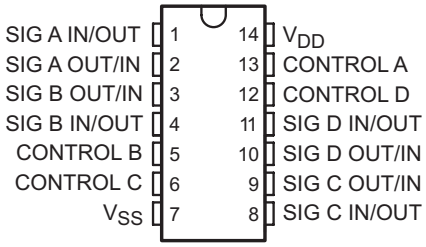
5 Pin Configuration and Functions

N, J, D, NS, or PW Packages
14-Pin PDIP, CDIP, SOIC, SO, or TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SIG A IN/OUT	I/O	Input/Output for Switch A
2	SIG A OUT/IN	I/O	Output/Input for Switch A
3	SIG B OUT/IN	I/O	Output/Input for Switch B
4	SIG B IN/OUT	I/O	Input/Output for Switch B
5	CONTROL B	I	Control pin for Switch B
6	CONTROL C	I	Control pin for Switch C
7	V_{SS}	—	Low Voltage Power Pin
8	SIG C IN/OUT	I/O	Input/Output for Switch C
9	SIG C OUT/IN	I/O	Output/Input for Switch C
10	SIG D OUT/IN	I/O	Output/Input for Switch D
11	SIG D IN/OUT	I/O	Input/Output for Switch D
12	CONTROL D	I	Control Pin for D
13	CONTROL A	I	Control Pin for A
14	V_{DD}	—	Power Pin

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{DD}	DC supply-voltage	Voltages referenced to V_{SS} pin	–0.5	20	V
V_{is}	Input voltage	All inputs	–0.5	V_{DD} + 0.5	V
I_{IN}	DC input current	Any one input		±10	mA
T_{JMAX1}	Maximum junction temperature, ceramic package			175	°C
T_{JMAX2}	Maximum junction temperature, plastic package			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	3	18	V
T_A	Operating free-air temperature	–55	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		CD4066B				UNIT
		N (PDIP)	D (SOIC)	NS (SO)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.7	89.5	88.2	119.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.0	49.7	46.1	48.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.6	43.8	47.0	61.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	25.8	17.4	16.3	5.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.5	43.5	46.6	60.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{os}	Switch output voltage	V_{DD} = 5 V V_{is} = 0 V				0.4	V
		V_{DD} = 5 V V_{is} = 5 V		4.6			V
		V_{DD} = 10 V V_{is} = 0 V				0.5	V
		V_{DD} = 10 V V_{is} = 10 V		9.5			V
		V_{DD} = 15 V V_{is} = 0 V				1.5	V
		V_{DD} = 15 V V_{is} = 15 V		13.5			V
Δr_{on}	On-state resistance difference between any two switches	R_L = 10 kΩ, V_C = V_{DD}	V_{DD} = 5 V		15		Ω
			V_{DD} = 10 V		10		
			V_{DD} = 15 V		5		
THD	Total harmonic distortion	V_C = V_{DD} = 5 V, V_{SS} = –5 V, $V_{is(p-p)}$ = 5 V (sine wave centered on 0 V), R_L = 10 kΩ, f_{is} = 1-kHz sine wave			0.4%		
	–3-dB cutoff frequency (switch on)	V_C = V_{DD} = 5 V, V_{SS} = –5 V, $V_{is(p-p)}$ = 5 V (sine wave centered on 0 V), R_L = 1 kΩ			40		MHz
	–50-dB feedthrough frequency (switch off)	V_C = V_{SS} = –5 V, $V_{is(p-p)}$ = 5 V (sine wave centered on 0 V), R_L = 1 kΩ			1		MHz
	–50-dB crosstalk frequency	V_C(A) = V_{DD} = 5 V, V_C(B) = V_{SS} = –5 V, V_{is}(A) = 5 V_{p-p}, 50-Ω source, R_L = 1 kΩ			8		MHz
C_{is}	Input capacitance	V_{DD} = 5 V, V_C = V_{SS} = –5 V			8		pF
C_{os}	Output capacitance	V_{DD} = 5 V, V_C = V_{SS} = –5 V			8		pF
C_{ios}	Feedthrough	V_{DD} = 5 V, V_C = V_{SS} = –5 V			0.5		pF
V_{IHC}	Control input, high voltage	See Figure 7	V_{DD} = 5 V	3.5			V
			V_{DD} = 10 V	7			
			V_{DD} = 15 V	11			
	Crosstalk (control input to signal output)	V_C = 10 V (square wave), t_r, t_f = 20 ns, R_L = 10 kΩ V_{DD} = 10 V			50		mV
	Turnon and turnoff propagation delay	V_{IN} = V_{DD}, t_r, t_f = 20 ns, C_L = 50 pF, R_L = 1 kΩ	V_{DD} = 5 V		35	70	ns
			V_{DD} = 10 V		20	40	
			V_{DD} = 15 V		15	30	
	Maximum control input repetition rate	V_{is} = V_{DD}, V_{SS} = GND, R_L = 1 kΩ to GND, C_L = 50 pF, V_C = 10 V (square wave centered on 5 V), t_r, t_f = 20 ns, V_{os} = 1/2 V_{os} at 1 kHz	V_{DD} = 5 V		6		MHz
			V_{DD} = 10 V		9		
			V_{DD} = 15 V		9.5		
C_I	Input capacitance				5	7.5	pF

Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{is}	Switch input current	V_{DD} = 5 V, V_{is} = 0 V	T_A = –55°C			0.64	mA
			T_A = –40°C			0.61	
			T_A = 25°C		0.51		
			T_A = 85°C			0.42	
			T_A = 125°C			0.36	
		V_{DD} = 5 V, V_{is} = 5 V	T_A = –55°C			–0.64	mA
			T_A = –40°C			–0.61	
			T_A = 25°C		–0.51		
			T_A = 85°C			–0.42	
			T_A = 125°C			–0.36	
		V_{DD} = 10 V, V_{is} = 0 V	T_A = –55°C			1.6	mA
			T_A = –40°C			1.5	
			T_A = 25°C		1.3		
			T_A = 85°C			1.1	
			T_A = 125°C			0.9	
		V_{DD} = 10 V, V_{is} = 10 V	T_A = –55°C			–1.6	mA
			T_A = –40°C			–1.5	
			T_A = 25°C		–1.3		
			T_A = 85°C			–1.1	
			T_A = 125°C			–0.9	
		V_{DD} = 15 V, V_{is} = 0 V	T_A = –55°C			4.2	mA
			T_A = –40°C			4	
			T_A = 25°C		3.4		
			T_A = 85°C			2.8	
			T_A = 125°C			2.4	
		V_{DD} = 15 V, V_{is} = 15 V	T_A = –55°C			–4.2	mA
			T_A = –40°C			–4	
			T_A = 25°C		–3.4		
			T_A = 85°C			–2.8	
			T_A = 125°C			–2.4	

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Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{DD}	Quiescent device current	V_{IN} = 0 to 5 V, V_{DD} = 5 V	T_A = –55°C				0.25	µA
			T_A = –40°C				0.25	
			T_A = 25°C			0.01	0.25	
			T_A = 85°C				7.5	
			T_A = 125°C				7.5	
		V_{IN} = 0 to 10 V, V_{DD} = 10 V	T_A = –55°C				0.5	µA
			T_A = –40°C				0.5	
			T_A = 25°C			0.01	0.5	
			T_A = 85°C				15	
			T_A = 125°C				15	
		V_{IN} = 0 to 15 V, V_{DD} = 15 V	T_A = –55°C				1	µA
			T_A = –40°C				1	
			T_A = 25°C			0.01	1	
			T_A = 85°C				30	
			T_A = 125°C				30	
		V_{IN} = 0 to 20 V, V_{DD} = 20 V	T_A = –55°C				5	µA
			T_A = –40°C				5	
			T_A = 25°C			0.02	5	
			T_A = 85°C				150	
			T_A = 125°C				150	
r_{on}	On-state resistance (max)	to $V_C = \frac{(V_{DD} - V_{SS})}{2}$, R_L = 10 kΩ returned $V_{is} = V_{SS}$ to V_{DD}	V_{DD} = 5 V	T_A = –55°C			800	Ω
				T_A = –40°C			850	
				T_A = 25°C		470	1050	
				T_A = 85°C			1200	
				T_A = 125°C			1300	
			V_{DD} = 10 V	T_A = –55°C			310	
				T_A = –40°C			330	
				T_A = 25°C		180	400	
				T_A = 85°C			500	
				T_A = 125°C			500	
			V_{DD} = 15 V	T_A = –55°C			200	
				T_A = –40°C			210	
				T_A = 25°C		125	240	
				T_A = 85°C			300	
				T_A = 125°C			320	

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Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{ILC}	Control input, low voltage (max)	$\|I_{is}\| < 10\ \mu A$, $V_{is} = V_{SS}$, $V_{OS} = V_{DD}$, and $V_{is} = V_{DD}$, $V_{OS} = V_{SS}$	$V_{DD} = 5\ V$	$T_A = -55°C$		1		V
				$T_A = -40°C$		1		
				$T_A = 25°C$		1		
				$T_A = 85°C$		1		
				$T_A = 125°C$		1		
			$V_{DD} = 10\ V$	$T_A = -55°C$		2		
				$T_A = -40°C$		2		
				$T_A = 25°C$		2		
				$T_A = 85°C$		2		
				$T_A = 125°C$		2		
			$V_{DD} = 15\ V$	$T_A = -55°C$		2		
				$T_A = -40°C$		2		
				$T_A = 25°C$		2		
				$T_A = 85°C$		2		
				$T_A = 125°C$		2		
I_{IN}	Input current (max)	$V_{is} \le V_{DD}$, $V_{DD} - V_{SS} = 18\ V$, $V_{CC} \le V_{DD} - V_{SS}$ $V_{DD} = 18\ V$	$T_A = -55°C$				±0.1	µA
			$T_A = -40°C$				±0.1	
			$T_A = 25°C$			$\pm 10^{-5}$	±0.1	
			$T_A = 85°C$				±1	
			$T_A = 125°C$				±1	

6.6 Switching Characteristics

$T_A = 25°C$

PARAMETER	FROM	TO	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	Signal input	Signal output	$V_{IN} = V_{DD}$, t_r, $t_f = 20\ ns$, $C_L = 50\ pF$, $R_L = 1\ k\Omega$	5 V		20	40	ns
				10 V		10	20	
				15 V		7	15	
t_{plh}	Signal input	Signal output	$V_{IN} = V_{DD}$, t_r, $t_f = 20\ ns$, $C_L = 50\ pF$, $R_L = 1\ k\Omega$	5 V		35	70	ns
				10 V		20	40	
				15 V		15	30	
t_{phl}	Signal input	Signal output	$V_{IN} = V_{DD}$, t_r, $t_f = 20\ ns$, $C_L = 50\ pF$, $R_L = 1\ k\Omega$	5 V		35	70	ns
				10 V		20	40	
				15 V		15	30	

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6.7 Typical Characteristics

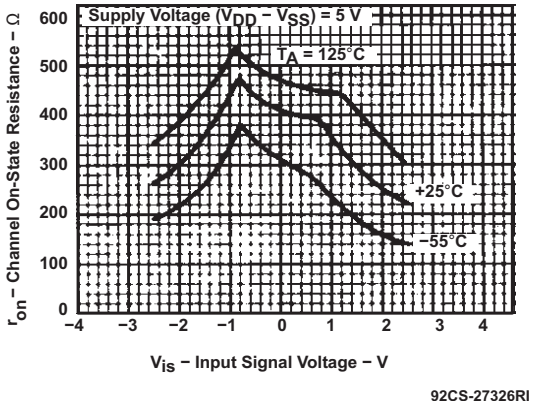

Figure 1. Typical ON-State Resistance vs Input Signal Voltage (All Types)

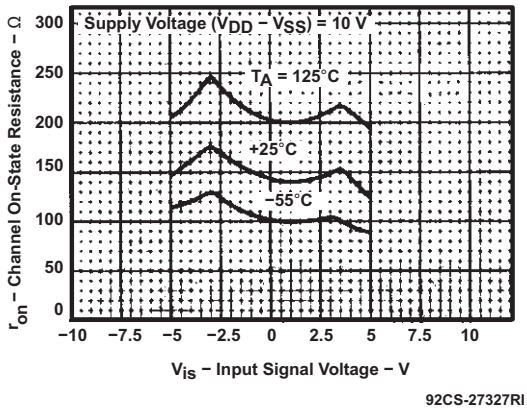

Figure 2. Typical ON-State Resistance vs Input Signal Voltage (All Types)

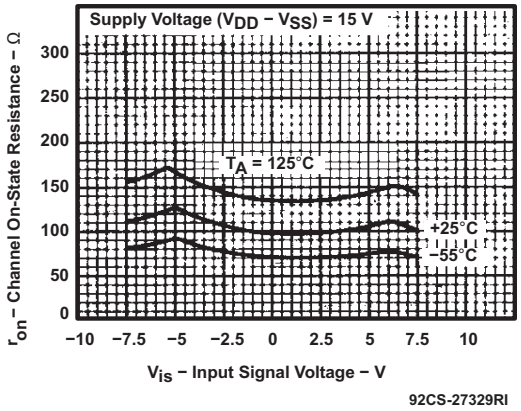

Figure 3. Typical ON-State Resistance vs Input Signal Voltage (All Types)

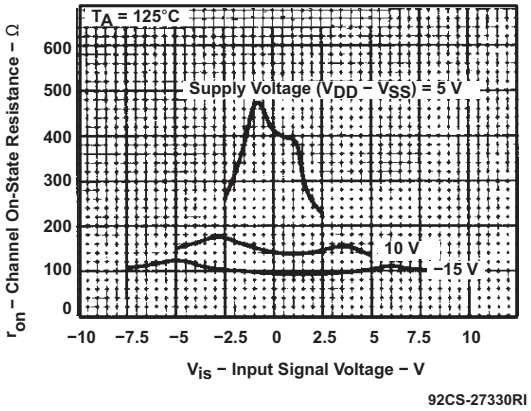

Figure 4. Typical ON-State Resistance vs Input Signal Voltage (All Types)

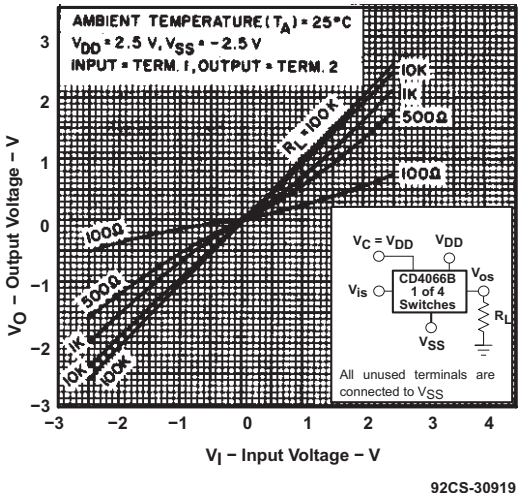

Figure 5. Typical ON Characteristics for 1 of 4 Channels

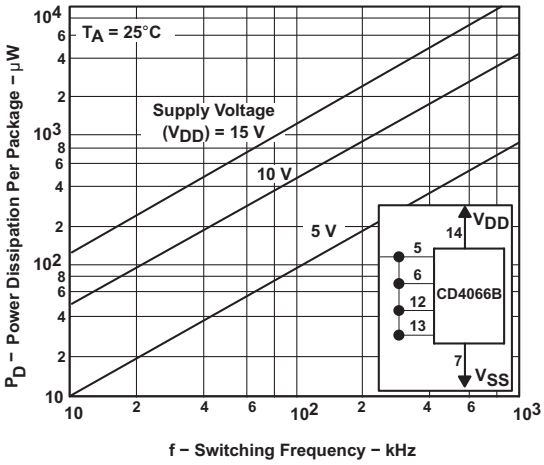

Figure 6. Power Dissipation per Package vs Switching Frequency

7 Parameter Measurement Information

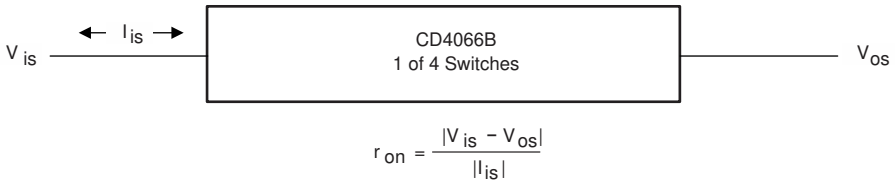

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Figure 7. Determination of r_{on} as a Test Condition for Control-Input High-Voltage (V_{IHC}) Specification

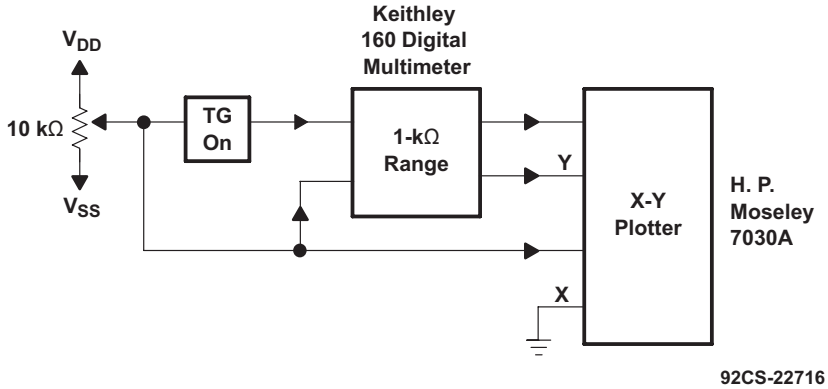
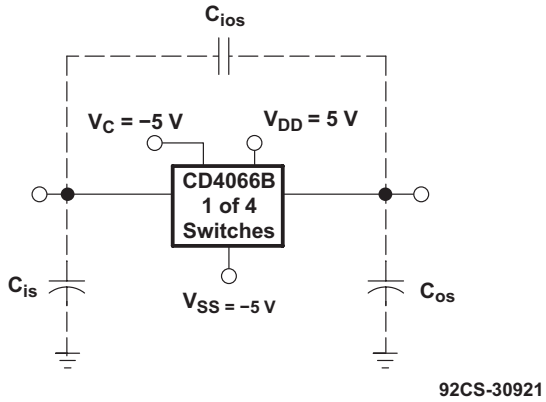


Figure 8. Channel On-State Resistance Measurement Circuit



Measured on Boonton capacitance bridge, model 75a (1 MHz);
test-fixture capacitance nulled out.

Figure 9. Typical On Characteristics for One of Four Channels

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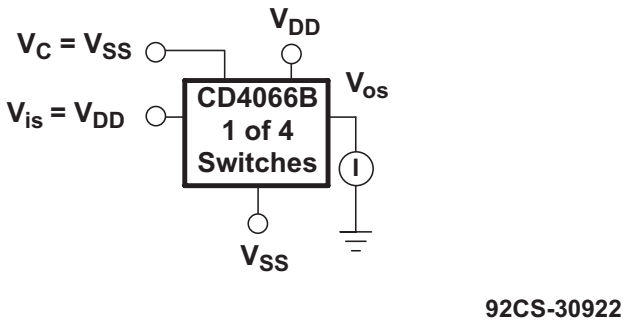
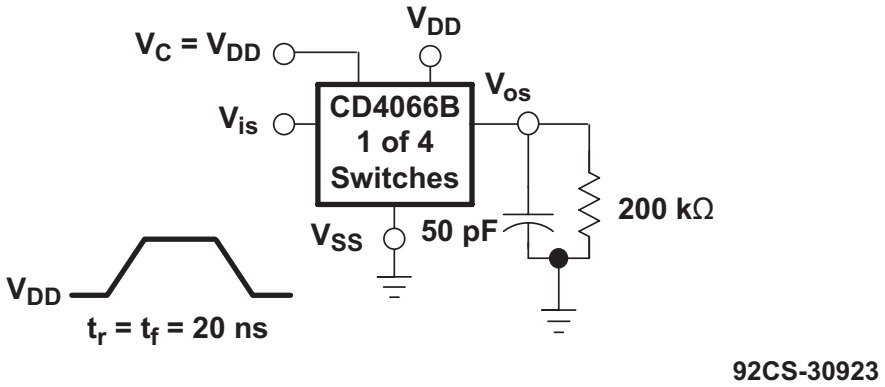
Parameter Measurement Information (continued)



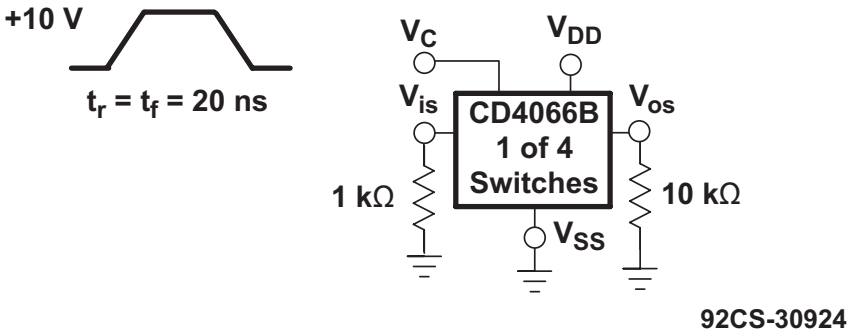
All unused terminals are connected to V_{SS}.

Figure 10. Off-Switch Input or Output Leakage



All unused terminals are connected to V_{SS}.

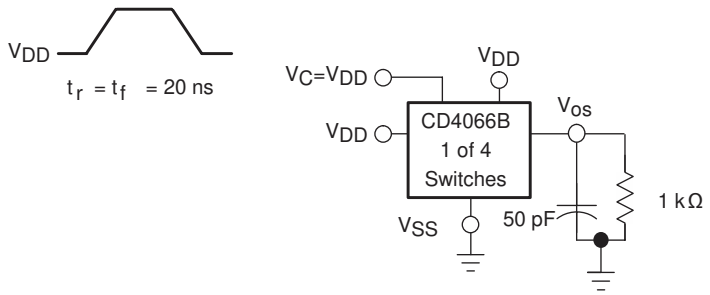
Figure 11. Propagation Delay Time Signal Input (V_{is}) to Signal Output (V_{os})



All unused terminals are connected to V_{SS}.

Figure 12. Crosstalk-Control Input to Signal Output

Parameter Measurement Information (continued)



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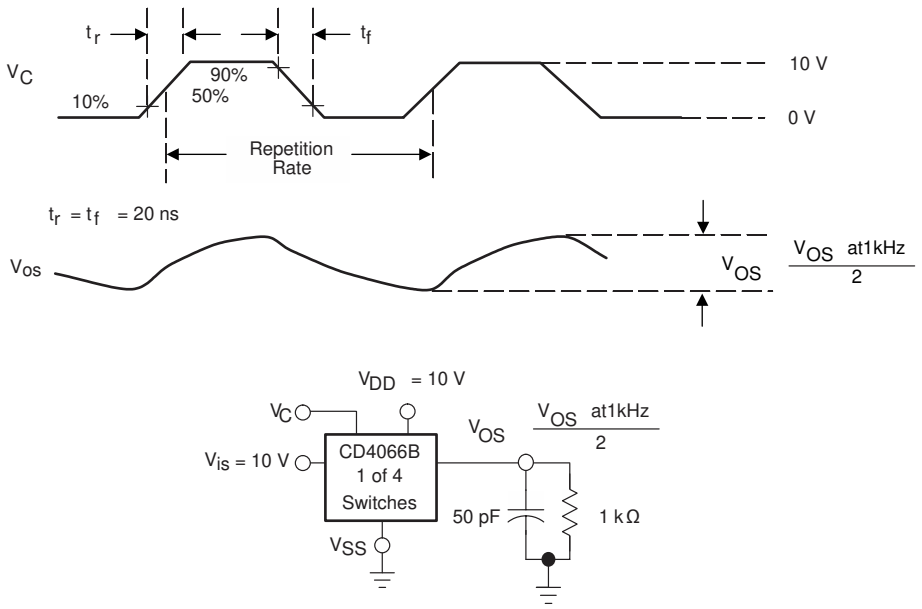
All unused pins are connected to V_{SS}.

Delay is measured at V_{os} level of +10% from ground (turn-on) or on-state output level (turn-off).

Figure 13. Propagation Delay, t_{PLH}, t_{PHL} Control-Signal Output



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All unused pins are connected to V_{SS}.

Figure 14. Maximum Allowable Control-Input Repetition Rate

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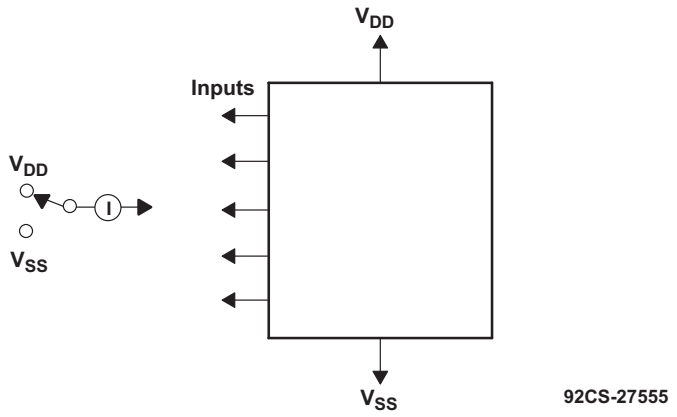
Parameter Measurement Information (continued)



Measure inputs sequentially to both V_{DD} and V_{SS}. Connect all unused inputs to either V_{DD} or V_{SS}. Measure control inputs only.

Figure 15. Input Leakage-Current Test Circuit

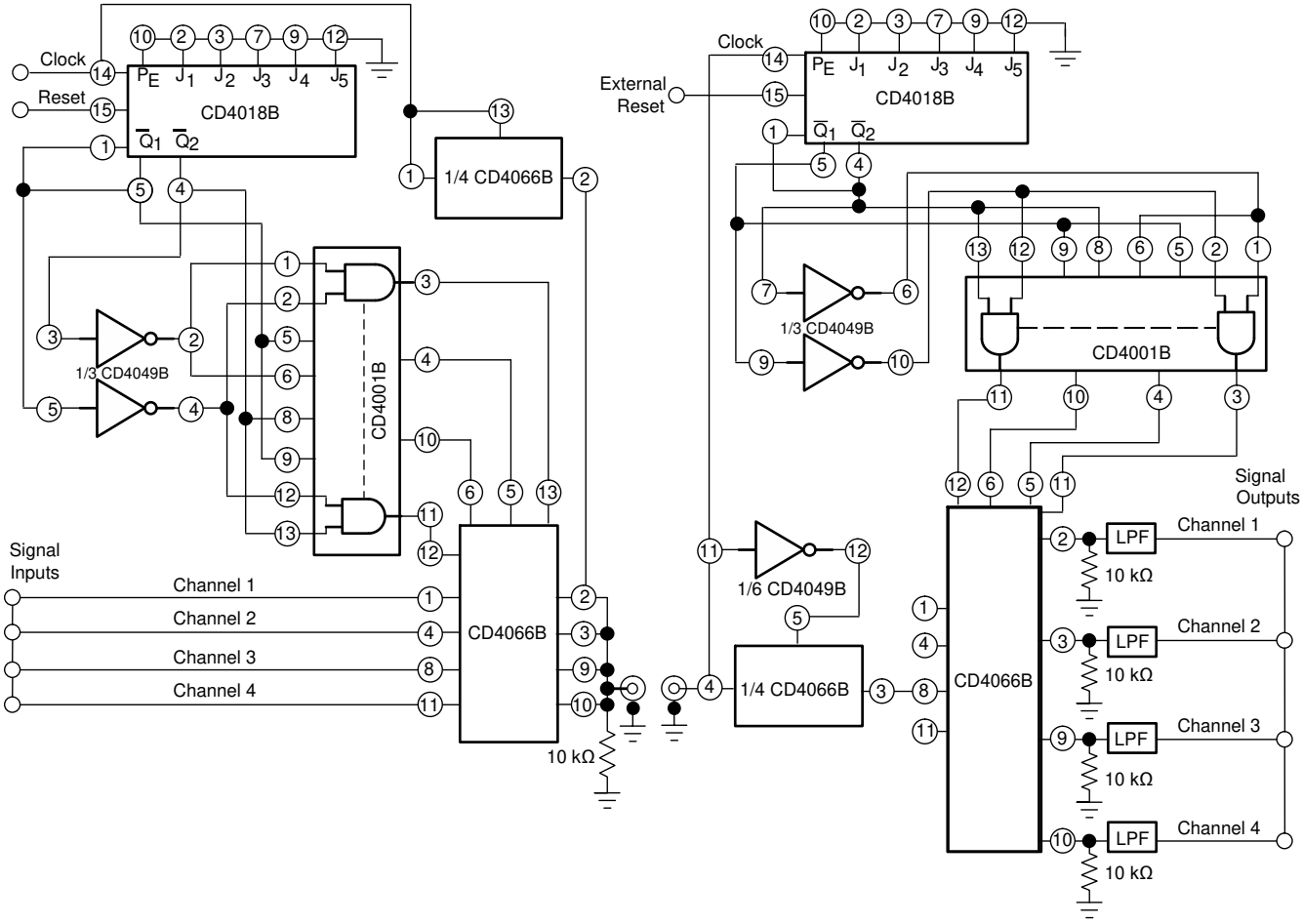


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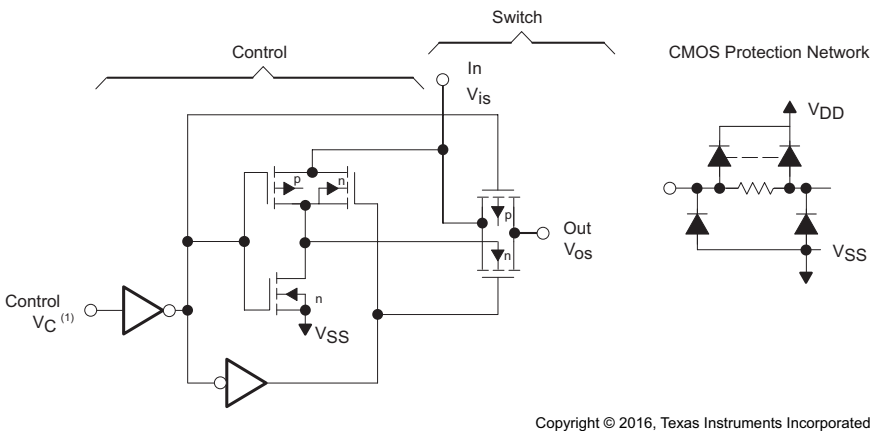
Figure 16. Four-Channel PAM Multiplex System Diagram

8 Detailed Description

8.1 Overview

CD4066B has four independent digitally controlled analog switches with a bias voltage of V_{SS} to allow for different voltage levels to be used for low output. Both the p and the n devices in a given switch are biased on or off simultaneously by the control signal. As shown in Figure 17, the well of the n-channel device on each switch is tied to either the input (when the switch is on) or to V_{SS} (when the switch is off). Thus, when the control of the device is low, the output of the switch goes to V_{SS} and when the control is high the output of the device goes to V_{DD}.

8.2 Functional Block Diagram



(1) All control inputs are protected by the CMOS protection network.

(2) All p substrates are connected to V_{DD}.

(3) Normal operation control-line biasing: switch on (logic 1), $V_C = V_{DD}$; switch off (logic 0), $V_C = V_{SS}$.

(4) Signal-level range: $V_{SS} \leq V_{is} \leq V_{DD}$.

Figure 17. Schematic Diagram of One-of-Four Identical Switches and Associated Control Circuitry

8.3 Feature Description

Each switch has different control pins, which allows for more options for the outputs. Bias Voltage allows the device to output a voltage other than 0 V when the device control is low. The CD4066B has a large absolute maximum voltage for V_{DD} of 20 V.

8.4 Device Functional Modes

Added Junction Temperature details to the *Absolute Maximum Ratings* table lists the functions of this device.

Table 1. Function Table

INPUTS		OUTPUT
SIG IN/OUT	CONTROL	SIG OUT/IN
H	H	H
L	H	L
X	L	Hi-Z

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

In applications that employ separate power sources to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the four CD4066B device bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the CD4066B device.

In certain applications, the external load-resistor current can include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into pins 1, 4, 8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8 V (calculated from r_{on} values shown).

No V_{DD} current flows through R_L if the switch current flows into pins 2, 3, 9, or 10.

9.2 Typical Application

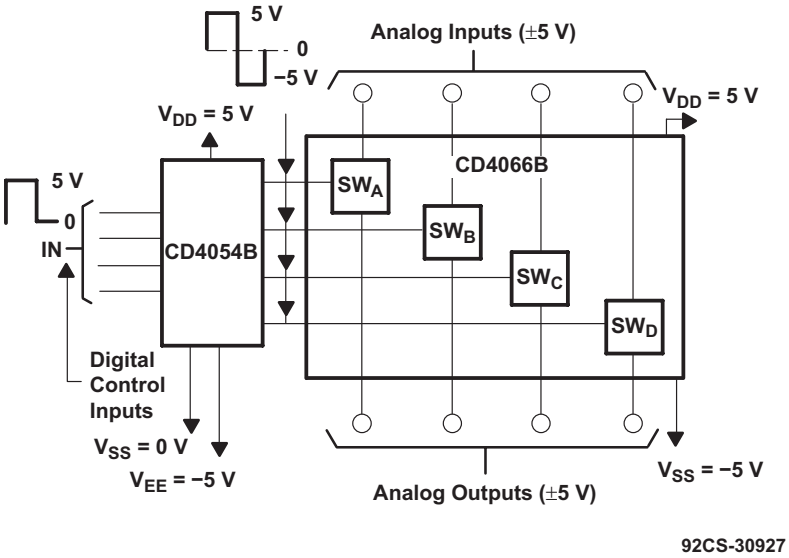

Figure 18. Bidirectional Signal Transmission Through Digital Control Logic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Avoid bus contention because it can drive currents in excess of maximum limits. The high drive also creates fast edges into light loads, so consider routing and load conditions to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   – For rise time and fall time specifications, see Δt/Δv in *Recommended Operating Conditions*.
   – For specified high and low levels, see V_{IH} and V_{IL} in *Recommended Operating Conditions*.
2. Recommended Output Conditions:
   – Load currents should not exceed ±10 mA.

Typical Application (continued)

9.2.3 Application Curve

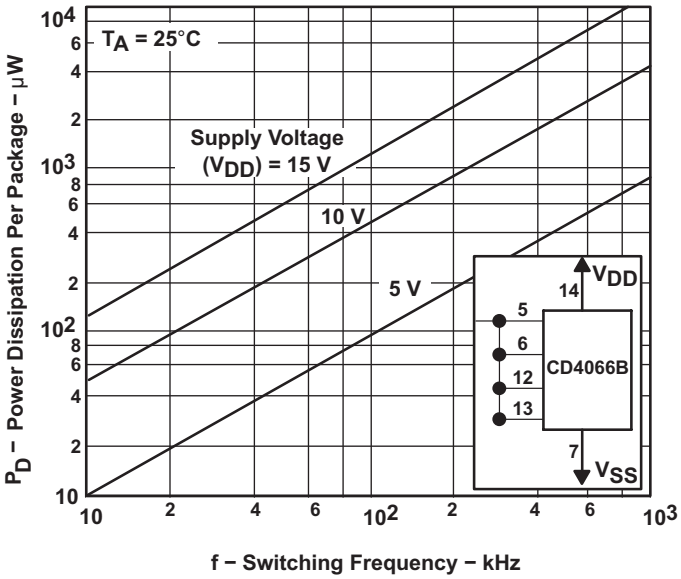

Figure 19. Power Dissipation vs. Switching Frequency

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10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in *Recommended Operating Conditions*.

Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1-µF is recommended; if there are multiple VCC pins, then 0.01-µF or 0.022-µF is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1-µF and a 1-µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs must never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input *and* gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or VCC, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted. This does not disable the input section of the I/Os, so they cannot float when disabled.

11.2 Layout Example

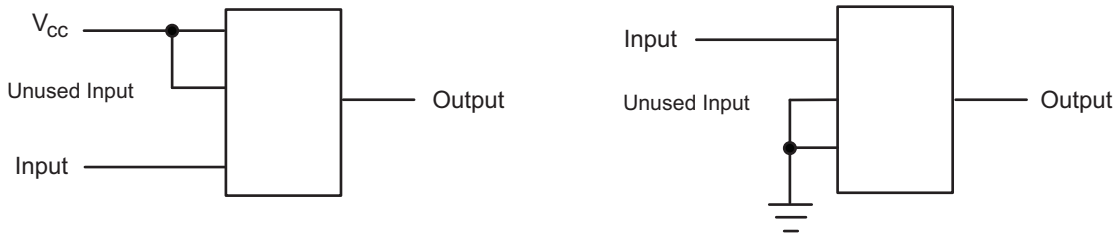

Figure 20. Diagram for Unused Inputs

12 器件和文档支持

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.3 商标

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12.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4066BE	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU | SN	N / A for Pkg Type	-55 to 125	CD4066BE	Samples
CD4066BEE4	ACTIVE	PDIP	N	14	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4066BE	Samples
CD4066BF	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD4066BF	Samples
CD4066BF3A	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD4066BF3A	Samples
CD4066BM	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4066BM	Samples
CD4066BM96	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	CD4066BM	Samples
CD4066BM96E4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4066BM	Samples
CD4066BM96G4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4066BM	Samples
CD4066BMT	ACTIVE	SOIC	D	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4066BM	Samples
CD4066BNS	ACTIVE	SO	NS	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		CD4066B	Samples
CD4066BNSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4066B	Samples
CD4066BPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM066B	Samples
CD4066BPWG4	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM066B	Samples
CD4066BPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	CM066B	Samples
CD4066BPWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM066B	Samples
JM38510/05852BCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 05852BCA	Samples
M38510/05852BCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 05852BCA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD4066B, CD4066B-MIL :

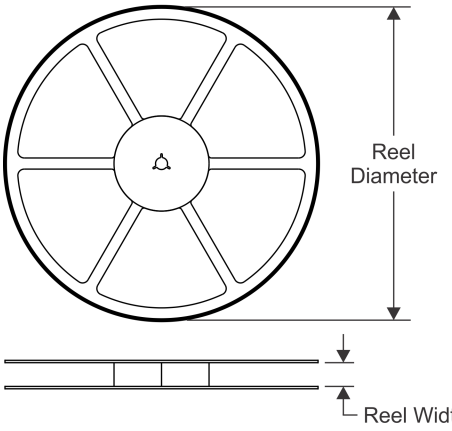
- Catalog : CD4066B
- Automotive : CD4066B-Q1, CD4066B-Q1
- Military : CD4066B-MIL

NOTE: Qualified Version Definitions:

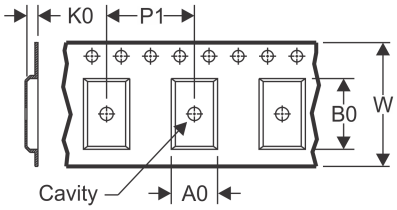
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

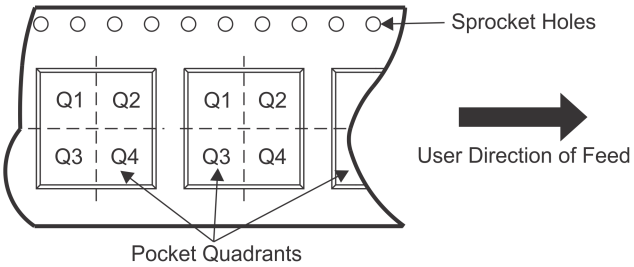


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

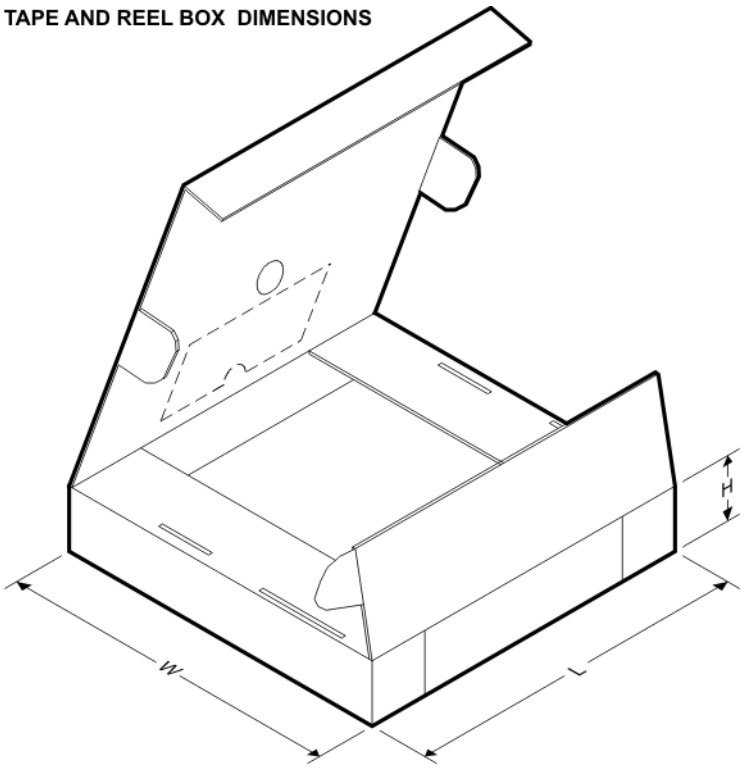
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4066BM96	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
CD4066BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4066BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4066BM96G4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4066BM96G4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4066BMT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4066BNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4066BPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4066BPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4066BPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

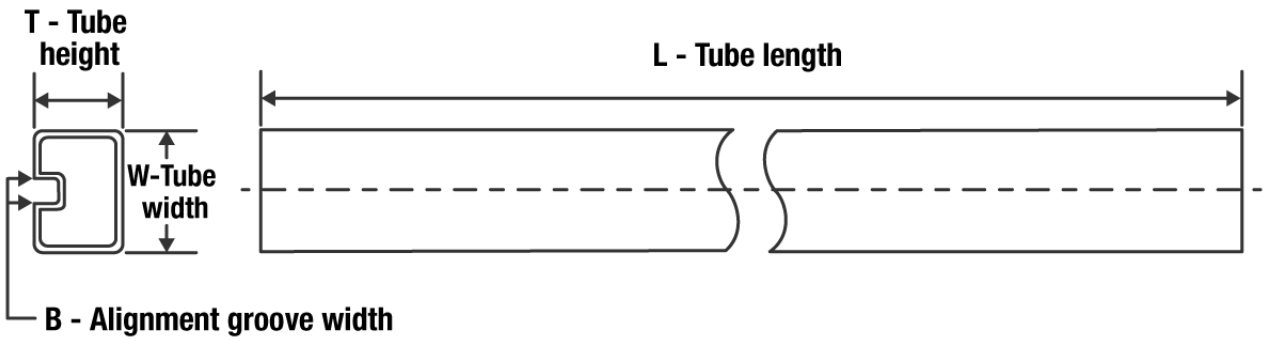
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4066BM96	SOIC	D	14	2500	364.0	364.0	27.0
CD4066BM96	SOIC	D	14	2500	853.0	449.0	35.0
CD4066BM96	SOIC	D	14	2500	340.5	336.1	32.0
CD4066BM96G4	SOIC	D	14	2500	340.5	336.1	32.0
CD4066BM96G4	SOIC	D	14	2500	853.0	449.0	35.0
CD4066BMT	SOIC	D	14	250	210.0	185.0	35.0
CD4066BNSR	SO	NS	14	2000	853.0	449.0	35.0
CD4066BPWR	TSSOP	PW	14	2000	364.0	364.0	27.0
CD4066BPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
CD4066BPWRG4	TSSOP	PW	14	2000	853.0	449.0	35.0

TUBE



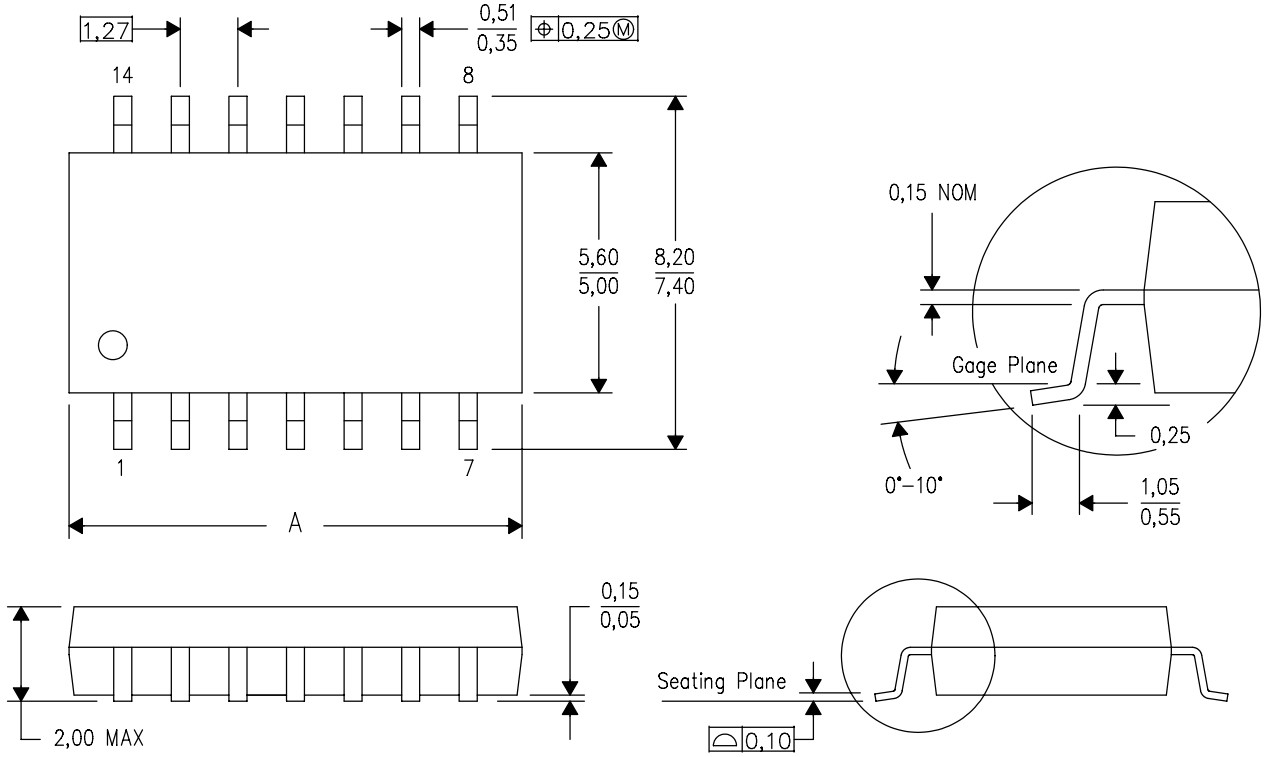
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD4066BE	N	PDIP	14	25	506	13.97	11230	4.32
CD4066BE	N	PDIP	14	25	506	13.97	11230	4.32
CD4066BE	N	PDIP	14	25	506.1	9	600	5.4
CD4066BEE4	N	PDIP	14	25	506	13.97	11230	4.32
CD4066BEE4	N	PDIP	14	25	506	13.97	11230	4.32
CD4066BEE4	N	PDIP	14	25	506.1	9	600	5.4
CD4066BM	D	SOIC	14	50	506.6	8	3940	4.32
CD4066BNS	NS	SOP	14	50	530	10.5	4000	4.1
CD4066BPW	PW	TSSOP	14	90	530	10.2	3600	3.5
CD4066BPWG4	PW	TSSOP	14	90	530	10.2	3600	3.5

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



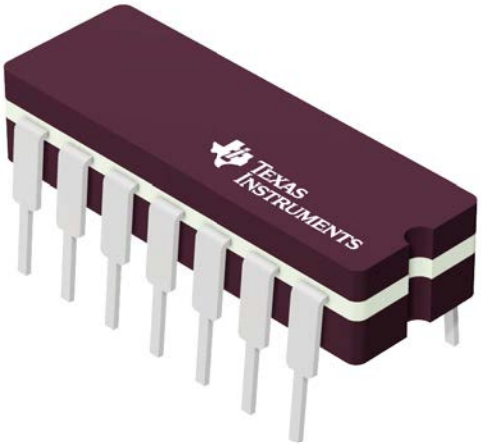
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

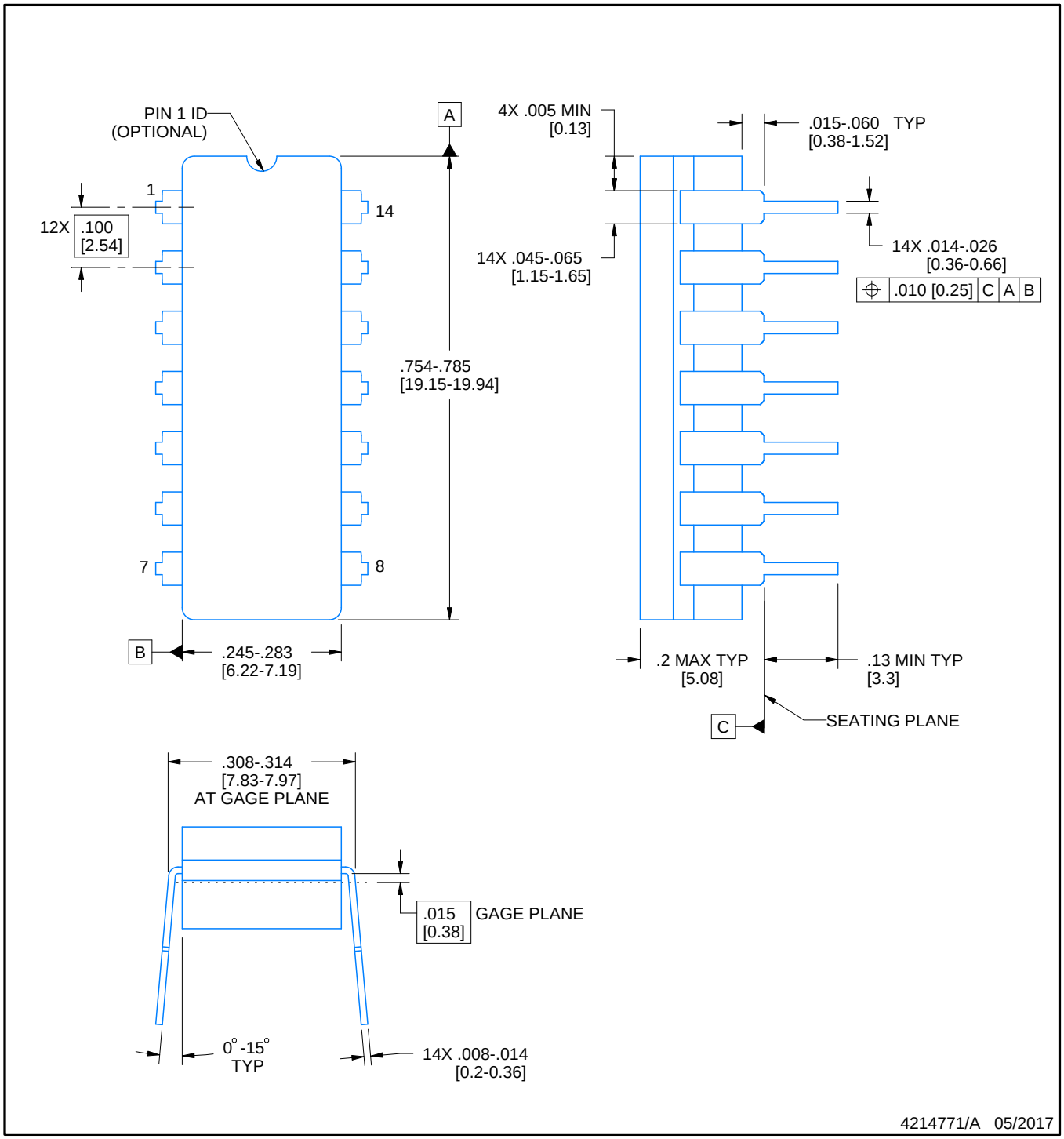
4040083-5/G

PACKAGE OUTLINE

J0014A

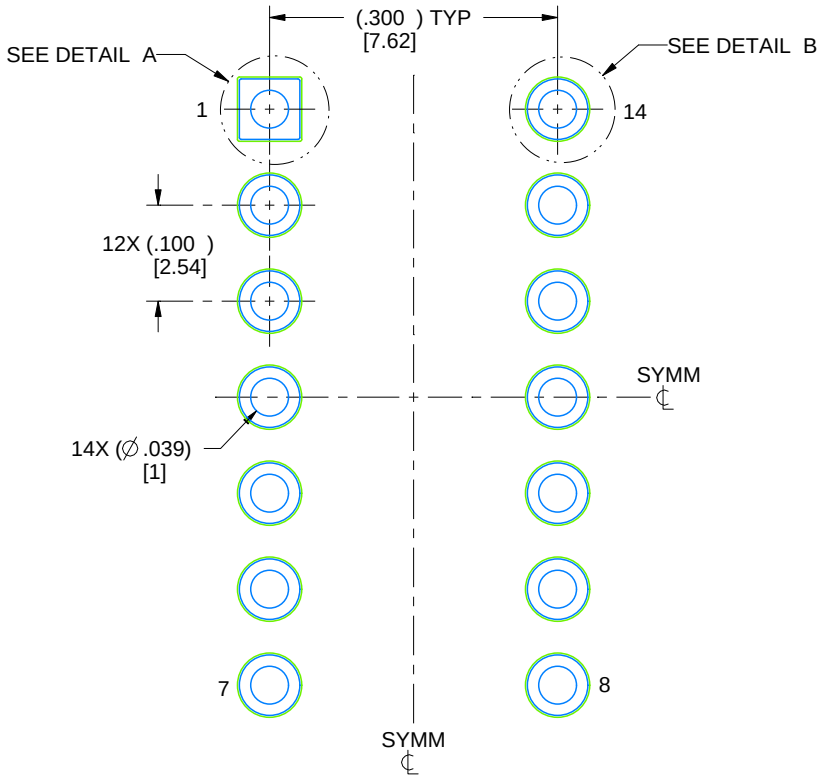
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE

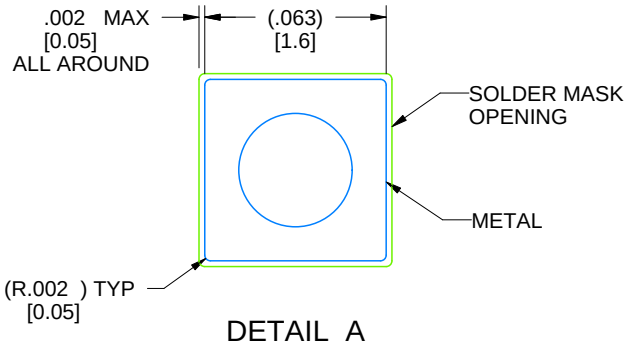


NOTES:

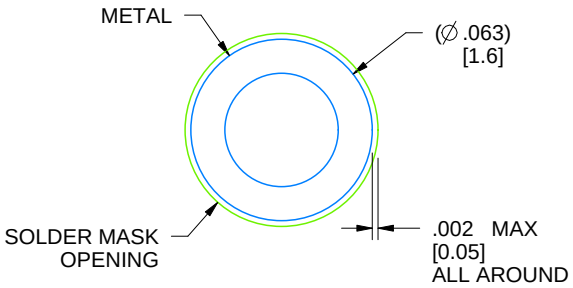
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



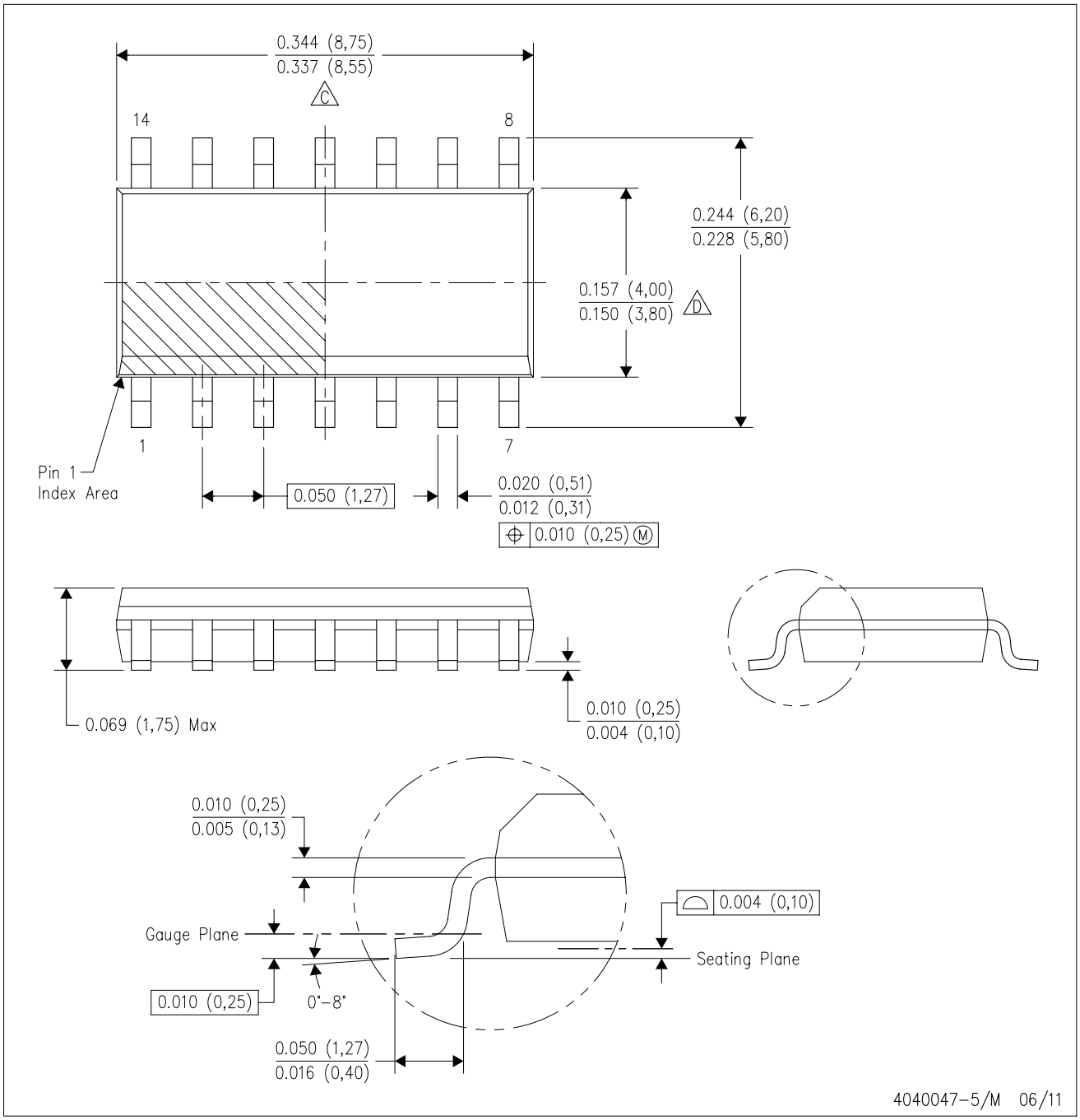
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

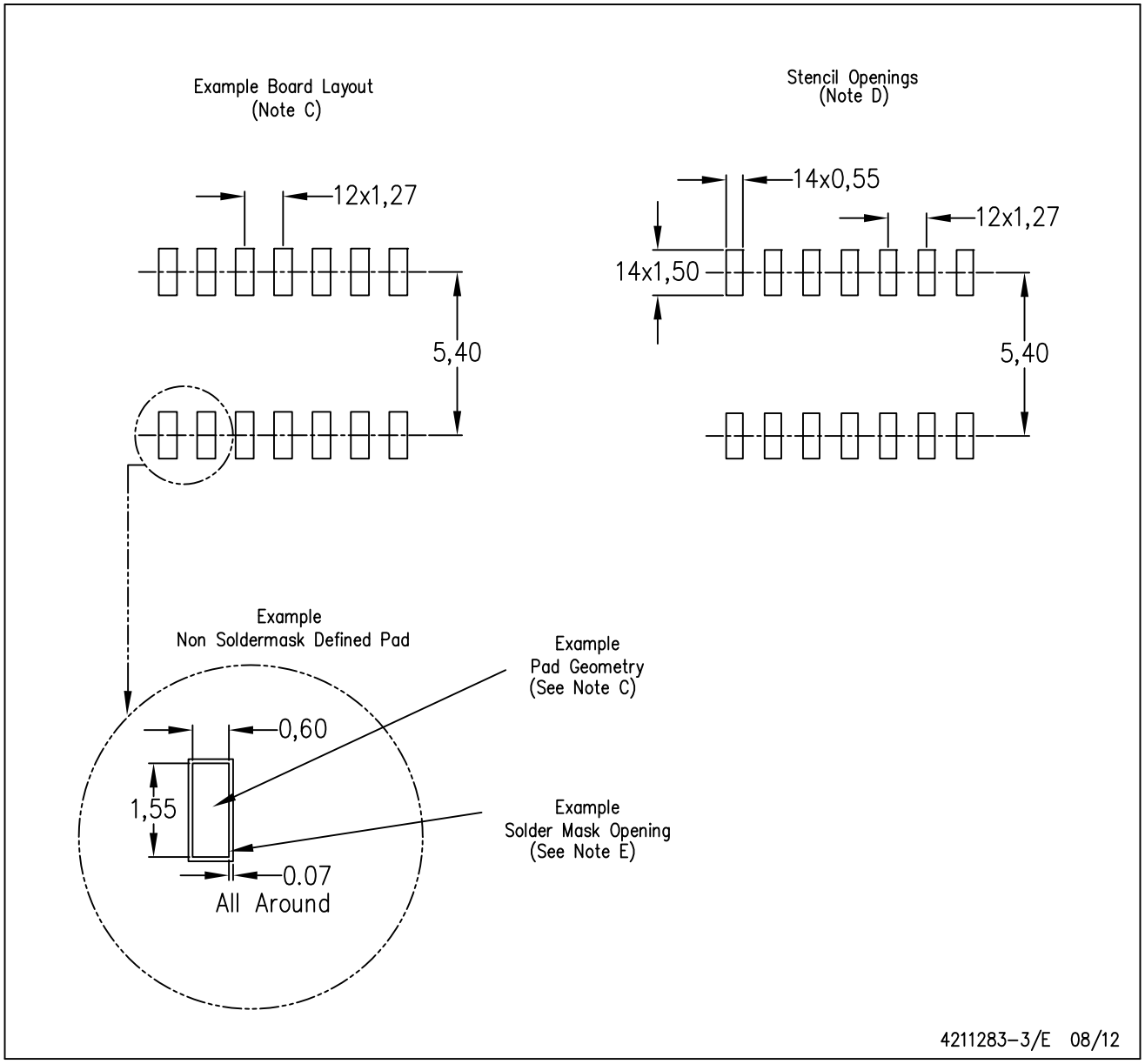
4214771/A 05/2017

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



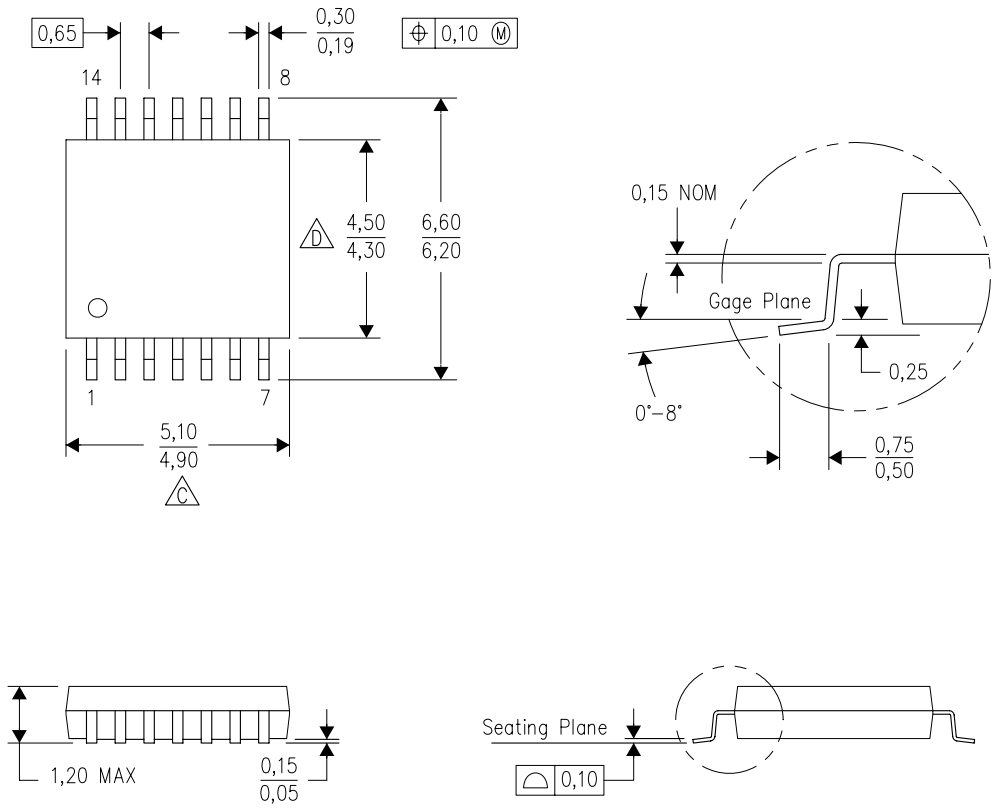
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



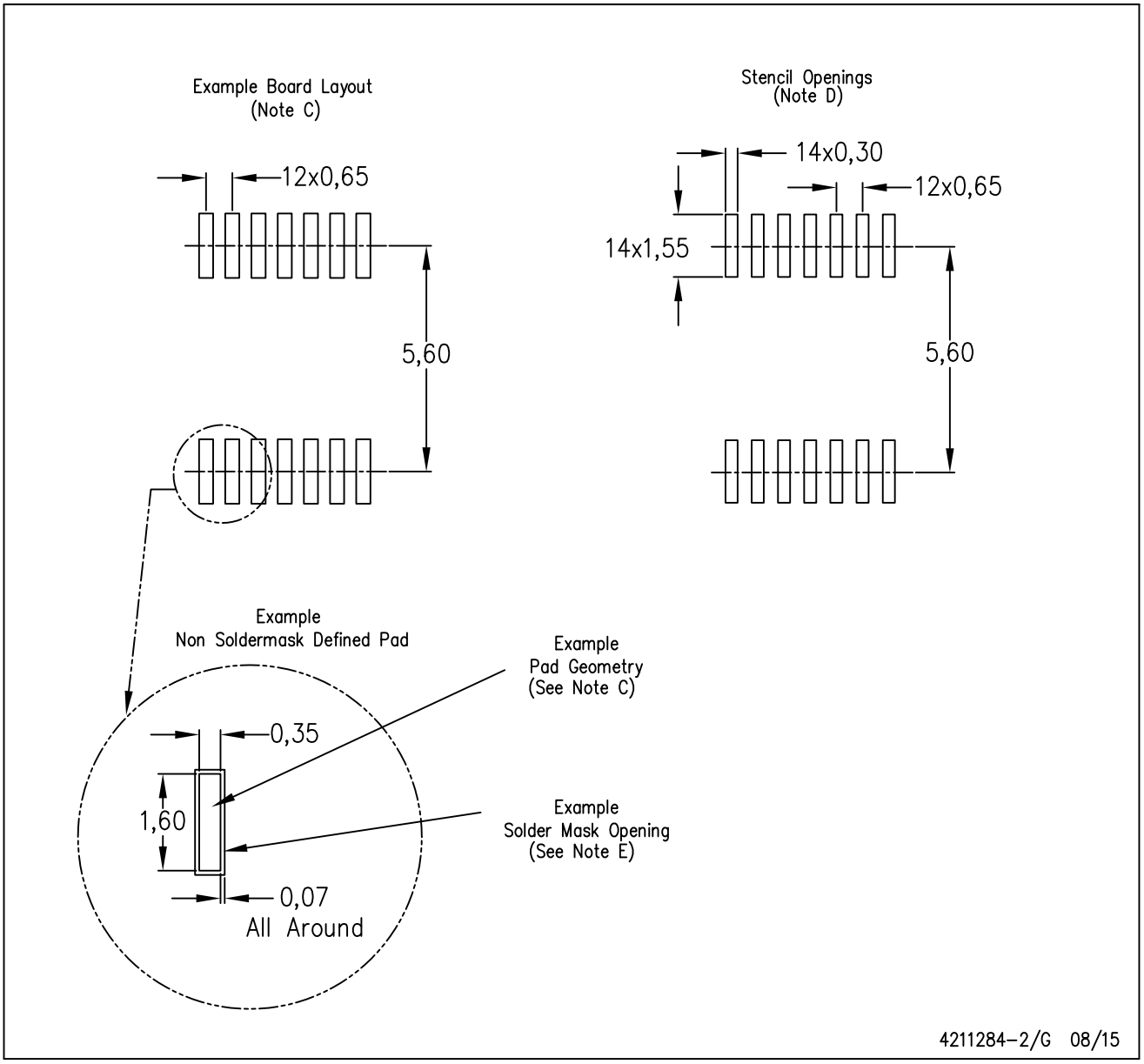
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

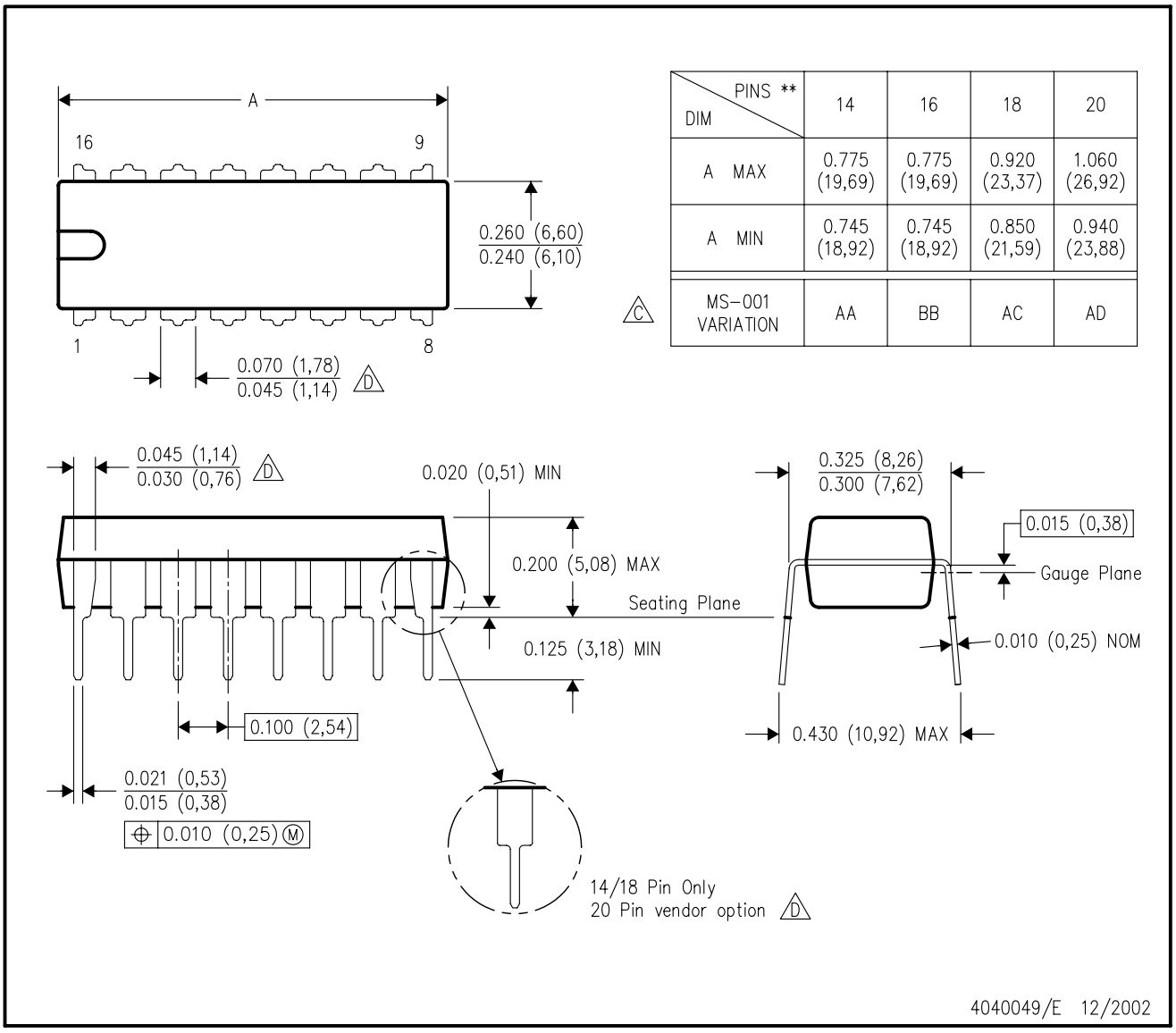
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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