具有三态输出的 CDx4HCT573 八路透明 D 类锁存器

1 特性

- 4.5V 至 5.5V V_{CC} 运行
- −55°C 至 125°C 的宽工作温度范围
- 平衡的传播延迟及转换时间
- 标准输出可驱动多达 10 个 LS-TTL 负载
- 与 LS-TTL 逻辑 IC 相比，可显著降低功耗
- 输入兼容 TTL 电压

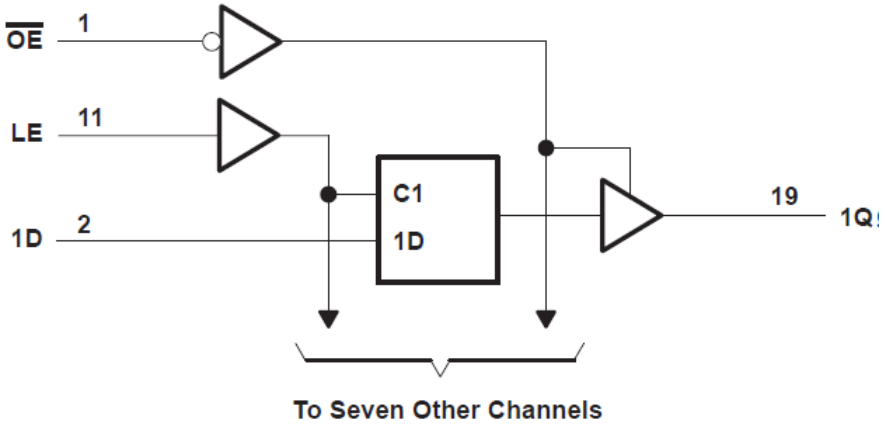
2 说明

HCT573 器件是八路透明 D 型锁存器。在锁存器使能 (LE) 输入为高电平时，Q 输出将跟随数据 (D) 输入。当 LE 为低电平时，Q 输出被锁存在 D 输入端的逻辑电平。

器件信息

器件型号	封装[1]	封装尺寸（标称值）
CD74HCT573M	SOIC (20)	12.80mm × 7.50mm
CD74HCT573DBR	SSOP (20)	7.20mm × 5.30mm
CD74HCT573E	PDIP (20)	25.40mm × 6.35mm
CD54HCT573F	CDIP (20)	26.92mm × 6.92mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



功能方框图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。
English Data Sheet: SCLS455

Table of Contents

1 特性.... 1
2 说明.... 1
3 Revision History.... 2
4 Pin Configuration and Functions.... 3
5 Specifications.... 4
5.1 Absolute Maximum Ratings.... 4
5.2 Recommended Operating Conditions[(1)] 4
5.3 Thermal Information.... 4
5.4 Electrical Characteristics.... 5
5.5 Timing Requirements.... 5
5.6 Switching Characteristics 5
5.7 Operating Characteristics.... 5
6 Parameter Measurement Information.... 6
7 Detailed Description.... 7
7.1 Overview.... 7
7.2 Functional Block Diagram.... 7
7.3 Device Functional Modes.... 7
8 Power Supply Recommendations.... 8
9 Layout.... 8
9.1 Layout Guidelines.... 8
10 Device and Documentation Support.... 9
10.1 接收文档更新通知.... 9
10.2 支持资源.... 9
10.3 Trademarks.... 9
10.4 Electrostatic Discharge Caution.... 9
10.5 术语表.... 9
11 Mechanical, Packaging, and Orderable Information.... 9

3 Revision History

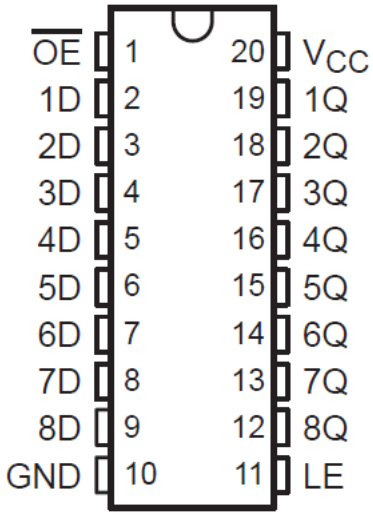
注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (January 2022) to Revision E (June 2022)	Page
• Junction-to-ambient thermal resistance values increased. DW was 58 is now 109.1, DB was 70 is now 122.7, N was 69 is now 84.6	4

Changes from Revision C (May 2004) to Revision D (January 2022)	Page
• 更新了整个文档中的编号、格式、表格、图和交叉参考，以反映现代数据表标准	1

Copyright © 2022 Texas Instruments Incorporated

4 Pin Configuration and Functions



J, DB, N, or DW Package
20-Pin CDIP, SSOP, PDIP, SOIC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
I_{IK}	Input clamp current[2]	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current[2]	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output drain current per output	$V_O = 0$ to V_{CC}		±35	mA
I_O	Continuous output source or sink current per output	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature			150	℃
T_{stg}	Storage temperature range		–65	150	℃

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions[1]

		T_A = 25°C		T_A = −55°C to 125°C		T_A = −40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		2		V
V_{IL}	Low-level input voltage		0.8		0.8		0.8	V
V_I	Input voltage		V_{CC}		V_{CC}		V_{CC}	V
V_O	Output voltage		V_{CC}		V_{CC}		V_{CC}	V
Δt/Δv	Input transition rise or fall rate		500		500		500	ns

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.3 Thermal Information

THERMAL METRIC		DW (SOIC) 20 PINS	DB (SSOP) 20 PINS	N (PDIP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[1]	109.1	122.7	84.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76	81.6	72.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.6	77.5	65.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	51.5	46.1	55.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	77.1	77.1	65.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

Copyright © 2022 Texas Instruments Incorporated

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TESTCONDITIONS		V_{CC}	T_A = 25°C		T_A = −55°C to 125°C		T_A = −40°C to 85°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = −20 µA	4.5 V	4.4		4.4		4.4		V
		I_{OH} = −6 mA		3.98		3.7		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	4.5 V		0.1		0.1		0.1	V
		I_{OL} = 6 mA			0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		5.5 V		±0.1		±1		±1	µA
I_{OZ}	$V_O = V_{CC}$ or 0		5.5 V		±0.5		±10		±5	µA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0		5.5 V		8		160		80	µA
ΔI_{CC} (1)	$\overline{OE}$ input held at V_{CC}− 2.1 V		4.5 V to 5.5 V		450		612.5		562.5	µA
	Any D input held at V_{CC} – 2.1 V		4.5 V to 5.5 V		108		147		135	µA
	LE input held at V_{CC} – 2.1 V		4.5 V to 5.5 V		234		318.5		292.5	µA
C_i					10		10		10	pF
C_o					20		20		20	pF

(1) Additional quiescent supply current per input pin, TTL inputs high, 1 unit load. For dual-supply systems, theoretical worst-case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

5.5 Timing Requirements

over recommended operating free-air temperature range, V_{CC} = 4.5 V (unless otherwise noted) (see 图 6-1)

		T_A = 25°C		T_A = −55°C to 125°C		T_A = −40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	16		24		20		ns
t_{su}	Setup time, data before LE ↓	13		20		16		ns
t_h	Hold time, data after LE ↓	10		15		13		ns

5.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} =4.5 V (unless otherwise noted) (see 图 6-1)

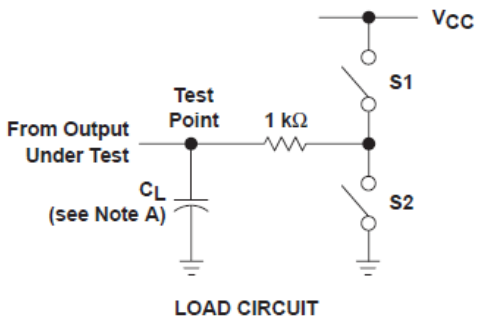
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C		T_A = −55°C to 125°C		T_A = −40°C to 85°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	C_L = 50 pF		35		53		44	ns
	LE				35		53		44	
t_{en}	$\overline{OE}$	Q	C_L = 50 pF		35		53		44	ns
t_{dis}	$\overline{OE}$	Q	C_L = 50 pF		35		53		44	ns
t_t		Q	C_L = 50 pF		12		18		15	ns

5.7 Operating Characteristics

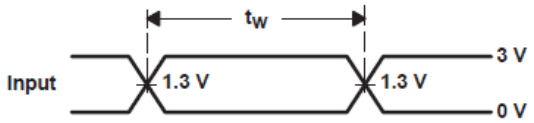
V_{CC} = 5 V, T_A = 25°C

PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance	53	pF

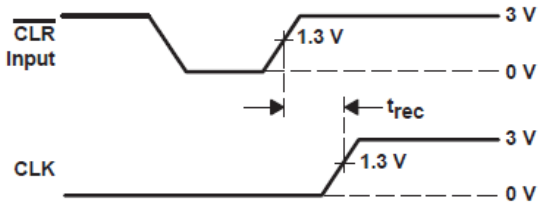
6 Parameter Measurement Information



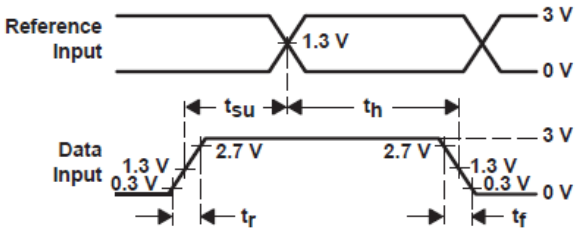
PARAMETER		S1	S2
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd} or t_t		Open	Open



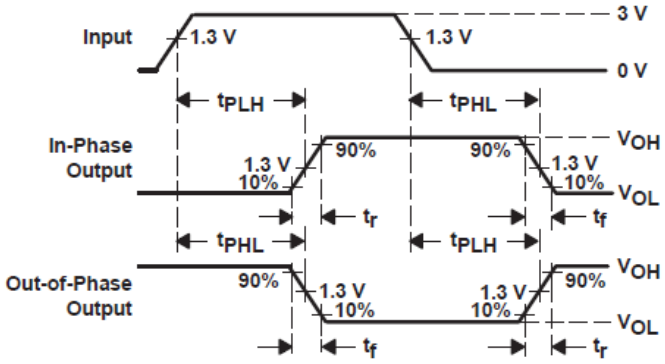
VOLTAGE WAVEFORMS
PULSE DURATION



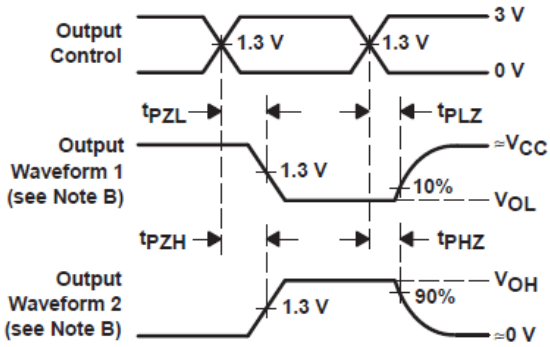
VOLTAGE WAVEFORMS
RECOVERY TIME



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{msx} is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time, with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

图 6-1. Load Circuit and Voltage Waveforms

Copyright © 2022 Texas Instruments Incorporated

7 Detailed Description

7.1 Overview

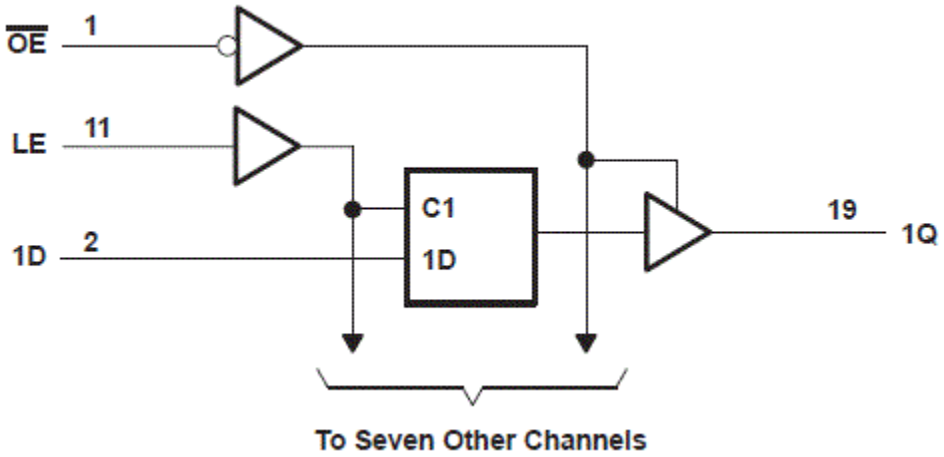
The ’HCT573 devices are octal transparent D-type latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram



7.3 Device Functional Modes

表 7-1. Function Table (each latch)

INPUTS			OUTPUT Q
$\overline{OE}$	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

Copyright © 2022 Texas Instruments Incorporated

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8685601RA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8685601RA CD54HCT573F3A	Samples
CD54HCT573F	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HCT573F	Samples
CD54HCT573F3A	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8685601RA CD54HCT573F3A	Samples
CD74HCT573DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HK573	Samples
CD74HCT573E	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT573E	Samples
CD74HCT573EE4	ACTIVE	PDIP	N	20	20	TBD	Call TI	Call TI	-55 to 125		Samples
CD74HCT573M	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT573M	Samples
CD74HCT573M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT573M	Samples
CD74HCT573M96G4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT573M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HCT573, CD74HCT573 :

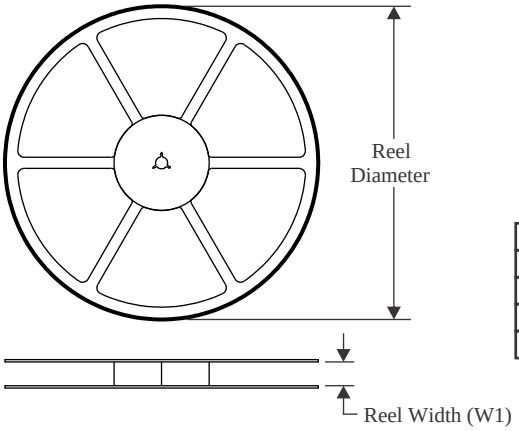
- Catalog : CD74HCT573
- Military : CD54HCT573

NOTE: Qualified Version Definitions:

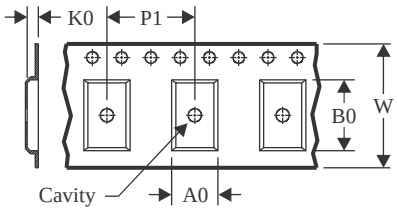
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

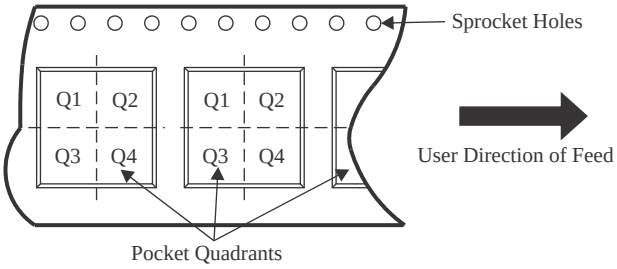


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

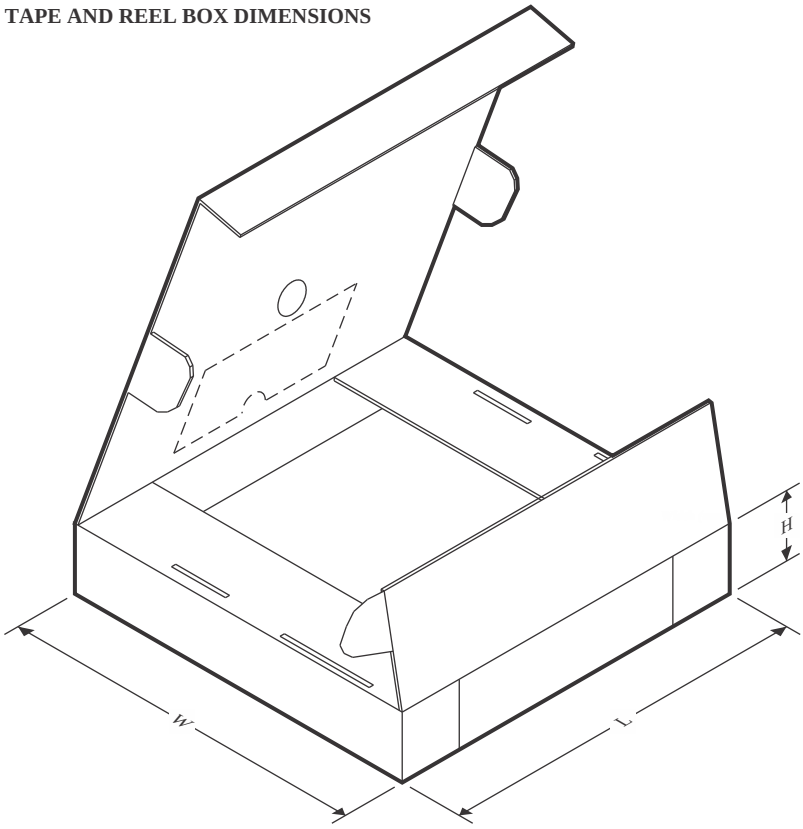
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HCT573DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
CD74HCT573M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

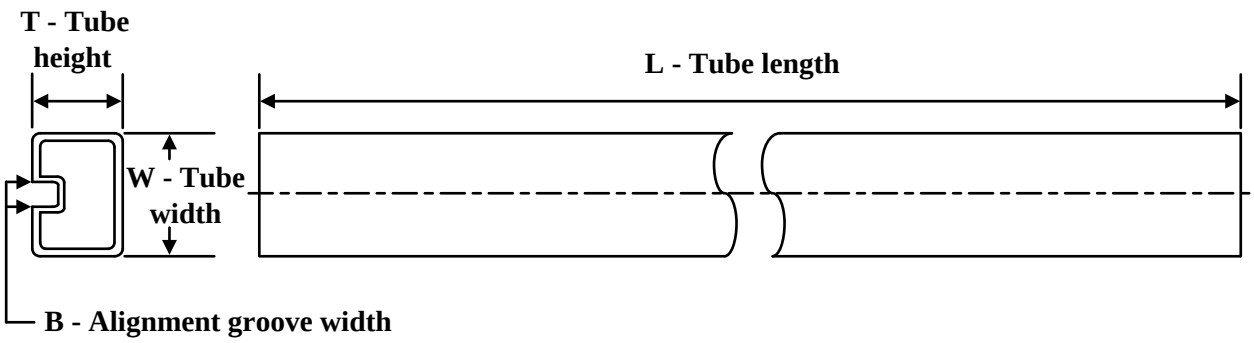
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

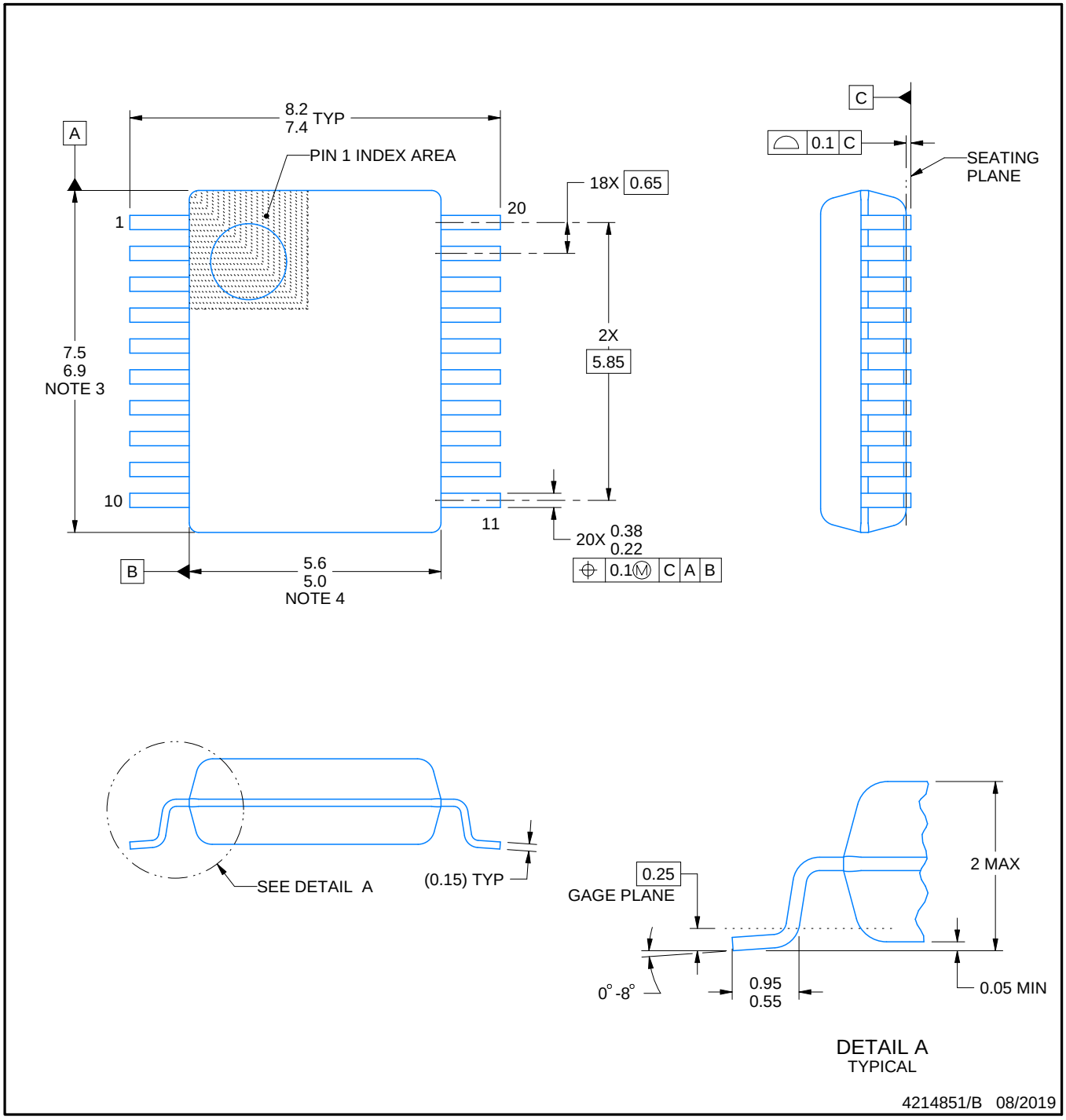
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HCT573DBR	SSOP	DB	20	2000	356.0	356.0	35.0
CD74HCT573M96	SOIC	DW	20	2000	367.0	367.0	45.0

TUBE



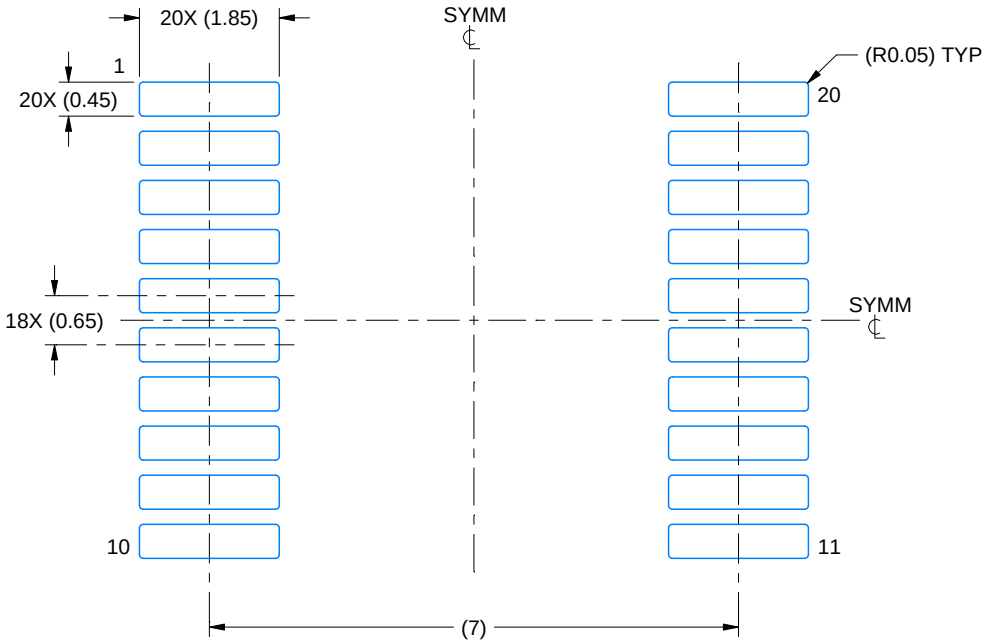
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HCT573E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT573M	DW	SOIC	20	25	507	12.83	5080	6.6

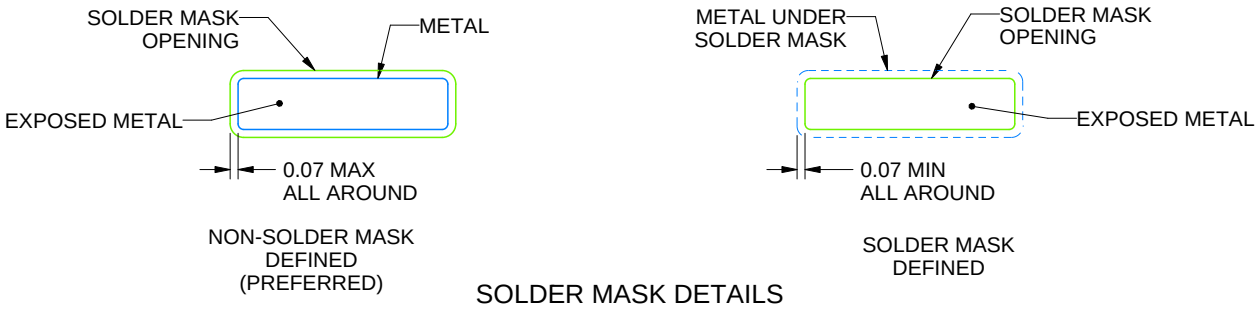


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

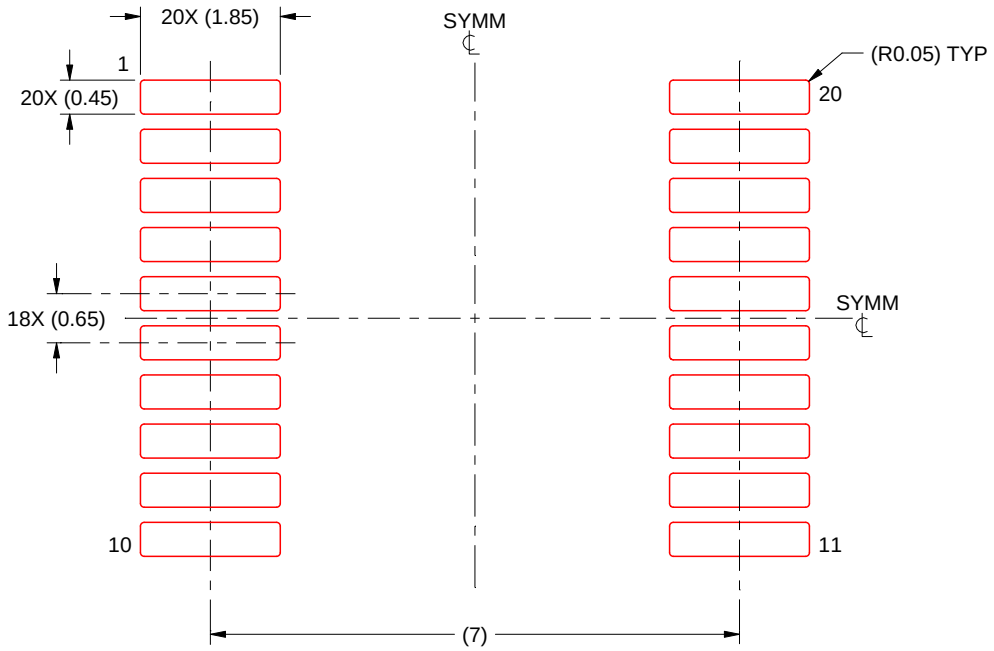


SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

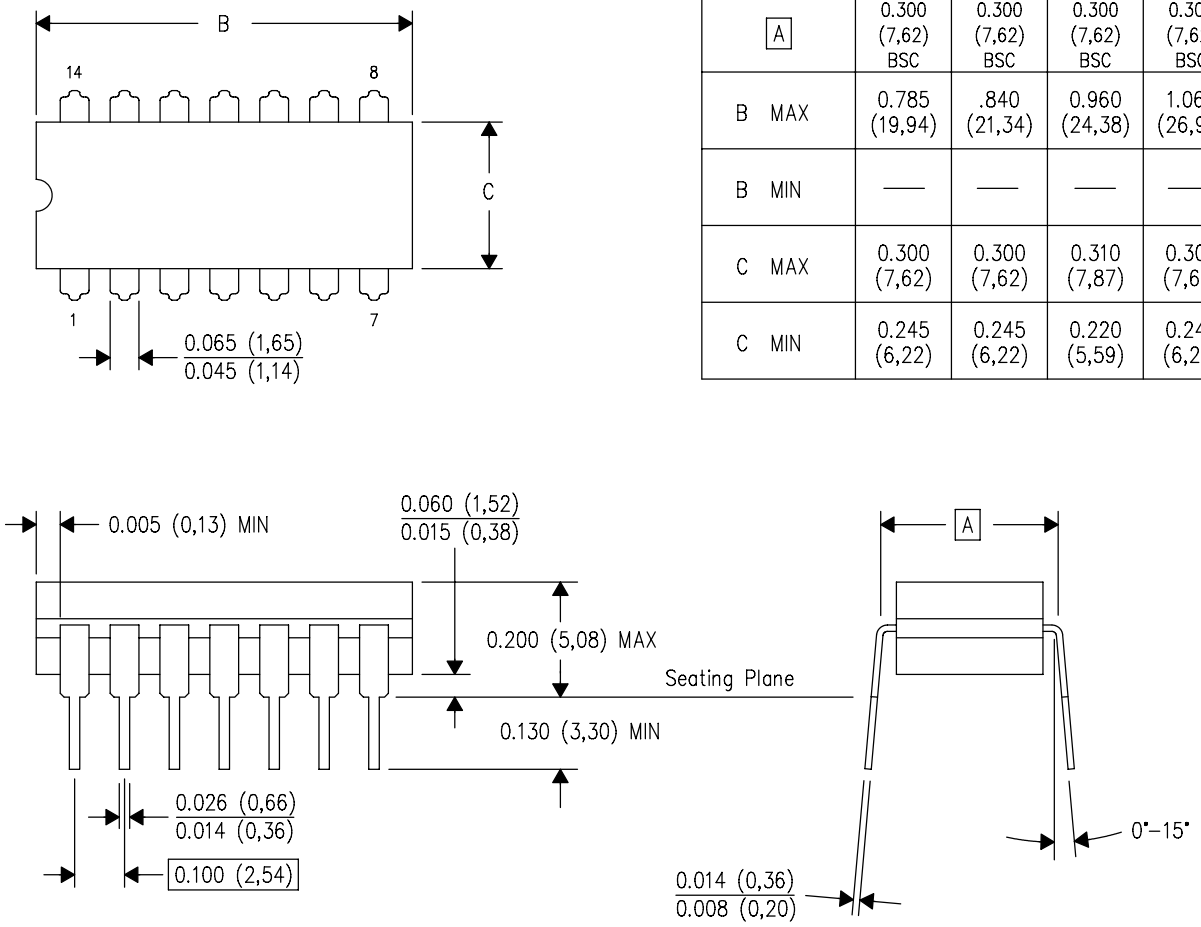
4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



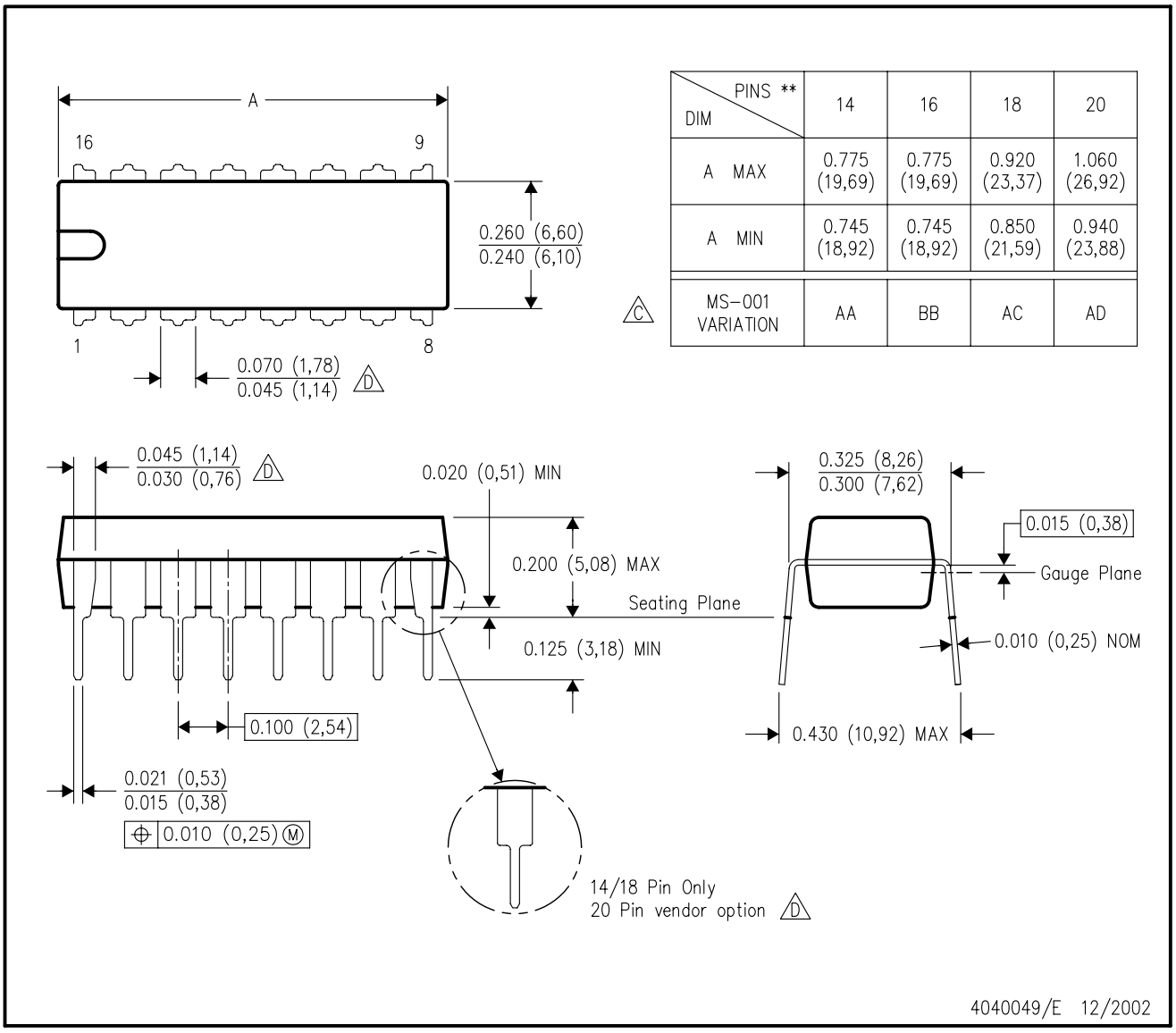
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

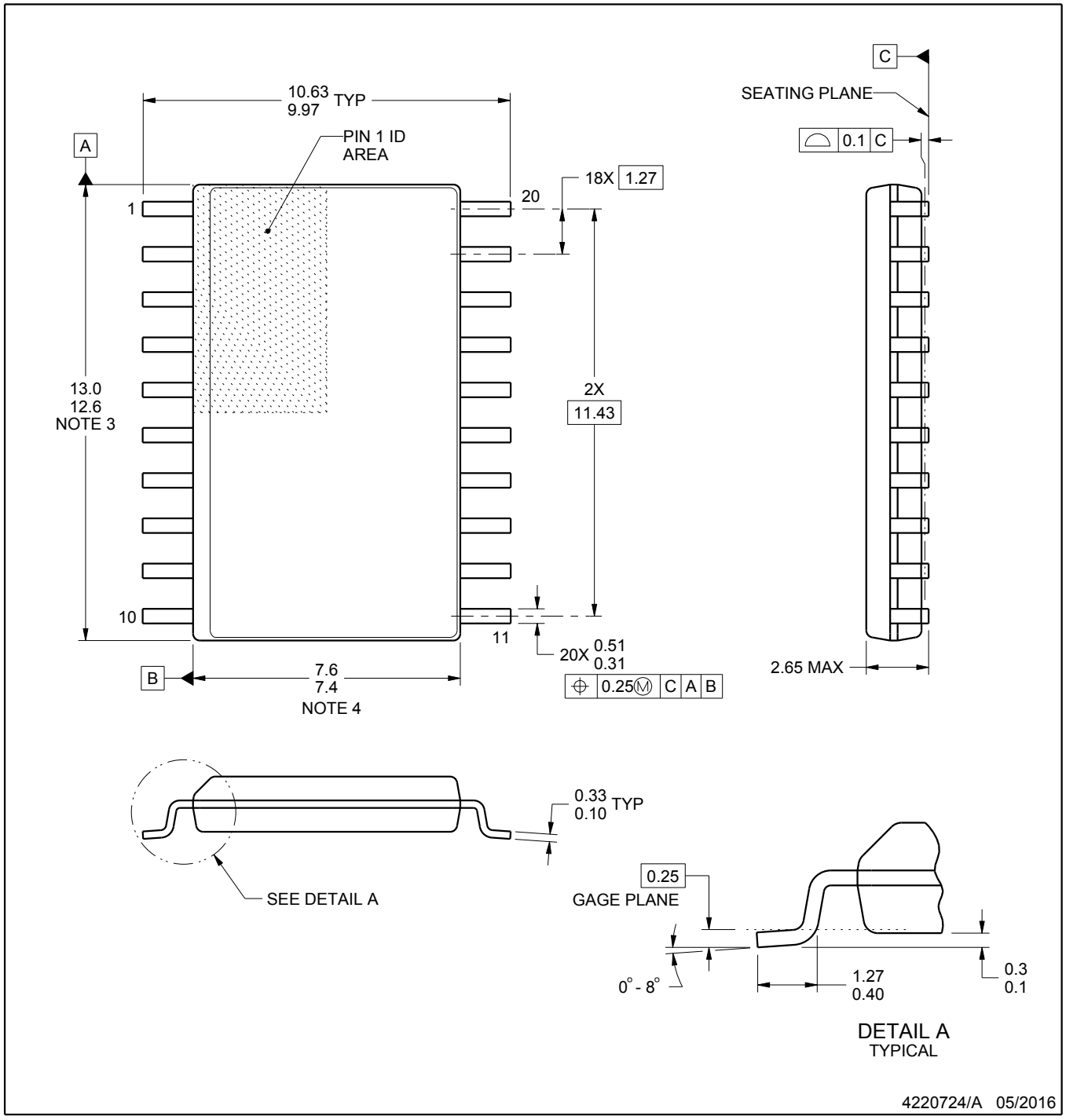
N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



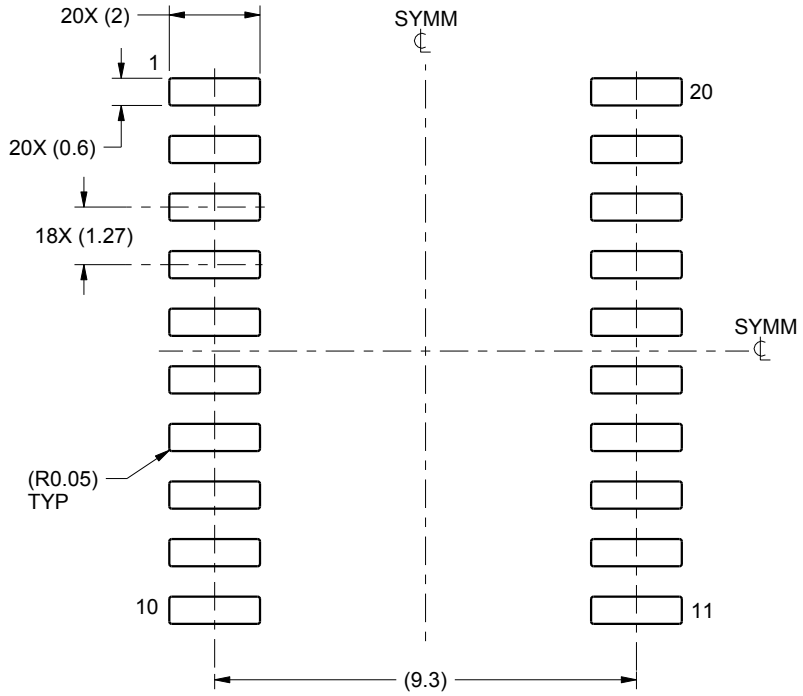
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

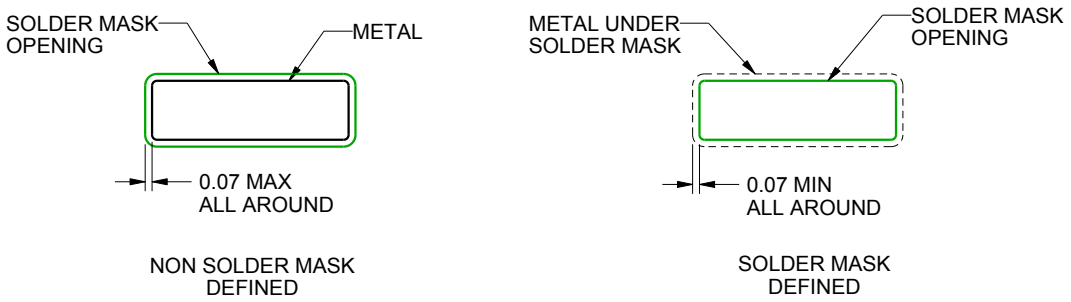


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

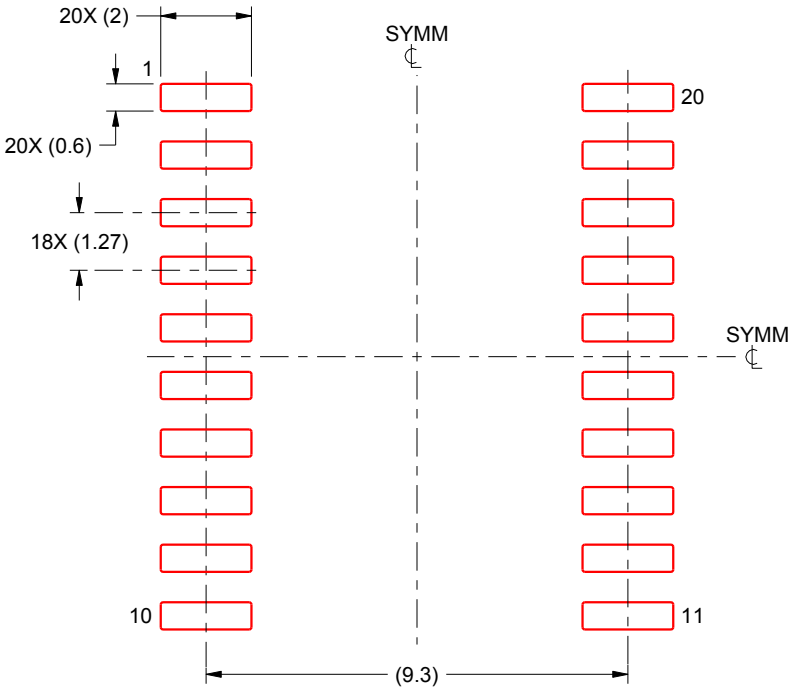


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022，德州仪器 (TI) 公司