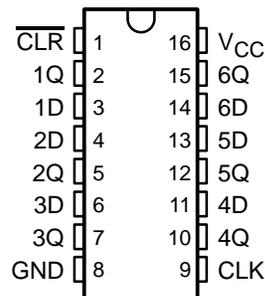


CD54ACT174, CD74ACT174 HEX D-TYPE FLIP-FLOPS WITH CLEAR

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- Inputs Are TTL-Voltage Compatible
- Contain Six Flip-Flops With Single-Rail Outputs
- Buffered Inputs
- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Balanced Propagation Delays
- ± 24 -mA Output Drive Current
 - Fanout to 15 F Devices
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015
- Applications Include:
 - Buffer/Storage Registers
 - Shift Registers

CD54ACT174 . . . F PACKAGE
CD74ACT174 . . . E OR M PACKAGE
(TOP VIEW)



description/ordering information

The 'ACT174 devices are positive-edge-triggered D-type flip-flops with a direct clear ($\overline{\text{CLR}}$) input and are designed for 4.5-V to 5.5-V V_{CC} operation.

Information at the data (D) inputs that meets the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	PDIP – E	Tube	CD74ACT174E	CD74ACT174E
	SOIC – M	Tube	CD74ACT174M	ACT174M
		Tape and reel	CD74ACT174M96	
	CDIP – F	Tube	CD54ACT174F3A	CD54ACT174F3A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each flip-flop)

INPUTS			OUTPUT
$\overline{\text{CLR}}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q ₀



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

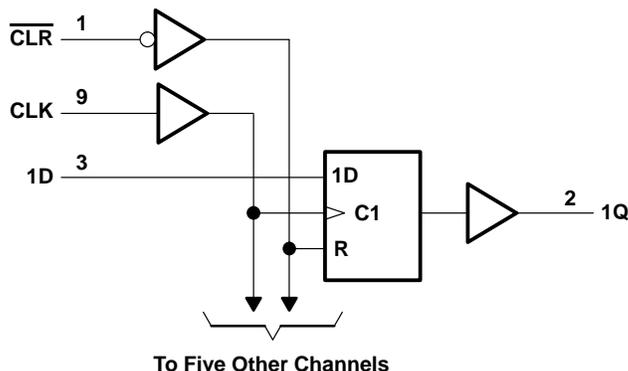
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

CD54ACT174, CD74ACT174 HEX D-TYPE FLIP-FLOPS WITH CLEAR

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 6 V
Input clamp current, I_{IK} ($V_I < 0$ V or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ V or $V_O > V_{CC}$) (see Note 1)	± 50 mA
Continuous output current, I_O ($V_O > 0$ V or $V_O < V_{CC}$)	± 50 mA
Continuous current through V_{CC} or GND	± 150 mA
Package thermal impedance, θ_{JA} (see Note 2): E package	67°C/W
M package	73°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

	$T_A = 25^\circ\text{C}$		$-55^\circ\text{C to } 125^\circ\text{C}$		$-40^\circ\text{C to } 85^\circ\text{C}$		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH} High-level input voltage	2		2		2		V
V_{IL} Low-level input voltage		0.8		0.8		0.8	V
V_I Input voltage	0	V_{CC}	0	V_{CC}	0	V_{CC}	V
V_O Output voltage	0	V_{CC}	0	V_{CC}	0	V_{CC}	V
I_{OH} High-level output current		-24		-24		-24	mA
I_{OL} Low-level output current		24		24		24	mA
$\Delta t/\Delta v$ Input transition rise or fall rate		10		10		10	ns/V

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



**CD54ACT174, CD74ACT174
HEX D-TYPE FLIP-FLOPS
WITH CLEAR**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C		–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = –50 μA	4.5 V	4.4	4.4	4.4			V
		I _{OH} = –24 mA	4.5 V	3.94	3.7	3.8			
		I _{OH} = –50 mA†	5.5 V		3.85				
		I _{OH} = –75 mA†	5.5 V			3.85			
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 50 μA	4.5 V	0.1	0.1	0.1			V
		I _{OL} = 24 mA	4.5 V	0.36	0.5	0.44			
		I _{OL} = 50 mA†	5.5 V		1.65				
		I _{OL} = 75 mA†	5.5 V			1.65			
I _I	V _I = V _{CC} or GND	5.5 V	±0.1	±1	±1			μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	8	160	80			μA	
ΔI _{CC} ‡	V _I = V _{CC} – 2.1 V	4.5 V to 5.5 V	2.4	3	2.8			mA	
C _i			10	10	10			pF	

† Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

‡ Additional quiescent supply current per input pin, TTL inputs high, 1 unit load

ACT INPUT LOAD TABLE

INPUT	UNIT LOAD
Data	0.5
CLR	0.5
CLK	0.83

Unit Load is ΔI_{CC} limit specified in electrical characteristics table (e.g., 2.4 mA at 25°C).

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

		–55°C to 125°C		–40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		80		91	MHz
t _w	Pulse duration	CLR low		4	3.5	ns
		CLK high or low		6.2	5.4	
t _{su}	Setup time before CLK↑	Data		2	2	ns
t _h	Hold time, data after CLK↑			2.5	2.2	ns
t _{rec}	Recovery time, before CLK↑	CLR↑		1.5	1.5	ns



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**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)**

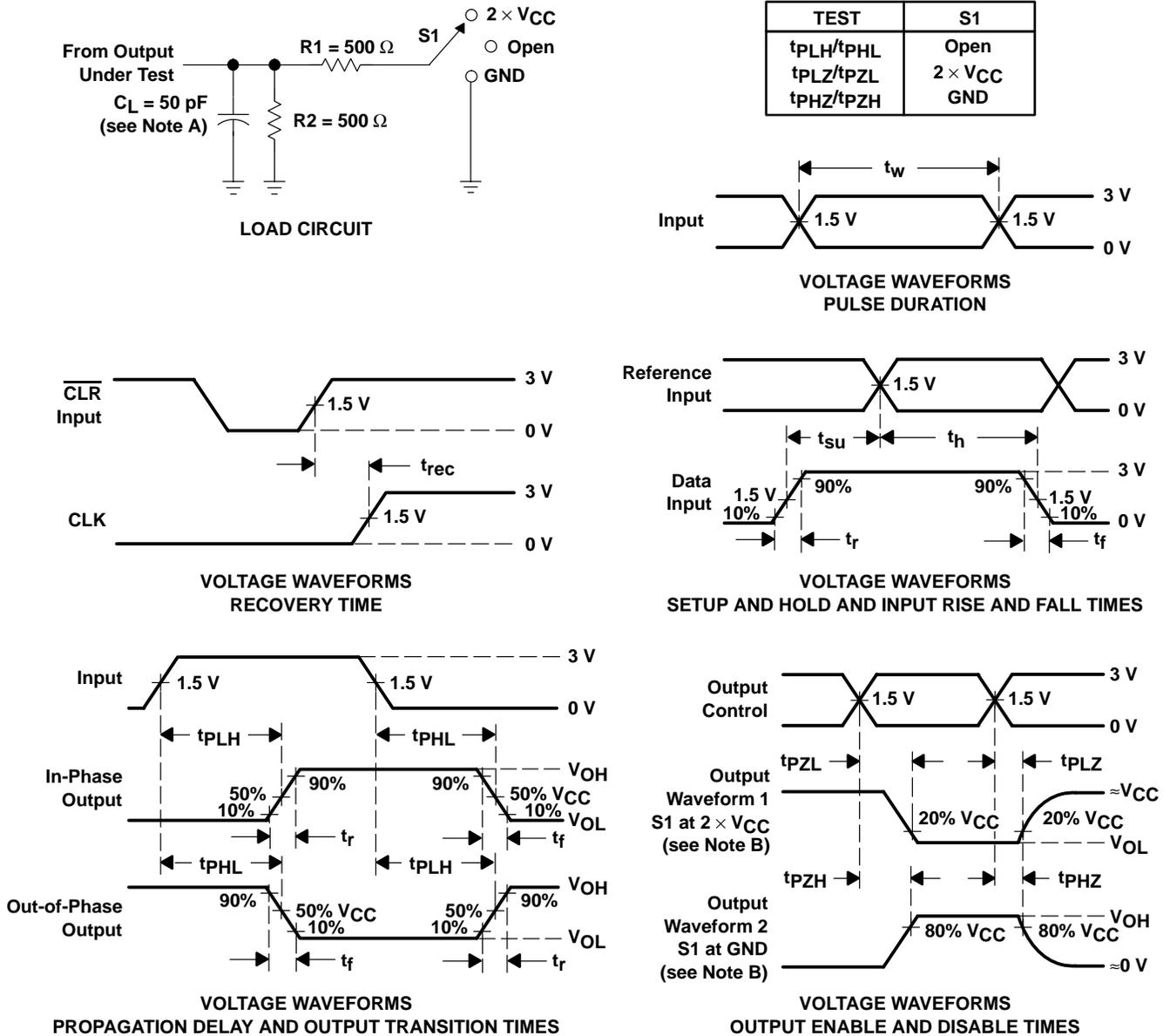
PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			80		91		MHz
t_{PLH}	CLK	Any Q	3.5	14	3.6	12.6	ns
t_{PHL}			3.5	14	3.6	12.6	
t_{PLH}	$\overline{\text{CLR}}$	Any Q	3.9	15.5	4	14.1	ns
t_{PHL}			3.9	15.5	4	14.1	

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance	37	pF



PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$. Phase relationships between waveforms are arbitrary.
 - D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
 - E. The outputs are measured one at a time with one input transition per measurement.
 - F. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - G. t_{PZL} and t_{PZH} are the same as t_{en} .
 - H. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - I. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD54ACT174F3A	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54ACT174F3A	Samples
CD74ACT174E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74ACT174E	Samples
CD74ACT174M	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT174M	Samples
CD74ACT174M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT174M	Samples
CD74ACT174M96G4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT174M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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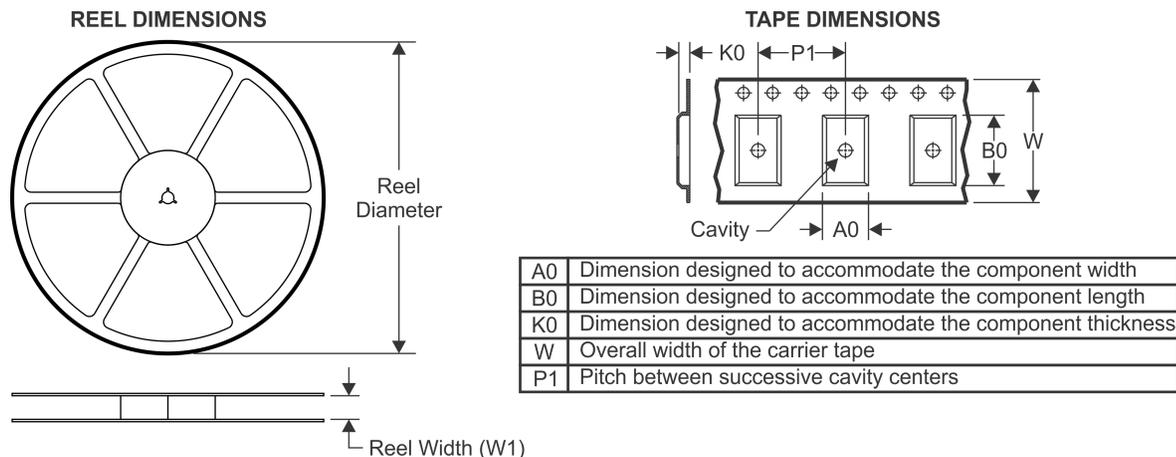
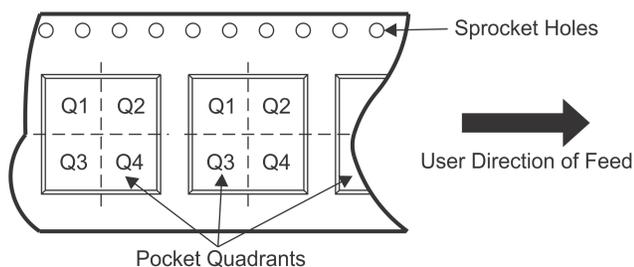
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OTHER QUALIFIED VERSIONS OF CD54ACT174, CD74ACT174 :

- Catalog : [CD74ACT174](#)
- Military : [CD54ACT174](#)

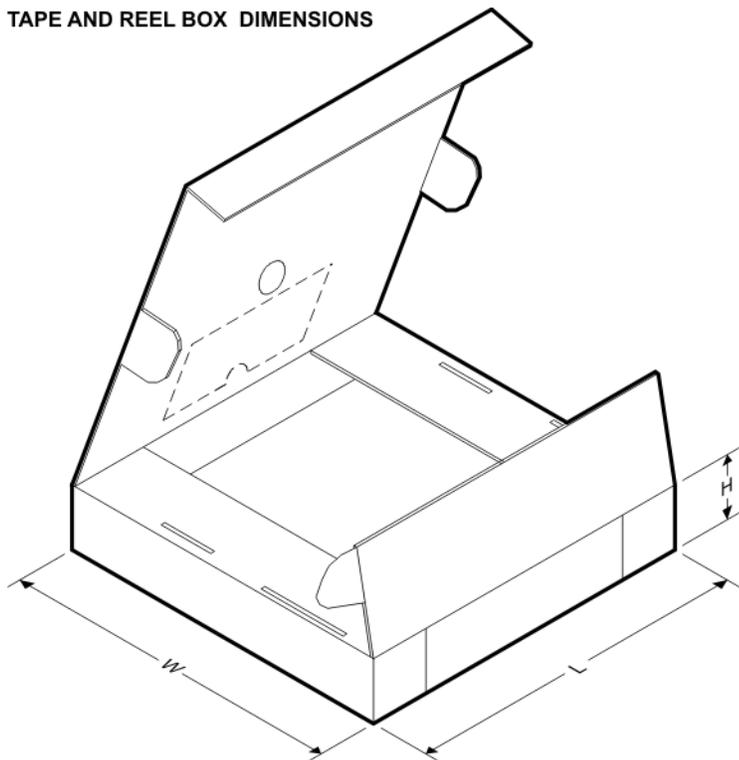
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- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


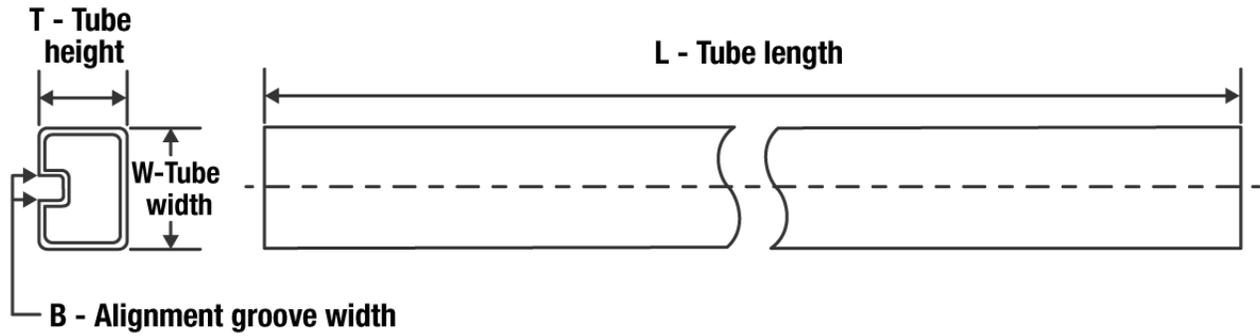
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74ACT174M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74ACT174M96	SOIC	D	16	2500	340.5	336.1	32.0

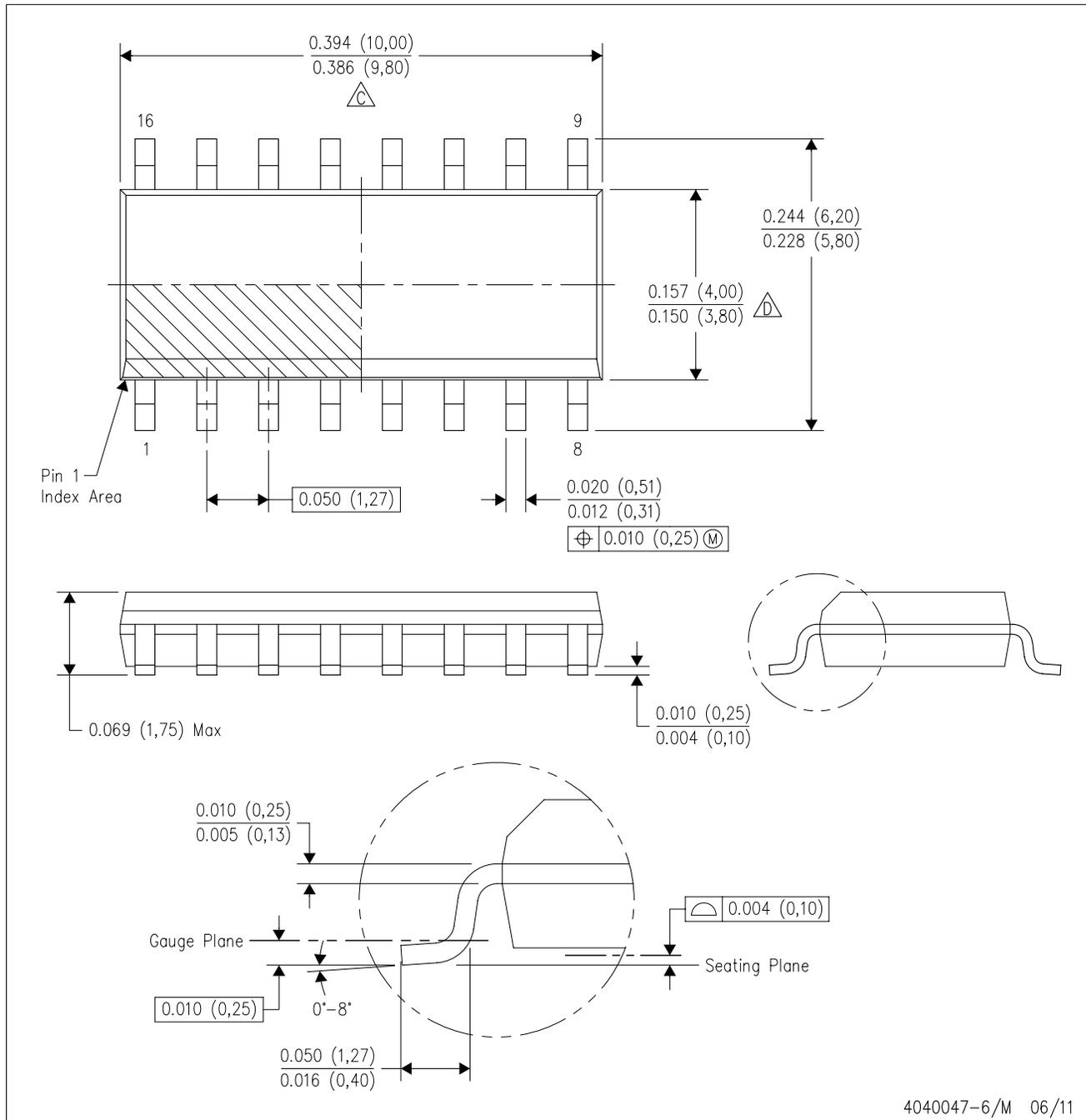
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74ACT174E	N	PDIP	16	25	506	13.97	11230	4.32
CD74ACT174E	N	PDIP	16	25	506	13.97	11230	4.32
CD74ACT174M	D	SOIC	16	40	507	8	3940	4.32

D (R-PDSO-G16)

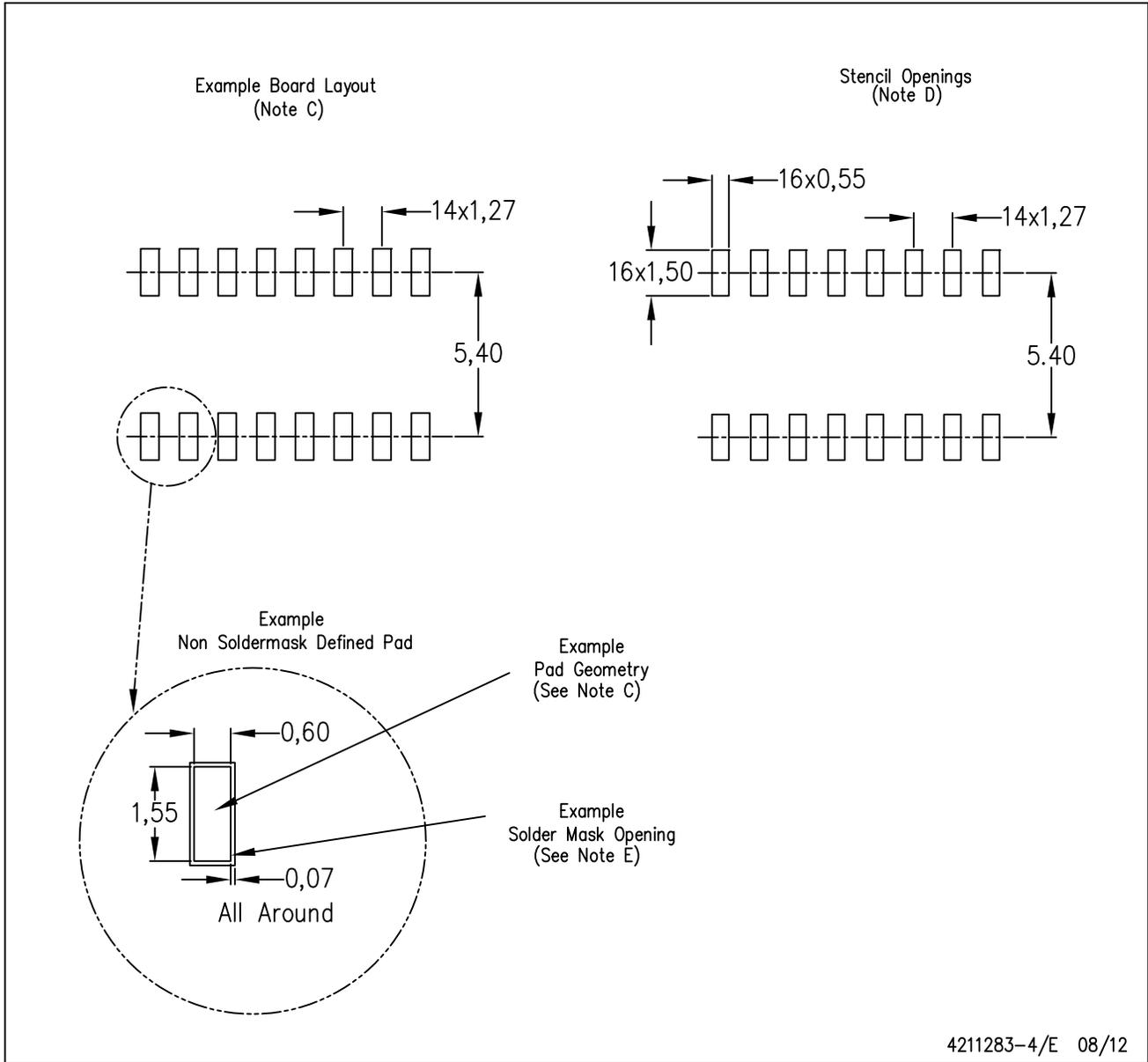
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



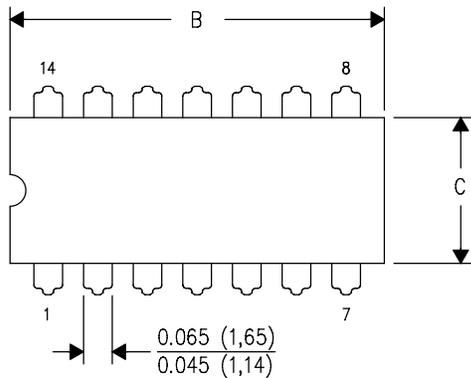
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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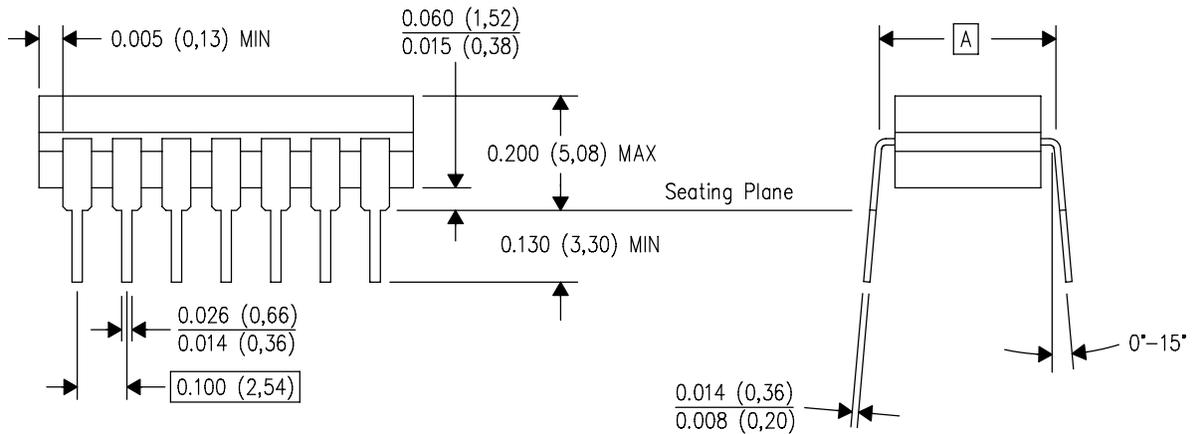
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

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