CDx4HC(T)259 高速 SMOS 逻辑 8 位可寻址锁存器

1 特性

- 缓冲输入和输出
- 四个工作模式
- 当 V_{CC} = 5V、C_L = 15pF、T_A = 25ºC 时的传播延迟典型值
- 扇出（在温度范围内）
  - 标准输出：10 个 LSTTL 负载
  - 总线驱动器输出：15 个 LSTTL 负载
- 宽工作温度范围：-55ºC 至 125ºC
- 平衡的传播延迟及转换时间
- 与 LSTTL 逻辑 IC 相比，可显著降低功耗
- HC 类型
  - 工作电压为 2 V 至 6 V
  - 高抗噪性：当 V_{CC} = 5 V 时，N_{IL} = 30%，N_{IH} = V_{CC} 的 30%
- HCT 类型
  - 工作电压为 4.5 V 至 5.5 V
  - 直接 LSTTL 输入逻辑兼容性，V_{IL} = 0.8V（最大值），V_{IH} = 2V（最小值）
  - CMOS 输入兼容性，当电压为 V_{OL}、V_{OH} 时，I_I ≤ 1μA

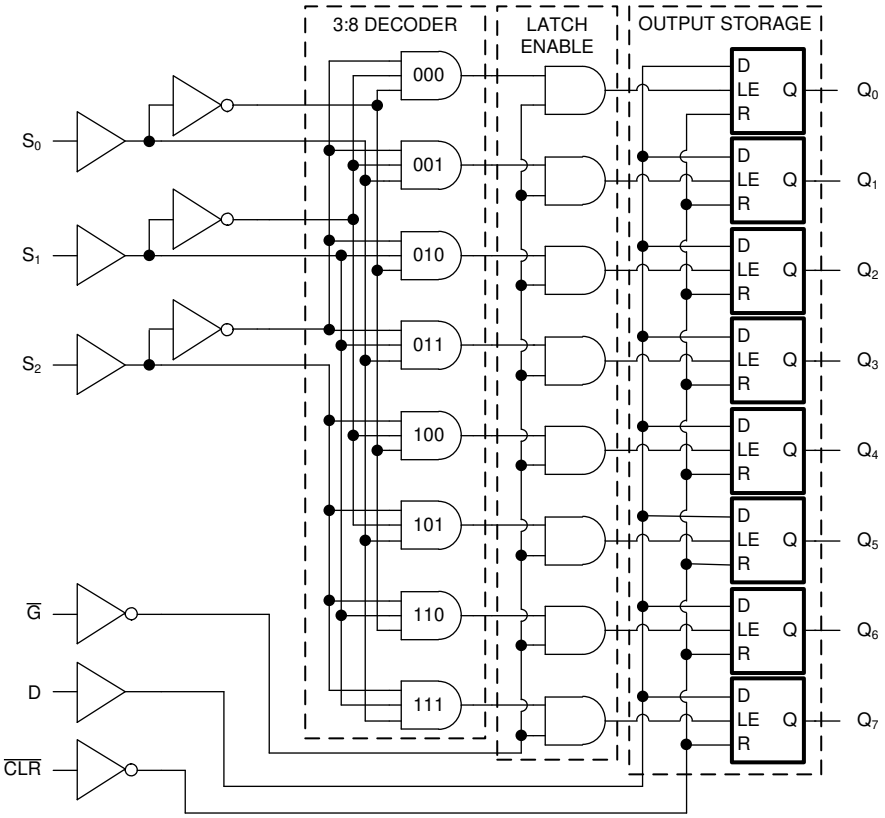
2 说明

CDx4HC(T)259 是具有三个有效工作模式（可寻址锁存器、存储器和 8 线解码器）和一个复位模式的 8 位可寻址锁存器。

器件信息

器件型号	封装[(1)]	封装尺寸（标称值）
CD54HC259F3A	陶瓷双列直插封装 (CDIP) (16)	21.34mm × 6.92mm
CD54HCT259F3A	陶瓷双列直插封装 (CDIP) (16)	21.34mm × 6.92mm
CD74HC259E	PDIP (16)	19.31mm × 6.35mm
CD74HCT259E	PDIP (16)	19.31mm × 6.35mm
CD74HC259M	SOIC (16)	9.90mm × 3.90mm
CD74HCT259M	SOIC (16)	9.90mm × 3.90mm

(1) 如需了解所有封装，请参阅数据表末尾的可订购产品附录。



功能框图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

Table of Contents

1 特性 1
2 说明 1
3 Revision History 2
4 Pin Configuration and Functions 3
5 Specifications 4
5.1 Absolute Maximum Ratings 4
5.2 Recommended Operating Conditions 4
5.3 Thermal Information 4
5.4 Electrical Characteristics 5
5.5 Prerequisite for Switching Characteristics 6
5.6 Switching Characteristics[(2)] 7
6 Parameter Measurement Information 8
7 Detailed Description 10
7.1 Overview 10
7.2 Functional Block Diagram 10
7.3 Device Functional Modes 11
8 Power Supply Recommendations 12
9 Layout 12
9.1 Layout Guidelines 12
10 Device and Documentation Support 13
10.1 Documentation Support 13
10.2 接收文档更新通知 13
10.3 支持资源 13
10.4 Trademarks 13
10.5 Electrostatic Discharge Caution 13
10.6 术语表 13
11 Mechanical, Packaging, and Orderable Information 13

3 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (October 2003) to Revision D (November 2021)	Page
• 更新了整个文档中的编号、格式、表格、图和交叉参考，以反映现代数据表标准	1
• Updated pin names to match current TI naming conventions. A_0 is now S_0, A_1 is now S_1, A_2 is now S_2	3

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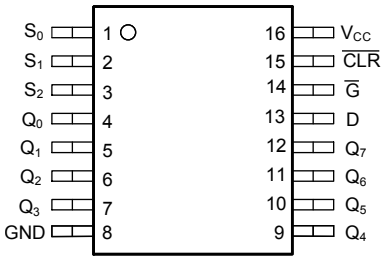
4 Pin Configuration and Functions



J, D or PW Package
16-Pin CDIP, SOIC or TSSOP
Top View

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		-0.5	7	V
I_{IK}	Input clamp diode current	For V_I < -0.5V or V_I > V_{CC} + 0.5V		±20	mA
I_{OK}	Output clamp diode current	For V_O < -0.5V or V_O > V_{CC} + 0.5V		±20	mA
I_O	Drain current, per output	For -0.5V < V_O < V_{CC} + 0.5V		±25	mA
I_O	Output source or sink current per output pin	For V_O > -0.5V or V_O < V_{CC} + 0.5V		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C
	Lead temperature (Soldering 10s) (SOIC - lead tips only)			300	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage range	HC Types	2	6	V
		HCT Types	4.5	5.5	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
t_t	Input rise and fall time	V_{CC} = 2V		1000	ns
		V_{CC} = 4.5V		500	
		V_{CC} = 6V		400	
T_A	Temperature range		-55	125	°C

5.3 Thermal Information

THERMAL METRIC		CD74HC259, CD74HCT259		UNIT
		N (PDIP)	D (SOIC)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[1]	67	73	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS	V_{CC} (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V_{IH}	High-level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		V
			6	4.2			4.2		4.2		V
V_{IL}	Low-level input voltage		2			0.5		0.5		0.5	V
			4.5			1.35		1.35		1.35	V
			6			1.8		1.8		1.8	V
V_{OH}	High-level output voltage	I_{OH} = – 20 µA	2	1.9			1.9		1.9		V
		I_{OH} = – 20 µA	4.5	4.4			4.4		4.4		V
		I_{OH} = – 20 µA	6	5.9			5.9		5.9		V
	High-level output voltage	I_{OH}= – 4 mA	4.5	3.98			3.84		3.7		V
		I_{OH} = – 5.2 mA	6	5.48			5.34		5.2		V
V_{OL}	Low-level output voltage	I_{OL} = 20 µA	2			0.1		0.1		0.1	V
		I_{OL} = 20 µA	4.5			0.1		0.1		0.1	V
		I_{OL} = 20 µA	6			0.1		0.1		0.1	V
	Low-level output voltage	I_{OL}= 4 mA	4.5			0.26		0.33		0.4	V
		I_{OL} = 5.2 mA	6			0.26		0.33		0.4	V
I_I	Input leakage current	V_I = V_{CC} or GND	6			±0.1		±1		±1	µA
I_{CC}	Supply current	V_I = V_{CC} or GND	6			8		80		160	µA
HCT TYPES											
V_{IH}	High-level input voltage		4.5 to 5.5	2			2		2		V
V_{IL}	Low-level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	High-level output voltage	V_{OH} = – 20 µA	4.5	4.4			4.4		4.4		V
	HIgh-level output voltage	V_{OH} = – 4 mA	4.5	3.98			3.84		3.7		V
V_{OL}	Low-level output voltage	V_{OL} = 20 µA	4.5			0.1		0.1		0.1	V
	Low-level output voltage	V_{OL} = 4 mA	4.5			0.26		0.33		0.4	V
I_I	Input leakage current	V_I = V_{CC} or GND	5.5			±0.1		±1		±1	µA
I_{CC}	Supply current	V_I = V_{CC} or GND	5.5			8		80		160	µA
ΔI_{CC}(1)	Additional supply current per input pin	One of A0 - A2 and $\overline{LE}$ inputs held at V_{CC} – 2.1	4.5 to 5.5		100	540		675		735	µA
		D input held at V_{CC} – 2.1	4.5 to 5.5		100	432		540		588	
		$\overline{MR}$ input held at V_{CC} – 2.1	4.5 to 5.5		100	270		337.5		367.5	

(1) V_I = V_{IH} or V_{IL}, unless otherwise noted.

5.5 Prerequisite for Switching Characteristics

PARAMETER		V_{CC} (V)	25°C			-40°C to 85°C			-55°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
HC TYPES												
t_{WL}	Pulse Width $\overline{G}$	2	70			90			105			ns
		4.5	14			18			21			
		5	12			15			18			
t_{WL}	$\overline{CLR}$	2	70			90			105			ns
		4.5	14			18			21			
		6	12			15			18			
t_{SU}	Setup time D to $\overline{G}$ S to $\overline{G}$	2	80			100			120			ns
		4.5	16			20			24			
		6	14			17			20			
t_H	Hold time D to $\overline{G}$ S to $\overline{G}$	2	0			0			0			ns
		4.5	0			0			0			
		6	0			0			0			
HCT TYPES												
t_{WL}	Pulse width $\overline{G}$ $\overline{CLR}$	4.5	18			23			27			ns
t_{SU}	Setup Time D to $\overline{G}$ S to $\overline{G}$	4.5	17			21			26			ns
t_H	Hold Time D to $\overline{G}$ S to $\overline{G}$	4.5	0			0			0			pF

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5.6 Switching Characteristics[2]

C_L = 50pF, Input t_t = 6ns

PARAMETER		V_{CC} (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
t_{pd}	D to Q	2			185		230		280	ns
		4.5		15[1]	37		46		56	
		6			31		39		48	
	$\overline{G}$ to Q	2			170		215		255	ns
		4.5		14[1]	34		43		51	
		6			29		37		43	
	S to Q	2			185		230		280	ns
		4.5		15[1]	37		46		56	
		6			31		39		48	
	$\overline{CLR}$ to Q	2			155		195		235	ns
		4.5		13[1]	31		39		47	
		6			26		33		40	
t_t	Output transition time	2			75		95		110	ns
		4.5			15		19		22	
		6			13		16		19	
C_{pd}	Power dissipation Capacitance[1]	5		21[1]						pF
C_i	Input capacitance		10		10		10		10	pF
HCT TYPES										
t_{pd}	D to Q	4.5		16[1]	39		49		59	ns
	$\overline{G}$ to Q	4.5		16[1]	38		48		57	ns
	S to Q	4.5		17[1]	41		51		61	ns
	$\overline{CLR}$ to Q	4.5		16[1]	39		49		59	pF
C_{pd}	Power dissipaction Capacitance[1]	5		22[1]						pF
C_i	Input Capacitance		10		10		10		10	pF
t_t	Output transition time	4.5			15		19		22	ns

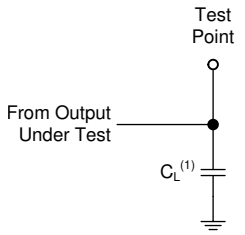
(1) C_L = 15pF and V_{CC} = 5 V.
(2) For details on CMOS power calculation see, SCAA053B.

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 6 ns.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1) C_L includes probe and test-fixture capacitance.

图 6-1. Load Circuit for Push-Pull Outputs

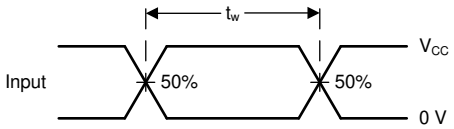


图 6-2. Voltage Waveforms, Standard CMOS Inputs Pulse Duration

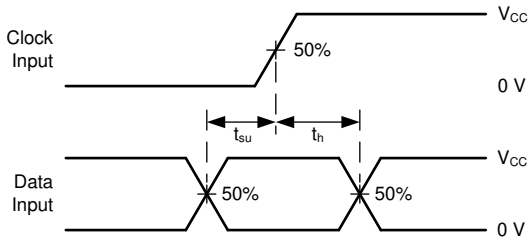
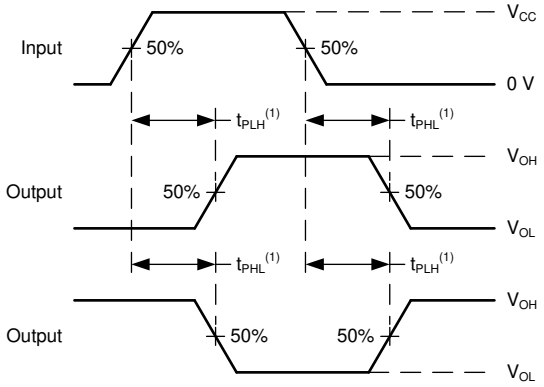
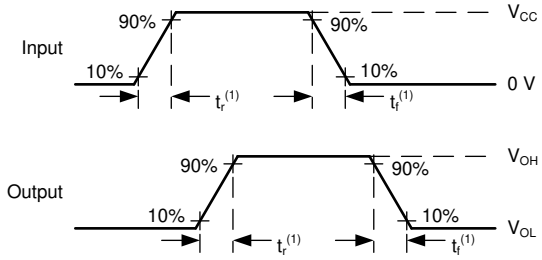


图 6-3. Voltage Waveforms, Standard CMOS Inputs Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

图 6-4. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs



(1) The greater between t_r and t_f is the same as t_t.

图 6-5. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs

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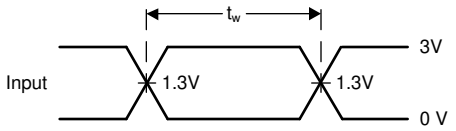


图 6-6. Voltage Waveforms, TTL-Compatible CMOS Inputs Pulse Duration

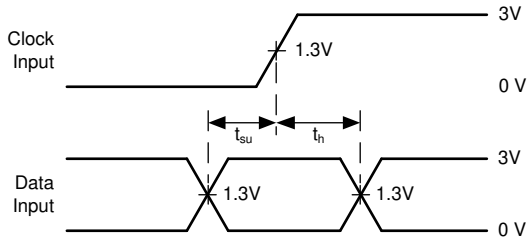
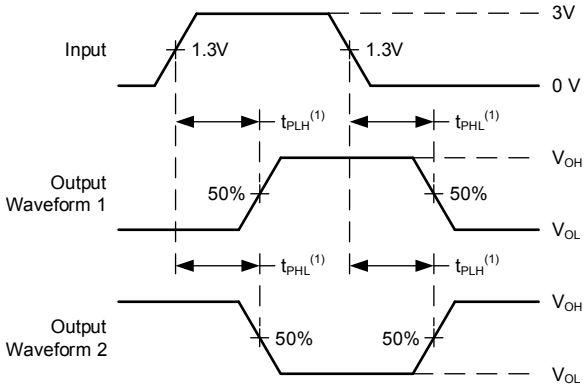


图 6-7. Voltage Waveforms, TTL-Compatible CMOS Inputs Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

图 6-8. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs

7 Detailed Description

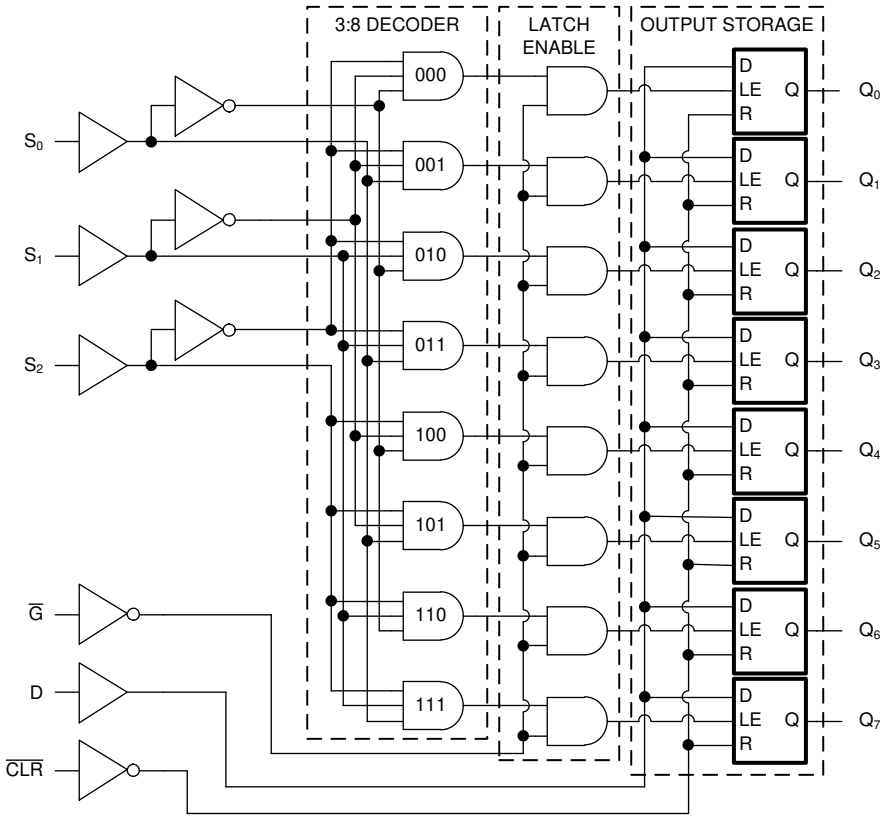
7.1 Overview

The CDx4HC(T)259 8-bit addressable latches are designed for general-purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches and being a 1-of-8 decoder or demultiplexer with active-high outputs.

Four distinct modes of operation are selectable by controlling the clear ($\overline{CLR}$) and enable ($\overline{G}$) inputs:

- Addressable-latch mode: $\overline{CLR}$ = HIGH; $\overline{G}$ = LOW
  - Data at the data-in terminal is written into the addressed latch
  - The addressed latch follows the data input, with all unaddressed latches remaining in their previous states
- Memory mode: $\overline{CLR}$ = HIGH; $\overline{G}$ = HIGH
  - All latches remain in their previous states and are unaffected by the data or address inputs
  - To eliminate the possibility of entering erroneous data in the latches, $\overline{G}$ should be held high (inactive) while the address lines are changing
- 1-of-8 decoding or demultiplexing mode: $\overline{CLR}$ = LOW; $\overline{G}$ = LOW
  - The addressed output follows the level of the D input with all other outputs low
- Clear mode: $\overline{CLR}$ = LOW; $\overline{G}$ = HIGH
  - All outputs are low and unaffected by the address and data inputs

7.2 Functional Block Diagram



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7.3 Device Functional Modes

The Function Tableand Latch Selection Table below list the functional modes of the CDx4HC(T)259.

表 7-1. Function Table

INPUTS[1]		OUTPUT OF ADDRESSED LATCH[2]	EACH OTHER OUTPUT[2]	FUNCTION
$\overline{CLR}$	$\overline{G}$			
H	L	D	Q_{iO}	Addressable latch
H	H	Q_{iO}	Q_{iO}	Memory
L	L	D	L	8-line demultiplexer
L	H	L	L	Clear

(1) H = High voltage level, L = Low voltage level
(2) Q_{iO} = Previous output state of selected latch, D = Data input logic value

表 7-2. Latch Selection Table

SELECT INPUTS[1]			LATCH ADDRESSED
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

(1) H = High Voltage Level, L = Low Voltage Level

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

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10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8985201EA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8985201EA CD54HCT259F3A	Samples
CD54HC259F3A	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8551901EA CD54HC259F3A	Samples
CD54HCT259F3A	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8985201EA CD54HCT259F3A	Samples
CD74HC259E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC259E	Samples
CD74HC259M	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC259M	Samples
CD74HC259M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	HC259M	Samples
CD74HC259MT	ACTIVE	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC259M	Samples
CD74HCT259E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT259E	Samples
CD74HCT259EE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT259E	Samples
CD74HCT259M	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT259M	Samples
CD74HCT259M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT259M	Samples
CD74HCT259M96E4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT259M	Samples
CD74HCT259MT	ACTIVE	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT259M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD54HC259, CD54HCT259, CD74HC259, CD74HCT259 :

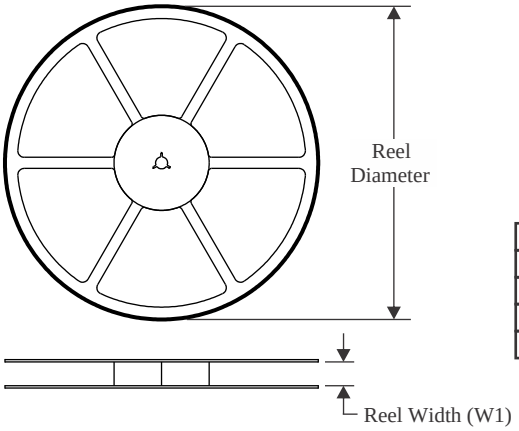
- Catalog : CD74HC259, CD74HCT259
- Military : CD54HC259, CD54HCT259

NOTE: Qualified Version Definitions:

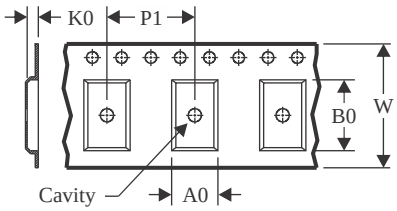
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

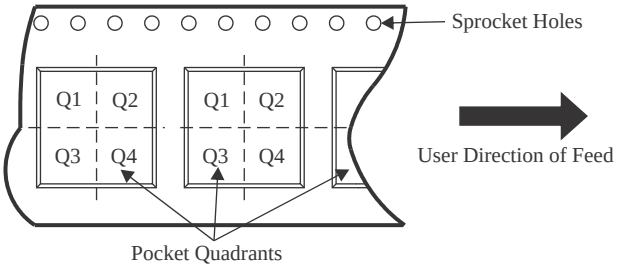


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

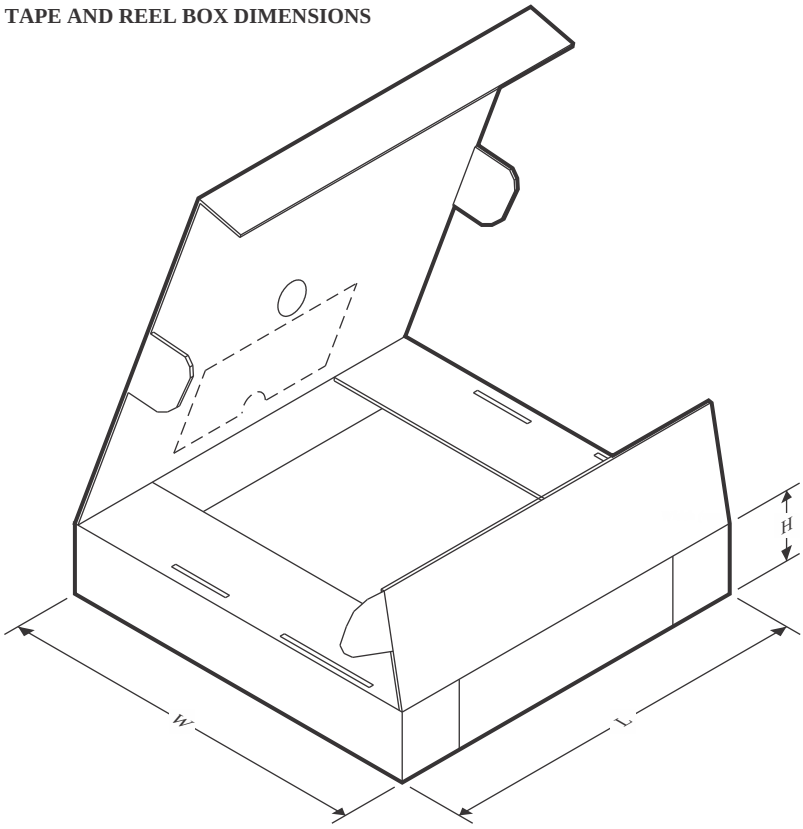
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC259M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC259M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC259M96	SOIC	D	16	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
CD74HCT259M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

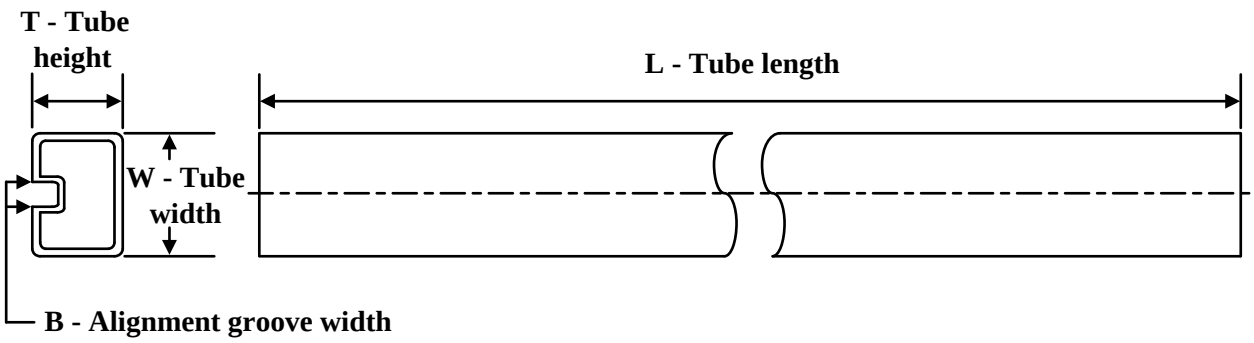
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC259M96	SOIC	D	16	2500	356.0	356.0	35.0
CD74HC259M96	SOIC	D	16	2500	340.5	336.1	32.0
CD74HC259M96	SOIC	D	16	2500	366.0	364.0	50.0
CD74HCT259M96	SOIC	D	16	2500	340.5	336.1	32.0

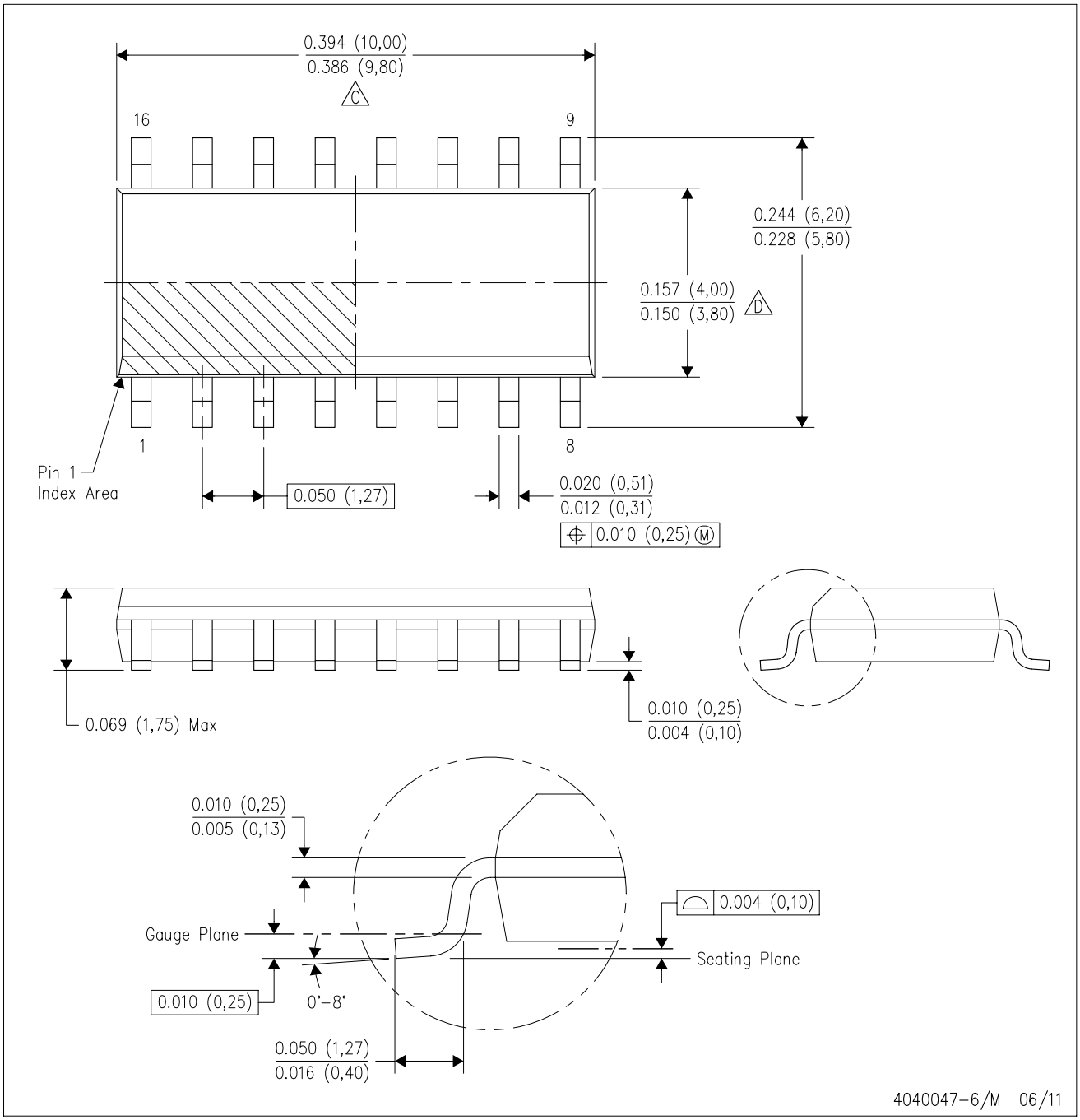
TUBE



*All dimensions are nominal

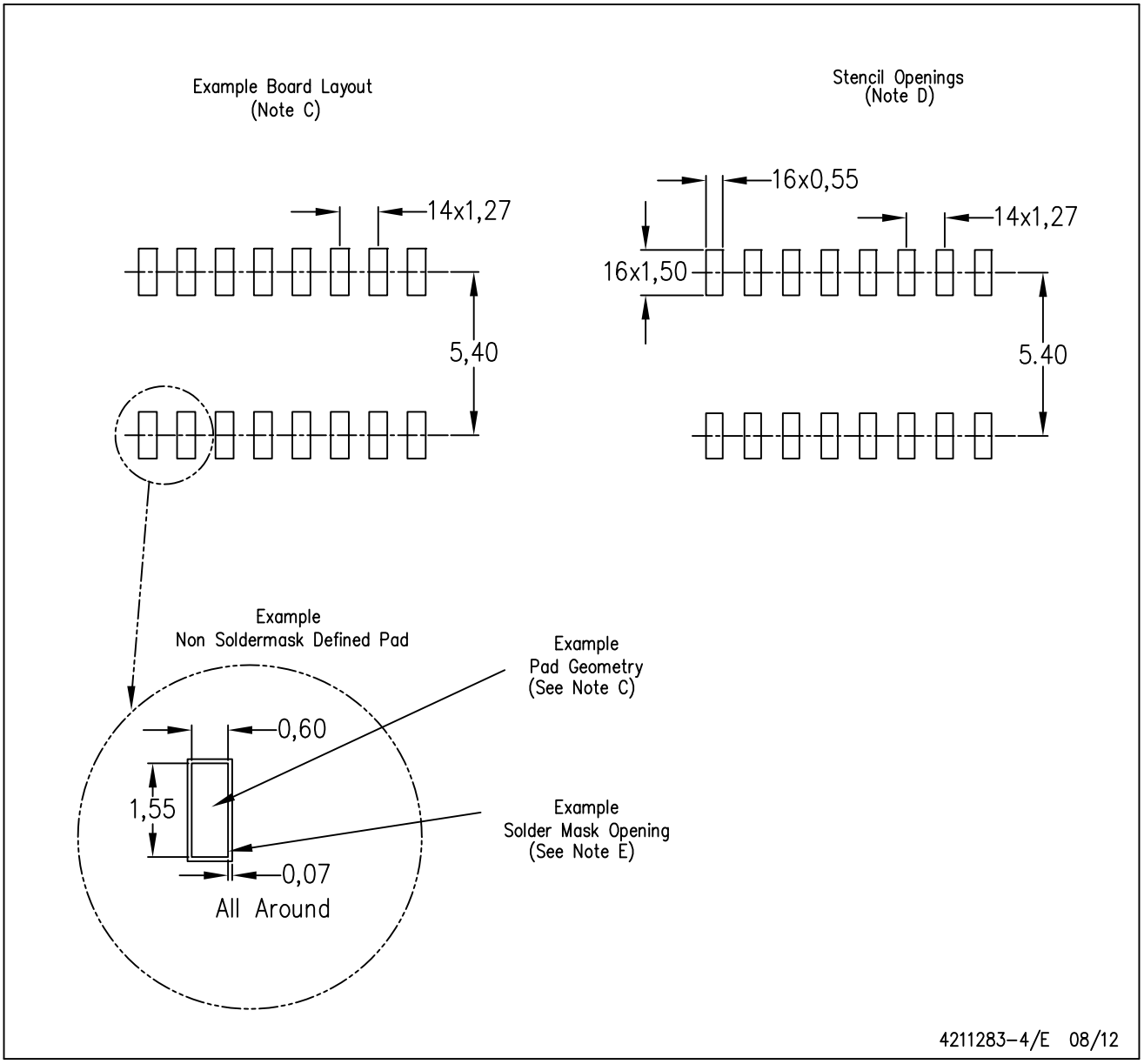
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC259E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC259E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC259M	D	SOIC	16	40	507	8	3940	4.32
CD74HCT259E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT259E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT259EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT259EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT259M	D	SOIC	16	40	507	8	3940	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

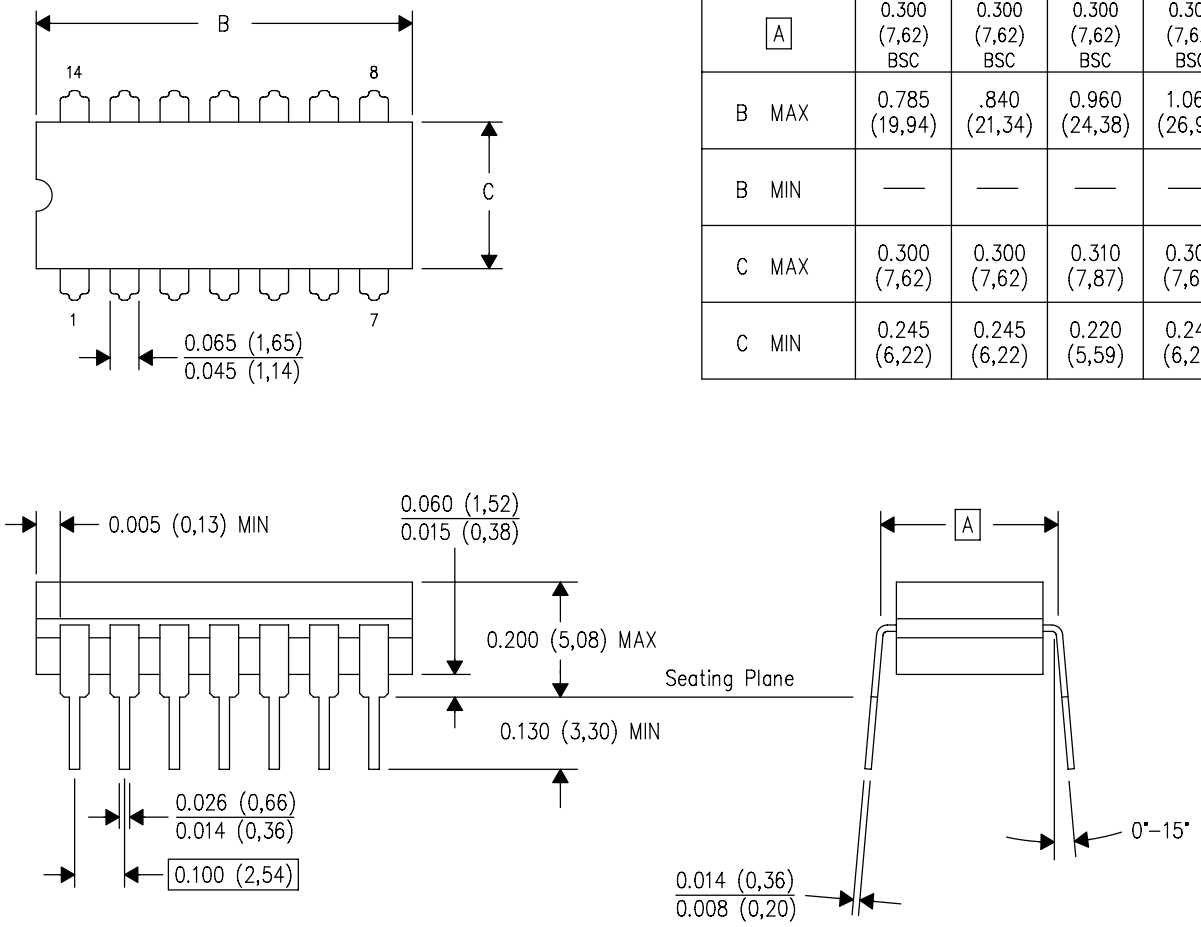
D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



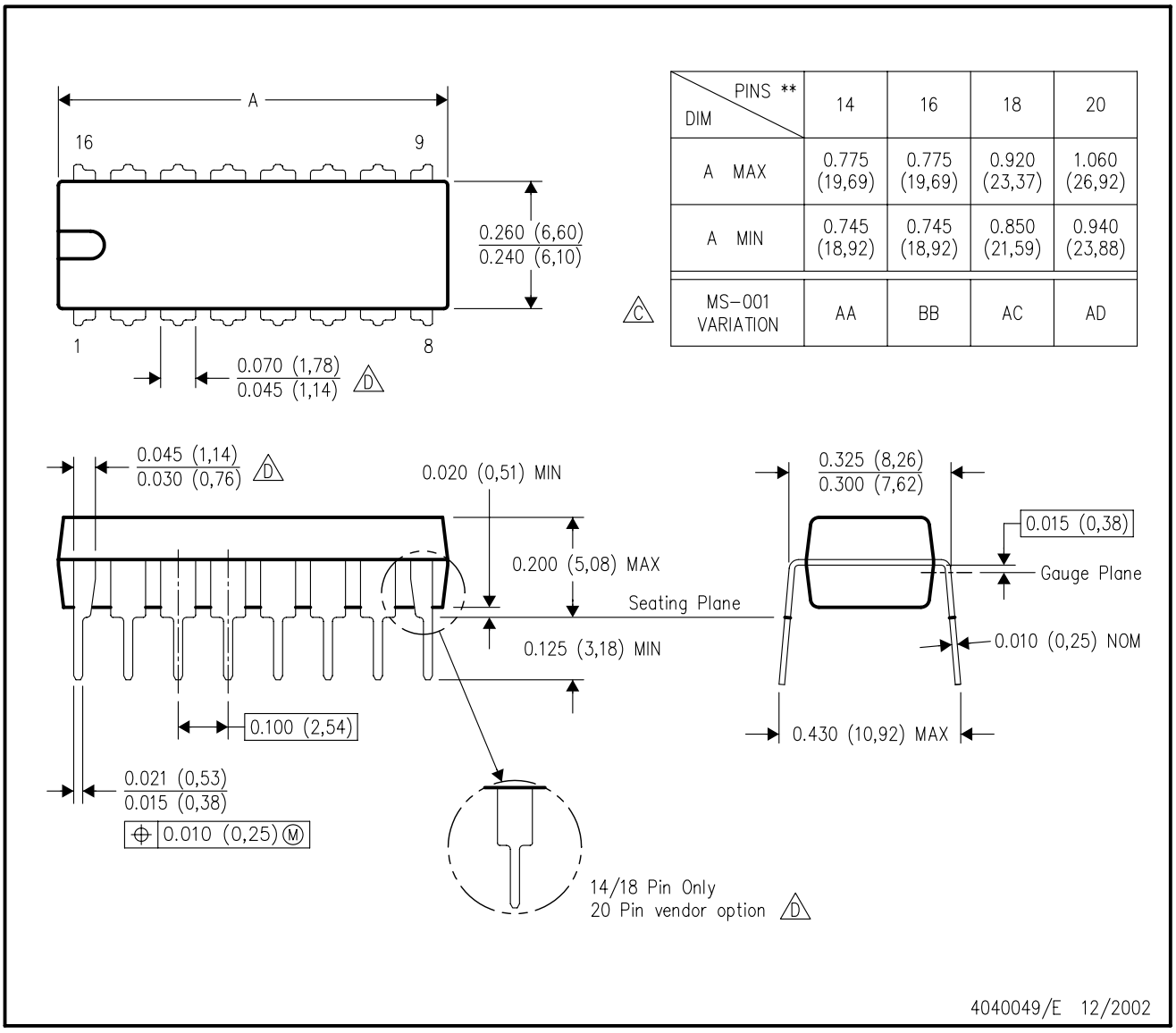
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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