

## High-Speed CMOS Logic Quad 2-Input Multiplexer with Three-State Non-Inverting Outputs

### Features

- Buffered Inputs
- Typical Propagation Delay ( In to Output ) = 12ns at  $V_{CC} = 5V$ ,  $C_L = 15pF$ ,  $T_A = 25^{\circ}C$
- Fanout (Over Temperature Range)
  - Standard Outputs ..... 10 LSTTL Loads
  - Bus Driver Outputs ..... 15 LSTTL Loads
- Wide Operating Temperature Range ...  $-55^{\circ}C$  to  $125^{\circ}C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Description

The 'HC257 and 'HCT257 are quad 2-input multiplexers which select four bits of data from two sources under the control of a common Select Input (S). The Output Enable input ( $\overline{OE}$ ) is active LOW. When  $\overline{OE}$  is HIGH, all of the outputs (1Y-4Y) are in the high impedance state regardless of

all other input conditions.

Moving data from two groups of registers to four common output buses is a common use of the 257. The state of the Select input determines the particular register from which the data comes. It can also be used as a function generator.

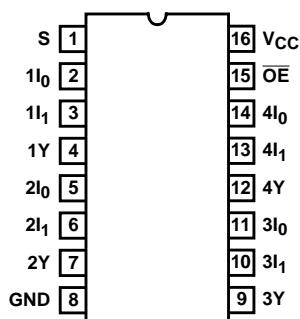
### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC257F3A	-55 to 125	16 Ld CERDIP
CD54HCT257F3A	-55 to 125	16 Ld CERDIP
CD74HC257E	-55 to 125	16 Ld PDIP
CD74HC257M	-55 to 125	16 Ld SOIC
CD74HC257MT	-55 to 125	16 Ld SOIC
CD74HC257M96	-55 to 125	16 Ld SOIC
CD74HCT257E	-55 to 125	16 Ld PDIP
CD74HCT257M	-55 to 125	16 Ld SOIC
CD74HCT257MT	-55 to 125	16 Ld SOIC
CD74HCT257M96	-55 to 125	16 Ld SOIC

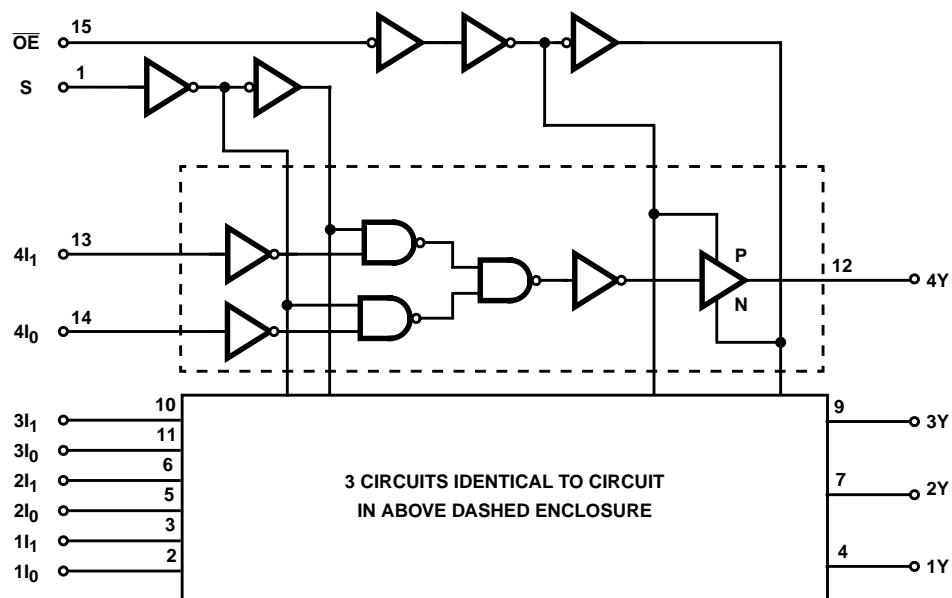
NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

### Pinout

**CD54HC257, CD54HCT257  
(CERDIP)  
CD74HC257, CD74HCT257  
(PDIP, SOIC)**  
TOP VIEW



**Functional Diagram**



**TRUTH TABLE**

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
		$l_0$	$l_1$	
$\overline{OE}$	$S$	X	X	Z
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H= High Voltage Level

L= Low Voltage Level

X= Don't Care

Z= High Impedance, OFF State

**Absolute Maximum Ratings**

DC Supply Voltage, $V_{CC}$	.....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$ For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	.....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$ For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	.....	$\pm 20mA$
DC Drain Current, per Output, $I_O$ For $-0.5V < V_O < V_{CC} + 0.5V$	.....	$\pm 35mA$
DC Output Source or Sink Current per Output Pin, $I_O$ For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	.....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$	.....	$\pm 70mA$

**Thermal Information**

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ ( $^{\circ}C/W$ )
E (PDIP) Package	67
M (SOIC) Package	73
Maximum Junction Temperature	150 $^{\circ}C$
Maximum Storage Temperature Range	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s)	300 $^{\circ}C$
(SOIC - Lead Tips Only)	

**Operating Conditions**

Temperature Range, $T_A$	.....	-55 $^{\circ}C$ to 125 $^{\circ}C$
Supply Voltage Range, $V_{CC}$	.....	
HC Types	.....	2V to 6V
HCT Types	.....	4.5V to 5.5V
DC Input or Output Voltage, $V_I, V_O$	.....	0V to $V_{CC}$
Input Rise and Fall Time	.....	
2V	.....	1000ns (Max)
4.5V	.....	500ns (Max)
6V	.....	400ns (Max)

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**NOTE:**

1. The package thermal impedance is calculated in accordance with JESD 51-7.

**DC Electrical Specifications**

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>												
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-6	4.5	3.98	-	-	3.84	-	3.7	-	V
			-7.8	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			6	4.5	-	-	0.26	-	0.33	-	0.4	V
			7.8	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	$I_I$	$V_{CC}$ or GND	-	6	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$

# CD54HC257, CD74HC257, CD54HCT257, CD74HCT257

## DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	6	-	-	8	-	80	-	160	µA
Three-State Leakage Current	I <sub>OZ</sub>	V <sub>IL</sub> or V <sub>IH</sub>	-	6	-	-	±0.5	-	±5	-	±10	µA
<b>HCT TYPES</b>												
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-6	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			6	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> to GND	0	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub> (Note 2)	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA
Three-State Leakage Current	I <sub>OZ</sub>	V <sub>IL</sub> or V <sub>IH</sub>	-	5.5	-	-	±0.5	-	±5	-	±10	µA

NOTE:

2. For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

## HCT Input Loading Table

INPUT	UNIT LOADS
Data	0.95
S	3
OE	0.6

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Specifications table, e.g., 360µA max at 25°C.

# CD54HC257, CD74HC257, CD54HCT257, CD74HCT257

## Switching Specifications Input $t_r, t_f = 6\text{ns}$

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
<b>HC TYPES</b>								
Propagation Delay In to Y	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	2	-	150	190	225	ns
			4.5	-	30	38	45	ns
		$C_L = 15\text{pF}$	5	12	-	-	-	ns
		$CL = 50\text{pF}$	6	-	26	33	38	ns
Propagation Delay S to Y	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	2	-	175	220	265	ns
			4.5	-	35	44	53	ns
		$C_L = 15\text{pF}$	5	14	-	-	-	ns
		$CL = 50\text{pF}$	6	-	30	37	45	ns
Propagation Delay $\overline{OE}$ to Y	$t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}$	$CL = 50\text{pF}$	2	-	150	190	225	ns
		$C_L = 50\text{pF}$	4.5	-	30	38	45	ns
		$C_L = 15\text{pF}$	5	12	-	-	-	ns
		$CL = 50\text{pF}$	6	-	26	33	38	ns
Output Transition Times	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	2	-	60	75	90	ns
			4.5	-	12	15	18	ns
			6	-	10	13	15	ns
Input Capacitance	$C_I$	-	-	-	10	10	10	pF
Three-State Output Capacitance	$C_O$	-	-	-	20	20	20	pF
Power Dissipation Capacitance (Notes 3, 4)	$C_{PD}$	-	5	45	-	-	-	pF
<b>HCT TYPES</b>								
Propagation Delay In to Y	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	33	41	50	ns
		$C_L = 15\text{pF}$	5	13	-	-	-	ns
Propagation Delay S to Y	$t_{PZL}, t_{PZH}$	$C_L = 50\text{pF}$	4.5	-	38	48	57	ns
		$C_L = 15\text{pF}$	5	12	-	-	-	ns
Propagation Delay $OE$ to Y	$t_{PLZ}, t_{PHZ}$	$C_L = 50\text{pF}$	4.5	-	30	38	45	ns
		$C_L = 15\text{pF}$	5	16	-	-	-	ns
Output Transition Times	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	4.5	-	12	15	18	ns
Input Capacitance	$C_I$	-	-	-	10	10	10	pF
Three-State Output Capacitance	$C_O$	-	-	-	20	20	20	pF
Power Dissipation Capacitance (Notes 3, 4)	$C_{PD}$	-	5	45	-	-	-	pF

### NOTES:

3.  $C_{PD}$  is used to determine the dynamic power consumption, per multiplexer.
4.  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = Input Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

## Test Circuits and Waveforms

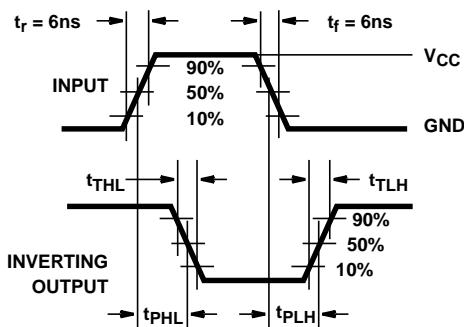


FIGURE 1. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

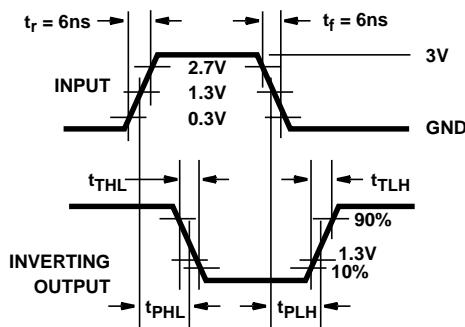


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

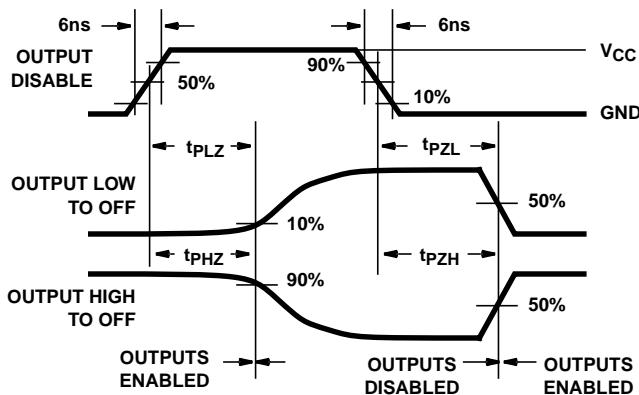


FIGURE 3. HC THREE-STATE PROPAGATION DELAY WAVEFORM

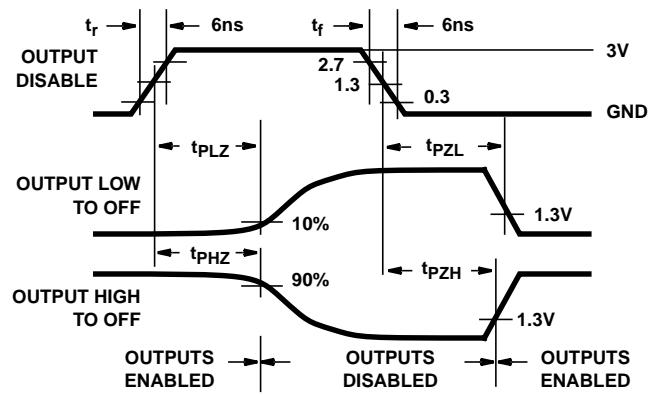
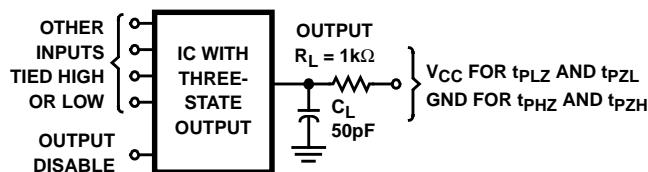


FIGURE 4. HCT THREE-STATE PROPAGATION DELAY WAVEFORM



NOTE: Open drain waveforms  $t_{PLZ}$  and  $t_{PZL}$  are the same as those for three-state shown on the left. The test circuit is Output  $R_L = 1k\Omega$  to  $V_{CC}$ ,  $C_L = 50pF$ .

FIGURE 5. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8970501EA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8970501EA CD54HCT257F3A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD54HC257F3A	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8512401EA CD54HC257F3A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD54HCT257F3A	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8970501EA CD54HCT257F3A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD74HC257E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC257E	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD74HC257M	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC257M	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD74HC257M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC257M	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD74HCT257E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT257E	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD74HCT257M	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT257M	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
CD74HCT257M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT257M	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF CD54HC257, CD54HCT257, CD74HC257, CD74HCT257 :**

- Catalog: [CD74HC257](#), [CD74HCT257](#)
- Military: [CD54HC257](#), [CD54HCT257](#)

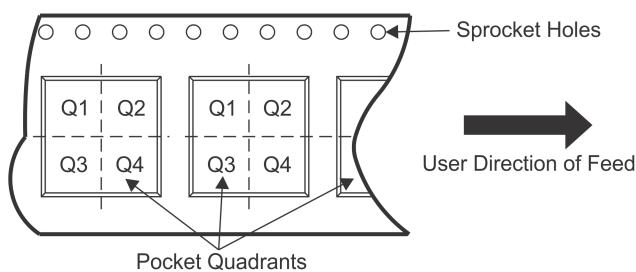
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

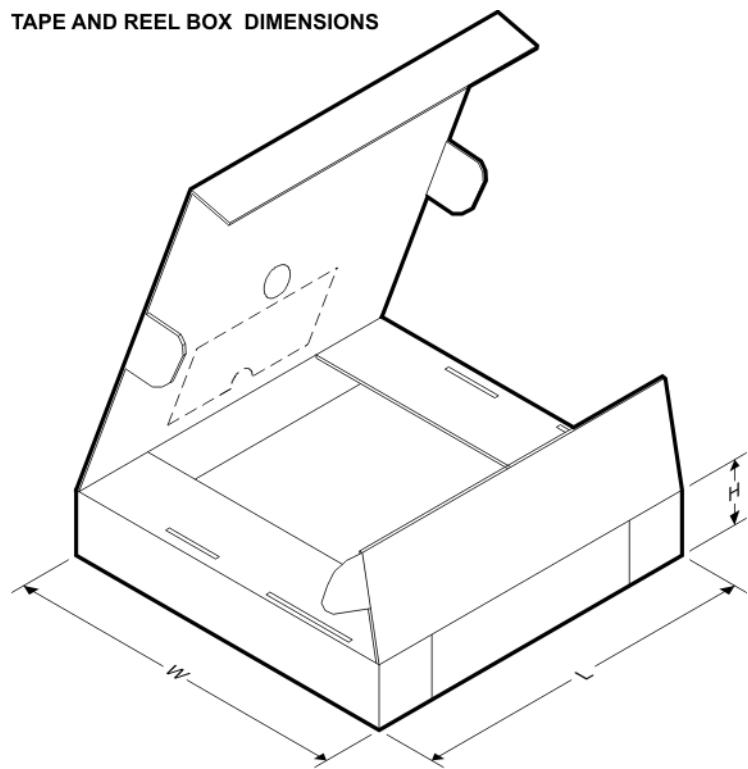
**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


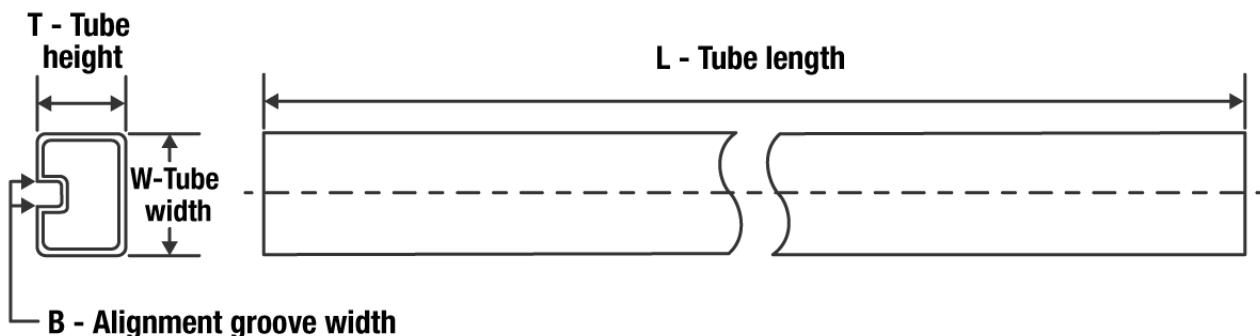
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC257M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT257M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC257M96	SOIC	D	16	2500	340.5	336.1	32.0
CD74HCT257M96	SOIC	D	16	2500	340.5	336.1	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC257E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC257E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC257M	D	SOIC	16	40	507	8	3940	4.32
CD74HCT257E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT257E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT257M	D	SOIC	16	40	507	8	3940	4.32

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

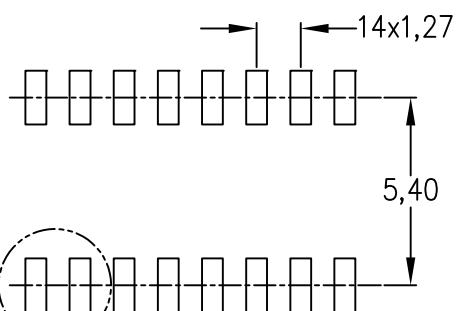
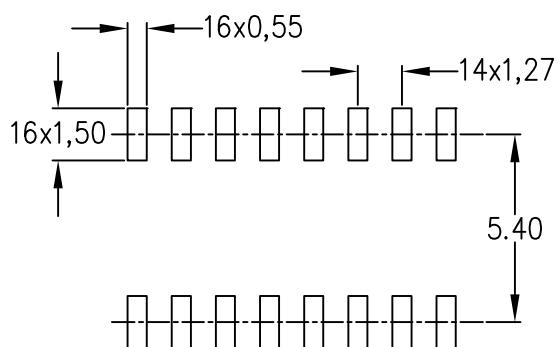
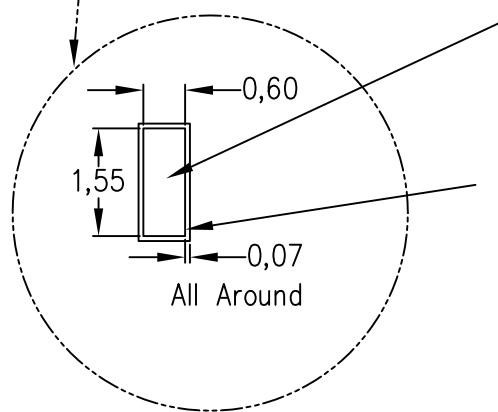
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)Example  
Non Soldermask Defined PadExample  
Pad Geometry  
(See Note C)Example  
Solder Mask Opening  
(See Note E)

4211283-4/E 08/12

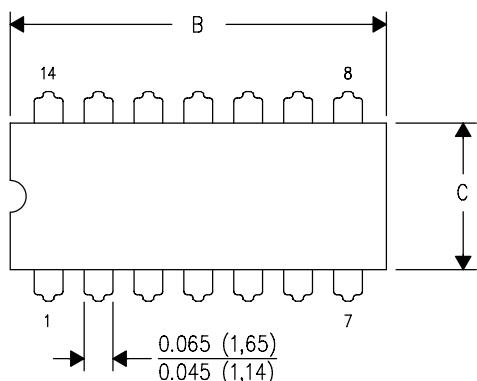
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

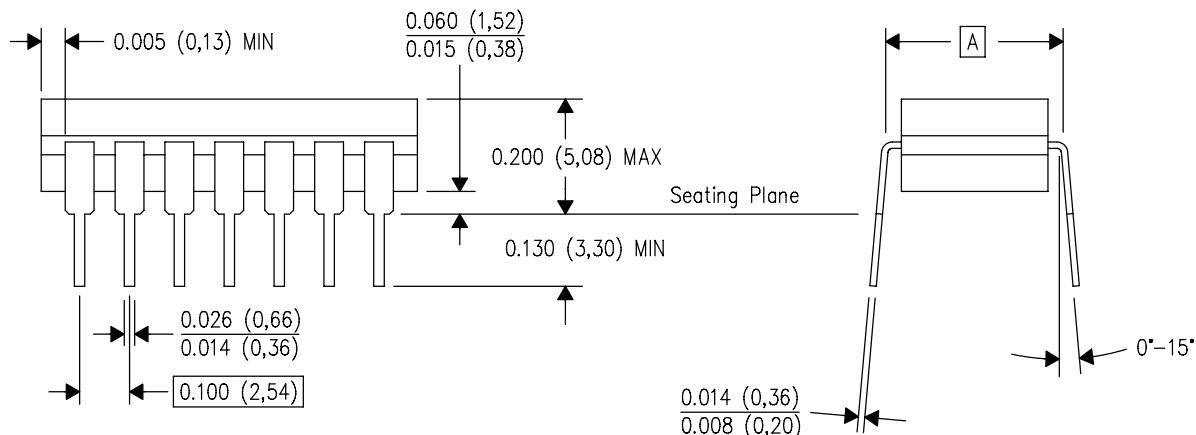
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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