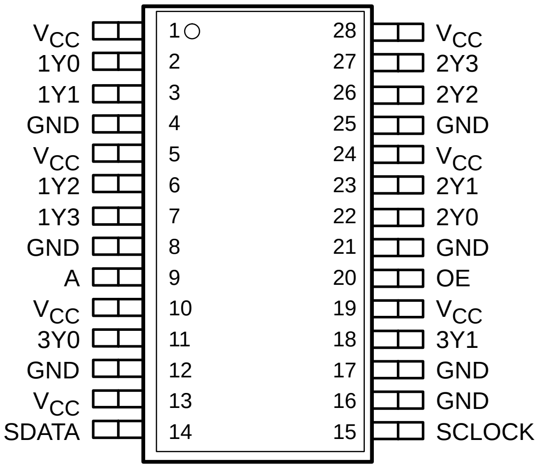
CDC319
1-LINE TO 10-LINE CLOCK DRIVER WITH I^{2}C CONTROL INTERFACE

SCAS590A – DECEMBER 1997 – REVISED OCTOBER 2001

- **High-Speed, Low-Skew 1-to-10 Clock Buffer for SDRAM (Synchronous DRAM) Clock Buffering Applications**
- **Output Skew, $t_{sk(o)}$, Less Than 250 ps**
- **Pulse Skew, $t_{sk(p)}$, Less Than 500 ps**
- **Supports up to Two Unbuffered SDRAM DIMMs (Dual Inline Memory Modules)**
- **I^{2}C Serial Interface Provides Individual Enable Control for Each Output**
- **Operates at 3.3 V**
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015**
- **Packaged in 28-Pin Shrink Small Outline (DB) Package**

DB PACKAGE
(TOP VIEW)



description

The CDC319 is a high-performance clock buffer that distributes one input (A) to 10 outputs (Y) with minimum skew for clock distribution. The CDC319 operates from a 3.3-V power supply, and is characterized for operation from 0°C to 70°C.

The device provides a standard mode (100K-bits/s) I^{2}C serial interface for device control. The implementation is as a slave/receiver. The device address is specified in the I^{2}C device address table. Both of the I^{2}C inputs (SDATA and SCLOCK) provide integrated pullup resistors (typically 140 kΩ) and are 5-V tolerant.

Three 8-bit I^{2}C registers provide individual enable control for each of the outputs. All outputs default to enabled at powerup. Each output can be placed in a disabled mode with a low-level output when a low-level control bit is written to the control register. The registers are write only and must be accessed in sequential order (i.e., random access of the registers is not supported).

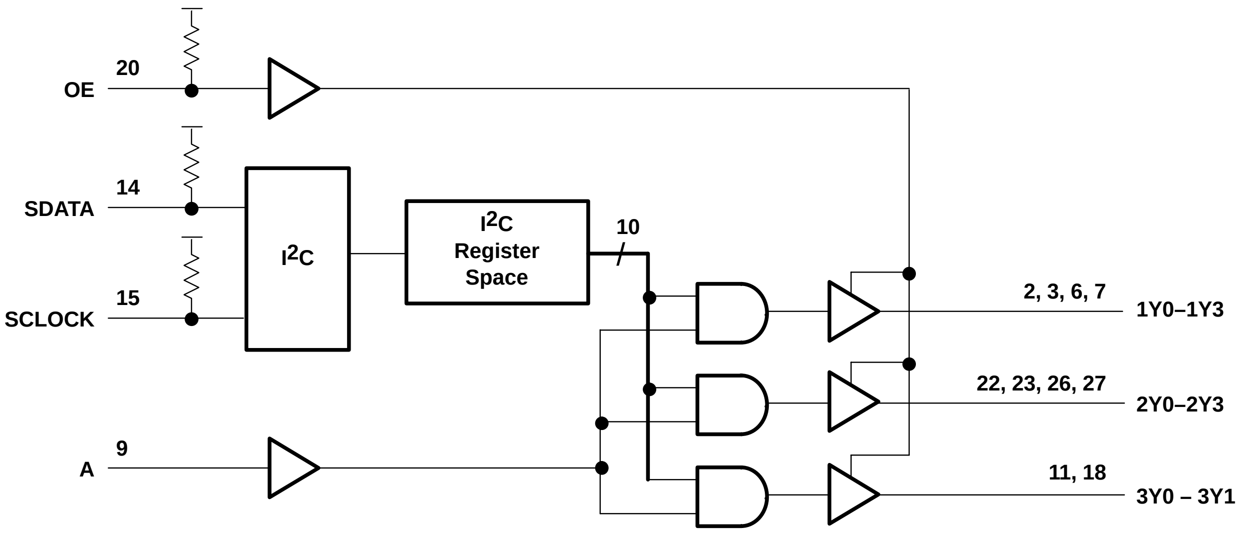
The CDC319 provides 3-state outputs for testing and debugging purposes. The outputs can be placed in a high-impedance state via the output-enable (OE) input. When OE is high, all outputs are in the operational state. When OE is low, the outputs are placed in a high-impedance state. OE provides an integrated pullup resistor.

FUNCTION TABLE

INPUTS		OUTPUTS		
OE	**A**	**1Y0–1Y3**	**2Y0–2Y3**	**3Y0–3Y1**
L	X	Hi-Z	Hi-Z	Hi-Z
H	L	L	L	L
H	H	H[†]	H[†]	H[†]

[†] The function table assumes that all outputs are enabled via the appropriate I^{2}C configuration register bit. If the output is disabled via the appropriate configuration bit, then the output is driven to a low state, regardless of the state of the A input.

logic diagram (positive logic)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
1Y0–1Y3	2, 3, 6, 7	O	3.3-V SDRAM byte 0 clock outputs
2Y0–2Y3	22, 23, 26, 27	O	3.3-V SDRAM byte 1 clock outputs
3Y0–3Y1	11, 18	O	3.3-V clock outputs provided for feedback control of external PLLs (phase-locked loops)
A	9	I	Clock input
OE	20	I	Output enable. When asserted, OE puts all outputs in a high-impedance state. A nominal 140-kΩ pullup resistor is internally integrated.
SCLOCK	15	I	I^{2}C serial clock input. A nominal 140-kΩ pullup resistor is internally integrated.
SDATA	14	I/O	Bidirectional I^{2}C serial data input/output. A nominal 140-kΩ pullup resistor is internally integrated.
GND	4, 8, 12, 16, 17, 21, 25		Ground
V_{CC}	1, 5, 10, 13, 19, 24, 28		3.3-V power supply

I²C DEVICE ADDRESS

A7	A6	A5	A4	A3	A2	A1	A0 (R/W)
H	H	L	H	L	L	H	—

I²C BYTE 0-BIT DEFINITION†

BIT	DEFINITION	DEFAULT VALUE
7	Reserved	H
6	Reserved	H
5	Reserved	H
4	Reserved	H
3	1Y3 enable (pin 7)	H
2	1Y2 enable (pin 6)	H
1	1Y1 enable (pin 3)	H
0	1Y0 enable (pin 2)	H

† When the value of the bit is high, the output is enabled. When the value of the bit is low, the output is forced to a low state. The default value of all bits is high.

I²C BYTE 1-BIT DEFINITION†

BIT	DEFINITION	DEFAULT VALUE
7	2Y3 enable (pin 27)	H
6	2Y2 enable (pin 26)	H
5	2Y1 enable (pin 23)	H
4	2Y0 enable (pin 22)	H
3	Reserved	H
2	Reserved	H
1	Reserved	H
0	Reserved	H

† When the value of the bit is high, the output is enabled. When the value of the bit is low, the output is forced to a low state. The default value of all bits is high.

I²C BYTE 2-BIT DEFINITION†

BIT	DEFINITION	DEFAULT VALUE
7	3Y1 enable (pin 18)	H
6	3Y0 enable (pin 11)	H
5	Reserved	H
4	Reserved	H
3	Reserved	H
2	Reserved	H
1	Reserved	H
0	Reserved	H

† When the value of the bit is high, the output is enabled. When the value of the bit is low, the output is forced to a low state. The default value of all bits is high.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 4.6 V
Input voltage range, V_I (SCLOCK, SDATA) (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V_O (SDATA) (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O	–0.5 V to V_{CC} + 0.5 V
Current into any output in the low state (except SDATA), I_O	48 mA
Current into SDATA in the low state, I_O	12 mA
Input clamp current, I_{IK} ($V_I < 0$) (SCLOCK)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$) (SDATA)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2)	120 °C/W
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

			MIN	TYP	MAX	UNIT
V_{CC}	3.3-V core supply voltage		3.135		3.465	V
V_{IH}	High-level input voltage	A, OE	2		V_{CC}+0.3	V
		SDATA, SCLOCK (see Note 3)	2.2		5.5	V
V_{IL}	Low-level input voltage	A, OE	–0.3		0.8	V
		SDATA, SCLOCK (see Note 3)	0		1.04	V
I_{OH}	High-level output current	Y outputs			– 24	mA
I_{OL}	Low-level output current	Y outputs			24	mA
R_I	Input resistance to V_{CC}	SDATA, SCLOCK (see Note 3)		140		kΩ
$f_{(SCL)}$	SCLOCK frequency				100	kHz
$t_{(BUS)}$	Bus free time		4.7			µs
$t_{su(START)}$	START setup time		4.7			µs
$t_{h(START)}$	START hold time		4			µs
$t_{w(SCLL)}$	SCLOCK low pulse duration		4.7			µs
$t_{w(SCLH)}$	SCLOCK high pulse duration		4			µs
$t_{r(SDATA)}$	SDATA input rise time				1000	ns
$t_{f(SDATA)}$	SDATA input fall time				300	ns
$t_{su(SDATA)}$	SDATA setup time		250			ns
$t_{h(SDATA)}$	SDATA hold time		0			ns
$t_{su(STOP)}$	STOP setup time		4			µs
T_A	Operating free-air temperature		0		70	°C

NOTE 3: The CMOS-level inputs fall within these limits: V_{IH} min = 0.7 × V_{CC} and V_{IL} max = 0.3 × V_{CC}.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

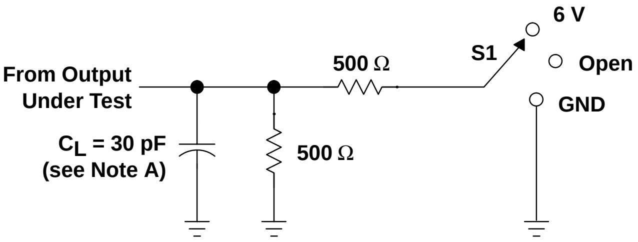
PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage		V_{CC} = 3.135 V,	I_I = –18 mA			–1.2	V
V_{OH}	High-level output voltage	Y outputs	V_{CC} = 3.135 V,	I_{OH} = –1 mA	2.4			V
V_{OL}	Low-level output voltage	Y outputs	V_{CC} = 3.135 V,	I_{OL} = 1 mA			0.4	V
		SDATA	V_{CC} = 3.135 V	I_{OL} = 3 mA	0.1		0.4	
				I_{OL} = 6 mA	0.2		0.6	
I_{OH}	High-level output current	SDATA	V_{CC} = 3.135 V,	V_O = V_{CC} MAX			20	µA
		Y outputs	V_{CC} = 3.135 V,	V_O = 2 V	–54		–126	mA
			V_{CC} = 3.3 V,	V_O = 2.6 V		–60		
			V_{CC} = 3.465 V,	V_O = 3.135 V	–21		–46	
I_{OL}	Low-level output current	Y outputs	V_{CC} = 3.135 V,	V_O = 1 V	49		118	mA
			V_{CC} = 3.3 V,	V_O = 0.7 V		58		
			V_{CC} = 3.465 V,	V_O = 0.4 V	23		53	
I_{IH}	High-level input current	A	V_{CC} = 3.465 V,	V_I = V_{CC}			5	µA
		OE					20	
		SCLOCK, SDATA					20	
I_{IL}	Low-level input current	A	V_{CC} = 3.465 V,	V_I = GND			–5	µA
		OE			–10		–50	
		SCLOCK, SDATA			–10		–50	
I_{OZ}	High-impedance-state output current		V_{CC} = 3.465 V,	V_O = 3.465 V or 0			±10	µA
I_{off}	Off-state current	SCLOCK, SDATA	V_{CC} = 0 V,	V_I = 0 V to 5.5 V			50	µA
I_{CC}	Supply current		V_{CC} = 3.465 V,	I_O = 0		0.2	0.5	mA
ΔI_{CC}	Change in supply current		V_{CC} = 3.135 V to 3.465 V, One input at V_{CC} – 0.6 V, All other inputs at V_{CC} or GND				500	µA
C_i	Input capacitiance		V_I = V_{CC} or GND,	V_{CC} = 3.3 V		4		pF
C_o	Output capacitance		V_O = V_{CC} or GND,	V_{CC} = 3.3 V		6		pF
$C_{I/O}$	SDATA I/O capacitance		$V_{I/O}$ = V_{CC} or GND,	V_{CC} = 3.3 V		7		pF

switching characteristics over recommended operating conditions

PARAMETER			FROM	TO	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Low-to-high level propagation delay time		A	Y		1.2	3.6	ns
			SCLOCK↓	SDATA valid	V_{CC} = 3.3 V ±0.185 V, See Figure 3		2	µs
t_{PLH}	Low-to-high level propagation delay time		SDATA↑	Y	V_{CC} = 3.3 V ±0.185 V, See Figure 3		150	ns
t_{PHL}	High-to-low level propagation delay time		A	Y		1.2	3.6	ns
			SCLOCK↓	SDATA valid	V_{CC} = 3.3 V ±0.185 V, See Figure 3		2	µs
t_{PHL}	High-to-low level propagation delay time		SDATA↑	Y	V_{CC} = 3.3 V ±0.185 V, See Figure 3		150	ns
t_{PZH}	Enable time to the high level		OE	Y		1	4.7	ns
t_{PZL}	Enable time to the low level							
t_{PHZ}	Disable time from the high level							
t_{PLZ}	Disable time from the low level							
$t_{sk(o)}$	Skew time		A	Y			250	ps
$t_{sk(p)}$	Skew time		A	Y			500	ps
$t_{sk(pr)}$	Skew time		A	Y			1	ns
t_r	Rise time			Y		0.5	1.3	ns
t_r	Rise time (see Note 4 and Figure 3)	SDATA			C_L = 10 pF	6		ns
					C_L = 400 pF		250	
t_f	Fall time			Y		0.5	1.3	ns
t_f	Fall time (see Note 4 and Figure 3)	SDATA			C_L = 10 pF	20		ns
					C_L = 400 pF		250	
f	Operating frequency (see Note 5)				C_L = 30 pF, T_A = 70°C		100	MHz
					C_L = 20 pF, T_A = 70°C		125	
					C_L = 15 pF, T_A = 70°C		140	

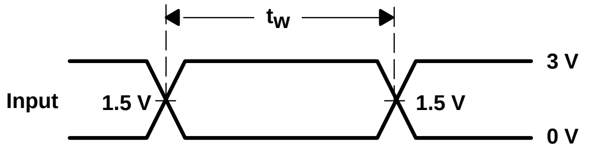
NOTES: 4. This parameter has a lower limit than BUS specification. This allows use of series resistors for current spike protection.
5. See Figure 4 (Frequency versus Capacitive Load).

PARAMETER MEASUREMENT INFORMATION

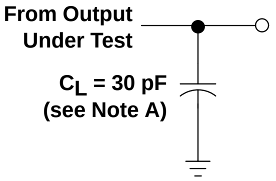


LOAD CIRCUIT FOR t_{pd} AND t_{sk}

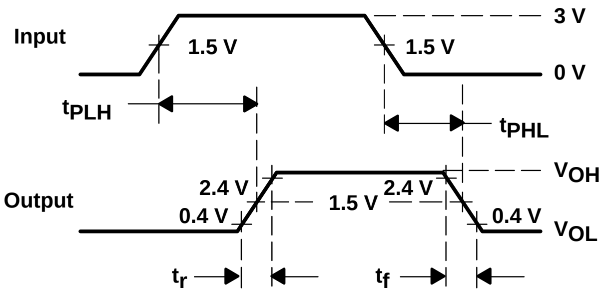
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



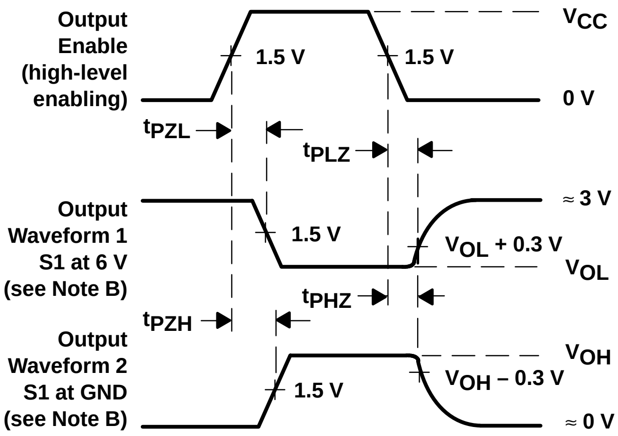
VOLTAGE WAVEFORMS



LOAD CIRCUIT FOR t_r AND t_f



VOLTAGE WAVEFORMS

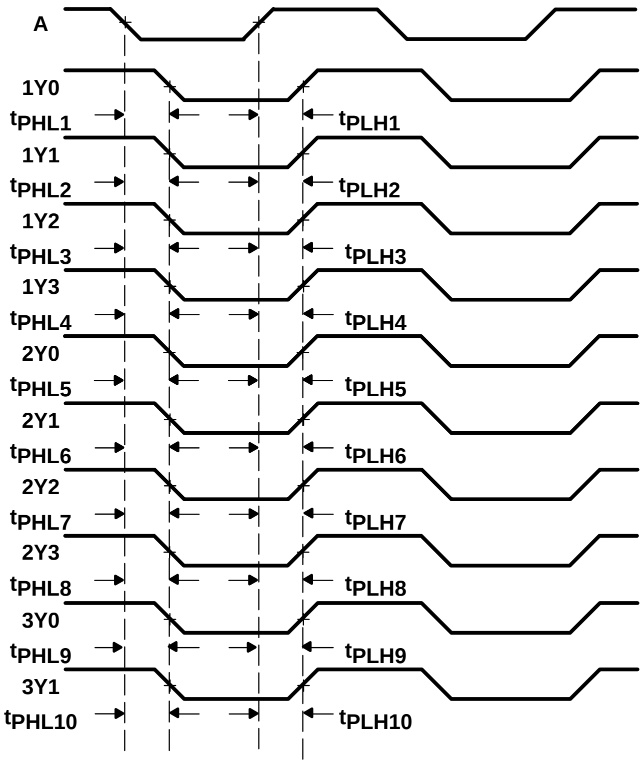


VOLTAGE WAVEFORMS

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



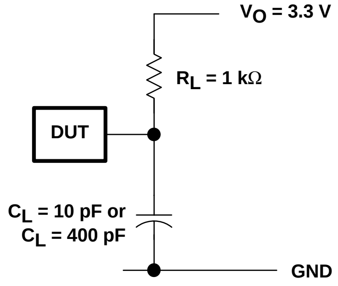
NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1:10)
- The difference between the fastest and slowest of t_{PHLn} (n = 1:10)

B. Pulse skew, $t_{sk(p)}$, is calculated as the greater of $|t_{PLHn} – t_{PHLn}|$ (n = 1:10).

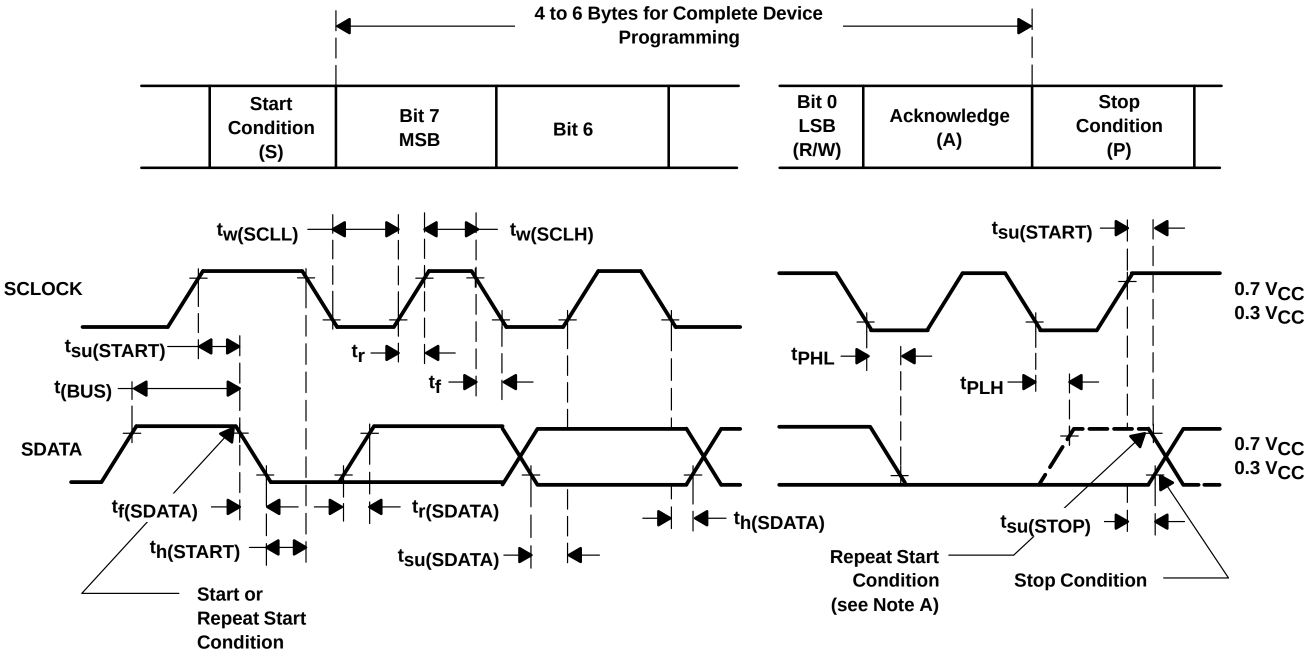
C. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1:10) across multiple devices under identical operating conditions
- The difference between the fastest and slowest of t_{PHLn} (n = 1:10) across multiple devices under identical operating conditions

Figure 2. Waveforms for Calculation of $t_{sk(o)}$, $t_{sk(p)}$, $t_{sk(pr)}$

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



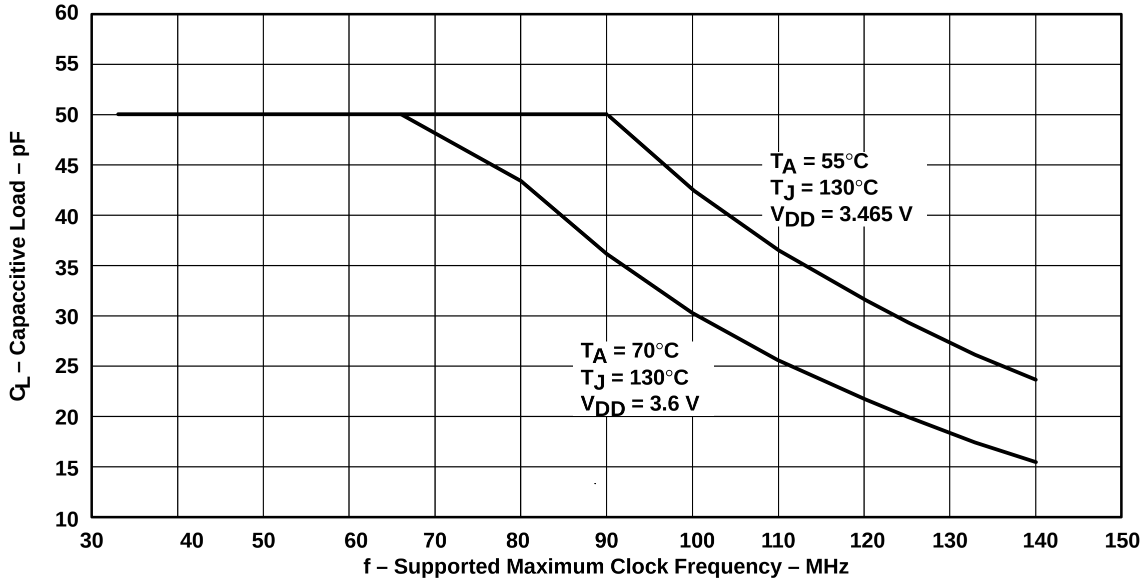
VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I²C address
2	Command (dummy value, ignored)
3	Byte count (dummy value, ignored)
4	I²C data byte 0
5	I²C data byte 1
6	I²C data byte 2

NOTES: A. The repeat start condition is not supported.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 100 kHz, Z_O = 50 Ω, t_r ≥ 10 ns, t_f ≥ 10 ns.

Figure 3. Propagation Delay Times, t_r and t_f

CAPACITIVE LOAD
vs
SUPPORTED MAXIMUM CLOCK FREQUENCY



NOTES: A. With a total capacitive load of 20 pF for each output, the CDC319 is capable of running up to about 125 MHz. A lower capacitive load will allow higher application frequencies, up to 133 MHz (140 MHz).

B. CPD for the CDC319 is about 25 pF per output (21 pF if C_L < 20 pF)

$P(\text{total}) = VDD^2 \times CPD \times F_O \times N + (V_{OH} - V_{OL})^2 \times C_L \times F_O \times N + \text{DC load}$

where:

N = number of switching outputs

F_O = clock frequency

Package thermal impedance (junction-to-ambient) = 92.4°C/W

Maximum junction temperature = 150°C (<125°C recommended)

Figure 4

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDC319DB	ACTIVE	SSOP	DB	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CDC319	Samples
CDC319DBR	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CDC319	Samples
CDC319DBRG4	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CDC319	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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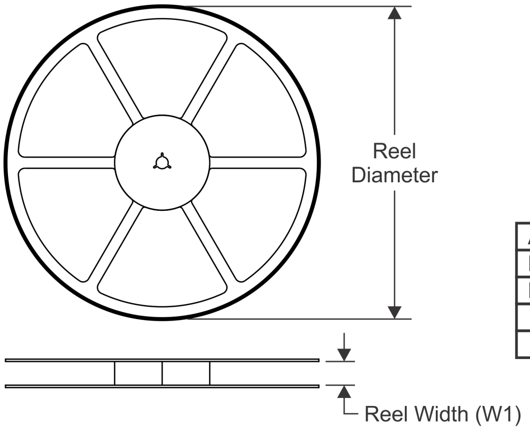
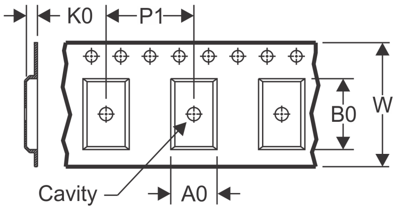
TAPE AND REEL INFORMATION

REEL DIMENSIONS

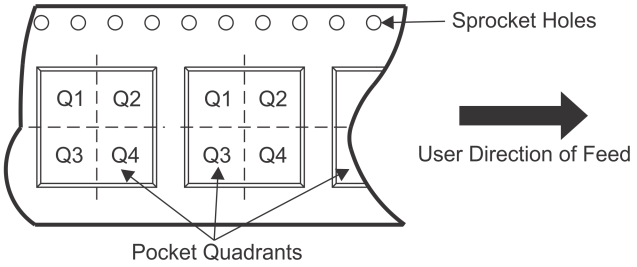


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

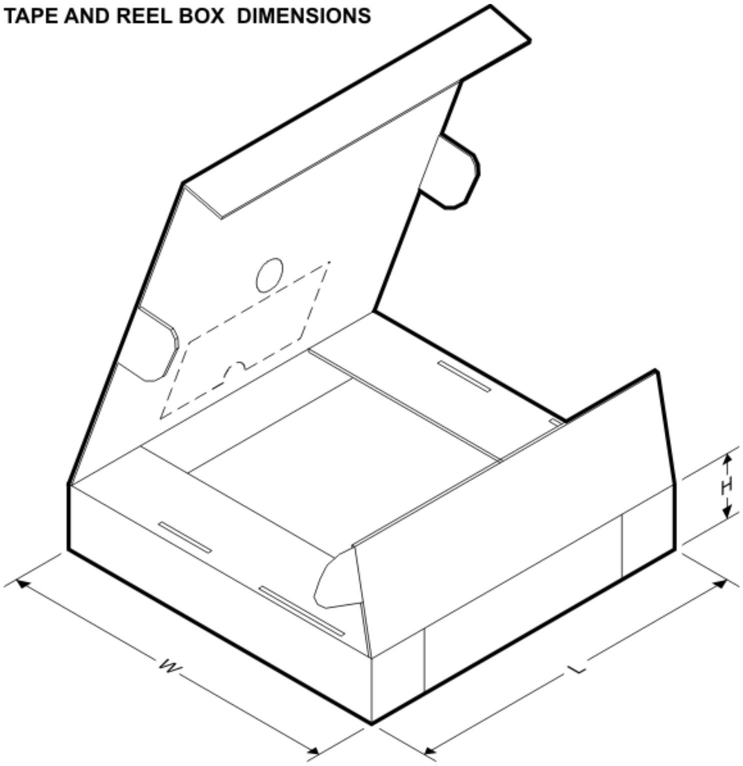
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC319DBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

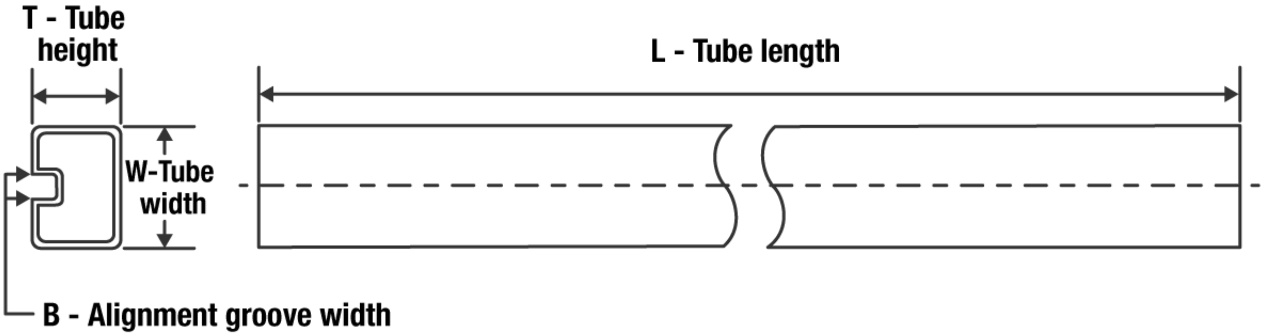
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC319DBR	SSOP	DB	28	2000	853.0	449.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CDC319DB	DB	SSOP	28	50	530	10.5	4000	4.1

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