CSD22206W -8V P 通道 NexFET™功率金属氧化物半导体场效应晶体管 (MOSFET)

1 特性

- 超低电阻
- 小尺寸封装 1.5mm x 1.5mm
- 无铅
- 栅极静电放电 (ESD) 保护
- 符合 RoHS 环保标准
- 无卤素
- 栅 - 源电压钳位

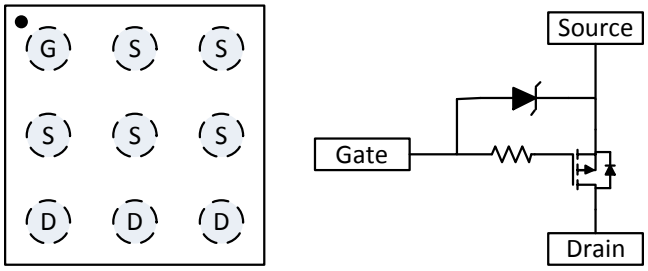
2 应用范围

- 负载开关 应用范围
- 电池管理
- 电池保护

3 说明

这款 –8V、4.7mΩ、1.5mm × 1.5mm 器件设计用于在超薄且具有出色散热特性的超小外形尺寸封装内提供最低的导通电阻和栅极电荷。低导通电阻与小型封装尺寸和低高度结合在一起，使得此器件非常适合于电池供电运行的空间受限 应用。

顶视图和电路配置



产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	-8		V
Q_g	栅极电荷总量 (-4.5V)	11.2		nC
Q_{gd}	栅极电荷（栅极到漏极）	1.8		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = -2.5V	6.8	mΩ
		V_{GS} = -4.5V	4.7	
$V_{GS(th)}$	阈值电压	-0.7		V

器件信息

器件	数量	包装介质	封装	运输
CSD22206W	3000	7 英寸卷带	1.50mm × 1.50mm 晶圆级球状引脚栅格阵列 (BGA) 封装	卷带封装
CSD22206WT	250			

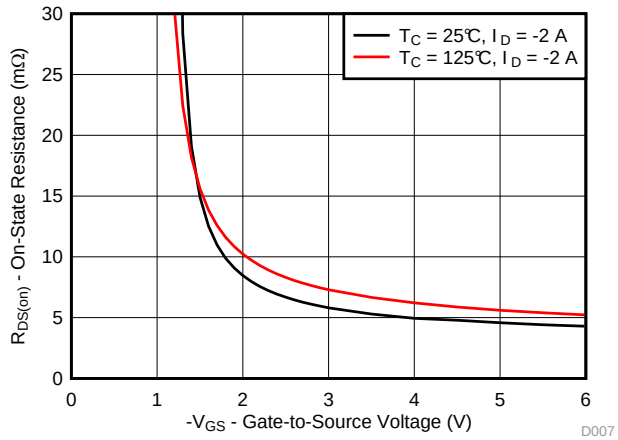
绝对最大额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	-8	V
V_{GS}	栅源电压	-6	V
I_D	持续漏极电流(1)	-5	A
	脉冲漏极电流(2)	–108	A
P_D	功率耗散	1.7	W
T_J, T_{stg}	工作结温，储存温度	-55 至 150	°C

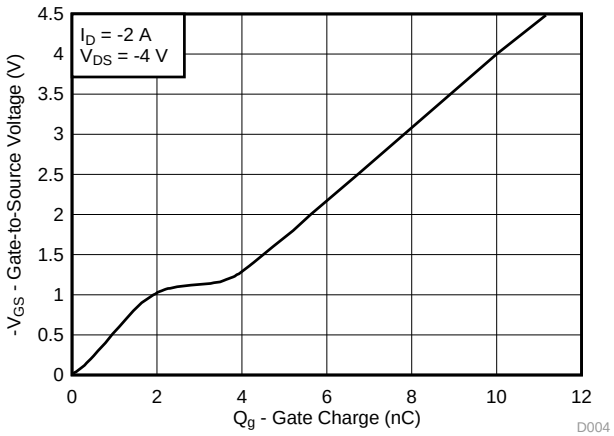
(1) 器件在 105ºC 温度下运行.

(2) 典型 $R_{\theta JA}$ = 75°C/W（安装于具有最大铜安装区域的 FR4 材料），脉宽 ≤ 100µs，占空比 ≤ 1%。

$R_{DS(on)}$ 与 V_{GS} 对比



栅极电荷



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 修订历史记录

日期	修订版本	注释
2017 年 5 月	*	初始发行版。

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5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = –250 μA	–8			V
BV_{GSS}	Gate-to-source voltage	V_{DS} = 0 V, I_G = –250 μA	–6			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = –6.4 V			–1	μA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = –6 V			–100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = –250 μA	–0.4	–0.7	–1.05	V
$R_{DS(on)}$	Drain-to-source on resistance	V_{GS} = –2.5 V, I_{DS} = –2 A		6.8	9.1	mΩ
		V_{GS} = –4.5 V, I_{DS} = –2 A		4.7	5.7	
g_{fs}	Transconductance	V_{DS} = –0.8 V, I_{DS} = –2 A		20		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input capacitance	V_{GS} = 0 V, V_{DS} = –4 V, f = 1 MHz		1750	2275	pF
C_{OSS}	Output capacitance			960	1250	pF
C_{RSS}	Reverse transfer capacitance			340	440	pF
R_G	Series gate resistance			30		Ω
Q_g	Gate charge total (–4.5 V)	V_{DS} = –4 V, I_D = –2 A		11.2	14.6	nC
Q_{gd}	Gate charge gate-to-drain			1.8		nC
Q_{gs}	Gate charge gate-to-source			2.1		nC
$Q_{g(th)}$	Gate charge at Vth			1.3		nC
Q_{OSS}	Output charge	V_{DS} = –4 V, V_{GS} = 0 V		7.2		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = –4 V, V_{GS} = –4.5 V, I_{DS} = –2 A, R_G = 0 Ω		37		ns
t_r	Rise time			17		ns
$t_{d(off)}$	Turnoff delay time			118		ns
t_f	Fall time			45		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{DS} = –2 A, V_{GS} = 0 V		–0.69	–1.0	
Q_{rr}	Reverse recovery charge	V_{DS}= –4 V, I_F = –1 A, di/dt = 200 A/μs		24		nC
t_{rr}	Reverse recovery time			59		ns

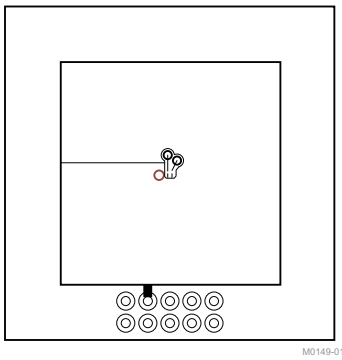
5.2 Thermal Information

T_A = 25°C (unless otherwise stated)

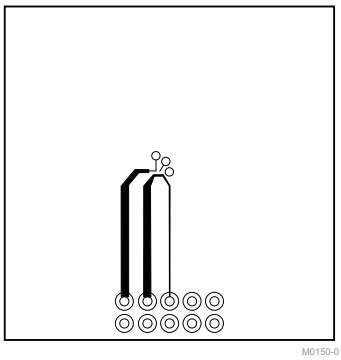
THERMAL METRIC		TYPICAL VALUES	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	75	°C/W
	Junction-to-ambient thermal resistance(2)	230	

(1) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

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Typ $R_{\theta JA}$ = 75°C/W when mounted on 1 in^2 of 2-oz Cu.



Typ $R_{\theta JA}$ = 230°C/W when mounted on minimum pad area of 2-oz Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

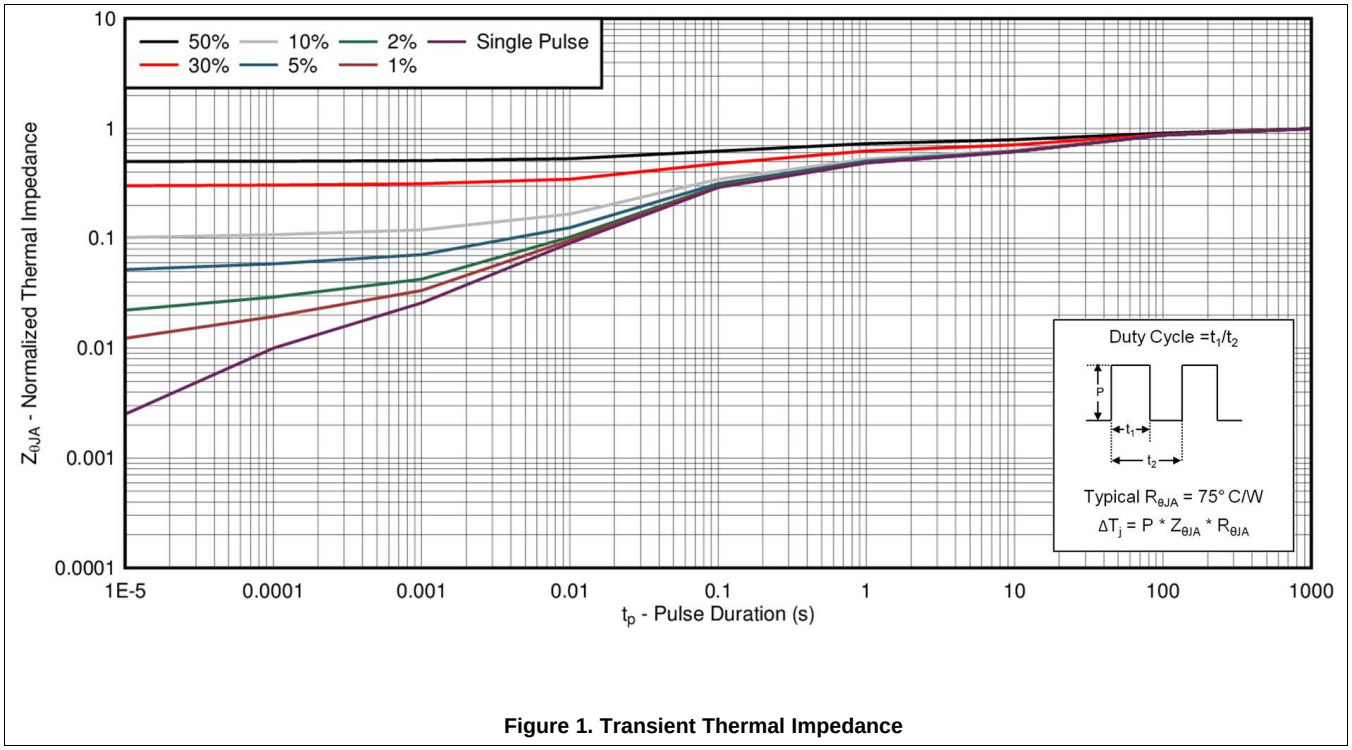


Figure 1. Transient Thermal Impedance

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Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

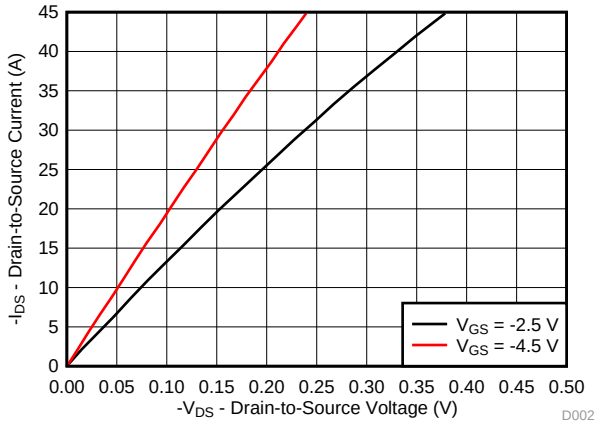
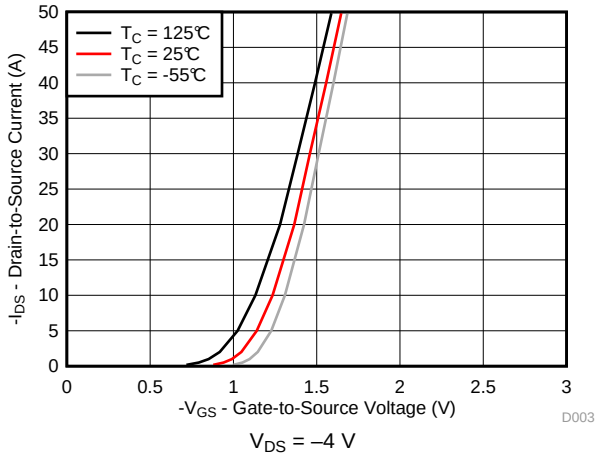
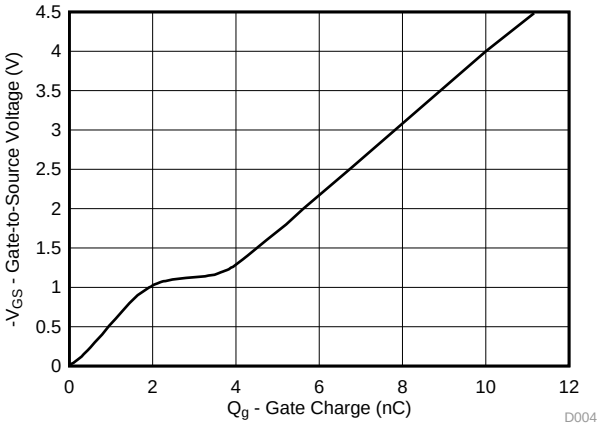


Figure 2. Saturation Characteristics



VDS = –4 V

Figure 3. Transfer Characteristics



ID = –2 A VDS = –4 V

Figure 4. Gate Charge

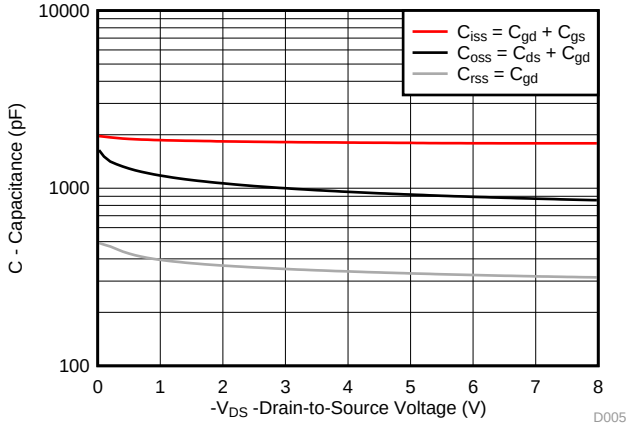
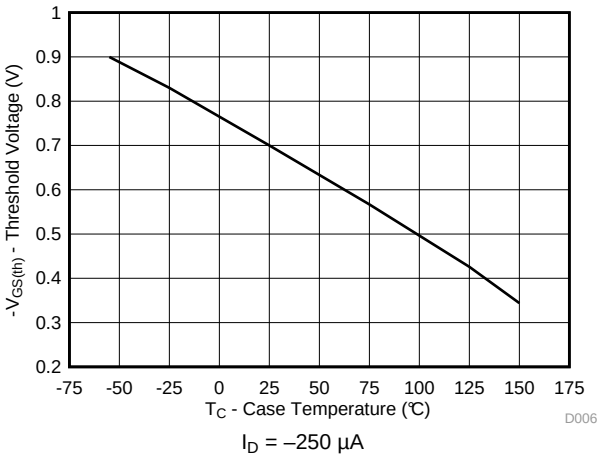


Figure 5. Capacitance



ID = –250 µA

Figure 6. Threshold Voltage vs Temperature

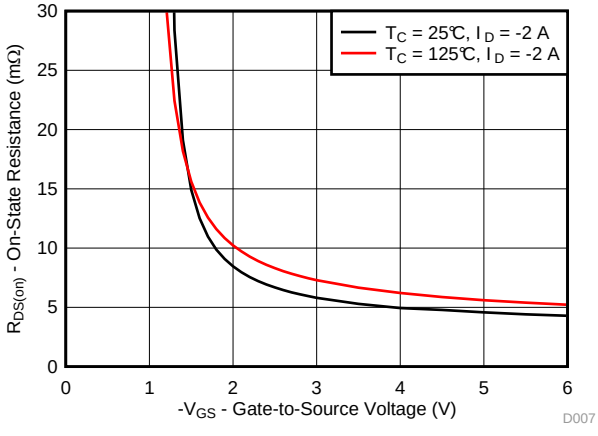


Figure 7. On-State Resistance vs Gate-to-Source Voltage

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Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

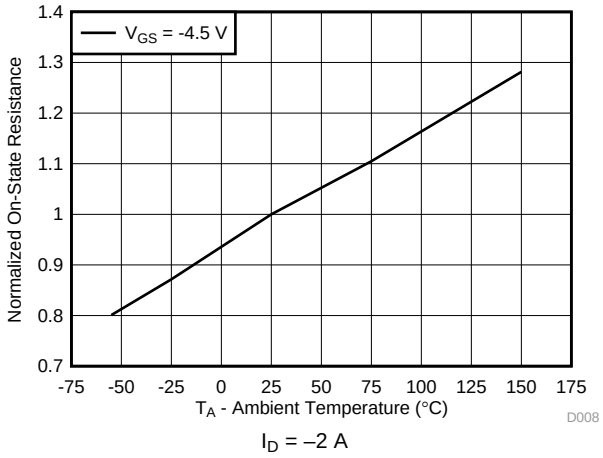


Figure 8. Normalized On-State Resistance vs Temperature

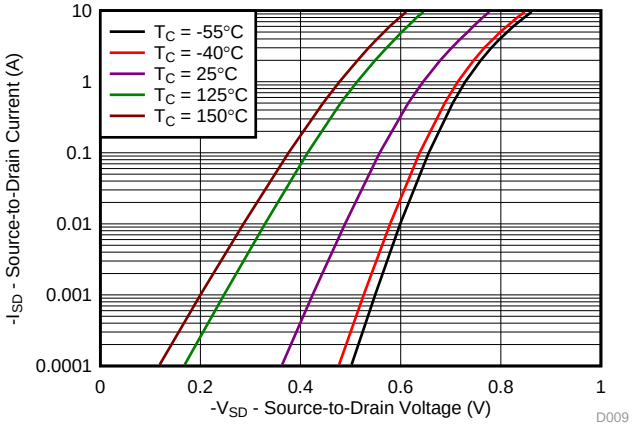


Figure 9. Typical Diode Forward Voltage

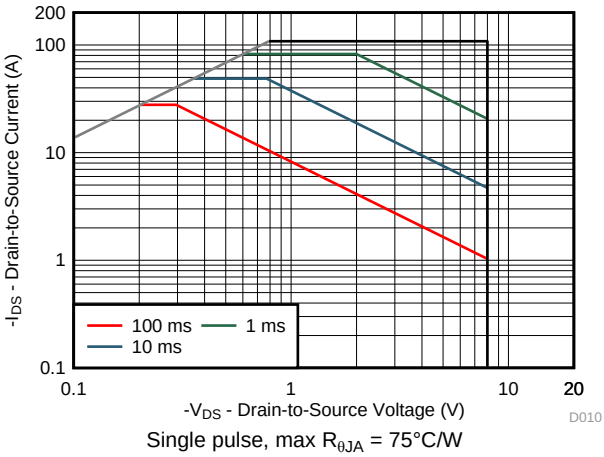


Figure 10. Maximum Safe Operating Area

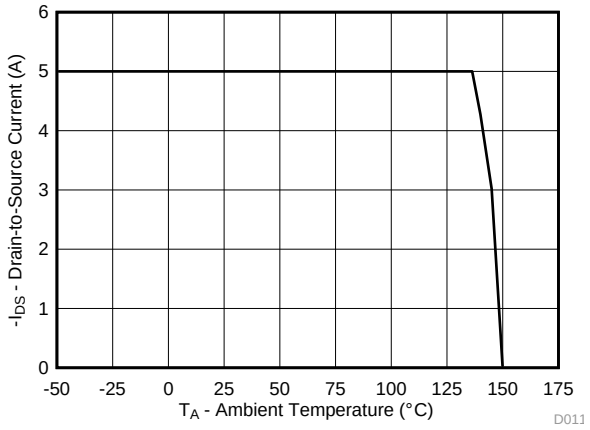


Figure 11. Maximum Drain Current vs Temperature

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6 器件和文档支持

6.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。请单击右上角的*通知我* 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

6.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 商标

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6.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.5 Glossary

SLYZ022 — *TI Glossary*.

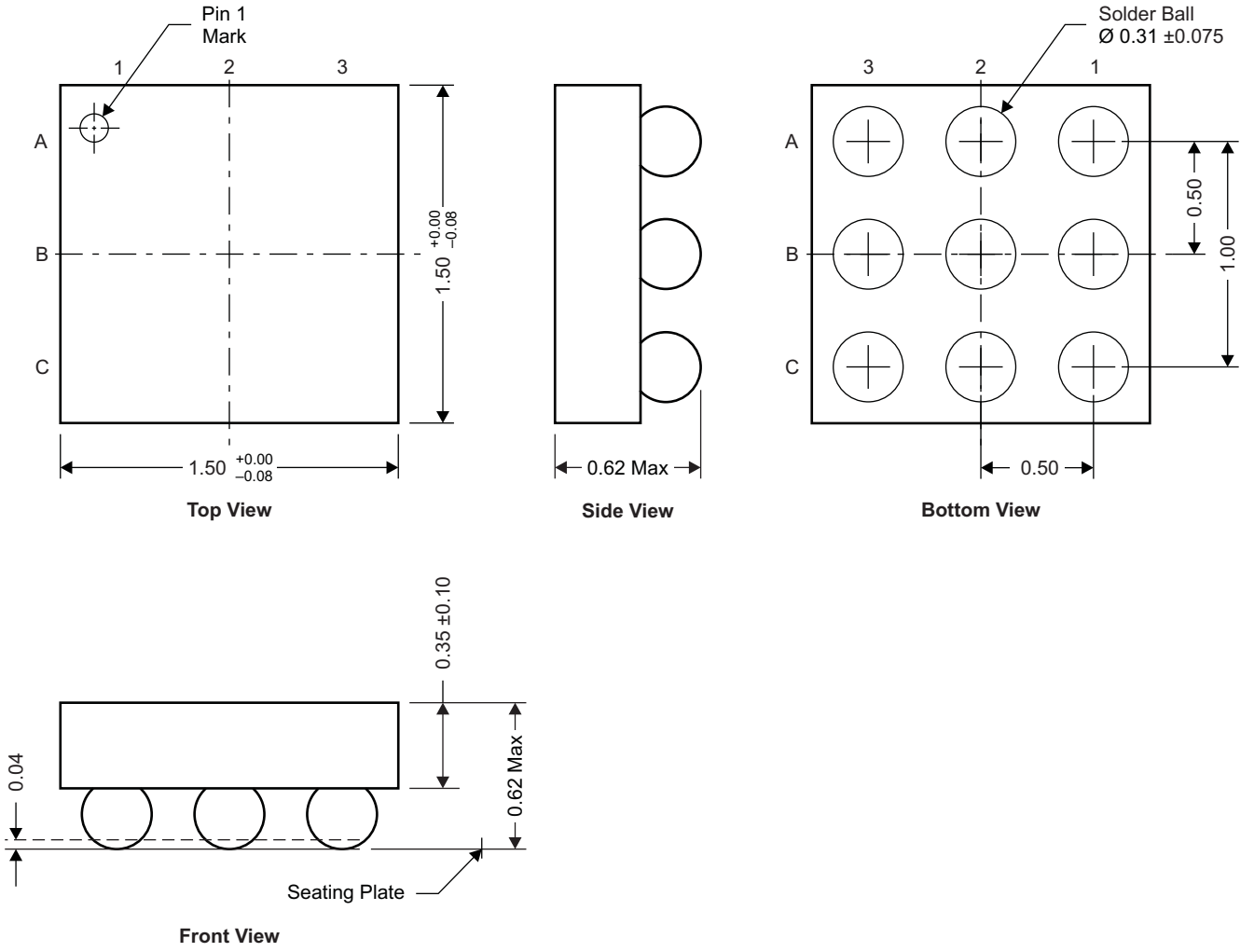
This glossary lists and explains terms, acronyms, and definitions.

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7 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

7.1 CSD22206W 封装尺寸



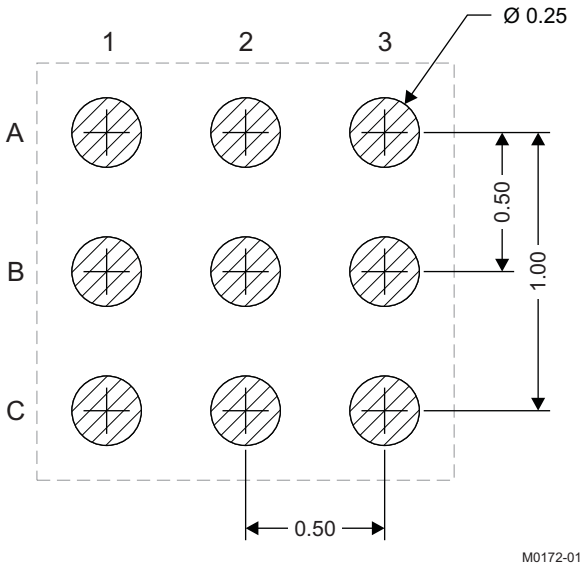
NOTE: 全部尺寸单位为 mm（除非另外注明）。

表 **1.** 引脚分配

位置	名称
A1	栅极
A2，A3，B1，B2，B3	源极
C1，C2，C3	漏极

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7.2 建议的焊盘图案



NOTE: 全部尺寸单位为 mm（除非另外注明）。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD22206W	ACTIVE	DSBGA	YZF	9	3000	RoHS & Green	SAC396 | SNAGCU	Level-1-260C-UNLIM	-55 to 150	22206	Samples
CSD22206WT	ACTIVE	DSBGA	YZF	9	250	RoHS & Green	SAC396 | SNAGCU	Level-1-260C-UNLIM	-55 to 150	22206	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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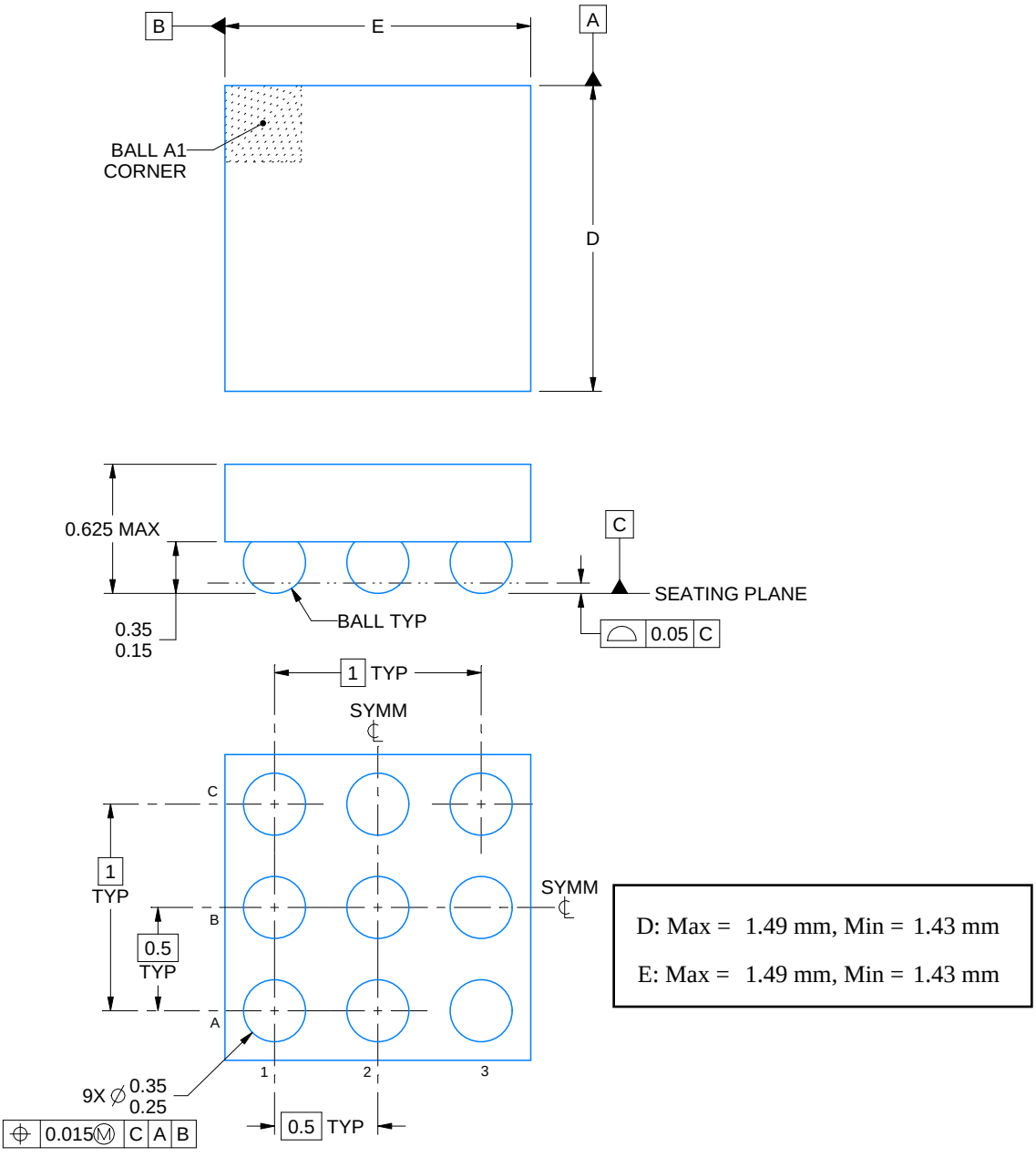
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

YZF0009

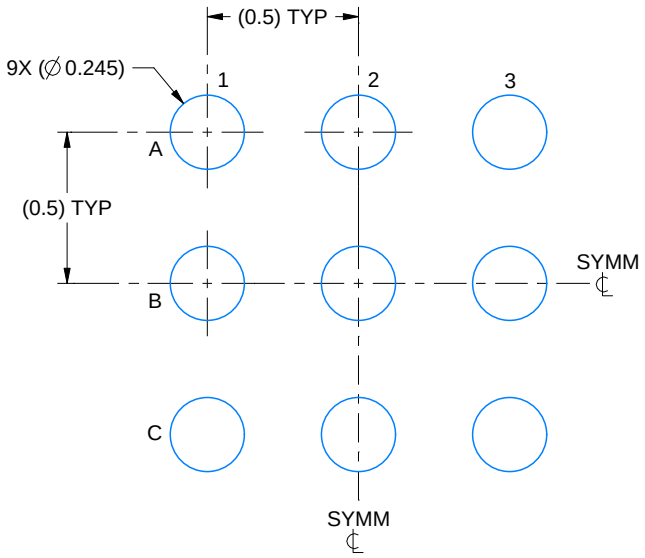
DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY

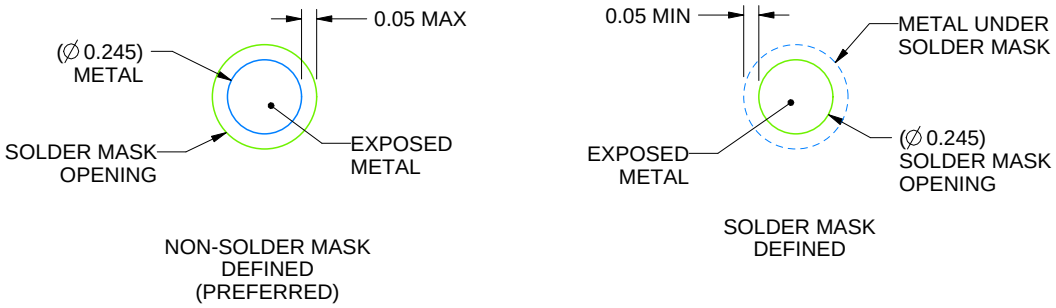


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X

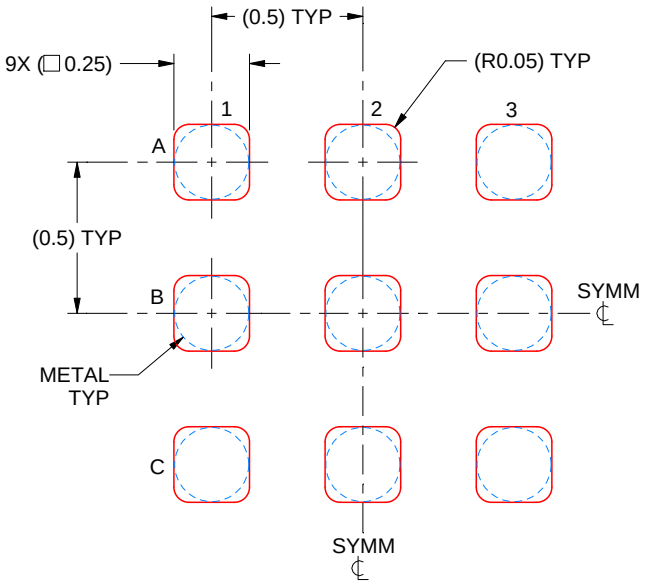


SOLDER MASK DETAILS
NOT TO SCALE

4219558/A 10/2018

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 40X

4219558/A 10/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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