CSD19535KCS 100V N 通道 NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET)

1 特性

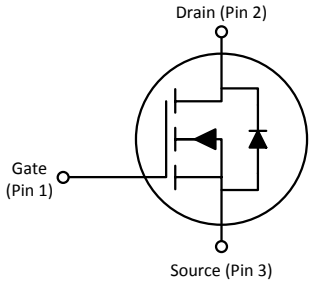
- 超低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩额定值
- 无铅引脚镀层
- 符合 RoHS 环保标准
- 无卤素
- 晶体管 (TO)-220 塑料封装

2 应用范围

- 次级侧同步整流器
- 电机控制

3 说明

这款 100V，3.1mΩ，TO-220 NexFET™ 功率 MOSFET 被设计成在功率转换应用中最大限度地降低损耗。





产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	100		V
Q_g	栅极电荷总量 (10V)	78		nC
Q_{gd}	栅漏栅极电荷	13		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 6V	3.4	mΩ
		V_{GS} = 10V	3.1	mΩ
$V_{GS(th)}$	阈值电压	2.7		V

订购信息(1)

器件	封装	介质	数量	出货
CSD19535KCS	TO-220 塑料封装	管	50	管

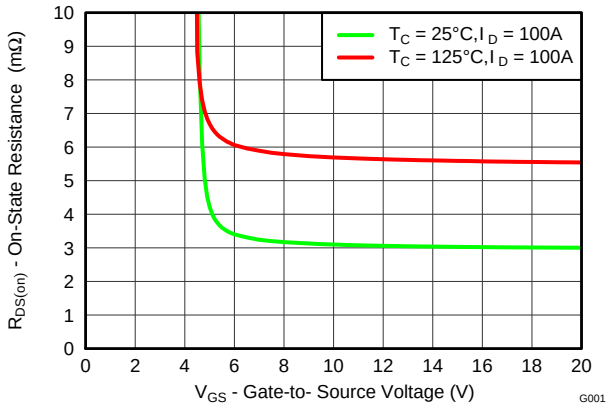
(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

最大绝对额定值

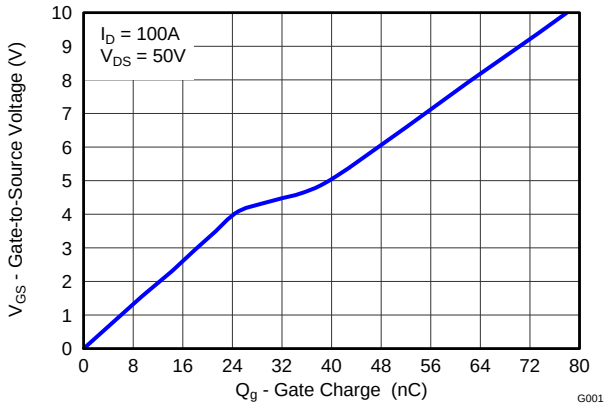
T_A = 25°C		值	单位
V_{DS}	漏源电压	100	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流（受封装限制）	150	A
	持续漏极电流（受芯片限制），T_C = 25°C 时测得	187	
	持续漏极电流（受芯片限制），T_C = 100°C 时测得	133	
I_{DM}	脉冲漏极电流 (1)	400	A
P_D	功率耗散	300	W
T_J，T_{stg}	运行结温和储存温度范围	-55 至 175	°C
E_{AS}	雪崩能量，单脉冲 I_D = 95A，L = 0.1mH，R_G = 25Ω	451	mJ

(1) 最大 $R_{\theta JC}$ = 0.5°C/W，持续时间 ≤100μs，占空比 ≤1%

$R_{DS(on)}$ 与 V_{GS} 间的关系



栅极电荷



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

目录

1 特性 ... 1
2 应用范围 ... 1
3 说明 ... 1
4 修订历史记录 ... 2
5 **Specifications** ... 3
5.1 Electrical Characteristics ... 3
5.2 Thermal Information ... 3
5.3 Typical MOSFET Characteristics ... 4
6 器件和文档支持 ... 7
6.1 商标 ... 7
6.2 静电放电警告 ... 7
6.3 术语表 ... 7
7 机械封装和可订购信息 ... 8
7.1 KCS 封装尺寸 ... 9

4 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2014) to Revision B **Page**

- 已更新脉冲漏极电流条件 ... 1
- Updated the SOA in Figure 10 ... 6

Changes from Original (January 2014) to Revision A **Page**

- 已将脉冲漏电流增加为 400A ... 1
- Updated SOA Curve ... 5

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5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 250 µA	100			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 80 V			1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.2	2.7	3.4	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 6 V, I_D = 100 A		3.4	4.4	mΩ
		V_{GS} = 10 V, I_D = 100 A		3.1	3.6	mΩ
g_{fs}	Transconductance	V_{DS} = 10 V, I_D = 100 A		274		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 50 V, f = 1 MHz		6100	7930	pF
C_{oss}	Output Capacitance			1160	1500	pF
C_{rss}	Reverse Transfer Capacitance			29	38	pF
R_G	Series Gate Resistance			1.4	2.8	Ω
Q_g	Gate Charge Total (10 V)	V_{DS} = 50 V, I_D = 100 A		78	101	nC
Q_{gd}	Gate Charge Gate to Drain			13		nC
Q_{gs}	Gate Charge Gate to Source			25		nC
$Q_{g(th)}$	Gate Charge at V_{th}			16		nC
Q_{oss}	Output Charge	V_{DS} = 40 V, V_{GS} = 0 V		196		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 50 V, V_{GS} = 10 V, I_{DS} = 100 A, R_G = 0 Ω		32		ns
t_r	Rise Time			15		ns
$t_{d(off)}$	Turn Off Delay Time			60		ns
t_f	Fall Time			5		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{SD} = 100 A, V_{GS} = 0 V		0.9	1.1	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 50 V, I_F = 100 A, di/dt = 300 A/µs		421		nC
t_{rr}	Reverse Recovery Time			89		ns

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance			0.5	°C/W
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance			62	

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5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

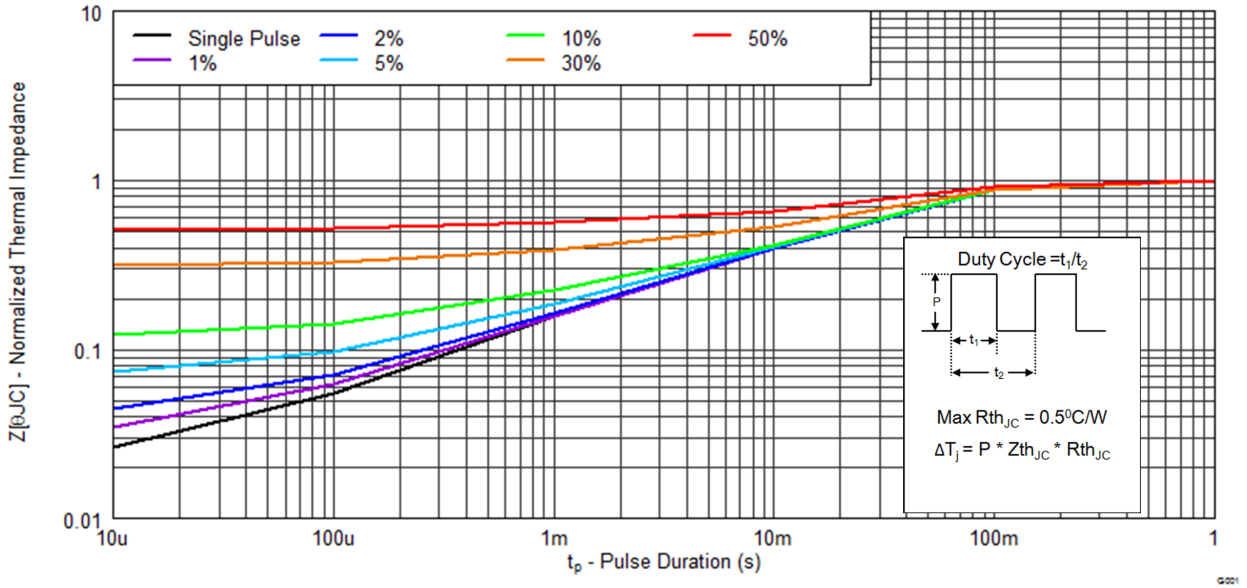


Figure 1. Transient Thermal Impedance

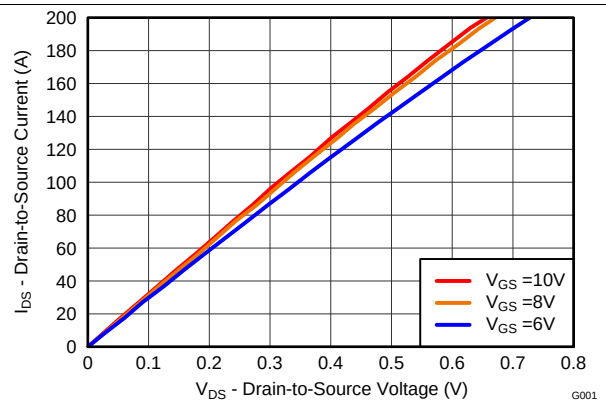


Figure 2. Saturation Characteristics

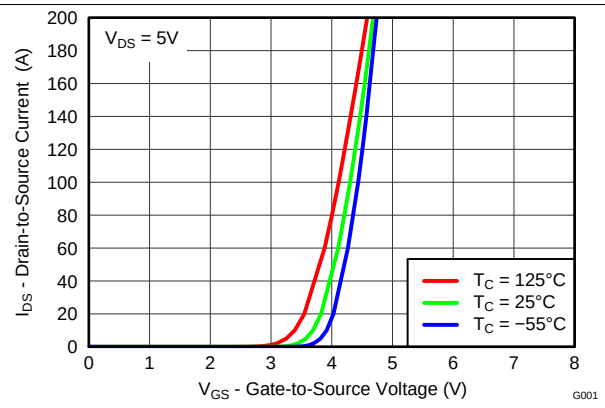


Figure 3. Transfer Characteristics

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Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

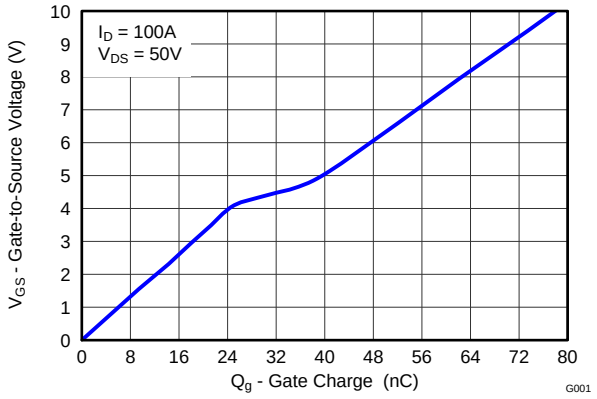


Figure 4. Gate Charge

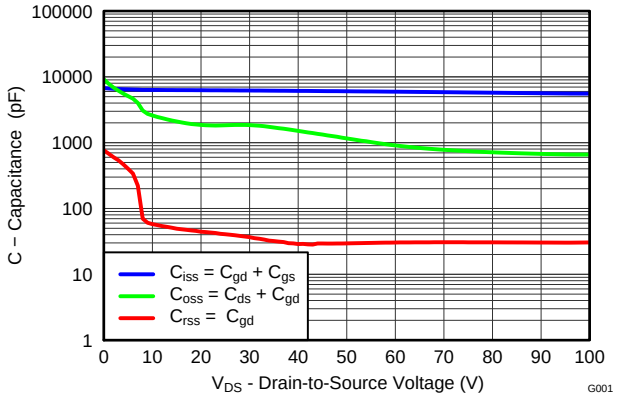


Figure 5. Capacitance

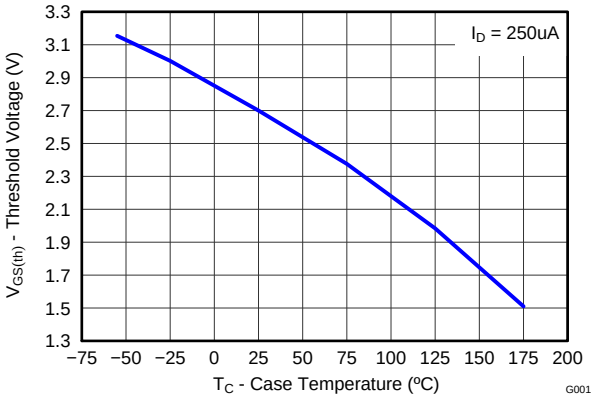


Figure 6. Threshold Voltage vs Temperature

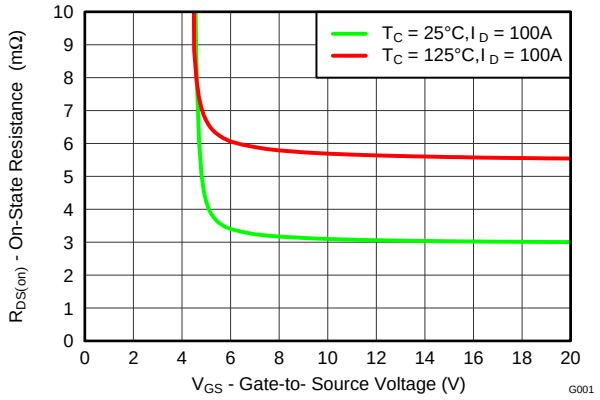


Figure 7. On-State Resistance vs Gate-to-Source Voltage

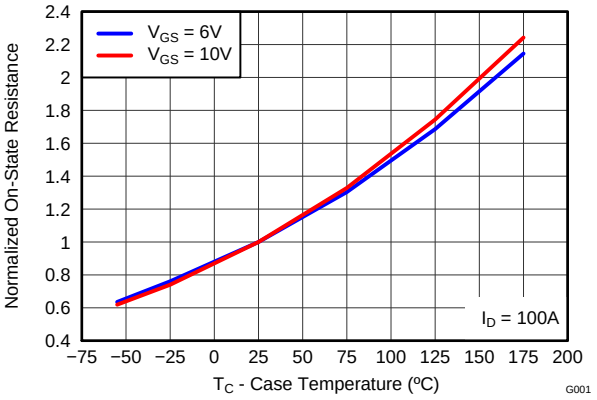


Figure 8. Normalized On-State Resistance vs Temperature

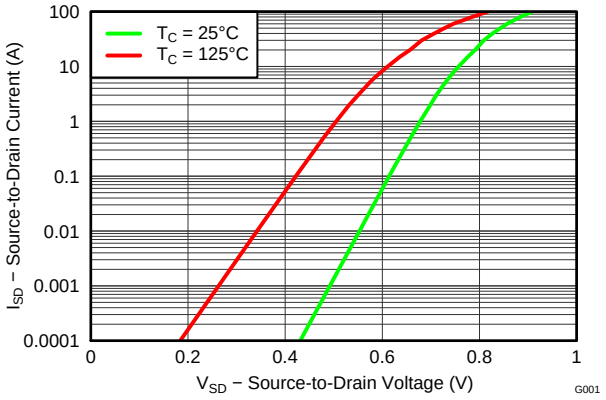


Figure 9. Typical Diode Forward Voltage

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Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

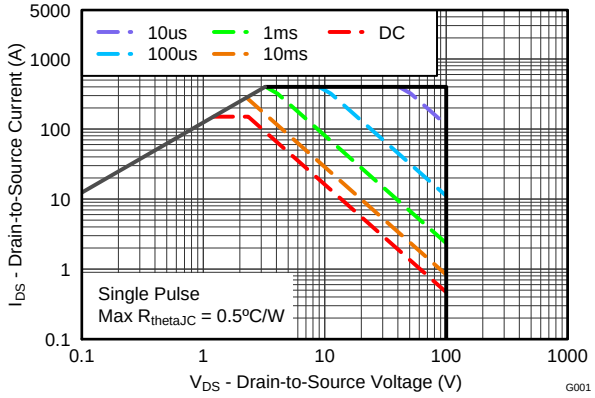


Figure 10. Maximum Safe Operating Area

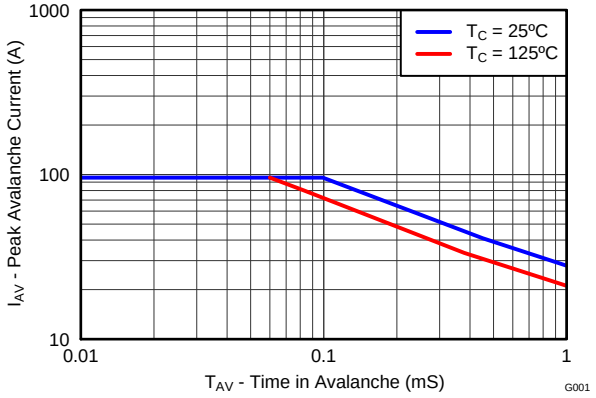


Figure 11. Single Pulse Unclamped Inductive Switching

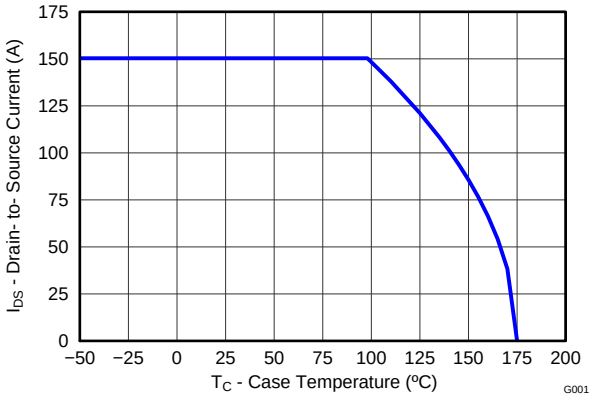


Figure 12. Maximum Drain Current vs Temperature

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6 器件和文档支持

6.1 商标

NexFET is a trademark of Texas Instruments.

6.2 静电放电警告



这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.3 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

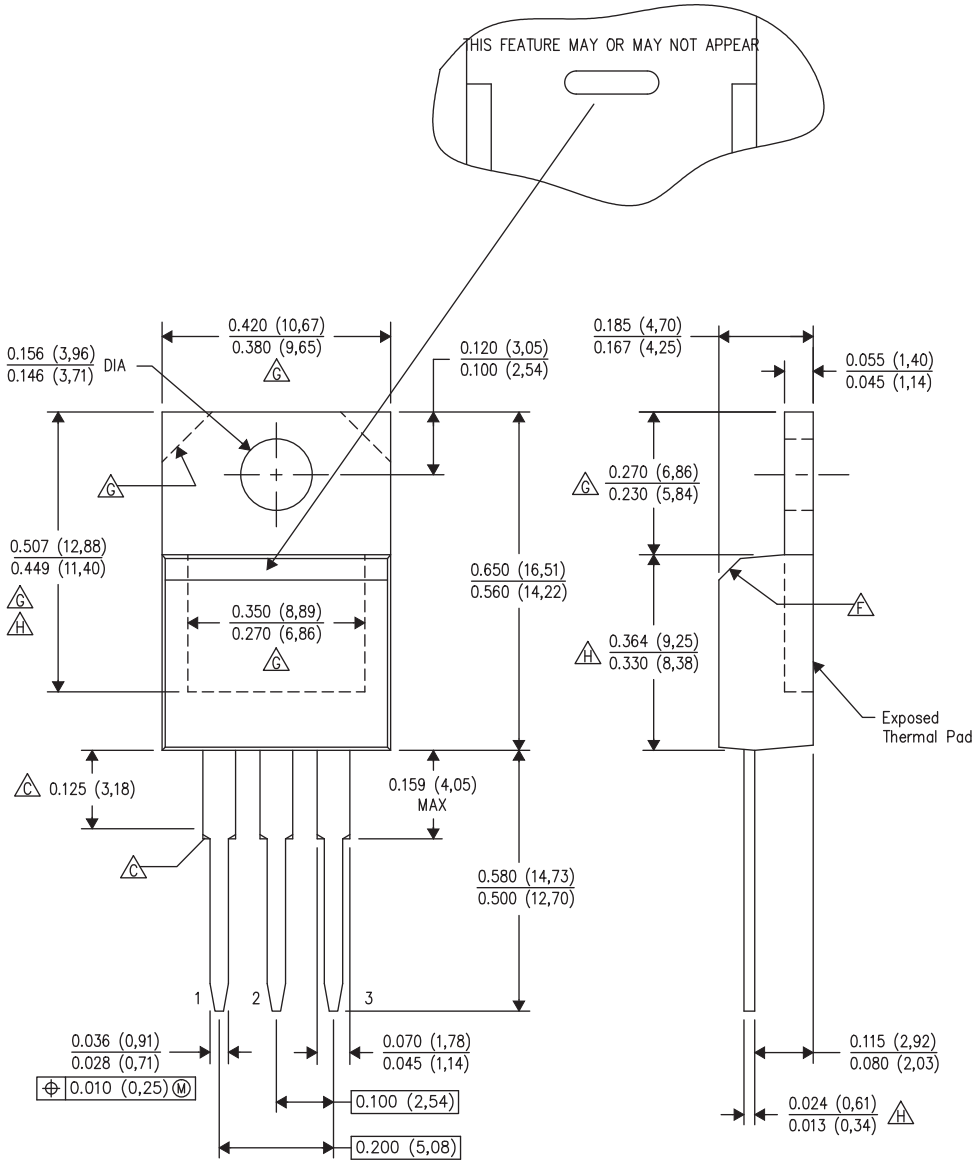
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7 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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7.1 KCS 封装尺寸



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead dimensions are not controlled within this area. Chamfer may or may not appear
D. All lead dimensions apply before solder dip.
E. The center lead is in electrical contact with the mounting tab.
F. The chamfer is optional.
G. Thermal pad contour optional within these dimensions.
H. Falls within JEDEC TO–220 variation AB, except minimum lead thickness, minimum exposed pad length, and maximum body length.

引脚配置

位置	名称
引脚 1	栅极
引脚 2 / 标签	漏
引脚 3	源

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD19535KCS	ACTIVE	TO-220	KCS	3	50	RoHS-Exempt & Non-Green	SN	N / A for Pkg Type	-55 to 175	CSD19535KCS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

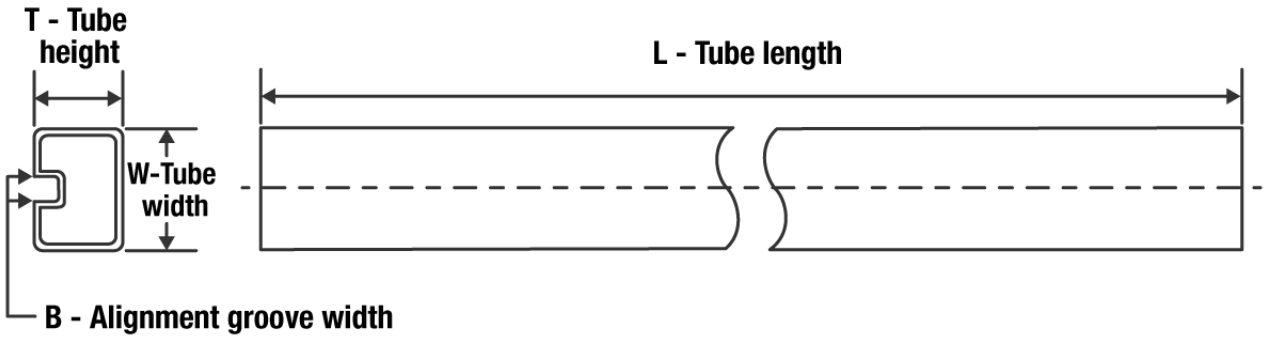
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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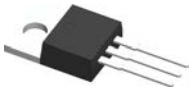
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CSD19535KCS	KCS	TO-220	3	50	534.5	33	7000	3.4
CSD19535KCS	KCS	TO-220	3	50	532	34.1	700	9.6

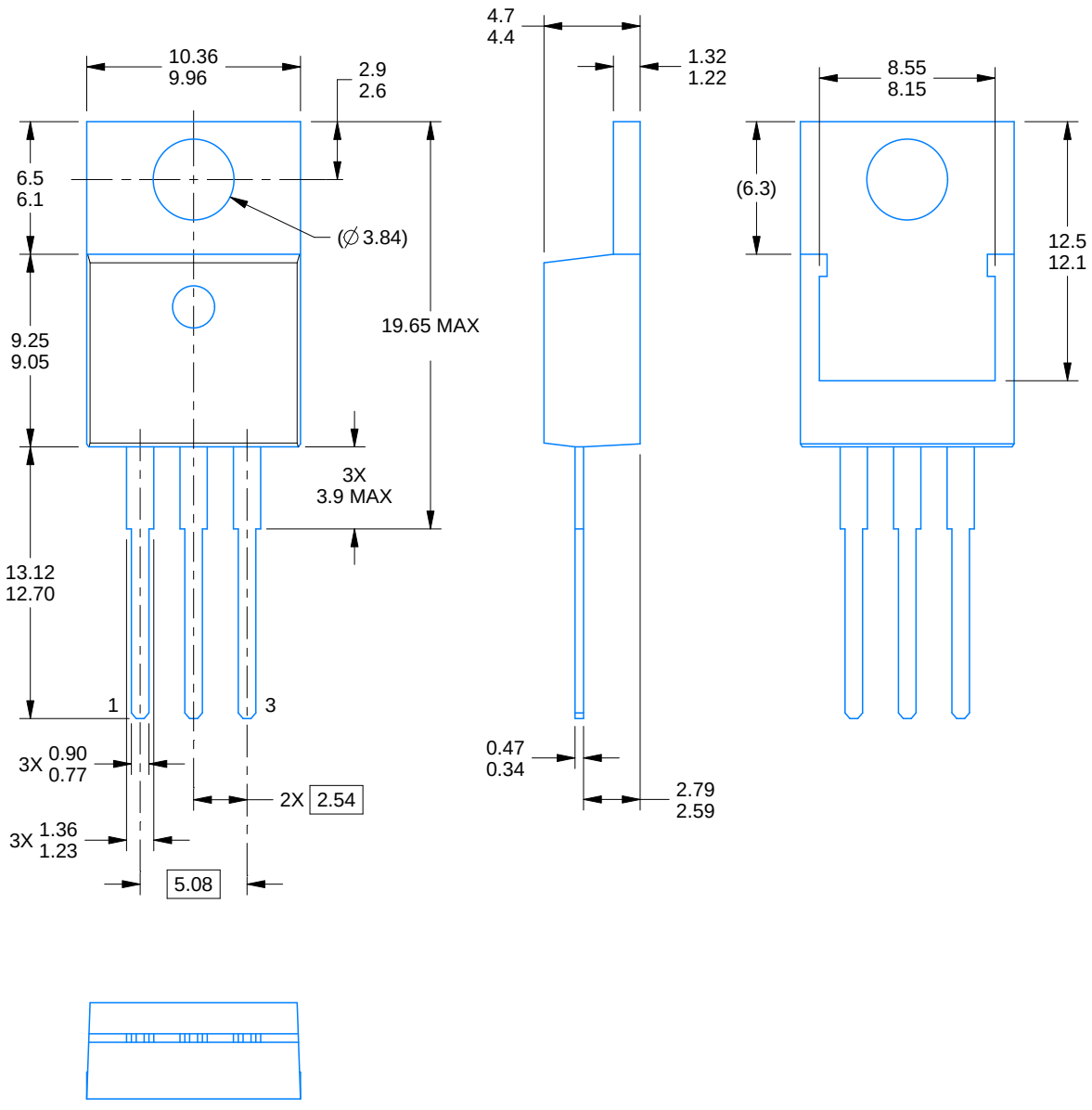
KCS0003B



PACKAGE OUTLINE

TO-220 - 19.65 mm max height

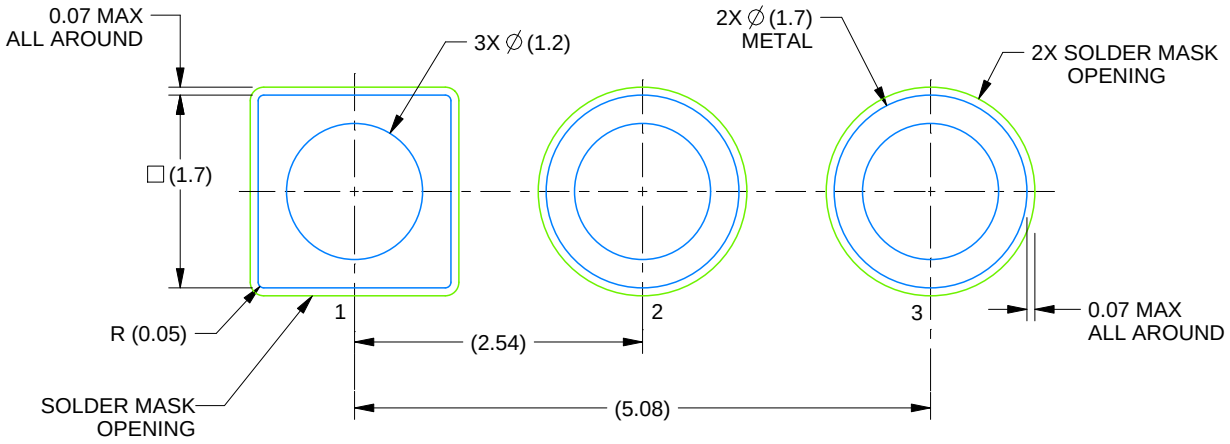
TO-220



4222214/B 08/2018

NOTES:

1. Dimensions are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-220.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:15X

4222214/B 08/2018

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