Dual-Channel, 10-/12-Bit, 500-MSPS Digital-to-Analog Converters (DACs)

Check for Samples: DAC3152, DAC3162

FEATURES

- **Low Power: 270 mW at 500 MSPS**
- **LVDS Input Data Bus**
  - **Interleaved DDR Data Load**
- **High DC Accuracy: ±0.25 LSB DNL (10-bit), ± 0.5 LSB INL (12-bit)**
- **Low Latency: 1.5 Clock Cycles**
- **Simple Control: No Software Required**
- **Differential Scalable Output: 2 mA to 20 mA**
- **On-Chip 1.2-V Reference**
- **1.8-V and 3.3-V DC Supplies**
- **Space Saving Package: 48-pin 7-mm × 7-mm QFN**

APPLICATIONS

- **Cellular Base Stations**
- **Wideband Communications**
- **Medical Instrumentation**
- **Test and Measurement**

DESCRIPTION

The DAC3152/DAC3162 is a low-power, low-latency, high-dynamic-range, dual-channel, 10-/12-bit, pin-compatible family of digital-to-analog converters (DACs) with a sample rate as high as 500 MSPS.

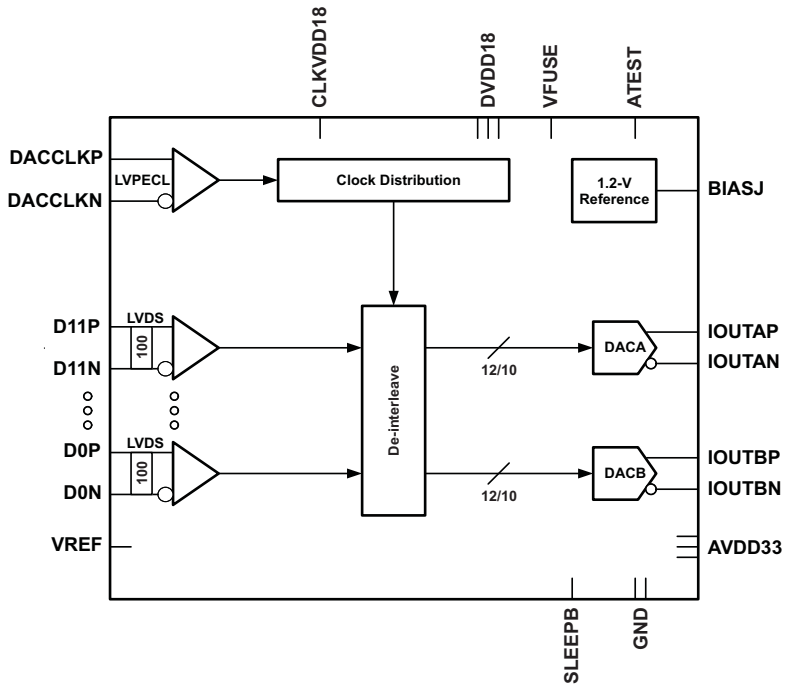
The device simplicity (no software required), low latency, and low power simplify the design of complex systems. The DACs interface seamlessly with the high-performance TRF370333 analog quadrature modulator for direct upconversion architectures.

Digital data for both DAC channels is interleaved through a single LVDS data bus with on-chip termination. The high input rate of the devices allows the processing of wide-bandwidth signals.

The devices are characterized for operation over the entire industrial temperature range of –40°C to 85°C and are available in a small 48-pin 7-mm × 7-mm QFN package.

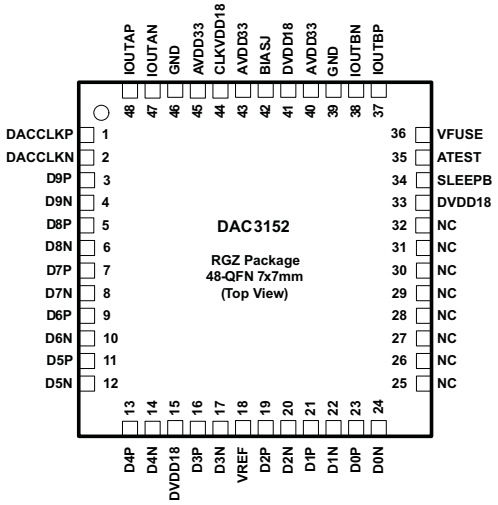
The low power, small size, speed, superior crosstalk, simplicity, and low latency of the DAC3152/DAC3162 make them an attractive fit for a variety of applications.

FUNCTIONAL BLOCK DIAGRAM



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

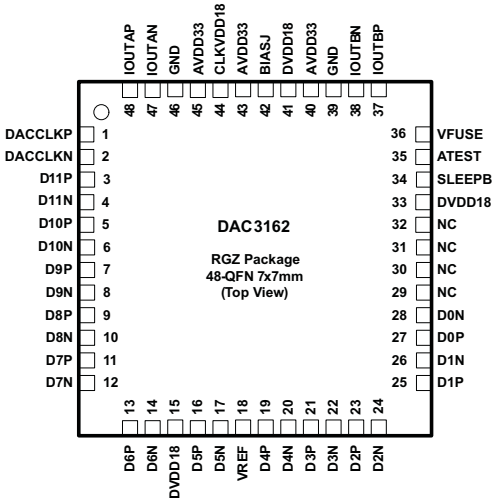
DAC3152 PINOUT AND PIN FUNCTIONS



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
ATEST	35	O	Factory use only. **Leave unconnected for normal operation.**
AVDD33	40, 43, 45	–	Analog supply voltage (3.3 V)
BIASJ	42	O	Full-scale output current bias. For 20-mA full-scale output current, connect a 960-Ω resistor to GND.
CLKVDD18	44	–	Internal clock buffer supply voltage (1.8 V) This supply can be shared with DIGVDD18.
D[9..0]P	3, 5, 7, 9, 11, 13, 16, 19, 21, 23	I	LVDS positive-input data bits 0 through 9. Each positive/negative LVDS pair has an internal 100-Ω termination resistor. Data format relative to DACCLKP/N clock is double data rate (DDR) with two data transfers per DACCLKP/N clock cycle. Dual-channel data is interleaved on this bus. D9P is most-significant data bit (MSB) – pin 3 D0P is least-significant data bit (LSB) – pin 23
D[9..0]N	4, 6, 8, 10, 12, 14, 17, 20, 22, 24	I	LVDS negative-input data bits 0 through 9. (See D[9:0]P description) D9N is most-significant data bit (MSB) – pin 4 D0N is least-significant data bit (LSB) – pin 24
DACCLKP	1	I	Positive external LVPECL clock input with a self-bias of approximately CLKVDD18/2. Input data is latched on both edges of DACCLKP/N (double data rate). The LVPECL clock signal should be AC coupled.
DACCLKN	2	I	Complementary external LVPECL clock input (see the DACCLKP description). The LVPECL clock signal should be AC coupled.
DVDD18	15, 33, 41	–	Digital supply voltage (1.8 V). This supply can be shared with CLKVDD18.
GND	39, 46, Thermal pad	–	Pins 39 and 46 and the thermal pad located on the bottom of the QFN package are ground for all supplies.
IOUTAP	48	O	A-channel DAC current output. An offset binary data pattern of 0x0000 at the DAC input results in a full-scale current sink and the least-positive voltage on the IOUTAP pin. Similarly, a 0x3FF data input results in a 0-mA current sink and the most-positive voltage on the IOUTAP pin.
IOUTAN	47	O	A-channel DAC complementary current output. IOUTAN has the opposite behavior of the IOUTAP described for IOUTAP. An input data value of 0x0000 results in a 0-mA sink and the most-positive voltage on the IOUTAN pin.
IOUTBP	37	O	B-channel DAC current output. See the IOUTAP description.
IOUTBN	38	O	B-channel DAC complementary current output. See the IOUTAN description.
NC	25–32	–	No connect. Leave unconnected for normal operation.
SLEEPB	34	I	Connect to GND to put the device in sleep mode or to AVDD for active mode. Internal pullup
VFUSE	36	–	Digital supply voltage (1.8 V). This supply pin is also used for factory fuse programming. **Connect to DVDD18 pins for normal operation.**
VREF	18	I/O	Factory use only. **Connect to a 0.1-µF decoupling capacitor to GND.**

DAC3162 PINOUT AND PIN FUNCTIONS



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
ATEST	35	O	Factory use only. **Leave unconnected for normal operation.**
AVDD33	40, 43, 45	–	Analog supply voltage (3.3 V)
BIASJ	42	O	Full-scale output current bias. For 20-mA full-scale output current, connect a 960-Ω resistor to GND.
CLKVDD18	44	–	Internal clock buffer supply voltage (1.8 V) This supply can be shared with DIGVDD18.
D[11..0]P	3, 5, 7, 9, 11, 13, 16, 19, 21, 23, 25, 27	I	LVDS positive-input data bits 0 through 11. Each positive/negative LVDS pair has an internal 100-Ω termination resistor. Data format relative to DACCLKP/N clock is double data rate (DDR) with two data transfers per DACCLKP/N clock cycle. Dual channel data is interleaved on this bus. D11P is most-significant data bit (MSB) – pin 3 D0P is least-significant data bit (LSB) – pin 27
D[11..0]N	4, 6, 8, 10, 12, 14, 17, 20, 22, 24, 26, 28	I	LVDS negative-input data bits 0 through 11. (See D[11:0]P description) D11N is most-significant data bit (MSB) – pin 4 D0N is least-significant data bit (LSB) – pin 28
DACCLKP	1	I	Positive external LVPECL clock input with a self-bias of approximately CLKVDD18/2. Input data is latched on both edges of DACCLKP/N (double data rate). The LVPECL clock signal should be AC coupled.
DACCLKN	2	I	Complementary external LVPECL clock input (see the DACCLKP description). The LVPECL clock signal should be AC coupled.
DVDD18	15, 33, 41	–	Digital supply voltage (1.8 V) This supply can be shared with CLKVDD18.
GND	39, 46, Thermal pad	–	Pins 39, 46 and the thermal pad located on the bottom of the QFN package are ground for all supplies.
IOUTAP	48	O	A-channel DAC current output. An offset binary data pattern of 0x0000 at the DAC input results in a full-scale current sink and the least-positive voltage on the IOUTAP pin. Similarly, a 0xFFF data input results in a 0-mA current sink and the most-positive voltage on the IOUTAP pin.
IOUTAN	47	O	A-channel DAC complementary current output. IOUTAN has the opposite behavior of the IOUTAP described for IOUTAP. An input data value of 0x0000 results in a 0-mA sink and the most-positive voltage on the IOUTAN pin.
IOUTBP	37	O	B-channel DAC current output. See the IOUTAP description.
IOUTBN	38	O	B-channel DAC complementary current output. See the IOUTAN description.
NC	25–32	–	No connect. Leave unconnected for normal operation.
SLEEPB	34	I	Connect to GND to put the device in sleep mode or to AVDD for active mode. Internal pullup.
VFUSE	36	–	Digital supply voltage (1.8 V). This supply pin is also used for factory fuse programming. **Connect to DVDD18 pins for normal operation.**
VREF	18	I/O	Factory use only. **Connect to a 0.1-µF decoupling capacitor to GND.**

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE		UNIT
		MIN	MAX	
Supply-voltage range(2)	DVDD18, CLKVDD18	–0.5	2.3	V
	VFUSE	–0.5	2.3	V
	AVDD33	–0.5	4	V
Pin-voltage range(2)	D[11..0]P/N	–0.5	DVDD18 + 0.5	V
	DACCLKP/N	–0.5	CLKVDD18 + 0.5 V	V
	BIASJ, SLEEPB	–0.5	AVDD33 + 0.7 V	V
	IOUTAP/N, IOUTBP/N	–1	AVDD33 + 0.7 V	V
Peak input current (any input)			±20	mA
Peak total input current (all inputs)			±30	mA
Operating free-air temperature range, T_A		–40	85	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured with respect to GND

THERMAL INFORMATION

THERMAL METRIC(1)(2)		DAC3152 DAC3162	UNIT
		RGZ (48 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	28.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	14.9	
θ_{JB}	Junction-to-board thermal resistance	5.62	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	5.6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

ELECTRICAL CHARACTERISTICS – DC SPECIFICATION

DVDD18 = CLKVDD18 = 1.8 V, AVDD33 = 3.3 V, f_{DAC} = 500 MSPS, f_{OUT} = 1 MHz over recommended operating free-air temperature range, $IOUT_{FS}$ = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	DAC3152			DAC3162			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution			10			12			Bits
DC ACCURACY									
DNL	Differential nonlinearity			±0.1			±0.4		LSB
INL	Integral nonlinearity			±0.15			±0.5		LSB
ANALOG OUTPUT(1)									
	Gain error			±1.6			±1.6		%FSR
	Gain mismatch			±0.2			±0.2		%FSR
	Full-scale output current		2		20	2		20	mA
	Output compliance range		AVDD – 0.5		AVDD + 0.5	AVDD – 0.5		AVDD + 0.5	V
	Output resistance			300			300		kΩ
	Output capacitance			5			5		pF
REFERENCE									
V_{REF}	Internal reference voltage		1.14	1.2	1.26	1.14	1.2	1.26	V
TEMPERATURE COEFFICIENTS									
	Gain drift			±60			±60		ppm/°C
	Reference-voltage drift			±41			±41		ppm/°C
POWER SUPPLY									
	AVDD33		3	3.3	3.6	3	3.3	3.6	V
	CLKVDD18, DVDD18		1.7	1.8	1.9	1.7	1.8	1.9	V
PSRR	Power-supply rejection ratio	DC tested		±0.1			±0.1		%FSR/V
POWER CONSUMPTION									
P_{DIS}	Power dissipation	f_{DAC} = 500 MSPS, f_{OUT} = 10 MHz		270	310		278	320	mW
		Power-down mode: no clock, DAC on sleep mode, static data pattern		16	23		17	25	mW
$I_{(AVDD33)}$	Analog supply current			55	65		56	65	mA
$I_{(DVDD18)}$ $I_{(CLKVDD)}$	Digital and clock supply current			50	55		53	63	mA
	Operating range		–40	25	85	–40	25	85	°C

(1) Measured differentially across IOUTAP/N or IOUTBP/N with 25 Ω each to AVDD.

ELECTRICAL CHARACTERISTICS – DIGITAL SPECIFICATIONS

DVDD18 = CLKVDD18 = 1.8 V, AVDD33 = 3.3 V, f_{DAC} = 500 MSPS, f_{OUT} = 1 MHz over recommended operating free-air temperature range, $IOUT_{FS}$ = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	DAC3152			DAC3162			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
LVDS INPUTS: DIGITAL INPUT DATA(1)									
$V_{A,B+}$	Logic-high differential input voltage threshold		150	400		150	400		mV
$V_{A,B-}$	Logic-low differential input voltage threshold			–400	–150		–400	–150	mV
V_{COM}	Input common mode		0.9	1.2	1.5	0.9	1.2	1.5	V
Z_T	Internal termination		85	110	135	85	110	135	Ω
C_L	LVDS input capacitance			2			2		pF
f_{INTERL}	Interleaved LVDS data rate				1000			1000	MSPS
f_{DATA}	Input data rate (per DAC)				500			500	MSPS
CLOCK INPUT: DACCLKP/N									
	Duty cycle		40%		60%	40%		60%	
	Differential voltage		0.2	1		0.2	1		V
	Clock frequency				500			500	MHz
CMOS INTERFACE: SLEEPB									
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IH}	High-level input current		-40		40	-40		40	µA
I_{IL}	Low-level input current		-40		40	-40		40	µA
C_I	CMOS Input capacitance			2			2		pF
DIGITAL INPUT DATA TIMING SPECIFICATIONS: *DOUBLE EDGE* LATCHING									
$t_{s(DATA)}$	Setup time, valid to either edge of DACCLKP/N		200			200			ps
$t_{h(DATA)}$	Hold time, valid after either edge of DACCLKP/N		200			200			ps

(1) See LVDS INPUTS section for terminology.

ELECTRICAL CHARACTERISTICS – AC SPECIFICATIONS

DVDD18 = CLKVDD18 = 1.8 V, AVDD33 = 3.3 V, f_{DAC} = 500 MSPS, f_{OUT} = 1 MHz over recommended operating free-air temperature range, $IOUT_{FS}$ = 20mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	DAC3152			DAC3162			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG OUTPUT (1)									
f_{DAC}	Maximum DAC rate		500			500			MSPS
$t_{s(DAC)}$	Output settling time to 0.1%	Transition: Code 0x0000 to 0xFFFF		10			10		ns
$t_{r(IOUT)}$	Output rise time, 10% to 90%			220			220		ps
$t_{f(IOUT)}$	Output fall time, 90% to 10%			220			220		ps
	Latency			1.5			1.5		DAC clock cycles
Power-up time	DAC wake-up time	IOUT current settling to 1% of $IOUT_{FS}$.		2			2		µs
	DAC sleep time	IOUT current settling to less than 1% of $IOUT_{FS}$.		2			2		µs
AC PERFORMANCE (2)									
SFDR	Spurious-free dynamic range, single tone at 0 dBFS	f_{DAC} = 500 MSPS, f_{OUT} = 10 MHz		78			79		dBc
		f_{DAC} = 500 MSPS, f_{OUT} = 20 MHz		74			74		
		f_{DAC} = 500 MSPS, f_{OUT} = 70 MHz		59			60		
IMD3	Third-order two-tone intermodulation distortion, each tone at –12 dBFS	f_{DAC} = 500 MSPS, f_{OUT} = 10 ± 0.5 MHz		91			93		dBc
		f_{DAC} = 500 MSPS, f_{OUT} = 20 ± 0.5 MHz		85			86		
		f_{DAC} = 500 MSPS, f_{OUT} = 70 ± 0.5 MHz		62			62		
NSD	Noise spectral density, single tone at 0 dBFS	f_{DAC} = 500 MSPS, f_{OUT} = 10 MHz		–145			–155		dBc/Hz
		f_{DAC} = 500 MSPS, f_{OUT} = 70 MHz		–140			–140		
ACLR (3)	Adjacent-channel leakage ratio, single carrier	f_{DAC} = 491.52 MSPS, f_{OUT} = 30 MHz		68			76		dBc
		f_{DAC} = 491.52 MSPS, f_{OUT} = 70 MHz		67			70		
	Channel isolation	f_{DAC} = 500 MSPS, f_{OUT} = 10 MHz		90			90		dBc

(1) Measured differentially across IOUTAP/N or IOUTBP/N with 25 Ω each to AVDD.
(2) 4:1 transformer output termination, 50-Ω doubly terminated load.
(3) Single carrier, W-CDMA with 3.84 MHz BW, 5-MHz spacing, centered at IF, PAR = 12 dB. TESTMODEL 1, 10 ms

Typical Characteristics

DVDD18 = CLKVDD18 = 1.8 V, AVDD33 = 3.3 V, f_{DAC} = 500 MSPS, f_{OUT} = 1 MHz, I_{OUTfs} = 20 mA (unless otherwise noted)

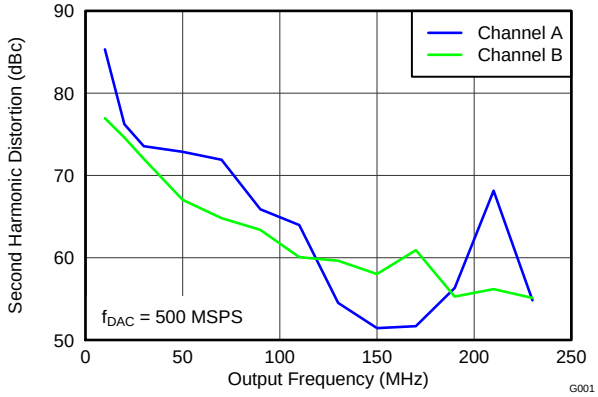


Figure 1. DAC3152 Second-Harmonic Distortion vs Frequency

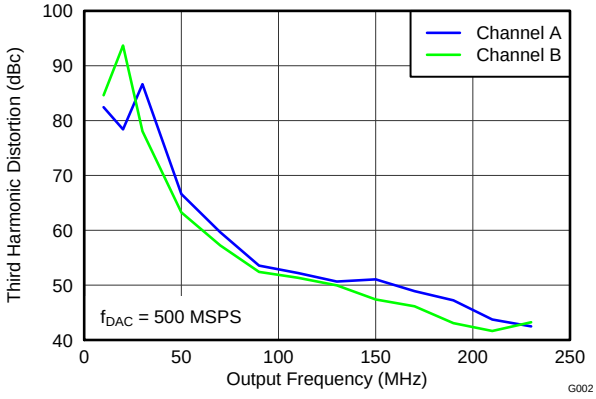


Figure 2. DAC3152 Third-Harmonic Distortion vs Frequency

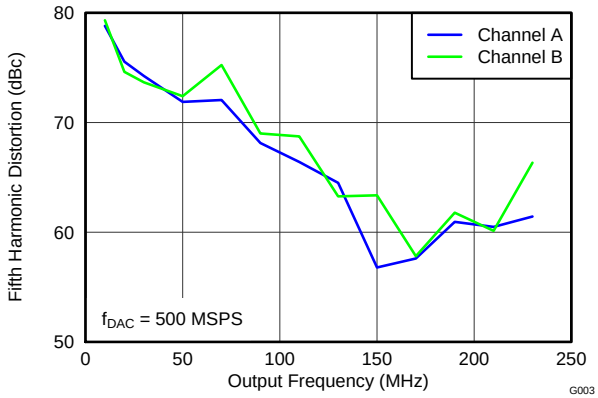


Figure 3. DAC3152 Fifth-Harmonic Distortion vs Frequency

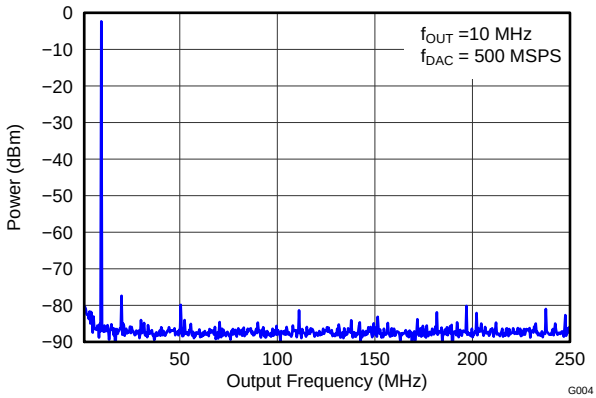


Figure 4. DAC3152 10-MHz Spectrum vs Frequency

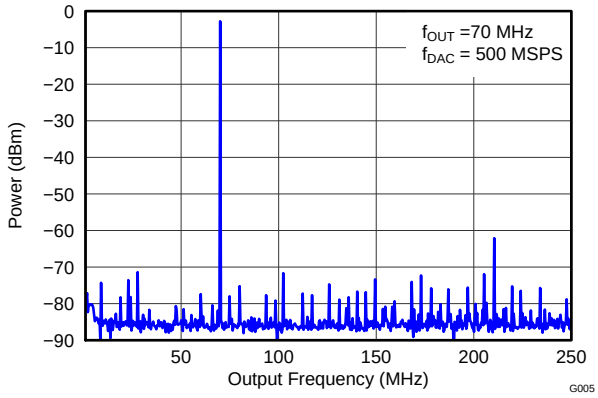


Figure 5. DAC3152 70-MHz Spectrum vs Frequency

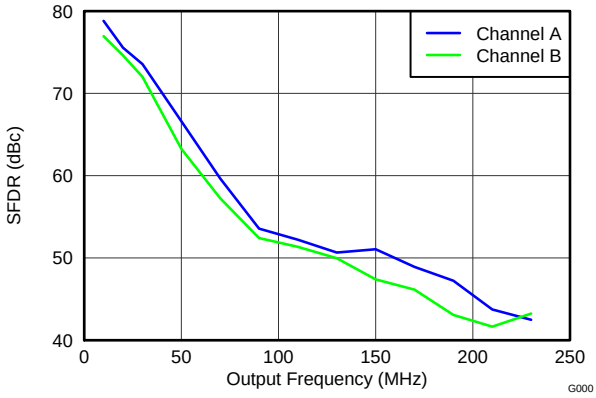


Figure 6. DAC3152 Spurious-Free Dynamic Range vs Frequency

Typical Characteristics (continued)

DVDD18 = CLKVDD18 = 1.8 V, AVDD33 = 3.3 V, f_{DAC} = 500 MSPS, f_{OUT} = 1 MHz, I_{OUTfs} = 20 mA (unless otherwise noted)

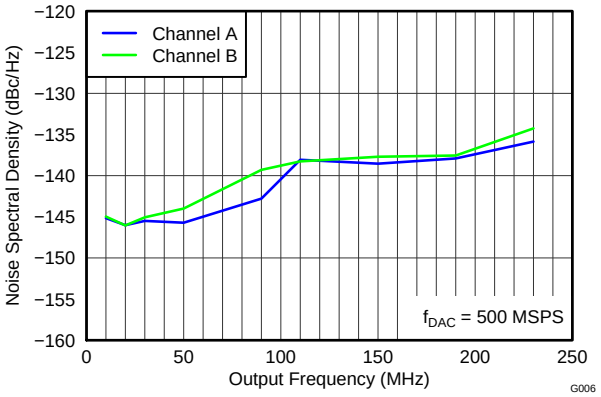


Figure 7. DAC3152 Noise Spectral Density vs Frequency

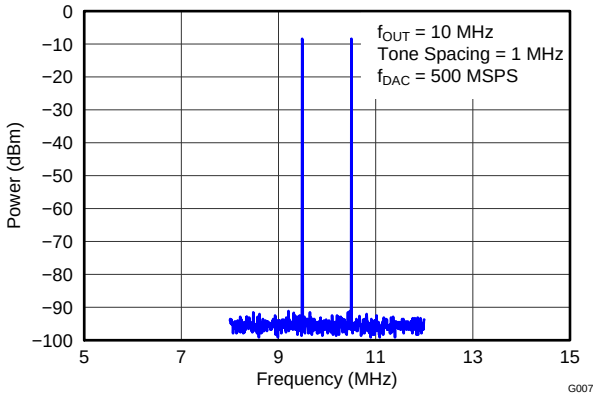


Figure 8. DAC3152 10-MHz Two-Tone Spectrum vs Frequency

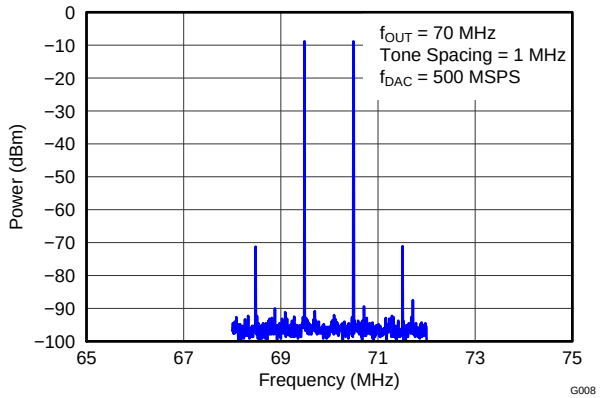


Figure 9. DAC3152 70-MHz Two-Tone Spectrum vs Frequency

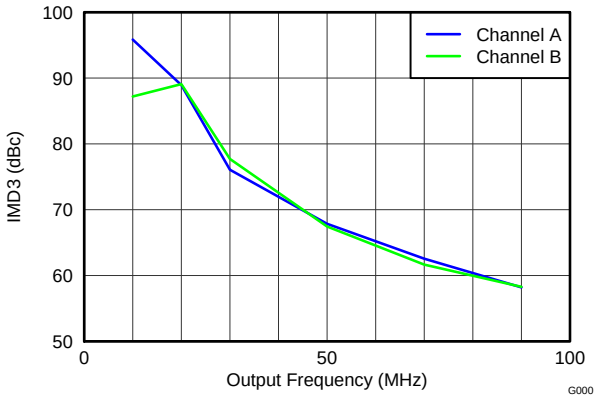


Figure 10. DAC3152 Intermodulation Distortion vs Frequency

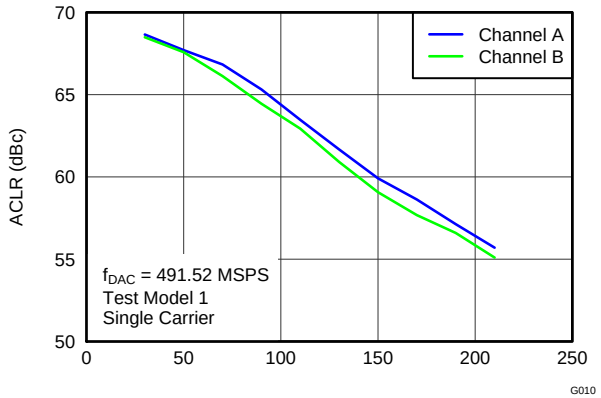


Figure 11. DAC3152 Alternate Channel vs Frequency

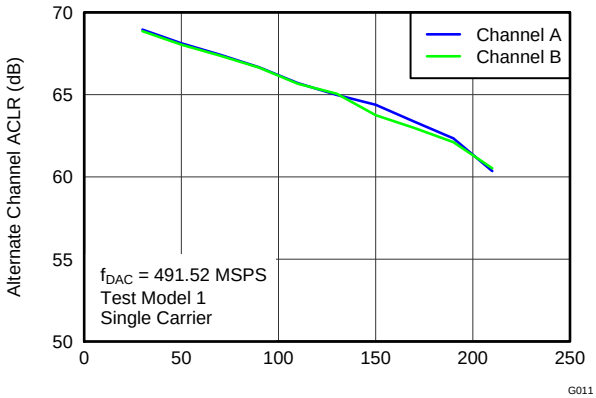


Figure 12. DAC3152 Alternate Channel vs Frequency

Typical Characteristics (continued)

DVDD18 = CLKVDD18 = 1.8 V, AVDD33 = 3.3 V, f_{DAC} = 500 MSPS, f_{OUT} = 1 MHz, I_{OUTfs} = 20 mA (unless otherwise noted)

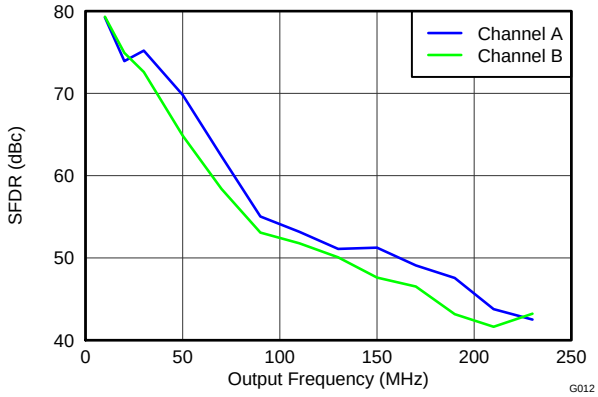


Figure 13. DAC3162 Spurious-Free Dynamic Range vs Frequency

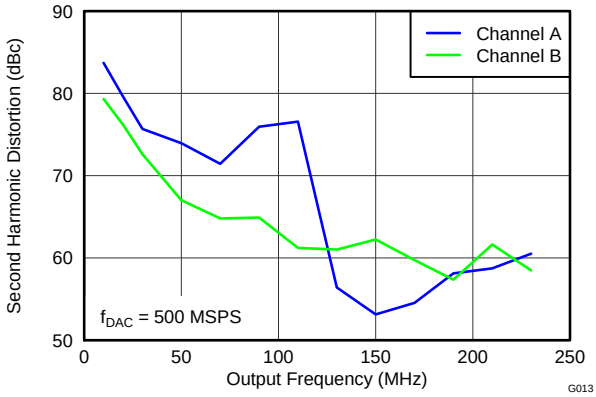


Figure 14. DAC3162 Second-Harmonic Distortion vs Frequency

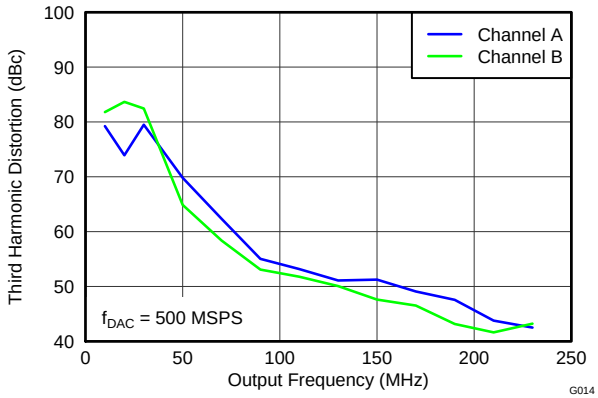


Figure 15. DAC3162 Third-Harmonic Distortion vs Frequency

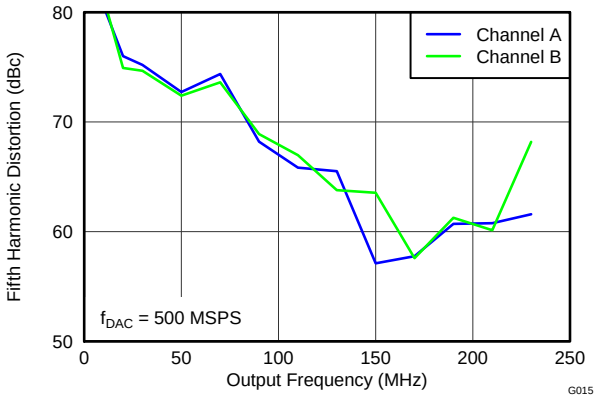


Figure 16. DAC3162 Fifth-Harmonic Distortion vs Frequency

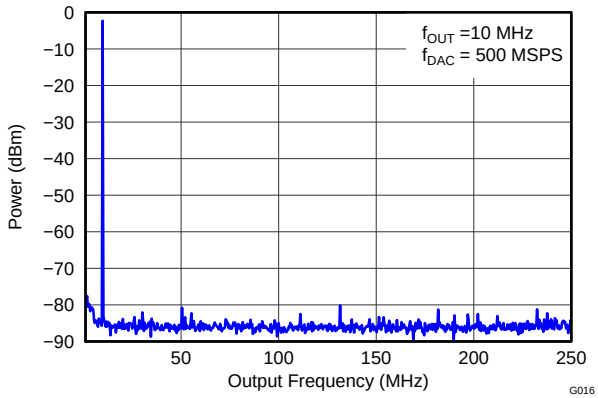


Figure 17. DAC3162 10-MHz Spectrum vs Frequency

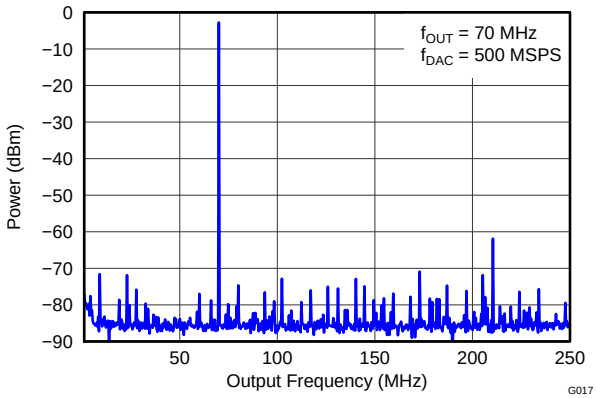


Figure 18. DAC3162 70-MHz Spectrum vs Frequency

Typical Characteristics (continued)

DVDD18 = CLKVDD18 = 1.8 V, AVDD33 = 3.3 V, f_{DAC} = 500 MSPS, f_{OUT} = 1 MHz, I_{OUTfs} = 20 mA (unless otherwise noted)

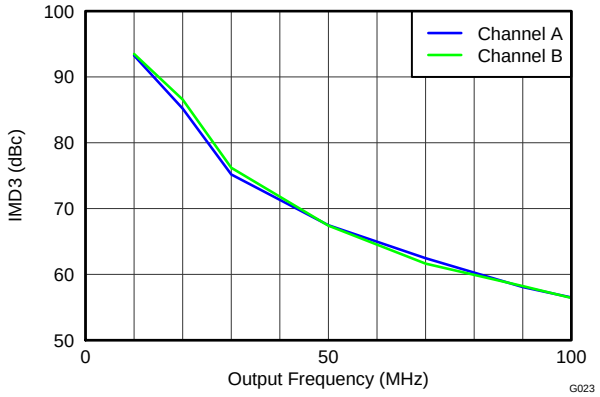


Figure 19. DAC3152 Intermodulation Distortion vs Frequency

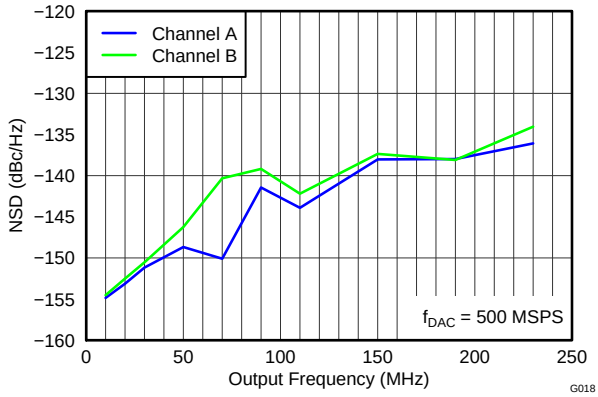


Figure 20. DAC3162 Noise Spectral Density vs Frequency

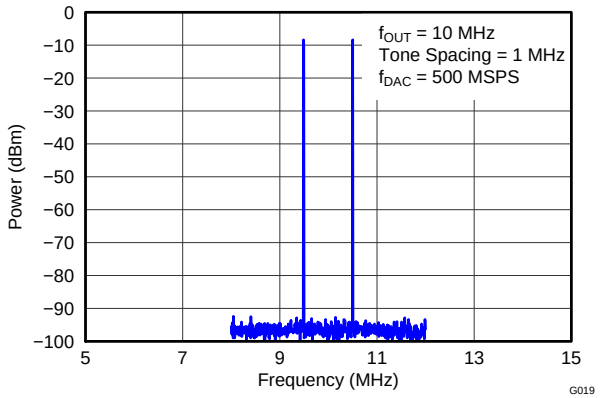


Figure 21. DAC3162 10-MHz Two-Tone Spectrum vs Frequency

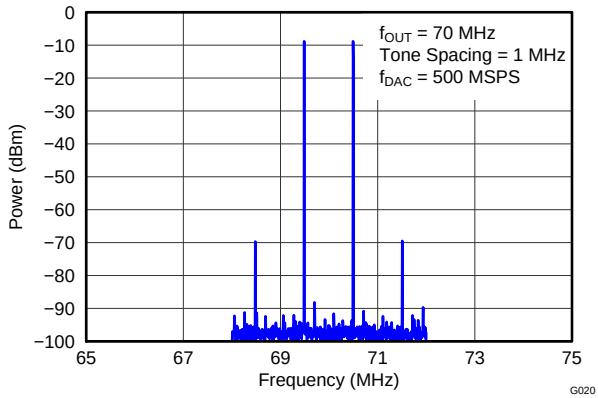


Figure 22. DAC3162 70-MHz Two-Tone Spectrum vs Frequency

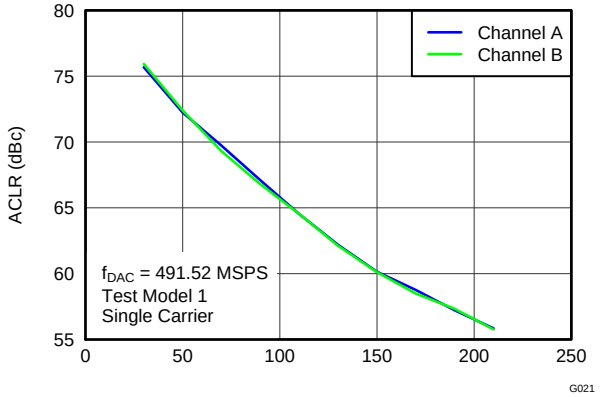


Figure 23. DAC3162 Alternate Channel vs Frequency

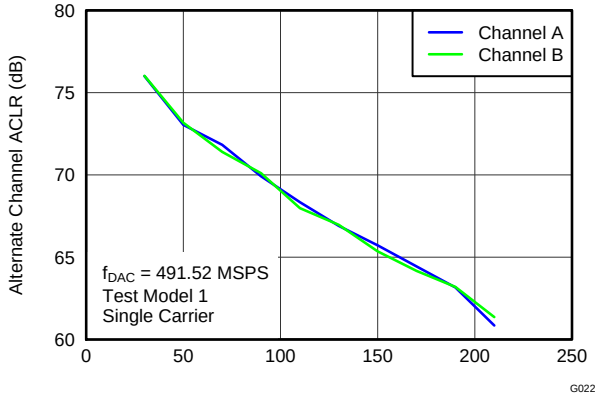


Figure 24. DAC3162 Alternate Channel vs Frequency

Typical Characteristics (continued)

DVDD18 = CLKVDD18 = 1.8 V, AVDD33 = 3.3 V, f_{DAC} = 500 MSPS, f_{OUT} = 1 MHz, I_{OUTfs} = 20 mA (unless otherwise noted)

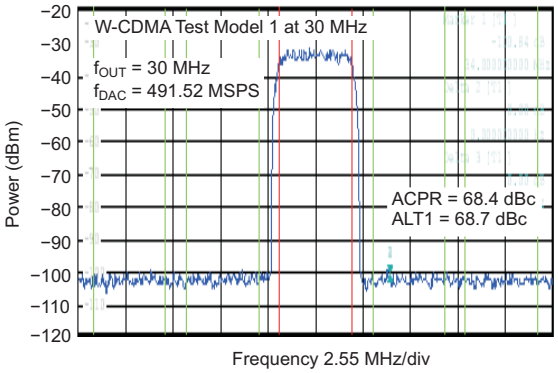


Figure 25. DAC3152 30-MHz WCDMA vs Frequency

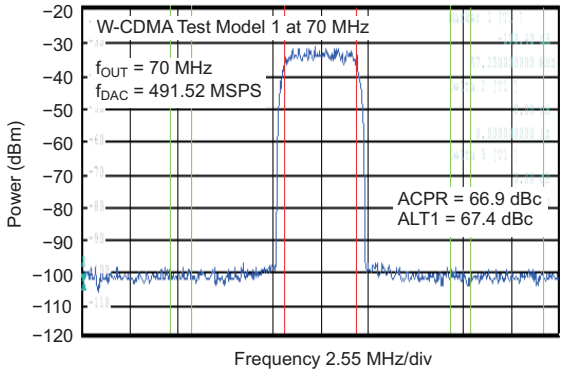


Figure 26. DAC3152 70-MHz WCDMA vs Frequency

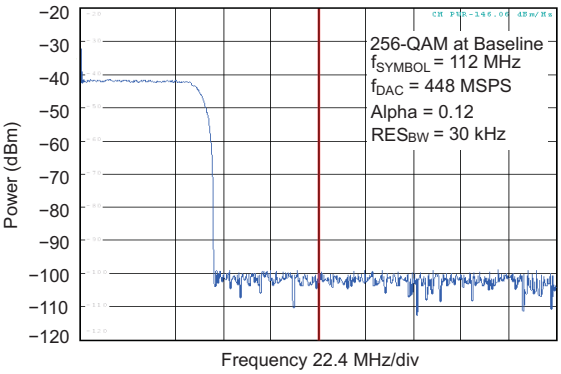


Figure 27. DAC3152 QAM vs Frequency

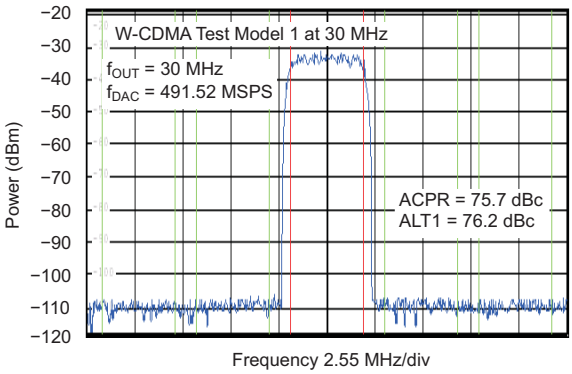


Figure 28. DAC3162 30-MHz WCDMA vs Frequency

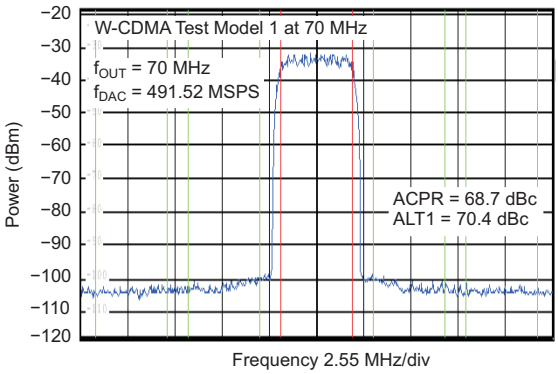


Figure 29. DAC3162 70-MHz WCDMA vs Frequency

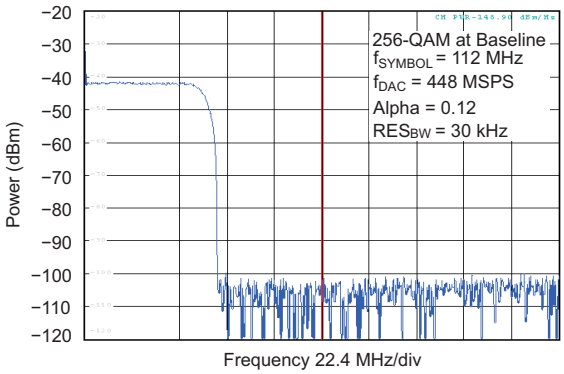


Figure 30. DAC3162 QAM vs Frequency

Typical Characteristics (continued)

DVDD18 = CLKVDD18 = 1.8 V, AVDD33 = 3.3 V, f_{DAC} = 500 MSPS, f_{OUT} = 1 MHz, I_{OUTfs} = 20 mA (unless otherwise noted)

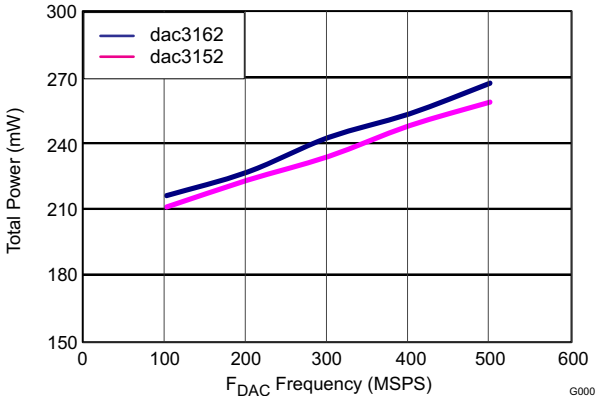


Figure 31. POWER vs Frequency

APPLICATION INFORMATION

DATA INTERFACE

The parallel-port data interface to the device consists of a single LVDS bus that accepts interleaved A and B data with up to 12-bit resolution. Data is sampled by the LVPECL double-data-rate (DDR) clock DACCLK. DACCLK is additionally used for the data conversion process, and hence a low-jitter source is recommended. Setup and hold requirements must be met for proper sampling.

The interleaved data for channels A and B is interleaved in the form A0, B0, A1, B1… into the data bus. Data into the device is formatted according to the diagram shown in Figure 32.

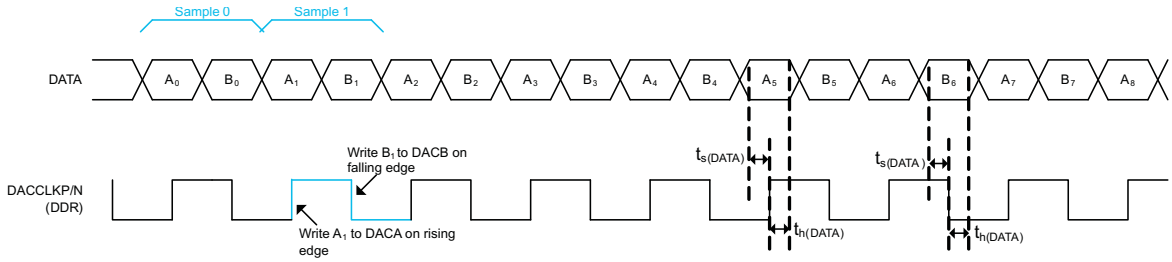


Figure 32. Data Transmission Format

CLOCK INPUT

The DAC clock (DACCLKP/N) is an internally biased differential input that for optimal performance should be driven by a low-jitter clock source. The DACCLK signal is used for both data latching (in DDR format) and as the data conversion clock. Figure 33 shows an equivalent circuit for the DAC input clock.

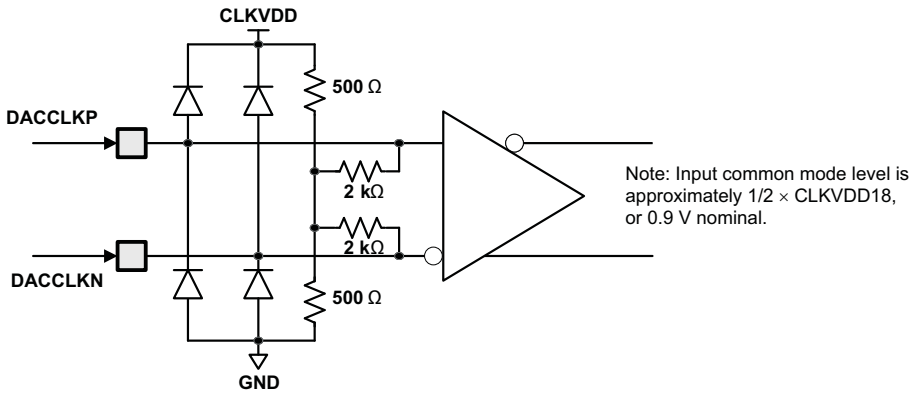


Figure 33. DACCLKP/N Equivalent Input Circuit

The preferred configuration for driving the DACCLK input consists of a differential ECL/PECL source as shown in Figure 34. Although not optimal due to the limited signal swing, an LVDS source can also be used to drive the clock input with the preferred configuration shown in Figure 35.

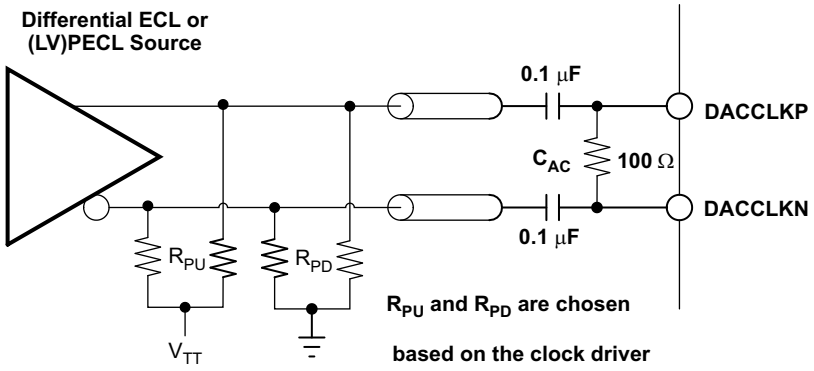


Figure 34. Clock Input Configuration LVPECL

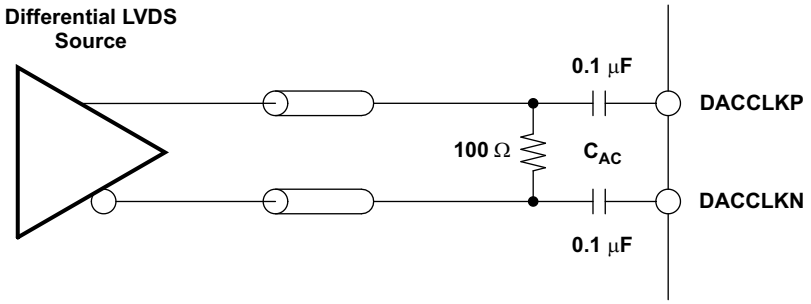


Figure 35. Clock Input Configuration LVDS

A single-ended clock, such as a clean sinusoid or a 1.8 V LVCMOS signal (for low-rate operation), can also be used to drive the clock if configured as in the input circuits of Figure 36 and Figure 37.

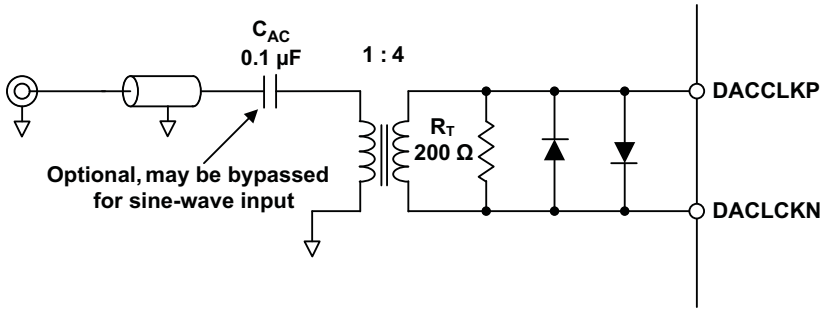


Figure 36. Clock Input Configuration Using 50-Ω Cable Input

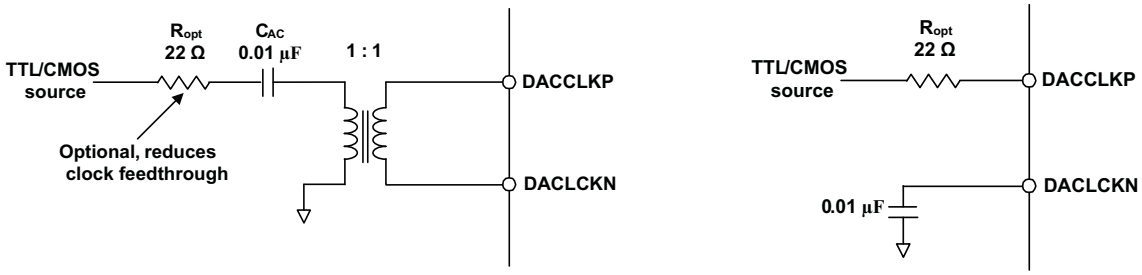


Figure 37. Clock Input Configuration With a Single-Ended TTL/CMOS Clock

DATA INPUTS

The input data LVDS pairs (D[11:0]P/N) have the input configuration shown in Figure 38. Figure 39 shows the typical input levels and common-mode voltage used to drive these inputs.

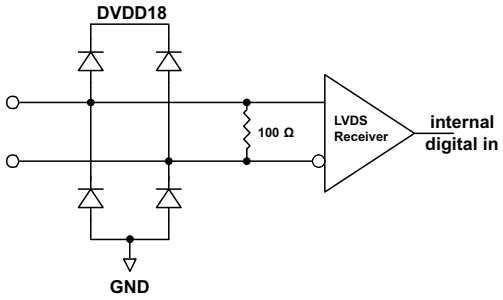


Figure 38. D[13:0]P/N LVDS Input Configuration

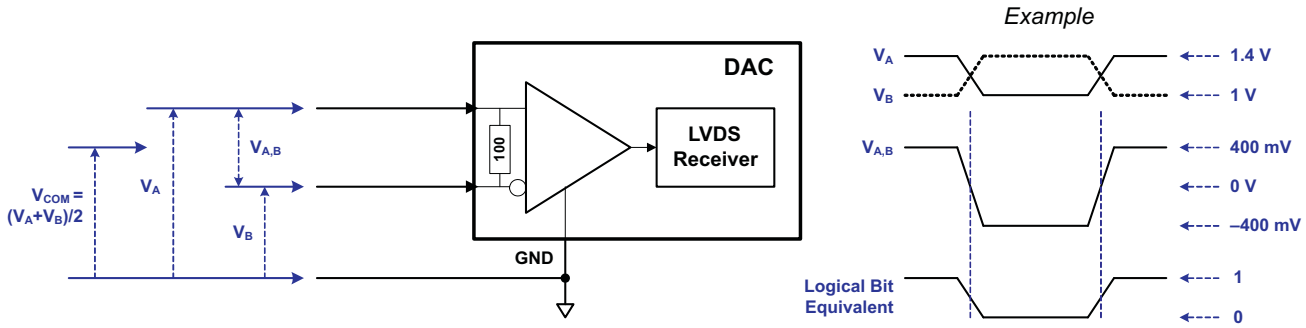


Figure 39. LVDS Data Input Levels

Table 1.

Applied Voltages		Resulting Differential Voltage	Resulting Common-Mode Voltage	Logical Bit Binary Equivalent
V_A	V_B	$V_{A,B}$	V_{COM}	
1.4 V	1 V	400 mV	1.2 V	1
1 V	1.4 V	–400 mV		0
1.2 V	0.8 V	400 mV	1 V	1
0.8 V	1.2 V	–400 mV		0

CMOS INPUT

Figure 40 shows a schematic of the SLEEPB equivalent CMOS digital inputs. See the specification table for logic thresholds. The pullup circuitry is approximately equivalent to 100 kΩ.

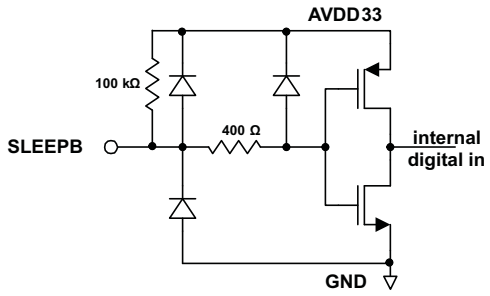


Figure 40. SLEEPB Digital Equivalent Input

REFERENCE OPERATION

The DAC3152/DAC3162 uses a band-gap reference and control amplifier for biasing the full-scale output current. The full-scale output current is set by applying an external resistor R_{BIAS} to pin BIASJ. The bias current I_{BIAS} through resistor R_{BIAS} is defined by the on-chip band-gap reference voltage and control amplifier. The default full-scale output current equals 16 times this bias current and can thus be expressed as:

$$IOUT_{FS} = 16 \times I_{BIAS} = 16 \times V_{BG} / R_{BIAS}$$

The band-gap reference voltage delivers an accurate voltage of 1.2 V. The full-scale output current can be adjusted from 20 mA down to 2 mA by varying resistor RBIAS. The internal control amplifier has a wide input range, supporting the full-scale output current range of 20 dB. The recommended value for R_{BIAS} is 960 Ω, which results in a full-scale output current of 20 mA.

DAC TRANSFER FUNCTION

The DAC outputs of the DAC3152/DAC3162 consist of a segmented array of NMOS current sinks, capable of sinking a full-scale output current up to 20 mA. Differential current switches direct the current to either one of the complementary output nodes IOUTP or IOUTN. Complementary output currents enable differential operation, thus canceling out common-mode noise sources (digital feed-through, on-chip and PCB noise), dc offsets, and even-order distortion components, and increasing signal output power by a factor of four.

The full-scale output current is set using external resistor R_{BIAS} in combination with an on-chip band-gap voltage reference source (1.2 V) and control amplifier. Current I_{BIAS} through resistor R_{BIAS} is mirrored internally to provide a maximum full-scale output current equal to 16 times I_{BIAS}.

The relation between IOUTP and IOUTN can be expressed as:

$$IOUT_{FS} = IOUTP + IOUTN$$

Current flowing into a node is denoted as – current, and current flowing out of a node as + current. Because the output stage is a current sink, the current flows from AVDD33 into the IOUTP and IOUTN pins. The output current flow in each pin driving a resistive load can be expressed as:

$$IOUTP = IOUT_{FS} \times ((2^N - 1) - CODE) / 2^N$$

$$IOUTN = IOUT_{FS} \times CODE / 2^N$$

where CODE is the decimal representation of the DAC data input word and N is the DAC bit resolution.

For the case where IOUTP and IOUTN drive resistor loads R_L directly, this translates into single-ended voltages at IOUTP and IOUTN:

$$VOUTP = AVDD - | IOUTP | \times R_L$$

$$VOUTN = AVDD - | IOUTN | \times R_L$$

Assuming that the data is full scale ($2^N - 1$ in offset binary notation) and the R_L is 25 Ω, the differential voltage between pins IOUTP and IOUTN can be expressed as:

$$VOUTP = AVDD - | - 0 \text{ mA} | \times 25\ \Omega = 3.3 \text{ V}$$

$$VOUTN = AVDD - | -20 \text{ mA} | \times 25\ \Omega = 2.8 \text{ V}$$

$$VDIFF = VOUTP - VOUTN = 0.5 \text{ V}$$

Note that care should be taken not to exceed the compliance voltages at nodes IOUTP and IOUTN, which would lead to increased signal distortion.

ANALOG CURRENT OUTPUTS

The DAC outputs can be easily configured to drive a doubly terminated 50-Ω cable using a properly selected RF transformer. Figure 41 and Figure 42 show the 50-Ω doubly terminated transformer configuration with 1:1 and 4:1 impedance ratios, respectively. Note that the center tap of the primary input of the transformer must be connected to AVDD to enable a dc current flow. Applying a 20-mA full-scale output current leads to a 0.5-Vpp output for a 1:1 transformer and a 1-Vpp output for a 4:1 transformer. The low dc impedance between IOUTP or IOUTN and the transformer center tap sets the center of the ac signal to AVDD, so the 1-Vpp output for the 4:1 transformer results in an output between AVDD – 0.5 V and AVDD + 0.5 V.

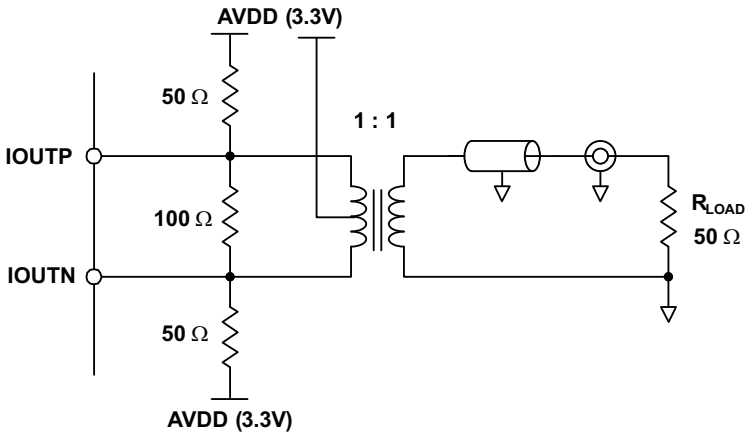


Figure 41. Driving a Doubly Terminated 50-Ω Cable Using a 1:1 Impedance-Ratio Transformer

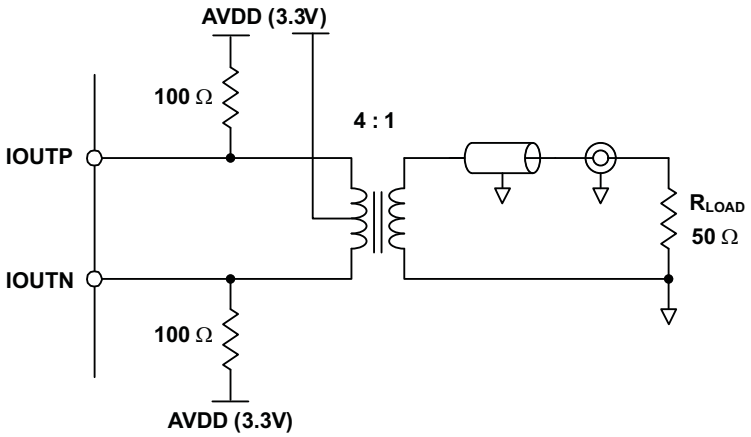


Figure 42. Driving a Doubly Terminated 50-Ω Cable Using a 4:1 Impedance-Ratio Transformer

PASSIVE INTERFACE TO ANALOG QUADRATURE MODULATORS

A common application in communication systems is to interface the DAC to an IQ modulator like the TRF3703 family of modulators from Texas Instruments. The input of the modulator is generally of high impedance and requires a specific common-mode voltage. A simple resistive network can be used to maintain 50-Ω load impedance for the DAC3152/DAC3162 and also provide the necessary common-mode voltages for both the DAC and the modulator.

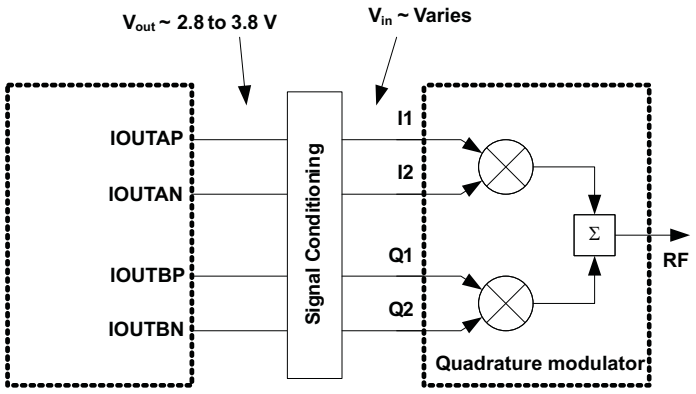


Figure 43. DAC3152/DAC3162 to Analog Quadrature Modulator Interface

The DAC3152/DAC3162 has a maximum 20-mA full-scale output and a voltage compliance range of AVDD ± 0.5 V. The TRF3703 IQ modulator family has three common-mode voltage options: 1.5 V, 1.7 V, and 3.3 V, and the TRF370417 IQ modulator has a 1.7-V common mode.

Figure 44 shows the recommended passive network to interface the DAC to the TRF370317, which has a common-mode voltage of 1.7 V. The network generates the 3.3-V common mode required by the DAC output and 1.7 V at the modulator input, while still maintaining a 50-Ω load for the DAC.

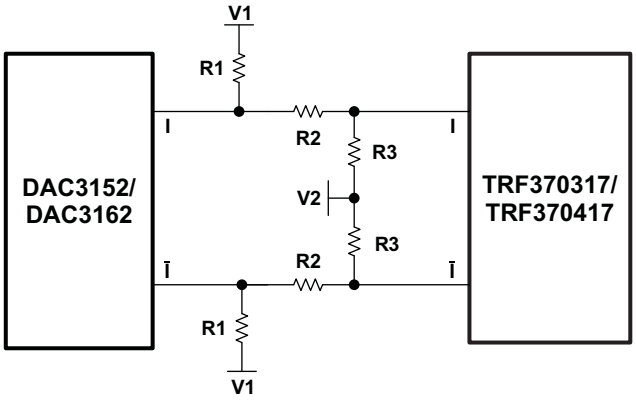


Figure 44. DAC3152/DAC3162 to TRF370317 or TRF370417 Interface

If V1 is set to 5 V and V2 is set to –5 V, the corresponding resistor values are R1 = 57 Ω, R2 = 80 Ω, and R3 = 336 Ω. The loss developed through R2 is about –1.86 dB. When there is no –5-V supply available and V2 is set to 0 V, the resistor values are R1 = 66 Ω, R2 = 101 Ω, and R3 = 107 Ω. The loss with these values is –5.76 dB.

Figure 45 shows the recommended network for interfacing with the TRF370333, which requires a common mode of 3.3 V. This is the simplest interface, as there is no voltage shift. With V1 = 5 V and V2 = 0 V, the resistor values are R1 = 66 Ω and R3 = 208 Ω.

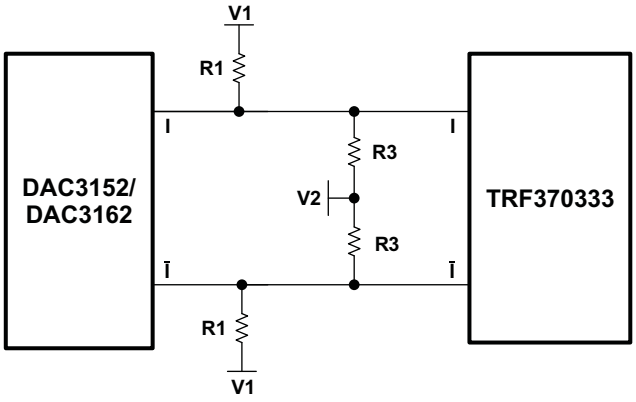


Figure 45. DAC3152/DAC3162 to TRF370333 Interface

In most applications, a baseband filter is required between the DAC and the modulator to eliminate the DAC images. This filter can be placed after the common-mode biasing network. For the DAC-to-modulator network shown in Figure 46, R2 and the filter load R4 must be considered into the DAC impedance. The filter must be designed for the source impedance created by the resistor combination of R3 || (R2 + R1). The effective impedance seen by the DAC is affected by the filter termination resistor, resulting in R1 || (R2 + R3 || (R4/2)).

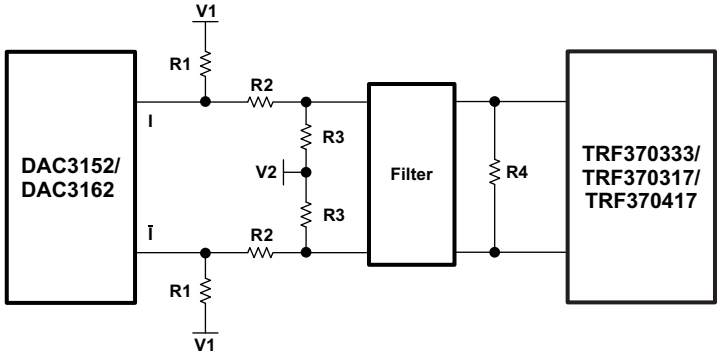


Figure 46. DAC to Modulator Interface With Filter

Factoring in R4 into the DAC load, a typical interface to the TRF370317 with V1 = 5 V and V2 = 0 V results in the following values: R1 = 72 Ω, R2 = 116 Ω, R3 = 124 Ω and R4 = 150 Ω. This implies that the filter must be designed for 75-Ω input and output impedance (single-ended impedance). The common-mode levels for the DAC and modulator are maintained at 3.3 V and 1.7 V, and the DAC load is 50 Ω. The added load of the filter termination causes the signal to be attenuated by –10.8 dB.

A filter can be implemented in a similar manner to interface with the TRF370333. In this case, it is much simpler to balance the loads and common-mode voltages, due to the absence of R2. An added benefit is that there is no loss in this network. With V1 = 5 V and V2 = 0 V, the network can be designed such that R1 = 115 Ω, R3 = 681 Ω, and R4 = 200 Ω. This results in a filter impedance of R1 || R2 = 100 Ω, and a DAC load of R1 || R3 || (R4/2), which is equal to 50 Ω. R4 is a differential resistor and does not affect the common-mode level created by R1 and R3. The common-mode voltage is set at 3.3 V for a full-scale current of 20 mA.

For more information on how to interface the DAC3152/DAC3162 to an analog quadrature modulator, see the application reports *Passive Terminations for Current Output DACs* (SLAA399) and *Design of Differential Filters for High-Speed Signal Chains* (SLWA053).

POWER-UP SEQUENCE

The following start-up sequence is recommended to power up the DAC3152/DAC3162:

- Supply 1.8 V to DVDD18 and CLKVDD18 simultaneously, and 3.3 V to AVDD33. Within AVDD33, the multiple AVDD33 pins should be powered up simultaneously. The 1.8-V and 3.3-V supplies can be powered up simultaneously or in any order.

  There are no specific requirements on the ramp rate for the supplies.
- Provide the DAC clock to the DACCLKP/N inputs.
- Toggle the SLEEPB pin for a minimum 25-ns low pulse duration.
- Provide the LVDS data inputs.

DEFINITION OF SPECIFICATIONS

Adjacent-Carrier Leakage Ratio (ACLR): Defined for a 3.84-Mcps 3GPP W-CDMA input signal measured in a 3.84-MHz bandwidth at a 5-MHz offset from the carrier with a 12-dB peak-to-average ratio.

Analog and Digital Power-Supply Rejection Ratio (APSRR, DPSRR): Defined as the percentage error in the ratio of the delta IOUT and delta supply voltage normalized with respect to the ideal IOUT current.

Differential Nonlinearity (DNL): Defined as the variation in analog output associated with an ideal 1-LSB change in the digital input code.

Gain Drift: Defined as the maximum change in gain, in terms of ppm of full-scale range (FSR) per °C, from the value at ambient (25°C) to values over the full operating temperature range.

Gain Error: Defined as the percentage error (in FSR%) for the ratio between the measured full-scale output current and the ideal full-scale output current.

Integral Nonlinearity (INL): Defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Intermodulation Distortion (IMD3): The two-tone IMD3 is defined as the ratio (in dBc) of the third-order intermodulation distortion product to either fundamental output tone.

Offset Drift: Defined as the maximum change in dc offset, in terms of ppm of full-scale range (FSR) per °C, from the value at ambient (25°C) to values over the full operating temperature range.

Offset Error: Defined as the percentage error (in FSR%) for the ratio between the measured mid-scale output current and the ideal mid-scale output current.

Output Compliance Range: Defined as the minimum and maximum allowable voltage at the output of the current-output DAC. Exceeding this limit may result in reduced reliability of the device or adversely affecting distortion performance.

Reference Voltage Drift: Defined as the maximum change of the reference voltage in ppm per degree Celsius from the value at ambient (25°C) to values over the full operating temperature range.

Noise Spectral Density (NSD): Defined as the difference of power (in dBc) between the output tone signal power and the noise floor of 1 Hz bandwidth within the first Nyquist zone, excluding harmonics.

Signal-to-Noise Ratio (SNR): Defined as the ratio of the rms value of the fundamental output signal to the RMS sum of all other spectral components below the Nyquist frequency, including noise, but excluding the first six harmonics and dc.

REVISION HISTORY

Changes from Original (November 2010) to Revision A **Page**

- Deleted the DAC3172 device 1

Changes from Revision A (November 2010) to Revision B **Page**

- Changed Feature bullet From: High DC Accuracy: ±1 LSB DNL, ±2 LSB INL To: High DC Accuracy: ±0.25 LSB DNL (10-bit), ± 0.5 LSB INL (12-bit) 1
- Added text "The LVPECL clock signal should be AC coupled" to Pin DACCLKP and DACCLKN descriptions. 2
- Added text "The LVPECL clock signal should be AC coupled" to Pin DACCLKP and DACCLKN descriptions. 3
- Added values to the Thermal Information table 4
- Changed the ELECTRICAL CHARACTERISTICS – DC SPECIFICATION table 5
- Added Min and Max values to V_{COM} - Internal common mode 6
- Added Min and Max values to Z_T - Internal termination 6
- Changed the AC Performance Typical values for DAC3152 and DAC3162 7
- Added the Typical Characteristics section 8
- Replaced Signal to Noise Ratio (SNR) with Noise Spectral Density (NSD) 22

Changes from Revision B (December 2011) to Revision C **Page**

- Changed the CLOCK INPUT: DACCLKP/N - Differential voltage MIN value From: 0.4V To: 0.2V for both devices 6
- Deleted Note 2 From the DIGITAL SPECIFICATIONS table- Driving the clock input with a differential voltage lower than 1 V results in degraded performance. 6

Changes from Revision C (February 2012) to Revision D **Page**

- Added Figure 31 12
- Changed Figure 34 15
- Added Figure 35 15
- Moved the DEFINITION OF SPECIFICATIONS to the end of the data sheet 22

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC3152IRGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC3152I	Samples
DAC3152IRGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC3152I	Samples
DAC3162IRGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC3162I	Samples
DAC3162IRGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC3162I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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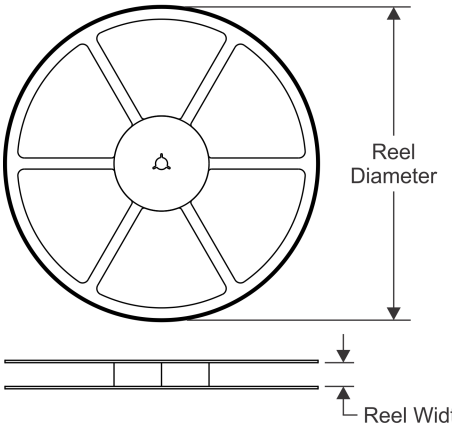
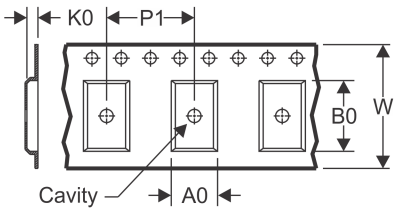
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

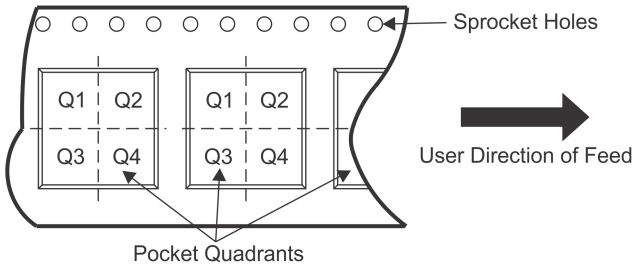


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

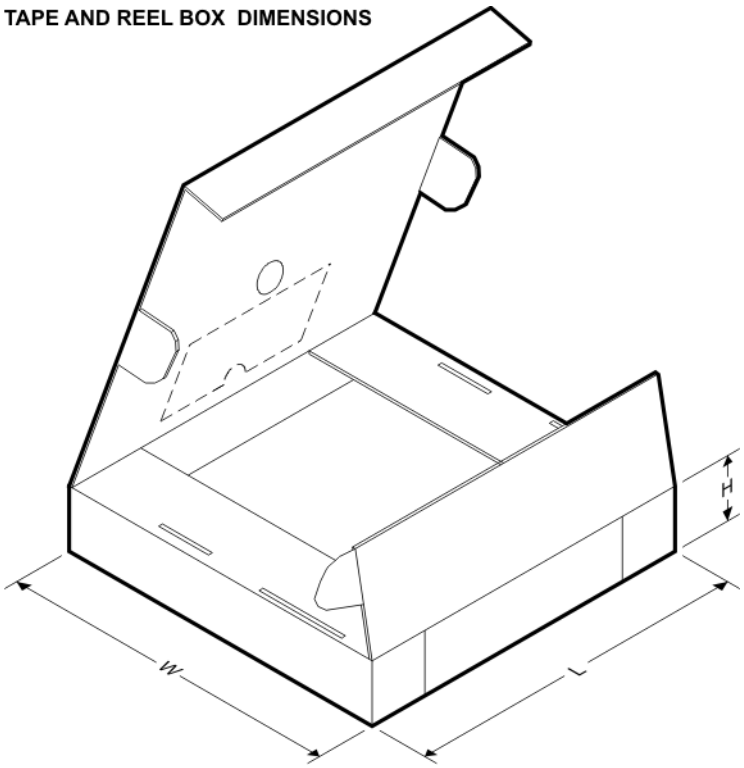
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC3152IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
DAC3162IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC3152IRGZR	VQFN	RGZ	48	2500	350.0	350.0	43.0
DAC3162IRGZR	VQFN	RGZ	48	2500	350.0	350.0	43.0

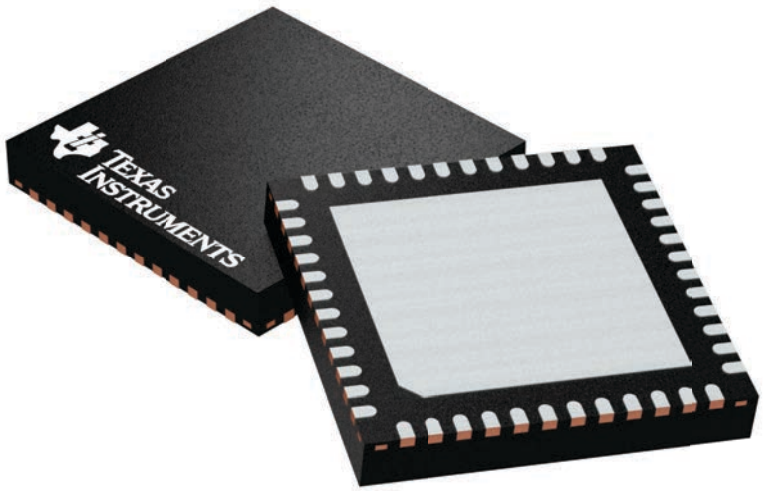
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

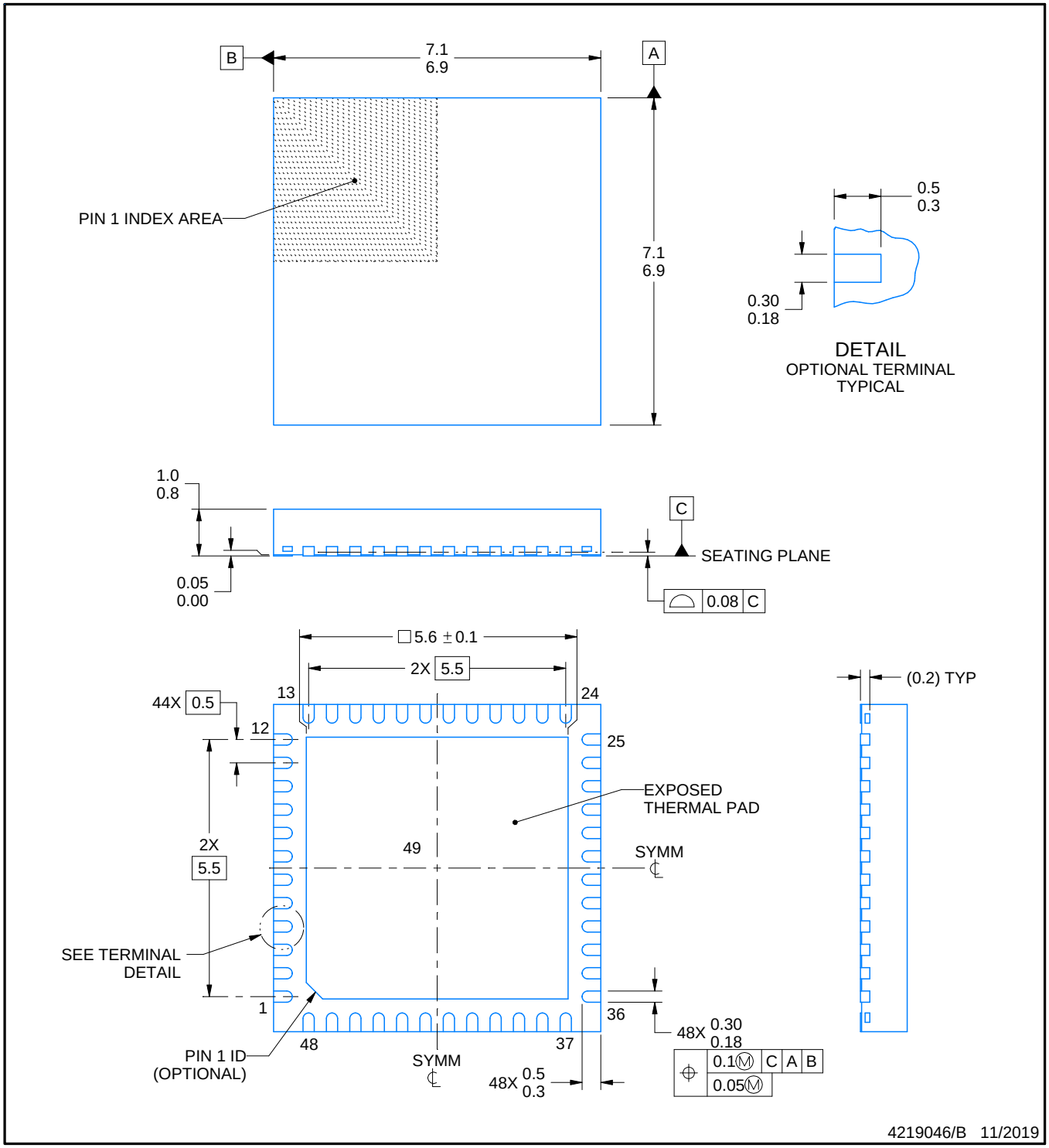
4224671/A

PACKAGE OUTLINE

RGZ0048D

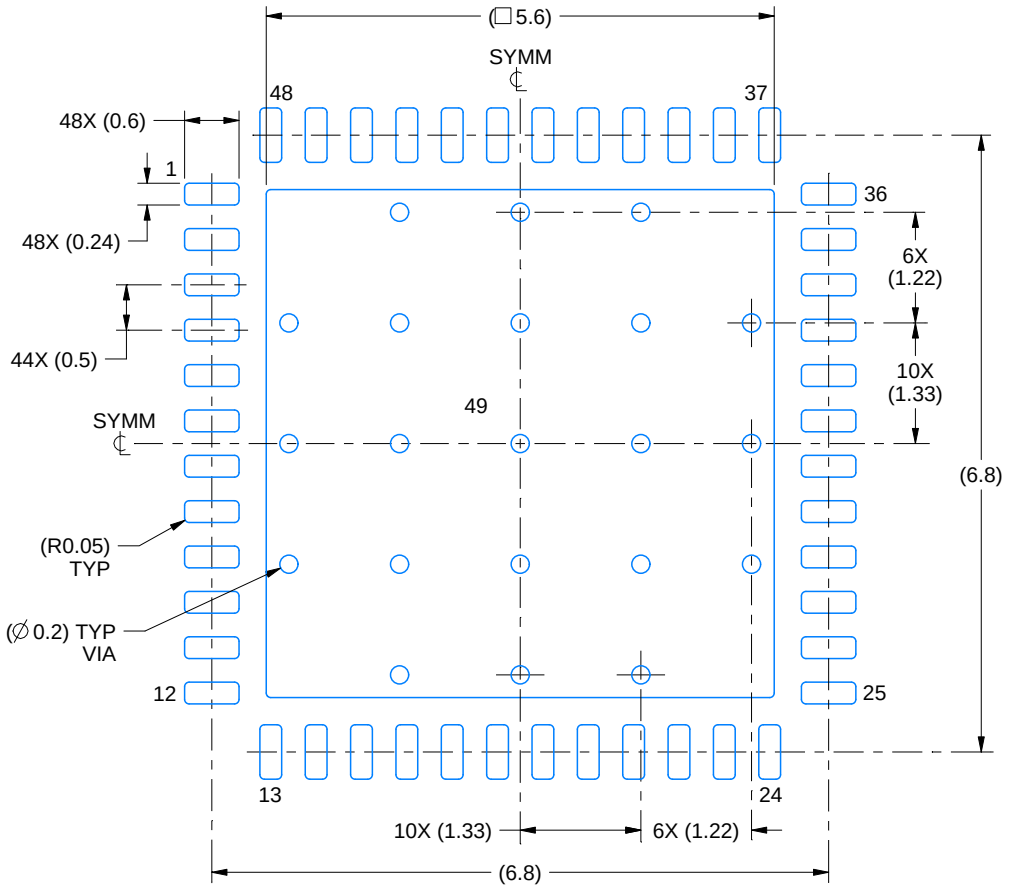
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

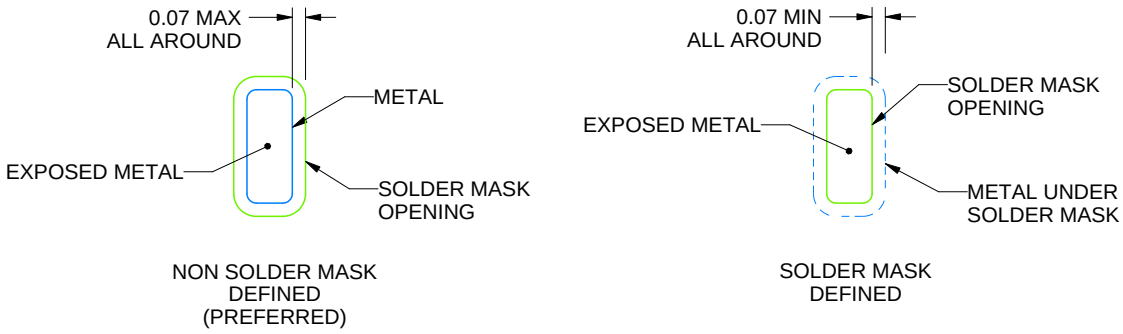


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

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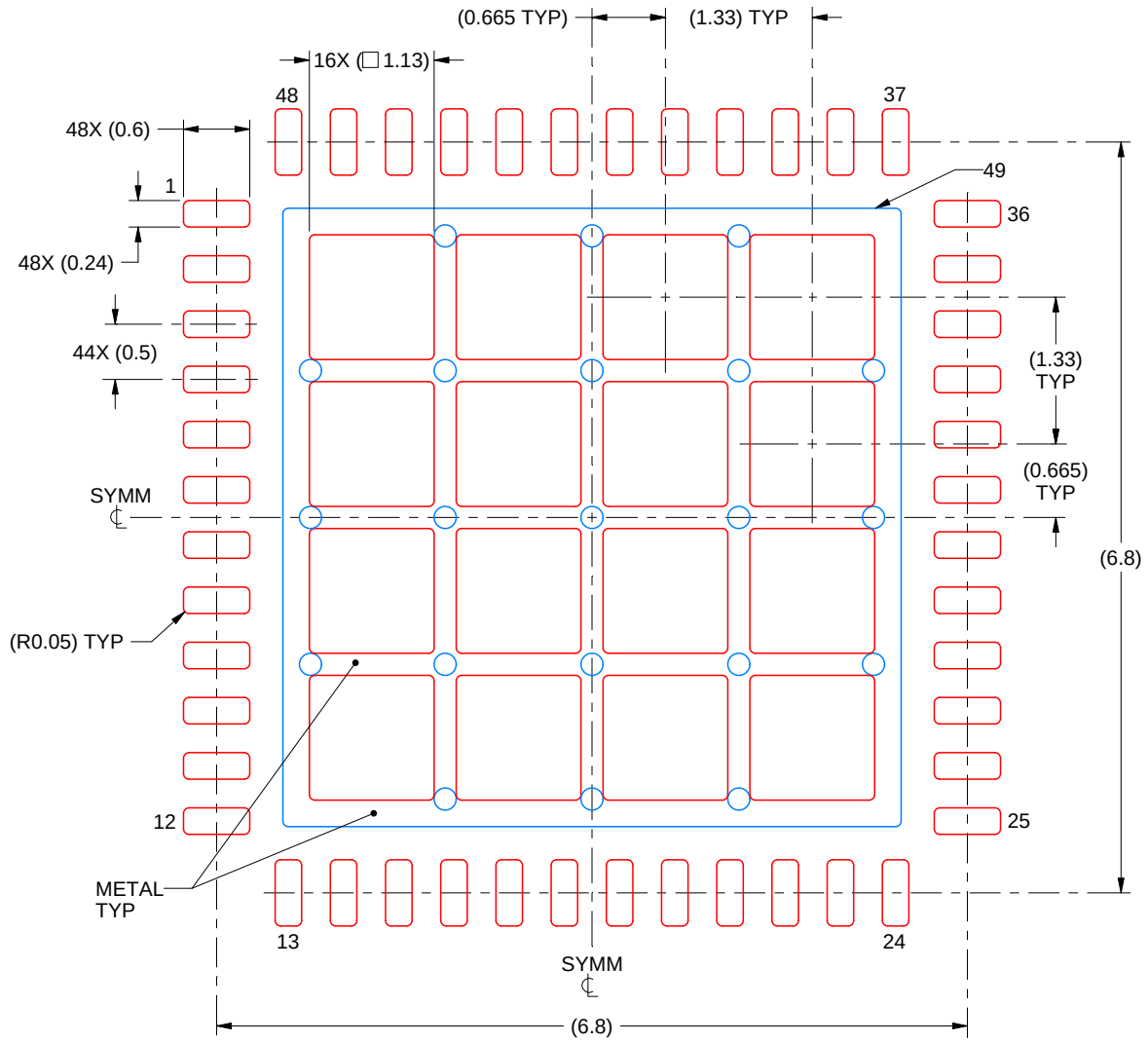
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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