DLP4500 0.45 WXGA DMD

1 特性

- 0.45 英寸对角线微镜阵列
  - 分辨率为 912 × 1140 的阵列（微镜数超过一百万）
  - 菱形阵列定向支持侧面照明，以实现简化高效光学设计
  - 能够支持 WXGA 的显示分辨率
  - 7.6µm 微镜间距
  - ±12° 倾斜角度
  - 5µs 微镜交叉时间
- 高效控制可见光
  - 窗透射率标称值 96%（420 至 700nm，单通道，两个窗面）
  - 偏振无关型铝制微镜
  - 阵列填充因子 92%（标称值）
- 针对可靠运行的专用 DLPC350 控制器
  - 二进制图形速率高达 4kHz
  - 图案序列模式，可对阵列内的每个微镜进行控制
- 集成微镜驱动器电路
- 对于便携式仪器为 9.1mm × 20.7mm
  - FQE 封装，具备简易连接器接口
  - FQD 封装，具备散热增强型接口

™

2 应用

- 机器视觉
  - 3D 深度测量
  - 机器人导引
  - 挤压产品表面缺陷检测
  - 拾取与放置
  - 3D 捕捉
  - 坏点剔除
- 医疗仪器
  - 3D 牙科扫描仪
  - 血管成像
- 3D 生物识别技术
  - 指纹识别
  - 面部识别
- 虚拟量规
- 扩增实境
- 交互式显示屏
- 显微镜

3 说明

DLP4500 数字微镜器件 (DMD) 可用作空间光调制器 (SLM)，以快速、准确且高效地操控可见光光以及生成图案。由于具有高分频率和高亮度以及紧凑的外形，DLP4500 DMD 非常适合工业、医疗和安全应用中所采用的非常精确的便携式 3D 机器视觉与显示解决方案。

器件型号	封装(1)	散热接口区域
DLP4500	LCCC (80) (2)	无
	LCCC (98) (3)	7mm x 7mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。
(2) FQE 封装（241 系列）图。如需更多信息，请参阅《DLP® 241 系列 DMD 和系统安装概念》。
(3) FQD 封装（310 系列）图。如需更多信息，请参阅《DLP® 310 系列 DMD 和系统安装概念》。

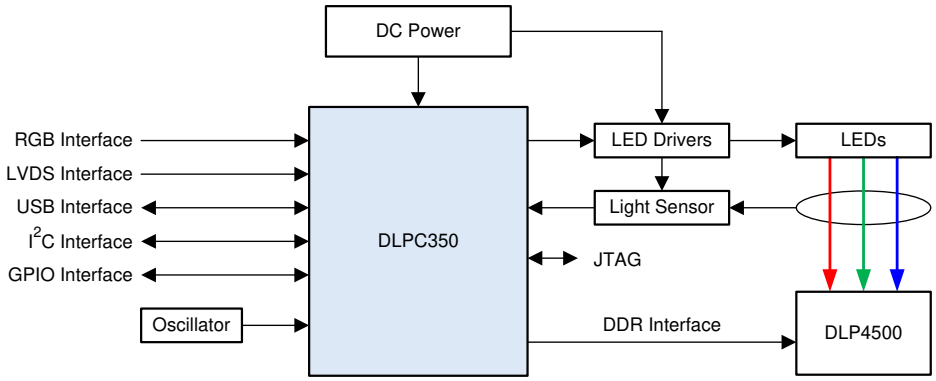

图 3-1. 简化版应用

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (January 2019) to Revision A (October 2021)	Page
• 更新了整个文档中的表、图和交叉参考的编号格式	1
• Updated $\lvert T_{DELTA} \rvert$ MAX from 30°C to 15°C	12

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5 Chipset Component Usage Specification

Note

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

The DLP4500 is a component of one or more ®DLP chipsets. Reliable function and operation of the DLP4500 requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology is the TI technology and devices for operating or controlling a DLP DMD.

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6 Pin Configuration and Functions

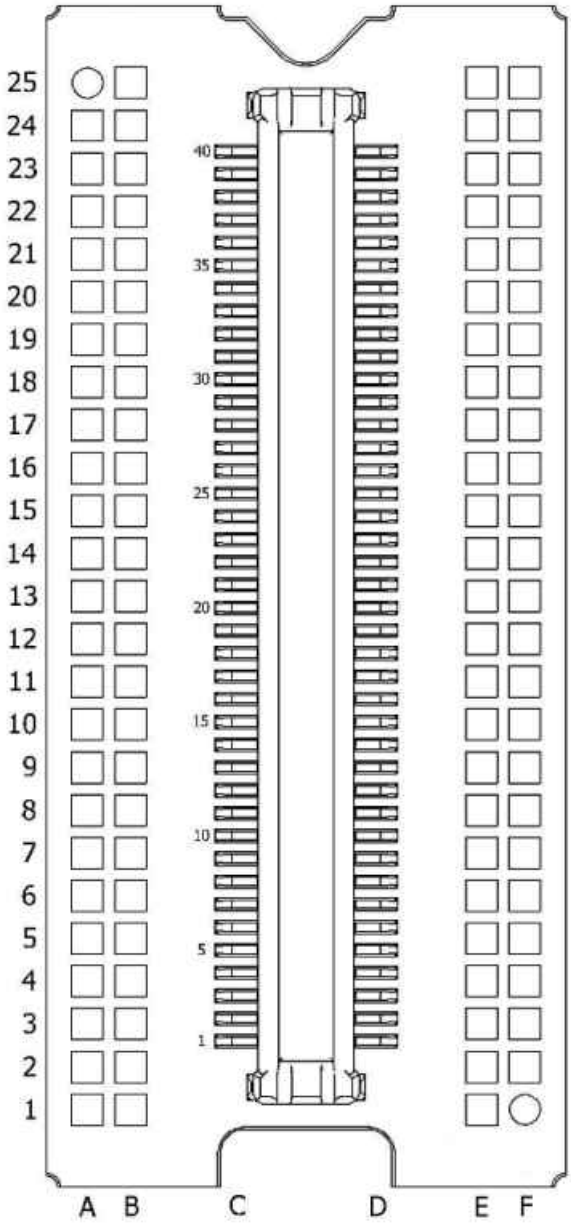

图 6-1. FQE Package. LCCC (80). Bottom View.

Connector Pins for FQE

PIN		TYPE	SIGNAL	DATA RATE (1)	INTERNAL TERMINATION	DESCRIPTION	TRACE (mm) (2)
NAME	NO.						
DATA INPUTS							
DATA(0)	C12	Input	LVCMOS	DDR	none	Input data bus, bit 0, LSB	8.11
DATA(1)	C10	Input	LVCMOS	DDR	none	Input data bus, bit 1	7.82
DATA(2)	C9	Input	LVCMOS	DDR	none	Input data bus, bit 2	7.88
DATA(3)	C7	Input	LVCMOS	DDR	none	Input data bus, bit 3	7.84
DATA(4)	C4	Input	LVCMOS	DDR	none	Input data bus, bit 4	8.10

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PIN		TYPE	SIGNAL	DATA RATE [1]	INTERNAL TERMINATION	DESCRIPTION	TRACE (mm) [2]
NAME	NO.						
DATA(5)	C6	Input	LVCMOS	DDR	none	Input data bus, bit 5	7.89
DATA(6)	C3	Input	LVCMOS	DDR	none	Input data bus, bit 6	7.87
DATA(7)	C13	Input	LVCMOS	DDR	none	Input data bus, bit 7	7.84
DATA(8)	C15	Input	LVCMOS	DDR	none	Input data bus, bit 8	8.13
DATA(9)	C16	Input	LVCMOS	DDR	none	Input data bus, bit 9	8.00
DATA(10)	C18	Input	LVCMOS	DDR	none	Input data bus, bit 10	8.12
DATA(11)	C19	Input	LVCMOS	DDR	none	Input data bus, bit 11	8.08
DATA(12)	C21	Input	LVCMOS	DDR	none	Input data bus, bit 12	9.27
DATA(13)	C22	Input	LVCMOS	DDR	none	Input data bus, bit 13	9.47
DATA(14)	D22	Input	LVCMOS	DDR	none	Input data bus, bit 14	9.46
DATA(15)	D21	Input	LVCMOS	DDR	none	Input data bus, bit 15	8.73
DATA(16)	D19	Input	LVCMOS	DDR	none	Input data bus, bit 16	8.10
DATA(17)	D4	Input	LVCMOS	DDR	none	Input data bus, bit 17	8.02
DATA(18)	D9	Input	LVCMOS	DDR	none	Input data bus, bit 18	8.07
DATA(19)	D10	Input	LVCMOS	DDR	none	Input data bus, bit 19	7.91
DATA(20)	D6	Input	LVCMOS	DDR	none	Input data bus, bit 20	8.52
DATA(21)	D16	Input	LVCMOS	DDR	none	Input data bus, bit 21	9.10
DATA(22)	D7	Input	LVCMOS	DDR	none	Input data bus, bit 22	8.00
DATA(23)	D15	Input	LVCMOS	DDR	none	Input data bus, bit 23, MSB	8.61
DCLK	D13	Input	LVCMOS	DDR	none	Input data bus clock	8.63
DATA CONTROL INPUTS							
$\overline{\text{LOADB}}$	D12	Input	LVCMOS	DDR	none	Parallel-data load enable	8.65
TRC	D3	Input	LVCMOS	DDR	none	Input-data toggle-rate control	4.67
SCTRL	D18	Input	LVCMOS	DDR	none	Serial control bus	9.40
SAC_BUS	D33	Input	LVCMOS	—	none	Stepped address-control serial-bus data	6.56
SAC_CLK	D29	Input	LVCMOS	—	none	Stepped address-control serial bus clock	8.07
MIRROR RESET CONTROL INPUTS							
DRC_BUS	C29	Input	LVCMOS	—	none	DMD reset-control serial bus	8.24
$\overline{\text{DRC_OE}}$	C33	Input	LVCMOS	—	none	Active-low output enable signal for internal DMD reset driver circuitry	4.43
DRC_STROBE	C36	Input	LVCMOS	—	none	Strobe signal for DMD reset control inputs	9.20
POWER INPUTS [3]							
VBIAS	C31	Power			none	Mirror-reset bias voltage	
VBIAS	C32	Power					
VOFFSET	D25	Power			none	Mirror-reset offset voltage	
VOFFSET	D26	Power					
VRESET	D31	Power			none	Mirror-reset voltage	
VRESET	D32	Power					
VREF	C25	Power			none	Power supply for low-voltage CMOS double-data-rate (DDR) interface	
VREF	C26	Power					

PIN		TYPE	SIGNAL	DATA RATE (1)	INTERNAL TERMINATION	DESCRIPTION	TRACE (mm) (2)
NAME	NO.						
VCC	C1	Power			none	Power supply for LVCMOS logic	
VCC	C2	Power					
VCC	C34	Power					
VCC	C35	Power					
VCC	C37	Power					
VCC	C38	Power					
VCC	C39	Power					
VCC	C40	Power					
VCC	D1	Power					
VCC	D2	Power					
VCC	D34	Power					
VCC	D35	Power					
VCC	D37	Power					
VCC	D38	Power					
VCC	D39	Power					
VCC	D40	Power					
VSS	C5	Power			none	Ground – Common return for all power inputs	
VSS	C8	Power					
VSS	C11	Power					
VSS	C14	Power					
VSS	C17	Power					
VSS	C20	Power					
VSS	C23	Power					
VSS	C24	Power					
VSS	C27	Power					
VSS	C28	Power					
VSS	C30	Power					
VSS	D5	Power					
VSS	D8	Power					
VSS	D11	Power					
VSS	D14	Power					
VSS	D17	Power					
VSS	D20	Power					
VSS	D23	Power					
VSS	D24	Power					
VSS	D27	Power					
VSS	D28	Power					
VSS	D30	Power					

(1)
- DDR = Double data rate
- SDR = Single data rate
- Refer to *Timing Requirements* for specifications and relationships.

(2) Net trace lengths inside the package:
- Relative dielectric constant for the FQE package is 9.8.
- Propagation speed = 11.8 / $\sqrt{(9.8)}$ = 3.769 inches/ns.
- Propagation delay = 0.265 ns/inch = 265 ps/inch = 10.43 ps/mm.

(3) The following power supplies are all required to operate the DMD: VSS, VCC, VOFFSET, VBIAS, VRESET.

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表 6-1. Connector Pins for FQE

NAME	PIN	SIGNAL	DESCRIPTION
UNUSED	A1 thru A25	Test pads	Do not connect
	B1 thru B25		
	D36		
	E1 thru E25		
	F1 thru F25		

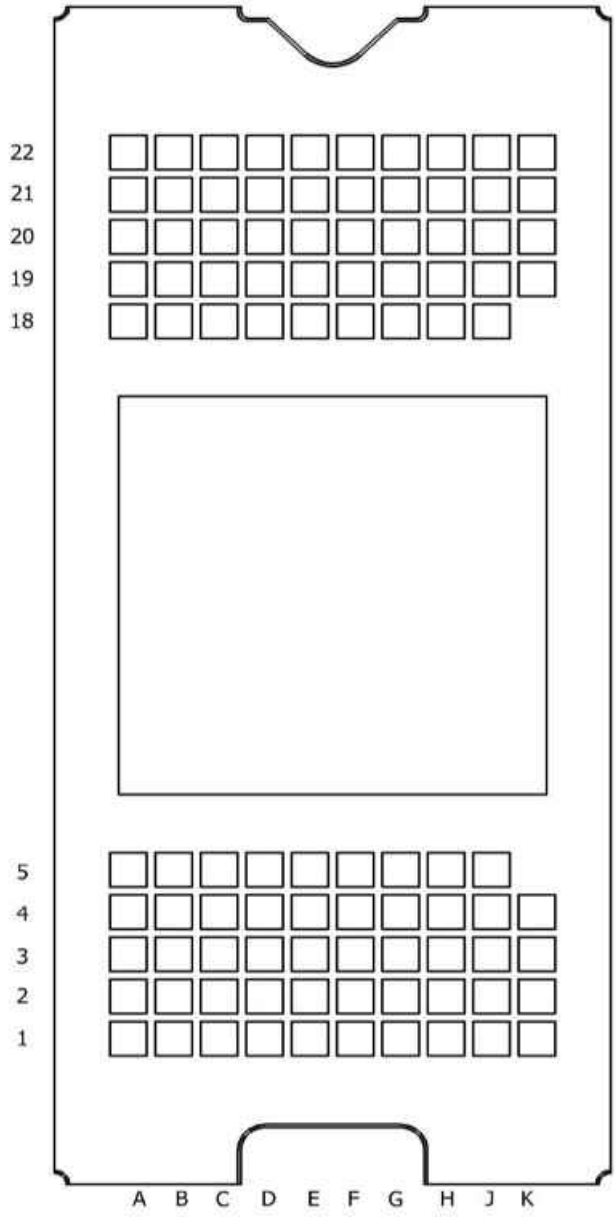

图 6-2. FQD Package LCCC (98) Bottom View

表 6-2. Connector Pins for FQD

PIN		TYPE	SIGNAL	DATA RATE [1]	INTERNAL TERMINATION	DESCRIPTION	PACKAGE NET LENGTH (mm) [2]
NAME	NO.						
DATA INPUTS							
DATA(0)	A1	Input	LVCMOS	DDR	none	Input data bus, bit 0, LSB	3.77
DATA(1)	A2	Input	LVCMOS	DDR	none	Input data bus, bit 1	3.77
DATA(2)	A3	Input	LVCMOS	DDR	none	Input data bus, bit 2	3.73
DATA(3)	A4	Input	LVCMOS	DDR	none	Input data bus, bit 3	3.74
DATA(4)	B1	Input	LVCMOS	DDR	none	Input data bus, bit 4	3.79
DATA(5)	B3	Input	LVCMOS	DDR	none	Input data bus, bit 5	3.75
DATA(6)	C1	Input	LVCMOS	DDR	none	Input data bus, bit 6	3.72
DATA(7)	C3	Input	LVCMOS	DDR	none	Input data bus, bit 7	3.75
DATA(8)	C4	Input	LVCMOS	DDR	none	Input data bus, bit 8	3.78
DATA(9)	D1	Input	LVCMOS	DDR	none	Input data bus, bit 9	3.75
DATA(10)	D4	Input	LVCMOS	DDR	none	Input data bus, bit 10	3.77
DATA(11)	E1	Input	LVCMOS	DDR	none	Input data bus, bit 11	3.75
DATA(12)	E4	Input	LVCMOS	DDR	none	Input data bus, bit 12	3.71
DATA(13)	F1	Input	LVCMOS	DDR	none	Input data bus, bit 13	3.76
DATA(14)	F3	Input	LVCMOS	DDR	none	Input data bus, bit 14	3.73
DATA(15)	G1	Input	LVCMOS	DDR	none	Input data bus, bit 15	3.72
DATA(16)	G2	Input	LVCMOS	DDR	none	Input data bus, bit 16	3.77
DATA(17)	G4	Input	LVCMOS	DDR	none	Input data bus, bit 17	3.73
DATA(18)	H1	Input	LVCMOS	DDR	none	Input data bus, bit 18	3.74
DATA(19)	H2	Input	LVCMOS	DDR	none	Input data bus, bit 19	3.76
DATA(20)	H4	Input	LVCMOS	DDR	none	Input data bus, bit 20	3.70
DATA(21)	J1	Input	LVCMOS	DDR	none	Input data bus, bit 21	3.77
DATA(22)	J3	Input	LVCMOS	DDR	none	Input data bus, bit 22	3.76
DATA(23)	J4	Input	LVCMOS	DDR	none	Input data bus, bit 23, MSB	3.77
DCLK	K1	Input	LVCMOS	DDR	none	Input data bus clock	3.74
DATA CONTROL INPUTS							
$\overline{\text{LOADB}}$	K2	Input	LVCMOS	DDR	none	Parallel-data load enable	3.74
TRC	K4	Input	LVCMOS	DDR	none	Input-data toggle rate control	4.70
SCTRL	K3	Input	LVCMOS	DDR	none	Serial-control bus	3.75
SAC_BUS	C20	Input	LVCMOS	—	none	Stepped address-control serial-bus data	3.77
SAC_CLK	C22	Input	LVCMOS	—	none	Stepped address-control serial-bus clock	1.49
MIRROR RESET CONTROL INPUTS							
DRC_BUS	B21	Input	LVCMOS	—	none	DMD reset-control serial bus	3.73
$\overline{\text{DRC_OE}}$	A20	Input	LVCMOS	—	none	Active-low output enable signal for internal DMD reset driver circuitry	3.74
DRC_STROBE	A22	Input	LVCMOS	—	none	Strobe signal for DMD reset-control inputs	3.73
POWER INPUTS [3]							
VBIAS	C19	Power				Mirror-reset bias voltage	
VBIAS	D19	Power					
VOFFSET	A19	Power				Mirror-reset offset voltage	
VOFFSET	K19	Power					

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表 6-2. Connector Pins for FQD (continued)

PIN		TYPE	SIGNAL	DATA RATE (1)	INTERNAL TERMINATION	DESCRIPTION	PACKAGE NET LENGTH (mm) (2)
NAME	NO.						
VRESET	E19	Power				Mirror-reset voltage	
VRESET	F19	Power					
VREF	B19	Power				Power supply for LVCMOS double-data-rate (DDR) interface	
VREF	J19	Power					
VCC	B22	Power				Power supply for LVCMOS logic	
VCC	C2	Power					
VCC	D21	Power					
VCC	E2	Power					
VCC	E20	Power					
VCC	E22	Power					
VCC	F21	Power					
VCC	G3	Power					
VCC	G19	Power					
VCC	G20	Power					
VCC	G22	Power					
VCC	H19	Power					
VCC	H21	Power					
VCC	J20	Power					
VCC	J22	Power					
VCC	K21	Power					
VSS	A21	Power				Ground – Common return for all power inputs	
VSS	B2	Power					
VSS	B4	Power					
VSS	B20	Power					
VSS	C21	Power					
VSS	D2	Power					
VSS	D3	Power					
VSS	D20	Power					
VSS	D22	Power					
VSS	E3	Power					
VSS	E21	Power					
VSS	F2	Power					
VSS	F4	Power					
VSS	F20	Power					
VSS	F22	Power					
VSS	G21	Power					
VSS	H3	Power					
VSS	H20	Power					
VSS	H22	Power					
VSS	J2	Power					
VSS	J21	Power					
VSS	K20	Power					

(1)
- DDR = Double data rate
- SDR = Single data rate

- Refer to *Timing Requirements* for specifications and relationships.

(2) Net trace lengths inside the package:

- Relative dielectric constant for the FQD ceramic package is 9.8.
- Propagation speed = 11.8 / sqrt(9.8) = 3.769 inches/ns.
- Propagation delay = 0.265 ns/inch = 265 ps/inch = 10.43 ps/mm.

(3) The following power supplies are all required to operate the DMD: VSS, VCC, VOFFSET, VBIAS, VRESET.

表 6-3. Pin Configuration and Functions – Test Pads for FQD Package

NAME	PIN	SIGNAL	DESCRIPTION
UNUSED	A5, A18, B5, B18, C5, C18, D5, D18, E5, E18, F5, F18, G5, G18, H5, H18, J5, J18, K22	Test pads	Do not connect

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
SUPPLY VOLTAGES (2)					
VCC	Supply voltage for LVCMOS core logic		– 0.5	4	V
VREF	Supply voltage for LVCMOS DDR interface		– 0.5	4	V
VOFFSET	Supply voltage for high voltage CMOS and micromirror electrode		– 0.5	8.75	V
VBIAS (3)	Supply voltage for micromirror electrode		– 0.5	17	V
VRESET	Supply voltage for micromirror electrode		– 11	0.5	V
|VBIAS - VOFFSET| (3)	Supply voltage delta (absolute value)			8.75	V
INPUT VOLTAGES (2)					
	Input voltage to all other input pins		– 0.5	VREF + 0.5	V
INPUT CURRENTS					
	Current required from a high-level output	V_{OH} = 1.4 V		– 9	mA
	Current required from a low-level output	V_{OL} = 0.4 V		18	mA
CLOCKS					
f_{CLK}	DCLK clock frequency		80	120	MHz
ENVIRONMENTAL					
T_{CASE}	Case temperature - operational (4)		– 20	90	°C
	Case temperature - non-operational (4)		– 40	90	°C
T_{DP}	Dew Point (operation and non-operational)			81	°C
	Operating Relative Humidity (non-condensing)		0	95	%RH

(1) Stresses beyond those listed under 节 7.1 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device is not implied at these or any conditions beyond those indicated under 节 7.4. Exposure above Recommended Operating Conditions for extended periods may affect device reliability.
(2) All voltage values are referenced to common ground VSS. Supply voltages VCC, VREF, VOFFSET, VBIAS, and VRESET are all required for proper DMD operation. VSS must also be connected.
(3) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than the specified limit.
(4) DMD Temperature is the worst-case of any test point shown in 图 8-3 or 图 8-4, or the active array as calculated by the Micromirror Array Temperature Calculation, or any point along the Window Edge as defined in 图 8-3 or 图 8-4. The locations of thermal test point TP2 is intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, a test point should be added to that location.

7.2 Storage Conditions

applicable before the DMD is installed in the final product

		MIN	MAX	UNIT
T_{stg}	Storage temperature (1)	– 40	85	°C
	Storage humidity, non-condensing (1)	0	95%	RH
	Long-term storage dew point (1) (2)		24	°C
	Short-term storage dew point (1) (3)		28	°C

(1) As a best practice, TI recommends storing the DMD in a temperature and humidity controlled environment.
(2) Long-term is defined as the average over the usable life.
(3) Short-term is defined as <60 cumulative days over the usable life of the device.

7.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) (2) (3)	±2000	V

(1) *ESD Ratings* are applicable before the DMD is installed in final product.
(2) All CMOS devices require proper Electrostatic Discharge (ESD) handling procedures.
(3) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
SUPPLY VOLTAGES (1)					
VCC	Supply voltage for LVCMOS core logic	2.375	2.5	2.625	V
VREF	Supply voltage for LVCMOS DDR interface	1.6	1.9	2	V
VOFFSET	Supply voltage for HVCMOS and micromirror electrode (3) (2)	8.25	8.5	8.75	V
VBIAS	Supply voltage for micromirror electrode (3)	15.5	16	16.5	V
VRESET	Supply voltage for micromirror electrode	–9.5	–10	–10.5	V
|VBIAS – VOFFSET|	Supply voltage delta (absolute value) (3)			8.75	V
VOLTAGE RANGE					
V_{T+}	Positive-going threshold voltage	0.4 × VREF		0.7 × VREF	V
V_{T-}	Negative-going threshold voltage	0.3 × VREF		0.6 × VREF	V
V_{hys}	Hysteresis voltage (V_{T+} – V_{T-})	0.1 × VREF		0.4 × VREF	V
CLOCK FREQUENCY					
$f_{(CLK)}$	DCLK clock frequency	80		120	MHz
ENVIRONMENTAL (4)					
T_{DMD}	DMD temperature - operational, long-term (5) (7)	10		40 to 70 (6)	°C
	DMD temperature - operational, short-term	–20		70	°C
T_{Window}	DMD window temperature - operational	0		90	°C
$T_{CERAMIC-WINDOW-DELTA}$	DMD |ceramic TP1 - window| temperature delta - operational (8) (10)	0		15	°C
	DMD long-term dewpoint (operational, non-operational)			24	°C
	DMD short-term dewpoint (operational, non-operational) (9)			28	°C
ILLUMINATION					
ILL_{UV-VIS}	Illumination power - spectral region <420 nm			0.68	mW/cm^2
ILL_{VIS}	Illumination power - spectral region 420 to 700 nm, FQE package			Thermally Limited (11)	mW/cm^2
	Illumination power - spectral region 420 to 700 nm, FQD package			Thermally Limited (11)	mW/cm^2
ILL_{IR}	Illumination power - spectral region >700 nm			10	mW/cm^2

(1) Supply voltages VCC, VREF, VOFFSET, VBIAS, and VRESET are all required for proper DMD operation. All voltage values are referenced to common ground VSS.
(2) VOFFSET supply transients must fall within specified max voltages.
(3) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit.
(4) Optimal long-term performance and optical efficiency of the digital micromirror device (DMD) can be affected by various application parameters, including illumination spectrum, illumination power density, micromirror landed duty cycle, ambient temperature (storage and operating), DMD temperature, ambient humidy (storage and operating), and power on or off duty cycle.
(5) DMD temperature is the worst-case of any test point shown in 图 8-3 or 图 8-4, or the active array as calculated by the *Micromirror Array Temperature Calculation*, or any point along the window edge as defined in 图 8-3 or 图 8-4. The locations of thermal test point TP2 in 图 8-3 or 图 8-4 is intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, a test point should be added to that location.

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(6) Per 图 7-1, the maximum operational case temperature at test points TP1 and TP2 as shown in 图 8-3 or 图 8-4 should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. Refer to *Micromirror Landed-on/Landed-Off Duty Cycle* for a definition of landed duty cycle.
(7) Long-term is defined as the average over the usable life.
(8) Ceramic package and window temperature as measured at test points TP1 and TP2 in 图 8-3 or 图 8-4.
(9) Dew points beyond the specified long-term dew point (operating, non-operating, or storage) are for short-term conditions only, where short-term is defined as <60 cumulative days over the useful life of the device.
(10) Between any two points on or within the package including the mirror array.
(11) Refer to *Micromirror Array Temperature Calculation* and *Temperature Calculation* for information related to calculating the micromirror array temperature.

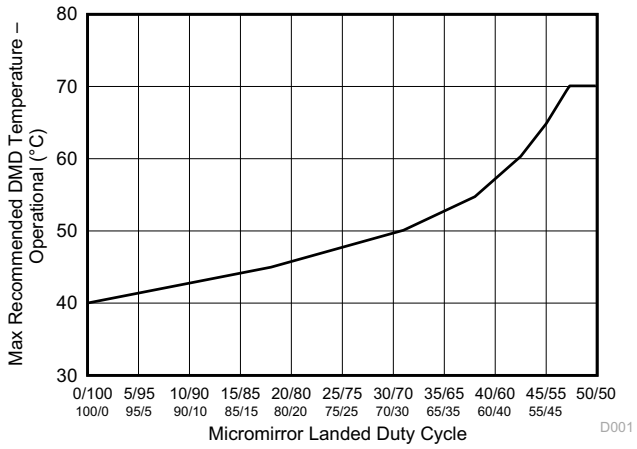

图 7-1. Maximum Recommended DMD Temperature – Derating Curve

7.5 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC	DLP4500		UNIT
	FQE (LCCC)	FQD (LCCC)	
	80 PINS	98 PINS	
Thermal resistance - Active area to case ceramic	2	2	°C/W

7.6 Electrical Characteristics

over the range of recommended supply voltage and recommended case operating temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
I_{IL}	Low-level input current (1)	VREF = 2.00 V, V_I = 0 V	–50			nA
I_{IH}	High-level input current (1)	VREF = 2.00 V, V_I = VREF			50	nA
CURRENT						
I_{REF}	Current into VREF pin	VREF = 2.00 V, f_{DCLK} = 120 MHz		2.15	2.75	mA
I_{CC}	Current into VCC pin	VCC = 2.75 V, f_{DCLK} = 120 MHz		125	160	mA
I_{OFFSET}	Current into VOFFSET pin (2)	VOFFSET = 8.75 V, Three global resets within time period = 200 μs		3	3.3	mA
I_{BIAS}	Current into VBIAS pin (2) (3)	VBIAS = 16.5 V, Three global resets within time period = 200 μs		2.55	6.5	mA
I_{RESET}	Current into VRESET pin	VRESET = –10.5 V		2.45	3.1	mA
I_{TOTAL}				135.15	175.65	mA
POWER						
P_{REF}	Power into VREF pin (4)	VREF = 2.00 V, f_{DCLK} = 120 MHz		4.15	5.5	mW
P_{CC}	Power into VCC pin (4)	VCC = 2.75 V, f_{DCLK} = 120 MHz		343.75	440	mW

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
P_{OFFSET}	Power into VOFFSET pin (4)	VOFFSET = 8.75 V, Three global resets within time period = 200 μs		26.25	28.9	mW
P_{BIAS}	Power into VBIAS pin (4)	VBIAS = 16.5 V, Three global resets within time period = 200 μs		42.1	58.6	mW
P_{RESET}	Power into VRESET pin (4)	VRESET = –10.5 V		25.71	32.6	mW
P_{TOTAL}				442	566	mW
CAPACITANCE						
C_I	Input capacitance	f = 1 MHz			10	pF
C_O	Output capacitance	f = 1 MHz			10	pF

(1) Applies to LVCMOS pins only. LVCMOS pins do not have pullup or pulldown configurations.
(2) Exceeding the maximum allowable absolute voltage difference between VBIAS and VOFFSET may result in excess current draw. See the 节 7.1 for further details.
(3) When $\overline{DRC_OE}$ = HIGH, the internal reset drivers are tri-stated and I_{BIAS} standby current is 6.5 mA.
(4) In some applications, the total DMD heat load can be dominated by the amount of incident light energy absorbed. See the 节 8.5 for further details.

7.7 Timing Requirements

Over operating free-air temperature range (unless otherwise noted). This data sheet provides timing at the device pin.

		MIN	NOM	MAX	UNIT
$t_{su(1)}$	Setup time: DATA before rising or falling edge of DCLK (1)	0.7			ns
	Setup time: TRC before rising or falling edge of DCLK (1)	0.7			
	Setup time: SCTRL before rising or falling edge of DCLK (1)	0.7			
$t_{su(2)}$	Setup time: $\overline{LOADB}$ low before rising edge of DCLK (1)	0.7			ns
$t_{su(3)}$	Setup time: SAC_BUS low before rising edge of SAC_CLK (1)	1			ns
$t_{su(4)}$	Setup time: DRC_BUS high before rising edge of SAC_CLK (1)	1			ns
$t_{su(5)}$	Setup time: DRC_STROBE high before rising edge of SAC_CLK (1)	2			ns
$t_{h(1)}$	Hold time: DATA after rising or falling edge of DCLK (1)	0.7			ns
	Hold time: TRC after rising or falling edge of DCLK (1)	0.7			
	Hold time: SCTRL after rising or falling edge of DCLK (1)	0.7			
$t_{h(2)}$	Hold time: $\overline{LOADB}$ low after falling edge of DCLK (1)	0.7			ns
$t_{h(3)}$	Hold time: SAC_BUS low after rising edge of SAC_CLK (1)	1			ns
$t_{h(4)}$	Hold time: DRC_BUS after rising edge of SAC_CLK (1)	1			ns
$t_{h(5)}$	Hold time: DRC_STROBE after rising edge of SAC_CLK (1)	2			ns
t_r	Rise time (20% to 80%): DCLK / SAC_CLK, VREF = 1.8 V			1.08	ns
	Rise time (20% to 80%): DATA / TRC / SCTRL / $\overline{LOADB}$, VREF = 1.8 V			1.08	
t_f	Fall time (20% to 80%): DCLK / SAC_CLK, VREF = 1.8 V			1.08	ns
	Fall time (20% to 80%): DATA / TRC / SCTRL / $\overline{LOADB}$			1.08	
t_{c1}	Clock cycle: DCLK	8.33	10	12.5	ns
t_{c3}	Clock cycle: SAC_CLK	12.5	13.33	14.3	ns
t_{w1}	Pulse width high or low: DCLK	3.33			ns
t_{w2}	Pulse width low: $\overline{LOADB}$	4.73			ns
t_{w3}	Pulse width high or low: SAC_CLK	5			ns
t_{w5}	Pulse width high: DRC_STROBE	7			ns

(1) Setup and hold times shown are for fast input slew rates >1 V/ns. For slow slew rates >0.5 V/ns and <1 V/ns, the setup and hold times are longer. For every 0.1 V/ns decrease in slew rate from 1 V/ns, add 150 ps on setup and hold.

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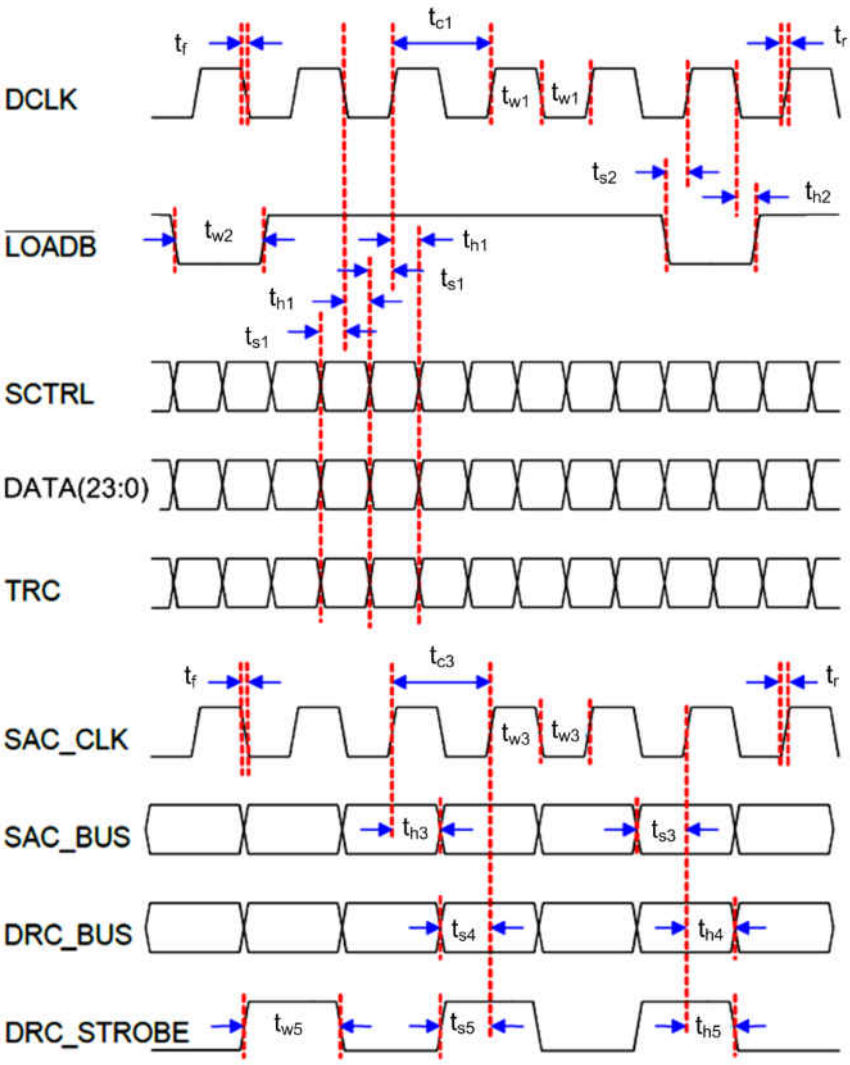

图 7-2. Timing Diagram

7.8 System Mounting Interface Loads

			MIN	NOM	MAX	UNIT
Static load applied to the package electrical connector area (1)	FQE package (3)	Uniformly distributed across the three datum-A areas and the datum-E area.			110	N
Static load applied to the DMD mounting area (1)					110	N
Load applied to the thermal interface area (2)	FQD package (4)	Uniformly distributed over Thermal Interface area			62	N
Load applied to the electrical interface areas (2)		Uniformly distributed over each of the two areas			55	N

(1) See 节 13 for diagrams.
(2) See 图 7-4 for diagrams.
(3) See Mounting Concepts DLP4500FQE.
(4) See Mounting Concepts DLP4500FQD.

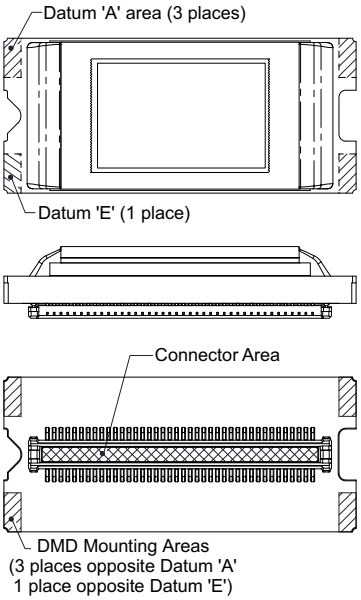

图 7-3. System Interface Loads for FQE

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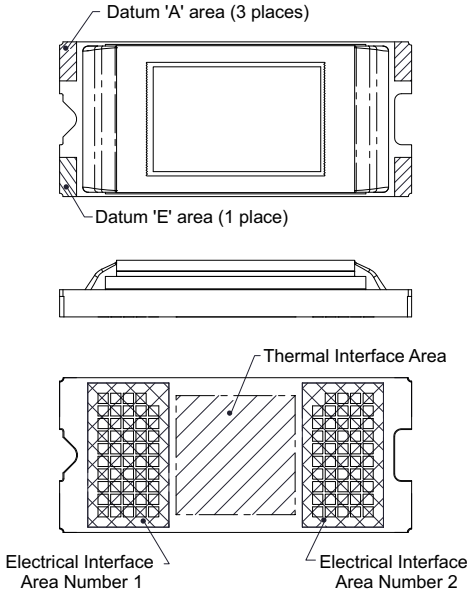

图 7-4. System Interface Loads for FQD

7.9 Micromirror Array Physical Characteristics

	VALUE	UNIT
Number of active micromirror rows (2)	1140	micromirrors
Number of active micromirror columns (2)	912	micromirrors
Micromirror pitch, diagonal (2)	7.6	µm
Micromirror pitch, vertical and horizontal (2)	10.8	µm
Micromirror active array height (3)	1140	micromirrors
	6161.4	µm
Micromirror active array width (3)	912	micromirrors
	9855	µm
Micromirror array border (1)	10	mirrors/side

(1) The mirrors that form the array border are hard-wired to tilt in the –12° (“Off”) direction once power is applied to the DMD (see *图 8-1* and *图 8-2*).
(2) See *图 8-1*.
(3) See Micromirror Active Area in *图 7-5*.

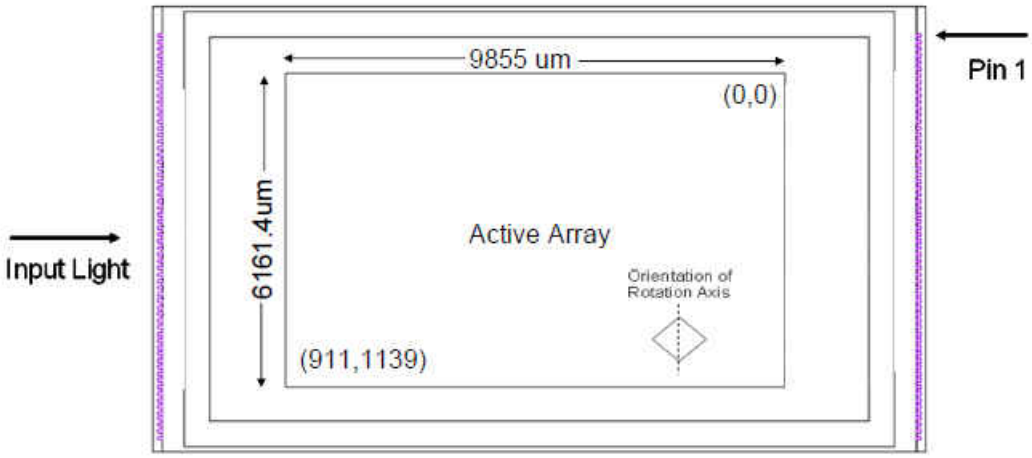

图 7-5. DLP4500 Micromirror Active Area

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7.10 Micromirror Array Optical Characteristics

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. See the related application reports in 节 12.3.1 for specificguidelines.

表 7-1. Micromirror Array Optical Characteristics

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
α	Micromirror tilt angle	DMD *parked* state (1) (3) (4), see (10)		0		degrees
		DMD *landed* state (1) (5) (6), see (10)	11	12	13	
β	Micromirror tilt angle variation (1) (5) (7) (8) (9)	See (10)	–1		1	degrees
	Micromirror crossover time (2) (12)			5		µs
	Micromirror switching time (12)			16		µs
	Non-operating micromirrors (11)	Non-adjacent micromirrors			10	micromirrors
		Adjacent micromirrors			0	
	Orientation of the micromirror axis-of-rotation (13)		89	90	91	degrees
	Micromirror array fill factor (14) (15) (18)	f/3 illumination at 24 degree angle, mirrors tilted toward illumination		92%		
	Mirror metal specular reflectivity (14) (15)	420 nm to 700 nm		89%		
	Window material			Corning Eagle XG		
	Window aperture			See (16)		
	Illumination overfill (17)			See (17)		
	Window transmittance (single pass through two window surfaces) (14) (15)	420 nm to 700 nm, See		96%		

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Micromirror crossover time is primarily a function of the natural response time of the micromirrors.
(3) *Parking* the micromirror array returns all of the micromirrors to a relatively flat (0˚) state (as measured relative to the plane formed by the overall micromirror array).
(4) When the micromirror array is *parked*, the tilt angle of each individual micromirror is uncontrolled.
(5) Additional variation exists between the micromirror array and the package datums.
(6) When the micromirror array is *landed*, the tilt angle of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror *landing* in an nominal angular position of +12°. A binary value of 0 results in a micromirror *landing* in an nominal angular position of –12°.
(7) Represents the *landed* tilt angle variation relative to the nominal *landed* tilt angle
(8) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(9) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations or system contrast variations.
(10) See 图 8-2.
(11) Non-operating micromirror is defined as a micromirror that is unable to transition nominally from the –12° position to +12° or vice versa.
(12) Performance as measured at the start of life.
(13) Measured relative to the package datums B and C, shown in the Package Mechanical Data section in *节 13*.
(14) The nominal DMD total optical efficiency results from the following four components:
- Micromirror array fill factor
- Micromirror array diffraction efficiency
- Micromirror surface reflectivity (very similar to the reflectivity of bulk Aluminum)
- Window Transmission (single pass through two surfaces for incoming light, and single pass through two surfaces for reflected light)

(15) The DMD diffraction efficiency and total optical efficiency observed in a specific application depends on numerous application-specific design variables, such as:
- Illumination wavelength, bandwidth or line-width, degree of coherence
- Illumination angle, plus angle tolerence
- Illumination and projection aperture size, and location in the system optical path

- Illumination overfill of the DMD micromirror array
- Aberrations present in the illumination source or path, or both
- Aberrations present in the projection path

Does not account for the effect of micromirror switching duty cycle, which is application dependent. Micromirror switching duty cycle represents the percentage of time that the micromirror is actually reflecting light from the optical illumination path to the optical projection path. This duty cycle depends on the illumination aperture size, the projection aperture size, and the micromirror array update rate.

(16) See the Package Mechanical Characteristics in 节 13for details regarding the size and location of the window aperture.

(17) The active area of the DLP4500 device is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can scatter and create adverse effects to the performance of an end application using the DMD. Design the illumination optical system as to limit light flux incident outside the active array to less than 10% of the light flux level in the active area. Depending on the particular system's optical architecture and assembly tolerances, the amount of overfill light on the outside of the active array may cause system performance degradation .

(18) The Micromirror array fill factor depends on numerous application-specific design variables, such as:

- Illumination angle, plus angle tolerance
- Illumination and projection aperture size, and location in the system optical path

7.11 Typical Characteristics

Single pass through two window surfaces.

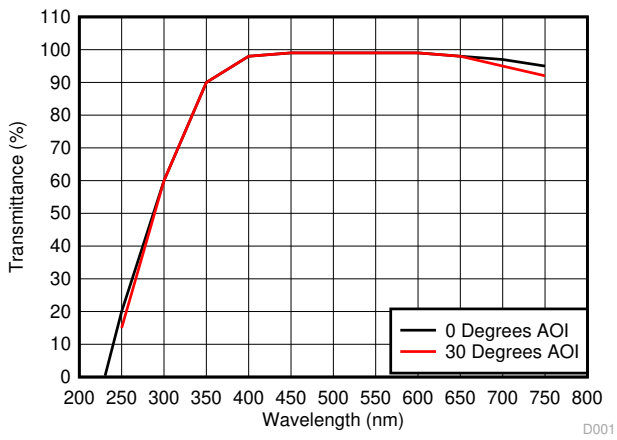

图 7-6. DLP4500 DMD Window Transmittance

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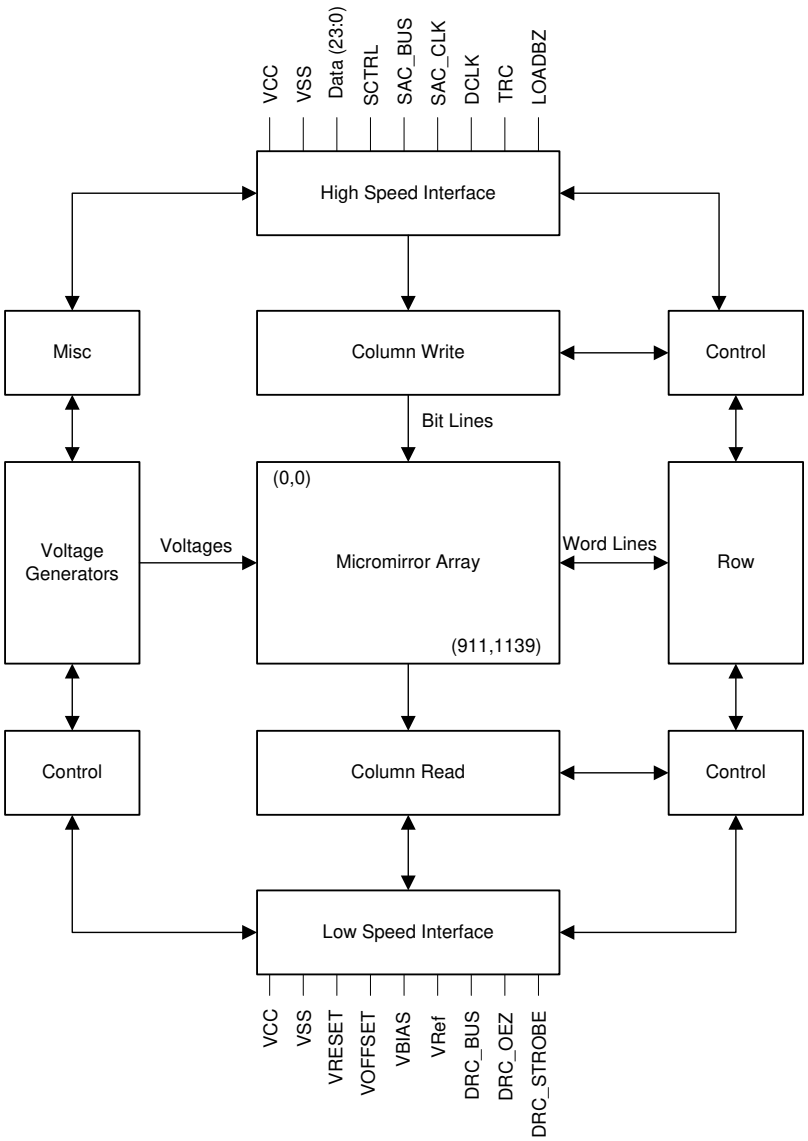
8 Detailed Description

8.1 Overview

Electrically, the DLP4500 device consists of a two-dimensional array of 1-bit CMOS memory cells, organized in a grid of 912 memory cell columns by 1140 memory cell rows. The CMOS memory array is addressed on a column-by-column basis, over a 24-bit DDR bus. Addressing is handled through a serial control bus. The specific CMOS memory access protocol is handled by the DLPC350 digital controller.

Optically, the DLP4500 device consists of 1039680 highly reflective, digitally switchable, micrometer-sized mirrors (micromirrors) organized in a two-dimensional array. The micromirror array consists of 912 micromirror columns by 1140 micromirror rows in diamond pixel configuration (图 8-1). Due to the diamond pixel configuration, the columns of each odd row are offset by half a pixel from the columns of the even row.

8.2 Functional Block Diagram



8.3 Feature Description

Each aluminum micromirror is approximately 7.6 microns in size and arranged in row and columns as shown in 图 8-1. Due to the diamond pixel array of the DMD, the pixel data does not appear on the DMD exactly as it would in an orthogonal pixel arrangement. Pixel arrangement and numbering for the DLP4500 is shown in 图 8-1.

Each micromirror is switchable between two discrete angular positions: –12° and 12°. The angular positions α and β are measured relative to a 0° *flat reference when the mirrors are parked in their inactive state*, parallel to the array plane (see 图 8-2). The parked position is not a latched position. Individual micromirror angular positions are relatively flat, but do vary. The tilt direction is perpendicular to the hinge-axis. The on-state landed position is directed toward the left side of the package (see 图 8-2).

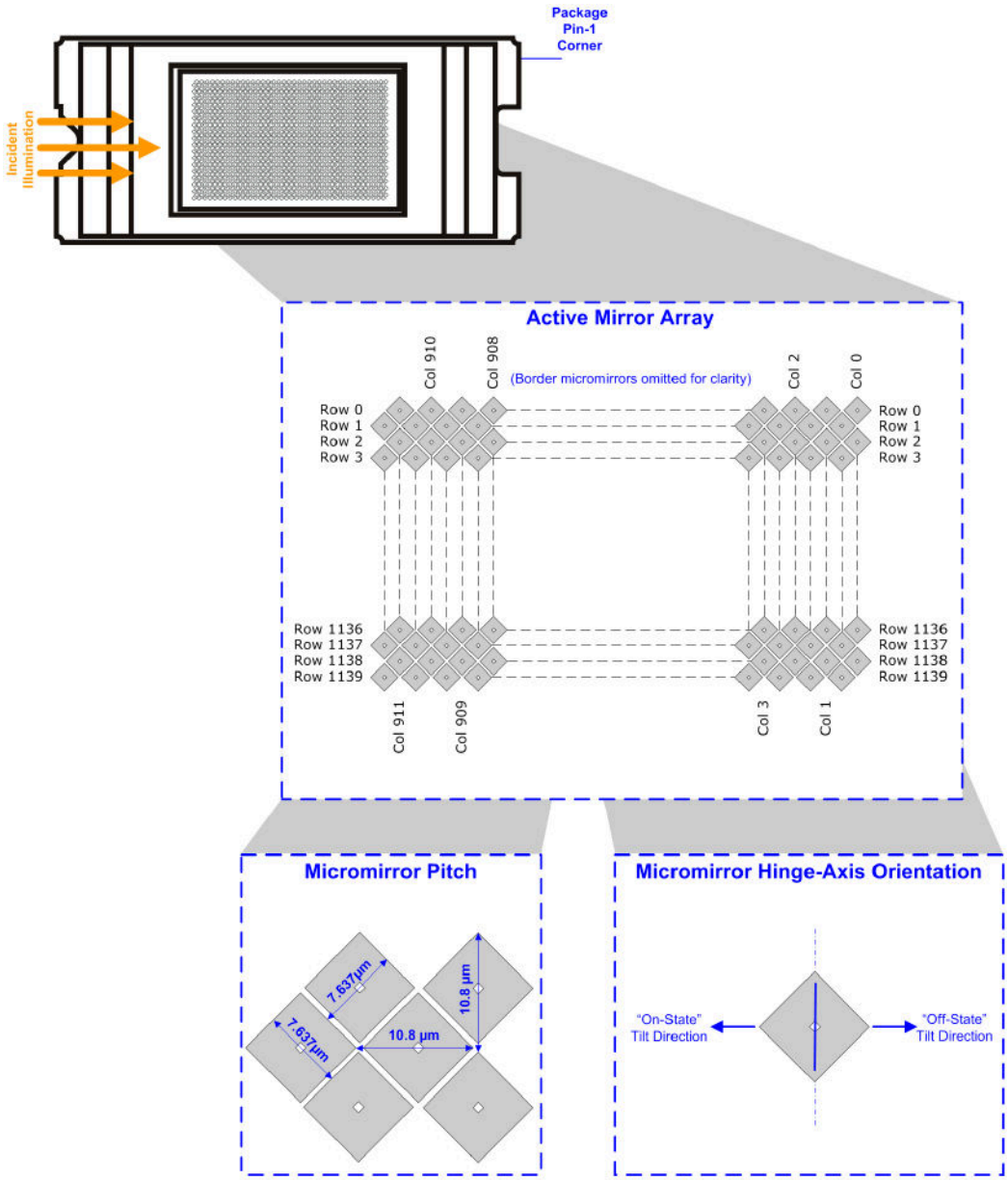


图 8-1. Micromirror Array, Pitch, and Hinge-Axis Orientation

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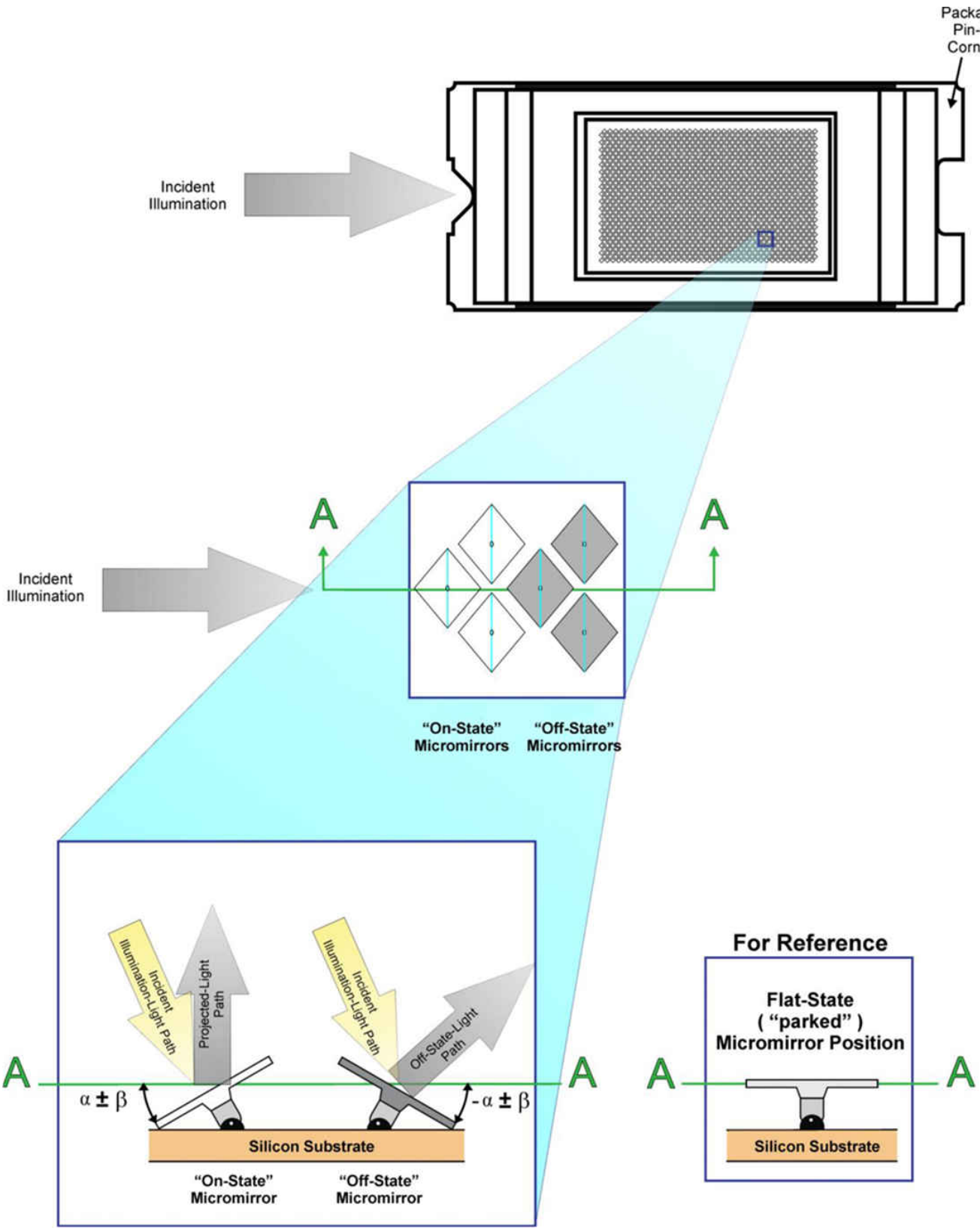

图 8-2. Micromirror Landed Positions and Light Paths

Each individual micromirror is positioned over a corresponding CMOS memory cell. The angular position of a specific micromirror is determined by the binary state (logic 0 or 1) of the corresponding CMOS memory cell contents, after the mirror *clocking pulse* is applied. The angular position (–12° or 12°) of the individual micromirrors changes synchronously with a micromirror clocking pulse, rather than being coincident with the CMOS memory cell data update. Therefore, writing a logic 1 into a memory cell followed by a mirror clocking pulse results in the corresponding micromirror switching to a 12° position. Writing a logic 0 into a memory cell followed by a mirror clocking pulse results in the corresponding micromirror switching to a –12° position.

Updating the angular position of the micromirror array consists of two steps.

1. Update the contents of the CMOS memory.
2. Applying a mirror clocking pulse to the entire micromirror array.

Mirror reset pulses are generated internally by the DLP4500 DMD, with initiation of the pulses being coordinated by the DLPC350 controller. For timing specifications, see 节 *7.7*.

Around the perimeter of the 912 × 1140 array of micromirrors is a uniform band of *border* micromirrors. The border micromirrors are not user-addressable. The border micromirrors land in the –12° position after power has been applied to the device. There are 10 border micromirrors on each side of the 912 × 1140 active array.

8.4 Device Functional Modes

DLP4500 is part of the chipset comprising of the DLP4500 DMD and DLPC350 display controller. To ensure reliable operation, the DLP4500 DMD must always be used with the DLPC350 display controller. DMD functional modes are controlled by the DLPC350 digital display controller. See the DLPC350 data sheet listed in 节 *12.3.1*.

8.4.1 Operating Modes

The DLPC350 is capable of sending patterns to the DLP4500 DMD in two different streaming modes. The first mode is continuous streaming mode, where the DLPC350 uses the parallel RGB interface to stream the 24-bit patterns to the DMD. The second mode is burst mode, where the DLPC350 loads up to 48 binary patterns from flash storage into internal memory, and then streams those patterns to the DMD. 表 8-1 shows the maximum pattern and data rates for both modes of operation.

表 8-1. Pattern and Data Rates

OPERATING MODE	PATTERN RATE (Hz)	DATA RATE (Gbps)	MAXIMUM BINARY PATTERNS
Continuous Streaming(1)	2880	2.99	Unlimited
Burst(2)	4220	4.39	48

(1) Continuous streaming mode uses patterns from RGB interface.
(2) Burst mode uses patterns from internal memory.

8.5 Micromirror Array Temperature Calculation

Achieving optimal DMD performance requires proper management of the maximum DMD case temperature, the maximum temperature of any individual micromirror in the active array, the maximum temperature of the window aperture, and the temperature gradient between any two points on or within the package.

See the *Absolute Maximum Ratings* and 节 *7.4* for applicable temperature limits.

8.5.1 Package Thermal Resistance

The DMD is designed to conduct the absorbed and dissipated heat back to the package where it can be removed by an appropriate thermal management system. The thermal management system must be capable of maintaining the package within the specified operational temperatures at the Thermal test point location, see 图 8-3. The total heat load on the DMD is typically driven by the incident light absorbed by the active area; although other contributions can include light energy absorbed by the window aperture, electrical power dissipation of the array, and/or parasitic heating.

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8.5.2 Case Temperature

The temperature of the DMD case can be measured directly. For consistency, a thermal test point location TP1 representing the case temperature is defined as shown in 图 8-3 and 图 8-4.

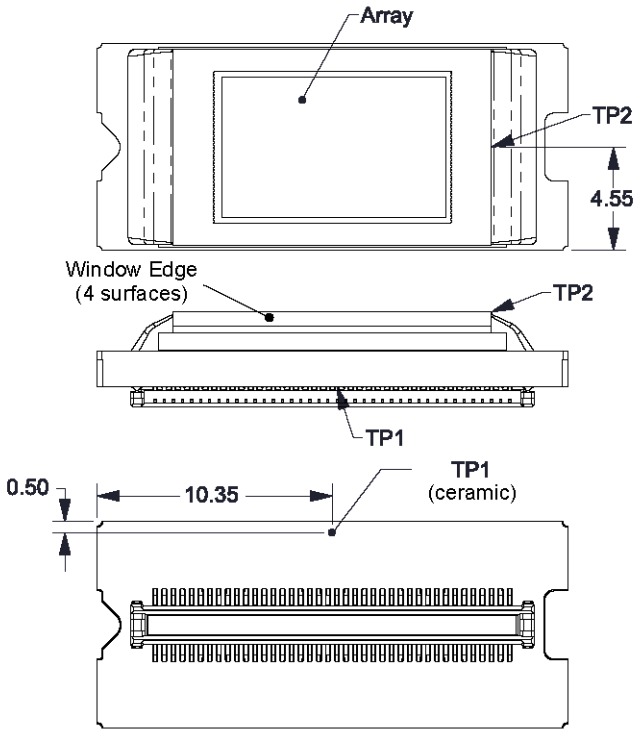

图 8-3. Thermal Test Point Location - FQE Package

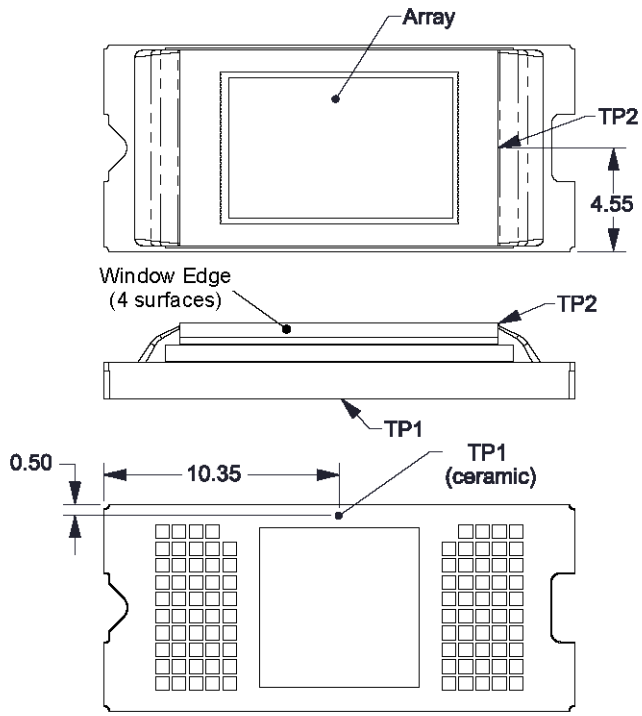

图 8-4. Thermal Test Point Location - FQD Package

8.5.2.1 Temperature Calculation

Micromirror array temperature cannot be measured directly, therefore it must be computed analytically using one or more of these conditions:

- Thermal test point location (see 图 8-3 or 图 8-4)
- Package thermal resistance
- Electrical power dissipation
- Illumination heat load

The relationship between the micromirror array and the case temperature is provided by the following equations:

$$T_{Array} = T_{Ceramic} + (Q_{Array} \times R_{Array\text{-}To\text{-}Ceramic}) \quad (1)$$

$$Q_{Array} = Q_{Elec} + Q_{Illum} \quad (2)$$

$$Q_{Illum} = C_{L2W} \times SL\ P_D \times A \times \text{DMD Absorption Constant} \quad (3)$$

where

- T_{Array} = Computed micromirror array temperature (°C)
- $T_{Ceramic}$ = Ceramic case temperature (°C), located at TP1
- Q_{Array} = Total (electrical + absorbed) DMD array power (W)
- $R_{Array\text{-}to\text{-}Ceramic}$ = Thermal resistance of DMD package from array to TP1 (°C/W)
- Q_{Elec} = Nominal electrical power (W)
- Q_{Illum} = Absorbed illumination heat (W)
- C_{L2W} = Lumens-to-watts constant, estimated at 0.00293 W/lm, based on array characteristics. It assumes a spectral efficiency of 300 lm/W for the projected light, illumination distribution of 83.7% on the active array, and 16.3% on the array border and window aperture P_D = Illumination power density
- SL = Screen lumens A = Illumination area on DMD

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An example calculation is provided in 方程式 4 and 方程式 5. DMD electrical power dissipation varies and depends on the voltage, data rates, and operating frequencies. The nominal electrical power dissipation is used in this calculation with nominal screen lumens of 200 lm and a ceramic case temperature at TP1 of 55°C with a power density of 2 W/cm^2, an illumination area of 0.725 cm^2, and a ceramic case temperature at TP1 of 55°C. The DMD absorption constant of 0.42 assumes nominal operation with an illumination distribution of 83.7% on the active array, 11.9% on the array border, and 4.4% on the window aperture. A system aperture may be required to limit power incident on the package aperture since this area absorbs much more efficiently than the array. Using these values in the previous equations, the following values are computed:

$$Q_{Array} = Q_{Elec} + C_{L2W} \times SL = 0.442\ W + (0.00293\ W/lm \times 200\ lm) = 1.028\ W + Q_{Illum} = 0.442\ W + (2\ W/cm^2 \times 0.725\ cm^2 \times 0.42) = 1.05\ W \quad (4)$$

$$T_{Array} = T_{Ceramic} + (Q_{Array} \times R_{Array\text{-}To\text{-}Ceramic}) = 55°C + (1.028\ W\ 1.05\ W \times 2°C/W) = 57.1°C \quad (5)$$

8.6 Micromirror Landed-on/Landed-Off Duty Cycle

8.6.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the On－state versus the amount of time the same micromirror is landed in the Off－state.

As an example, a landed duty cycle of 75/25 indicates that the referenced micromirror is in the On－state 75% of the time (and in the Off－state 25% of the time); whereas 25/75 would indicate that the micromirror is in the On－state 25% of the time. Likewise, 50/50 indicates that the micromirror is On 50% of the time and Off 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

8.6.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD’s micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD’s usable life.

The symmetry of the landed duty cycle is determined by how close the On-state and Off-state percentages are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

For extended useful lifetime of the DMD, it is strongly recommended not to put any individual pixel in a 100/0 or 0/100 duty cycle for prolonged periods of time. It’s recommended as much as possible to put the DMD in a 50/50 duty cycle across the entire DMD mirror array, where all the mirrors are continuously flipped between the on and off states. A few examples when the DMD could be in a 50/50 duty cycle mode include: when the system is idle, the illumination is disabled, between sequential pattern exposures, or when the exposure pattern sequence is stopped for any reason.

8.6.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect the DMD’s usable life, and this interaction can be exploited to reduce the impact that an asymmetrical landed duty cycle has on the DMD’s usable life. This is quantified in the de-rating curve shown in 图 7-1. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).

- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the maximum operating DMD temperature for a given long-term average landed duty cycle.

8.6.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the landed duty cycle of a given micromirror follows from the image content being displayed by that micromirror.

For example, in the simplest case, when displaying pure-white on a given micromirror for a given time period, that micromirror experiences a 100/0 landed duty cycle during that time period. Likewise, when displaying pure-black, the micromirror experiences a 0/100 landed duty cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the landed duty cycle tracks one-to-one with the linear gray scale value, as shown in 表 8-2.

表 8-2. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	NOMINAL LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given micromirror as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

During a given period of time, the landed duty cycle of a given micromirror can be calculated as follows:

$$\text{Landed Duty Cycle} = (\text{Red_Cycle_\%} \times \text{Red_Scale_Value}) + (\text{Green_Cycle_\%} \times \text{Green_Scale_Value}) + (\text{Blue_Cycle_\%} \times \text{Blue_Scale_Value}) \quad (6)$$

where

- Red_Cycle_%, Green_Cycle_%, and Blue_Cycle_%, represent the percentage of the frame time that Red, Green, and Blue are displayed (respectively) to achieve the desired white point.

For example, assume that the red, green and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the landed duty cycle for various combinations of red, green, blue color intensities would be as shown in 表 8-3.

表 8-3. Example Landed Duty Cycle for Full-Color

RED CYCLE PERCENTAGE 50%	GREEN CYCLE PERCENTAGE 20%	BLUE CYCLE PERCENTAGE 30%	NOMINAL LANDED DUTY CYCLE
RED SCALE VALUE	GREEN SCALE VALUE	BLUE SCALE VALUE	
0%	0%	0%	0/100

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表 8-3. Example Landed Duty Cycle for Full-Color (continued)

RED CYCLE PERCENTAGE 50%	GREEN CYCLE PERCENTAGE 20%	BLUE CYCLE PERCENTAGE 30%	NOMINAL LANDED DUTY CYCLE
RED SCALE VALUE	GREEN SCALE VALUE	BLUE SCALE VALUE	
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

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9 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

For reliable operation, the DLP4500 DMD must be coupled with the DLPC350 controller. The DMD is a spatial light modulator which reflects incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC350. Applications of interest include 3D measurement systems, spectrometers, medical systems, and compressive sensing.

9.2 Typical Application

图 9-1 shows a typical embedded system application using the DLPC350 controller and DLP4500 DMD. In this configuration, the DLPC350 controller supports a 24-bit parallel RGB input, typical of LCD interfaces, from an external source or processor. This system supports both still and motion video sources. However, the controller only supports sources with periodic synchronization pulses. This is ideal for motion video sources, but can also be used for still images by maintaining periodic syncs and only sending a new frame of data when needed. The still image must be fully contained within a single video frame and meet the frame timing constraints. The DLPC350 controller refreshes the displayed image at the source frame rate and repeats the last active frame for intervals in which no new frame has been received.

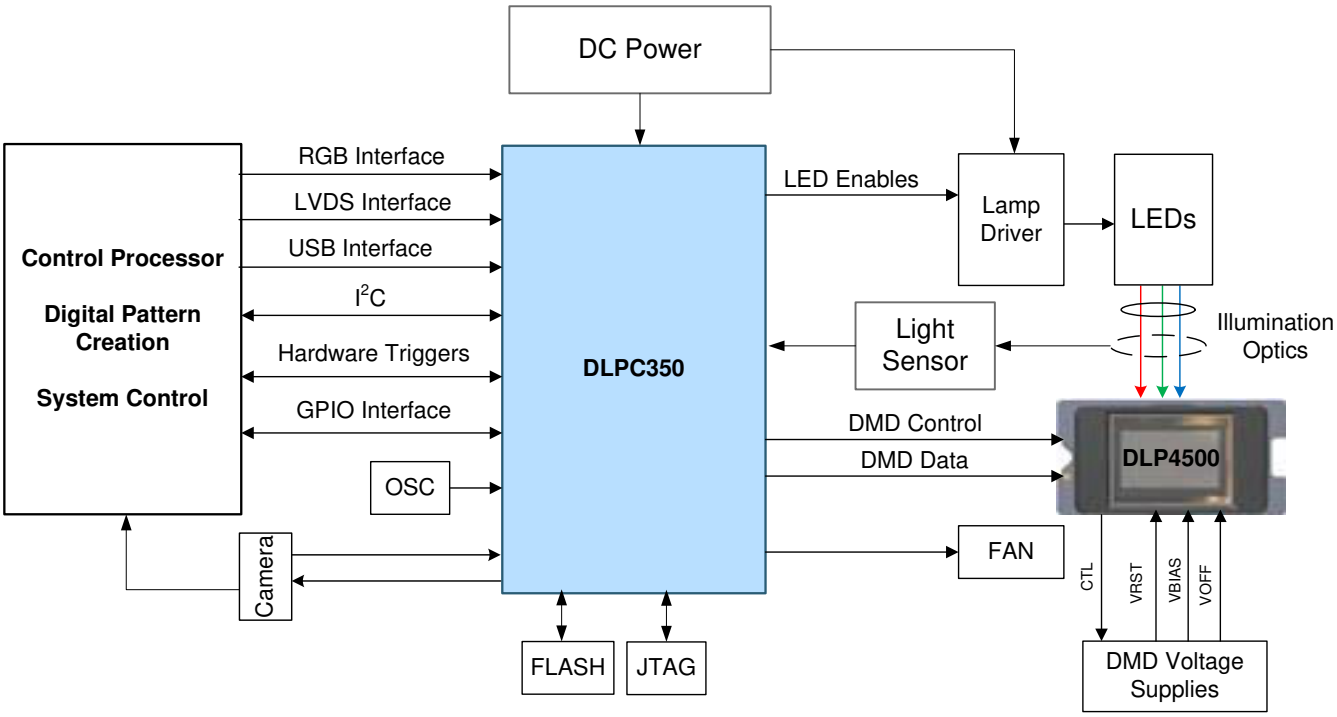

图 9-1. Typical Application Schematic

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9.2.1 Design Requirements

All applications using the DLP4500 chipset require both the controller and DMD components for operation. The system also requires an external parallel flash memory device loaded with the DLPC350 configuration and support firmware. The chipset has several system interfaces and requires some support circuitry. The following interfaces and support circuitry are required:

- DLPC350 system interfaces:
  - Control interface
  - Trigger interface
  - Input data interface
  - Illumination interface
- DLPC350 support circuitry and interfaces:
  - Reference clock
  - PLL
  - Program memory flash interface
- DMD interfaces:
  - DLPC350 to DMD digital data
  - DLPC350 to DMD control interface
  - DLPC350 to DMD micromirror reset control interface

9.2.2 Detailed Design Procedure

9.2.2.1 DLPC350 System Interfaces

The DLP4500 chipset supports a 30-bit parallel RGB interface for image data transfers from another device and a 30-bit interface for video data transfers. The system input requires proper generation of the PWRGOOD and POSENSE inputs to ensure reliable operation. The two primary output interfaces are the illumination driver control interface and sync outputs.

9.2.2.1.1 Control Interface

The DLP4500 chipset accepts control interface commands via the I^{2}C or USB input buses. The control interface allows another master processor to send commands to the DLP4500 chipset to query system status or perform realtime operations such as programming LED driver current settings.

The DLPC350 controller offers two different sets of slave addresses. The I2C_ADDR_SEL pin provides the ability to select an alternate set of 7-bit I^{2}C slave addresses only during power-up. If the I2C_ADDR_SEL pin is set low (logic '0'), then the DLPC350 slave addresses are 0x34 and 0x35. If the I2C-ADDR_SEL pin is set high (logic '1'), then the DLPC350 slave address is 0x3A and 0x3B. The I2C_ADDR_SEL pin also changes the serial number for the USB device so that two DLPC350s can be connected to one computer through USB. Once the system initialization is complete, this pin is available as a GPIO. See the DLPC350 Programmer's Guide (listed in *节 12.3.1*) for detailed information about these operations.

表 9-1 lists a description for active signals used by the DLPC350 to support the I^{2}C interface.

表 9-1. Active Signals – I^{2}C Interface

Signal Name	Description
I2C1_SCL	I^{2}C clock. Bidirectional open-drain signal. I^{2}C slave clock input from the external processor.
I2C1_SDA	I^{2}C data. Bidirectional open-drain signal. I^{2}C slave to accept command or transfer data to and from the external processor.
I2C0_SCL	I^{2}C bus 0, clock; I^{2}C master for on-board peripherals
I2C0_SDA	I^{2}C bus 0, data; I^{2}C master for on-board peripherals

9.2.2.1.2 Input Data Interface

The data interface has two input data ports: a parallel RGB-input port and an FPD-Link LVDS input port. Both input ports can support up to 30 bits and have a nominal I/O voltage of 3.3 V. See the DLPC350 controller data sheet (listed in 节 12.3.1) for details relating to maximum and minimum input timing specifications.

The parallel RGB port can support up to 30 bits in video mode. In pattern mode, only the upper 8 bits of each color are recognized, thereby creating a 24 bit bus from the 30 bit input bus.

The FPD-Link input port can be configured to connect to a video decoder device or an external processor through a 24-, 27-, or 30-bit interface.

表 9-2 provides a description of the signals associated with the data interface.

表 9-2. Active Signals – Data Interface

SIGNAL NAME	DESCRIPTION
RGB Parallel Interface	
P1_(A, B, C)_[0:9]	30-bit data inputs 10 bits for each of the red, green, and blue channels). If interfacing to a system with less than 10-bits per color, connect the bus of the red, green, and blue channels to the upper bits of the DLPC350 10-bit bus.
P1A_CLK	Pixel clock; all input signals on data interface are synchronized with this clock.
P1_VSYNC	Vertical sync
P1_HSYNC	Horizontal sync
P1_DATAEN	Input data valid
FPD-Link LVDS Input	
RCK	Differential input signal for clock
RA_IN	Differential input signal for data channel A
RB_IN	Differential input signal for data channel B
RC_IN	Differential input signal for data channel C
RD_IN	Differential input signal for data channel D
RE_IN	Differential input signal for data channel E

The A, B, and C input data channels of Port 1 can be internally swapped for optimum board layout.

9.2.2.2 DLPC350 System Output Interfaces

9.2.2.2.1 Illumination Interface

An illumination interface is provided that supports an LED driver with up to 3 individual channels.

表 9-3 describes the active signals for the illumination interface.

表 9-3. Active Signals – Illumination Interface

SIGNAL NAME	DESCRIPTION
HEARTBEAT	LED blinks continuously to indicate system is running fine
FAULT_STATUS	LED off indicates system fault
LEDR_EN	Red LED enable
LEDG_EN	Green LED enable
LEDB_EN	Blue LED enable
LEDR_PWM	Red LED PWM signal used to control the LED current
LEDG_PWM	Green LED PWM signal used to control the LED current
LEDB_PWM	Blue LED PWM signal used to control the LED current

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9.2.2.2.2 Trigger Interface (Sync Outputs)

The DLPC350 controller outputs a set of trigger signals for synchronizing displayed patterns with a camera, sensor, or other peripherals. The DLPC350 also has input triggers, where an external processor controls when the patterns are displayed.

表 9-4. Active Signals – Trigger and Sync Interface

SIGNAL NAME	DESCRIPTION
P1_HSYNC	Horizontal sync
P1_VSYNC	Vertical sync
TRIG_IN_1	Advances the pattern display or displays two alternating patterns, depending on the mode
TRIG_IN_2	Pauses the pattern display or advances the pattern by two, depending on the mode
TRIG_OUT_1	Active high during pattern exposure
TRIG_OUT_2	Active high to indicate first pattern display

9.2.2.3 DLPC350 System Support Interfaces

9.2.2.3.1 Reference Clock

The DLPC350 controller requires a 32-MHz 3.3-V external input from an oscillator. This signal serves as the DLP4500 chipset reference clock from which the majority of the interfaces derive their timing. This includes DMD interfaces and serial interfaces.

9.2.2.3.2 PLL

The DLPC350 controller contains two PLLs (PLLM and PLLD), each of which have dedicated 1.2-V digital and 1.8-V analog supplies. These 1.2-V PLL pins must be individually isolated from the main 1.2-V system supply via a ferrite bead. The impedance of the ferrite bead must be much greater than the capacitor at frequencies where noise is expected. The impedance of the ferrite bead must also be less than 0.5 Ω in the frequency range of 100 to 300 kHz and greater than 10 Ω at frequencies greater than 100 MHz.

Isolate the 1.8-V analog PLL power and ground pins as a minimum, using an LC filter with a ferrite bead serving as the inductor and a 0.1-µF capacitor on the DLPC350 side of the ferrite bead. TI recommends that this 1.8-V PLL power be supplied from a dedicated linear regulator and each PLL should be individually isolated from the regulator. The same ferrite recommendations described for the 1.8-V analog PLL supply apply to the 1.2-V digital PLL supply.

When designing the overall supply filter network, care must be taken to ensure that no resonances occur. Take special care when using the 1- to 2-MHz band because this coincides with the PLL natural loop frequency.

9.2.2.3.3 Program Memory Flash Interface

The DLPC350 controller provides two external program memory chip selects:

- $\overline{\text{PM_CS_1}}$ must be used as the chip select for the boot flash device. (Standard *NOR* Flash ⩽ 128 Mb).
- $\overline{\text{PM_CS_2}}$ is available for an optional flash device (⩽128 Mb).

The flash access timing is fixed at 100.5 ns for read timing, and 154.1 ns for write timing. In standby mode, these values change to 803.5 ns for read timing and 1232.1 ns for write timing.

These timing values assume a maximum single direction trace length of 75 mm. When an additional flash is used in conjunction with the boot flash, stub lengths must be kept short and located as close as possible to the flash end of the route.

The DLPC350 controller provides enough program memory address pins to support a flash device up to 128 Mb. PM_ADDR_22 and PM_ADDR_21 are tri-stated GPIO pins during reset, so they require board-level pulldown resistors to prevent the flash address bits from floating during initial bootload.

9.2.2.4 DMD Interfaces

9.2.2.4.1 DLPC350 to DMD Digital Data

The DLPC350 controller provides the pattern data to the DMD over a double data rate (DDR) interface. Data is clocked on both rising and falling edges of the DCLK.

表 9-5 describes the signals used for this interface.

表 9-5. Active Signals – DLPC350 to DMD Digital Data Interface

DLPC350 SIGNAL NAME	DMD SIGNAL NAME
DMD_D(23:0)	DATA(23:0)
DMD_DCLK	DCLK

9.2.2.4.2 DLPC350 to DMD Control Interface

The DLPC350 controller provides the control data to the DMD over a serial bus.

表 9-6 describes the signals used for this interface.

表 9-6. Active Signals – DLPC350 to DMD Control Interface

DLPC350 SIGNAL NAME	DMD SIGNAL NAME	DESCRIPTION
DMD_SAC_BUS	SAC_BUS	DMD stepped-address control (SAC) bus data
DMD_SAC_CLK	SAC_CLK	DMD stepped-address control (SAC) bus clock
$\overline{\text{DMD_LOADB}}$	$\overline{\text{LOADB}}$	DMD data load signal
DMD_SCTRL	SCTRL	DMD data serial control signal
DMD_TRC	TRC	DMD data toggle rate control

9.2.2.4.3 DLPC350 to DMD Micromirror Reset Control Interface

The DLPC350 controls the micromirror clock pulses in a manner to ensure proper and reliable operation of the DMD.

表 9-7 describes the signals used for this interface.

表 9-7. Active Signals – DLPC350 to DMD Micromirror Reset Control Interface

DLPC350 SIGNAL NAME	DMD SIGNAL NAME	DESCRIPTION
DMD_DRC_BUS	DRC_BUS	DMD reset control serial bus
$\overline{\text{DMD_DRC_OE}}$	$\overline{\text{DRC_OE}}$	DMD reset control output enable
DMD_DRC_STRB	DRC_STRB	DMD reset control strobe

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10 Power Supply Recommendations

10.1 Power Supply Sequencing Requirements

The DLP4500 DMD includes five voltage-level supplies (V_{CC}, V_{REF}, V_{OFFSET}, V_{BIAS}, and V_{RESET}), all referenced to VSS ground. For reliable operation of the DLP4500 DMD, the following power supply sequencing requirements must be followed.

Note

Reliable performance of the DMD requires that the following conditions be met:

1. The V_{CC}, V_{REF}, V_{OFFSET}, V_{BIAS}, and V_{RESET} power supply inputs must all be present during operation. All voltages must be referenced to DMD ground (VSS).
2. The V_{CC}, V_{REF}, V_{OFFSET}, V_{BIAS}, and V_{RESET} power supplies must be sequenced on and off in the manner prescribed.

Repeated failure to adhere to the prescribed power-up and power-down procedures may affect device reliability

10.2 DMD Power Supply Power-Up Procedure

1. Power up V_{CC} and V_{REF} in any order.
2. Wait for V_{CC} and V_{REF} to each reach a stable level within their respective recommended operating ranges.
3. Power up V_{BIAS}, V_{OFFSET}, and V_{RESET} in any order, provided that the maximum delta-voltage between V_{BIAS} and V_{OFFSET} is not exceeded (see *Absolute Maximum Ratings* for details).

Note

During the power-up procedure, the DMD LVCMOS inputs should not be driven high until after step 2 is complete.

Note

Power supply slew rates during power up are unrestricted, provided that all other conditions are met.

10.3 DMD Power Supply Power-Down Procedure

1. Command the chipset controller to execute a mirror-parking sequence. See the controller data sheet (listed in *节 12.3.1*) for details.
2. Power down V_{BIAS}, V_{OFFSET}, and V_{RESET} in any order, provided that the maximum delta voltage between V_{BIAS} and V_{OFFSET} is not exceeded (see *Absolute Maximum Ratings* for details).
3. Wait for V_{BIAS}, V_{OFFSET}, and V_{RESET} to each discharge to a stable level within 4 V of the reference ground.
4. Power down V_{CC} and V_{REF} in any order.

Note

During the power-down procedure, the DMD LVCMOS inputs should be held at a level less than V_{REF} + 0.3 V.

Note

Power-supply slew rates during power down are unrestricted, provided that all other conditions are met.

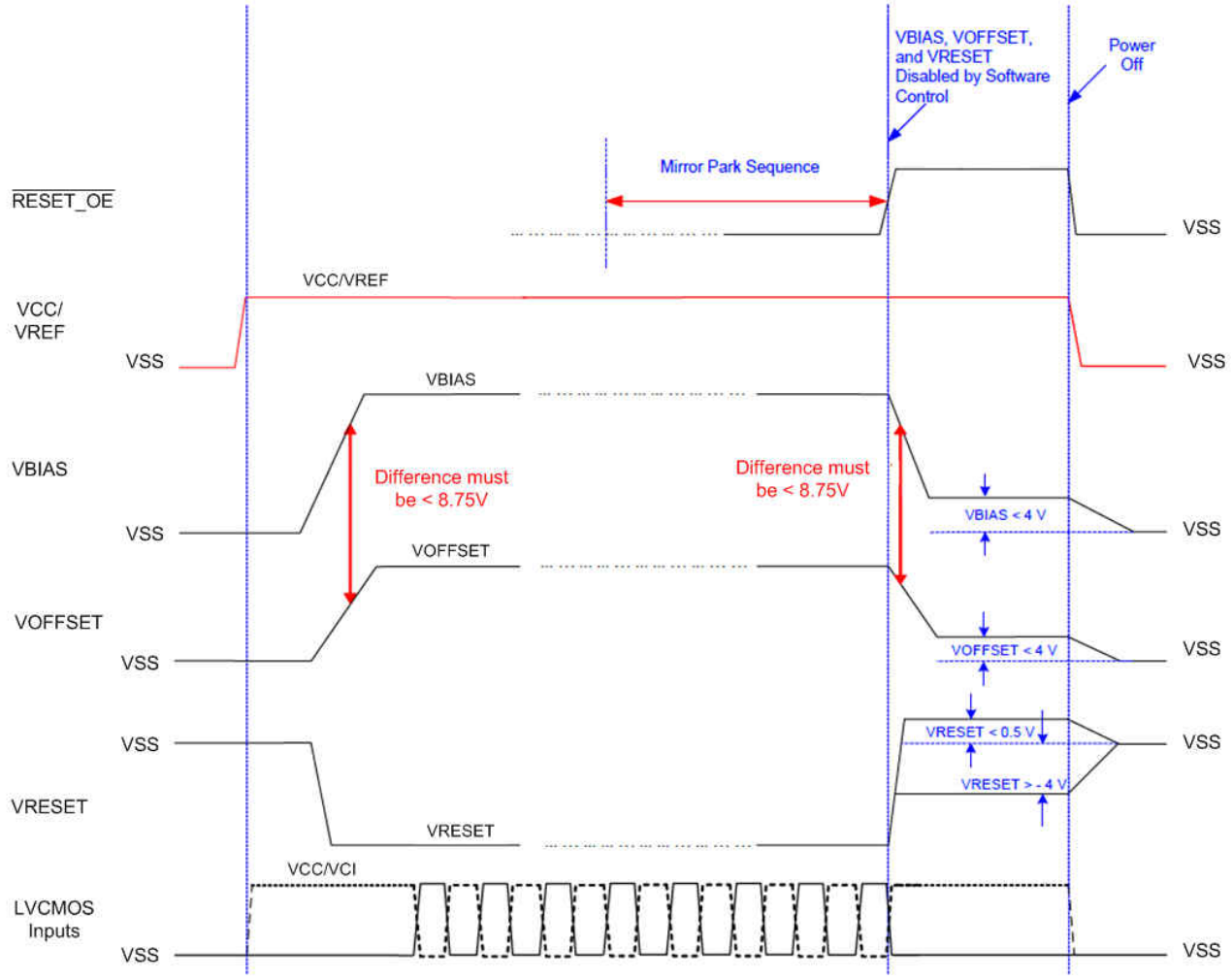

图 10-1. Power-Up and Power-Down Timing

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11 Layout

11.1 Layout Guidelines

11.1.1 DMD Interface Design Considerations

The DMD interface is modeled after the low-power DDR-memory (LPDDR) interface. To minimize power dissipation, the LPDDR interface is defined to be unterminated. As a result, PCB signal-integrity management is imperative. Impedance control and crosstalk mitigation is critical to robust operation. LPDDR board design recommendations include trace spacing that is three times the trace width, impedance control within 10%, and signal routing directly over a neighboring reference plane (ground or 1.9-V plane).

DMD interface performance is also a function of trace length; therefore the length of the trace limits performance. The DLPC350 controller only works over a narrow range of DMD signal routing lengths at 120 MHz. Ensuring positive timing margins requires attention to many factors.

As an example, the DMD interface system timing margin can be calculated as follows.

$$\text{Setup Margin} = (\text{DLPC350 Output Setup}) - (\text{DMD Input Setup}) - (\text{PCB Routing Mismatch}) - (\text{PCB SI Degradation}) \quad (7)$$

$$\text{Hold-Time Margin} = (\text{DLPC350 Output Hold}) - (\text{DMD Input Hold}) - (\text{PCB Routing Mismatch}) - (\text{PCB SI Degradation}) \quad (8)$$

PCB signal integrity degradation can be minimized by reducing the affects of simultaneously switching output (SSO) noise, crosstalk, and inter-symbol interface (ISI). Additionally, PCB routing mismatch can be budgeted via controlled PCB routing.

In an attempt to minimize the need for signal integrity analysis that would otherwise be required, the following PCB design guidelines are provided. They describe an interconnect system that satisfies both waveform quality and timing requirements (accounting for both PCB routing mismatch and PCB SI degradation). Variation from these recommendations may also work, but should be confirmed with PCB signal integrity analysis or lab measurements.

11.1.2 DMD Termination Requirements

表 11-1 lists the termination requirements for the DMD interface. These series resistors should be placed as close to the DLPC350 pins as possible while following all PCB guidelines.

表 11-1. Termination Requirements for DMD Interface

SIGNALS	SYSTEM TERMINATION
DMD_D(23:0), DMD_TRC, DMD_SCTRL, $\overline{\text{DMD_LOADB}}$, DMD_DRC_STRB, DMD_DRC_BUS, DMD_SAC_CLK, and DMD_SAC_BUS	External 5-Ω series termination at the transmitter
DMD_DCLK	External 5-Ω series termination at the transmitter
$\overline{\text{DMD_DRC_OE}}$	External 0-Ω series termination. This signal must be externally pulled-up to VDD_DMD via a 30-kΩ to 51-kΩ resistor

DMD_CLK and DMD_SAC_CLK clocks should be equal lengths, as shown in 图 11-1.

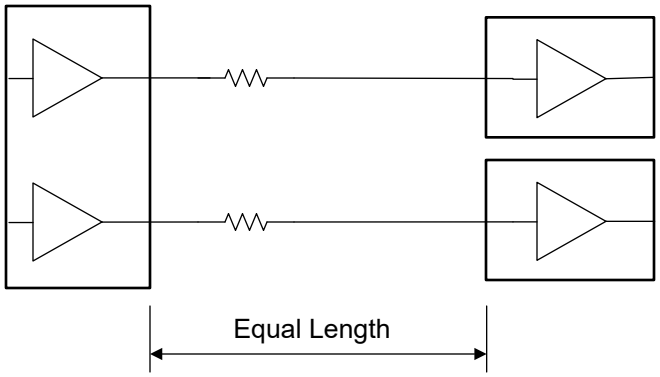

图 11-1. Series-Terminated Clocks

11.1.3 Decoupling Capacitors

The decoupling capacitors should be given placement priority. The supply voltage pin of the capacitor should be located close to the DLPC350 supply voltage pin or pins. Decoupling capacitors should have two vias connecting the capacitor to ground and two vias connecting the capacitor to the power plane, but if the trace length is less than 0.05 inches, the device can be connected directly to the decoupling capacitor. The vias should be located on opposite sides of the long side of the capacitor, and those connections should be less than 0.05 inches as well.

11.1.4 Power Plane Recommendations

For best performance, TI recommends the following:

- Two power planes
  - One solid plane for ground (GND)
  - One split plane for other voltages with no signal routing on the power planes
- Power and ground pins should be connected to these planes through a via for each pin.
- All device pin and via connections to these planes should use a thermal relief with a minimum of four spokes.
- Trace lengths for the component power and ground pins should be minimized to 0.03 inches or less.
- Vias should be spaced out to avoid forming slots on the power planes.
- High speed signals should not cross over a slot in the adjacent power planes.
- Vias connecting all the digital layers should be placed around the edge of the rigid PCB regions 0.03 inches from the board edges with 0.1 inch spacing prior to routing.
- Placing extra vias is not required if there are sufficient ground vias due to normal ground connections of devices.
- All signal routing and signal vias should be inside the perimeter ring of ground vias.

11.1.5 Signal Layer Recommendations

The PCB signal layers should follow typical good practice guidelines including:

- Layer changes should be minimized for single-ended signals.
- Individual differential pairs can be routed on different layers, but the signals of a given pair should not change layers.
- Stubs should be avoided.
- Only voltage or low-frequency signals should be routed on the outer layers, except as noted previously in this document.
- Double data rate signals should be routed first for best impedance and trace length matching.

The PCB should have a solder mask on the top and bottom layers. The mask should not cover the vias.

- Except for fine pitch devices (pitch ⩽ 0.032 inches), the copper pads and the solder mask cutout should be of the same size.
- Solder mask between pads of fine pitch devices should be removed.

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- In the BGA package, the copper pads and the solder mask cutout should be of the same size.

11.1.6 General Handling Guidelines for CMOS-Type Pins

To avoid potentially damaging current caused by floating CMOS input-only pins, TI recommends that unused input pins be tied through a pullup resistor to its associated power supply, or a pulldown to ground. For inputs with internal pullup or pulldown resistors, adding an external pullup or pulldown resistor is unnecessary unless specified in the Pin Configuration and Functions section. Note that internal pullup and pulldown resistors are weak and should not be expected to drive an external line.

After power-up or device reset, bidirectional pins are configured as inputs as a reset default until directed otherwise.

Unused output-only pins can be left open.

11.1.7 PCB Manufacturing

The DLPC350 Controller and DMD are a high-performance (high-frequency and high-bandwidth) set of components. This section provides PCB guidelines to help ensure proper operation of these components.

The DLPC350 controller board will be a multi-layer PCB with surface mount components on both sides. The majority of large surface mount components are placed on the top side of the PCB. Circuitry is high speed digital logic. The high speed interfaces include:

- 120-MHz DDR interface from DLPC350 to DMD
- 150-MHz LVTTL interface from a video decoder to the DLPC350
- 150-MHz pixel clock supporting 30-bit parallel RGB interface
- LVTTL parallel memory interface between the DLPC350 controller and flash with 70-ns access time
- LVDS flat panel display port to DLPC350

The PCB should be designed to IPC2221 and IPC2222, Class 2, Type Z, at level B producibility and built to IPC6011 and IPC6012, Class 2.

11.1.7.1 General Guidelines

表 11-2. PCB General Recommendations

DESCRIPTION	RECOMMENDATION
Configuration	Asymmetric dual stripline
Etch thickness (T)	1.0-oz. (1.2-mil thick) copper
Single-ended signal impedance	50 Ω (±10%)
Differential signal impedance	100 Ω differential (±10%)

11.1.7.2 Trace Widths and Minimum Spacings

For best performance, TI recommends the trace widths and minimum spacings shown in 表 11-3.

表 11-3. Trace Widths and Minimum Spacings

SIGNAL NAME	TRACE WIDTH (inches)	MINIMUM TRACE SPACING (inches)
P1P2, P1P2V_PLLM, P1P2V_PLLD, P2P5V, P3P3V, P1P9V, A1P8V, A1P8V_PLLD, A1P8V_PLLM	0.02	0.010
VRST, VBIAS, VOFFSET	0.02	0.010
VSS (GND)	0.02	0.005
FANx_OUT	0.02	0.020
DMD_DCLK		0.030
P1A_CLK, P1B_CLK, P1C_CLK		0.030
MOSC, MOSCN		0.030

11.1.7.3 Routing Constraints

In order to meet the specifications listed in the following tables, typically the PCB designer must route these signals manually (not using automated PCB routing software). In case of length matching requirements, routing traces in a serpentine fashion may be required. Keep the number of turns to a minimum and the turn angles no sharper than 45°. Traces must be 0.1 inches from board edges when possible; otherwise they must be 0.05 inches minimum from the board edges. Avoid routing long traces all around the PCB. PCB layout assumes adjacent trace spacing is twice the trace width. However, three times the trace width will reduce crosstalk and significantly help performance.

The maximum and minimum signal routing trace lengths include escape routing.

表 11-4. Signal Length Routing Constraints for DMD Interface

SIGNALS	MINIMUM SIGNAL ROUTING LENGTH(1)	MAXIMUM SIGNAL ROUTING LENGTH(2)
DMD_D(23:0), DMD_DCLK, DMD_TRC, DMD_SCTRL, DMD_LOADB,	2480 mil (63 mm)	2953 mil (75 mm)
DMD_OE, DMD_DRC_STRB, DMD_DRC_BUS, DMD_SAC_CLK, and DMD_SAC_BUS	512 mil (13 mm)	5906 mil (150 mm)

(1) Signal lengths below the stated minimum will likely result in overshoot or undershoot.
(2) DMD-DDR maximum signal length is a function of the DMD_DCLK rate.

Each high-speed, single-ended signal should be routed in relation to its reference signal, such that a constant impedance is maintained throughout the routed trace. Avoid sharp turns and layer switching while keeping total trace lengths to a minimum. The following signals should follow the signal matching requirements described in 表 11-5.

表 11-5. High-Speed Signal Matching Requirements for DMD Interface

SIGNALS	REFERENCE SIGNAL	MAX MISMATCH	UNIT
DMD_D(23:0), DMD_TRC, DMD_SCTRL, DMD_LOADB	DMD_DCLK	±200 (±5.08)	mil (mm)
DMD_DRC_STRB, DMD_DRC_BUS, DMD_SAC_BUS, DMD_OE	DMD_SAC_CLK	±200 (±5.08)	mil (mm)

The values in 表 11-5 apply to the PCB routing only. They do not include any internal package routing mismatch associated with the DLPC350 or DMD. Additional margin can be attained if internal DLPC350 package skew is taken into account. Additionally, to minimize EMI radiation, serpentine routes added to facilitate trace length matching should only be implemented on signal layers *between* reference planes.

Both the DLPC350 output timing parameters and the DMD input timing parameters include a timing budget to account for their respective internal package routing skew. Thus, additional system margin can be attained by comprehending the package variations and compensating for them in the PCB layout. To increase the system timing margin, TI recommends that the DLPC350 package variation be compensated for (by signal group), but it may not be desirable to compensate for DMD package skew. This is due to the fact that each DMD has a different skew profile, making the PCB layout DMD specific. To use a common PCB design for different DMDs, TI recommends that either the DMD package skew variation not be compensated for on the PCB, or the package lengths for all applicable DMDs being considered. 表 11-6 provides the DLPC350 package output delay at the package ball for each DMD interface signal.

The total length of all the traces in 表 11-6 should be matched to the DMD_DCLK trace length. Total trace length includes package skews, PCB length, and DMD flex cable length.

表 11-6. DLPC350 Package Skew and Routing Trace Length for the DMD Interface

SIGNAL	TOTAL DELAY (Package Skews)		PACKAGE PIN
	(ps)	(mil)	
DMD_D0	25.9	152.35	A8

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表 11-6. DLPC350 Package Skew and Routing Trace Length for the DMD Interface (continued)

SIGNAL	TOTAL DELAY (Package Skews)		PACKAGE PIN
	(ps)	(mil)	
DMD_D1	19.6	115.29	B8
DMD_D2	13.4	78.82	C8
DMD_D3	7.4	43.53	D8
DMD_D4	18.1	106.47	B11
DMD_D5	11.1	65.29	C11
DMD_D6	4.4	25.88	D11
DMD_D7	0.0	0.00	E11
DMD_D8	14.8	87.06	C7
DMD_D9	18.4	108.24	B10
DMD_D10	6.4	37.65	E7
DMD_D11	4.8	28.24	D10
DMD_D12	29.8	175.29	A6
DMD_D13	25.7	151.18	A12
DMD_D14	19.0	111.76	B12
DMD_D15	11.7	68.82	C12
DMD_D16	4.7	27.65	D12
DMD_D17	21.5	126.47	B7
DMD_D18	24.8	145.88	A10
DMD_D19	8.3	48.82	D7
DMD_D20	23.9	140.59	B6
DMD_D21	1.6	9.41	E9
DMD_D22	10.7	62.94	C10
DMD_D23	16.7	98.24	C6
DMD_DCLK	24.8	145.88	A9
$\overline{\text{DMD_LOADB}}$	18.0	105.88	B9
DMD_SCTRL	11.4	67.06	C9
DMD_TRC	4.6	27.06	D9

表 11-7. Routing Priority

SIGNAL	ROUTING PRIORITY	ROUTING LAYER	MATCHING REFERENCE SIGNAL	TOLERANCE
DMD_DCLK(1) (2) (3)	1	3	–	–
DMD_D[23:0], DMD_SCTRL, DMD_TRC, DMD_LOADB(1) (2) (3) (4)	1	3, 4	DMD_DCLK	±150 mils
P1_A[9:0], P1_B[9:0], P1_C[9:0], P1_HSYNC, P1_VSYNC, P1_DATAEN, P1X_CLK	1	3, 4	P1X_CLK	±0.1 inches
R[A-E]_IN_P, R[A-E]_IN_N, RCK_IN_P, RCK_IN_N	2	3, 4	RCK	±150 mils Differential signals need to be matched within ±12 mils

(1) Total signal length from the DLPC350 and the DMD, including flex cable traces and PCB signal trace lengths must be held to the lengths specified in 表 11-4.
(2) Switching routing layers is not permitted except at the beginning and end of a trace.
(3) Minimize vias on DMD traces.
(4) Matching includes PCB trace length plus the DLPC350 package length plus the DMD flex cable length.

11.1.7.4 Fiducials

Fiducials for automatic component insertion should be 0.05 inch diameter copper with a 0.1-inch cutout (antipad). Fiducials for optical auto insertion are placed on three corners of both sides of the PCB.

11.1.7.5 Flex Considerations

表 11-8 shows the general DMD flex design recommendations. 表 11-9 lists the minimum flex design requirements.

表 11-8. Flex General Recommendations

DESCRIPTION	RECOMMENDATION
Configuration	Two-layer micro strip
Reference plane 1	Ground plan for proper return
Vias	Maximum two per signal
Single trace width	4-mil minimum
Etch thickness (T)	0.5-oz. (0.6 mil thick) copper
Single-ended signal impedance	50 Ω (± 10%)

表 11-9. Minimum Flex Design Requirements

PARAMETER	APPLICATION	SINGLE-ENDED SIGNALS	UNIT
Line width (W)(1)	Escape routing in ball field	4 (0.1)	mil (mm)
	PCB etch data and control	5 (0.13)	mil (mm)
	PCB etch clocks	7 (0.18)	mil (mm)
Minimum line spacing to other signals (S)	Escape routing in ball field	4 (0.1)	mil (mm)
	PCB etch data and control	2x the line width(2)	mil (mm)
	PCB etch clocks	3x the line width	mil (mm)

(1) Line width is expected to be adjusted to achieve impedance requirements.
(2) Three times the line spacing is recommended for all signals to help achieve the desired signal integrity.

11.1.7.6 DLPC350 Thermal Considerations

The underlying thermal limitation for the DLPC350 controller is that the maximum operating junction temperature (T_J) must not be exceeded (see *Recommended Operating Conditions* in *Specifications*). This temperature is dependent on operating ambient temperature, airflow, PCB design (including the component layout density and the amount of copper used), power dissipation of the DLPC350 controller, and power dissipation of surrounding components. The DLPC350 package is designed to extract heat through the power and ground planes of the PCB, thus copper content and airflow over the PCB are important factors.

11.2 Layout Example

11.2.1 Printed Circuit Board Layer Stackup Geometry

The DLPC350 PCB is targeted at six layers with layer stack up shown in 图 11-2. The PCB layer stack may vary depending on system design. However, careful attention is required to meet design considerations. Layers one and six should consist of the components layers. Low-speed routing and power splits are allowed on these layers. Layer two should consist of a solid ground plane. Layer five should be a split voltage plane. Layers three and four should be used as the primary routing layers. Routing on external layers should be less than 0.25 inches for priority one and two signals. Refer to 表 11-7 for signal priority groups.

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Board material should be FR-370HR or similar. PCB should be designed for lead-free assembly with the stackup geometry shown in 图 11-2.

Controlled Impedance Stack-up form

Material: FR370HR

Layer	Thickness	Stack-up	Descript	Cu Oz	SE Trace	SE Calculated	SE Target	Ref Pln	Diff Pairs Trace	Diff Pairs Space	Diff Pairs (Pitch)	Diff Pairs Calculated	Diff Pairs Target	Ref Pln
	0.7	soldermask												
	1.2	plating												
1	0.6		sig	0.5	10.5	50.25	50	2	4.5	4.5	9	102.01	100	2
					4	74.93	75	2	5.25	4.75	10	99.14	100	2
	6	6.0 prepreg												
2	2.6		pln	2										
	5	5.0 core												
3	1.2		sig	1	7	50.36	50	2,5	4.25	5.75	10	99.11	100	2,5
	5	5.0	blank											
	18	18.0	blank	Filler to meet overall thickness										
	5	5.0 prepreg												
4	1.2		sig	1	7	50.36	50	2,5	4.25	5.75	10	99.11	100	2,5
	5	5.0 core												
5	2.6		pln	2										
	6	6.0 prepreg												
6	0.6		sig	0.5	10.5	50.25	50	5	4.5	4.5	9	102.01	100	5
	1.2	plating			4	74.93	75	5	5.25	4.75	10	99.14	100	5
	0.7	soldermask												

8.8 =copper
28 =core
22 =prepreg
3.8 =plating, s/m

Target thickness:

62.6 =total thickness | .062 +-10% | Calculated using Apsim RLGC (Impedance calculator) +-10% | 5/5/08

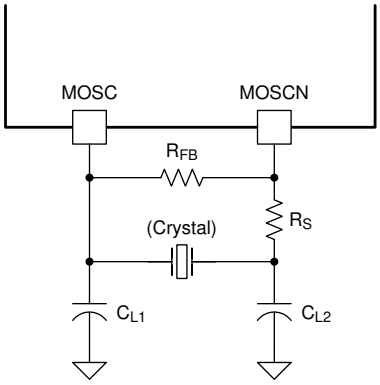
图 11-2. Layer Stackup

表 11-10. PCB Layer Stackup Geometry

PARAMETER	DESCRIPTION	RECOMMENDATION
Reference plane 1	Ground plane for proper return	
Reference plane 2	1.9-V DMD I/O power plane or ground	
Er	Dielectric FR4	4.3 at 1 GHz (nominal)
H1	Signal trace distance to reference plane 1	5 mil (0.127 mm)
H2	Signal trace distance to reference plane 2	30.4 mil

11.2.2 Recommended DLPC350 MOSC Crystal Oscillator Configuration

The DLPC350 controller requires an external reference clock to feed its internal PLL. This reference may be supplied via a crystal or oscillator. The DLPC350 controller accepts a reference clock of 32 MHz with a maximum frequency variation of 100 ppm (including aging, temperature, and trim component variation). When a crystal is used, several discrete components are also required, as shown in 图 11-3.



C_L = crystal load capacitance in F

$C_{L1} = 2 \times (C_L - C_{stray\text{-}MOSC})$

$C_{L2} = 2 \times (C_L - C_{stray\text{-}MOSCN}$

$C_{stray\text{-}MOSC}$ = sum of package and PCB capacitance at the crystal pin associated withe ASIC signal MOSC

$C_{stray\text{-}MOSCN}$ = sum of package and PCB capacitance at the crystal pin associated withe ASIC signal MOSCN

图 11-3. Recommended Crystal Oscillator Configuration

表 11-11. Crystal Port Electrical Characteristics

PARAMETER	NOM	UNIT
MOSC to GND capacitance	3.9	pF
MOSCN to GND capacitance	3.8	pF

表 11-12. Recommended Crystal Configuration

PARAMETER	RECOMMENDED	UNIT
Crystal circuit configuration	Parallel resonant	
Crystal type	Fundamental (first harmonic)	
Crystal nominal frequency	32	MHz
Crystal frequency tolerance (including accuracy, temperature, aging and trim sensitivity)	±100	PPM
Crystal equivalent series resistance (ESR)	50 maximum	Ω
Crystal load	10	pF
Crystal shunt load	7 maximum	pF
Crystal frequency temperature stability	±30	PPM
R_S drive resistor (nominal)	100	Ω
R_{FB} feedback resistor (nominal)	1	MΩ
C_{L1} external crystal load capacitor (MOSC)	Typical drive level with TCX9C3207001 crystal (ESRmax = 30 Ω) = 160 µW. See 图 11-3	pF
C_{L2} external crystal load capacitor (MOSCN)	Typical drive level with TCX9C3207001 crystal (ESRmax = 30 Ω) = 160 µW. See 图 11-3	pF
PCB layout	A ground isolation ring around the crystal	

If an external oscillator is used, then the oscillator output must drive the MOSC pin on the DLPC350 controller, and the MOSCN pin should be left unconnected. Note that the DLPC350 controller can only accept a triangular waveform.

Similar to the crystal option, the oscillator input frequency is limited to 32 MHz.

It is assumed that the external crystal or oscillator stabilizes within 50 ms after stable power is applied.

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11.2.3 Recommended DLPC350 PLL Layout Configuration

High-frequency decoupling is required for both 1.2-V and 1.8-V PLL supplies and should be provided as close as possible to each of the PLL supply package pins as shown in the example layout in 图 11-4. TI recommends that decoupling capacitors be placed under the package on the opposite side of the board. High quality, low-ESR, monolithic, surface mount capacitors should be used. Typically 0.1 µF for each PLL supply should be sufficient. The length of a connecting trace increases the parasitic inductance of the mounting and thus, where possible, there should be no trace, allowing the via to butt up against the land itself. Additionally, the connecting trace should be made as wide as possible. Further improvement can be made by placing vias to the side of the capacitor lands or doubling the number of vias.

The location of bulk decoupling depends on the system design. Typically, a good ceramic capacitor in the 10-µF range is adequate.

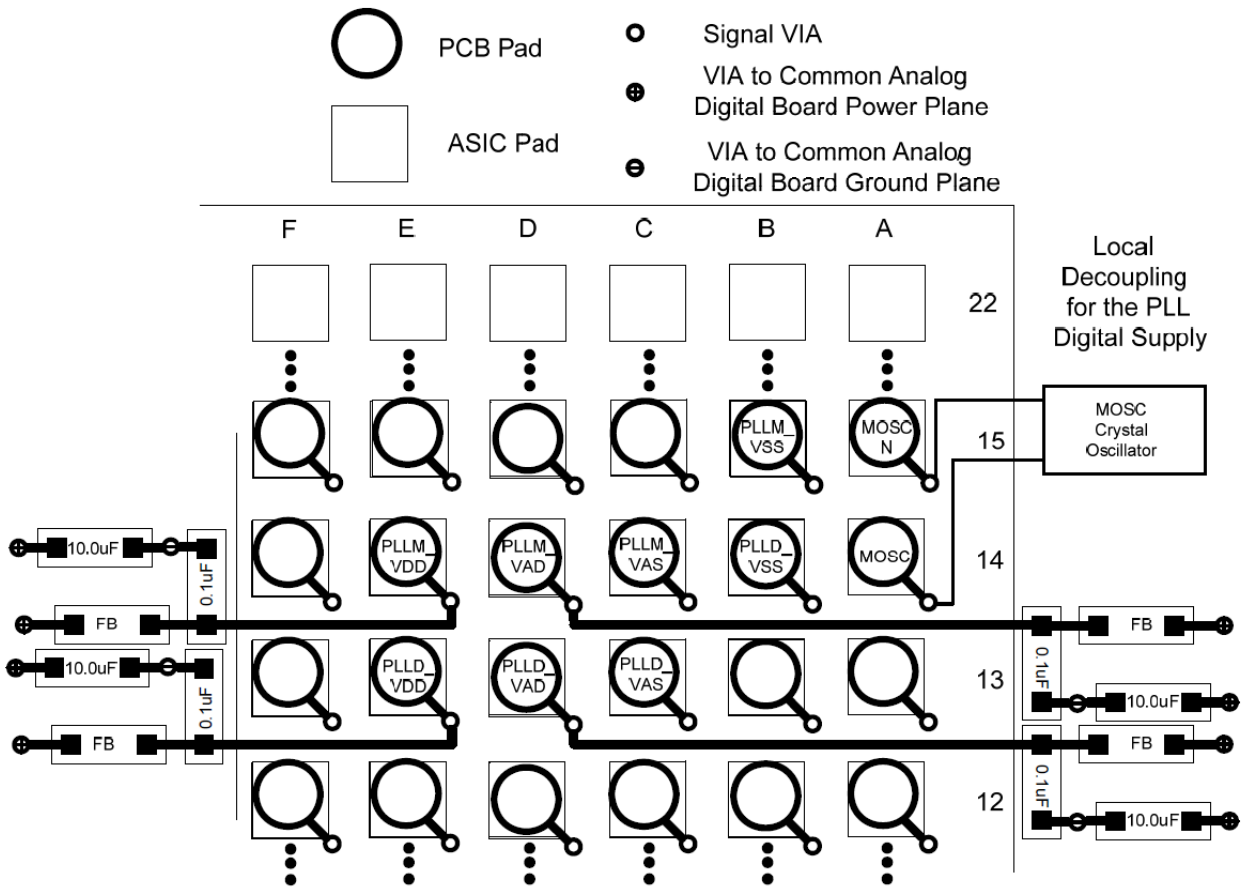

图 11-4. PLL Filter Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

节 12.1.1 provides a legend for reading the complete device name for any DLP device.

表 12-1. Package-Specific Information

PACKAGE TYPE	PACKAGE DRAWING	BODY SIZE	CONNECTOR
LCCC	FQE	9.1 mm x 20.7 mm	Panasonic AXT580124
LCCC	FQD	9.1 mm x 20.7 mm	Neoconix FBX0040CMFF6AU00

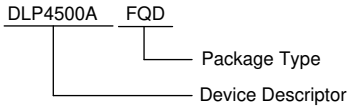

图 12-1. Device Nomenclature

12.2 Device Markings

The device marking consists of the fields shown in 图 12-2 图 12-3.

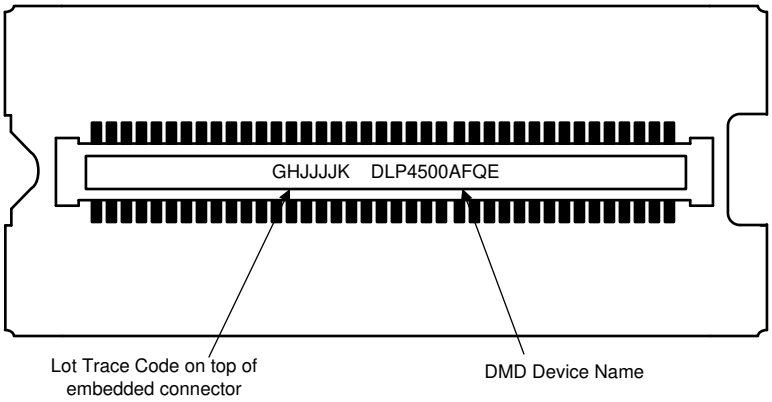

图 12-2. Device Marking for FQE

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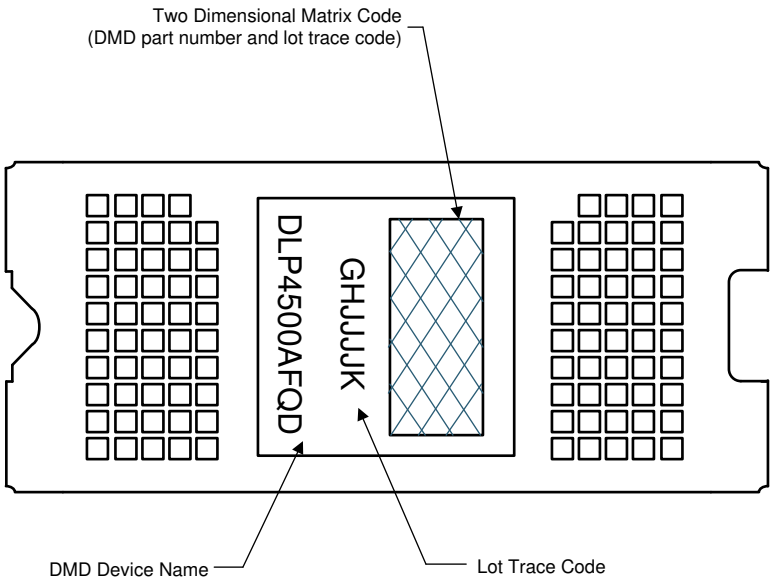

图 12-3. Device Markings for FQD

12.3 Documentation Support

12.3.1 Related Documentation

The following documents contain additional information related to the use of the DLP4500 device:

- DLPC350 Digital Controller Data Sheet, DLPS029 DLPS029
- DLPC350 Software Programmer's Guide, DLPU010
- DLP® LightCrafter™ 4500 Evaluation Module User's Guide, DLPU011
- Geometric Optics Application Note, DLPA044

12.4 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.5 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP4500AFQD	ACTIVE	CLGA	FQD	98	80	RoHS & Green	Call TI	N / A for Pkg Type	0 to 70		Samples
DLP4500AFQE	ACTIVE	CLGA	FQE	80	80	RoHS & non-Green	Call TI	N / A for Pkg Type	0 to 70		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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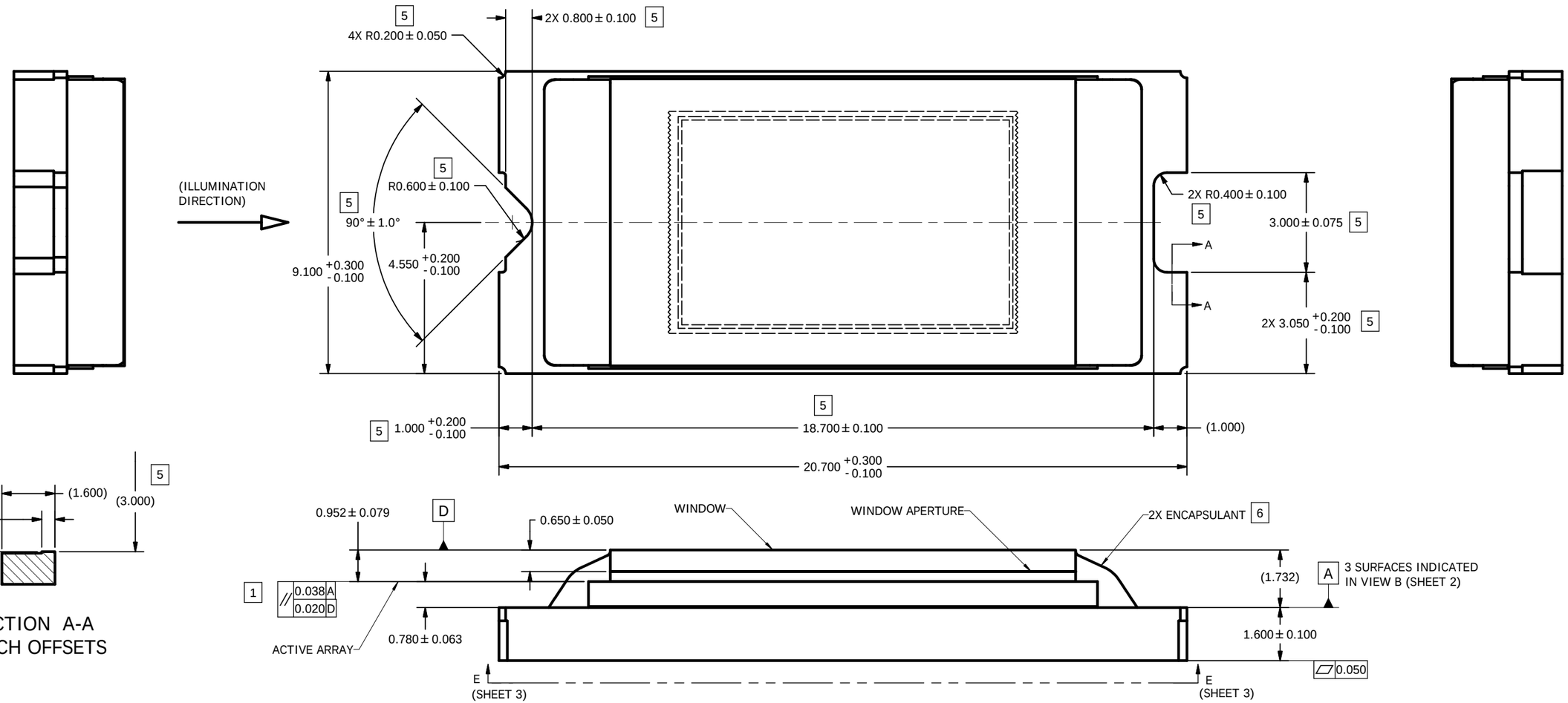
REVISIONS

REV	DESCRIPTION	DATE	BY
A	ECO 2104138 INITIAL RELEASE	01/20/2010	J. HOLM
B	ECO 2121955 CORRECT APERTURE X DIMENSIONS VIEW D	1/23/2012	BMH
C	ECO 2144971 ADD (FQD PACKAGE) TO TITLE	9/11/2014	MAA

NOTES UNLESS OTHERWISE SPECIFIED:

1. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
2. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.6 DEGREES.
3. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE ARRAY.
4. DMD MARKING TO APPEAR ON SYMBOLIZATION PAD.
5. NOTCH DIMENSIONS ARE DEFINED BY UPPERMOST LAYERS OF CERAMIC, AS SHOWN IN SECTION A-A.
6. ENCAPSULANT TO BE CONTAINED WITHIN DIMENSIONS SHOWN IN VIEWS C AND D (SHEET 2).
7. WHILE ONLY THE THREE DATUM A TARGET AREAS A1, A2, AND A3 ARE USED FOR MEASUREMENT, ALL 4 CORNERS SHOULD BE CONTACTED, INCLUDING E1, WHEN MOUNTING IN SYSTEM.



NONE	0314DA
NEXT ASSY	USED ON
APPLICATION	

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES:
  - ANGLES ± 1°
  - 2 PLACE DECIMALS ± 0.25
  - 1 PLACE DECIMALS ± 0.50
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994
- REMOVE ALL BURRS AND SHARP EDGES
- PARENTHETICAL INFORMATION FOR REFERENCE ONLY

		DATE
DRAWN	J. HOLM	12/11/2009
ENGINEER	J. HOLM	12/11/2009
QA/CE	P. KONRAD	1/20/2010
CM	F. ARMSTRONG	1/20/2010
APPROVED	J. HALL	1/20/2010

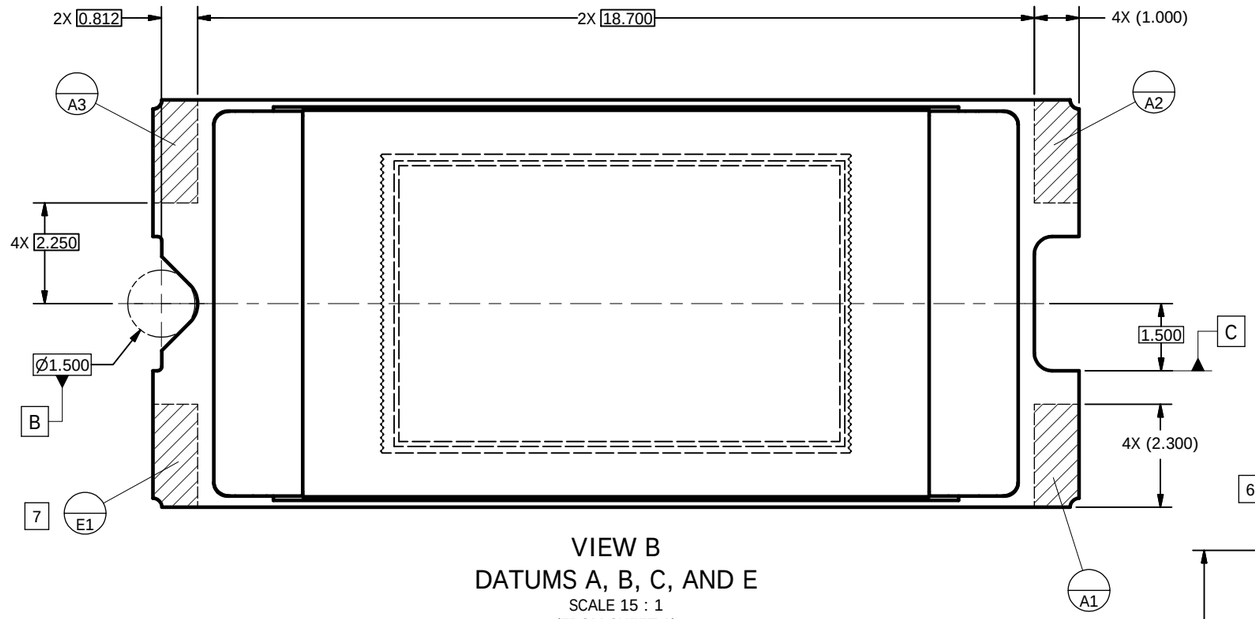
TEXAS INSTRUMENTS
Dallas Texas

TITLE
ICD, MECHANICAL, DMD,
.45 WXGA-800 DDR SERIES 310
(FQD PACKAGE)

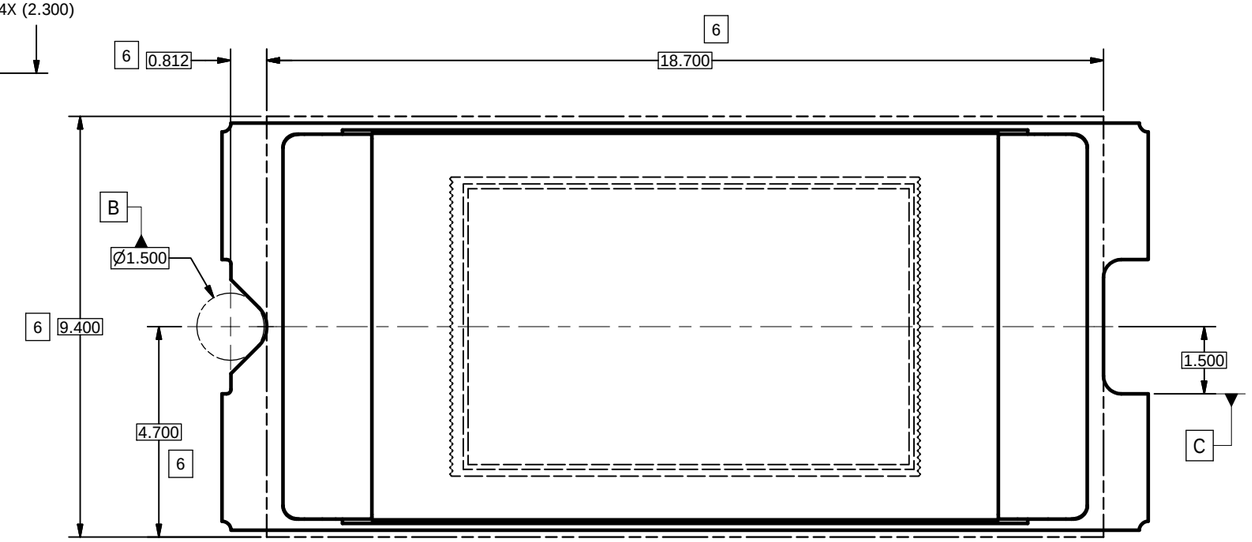
SIZE D | DWG NO 2510852 | REV C

SCALE 15:1 | SHEET 1 OF 3

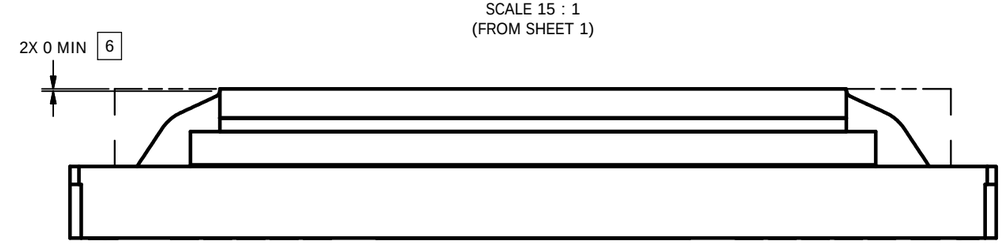
INV11-2006a



VIEW B
DATUMS A, B, C, AND E
SCALE 15 : 1
(FROM SHEET 1)



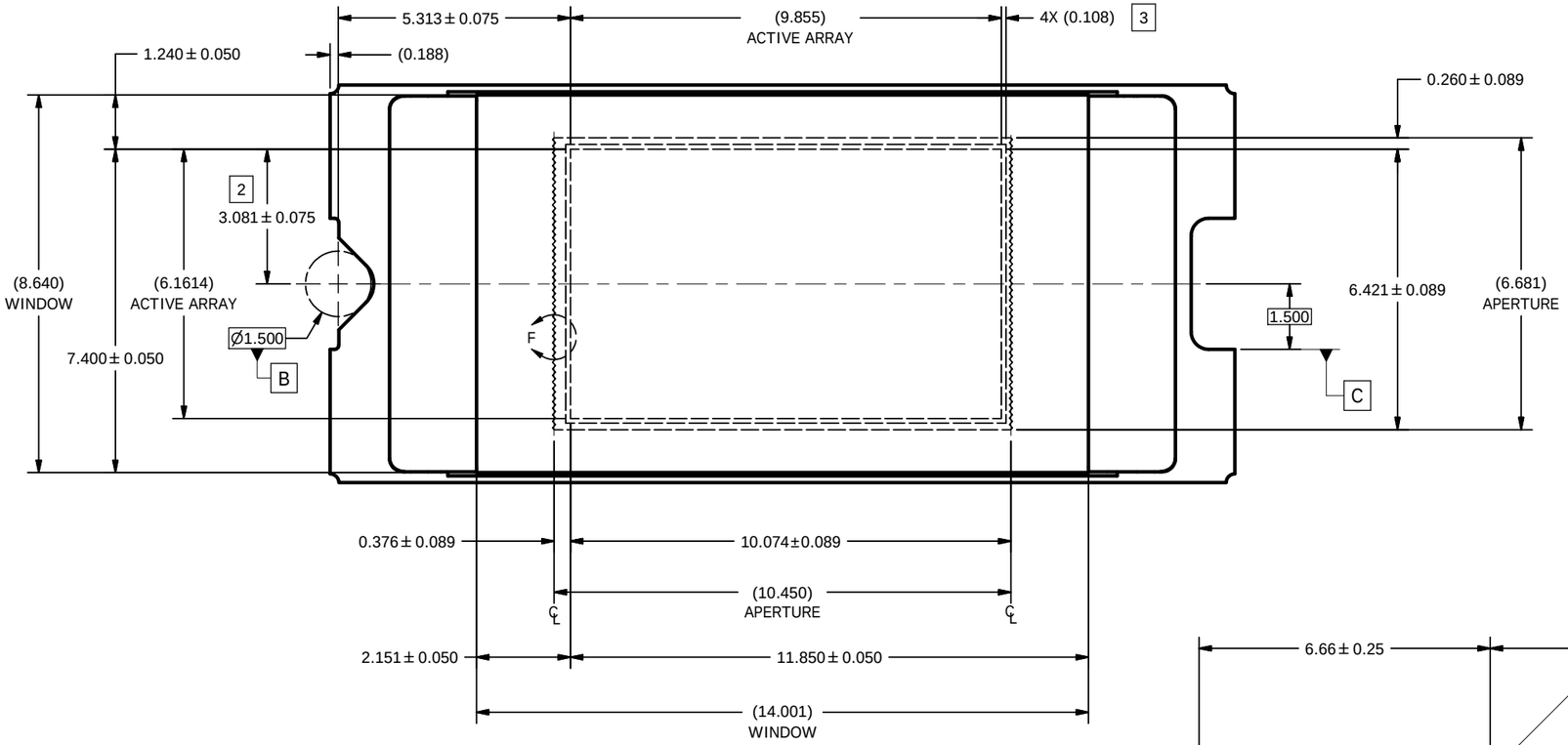
VIEW C
ENCAPSULANT MAXIMUM X/Y DIMENSIONS
SCALE 15 : 1
(FROM SHEET 1)



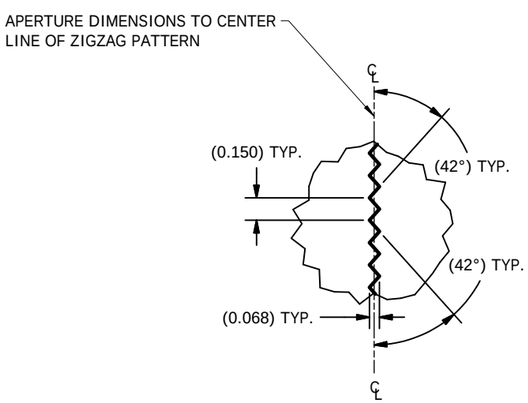
VIEW D
ENCAPSULANT MAXIMUM HEIGHT
SCALE 15 : 1

TEXAS INSTRUMENTS Dallas Texas	DRAWN J. HOLM	DATE 12/11/2009	SIZE D		DWG NO 2510852	REV C
			SCALE		SHEET 2 OF 3	

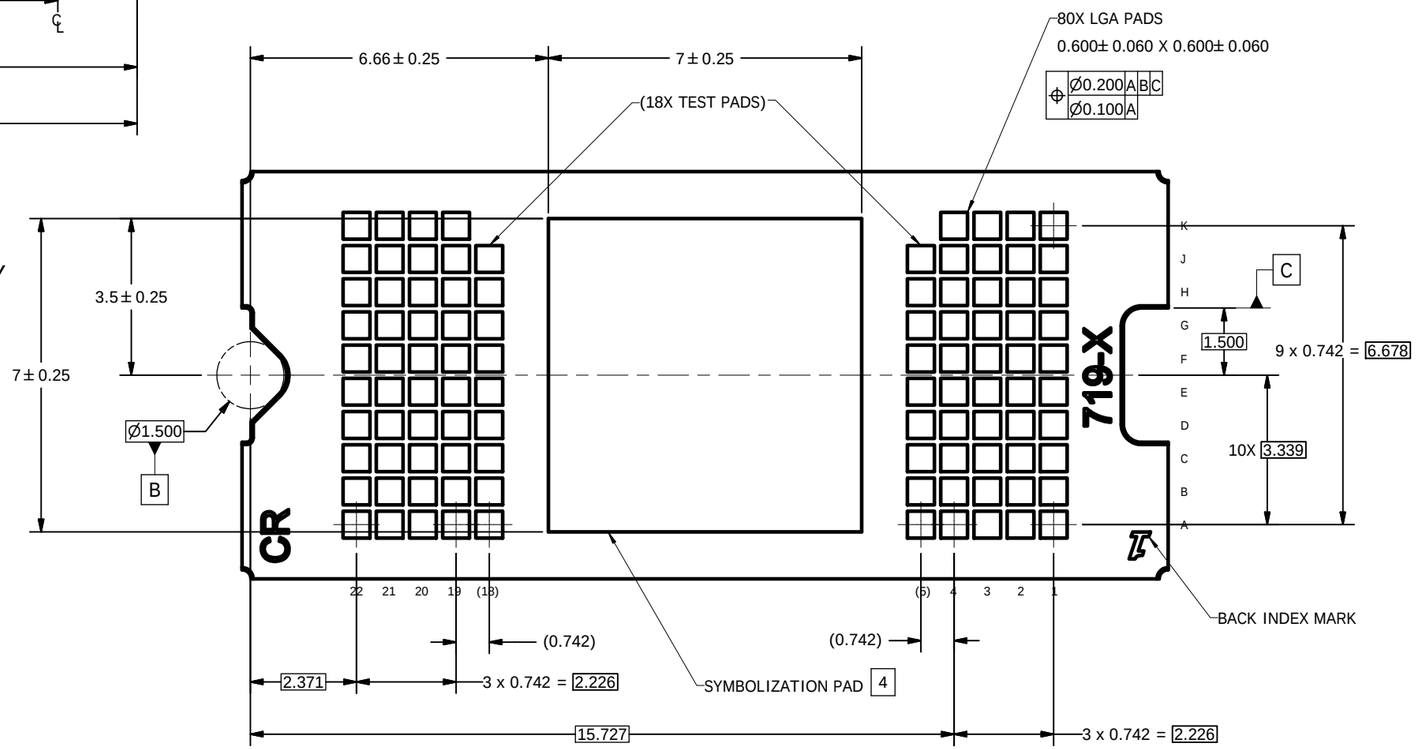
INV11-2006a



VIEW D
WINDOW AND ACTIVE ARRAY
(FROM SHEET 1)



DETAIL F
APERTURE SHORT EDGES
SCALE 50 : 1



VIEW E-E
BACK SIDE METALLIZATION
(FROM SHEET 1)

TEXAS INSTRUMENTS Dallas Texas	DRAWN J. HOLM	DATE 12/11/2009	SIZE D	DWG NO 2510852	REV C
			SCALE	SHEET 3 OF 3	

INV11-2006a

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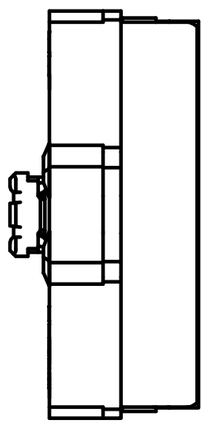
REVISIONS

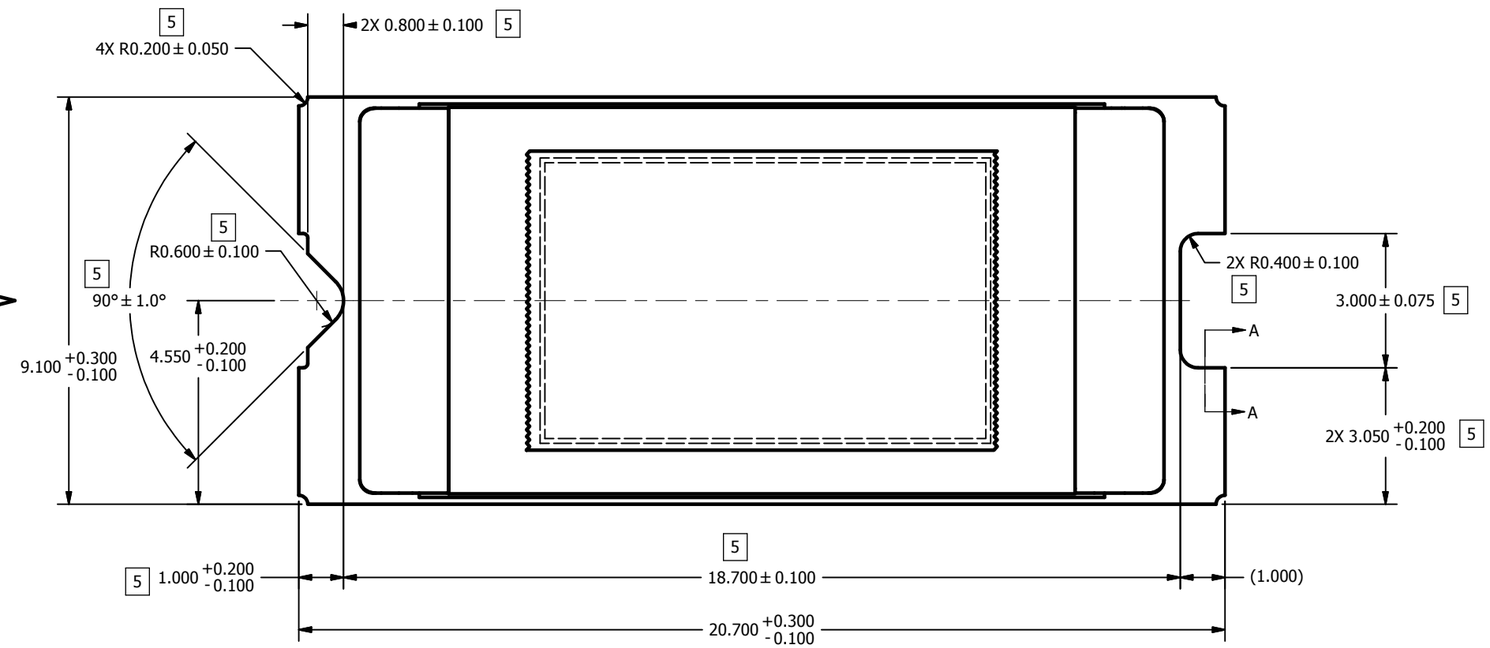
REV	DESCRIPTION	DATE	BY
A	ECO #2109845 - INITIAL RELEASE	8/16/2010	JLH
B	ECO #2121955 - CORRECT APERTURE X DIM'S IN VIEW D	1/23/2012	BMH
C	ECO #2144972 - ADD (FQE PACKAGE) TO TITLE BLOCK	9/11/2014	MAA

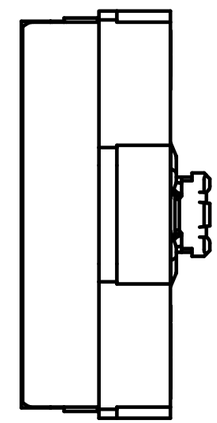
NOTES UNLESS OTHERWISE SPECIFIED:

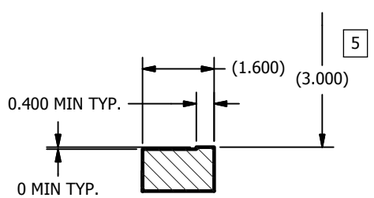
1. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
2. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.6 DEGREES.
3. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE ARRAY.
4. DMD MARKING TO APPEAR IN CONNECTOR RECESS.
5. NOTCH DIMENSIONS ARE DEFINED BY UPPERMOST LAYERS OF CERAMIC, AS SHOWN IN SECTION A-A.
6. ENCAPSULANT TO BE CONTAINED WITHIN DIMENSIONS SHOWN IN VIEWS C AND D (SHEET 2). NO ENCAPSULANT IS ALLOWED ON TOP OF THE WINDOW.
7. WHILE ONLY THE THREE DATUM A TARGET AREAS A1, A2, AND A3 ARE USED FOR MEASUREMENT, ALL 4 CORNERS SHOULD BE CONTACTED, INCLUDING E1, WHEN MOUNTING IN SYSTEM.
8. ENCAPSULANT NOT TO EXCEED THE HEIGHT OF THE WINDOW.



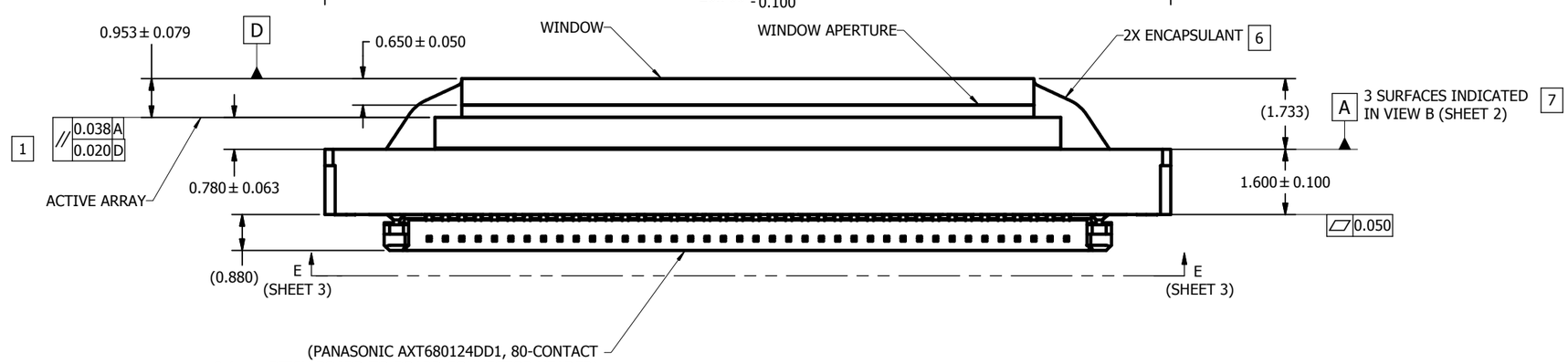
(ILLUMINATION DIRECTION)







5 SECTION A-A
NOTCH OFFSETS



NEXT ASSY	USED ON
NONE	0314DA

APPLICATION

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES:
  - ANGLES ± 1°
  - 2 PLACE DECIMALS ± 0.25
  - 1 PLACE DECIMALS ± 0.50
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994
- REMOVE ALL BURRS AND SHARP EDGES
- PARENTHETICAL INFORMATION FOR REFERENCE ONLY

		DATE
DRAWN	J. HOLM	7/14/2010
ENGINEER	J. HOLM	7/14/2010
QA/CE		
CM		
APPROVED		

TEXAS INSTRUMENTS
Dallas Texas

TITLE
ICD, MECHANICAL, DMD,
.45 WXGA-800 DDR SERIES 241
(FQE PACKAGE)

SIZE	DWG NO	REV
D	2511423	C

SCALE 15:1 SHEET 1 OF 3

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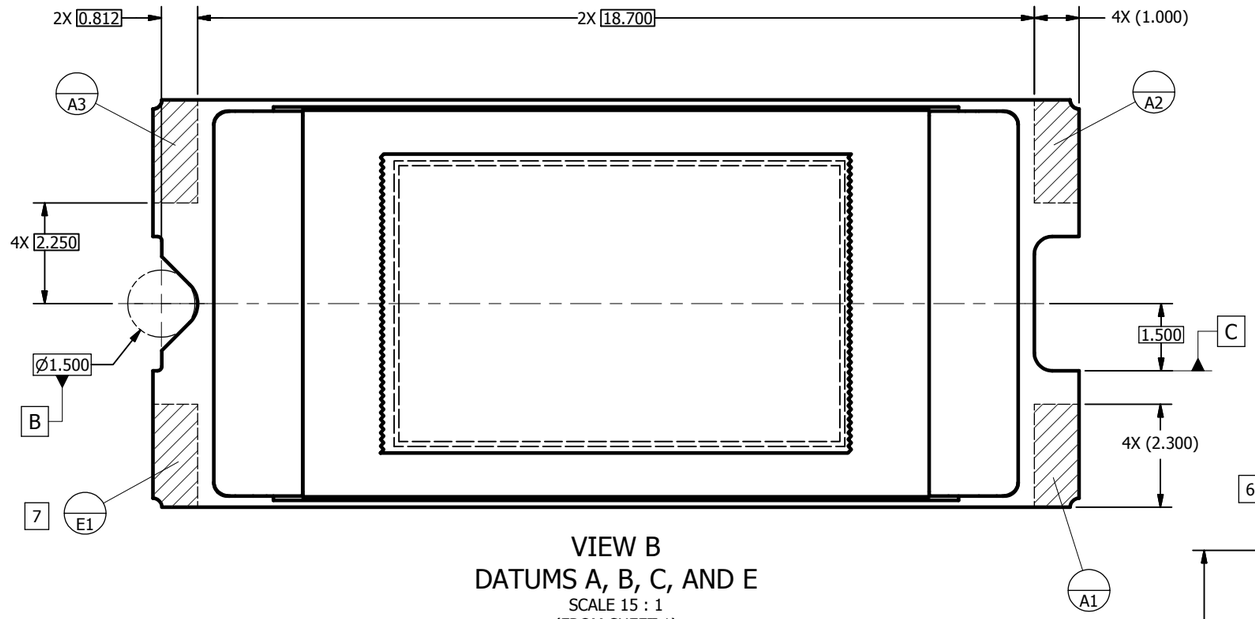
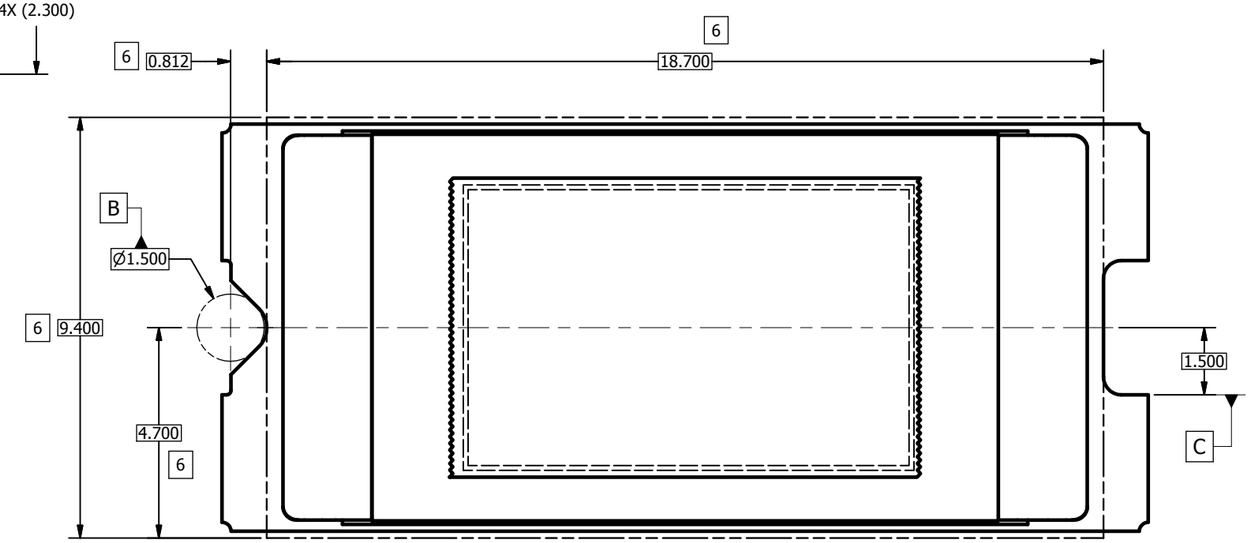
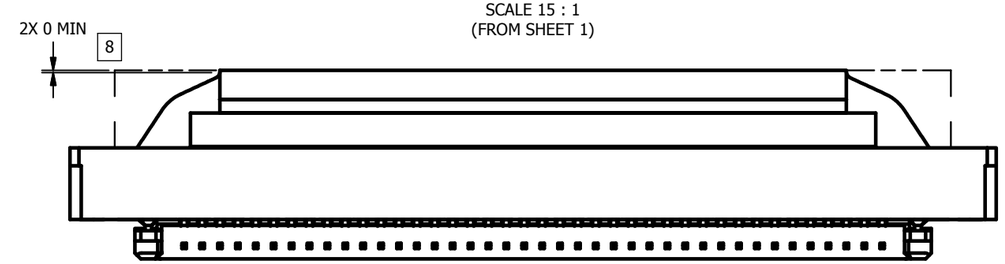


VIEW B
DATUMS A, B, C, AND E
SCALE 15 : 1
(FROM SHEET 1)



VIEW C
ENCAPSULANT MAXIMUM X/Y DIMENSIONS
SCALE 15 : 1
(FROM SHEET 1)



VIEW D
ENCAPSULANT MAXIMUM HEIGHT
SCALE 15 : 1

TEXAS INSTRUMENTS Dallas Texas	DRAWN J. HOLM	DATE 7/14/2010	SIZE D		DWG NO 2511423	REV C
			SCALE		SHEET 2 OF 3	

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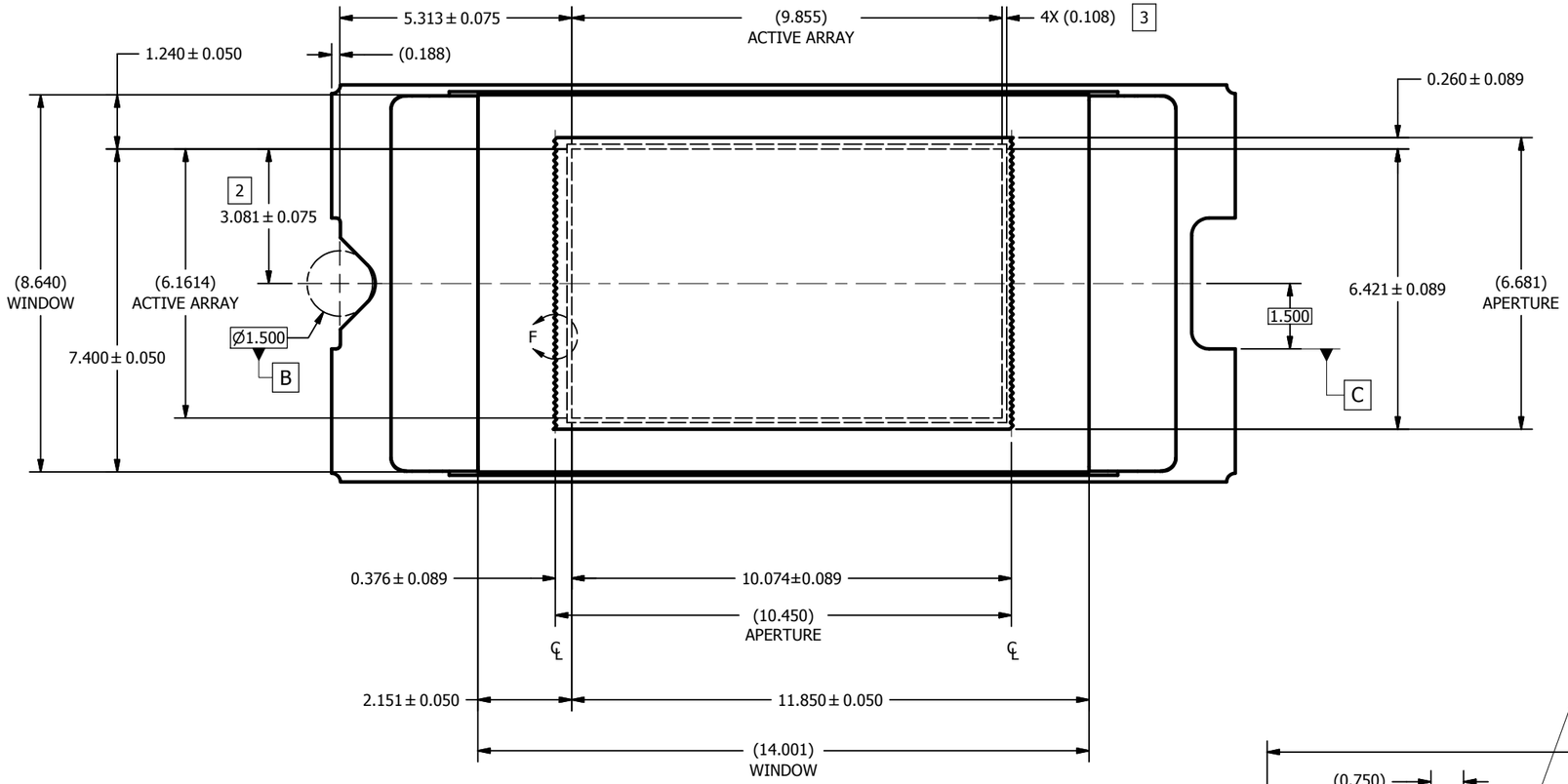
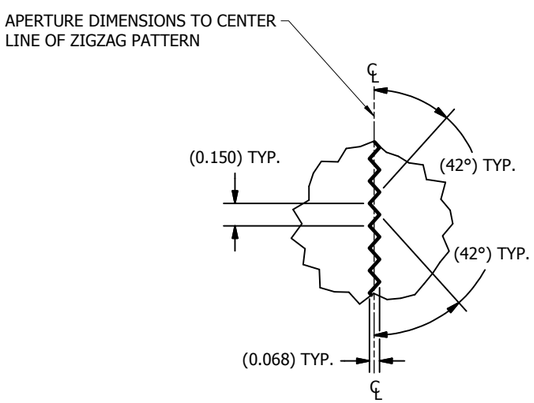
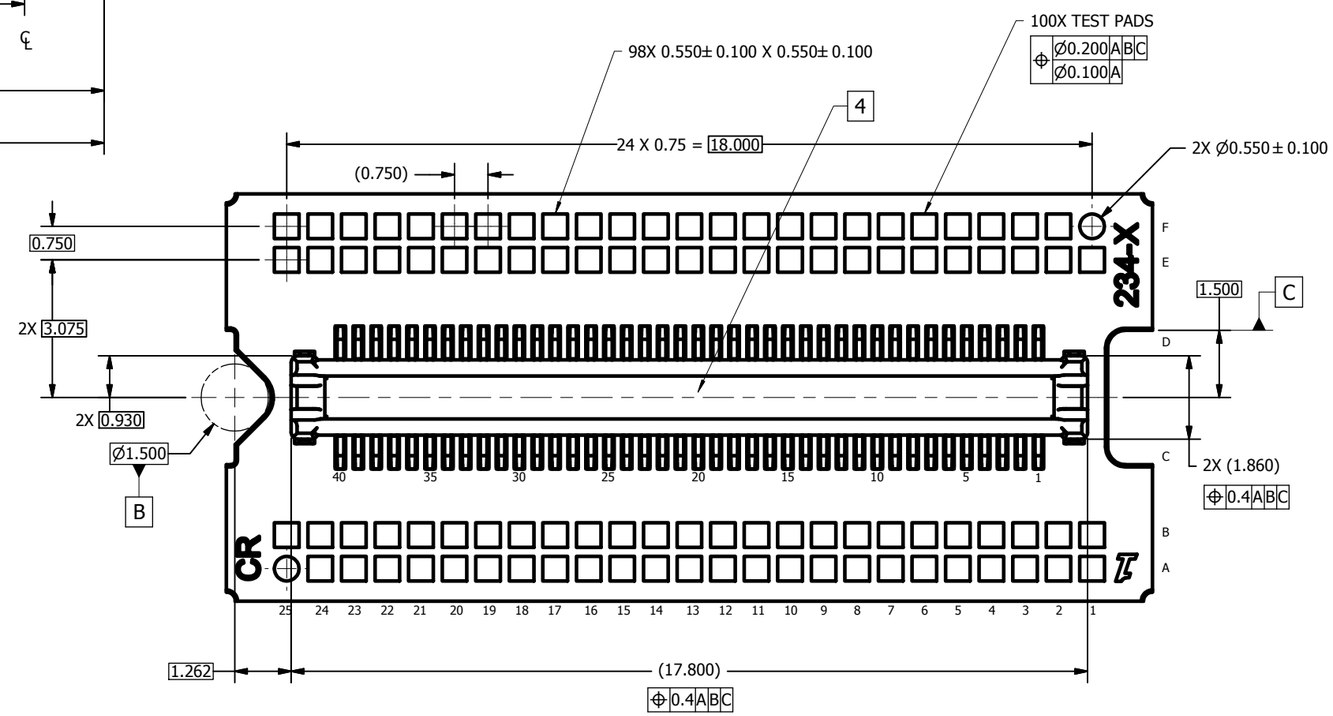


VIEW D
WINDOW AND ACTIVE ARRAY
(FROM SHEET 1)



DETAIL F
APERTURE SHORT EDGES
SCALE 50 : 1



VIEW E-E
TEST PADS AND CONNECTOR
(FROM SHEET 1)

TEXAS INSTRUMENTS Dallas Texas	DRAWN J. HOLM	DATE 7/14/2010	SIZE D	DWG NO 2511423	REV C
			SCALE	SHEET 3 OF 3	

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