

具有可编程固定增益的 2Vrms DirectPath™ 线路驱动器

 查询样品: [DRV612](#)

特性

- **DirectPath™**
 - 消除了噼啪声/喀哒声
 - 免除了输出隔直流电容器
 - **3V 至 3.6V** 电源电压
- 低噪声及THD
 - **SNR > 105dB** (在 **-1x** 增益条件下)
 - 典型 **Vn < 12µVms** (在 **20Hz 至 20kHz** 频率范围内和 **-1x** 增益条件下)
 - **THD + N < 0.003%** (在 **10kΩ** 负载和 **-1x** 增益条件下)
- 可为 **600Ω** 负载提供 **2Vrms** 输出电压
- 单端输入和输出
- 可编程增益选择减少了组件的数量
 - **13x** 增益值
- 具有大于 **80 dB** 衰减的有源静音
- 具短路和热保护功能
- **±8 kV HBM ESD** 保护输出

应用

- **PDP / LCD TV**
- **DVD 播放机**
- 迷你型/微型组合音响系统
- 声卡

说明

DRV612 是一款单端、2Vrms 立体声线路驱动器，专为缩减组件数量、板级空间和成本而设计。对于那些将尺寸和成本作为关键设计参数的单电源电子产品而言，该器件是理想的选择。

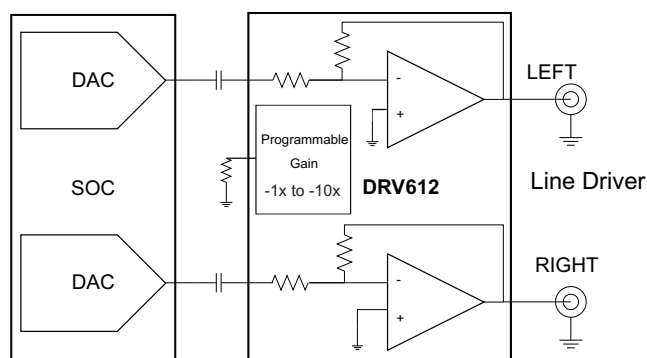
DRV612 既不需要采用一个高于 3.3V 的电源来产生其 5.6V_{pp} 输出，也不需要一个分离轨电源。

DRV612 的设计运用了 TI 的 DirectPath 专利技术，集成了一个充电泵以产生一个负电源轨，可提供干净、无噼啪声的接地偏置输出。DRV612 能够向一个 600Ω 负载输送 2Vrms 驱动电压。另外，DirectPath 技术还允许去除昂贵的输出隔直流电容器。

该器件具有固定增益单端输入和一个增益选择引脚。通过在该引脚上使用单个电阻器，设计人员就能够从 13 种内部可编程增益设定值中进行选择，以使线路驱动器与编解码器输出电平相匹配。另外，它还削减了组件数量和板级空间。

线路输出具有 ±8 kV HBM ESD 保护等级，从而实现了简单的 ESD 保护电路。DRV612 内置了具有大于 80 dB 衰减的有源静音控制功能电路，用于实现无噼啪声的静音接通/关断控制。

DRV612 采用 14 引脚 TSSOP 封装和 16 引脚 QFN 封装。如需一款具有兼容焊脚的立体声头戴式耳机驱动器，请查阅 TPA6139A2 的文档资料 ([SLOS700](#))。



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DirectPath is a trademark of Texas Instruments.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

版权 © 2010–2011, Texas Instruments Incorporated
English Data Sheet: [SLOS690B](#)

DRV612

ZHCS317B – DECEMBER 2010 – REVISED APRIL 2011

www.ti.com.cn



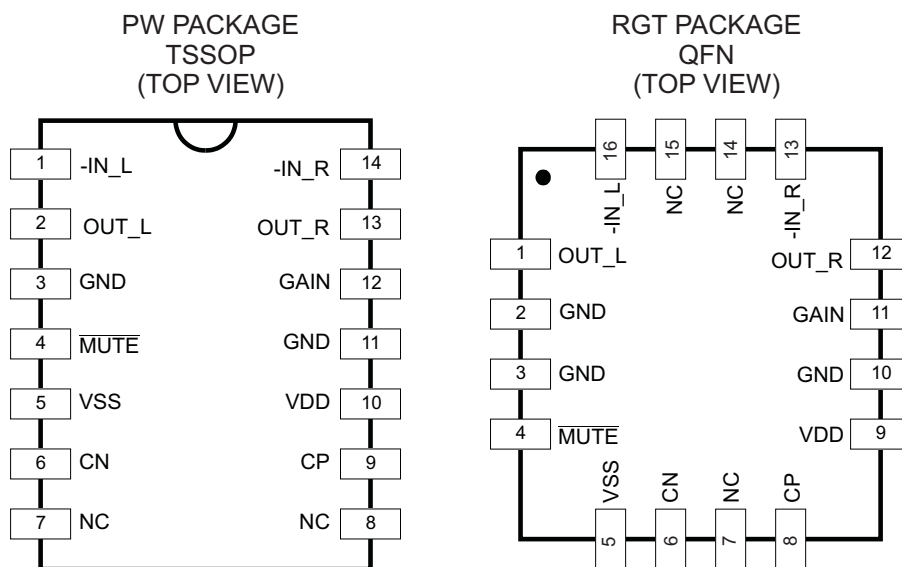
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

GENERAL INFORMATION

TERMINAL ASSIGNMENT

The DRV612 is available in package:

- 14-pin TSSOP package (PW) or 16-pin QFN package (RGT)

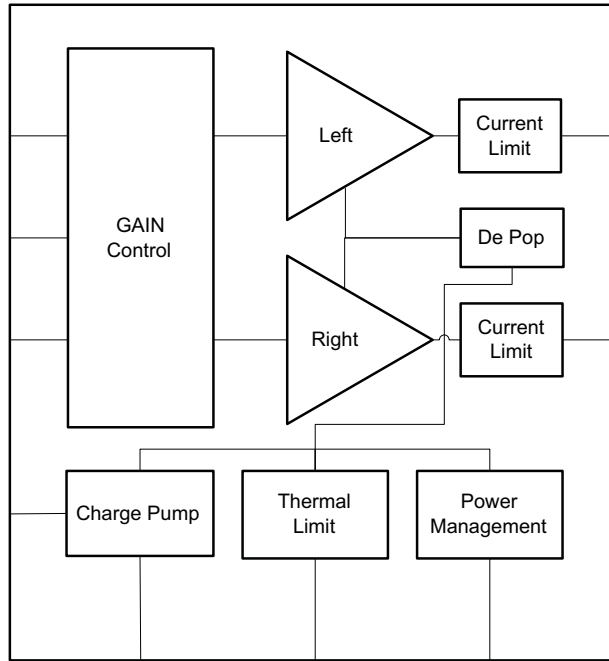


PIN FUNCTIONS

PIN		RGT NO.	FUNCTION ⁽¹⁾	DESCRIPTION
NAME	PW NO.			
-IN_L	1	16	I	Negative input, left channel
OUT_L	2	1	O	Output, left channel
GND	3, 11	2, 3, 10	P	Ground
$\overline{\text{MUTE}}$	4	4	I	MUTE, active low
VSS	5	5	O	Change Pump negative supply voltage
CN	6	6	I/O	Charge Pump flying capacitor negative connection
NC	7, 8	7, 14, 15		No internal connection
CP	9	8	I/O	Charge Pump flying capacitor positive connection
VDD	10	9	P	Supply voltage, connect to positive supply
GAIN	12	11	I	Gain set programming pin; connect a resistor to ground. See 表 1 for recommended resistor values
OUT_R	13	12	O	Output, right channel
-IN_R	14	13	I	Negative input, right channel
Thermal Pad	n/a	Thermal Pad	P	Connect to ground

(1) I = input, O = output, P = power

SYSTEM BLOCK DIAGRAM



ORDERING INFORMATION⁽¹⁾

T_A	PACKAGE	DESCRIPTION
-40°C to 85°C	DRV612PW	14-pin TSSOP
	DRV612RGT	16-pin QFN

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		DRV612	DRV612	UNITS
		RGT (16-Pin)	PW (14-Pin)	
θ_{JA}	Junction-to-ambient thermal resistance	52	130	°C/W
θ_{JCTop}	Junction-to-case (top) thermal resistance	71	49	
θ_{JB}	Junction-to-board thermal resistance	26	63	
Ψ_{JT}	Junction-to-top characterization parameter	3.0	3.6	
Ψ_{JB}	Junction-to-board characterization parameter	26	62	
θ_{JCbott}	Junction-to-case (bottom) thermal resistance	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](http://www.ti.com/lit/an/spra953).

DRV612

ZHCS317B – DECEMBER 2010 – REVISED APRIL 2011

www.ti.com.cn

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Voltage range	VDD to GND	–0.3	4	V
	V _I , Input voltage	VSS – 0.3	VDD + 0.3	
	$\overline{\text{MUTE}}$ to GND	–0.3	VDD + 0.3	
Temperature	Maximum operating junction temperature range, T _J	–40	150	°C
	Storage temperature	–65	150	
Electrostatic discharge (HBM) QSS 009-105 (JESD22-A114A)	OUT_L, OUT_R	8		kV
	All other pins	2		

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range unless otherwise noted

		MIN	NOM	MAX	UNIT		
VDD	Supply voltage	DC supply voltage		3.0	3.3	3.6	V
R _L		600	10k				Ω
V _{IL}	Low-level input voltage	$\overline{\text{MUTE}}$		38	40	43	%VDD
V _{IH}	High-level input voltage	$\overline{\text{MUTE}}$		57	60	66	%VDD
T _A	Free-air temperature	–0	25	85			°C

ELECTRICAL CHARACTERISTICS

VDD = 3.3V, R_{LD} = 5 kΩ, T_A = 25°C, Charge pump: C_{CP} = 1 μF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OS}	Output offset voltage	VDD = 3.3 V, input ac-coupled		0.5	1	mV
PSRR	Power-supply rejection ratio		70	80		dB
V _{OH}	High-level output voltage	VDD = 3.3 V	3.1			V
V _{OL}	Low-level output voltage	VDD = 3.3 V			-3.05	V
V _{uvp_on}	VDD, undervoltage detection				2.8	V
V _{uvp_hysteresis}	VDD, undervoltage detection, hysteresis			200		mV
F _{CP}	Charge-pump switching frequency			350		kHz
I _{IH}	High-level input current, $\overline{\text{MUTE}}$	VDD = 3.3 V, V _{IH} = VDD			1	μA
I _{IL}	Low-level input current, $\overline{\text{MUTE}}$	VDD = 3.3 V, V _{IL} = 0 V			1	μA
I _(VDD)	Supply current, no load	VDD, $\overline{\text{MUTE}} = 3.3 \text{ V}$		18		mA
	Supply current, MUTED	VDD = 3.3 V, $\overline{\text{MUTE}} = \text{GND}$		18		mA
T _{SD}	Thermal shutdown			150		°C
	Thermal shutdown hysteresis			15		°C

ELECTRICAL CHARACTERISTICS, LINE DRIVER

VDD = 3.3 V, R_{LOAD} = 10 kΩ, T_A = 25°C, Charge pump: C_{CP} = 1 μF, 1× gain select (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _O	Output voltage, outputs in phase	1% THD+N, f = 1 kHz, 10 -kΩ load		2.2		V _{rms}
THD+N	Total harmonic distortion plus noise	f = 1 kHz, 10-kΩ load, V _O = 2 V _{rms}		0.007%		
SNR	Signal-to-noise ratio	A-weighted, AES17 filter, 2 V _{rms} ref		105		dB
DNR	Dynamic range	A-weighted, AES17 filter, 2 V _{rms} ref		105		dB
V _n	Noise voltage	A-weighted, AES17 filter		12		μV
Z _o	Output impedance when muted	$\overline{\text{MUTE}} = \text{GND}$		0.07	1	Ω
	Input-to-output attenuation when muted	1 V _{rms} , 1-kHz input		80		dB
	Slew rate			4.5		V/μs
G _{BW}	Unity-gain bandwidth			8		MHz
	Crosstalk – Line L-R and R-L	10-kΩ load, V _O = 2 V _{rms}		-91		dB
I _{limit}	Current limit	VDD = 3.3 V		25		mA

DRV612

ZHCS317B–DECEMBER 2010–REVISED APRIL 2011

www.ti.com.cn

PROGRAMMABLE GAIN SETTINGS⁽¹⁾⁽²⁾

 VDD = 3.3 V, R_{load} = 10 kΩ, T_A = 25°C, Charge pump: C_{CP} = 1 μF, 1× gain select, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_Tol	Gain programming resistor tolerance			2%	
ΔA _V	Gain matching	Between left and right channels		0.25	dB
	Gain step tolerance		0.1		dB
Gain steps	Gain resistor 2% tolerance				V/V
	249k or higher		–2		
	82k5		–1		
	51k1		–1.5		
	34k8		–2.3		
	27k4		–2.5		
	20k5		–3		
	15k4		–3.5		
	11k5		–4		
	9k09		–5		
	7k50		–5.6		
	6k19		–6.4		
5k11		–8.3			
4k22		–10			
Input impedance	Gain resistor 2% tolerance				kΩ
	249k or higher		37		
	82k5		55		
	51k1		44		
	34k8		33		
	27k4		31		
	20k5		28		
	15k4		24		
	11k5		22		
	9k09		18		
	7k50		17		
	6k19		15		
5k11		12			
4k22		10			

- (1) If the GAIN pin is left floating, an internal pullup sets the gain to –2×.
- (2) Gain setting is latched during power up.

TYPICAL CHARACTERISTICS, LINE DRIVER

$V_{DD} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 2.5\text{ k}\Omega$, $C_{PUMP} = C_{(VSS)} = 1\ \mu\text{F}$, Gain = -2V/V (unless otherwise noted)

THD+N vs OUTPUT VOLTAGE
3.3 V, 10 k Ω , 1 kHz

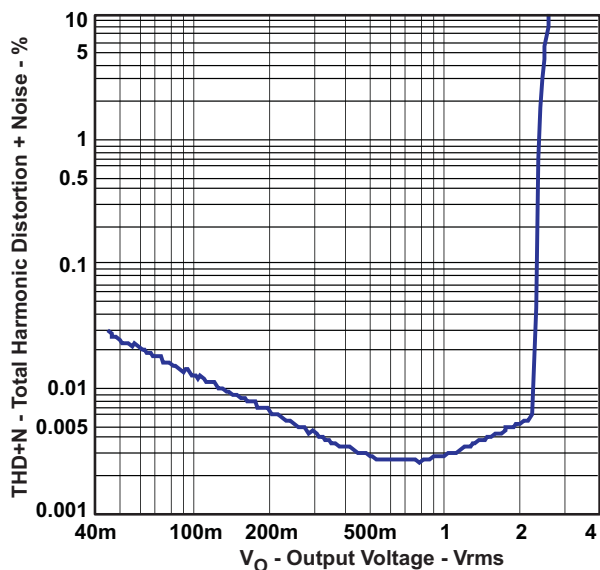


图 1.

THD+N vs OUTPUT VOLTAGE
3.3 V, 600 Ω load, 1 kHz

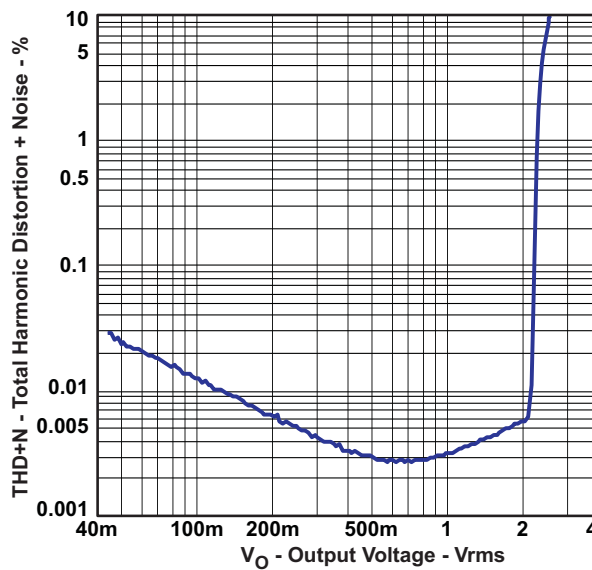


图 2.

THD+N vs FREQUENCY
3.3 V, 10 k Ω load, 2 Vrms

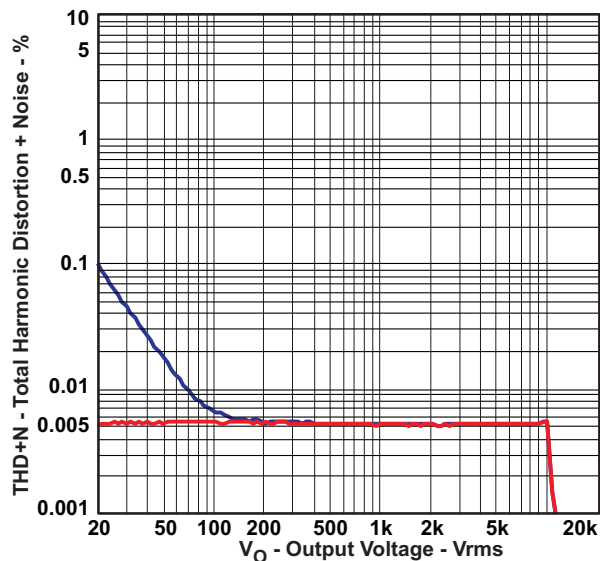


图 3.

CHANNEL SEPARATION

3.3 V, 5 k Ω load, 2 Vrms, Blue L to R, Red R to L

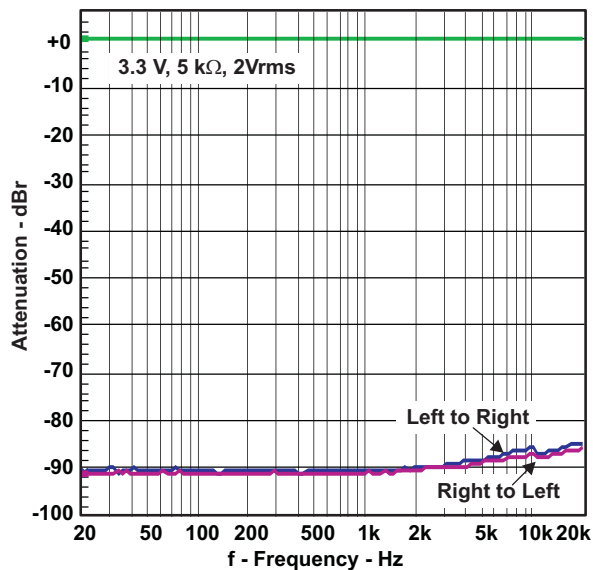


图 4.

Blue: 10- μF ceramic ac-coupling capacitor.

Red: 10- μF electrolytic ac-coupling capacitor

TYPICAL CHARACTERISTICS, LINE DRIVER (接下页)

$V_{DD} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 2.5\text{ k}\Omega$, $C_{PUMP} = C_{(VSS)} = 1\text{ }\mu\text{F}$, Gain = $-2V/V$ (unless otherwise noted)

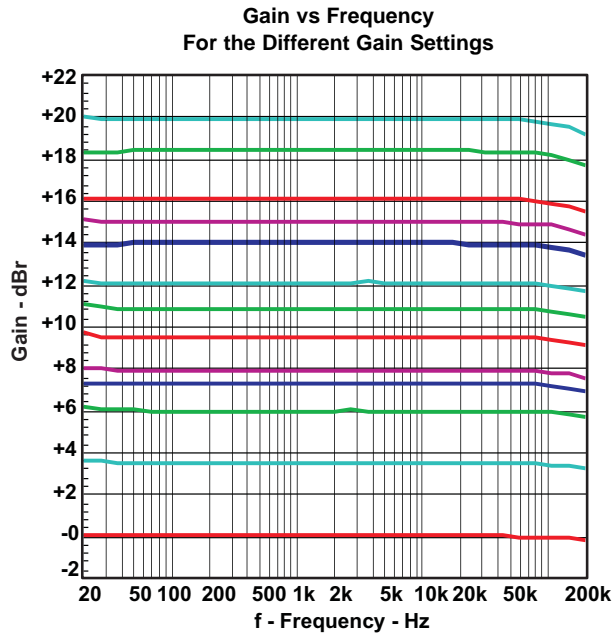


图 5.

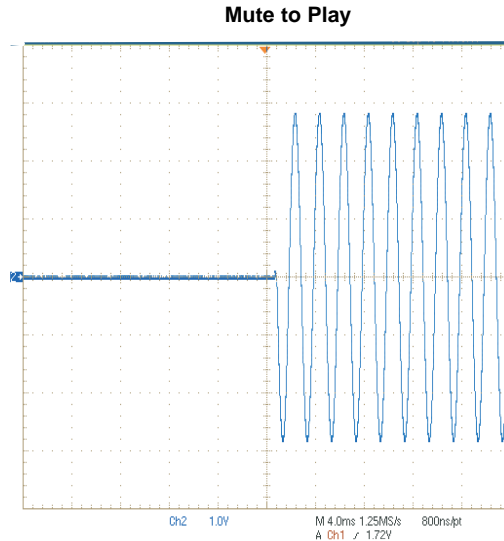


图 6.

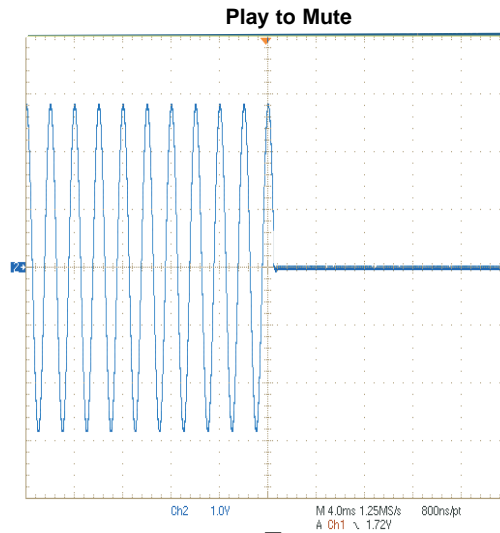


图 7.

APPLICATION INFORMATION

LINE DRIVER AMPLIFIERS

Single-supply line-driver amplifiers typically require dc-blocking capacitors. The top drawing in 图 8 illustrates the conventional line-driver amplifier connection to the load and output signal.

DC blocking capacitors are often large in value, and a mute circuit is needed during power up to minimize click and pop. The output capacitor and mute circuit consume PCB area and increase cost of assembly, and can reduce the fidelity of the audio output signal.

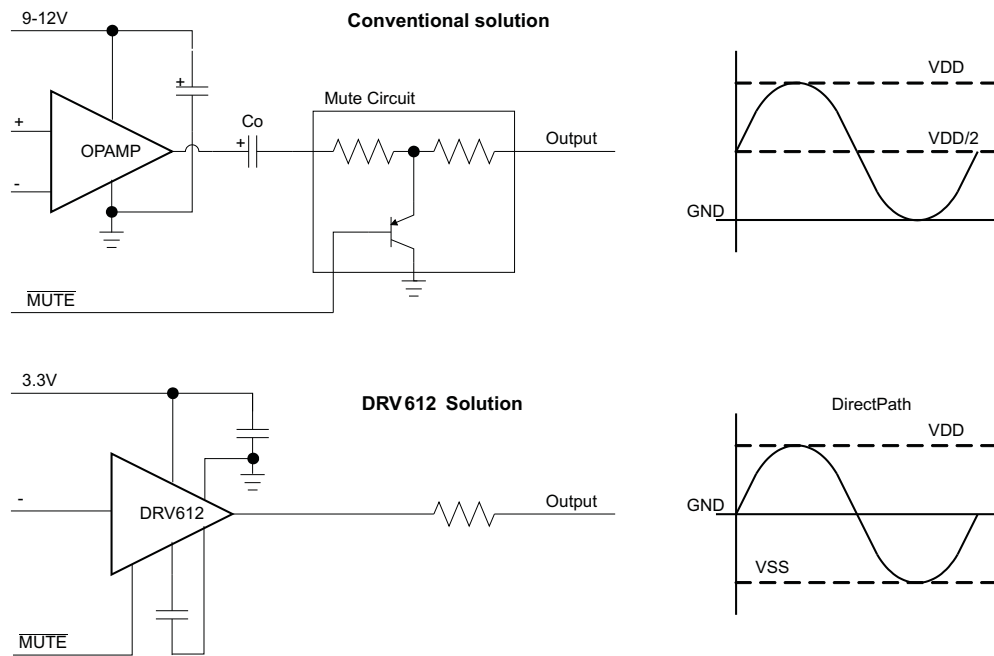


图 8. Conventional and DirectPath Line Driver

The DirectPath amplifier architecture operates from a single supply but makes use of an internal charge pump to provide a negative voltage rail.

Combining the user-provided positive rail and the negative rail generated by the IC, the device operates in what is effectively a split supply mode.

The output voltages are now centered at zero volts with the capability to swing to the positive rail or negative rail. Combining this with the built-in click- and pop-reduction circuit, the DirectPath amplifier requires no output dc-blocking capacitors.

The bottom block diagram and waveform of 图 8 illustrate the ground-referenced line-driver architecture. This is the architecture of the DRV612.

COMPONENT SELECTION

Charge Pump Flying Capacitor and VSS Capacitor

The charge-pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The VSS capacitor must be at least equal to the charge pump capacitor in order to allow maximum charge transfer. Low-ESR capacitors are an ideal selection, and a value of 1 μF is typical.

Decoupling Capacitors

The DRV612 is a DirectPath line-driver amplifier that requires adequate power-supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 μF , placed as close as possible to the device VDD lead works best. Placing this decoupling capacitor close to the DRV612 is important for the performance of the amplifier. For filtering lower-frequency noise signals, a 10- μF or greater capacitor placed near the audio power amplifier also helps, but it is not required in most applications because of the high PSRR of this device.

Gain-Setting

The gain setting is programmed with the GAIN pin. Gain setting is latched during power on. 表 1 lists the gain settings.

NOTE: If gain pin is left unconnected (open) default gain of $-2\times$ is selected.

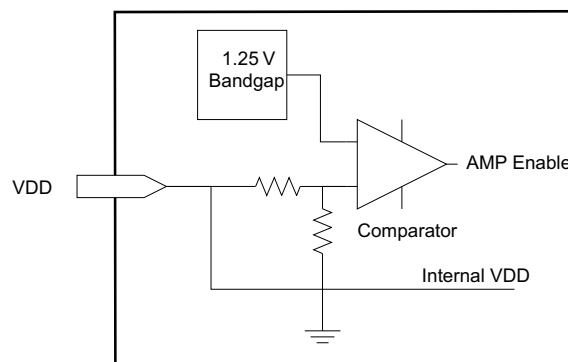
表 1. Gain Settings

Gain_set RESISTOR	GAIN	GAIN (dB)	INPUT RESISTANCE
249 k Ω ⁽¹⁾	$-2\times$	6	37 k Ω
82k5	$-1\times$	0.0	55 k Ω
51k1	$-1.5\times$	3.5	44 k Ω
34k8	$-2.3\times$	7.2	33 k Ω
27k4	$-2.5\times$	8	31 k Ω
20k5	$-3\times$	9.5	28 k Ω
15k4	$-3.5\times$	10.9	24 k Ω
11k5	$-4.0\times$	12	22 k Ω
9k09	$-5\times$	14	18 k Ω
7k5	$-5.6\times$	15	17 k Ω
6k19	$-6.4\times$	16.1	15 k Ω
5k11	$-8.3\times$	18.4	12 k Ω
4k22	$-10\times$	20	10 k Ω

(1) or higher

Internal Undervoltage Detection

The DRV612 contains an internal precision band-gap reference voltage and a comparator used to monitor the supply voltage, VDD. The internal VDD monitor is set at 2.8 V with 200-mV hysteresis.



Input-Blocking Capacitors

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the DRV612. These capacitors block the dc portion of the audio source and allow the DRV612 inputs to be properly biased to provide maximum performance. The input blocking capacitors also limit the dc gain to 1, limiting the dc-offset voltage at the output.

These capacitors form a high-pass filter with the input resistor, R_{IN} . The cutoff frequency is calculated using [公式 1](#). For this calculation, the capacitance used is the input-blocking capacitor and the resistance is the input resistor chosen from [表 2](#). Then the frequency and/or capacitance can be determined when one of the two values is given.

$$f_{C_{IN}} = \frac{1}{2\pi R_{IN} C_{IN}} \quad \text{or} \quad C_{IN} = \frac{1}{2\pi f_{C_{IN}} R_{IN}} \quad (1)$$

For a fixed cutoff frequency of 2 Hz, the size of the input capacitance is shown in [表 2](#) with the capacitors rounded up to nearest E6 values. For 20-Hz cutoff, simply divide the capacitor values with 10; e.g., for 1× gain, 150 nF is needed.

表 2. Input Capacitor for Different Gain and Cutoff

Gain_set RESISTOR	GAIN	Gain (dB)	INPUT RESISTANCE	2 Hz Cutoff
249 kΩ	-2 ×	6	37 kΩ	2.2 μF
82k5	-1 ×	0.0	55 kΩ	1.5 μF
51k1	-1.5×	3.5	44 kΩ	2.2 μF
34k8	-2.3×	7.2	33 kΩ	3.3 μF
27k4	-2.5×	8	31 kΩ	3.3 μF
20k5	-3×	9.5	28 kΩ	3.3 μF
15k4	-3.5×	10.9	24 kΩ	3.3 μF
11k5	-4×	12	22 kΩ	4.7 μF
9k09	-5×	14	18 kΩ	4.7 μF
7k5	-5.6×	15	17 kΩ	4.7 μF
6k19	-6.4×	16.1	15 kΩ	6.8 μF
5k11	-8.3×	18.4	12 kΩ	6.8 μF
4k22	-10×	20	10 kΩ	10 μF

Pop-Free Power Up

Pop-free power up is ensured by keeping the $\overline{\text{MUTE}}$ pin low during power-supply ramp-up and -down. The pins should be kept low until the input ac-coupling capacitors are fully charged before asserting the $\overline{\text{MUTE}}$ pin high, this way proper pre-charge of the ac-coupling is performed and pop-less power up is achieved. [图 9](#) illustrates the preferred sequence.

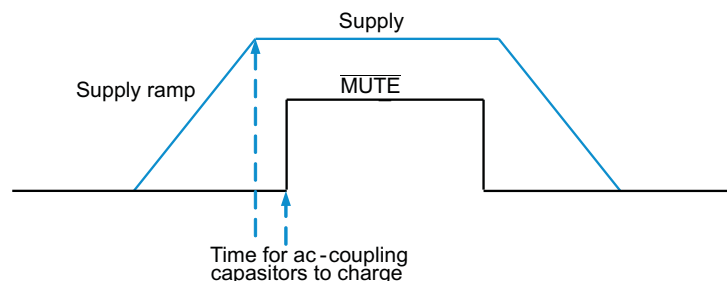


图 9. Power-Up/Down Sequence

DRV612

ZHCS317B–DECEMBER 2010–REVISED APRIL 2011

www.ti.com.cn

CAPACITIVE LOAD

The DRV612 has the ability to drive a high capacitive load up to 220 pF directly. Higher capacitive loads can be accepted by adding a series resistor of 47 Ω or larger for the line driver output.

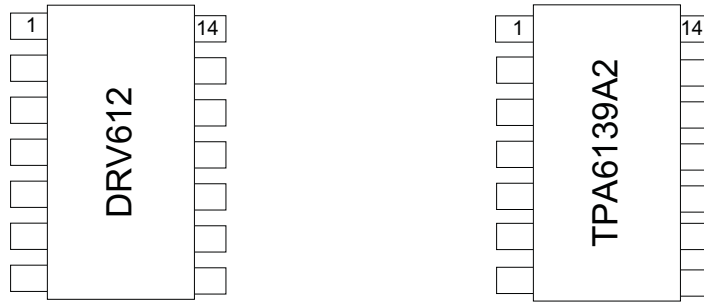
LAYOUT RECOMMENDATIONS

A proposed layout for the DRV612 can be seen in the DRV612EVM User's Guide ([SLOU248](#)), and the Gerber files can be downloaded from <http://focus.ti.com/docs/toolsw/folders/print/DRV612evm.html>. To access this information, open the DRV612 product folder and look in the Tools and Software folder.

Ground traces are recommended to be routed as a star ground to minimize hum interference. VDD, VSS decoupling capacitors and the charge-pump capacitors should be connected with short traces.

FOOTPRINT COMPATIBLE WITH TPA6139A2

The DRV612 stereo line driver is pin compatible with the headphone amplifier TPA6139A2. Therefore, a single PCB layout can be used with stuffing options for different board configurations.



APPLICATION CIRCUIT

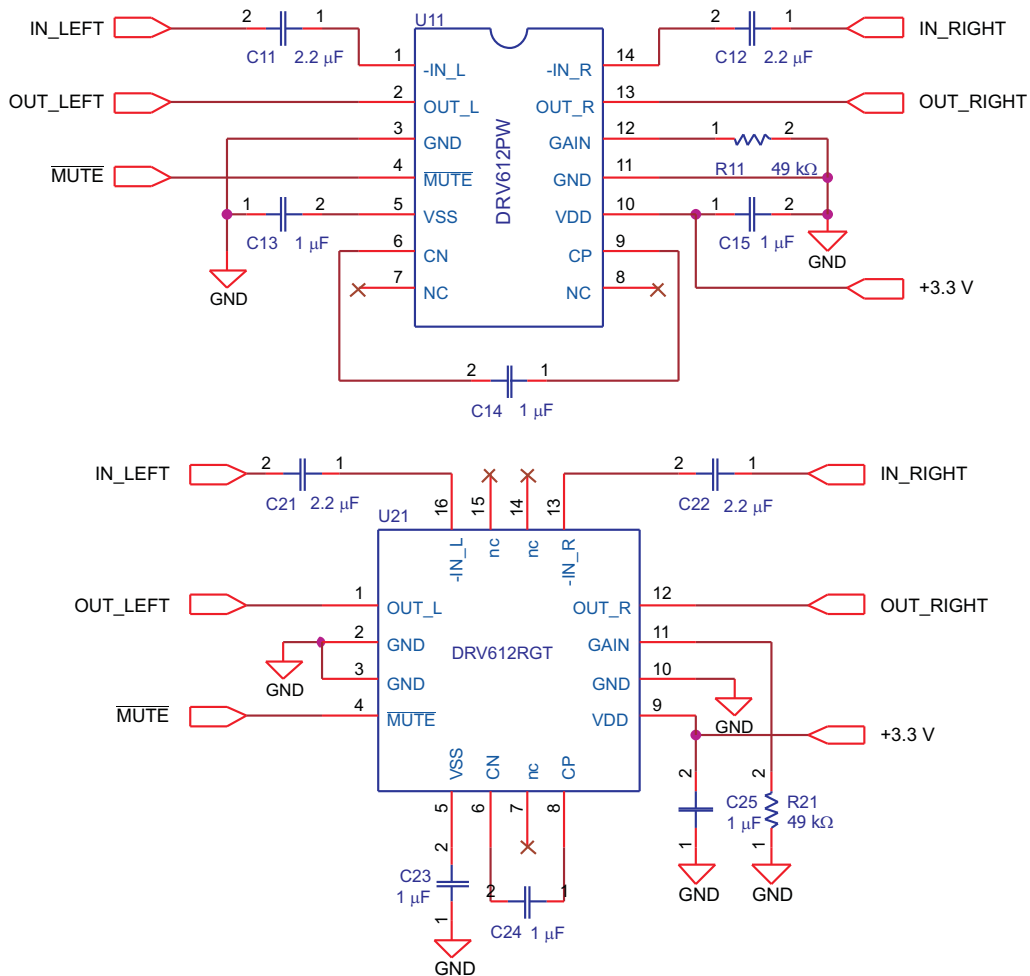


图 10. Single-Ended Input and Output, Gain Set to $-1.5\times$

REVISION HISTORY

Changes from Original (December 2010) to Revision A	Page
• Added the QFN pinout drawing	2
• Added the QFN device To the PIN FUNCTIONS table	2
• Changed the Abs Max Storage Temp From: MIN = -40 To: MIN = -65	4
• Changed the Gain resistor 2% tolerance values in the Programmable Gain Settings table For Gain Steps and Input Impedance	6
• Changed Note 1 of the PROGRAMMABLE GAIN SETTINGS table From: If pin 12, GAIN, is left floating To: If the GAIN pin is left floating	6
• Changed From: $C_{PUMP} = C_{(VSS)} = 10 \mu F$ To: $C_{PUMP} = C_{(VSS)} = 1 \mu F$ in the Typical Characteristics condition text	7
• Changed the Gain_set RESISTOR values in 表 1	10
• Changed the Gain_set RESISTOR values in 表 2	11
• Removed references to DRV614 from the FOOTPRINT COMPATIBLE WITH TPA6139A2 section	13
Changes from Revision A (February 2011) to Revision B	
• Deleted the Product Preview note from the RGT package	3
• Changed $R_{IN} = 10 \text{ k}\Omega$, $R_{fb} = 20 \text{ k}\Omega$ To Gain = -2V/V in the Typical Characteristics condition text	7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV612PW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV612	Samples
DRV612PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV612	Samples
DRV612RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	D612	Samples
DRV612RGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	D612	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV612PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DRV612RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DRV612RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV612PWR	TSSOP	PW	14	2000	350.0	350.0	43.0
DRV612RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
DRV612RGTT	VQFN	RGT	16	250	210.0	185.0	35.0

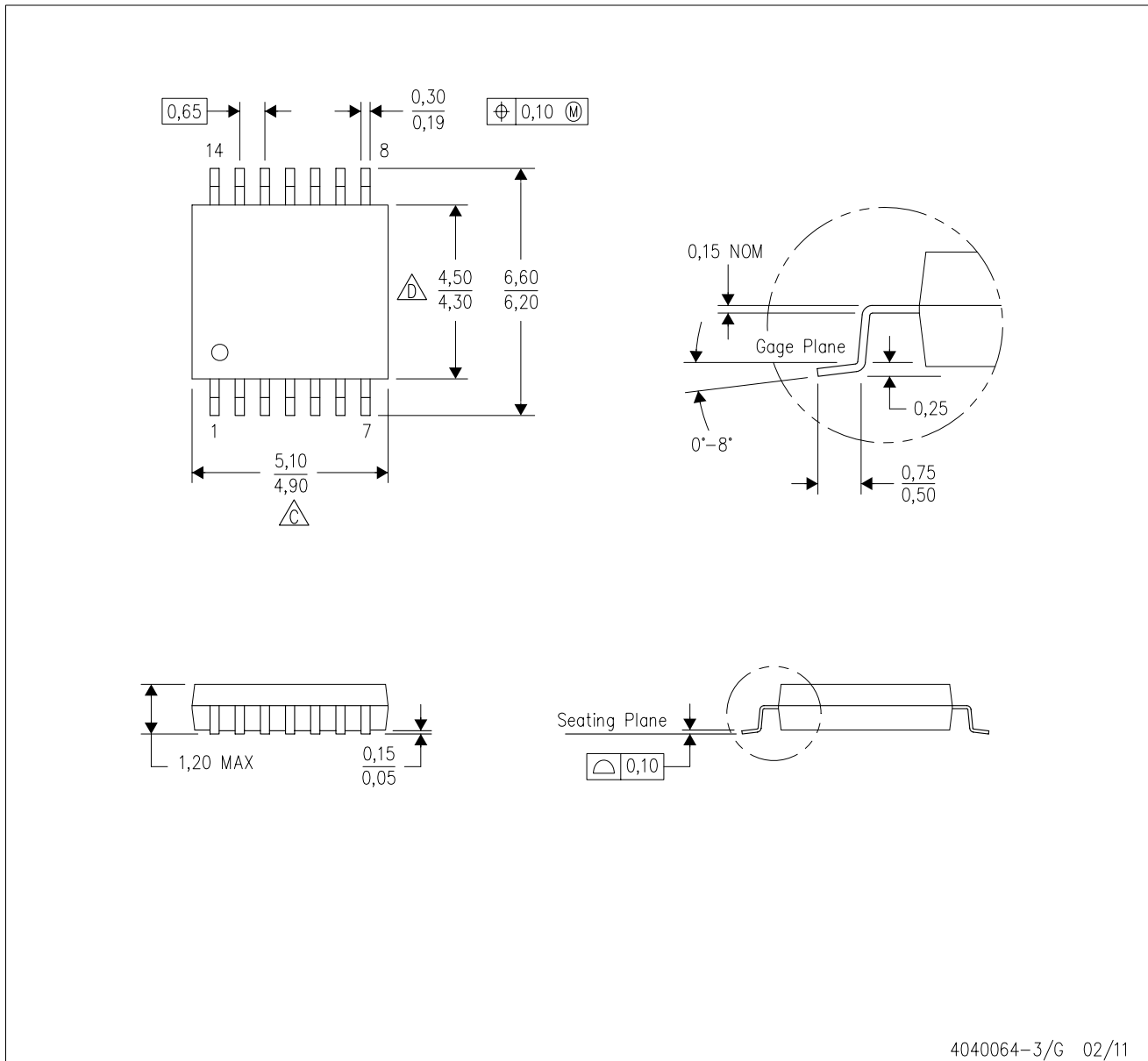
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
DRV612PW	PW	TSSOP	14	90	530	10.2	3600	3.5

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

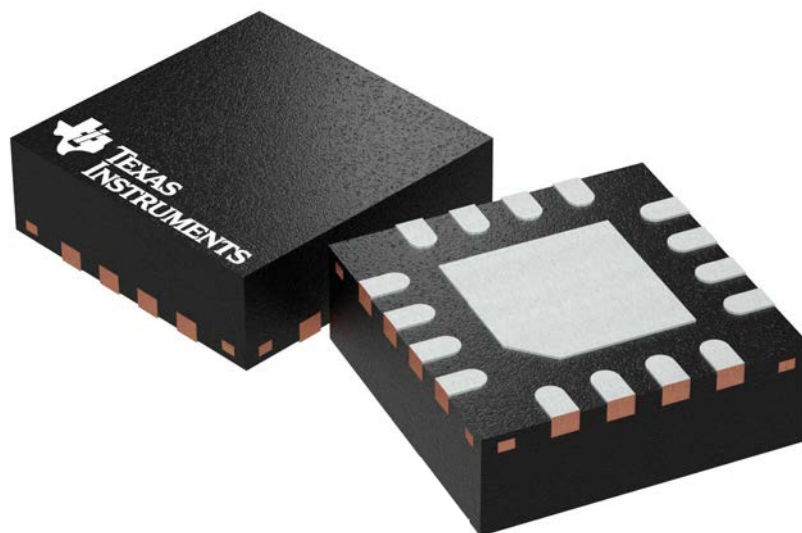
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGT 16

GENERIC PACKAGE VIEW

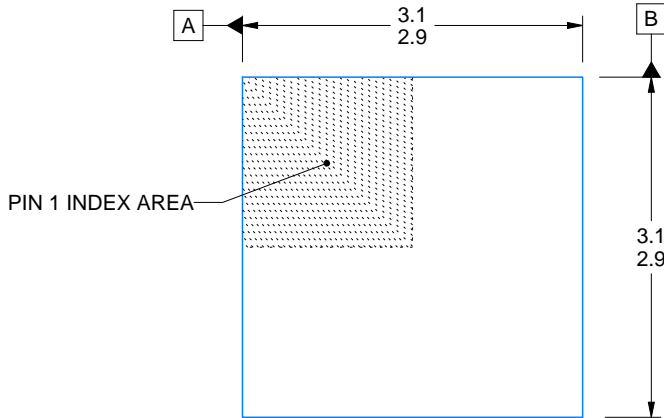
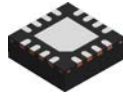
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

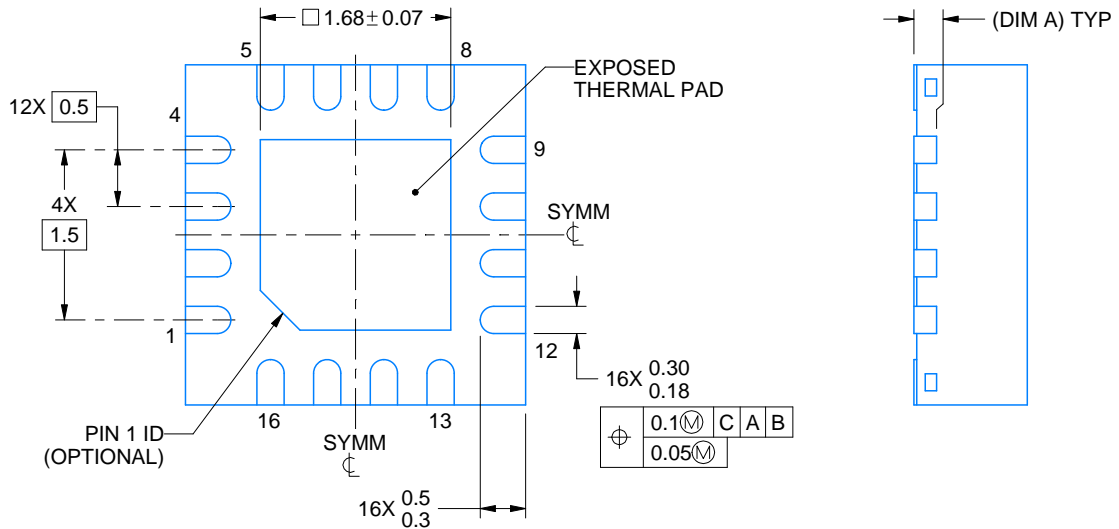
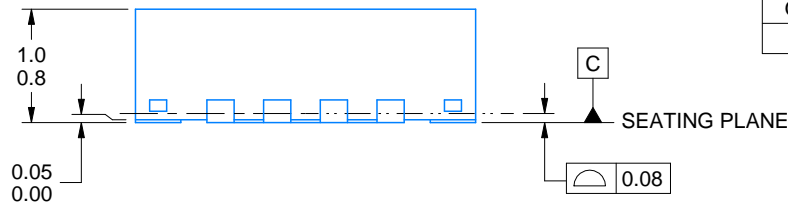


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203495/1



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



4222419/D 04/2022

NOTES:

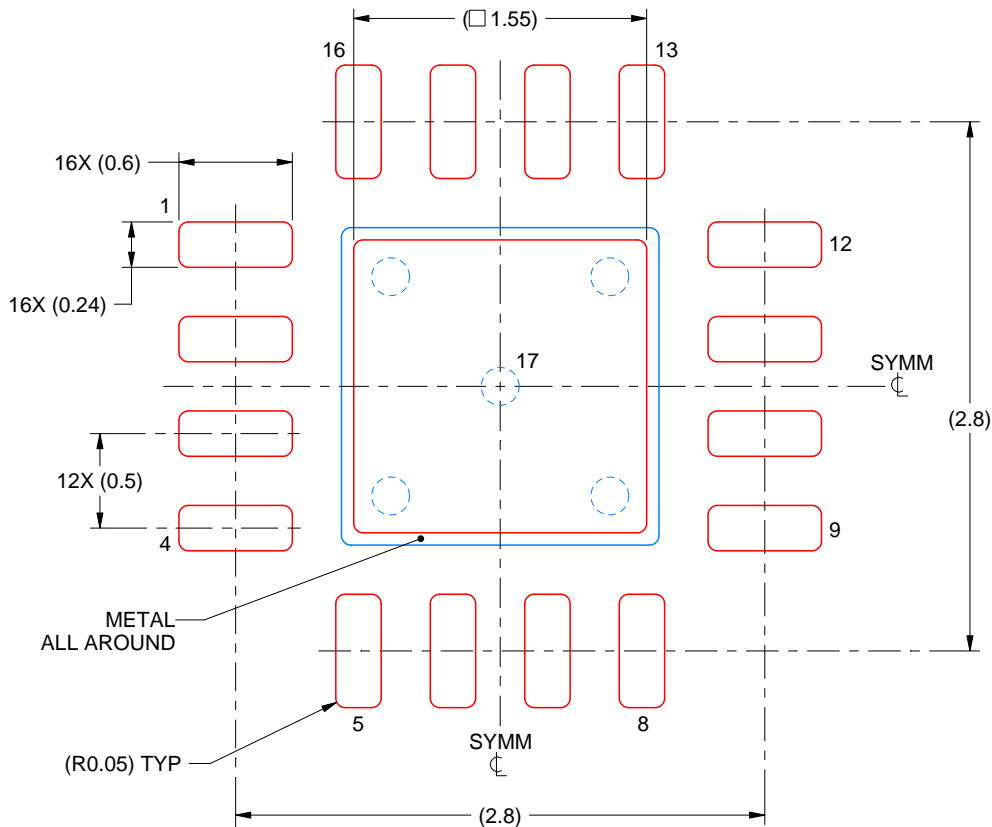
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE STENCIL DESIGN

RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/D 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2022，德州仪器 (TI) 公司