INA183 2.7-V to 26-V, High-Precision Current Sense Amplifier

1 Features

- Wide Common-Mode Range: 2.7 V to 26 V
- Offset Voltage: ±170 µV (Maximum) (Enables Shunt Drops of 10-mV Full-Scale)
- Accuracy:
  - Gain Error ±0.4% (Maximum Over Temperature):
  - 0.5-µV/°C Offset Drift (Maximum)
  - 10-ppm/°C Gain Drift (Maximum)
- Choice of Gains:
  - INA183A1: 50 V/V
  - INA183A2: 100 V/V
  - INA183A3: 200 V/V
- Quiescent Current: 130 µA (Maximum)
- Package: 5-Pin SOT-23

2 Applications

- Servers
- Power Supplies
- Battery Management
- Telecom Equipment

3 Description

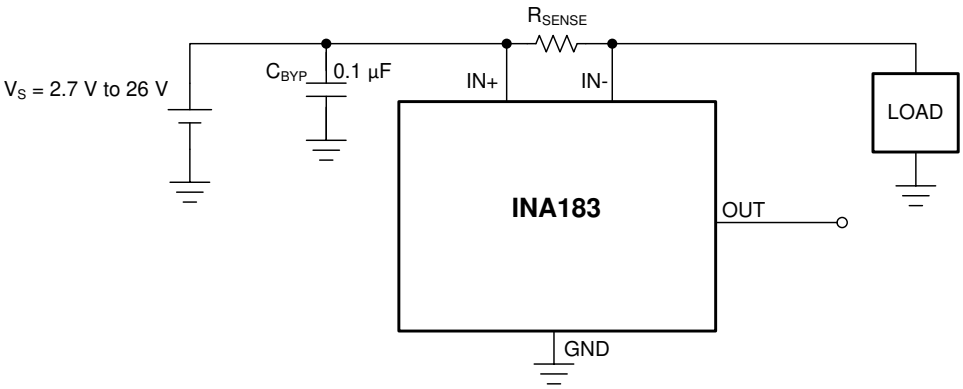
The INA183 is a high-precision voltage-output, current-shunt monitor (also called current-sense amplifier) commonly used for overcurrent protection, precision-current measurement for system optimization, or in closed-loop feedback circuits. This device can sense drops across shunt resistors at common-mode voltages from 2.7 V to 26 V. Three fixed gains are available: 50 V/V, 100 V/V, and 200 V/V. The low offset of the zero-drift architecture enables current sensing with maximum drops across the shunt as low as 10-mV full-scale.

This device operates by drawing power from the IN+ pin drawing a maximum of 130 µA of supply current. All versions are specified from –40 °C to 125 °C and are offered in the 5-pin SOT-23 package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA183	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	VERSION	NOTES
February 2021	*	Initial Release.

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5 Device Comparison

Table 5-1. Device Comparison

PRODUCT	GAIN
INA183A1	50
INA183A2	100
INA183A3	200

6 Pin Configuration and Functions

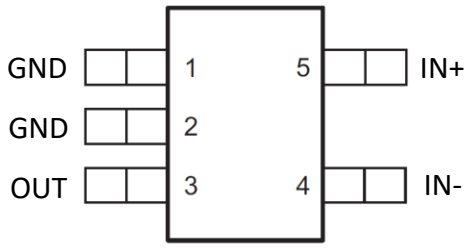


Figure 6-1. DBV Package 5-Pin SOT-23 Top View

Table 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	SOT-23		
GND	1, 2	Analog	Device ground. Both pins must be connected to ground.
IN–	4	Analog input	Connect to load side of shunt resistor.
IN+	5	Analog input	Connect to supply side of shunt resistor.
OUT	3	Analog output	Output voltage.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Analog inputs, , IN+, IN– (1)	Differential (V_{IN+}) – ($V_{IN–}$)	GND – 0.3	26	V
	Common-mode (2)	GND – 0.3	26	V
Output (2)		GND – 0.3	(IN+) + 0.3	V
Operating temperature		–55	150	°C
Junction temperature			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) V_{IN+} and $V_{IN–}$ are the voltages at the IN+ and IN– terminals, respectively.
(2) Input voltage at any terminal may exceed the voltage shown if the current at that terminal is limited to 5 mA.

7.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±3500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage range, voltage at IN+ pin	2.7	12	26	V
T_A	Operating free-air temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC (1)		INA183 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	164.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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7.5 Electrical Characteristics

at T_A = 25 °C, V_{SENSE} = V_{IN+} – $V_{IN–}$, and V_{IN+} = 12 V, unless otherwise noted.

PARAMETER			CONDITIONS	MIN	TYP	MAX	UNIT
INPUT							
V_{CM}	Common-mode input range		T_A = –40 °C to +125 °C	2.7		26	V
CMRR	Common-mode rejection ratio		V_{IN+} = 2.7 V to 26 V, V_{SENSE} = 10 mV, T_A = –40 °C to +125 °C	100	120		dB
V_{OS}	Offset voltage, RTI (1)		V_{CM} = 12 V		±25	±170	µV
dV_{OS}/dT	RTI vs temperature		T_A = –40 °C to +125 °C		0.1	0.5	µV/°C
I_{IB}	Input bias current (IB-)		V_{SENSE} = 0 mV		30	40	µA
OUTPUT							
G	Gain	A1 devices			50		V/V
		A2 devices			100		V/V
		A3 devices			200		V/V
E_G	Gain error		V_{OUT} = 0.5 V to V_{IN+} – 0.5 V, T_A = –40 °C to +125 °C		±0.1%	±0.4%	
	Gain error vs temperature		T_A = –40 °C to +125 °C		3	10	ppm/°C
	Nonlinearity error		V_{OUT} = 0.5 V to V_{IN+} – 0.5 V		±0.01%		
	Maximum capacitive load		No sustained oscillation		1		nF
VOLTAGE OUTPUT							
V_{SP}	Swing to IN+		R_L = 10 kΩ to GND, T_A = –40 °C to +125 °C		(V_{IN+}) – 0.05	(V_{IN+}) – 0.2	V
V_{SN}	Swing to GND		R_L = 10 kΩ to GND, V_{IN+} - V_{IN-} = -10 mV, T_A = –40 °C to +125 °C		(V_{GND}) + 0.005	(V_{GND}) + 0.05	V
FREQUENCY RESPONSE							
BW	Bandwidth	A1 devices	C_{LOAD} = 10 pF		80		kHz
		A2 devices	C_{LOAD} = 10 pF		30		kHz
		A3 devices	C_{LOAD} = 10 pF		14		kHz
SR	Slew rate				0.4		V/µs
NOISE, RTI (1)							
	Voltage noise density				25		nV/√Hz
POWER SUPPLY							
I_Q	Quiescent current, (IN+)		V_{SENSE} = 0 mV		83	130	µA
	I_Q over temperature		T_A = –40 °C to +125 °C			140	µA

(1) RTI = referred-to-input.

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7.6 Typical Characteristics

T_A = 25 °C, V_S = V_{IN+} = 12 V (unless otherwise noted)

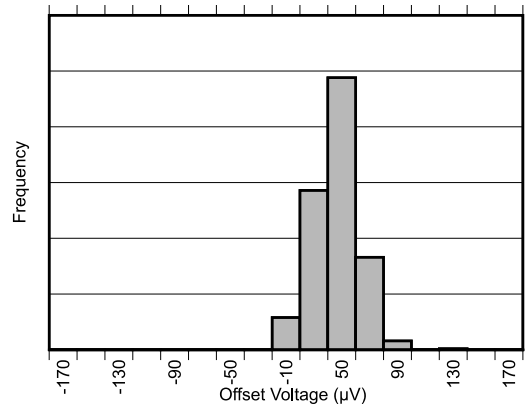


Figure 7-1. Input Offset Voltage Production Distribution

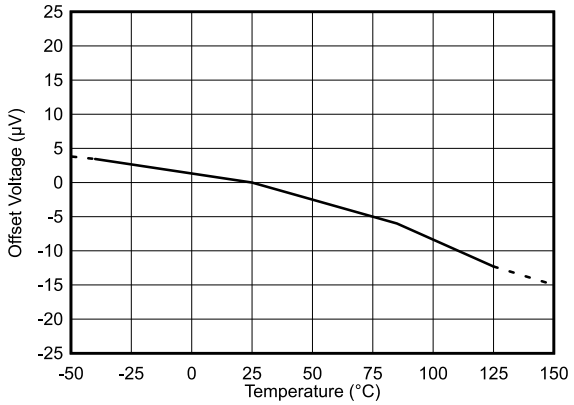


Figure 7-2. Offset Voltage vs. Temperature

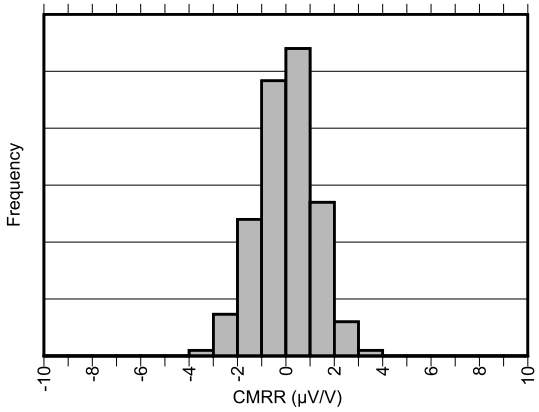


Figure 7-3. Common-Mode Rejection Production Distribution (A1 Devices)

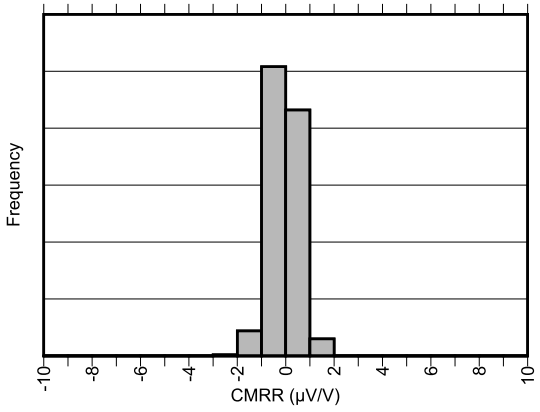


Figure 7-4. Common-Mode Rejection Production Distribution (A2 Devices)

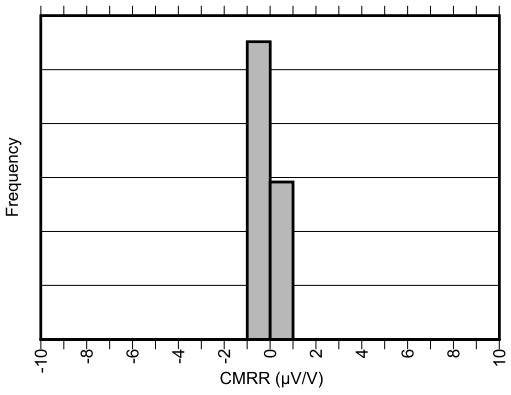


Figure 7-5. Common-Mode Rejection Production Distribution (A3 Devices)

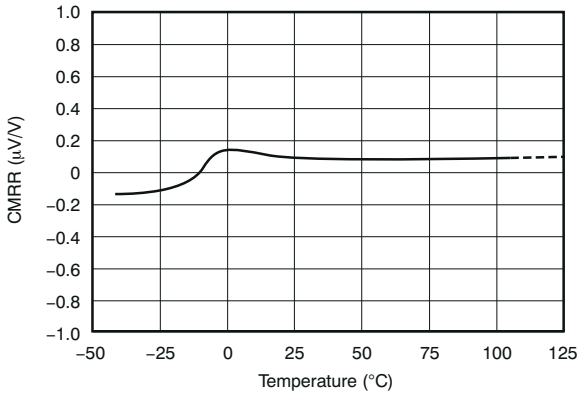


Figure 7-6. Common-Mode Rejection Ratio vs. Temperature

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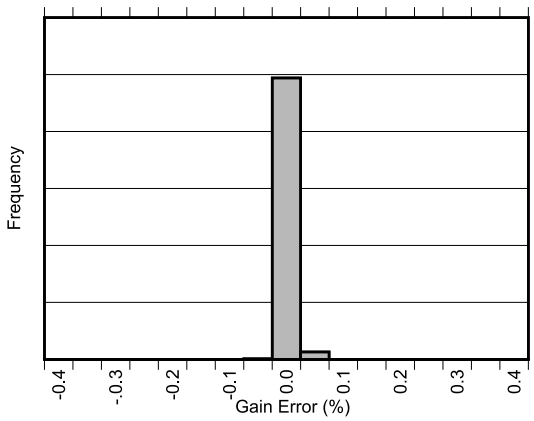


Figure 7-7. Gain Error Production Distribution (A1 Devices)

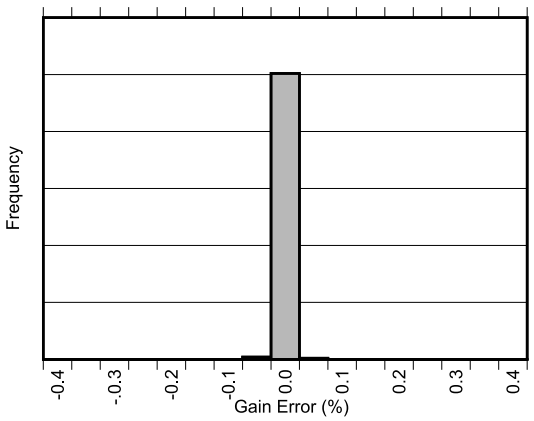


Figure 7-8. Gain Error Production Distribution (A2 Devices)

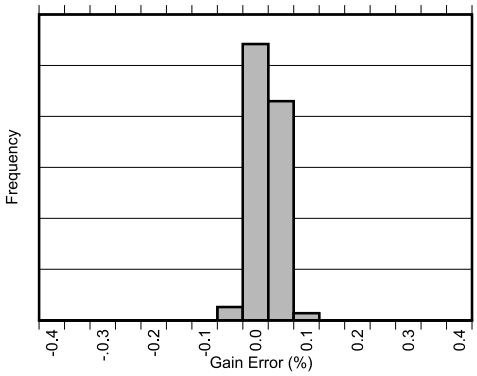


Figure 7-9. Gain Error Production Distribution (A3 Devices)

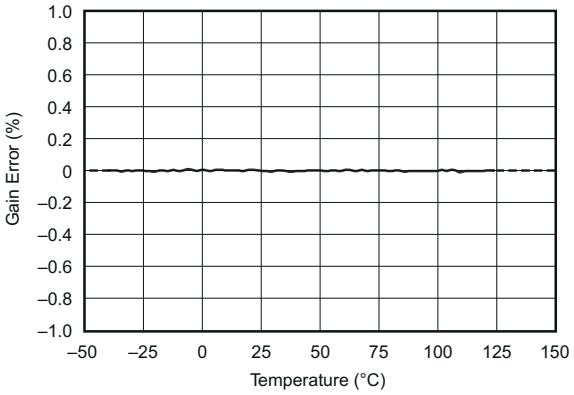


Figure 7-10. Gain Error vs. Temperature

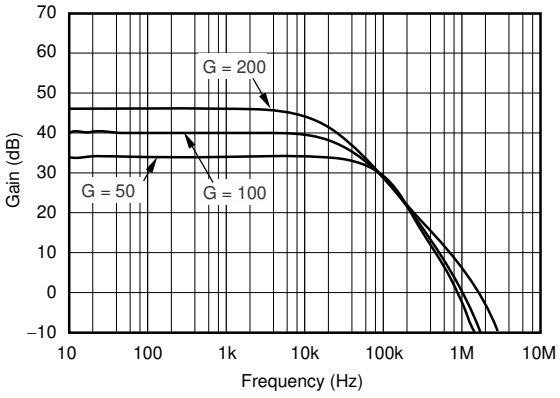


Figure 7-11. Gain vs. Frequency

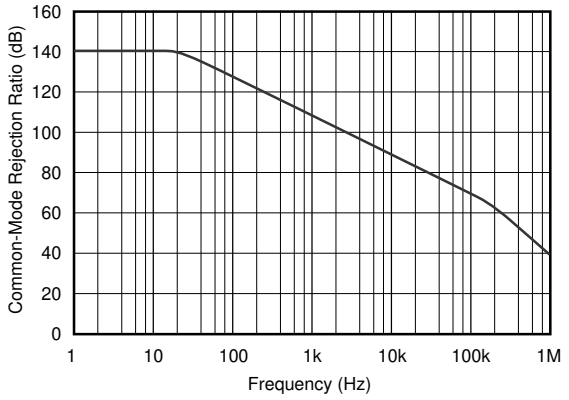


Figure 7-12. Common-Mode Rejection Ratio vs. Frequency

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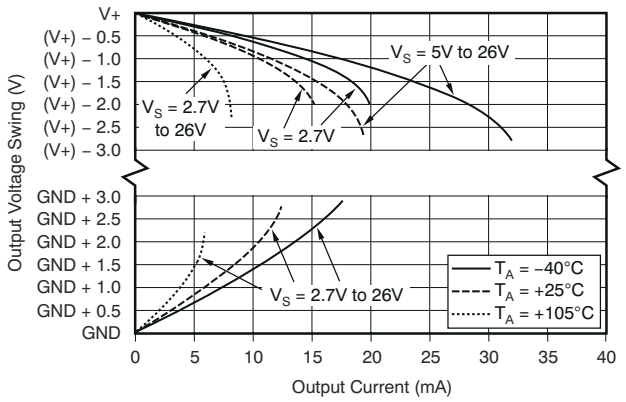


Figure 7-13. Output Voltage Swing vs. Output Current

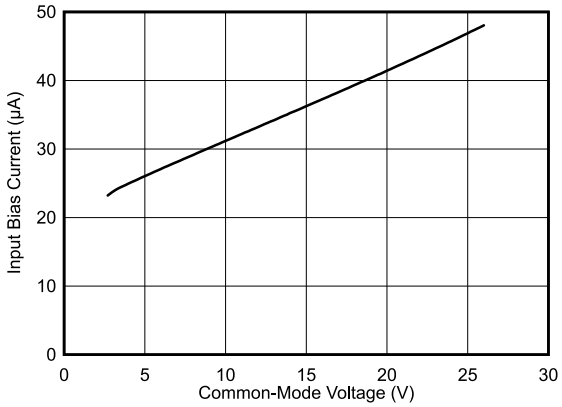


Figure 7-14. Input Bias Current vs. Common-Mode Voltage

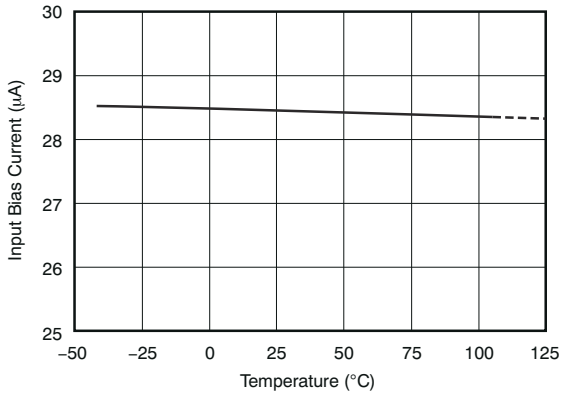


Figure 7-15. Input Bias Current vs. Temperature

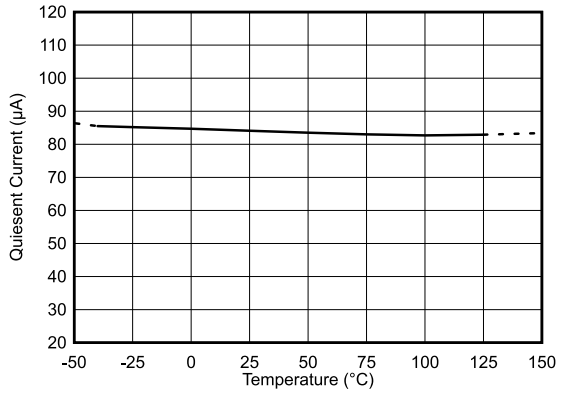


Figure 7-16. Quiescent Current vs. Temperature

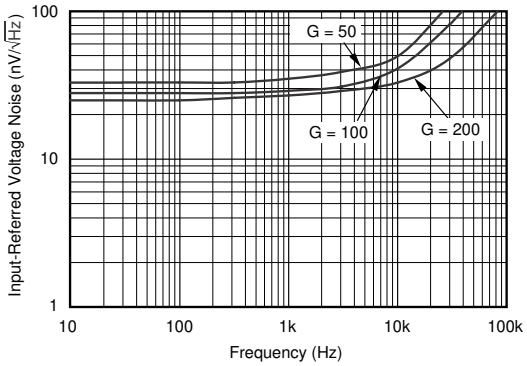


Figure 7-17. Input-Referred Voltage Noise vs. Frequency

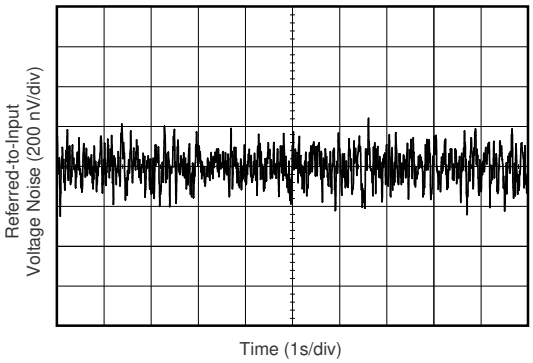


Figure 7-18. 0.1-Hz to 10-Hz Voltage Noise (Referred-to-Input)

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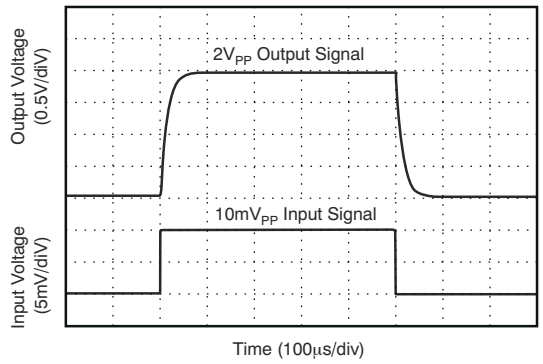


Figure 7-19. Step Response (10-mV_{PP} Input Step)

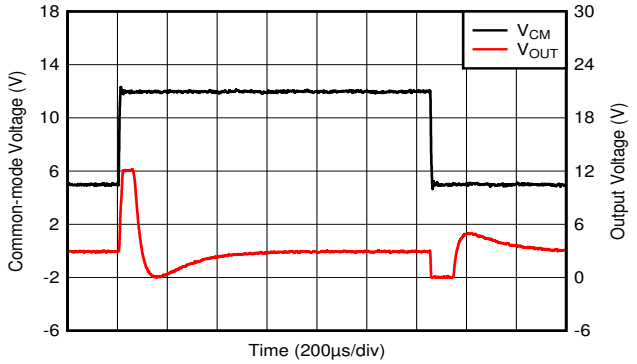


Figure 7-20. Common-Mode Voltage Transient Response

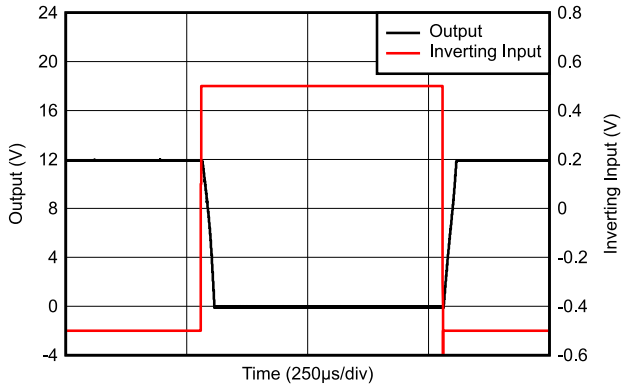
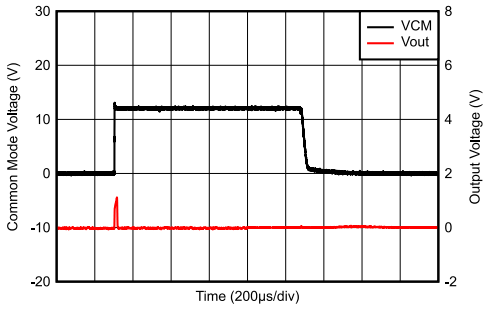


Figure 7-21. Inverting Differential Input Overload



V_{DIFF} = 0 V V_{CM} = 12-V Pulse

Figure 7-22. Start-Up Response

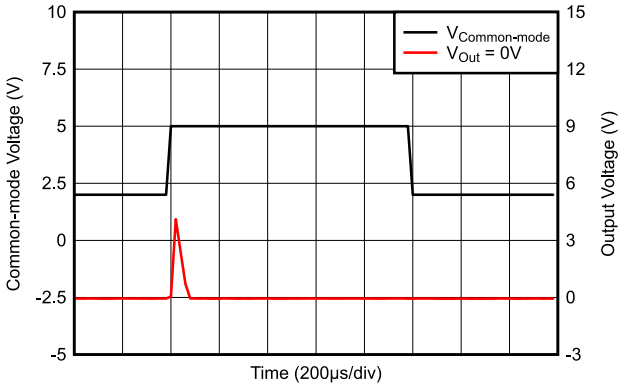


Figure 7-23. Brownout Recovery

8 Detailed Description

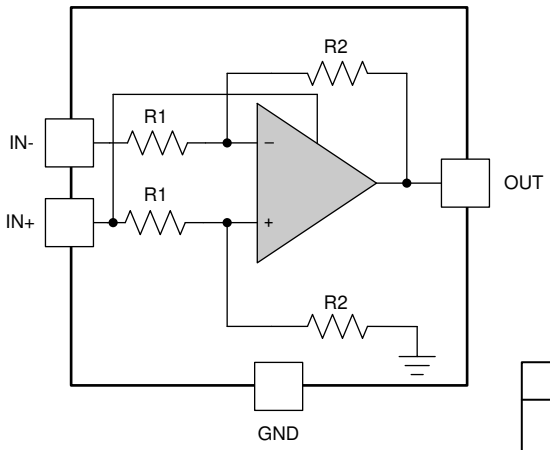
8.1 Overview

The INA183 is a 26-V common-mode, zero-drift topology, current-sensing amplifier meant for high-side, current-sensing applications. The device is a specially-designed, current-sensing amplifier that can accurately measure voltages developed across a current-sensing resistor. The device is capable of measuring current on input voltage rails as high as 26 V and as low as 2.7 V.

The zero-drift topology enables high-precision measurements with maximum input offset voltages as low as 170 µV with a maximum temperature contribution of 0.5 µV/°C over the full temperature range of –40 °C to +125 °C.

8.2 Functional Block Diagram

The simplified functional diagram below shows the device power is provided by the voltage on the IN+ pin. This diagram also shows the nominal values for the internal gain set resistors. The nominal value of these resistors can vary by 20% or more; however, the matching between these resistors is tightly controlled. The matching of these internal resistors results in a precise fixed gain that varies very little over temperature.



DEVICE	GAIN	R1	R2
INA183A1	50	20 kΩ	1 MΩ
INA183A2	100	10 kΩ	1 MΩ
INA183A3	200	5 kΩ	1 MΩ

8.3 Feature Description

8.3.1 Single-Supply Operation from IN+

The INA183 does not have a dedicated power-supply. Instead, an internal connection to the IN+ pin serves as the power supply for this device. This allows the device to be used in applications where lower voltage or sub-regulated supply rails are not present. The operational voltage range on this pin is 2.7 V to 26 V and is designed for power-supply applications. The maximum current drawn from the IN+ pin is 130 µA, when the current sense voltage is zero.

8.3.2 Low Gain Error and Offset Voltage

The maximum gain error of the INA183 is 0.4% and is specified over the full operational temperature range. The low gain error allows for accurate measurements as the sense voltage increases, and is designed for applications that need to detect overcurrent conditions accurately. The offset voltage of the INA183 is specified to be ±170 µV for all gain options. The low offset voltage allows for increased accuracy when the sense voltage is small or allows for reduction in the size of the current sense resistor with less impact on the total measurement accuracy. Smaller value resistors reduce the power loss in the application which allows the use of lower wattage resistors that are generally lower cost.

8.3.3 Low Drift Architecture

The INA183 features low drift for both the gain error and offset voltage specifications. The low gain error drift of 10 PPM/ºC results from the well matched internal resistor network that sets the device gain. The low offset drift

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is due to the internal chopping architecture of the amplifier. Input chopping reduces both the offset and offset drift since any change in offset is canceled with each chopping cycle. The maximum input offset drift of the INA183 is 0.5 µV/ºC. The low drift of the gain error and offset voltage provides accurate current measurement over the operational temperature range of -40ºC to 125ºC that exceeds the performance of most discrete current sensing implementations.

8.4 Device Functional Modes

8.4.1 Normal Operation

The INA183 is in normal operation when the following conditions are met:

- The voltage at the IN+ pin is between 2.7 V and 26 V.
- The maximum differential input signal times the gain is less than V_{IN+} minus the output voltage swing to V_{IN+}.
- The minimum differential input signal times the gain is greater than the swing to GND.

During normal operation, this device produces an output voltage that is the *amplified* representation of the difference voltage from IN+ to IN–.

8.4.2 Unidirectional, High-Side Operation

The INA183 measures the differential voltage developed by current flowing through a resistor that is commonly referred to as a current shunt resistor or current-sensing resistor. The INA183 operates in high-side, unidirectional mode only, meaning it only senses current sourced from a power supply to a system load as shown in Figure 8-1.

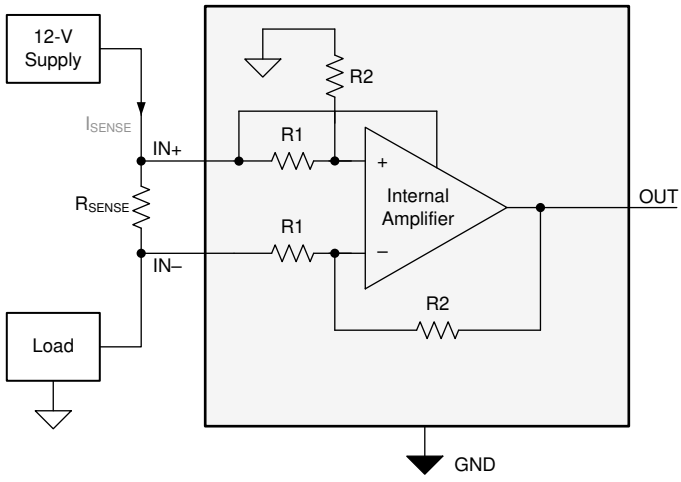


Figure 8-1. High-Side Unidirectional Application

8.4.3 Input Differential Overload

If the differential input voltage (V_{IN+} – $V_{IN–}$) times gain exceeds the voltage swing specification, the INA183 drives the output as close as possible to the IN+ pin or ground, and does not provide accurate measurement of the differential input voltage. If this input overload occurs during normal circuit operation, then reduce the value of the shunt resistor or use a lower-gain version with the chosen sense resistor to avoid this mode of operation. If a differential overload occurs in a fault event, then the output of the INA183 returns to the expected value approximately 30 µs after removal of the fault condition. When the input differential voltage is overloaded the bias currents will increase by a significant amount. The increase in bias currents will occur even with the device is powered down. Input differential overloads less than the absolute maximum voltage rating do not damage the device or result in an output inversion.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The INA183 measures the voltage developed across a current-sensing resistor when current passes through it. The ability to drive the reference pin to adjust the functionality of the output signal offers multiple configurations, as discussed throughout this section.

9.1.1 R_{SENSE} and Device Gain Selection

Choosing the largest possible shunt resistor will maximize the accuracy of any current-sense amplifier. A large sense resistor maximizes the differential input signal for a given amount of current flow and reduces the error contribution of the offset voltage. However, there are practical limits as to how large the current-sense resistor can be in a given application because of the resistor size and maximum allowable power dissipation. Equation 1 gives the maximum value for the current-sense resistor for a given power dissipation budget:

$$R_{SENSE} < \frac{PD_{MAX}}{I_{MAX}^2} \quad (1)$$

where:

- PD_{MAX} is the maximum allowable power dissipation in R_{SENSE}.
- I_{MAX} is the maximum current expected to flow through R_{SENSE}.

An additional limitation on the size of the current-sense resistor and device gain is due to the power-supply voltage at the IN+ pin, and device swing-to-rail limitations. To ensure that the current-sense signal is properly passed to the output, both positive and negative output swing limitations must be examined. Equation 2 provides the maximum values of R_{SENSE} and GAIN to keep the device from exceeding the positive swing limitation.

$$I_{MAX} \times R_{SENSE} \times GAIN < V_{SP} \quad (2)$$

where:

- I_{MAX} is the maximum current that will flow through R_{SENSE}.
- GAIN is the gain of the current-sense amplifier.
- V_{SP} is the positive output swing as specified in the data sheet.

Positive output swing limitations should be considered when selecting the value of R_{SENSE}. There is always a trade-off between the value of the sense resistor and the gain of the device under consideration. If the sense resistor selected for the maximum power dissipation is too large, then it is possible to select a lower-gain device to avoid positive swing limitations.

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The negative swing specification limits how small the sense resistor value can be for a given application. Equation 3 provides the limit on the minimum value of the sense resistor.

$$I_{MIN} \times R_{SENSE} \times GAIN > V_{SN} \quad (3)$$

where:

- I_{MIN} is the minimum current that will flow through R_{SENSE}.
- GAIN is the gain of the current-sense amplifier.
- V_{SN} is the negative output swing of the device.

9.2 Typical Application

Figure 9-1 shows the basic connections for the INA183. The input pins, IN+ and IN–, must be connected as close as possible to the shunt resistor to minimize any resistance in series with the shunt resistor.

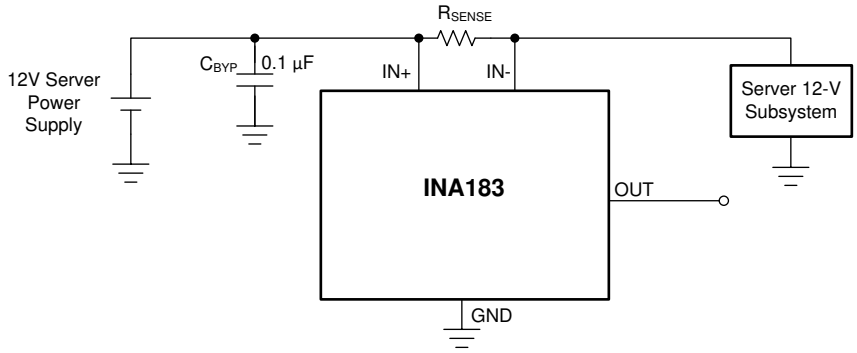


Figure 9-1. Typical Server Application

A power-supply bypass capacitor is required on the IN+ pin. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

In server applications, the INA183 typically monitors the current on the 12-V bus that is distributed to various server sub-systems like memory, storage, or CPU power. The monitored current can be used by the server for fault detection or sub-system power optimization.

9.2.1 Design Requirements

Table 9-1 lists the design setup for this application.

Table 9-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
High-side supply voltage (V_{IN+})	12 V
Maximum sense current (I_{MAX})	5 A
Gain option	50 V/V

9.2.2 Detailed Design Procedure

The maximum value of the current-sense resistor is calculated based on choice of gain, the value of the maximum current the be sensed (I_{MAX}), and the power-supply voltage (V_{IN+}). When operating at the maximum current, the output voltage must not exceed the positive output swing specification, V_{SP}. Under the given design parameters, Equation 4 calculates the maximum value for R_{SENSE} as 47.2 mΩ.

$$R_{SENSE} < \frac{V_{SP}}{I_{MAX} \times GAIN} \quad (4)$$

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For this design example, a value of 40.2 mΩ is selected because, while the 40.2 mΩ is less than the maximum value calculated, 40.2 mΩ is still large enough to give an adequate signal at the current-sense amplifier output. To reduce resistor power losses or to operate over a reduced output range, smaller value resistors can be used as the expense of dynamic range and low current accuracy.

9.2.3 Application Curve

Figure 9-2 shows the output response of the device to a sinusoidal current.

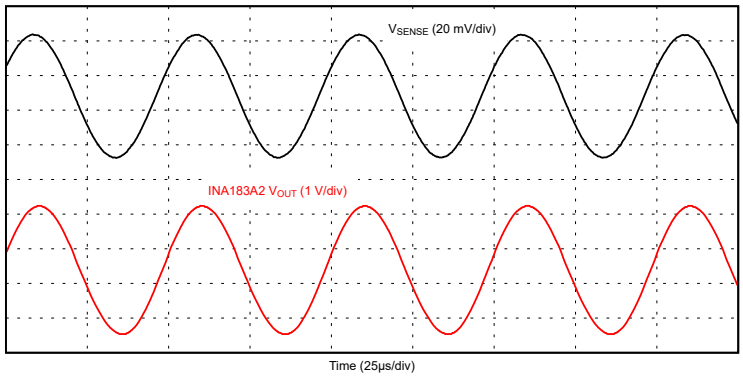


Figure 9-2. INA183 Output Response

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10 Power Supply Recommendations

The device is powered from the IN+ pin with a voltage from 2.7 V to 26 V. The voltage at the output will also be limited by this voltage during overload or fault conditions. Also, the INA183 can withstand the full input signal range up to 26 V on the IN– pin, regardless of whether the device has power applied or not.

11 Layout

11.1 Layout Guidelines

- Connect the input pins to the sensing resistor using a kelvin or 4-wire connection. This connection technique ensures that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.
- Place the power-supply bypass capacitor as close as possible to the IN+ pin and ground pins. TI recommends using a bypass capacitor with a value of 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

11.2 Layout Example

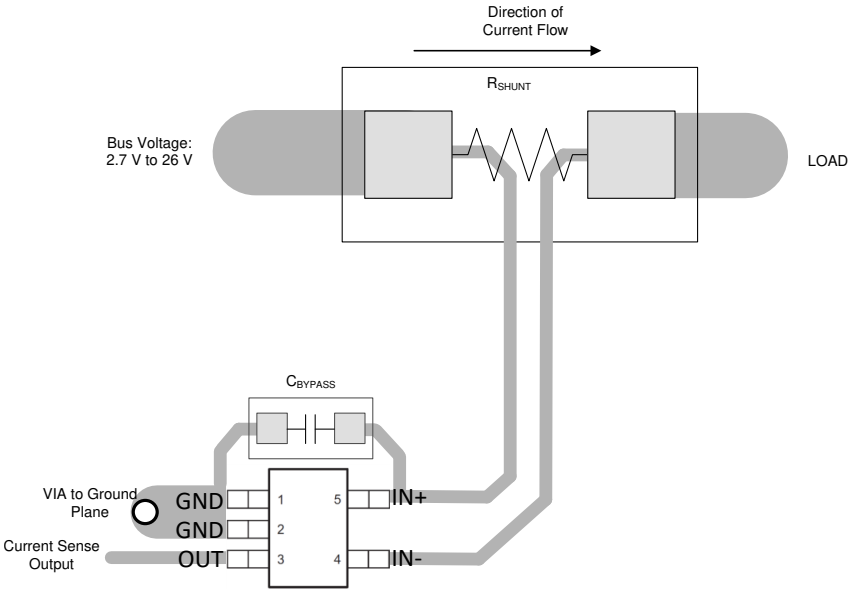


Figure 11-1. Recommended Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *INA183A1-A3EVM User's Guide*
- *TIDA-00302 Transient Robustness for Current Shunt Monitor*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

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All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA183A1IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2BRQ	Samples
INA183A1IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2BRQ	Samples
INA183A2IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2BSQ	Samples
INA183A2IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2BSQ	Samples
INA183A3IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2BTQ	Samples
INA183A3IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2BTQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

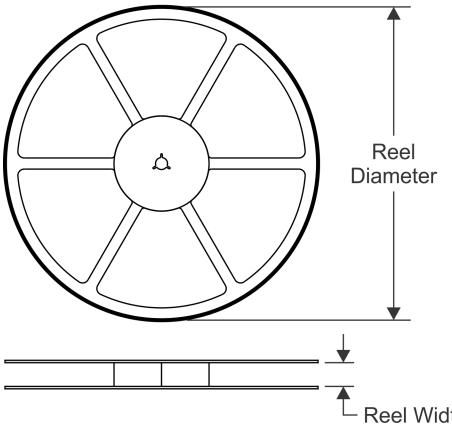
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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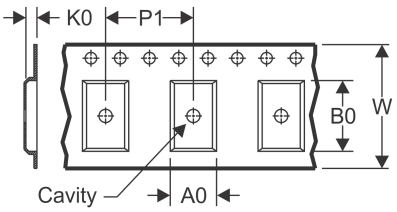
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

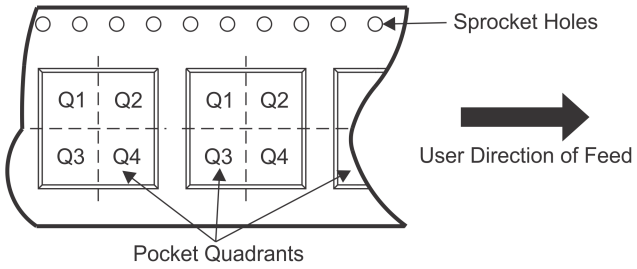


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

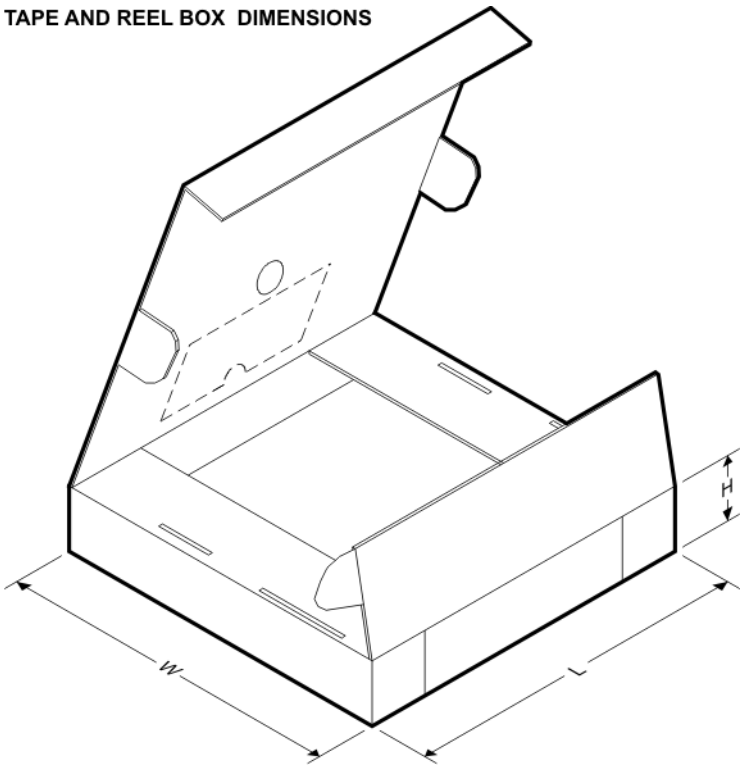
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA183A1IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
INA183A1IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
INA183A2IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
INA183A2IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
INA183A3IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
INA183A3IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

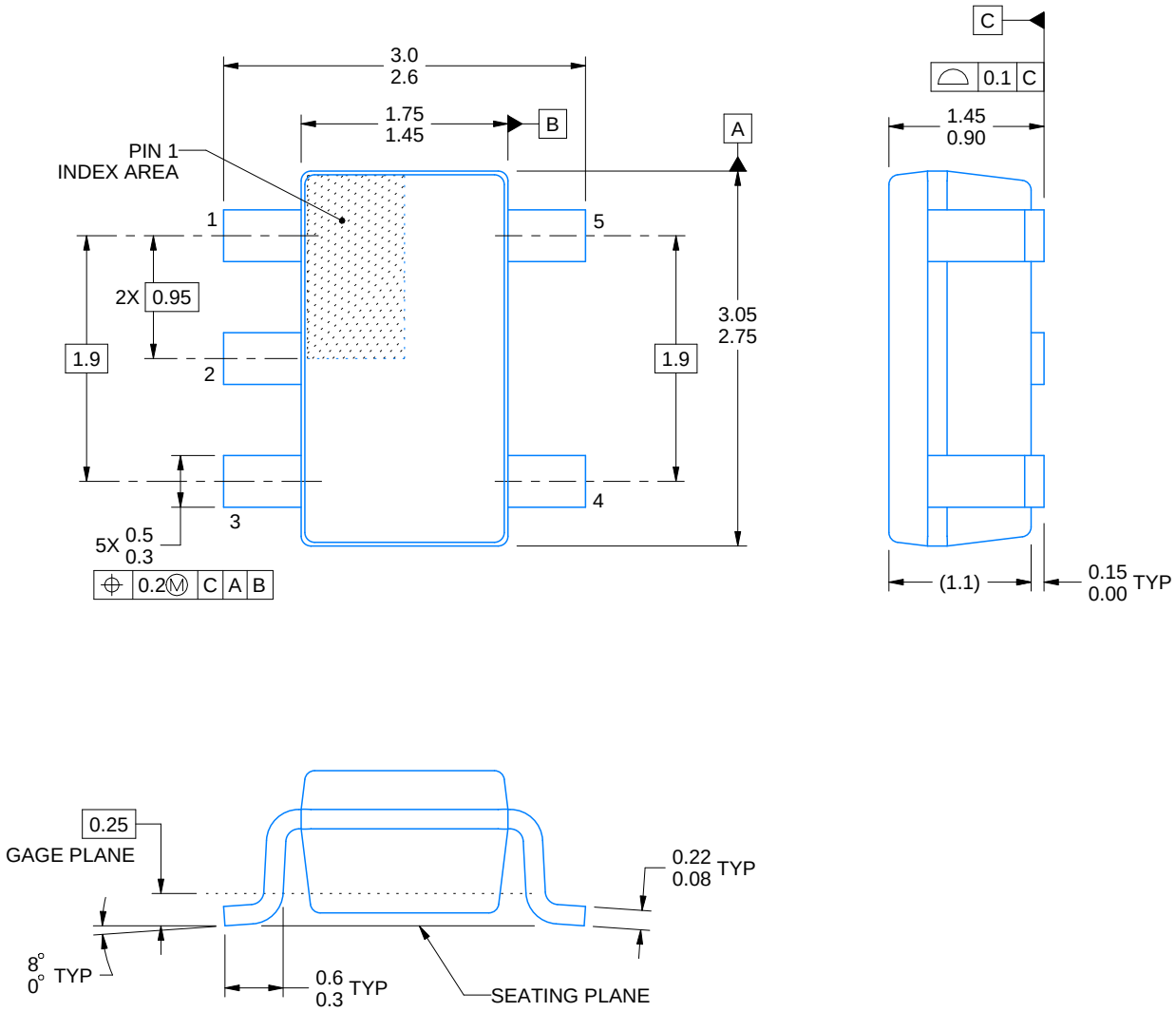
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA183A1IDBVR	SOT-23	DBV	5	3000	190.0	190.0	30.0
INA183A1IDBVT	SOT-23	DBV	5	250	190.0	190.0	30.0
INA183A2IDBVR	SOT-23	DBV	5	3000	190.0	190.0	30.0
INA183A2IDBVT	SOT-23	DBV	5	250	190.0	190.0	30.0
INA183A3IDBVR	SOT-23	DBV	5	3000	190.0	190.0	30.0
INA183A3IDBVT	SOT-23	DBV	5	250	190.0	190.0	30.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

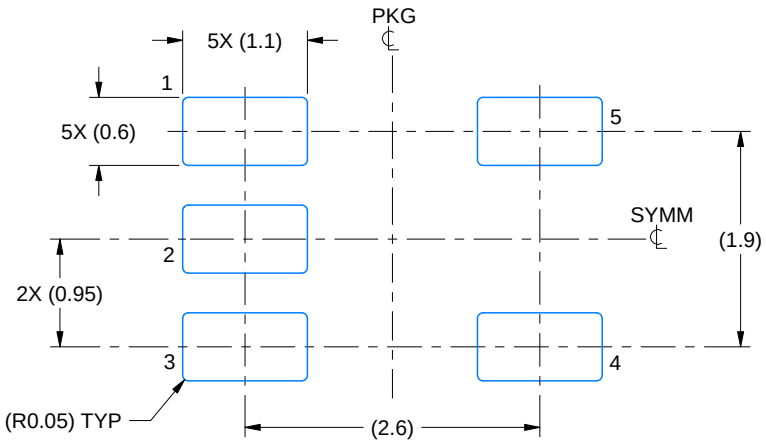
SMALL OUTLINE TRANSISTOR



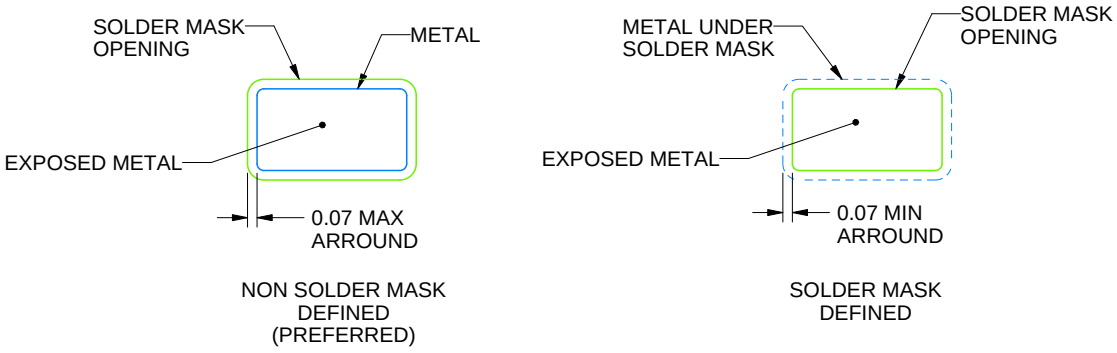
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

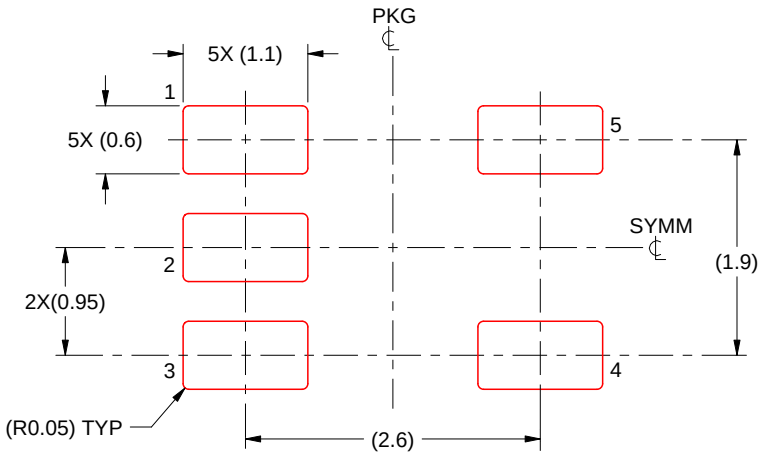


SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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