

# INA118 低功耗精密仪表放大器

此器件的新版本现已上市: [INA818](#)

## 1 特性

- 此器件的新版本现已上市: [INA818](#)
- 低失调电压: 50 $\mu$ V, 最大值
- 低温漂: 0.5 $\mu$ V/ $^{\circ}$ C, 最大值
- 低输入偏置电流: 5nA, 最大值
- 高 CMR: 110dB, 最小值
- 输入保护电压可达  $\pm$ 40V
- 宽电源电压范围:  $\pm$ 1.35V 至  $\pm$ 18V
- 低静态电流: 350 $\mu$ A
- 封装: 8 引脚塑料 DIP, SO-8

## 2 应用

- 桥接放大器
- 热电偶放大器
- RTD 传感器放大器
- 医疗仪器
- 数据采集

## 3 说明

INA118 是一款低功耗通用仪表放大器, 可提供出色的准确性。此器件采用多功能三级运算放大器设计, 尺寸小巧, 适用于多种应用。即使在高增益 ( $G = 100$  时为 70kHz) 情况下, 电流反馈输入电路也可提供宽带宽。

可通过单个外部电阻器在 1 到 10000 范围内设置增益。内部输入保护可经受高达  $\pm$ 40V 的电压且无损坏。

INA118 经过激光修整, 具有低失调电压 (50 $\mu$ V)、低温漂 (0.5 $\mu$ V/ $^{\circ}$ C) 和高共模抑制 ( $G = 1000$  时为 110dB)。INA118 采用低至  $\pm$ 1.35V 的电源电压, 静态电流仅 350 $\mu$ A, 因此非常适合电池供电系统。

INA118 采用 8 引脚塑料 DIP 和 SO-8 表面贴装式封装, 其额定温度范围为  $-40^{\circ}$ C 至  $+85^{\circ}$ C。

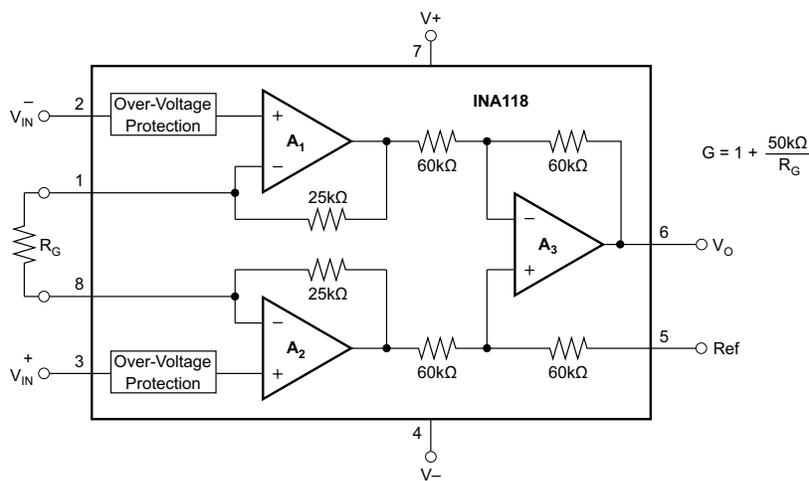
升级后的 [INA818](#) 在相同的静态电流下可提供更低的输入级失调电压 (最大值 35 $\mu$ V)、更低的输入偏置电流 (最大值 0.5nA) 和更低的噪声 (8nV/ $\sqrt{\text{Hz}}$ )。请参阅 [器件比较表](#), 以了解德州仪器 (TI) 提供的精密仪表放大器精选产品。

器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
INA118	SOIC (8)	3.91mm $\times$ 4.90mm
	PDIP (8)	6.35mm $\times$ 9.81mm

(1) 要了解所有可用封装, 请参见数据表末尾的封装选项附录。

简化原理图



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## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (January 2016) to Revision B	Page
• 已添加 添加了关于升级后的新版本 INA818 的信息 .....	1
• Added <i>Device Comparison Table</i> .....	3

Changes from Original (September 2000) to Revision A	Page
• 添加了 <i>ESD 额定值表</i> 、 <i>特性说明</i> 部分、 <i>器件功能模式</i> 部分、 <i>应用和实施</i> 部分、 <i>电源相关建议</i> 部分、 <i>布局</i> 部分、 <i>器件和文档支持</i> 部分以及 <i>机械、封装和可订购信息</i> 部分 .....	1

## 5 Device Comparison Table

DEVICE	DESCRIPTION	GAIN EQUATION	RG PINS AT PIN
INA818	35- $\mu$ V Offset, 0.4 $\mu$ V/ $^{\circ}$ C $V_{OS}$ Drift, 8-nV/ $\sqrt{\text{Hz}}$ Noise, Low-Power, Precision Instrumentation Amplifier	$G = 1 + 50 \text{ k}\Omega / R_G$	1, 8
INA819	35- $\mu$ V Offset, 0.4 $\mu$ V/ $^{\circ}$ C $V_{OS}$ Drift, 8-nV/ $\sqrt{\text{Hz}}$ Noise, Low-Power, Precision Instrumentation Amplifier	$G = 1 + 50 \text{ k}\Omega / R_G$	2, 3
INA821	35- $\mu$ V Offset, 0.4 $\mu$ V/ $^{\circ}$ C $V_{OS}$ Drift, 7-nV/ $\sqrt{\text{Hz}}$ Noise, High-Bandwidth, Precision Instrumentation Amplifier	$G = 1 + 49.4 \text{ k}\Omega / R_G$	2, 3
INA828	50- $\mu$ V Offset, 0.5 $\mu$ V/ $^{\circ}$ C $V_{OS}$ Drift, 7-nV/ $\sqrt{\text{Hz}}$ Noise, Low-Power, Precision Instrumentation Amplifier	$G = 1 + 50 \text{ k}\Omega / R_G$	1, 8
INA333	25- $\mu$ V $V_{OS}$ , 0.1 $\mu$ V/ $^{\circ}$ C $V_{OS}$ Drift, 1.8-V to 5-V, RRO, 50- $\mu$ A $I_Q$ , chopper-stabilized INA	$G = 1 + 100 \text{ k}\Omega / R_G$	1, 8
PGA280	20-mV to $\pm 10$ -V Programmable Gain IA With 3-V or 5-V Differential Output; Analog Supply up to $\pm 18$ V	Digital programmable	N/A
INA159	$G = 0.2$ V Differential Amplifier for $\pm 10$ -V to 3-V and 5-V Conversion	$G = 0.2 \text{ V/V}$	N/A
PGA112	Precision Programmable Gain Op Amp With SPI	Digital programmable	N/A

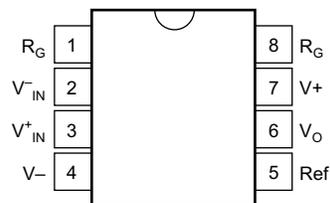
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**6 Pin Configuration and Functions**

**P and D Packages  
8-Pin PDIP and SOIC  
Top View**

**Pin Functions**

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$R_G$	—	Gain setting pin. For gains greater than 1, place a gain resistor between pin 1 and pin 8.
2	$V^-_{IN}$	I	Negative input
3	$V^+_{IN}$	I	Positive input
4	$V^-$	—	Negative supply
5	Ref	I	Reference input. This pin must be driven by low impedance or connected to ground.
6	$V_O$	O	Output
7	$V^+$	—	Positive supply
8	$R_G$	—	Gain setting pin. For gains greater than 1, place a gain resistor between pin 1 and pin 8.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
	Supply voltage		±18	V
	Analog input voltage		±40	V
	Output short-circuit (to ground)	Continuous		
	Operating temperature	–40	125	°C
	Junction temperature		150	°C
	Lead temperature (soldering, 10 s)		300	°C
T <sub>stg</sub>	Storage temperature	–40	125	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V	Power supply	±2.25	±15	±18	V
V <sub>O</sub> = 0	Input common-mode voltage	V <sup>–</sup> + 1.1		V <sup>+</sup> – 1	V
T <sub>A</sub>	Ambient temperature	–55		150	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		INA118		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	115	48	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	62	37	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	59	25	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	14	14	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	58	25	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

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**7.5 Electrical Characteristics**at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , and  $R_L = 10\text{ k}\Omega$  (unless otherwise noted\_

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>INPUT</b>							
Offset voltage, RTI	Initial	$T_A = 25^\circ\text{C}$	INA118PB, UB INA118P, U	$\pm 10 \pm 50/\text{G}$ $\pm 25 \pm 100/\text{G}$	$\pm 50 \pm 500/\text{G}$ $\pm 125 \pm 1000/\text{G}$		$\mu\text{V}$
	vs Temperature	$T_A = T_{\text{MIN}}$ to $T_{\text{MAX}}$	INA118PB, UB INA118P, U	$\pm 0.2 \pm 2/\text{G}$ $\pm 0.2 \pm 5/\text{G}$	$\pm 0.5 \pm 20/\text{G}$ $\pm 1 \pm 20/\text{G}$		$\mu\text{V}/^\circ\text{C}$
	vs Power supply	$V_S = \pm 1.35\text{ V}$ to $\pm 18\text{ V}$	INA118PB, UB INA118P, U	$\pm 1 \pm 10/\text{G}$ $\pm 1 \pm 10/\text{G}$	$\pm 5 \pm 100/\text{G}$ $\pm 10 \pm 100/\text{G}$		$\mu\text{V}/\text{V}$
	Long-term stability			$\pm 0.4 \pm 5/\text{G}$			$\mu\text{V}/\text{mo}$
	Impedance	Differential			$10^{10} \parallel 1$		
Common-mode				$10^{10} \parallel 4$			
Linear input voltage range				$(V^+) - 1$ $(V^-) + 1.1$	$(V^+) - 0.65$ $(V^-) + 0.95$		V
Safe input voltage						$\pm 40$	V
Common-mode rejection	$V_{\text{CM}} = \pm 10\text{ V}$ , $\Delta R_S = 1\text{ k}\Omega$ , $G = 1$		INA118PB, UB	80	90	dB	
			INA118P, U	73	90		
	$V_{\text{CM}} = \pm 10\text{ V}$ , $\Delta R_S = 1\text{ k}\Omega$ , $G = 10$		INA118PB, UB	97	110		
			INA118P, U	89	110		
	$V_{\text{CM}} = \pm 10\text{ V}$ , $\Delta R_S = 1\text{ k}\Omega$ , $G = 100$		INA118PB, UB	107	120		
			INA118P, U	98	120		
	$V_{\text{CM}} = \pm 10\text{ V}$ , $\Delta R_S = 1\text{ k}\Omega$ , $G = 1000$		INA118PB, UB	110	125		
			INA118P, U	100	125		
Bias current			INA118PB, UB	$\pm 1$	$\pm 5$	nA	
			INA118P, U	$\pm 1$	$\pm 10$		
vs Temperature				$\pm 40$		$\text{pA}/^\circ\text{C}$	
Offset current			INA118PB, UB	$\pm 1$	$\pm 5$	nA	
			INA118P, U	$\pm 1$	$\pm 10$		
vs Temperature				$\pm 40$		$\text{pA}/^\circ\text{C}$	
Noise voltage, RTI	f = 10 Hz	$G = 1000$ , $R_S = 0\ \Omega$		11		$\text{nV}/\sqrt{\text{Hz}}$	
	f = 100 Hz			10		$\text{nV}/\sqrt{\text{Hz}}$	
	f = 1 kHz			10		$\text{nV}/\sqrt{\text{Hz}}$	
	$f_B = 0.1\text{ Hz}$ to $10\text{ Hz}$			0.28		$\mu\text{Vp-p}$	
Noise current	f = 10 Hz			2		$\text{pA}/\sqrt{\text{Hz}}$	
	f = 1 kHz			0.3			
	$f_B = 0.1\text{ Hz}$ to $10\text{ Hz}$			80		$\text{pAp-p}$	
<b>GAIN</b>							
Gain equation				$1 + (50\text{ k}\Omega/R_G)$			V/V
Range of gain				1		10000	V/V
Gain error	$G = 1$			$\pm 0.01\%$		$\pm 0.024\%$	
	$G = 10$			$\pm 0.02\%$		$\pm 0.4\%$	
	$G = 100$			$\pm 0.05\%$		$\pm 0.5\%$	
	$G = 1000$			$\pm 0.5\%$		$\pm 1\%$	
Gain vs temperature		$G = 1$		$\pm 1$		$\pm 10$	$\text{ppm}/^\circ\text{C}$
50-k $\Omega$ resistance <sup>(1)</sup>				$\pm 25$		$\pm 100$	$\text{ppm}/^\circ\text{C}$
Nonlinearity	$G = 1$			$\pm 0.0003$		$\pm 0.001$	% of FSR
	$G = 10$			$\pm 0.0005$		$\pm 0.002$	
	$G = 100$			$\pm 0.0005$		$\pm 0.002$	
	$G = 1000$			$\pm 0.002$		$\pm 0.01$	

(1) Temperature coefficient of the 50-k $\Omega$  term in the gain equation.

## Electrical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , and  $R_L = 10\text{ k}\Omega$  (unless otherwise noted\_

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OUTPUT</b>						
Voltage:	Positive	$R_L = 10\text{ k}\Omega$	$(V^+) - 1$	$(V^+) - 0.8$		V
	Negative		$(V^-) + 0.35$	$(V^-) + 0.2$		
	Single supply high	$V_S = 2.7\text{ V}/0\text{ V}^{(2)}$ , $R_L = 10\text{ k}\Omega$	1.8	2		mV
	Single supply low		60	35		
Load capacitance stability				1000		pF
Short circuit current				+5/-12		mA
<b>FREQUENCY RESPONSE</b>						
Bandwidth, -3 dB	G = 1		800		kHz	
	G = 10		500			
	G = 100		70			
	G = 1000		7			
Slew rate		$V_O = \pm 10\text{ V}$ , G = 10		0.9		V/ $\mu\text{s}$
Settling time, 0.01%	G = 1		15		$\mu\text{s}$	
	G = 10		15			
	G = 100		21			
	G = 1000		210			
Overload recovery		50% Overdrive		20		$\mu\text{s}$
<b>POWER SUPPLY</b>						
Voltage range			$\pm 1.35$	$\pm 15$	$\pm 18$	V
Current		$V_{IN} = 0\text{ V}$		$\pm 350$	$\pm 385$	$\mu\text{A}$
<b>TEMPERATURE RANGE</b>						
Specification			-40		85	$^\circ\text{C}$
Operating			-40		125	$^\circ\text{C}$

(2) Common-mode input voltage range is limited. See text for discussion of low power supply and single power supply operation.

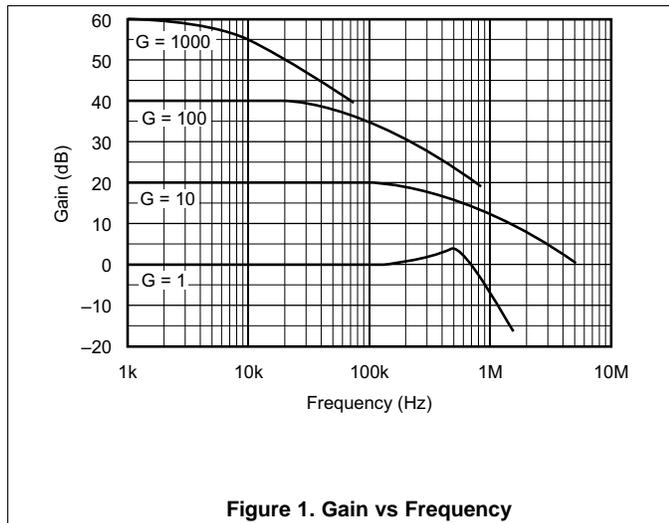
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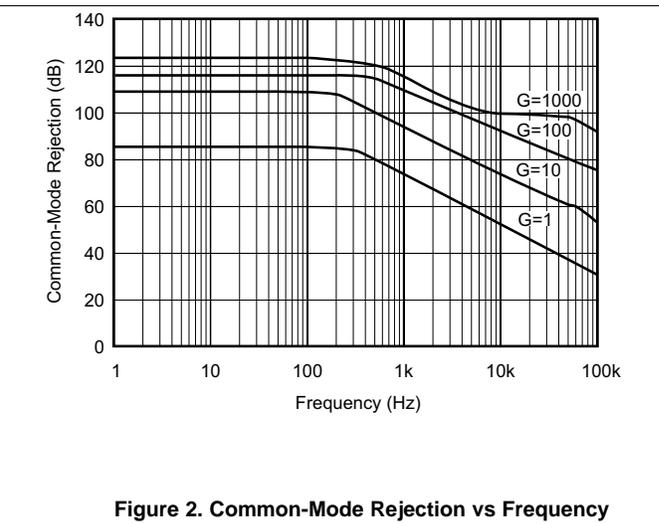
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**7.6 Typical Characteristics**

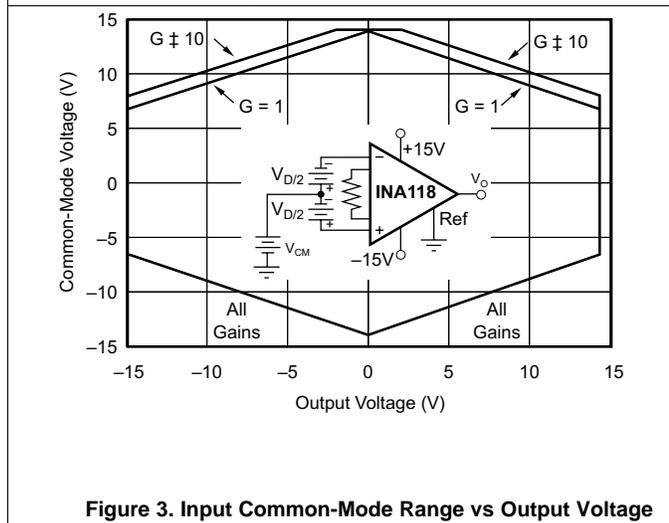
at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$  (unless otherwise noted)



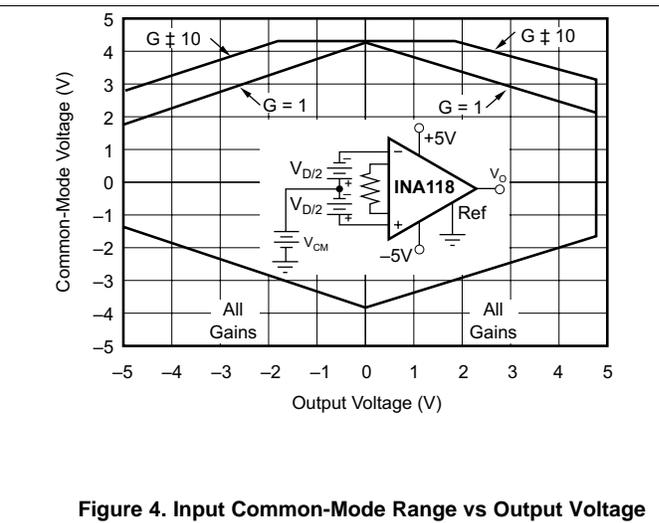
**Figure 1. Gain vs Frequency**



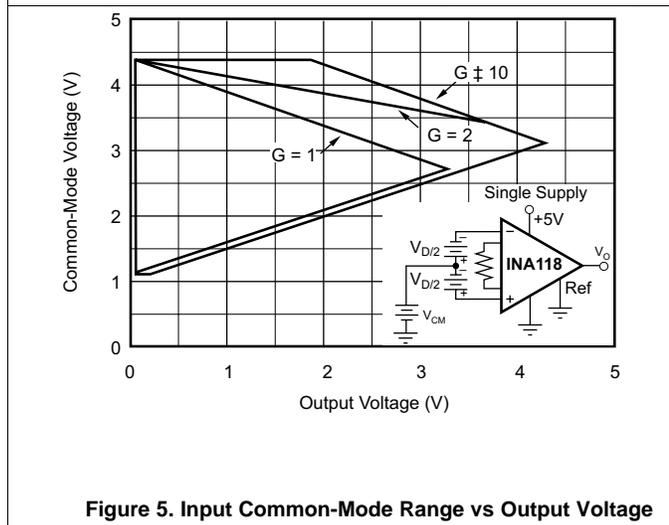
**Figure 2. Common-Mode Rejection vs Frequency**



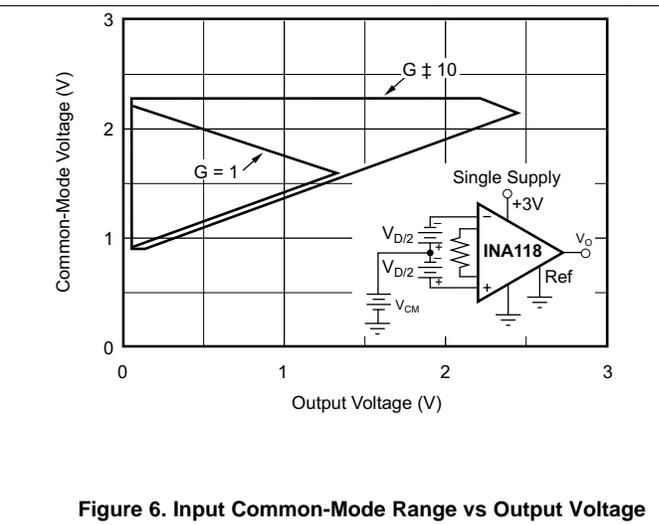
**Figure 3. Input Common-Mode Range vs Output Voltage**



**Figure 4. Input Common-Mode Range vs Output Voltage**



**Figure 5. Input Common-Mode Range vs Output Voltage**



**Figure 6. Input Common-Mode Range vs Output Voltage**

Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$  (unless otherwise noted)

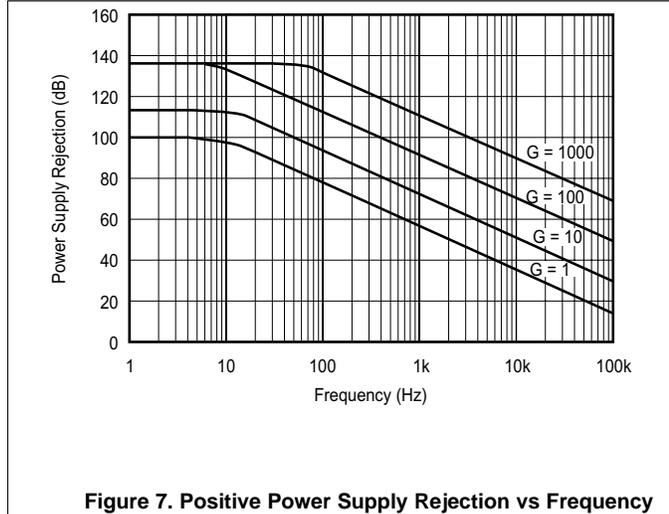


Figure 7. Positive Power Supply Rejection vs Frequency

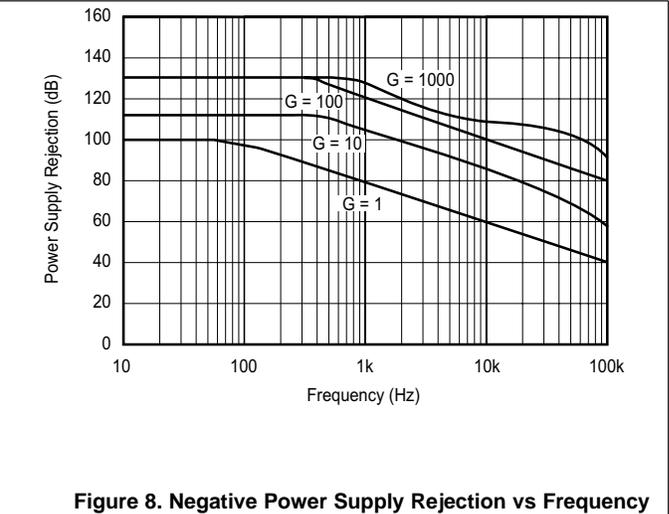


Figure 8. Negative Power Supply Rejection vs Frequency

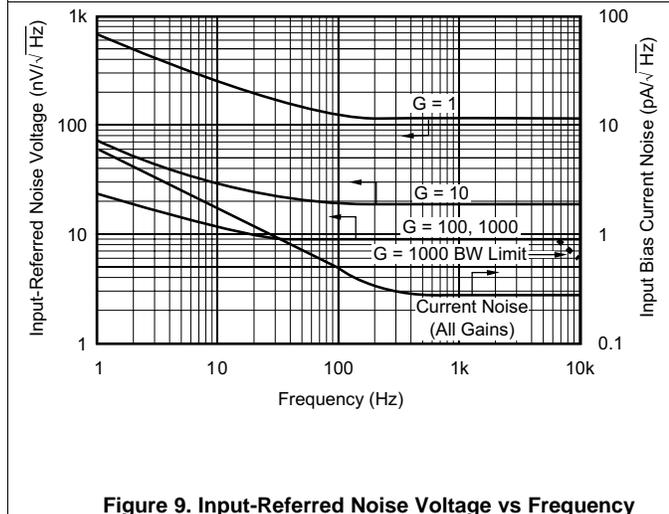


Figure 9. Input-Referred Noise Voltage vs Frequency

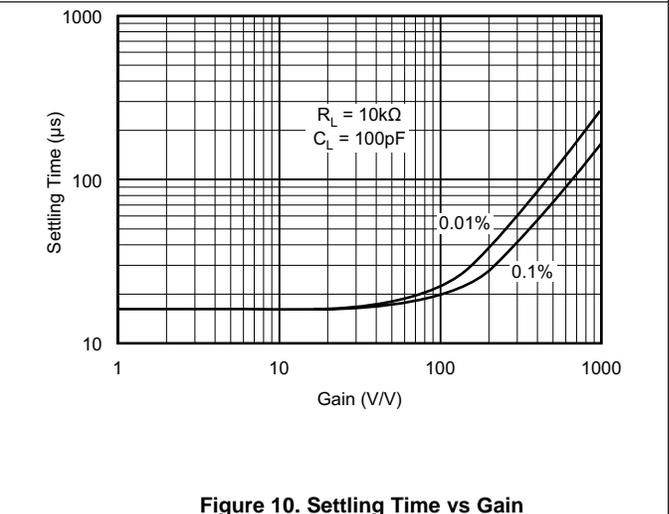


Figure 10. Settling Time vs Gain

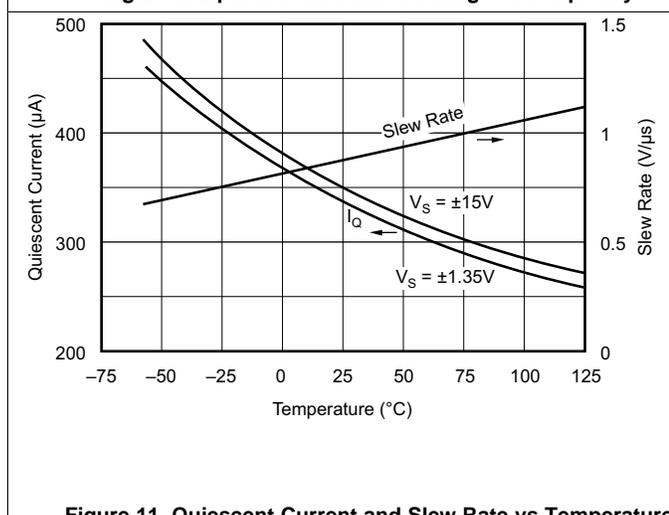


Figure 11. Quiescent Current and Slew Rate vs Temperature

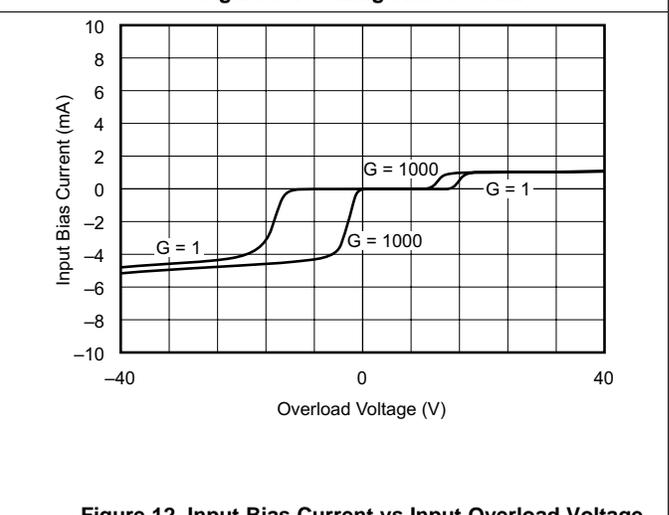


Figure 12. Input Bias Current vs Input Overload Voltage

### Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$  (unless otherwise noted)

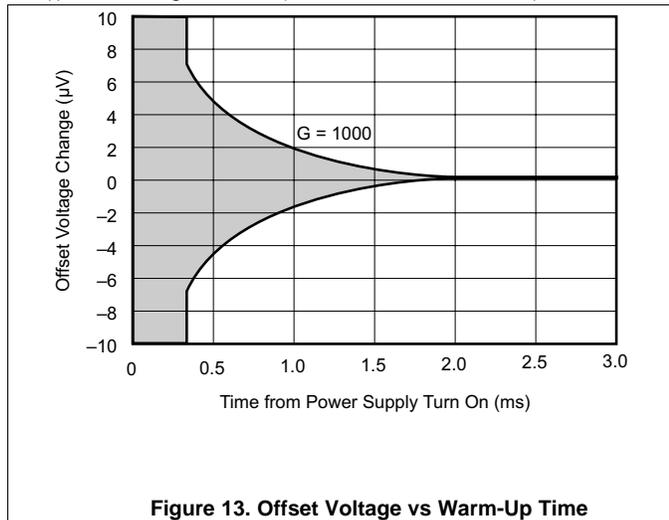


Figure 13. Offset Voltage vs Warm-Up Time

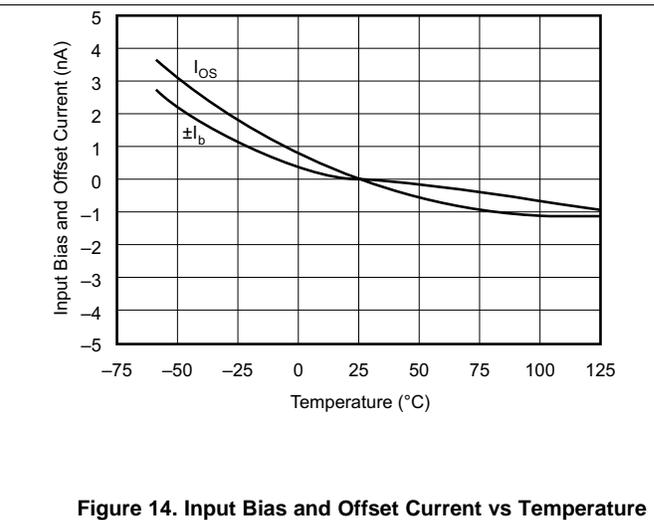


Figure 14. Input Bias and Offset Current vs Temperature

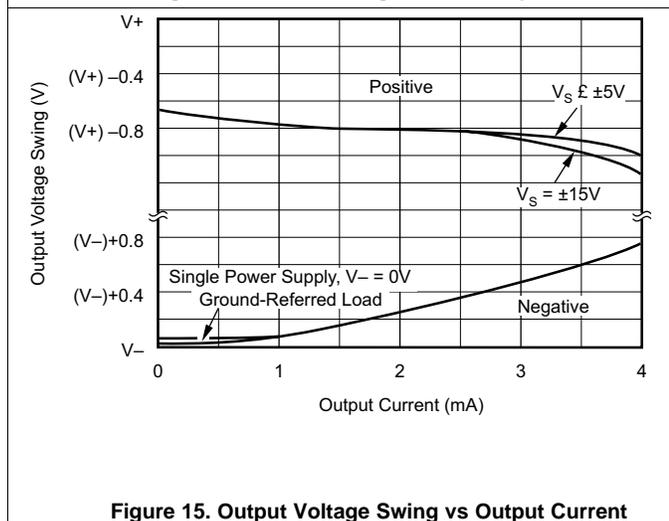


Figure 15. Output Voltage Swing vs Output Current

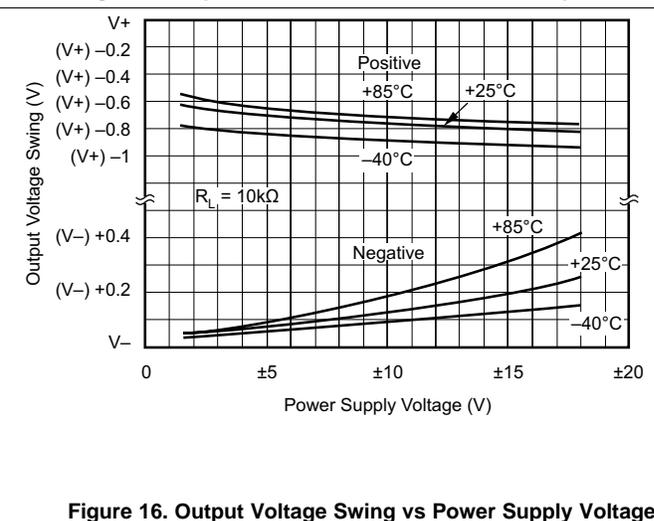


Figure 16. Output Voltage Swing vs Power Supply Voltage

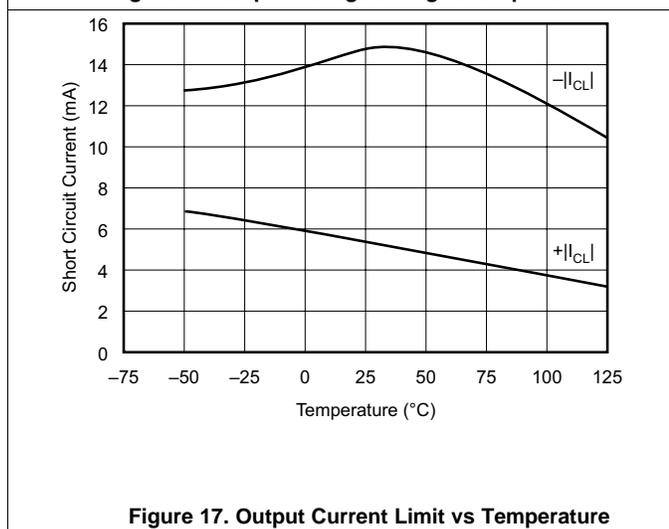


Figure 17. Output Current Limit vs Temperature

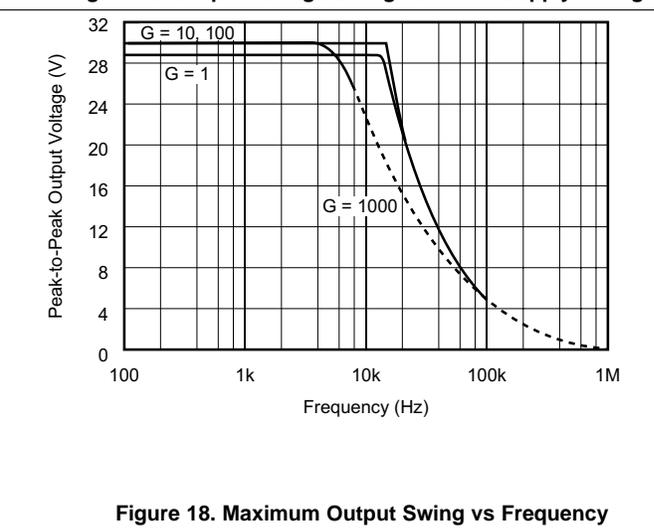


Figure 18. Maximum Output Swing vs Frequency

Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$  (unless otherwise noted)

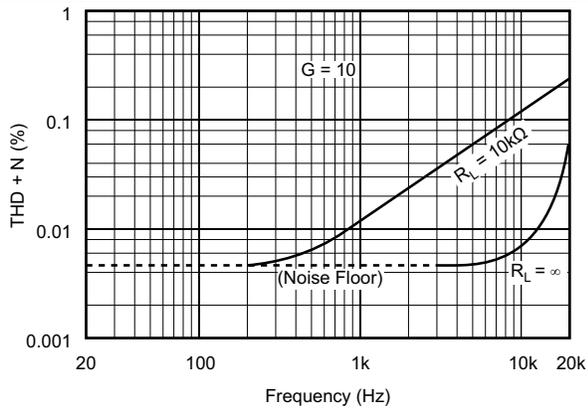


Figure 19. THD + N vs Frequency

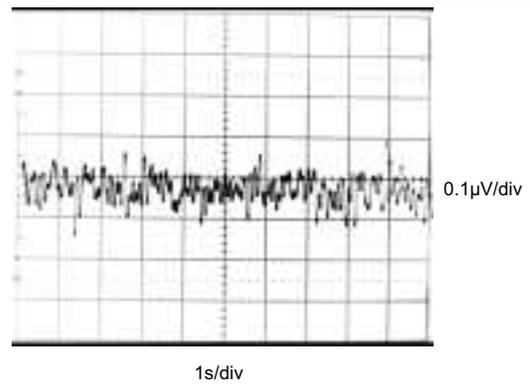


Figure 20. Input-Referred Noise, 0.1 Hz to 10 Hz

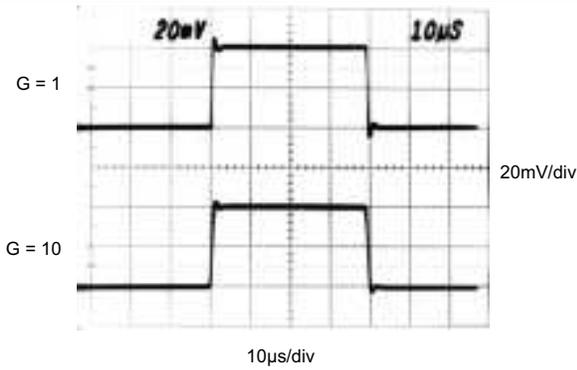


Figure 21. Small-Signal Response

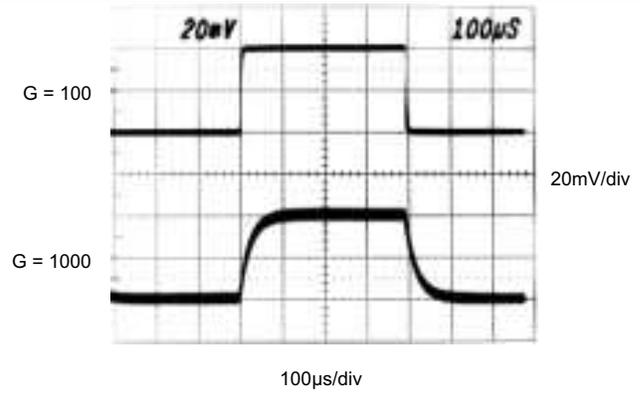


Figure 22. Small-Signal Response

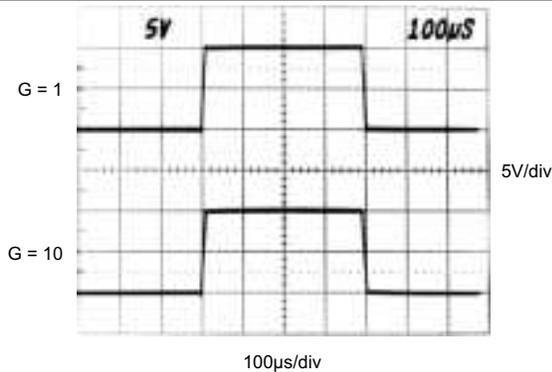


Figure 23. Large-Signal Response

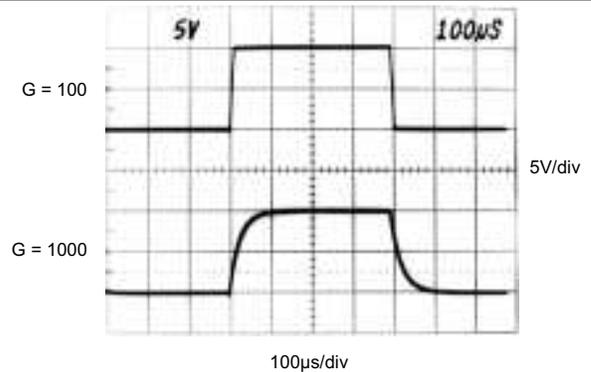


Figure 24. Large-Signal Response

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## 8 Detailed Description

### 8.1 Overview

Figure 25 shows a simplified representation of the INA118 and provides insight into its operation. Each input is protected by two FET transistors that provide a low series resistance under normal signal conditions, preserving excellent noise performance. When excessive voltage is applied, these transistors limit input current to approximately 1.5 to 5 mA.

The differential input voltage is buffered by  $Q_1$  and  $Q_2$  and impressed across  $R_G$ , causing a signal current to flow through  $R_G$ ,  $R_1$  and  $R_2$ . The output difference amp,  $A_3$ , removes the common-mode component of the input signal and refers the output signal to the Ref terminal.

The equations in Figure 25 describe the output voltages of  $A_1$  and  $A_2$ . The  $V_{BE}$  and IR drop across  $R_1$  and  $R_2$  produce output voltages on  $A_1$  and  $A_2$  that are approximately 1-V lower than the input voltages.

### 8.2 Functional Block Diagram

$$A_1 \text{ Out} = V_{CM} - V_{BE} - (10\mu\text{A} \cdot 25\text{k}\Omega) - V_O/2$$

$$A_2 \text{ Out} = V_{CM} - V_{BE} - (10\mu\text{A} \cdot 25\text{k}\Omega) + V_O/2$$

Output Swing Range  $A_1, A_2$ :  $(V_+) - 0.65\text{V}$  to  $(V_-) + 0.06\text{V}$   
 Amplifier Linear Input Range:  $(V_+) - 0.65\text{V}$  to  $(V_-) + 0.98\text{V}$

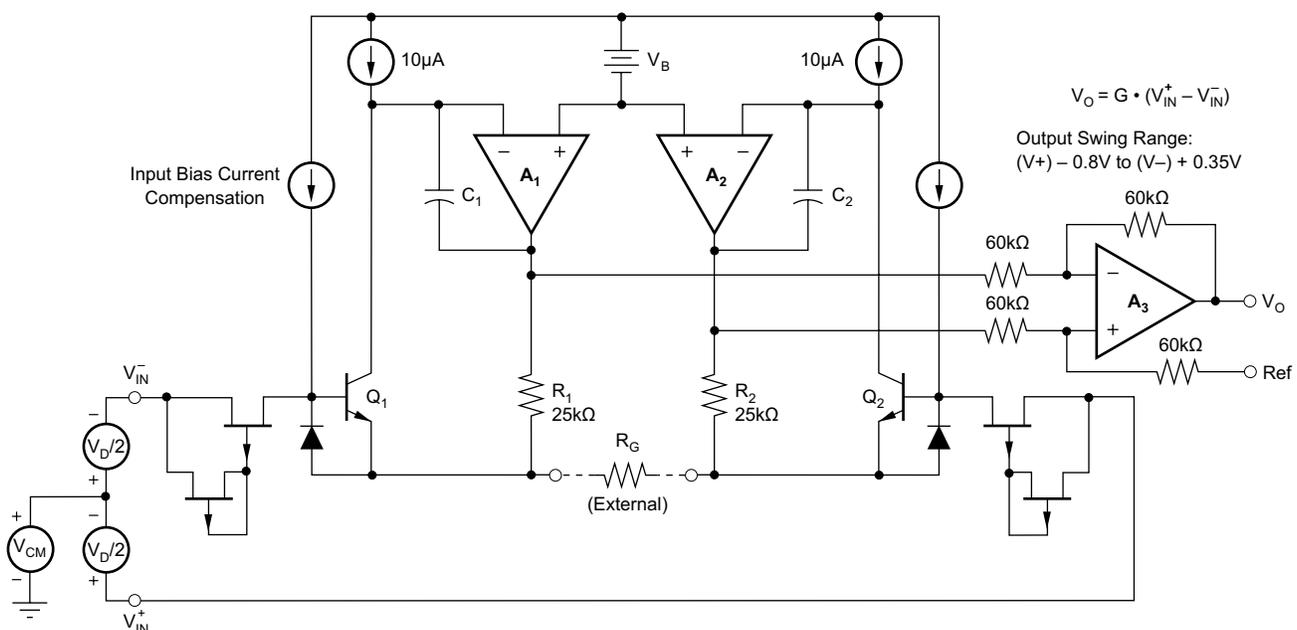


Figure 25. INA118 Simplified Circuit Diagram

### 8.3 Feature Description

The INA118 input sections use junction field effect transistors (JFET) connected to provide protection up to  $\pm 40$  V. The current-feedback architecture provides maximum bandwidth over the full range of gain settings.

### 8.4 Device Functional Modes

#### 8.4.1 Noise Performance

The INA118 provides low noise in most applications. For differential source impedances less than 1 k $\Omega$ , the INA103 may provide lower noise. For source impedances greater than 50 k $\Omega$ , the INA111 FET-Input Instrumentation Amplifier may provide lower noise.

Low-frequency noise of the INA118 is approximately 0.28  $\mu$ Vp-p, measured from 0.1 to 10 Hz ( $G \geq 100$ ). This provides dramatically improved noise when compared to state-of-the-art chopper-stabilized amplifiers.

#### 8.4.2 Input Common-Mode Range

The linear input voltage range of the input circuitry of the INA118 is from approximately 0.6-V less than the positive supply voltage to 1-V greater than the negative supply. As a differential input voltage causes the output voltage to increase, however, the linear input range is limited by the output voltage swing of amplifiers  $A_1$  and  $A_2$ . Thus, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage; see [Figure 6](#).

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier is near zero. The output of the INA118 is near 0 V even though both inputs are overloaded.

#### 8.4.3 Input Protection

The inputs of the INA118 are individually protected for voltages up to  $\pm 40$  V. For example, a condition of  $-40$  V on one input and  $+40$  V on the other input does not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value of approximately 1.5 to 5 mA. [Figure 12](#) shows this input current limit behavior. The inputs are protected even if the power supplies are disconnected or turned off.

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## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The INA118 measures a small differential voltage with a high common-mode voltage developed between the noninverting and inverting input. The high common-mode rejection makes the INA118 suitable for a wide range of applications. The ability to set the reference pin to adjust the functionality of the output signal offers additional flexibility that is practical for multiple configurations

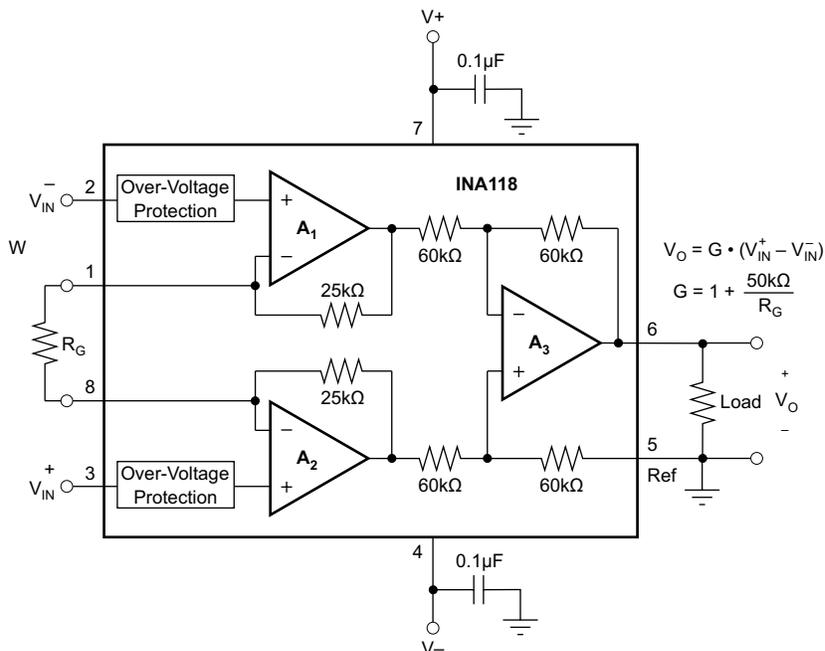
### 9.2 Typical Application

Figure 26 shows the basic connections required for operation of the INA118. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown. The output is referred to the output reference (Ref) terminal, which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 12 Ω in series with the Ref pin causes a typical device to degrade to approximately 80-dB CMR ( $G = 1$ ).

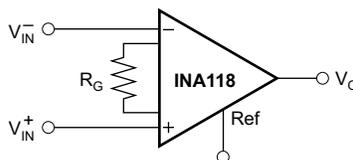
Figure 26 depicts an input signal with a 5-mV, 1-kHz signal with a 1-Vp-p common-mode signal, a condition often observed in process control systems. Figure 27 depicts the output of the INA118 (gain = 250) depicting the clean recovered 1-kHz waveform.

DESIRED GAIN	R <sub>G</sub> (Ω)	NEAREST 1% R <sub>G</sub> (Ω)
1	NC	NC
2	50.00k	49.9k
5	12.50k	12.4k
10	5.556k	5.62k
20	2.632k	2.61k
50	1.02k	1.02k
100	505.1	511
200	251.3	249
500	100.2	100
1000	50.05	49.9
2000	25.01	24.9
5000	10.00	10
10000	5.001	4.99

NC: No Connection.



Also drawn in simplified form:



**Figure 26. Basic Connections**

## Typical Application (continued)

### 9.2.1 Design Requirements

Figure 30 and Figure 29 depict the performance of a typical application of the INA118 in a shop floor vibration sensing application. Because industrial process control systems often involve the interconnecting of multiple subsystems, ground loops are frequently encountered and often are not easily solved. The inherent common-mode rejection of instrumentation amplifiers enables accurate measurements even in the presence of ground loop potentials.

The typical application was tested in a system with these requirements:

- Transducer signal  $\approx 5$  mVp-p
- Transducer center frequency = 1 kHz
- Common-Mode signal (required to be rejected): 1 Vp-p at 60 Hz

### 9.2.2 Detailed Design Procedure

#### 9.2.2.1 Setting the Gain

As shown in Equation 1, the gain of the INA118 is set by connecting a single external resistor,  $R_G$ , connected between pins 1 and 8.

$$G=1+ \frac{50k\Omega}{R_G} \quad (1)$$

Commonly used gains and resistor values are shown in Figure 26.

The 50-k $\Omega$  term in Equation 1 comes from the sum of the two internal feedback resistors of  $A_1$  and  $A_2$ . These on-chip metal film resistors are laser-trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA118.

The stability and temperature drift of the external gain setting resistor,  $R_G$ , also affects gain. The contribution of  $R_G$  to gain accuracy and drift can be directly inferred from Equation 1. Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance, which contributes additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

#### 9.2.2.2 Dynamic Performance

The Figure 1 shows that, despite its low quiescent current, the INA118 achieves wide bandwidth, even at high gain. This is due to the current-feedback topology of the INA118. Settling time also remains excellent at high gain.

The INA118 exhibits approximately 3-dB peaking at 500 kHz in unity gain. This is a result of its current-feedback topology and is not an indication of instability. Unlike an op amp with poor phase margin, the rise in response is a predictable 6-dB/octave due to a response zero. A simple pole at 300 kHz or lower produces a flat passband unity gain response.

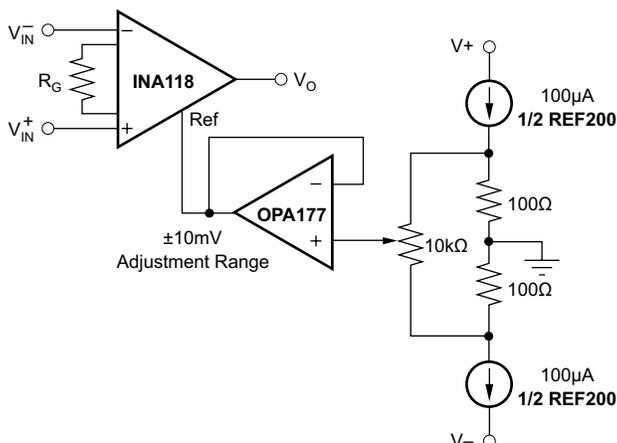
#### 9.2.2.3 Offset Trimming

The INA118 is laser-trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 27 shows an optional circuit for trimming the output offset voltage. The voltage applied to the Ref terminal is summed at the output. The op amp buffer provides low impedance at the Ref terminal to preserve good common-mode rejection.

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**Typical Application (continued)****Figure 27. Optional Trimming of Output Offset Voltage****9.2.2.4 Input Bias Current Return Path**

The input impedance of the INA118 is extremely high at approximately  $10^{10} \Omega$ . However, a path must be provided for the input bias current of both inputs. This input bias current is approximately  $\pm 5 \text{ nA}$ . High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. [Figure 28](#) shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential which exceeds the common-mode range of the INA118, and the input amplifiers saturates.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in [Figure 28](#)). With higher source impedance, using two equal resistors provides a balanced input, with the possible advantages of lower input offset voltage due to bias current, and better high-frequency common-mode rejection.

Typical Application (continued)

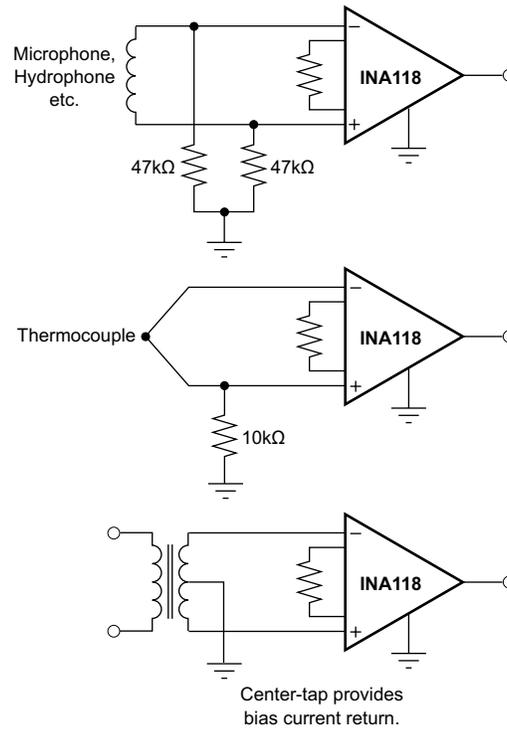
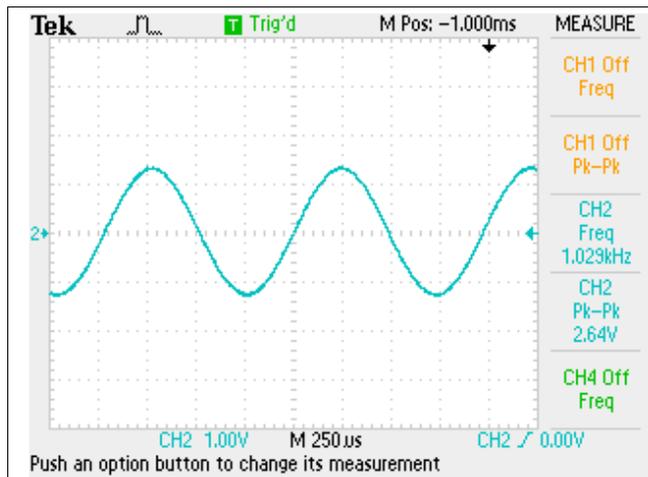


Figure 28. Providing an Input Common-Mode Current Path

9.2.3 Application Curves



1-kHz differential signal is also present but cannot be seen in this waveform.

Figure 29. Input of Typical Application Showing 60-Hz Common-Mode Signal

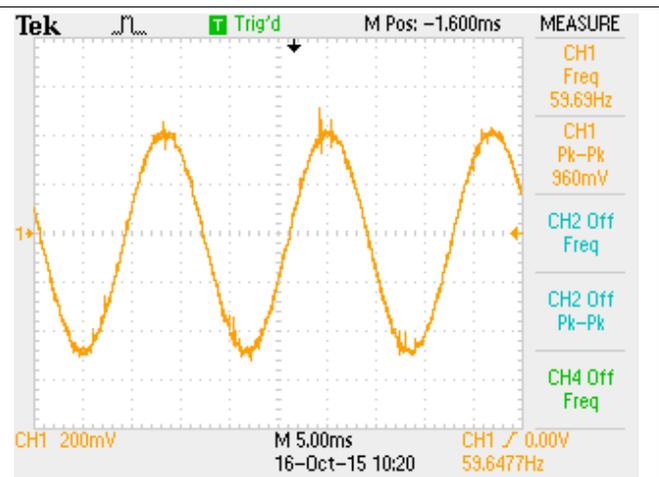


Figure 30. Output of Typical Application Shows Desired 1-kHz Waveform With Common-Mode Interference Rejected

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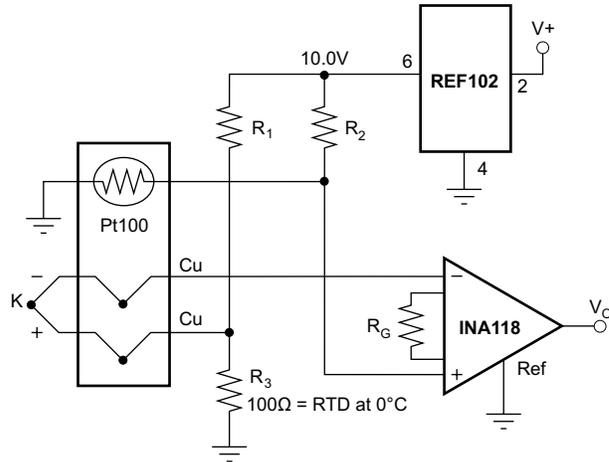
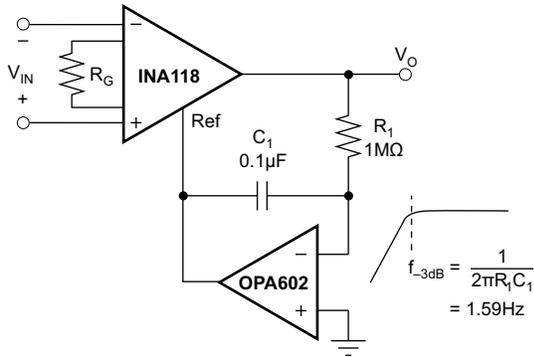
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## 10 Power Supply Recommendations

### 10.1 Low-Voltage Operation

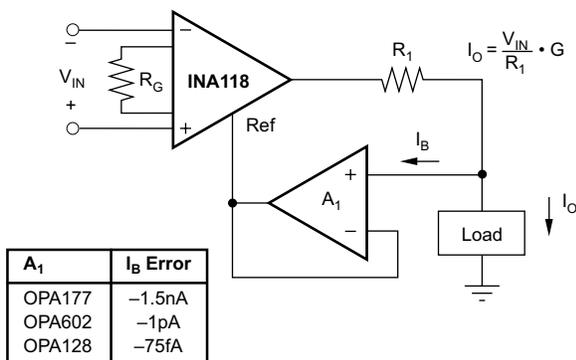
The INA118 can be operated on power supplies as low as  $\pm 1.35$  V. Performance of the INA118 remains excellent with power supplies ranging from  $\pm 1.35$  V to  $\pm 18$  V. Most parameters vary only slightly throughout this supply voltage range; see *Typical Characteristics*. Operation at low supply voltage requires careful attention to assure that the input voltages remain within their linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power supply voltage. **Figure 3** shows the range of linear operation for a various supply voltages and gains.



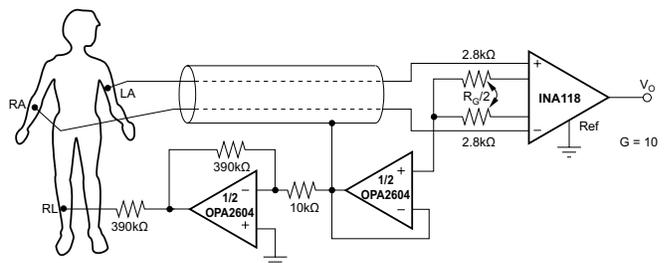
ISA TYPE	MATERIAL	COEFFICIENT ( $\mu\text{V}/^\circ\text{C}$ )	$R_1, R_2$
E	+ Chromel	58.5	66.5k $\Omega$
	- Constantan		
J	+ Iron	50.2	76.8k $\Omega$
	- Constantan		
K	+ Chromel	39.4	97.6k $\Omega$
	- Alumel		
T	+ Copper	38.0	102k $\Omega$
	- Constantan		

**Figure 31. AC-Coupled Instrumentation Amplifier**

**Figure 32. Thermocouple Amplifier With Cold Junction Compensation**



**Figure 33. Differential Voltage to Current Converter**



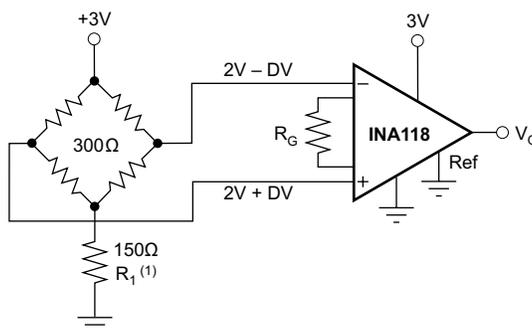
**Figure 34. ECG Amplifier With Right-Leg Drive**

## 10.2 Single-Supply Operation

The INA118 can be used on single power supplies of 2.7 V to 36 V. Figure 35 shows a basic single supply circuit. The output Ref terminal is connected to ground. Zero differential input voltage demands an output voltage of 0 V (ground). Actual output voltage swing is limited to approximately 35-mV above ground, when the load is referred to ground as shown. Figure 15 shows how the output voltage swing varies with output current.

With single supply operation,  $V_{IN}^+$  and  $V_{IN}^-$  must both be 0.98-V above ground for linear operation. It is not possible, for example, to connect the inverting input to ground and measure a voltage connected to the noninverting input.

To illustrate the issues affecting low voltage operation, consider the circuit in Figure 35, which shows the INA118 operating from a single 3-V supply. A resistor in series with the low side of the bridge assures that the bridge output voltage is within the common-mode range of the amplifier's inputs. See Figure 3 for 3-V single supply operation.



NOTE: (1)  $R_1$  required to create proper common-mode voltage, only for low voltage operation — see text.

**Figure 35. Single-Supply Bridge Amplifier**

## 11 Layout

### 11.1 Layout Guidelines

TI always recommends paying attention to good layout practices. For best operational performance of the device, use good printed-circuit-board (PCB) layout practices, including:

- Take care to ensure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals. In addition, parasitic capacitance at the gain-setting pins can also affect CMRR over frequency. For example, in applications that implement gain switching using switches or PhotoMOS® relays to change the value of  $R_G$ , select the component so that the switch capacitance is as small as possible.
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, and of the device itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry. Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from  $V^+$  to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques* (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Keep the traces as short as possible.

## 11.2 Layout Example

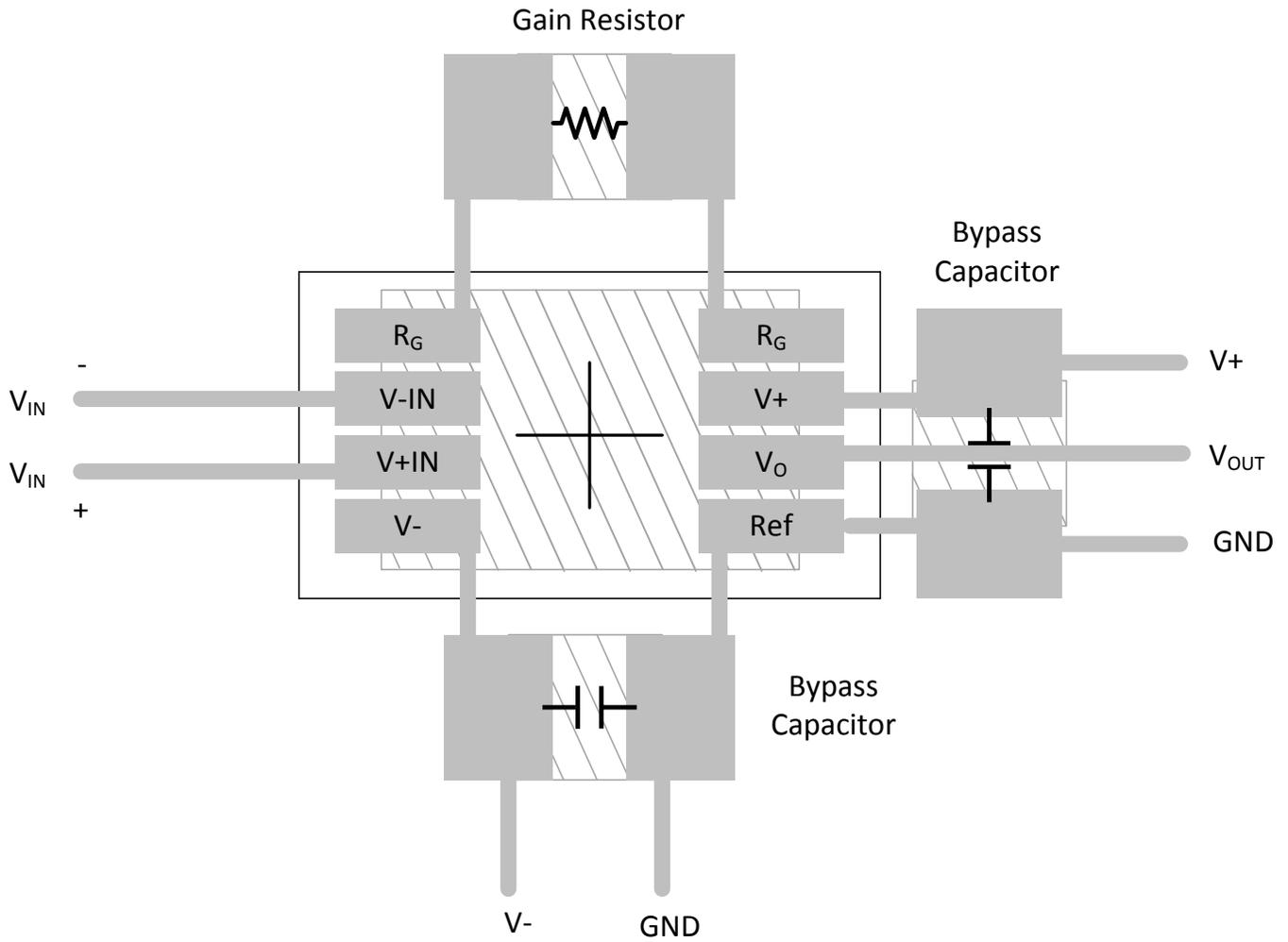


Figure 36. Layout Recommendation

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## 12 器件和文档支持

### 12.1 器件支持

#### 12.1.1 开发支持

表 1. 设计套件与评估模块

名称	部件号	类型
DIP 适配器评估模块	DIP-ADAPTER-EVM	评估模块和评估板
通用仪表放大器评估模块	INAEVM	评估模块和评估板

表 2. 开发工具

名称	部件号	类型
计算仪表放大器的输入共模范围	INA-CMV-CALC	计算工具
基于 SPICE 的模拟仿真程序	TINA-TI	电路设计和仿真

### 12.2 文档支持

#### 12.2.1 相关文档

相关文档如下：《[电路板布局技巧](#)》

### 12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 商标

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All other trademarks are the property of their respective owners.

### 12.5 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 12.6 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA118P	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type	-40 to 85	INA118P	<a href="#">Samples</a>
INA118PB	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		INA118P B	<a href="#">Samples</a>
INA118U	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 118U	<a href="#">Samples</a>
INA118U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 118U	<a href="#">Samples</a>
INA118U/2K5G4	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 118U	<a href="#">Samples</a>
INA118UB	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 118U B	<a href="#">Samples</a>
INA118UB/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 118U B	<a href="#">Samples</a>
INA118UBG4	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 118U B	<a href="#">Samples</a>
INA118UG4	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 118U	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

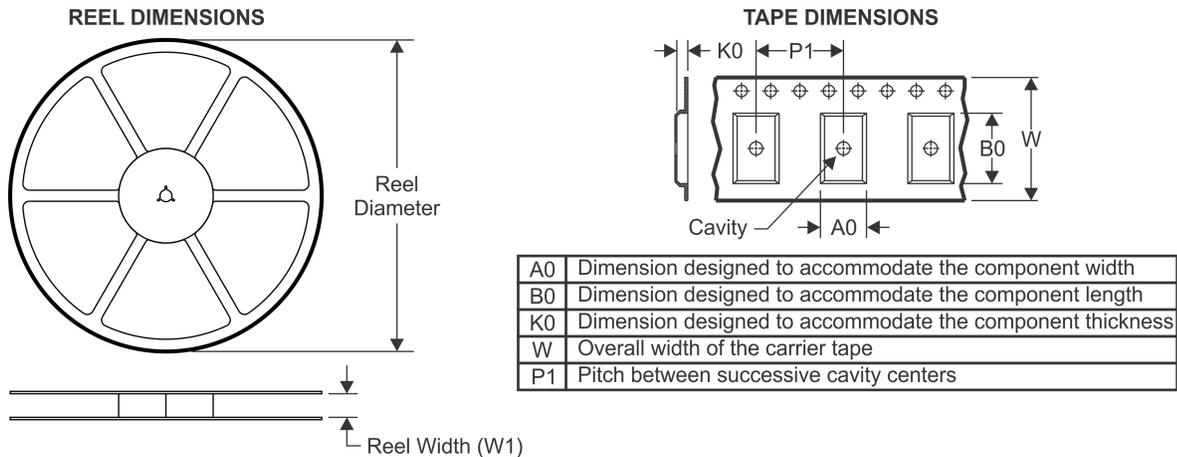
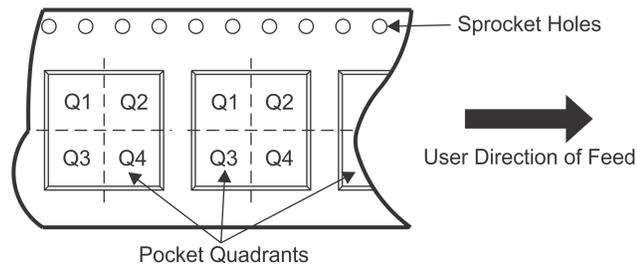
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

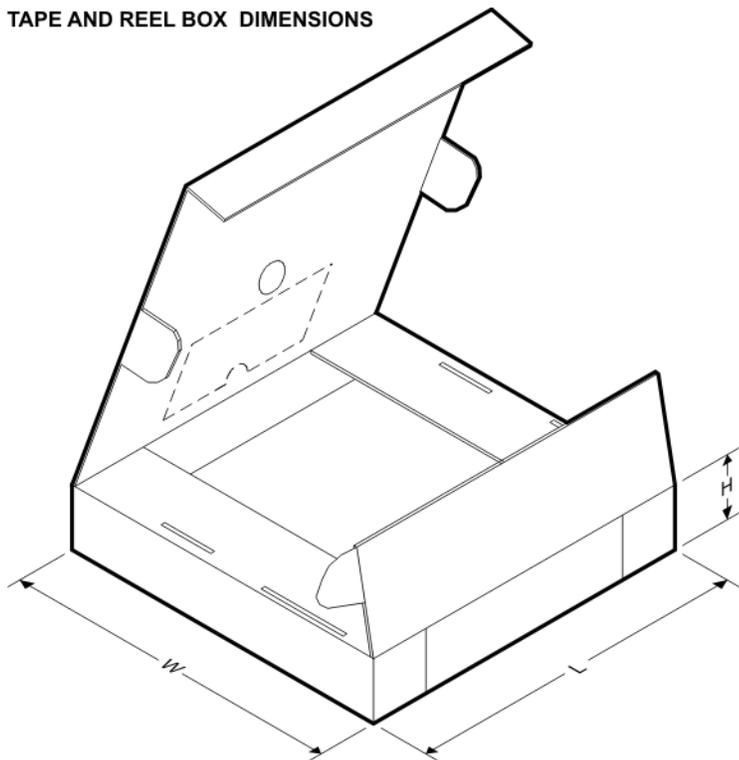
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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


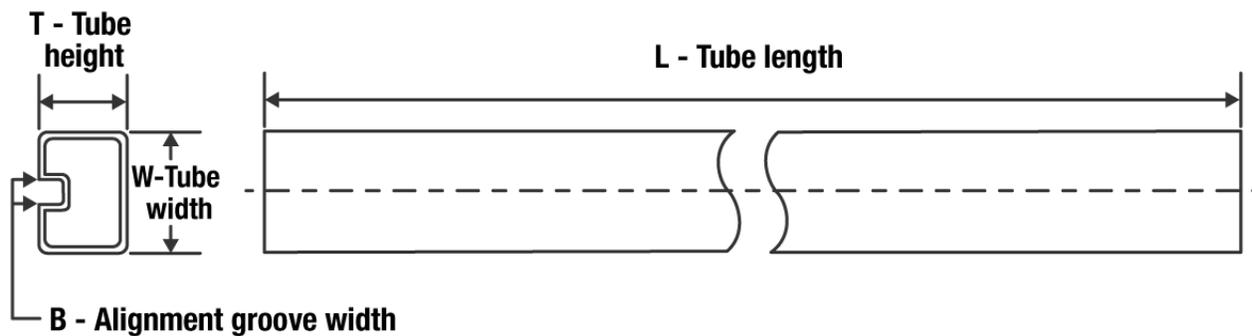
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA118U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA118UB/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA118U/2K5	SOIC	D	8	2500	853.0	449.0	35.0
INA118UB/2K5	SOIC	D	8	2500	367.0	367.0	35.0

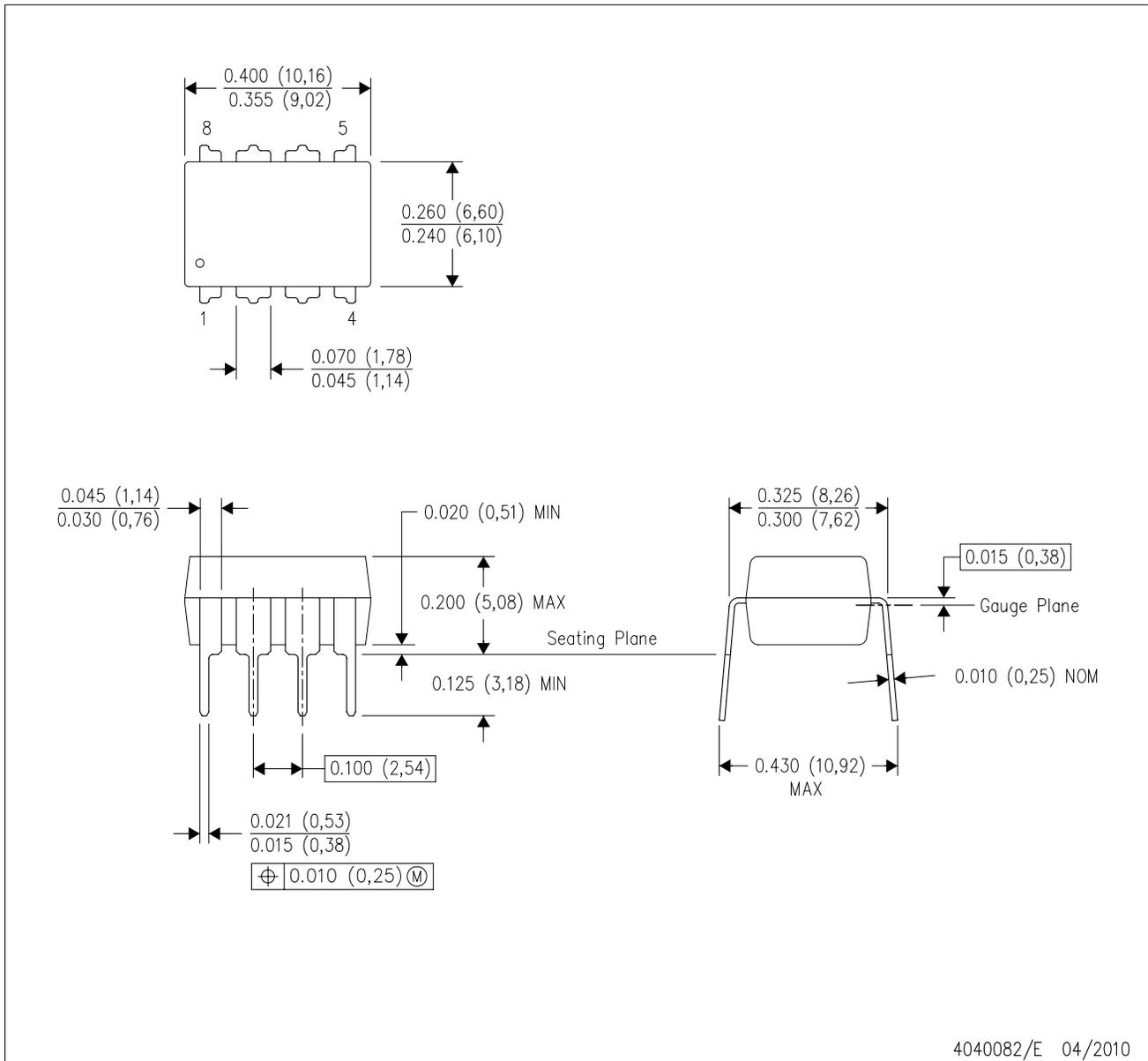
**TUBE**


\*All dimensions are nominal

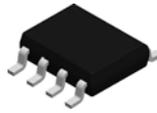
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
INA118P	P	PDIP	8	50	506	13.97	11230	4.32
INA118PB	P	PDIP	8	50	506	13.97	11230	4.32
INA118U	D	SOIC	8	75	506.6	8	3940	4.32
INA118UB	D	SOIC	8	75	506.6	8	3940	4.32
INA118UBG4	D	SOIC	8	75	506.6	8	3940	4.32
INA118UG4	D	SOIC	8	75	506.6	8	3940	4.32

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

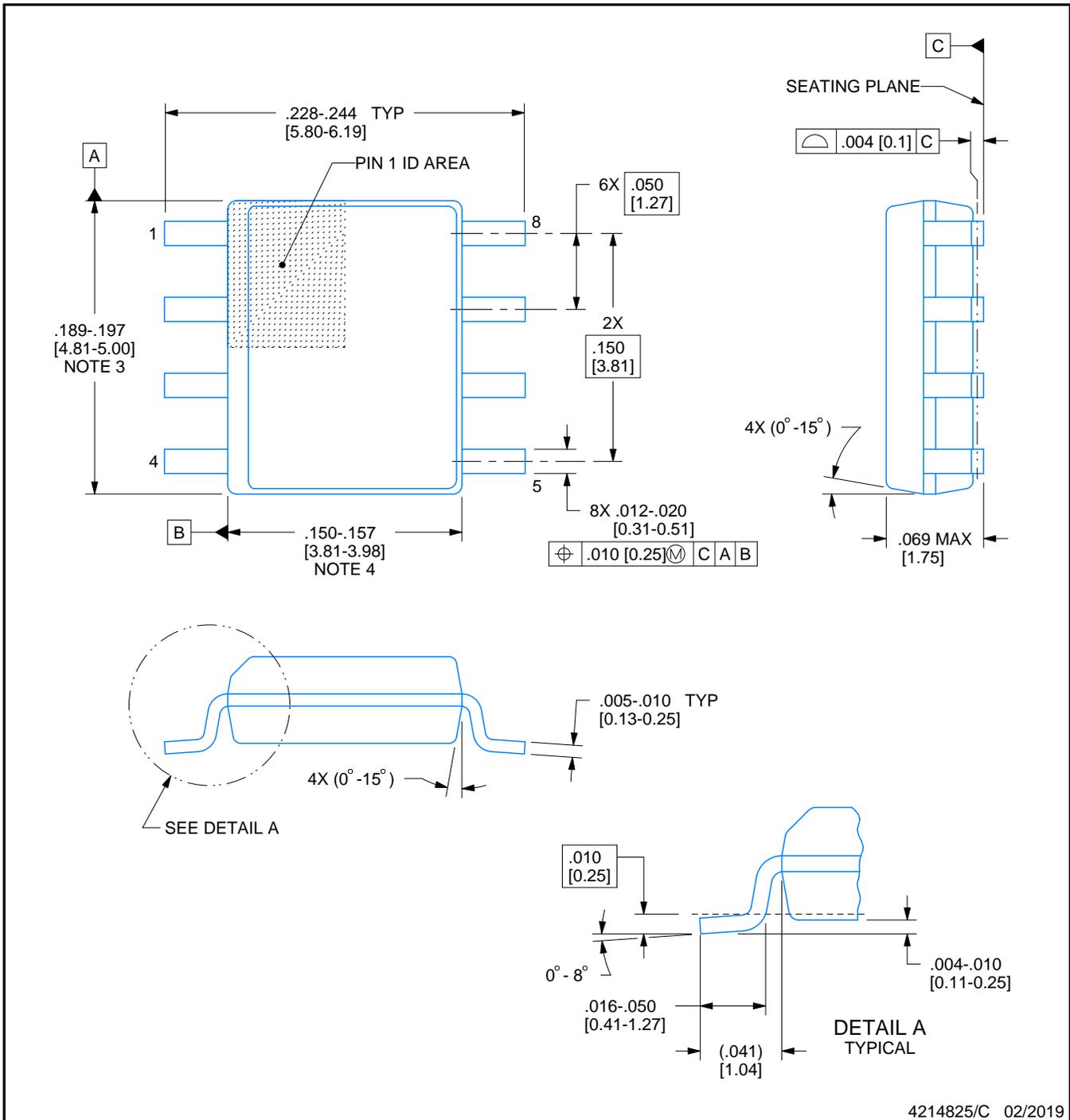


D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

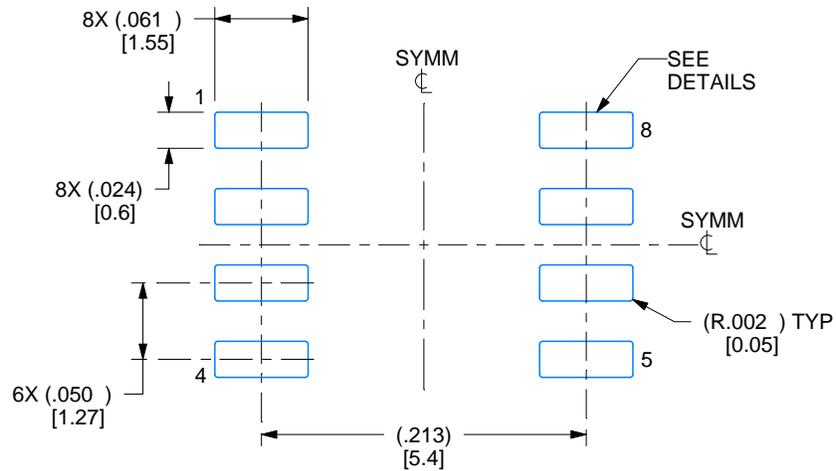
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

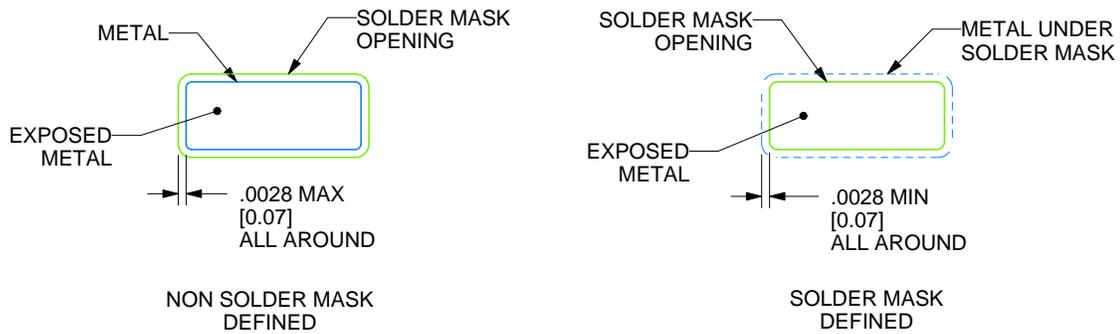
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

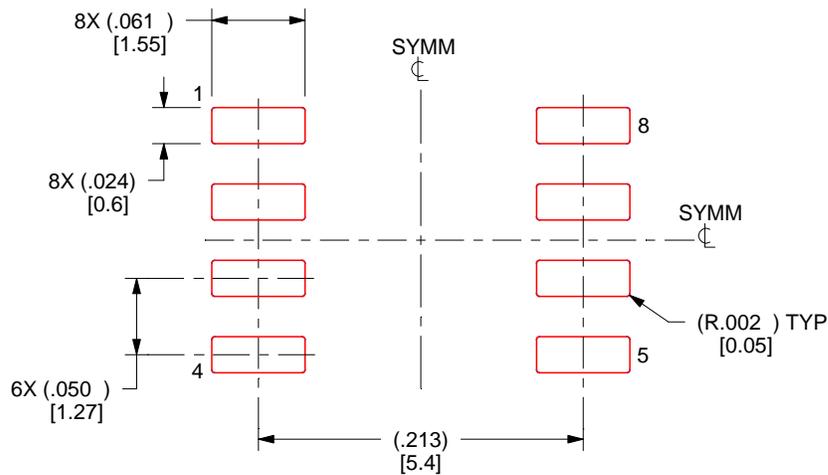
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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