DS92LV3221/DS92LV3222 20-50 MHz 32-Bit Channel Link II Serializer / Deserializer

Check for Samples: DS92LV3221, DS92LV3222

FEATURES

- **Wide Operating Range Embedded Clock SER/DES**
  - **Up to 32-bit Parallel LVCMOS Data**
  - **20 to 50 MHz Parallel Clock**
  - **Up to 1.6 Gbps Application Data Payload**
- **Simplified Clocking Architecture**
  - **No Separate Serial Clock Line**
  - **No Reference Clock Required**
  - **Receiver Locks to Random Data**
- **On-chip Signal Conditioning for Robust Serial Connectivity**
  - **Transmit Pre-Emphasis**
  - **Data Randomization**
  - **DC-Balance Encoding**
  - **Receive Channel Deskew**
  - **Supports up to 10m CAT-5 at 1.6Gbps**
- **Integrated LVDS Terminations**
- **Built-in AT-SPEED BIST for End-To-End System Testing**
- **AC-Coupled Interconnect for Isolation and Fault Protection**
- **> 4KV HBM ESD Protection**
- **Space-Saving 64-pin TQFP Package**
- **Full Industrial Temperature Range: -40° to +85°C**

APPLICATIONS

- **Industrial Imaging (Machine-vision) and Control**
- **Security and Surveillance Cameras and Infrastructure**
- **Medical Imaging**

DESCRIPTION

The DS92LV3221 (SER) serializes a 32-bit data bus into 2 embedded clock LVDS serial channels for a data payload rate up to 1.6 Gbps over cables such as CATx, or backplanes FR-4 traces. The companion DS92LV3222 (DES) deserializes the 2 LVDS serial data channels, de-skews channel-to-channel delay variations and converts the LVDS data stream back into a 32-bit LVCMOS parallel data bus.

On-chip data Randomization/Scrambling and DC balance encoding and selectable serializer Pre-emphasis ensure a robust, low-EMI transmission over longer, lossy cables and backplanes. The Deserializer automatically locks to incoming data without an external reference clock or special sync patterns, providing an easy "plug-and-lock" operation.

By embedding the clock in the data payload and including signal conditioning functions, the Channel-Link II SerDes devices reduce trace count, eliminate skew issues, simplify design effort and lower cable/connector cost for a wide variety of video, control and imaging applications. A built-in AT-SPEED BIST feature validates link integrity and may be used for system diagnostics.

BLOCK DIAGRAM
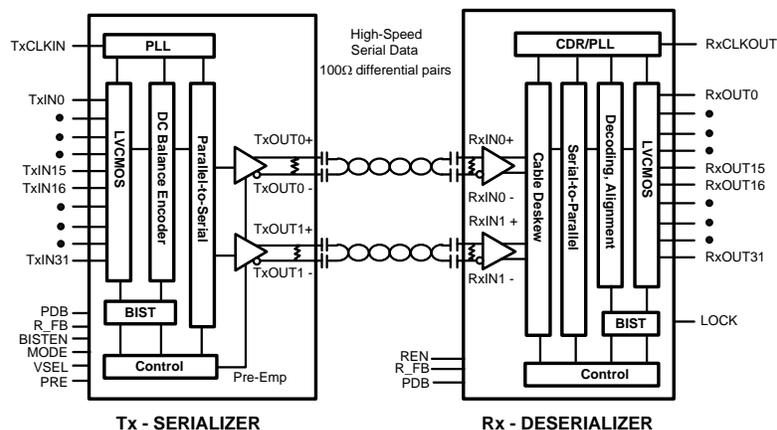
Top View
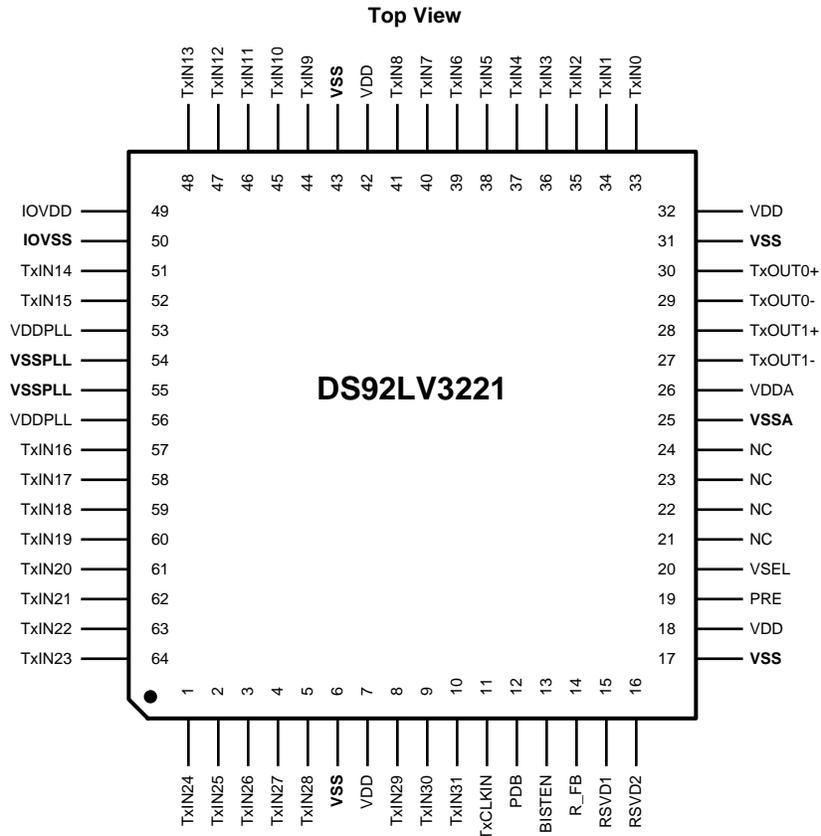
**Figure 1. DS92LV3221 Pin Diagram
64-Pin TQFP (PAG Package)**

Product Folder Links: *DS92LV3221 DS92LV3222*

DS92LV3221 Serializer PIN DESCRIPTIONS

Pin #	Pin Name	I/O, Type	Description
LVCMOS PARALLEL INTERFACE PINS			
10–8, 5–1, 64–57, 52–51, 48–44. 41–33	TxIN[31:29], TxIN[28:24], TxIN[23:16], TxIN[15:14], TxIN[13:9], TxIN[8:0]	I, LVCMOS	Serializer Parallel Interface Data Input Pins.
11	TxCLKIN	I, LVCMOS	Serializer Parallel Interface Clock Input Pin. Strobe edge set by R_FB configuration pin.
CONTROL AND CONFIGURATION PINS			
12	PDB	I, LVCMOS	Serializer Power Down Bar (ACTIVE LOW) PDB = L; Device Disabled, Differential serial outputs are put into TRI-STATE stand-by mode, PLL is shutdown PDB = H; Device Enabled
19	PRE	I, LVCMOS	PRE-emphasis level select pin PRE = (RPRE > 12kΩ); Imax = [(1.2/R) x 20 x 2], Rmin = 12kΩ. PRE = H or floating; pre-emphasis is disabled.
14	R_FB	I, LVCMOS	Rising/Falling Bar Clock Edge Select R_FB = H; Rising Edge, R_FB = L; Falling Edge
20	VSEL	I, LVCMOS	VOD (Differential Output Voltage) Llevel Select VSEL = L; Low Swing, VSEL = H; High Swing
13	BISTEN	I, LVCMOS	BIST Enable BISTEN = L; BIST OFF, (default), normal operating mode. BISTEN = H; BIST Enabled (ACTIVE HIGH)
15, 16	RSVD	I, LVCMOS	Reserved — MUST BE TIED LOW
21, 22, 23, 24	NC		Do Not Connect, leave pins floating
LVDS SERIAL INTERFACE PINS			
28, 30	TxOUT[1:0]+	O, LVDS	Serializer LVDS Non-Inverted Outputs(+)
27, 29	TxOUT[1:0]-	O, LVDS	Serializer LVDS Inverted Outputs(-)
POWER / GROUND PINS			
7, 18, 32, 42	VDD	VDD	Digital Voltage supply, 3.3V
6, 17, 31, 43	VSS	GND	Digital ground
53, 56	VDDPLL	VDD	Analog Voltage supply, PLL POWER, 3.3V
54, 55	VSSPLL	GND	Analog ground, PLL GROUND
26	VDDA	VDD	Analog Voltage supply
25	VSSA	GND	Analog ground
49	IOVDD	VDD	Digital IO Voltage supply Connect to 1.8V typ for 1.8V LVCMOS interface Connect to 3.3V typ for 3.3V LVCMOS interface
50	IOVSS	GND	Digital IO ground

Product Folder Links: *DS92LV3221 DS92LV3222*

Top View
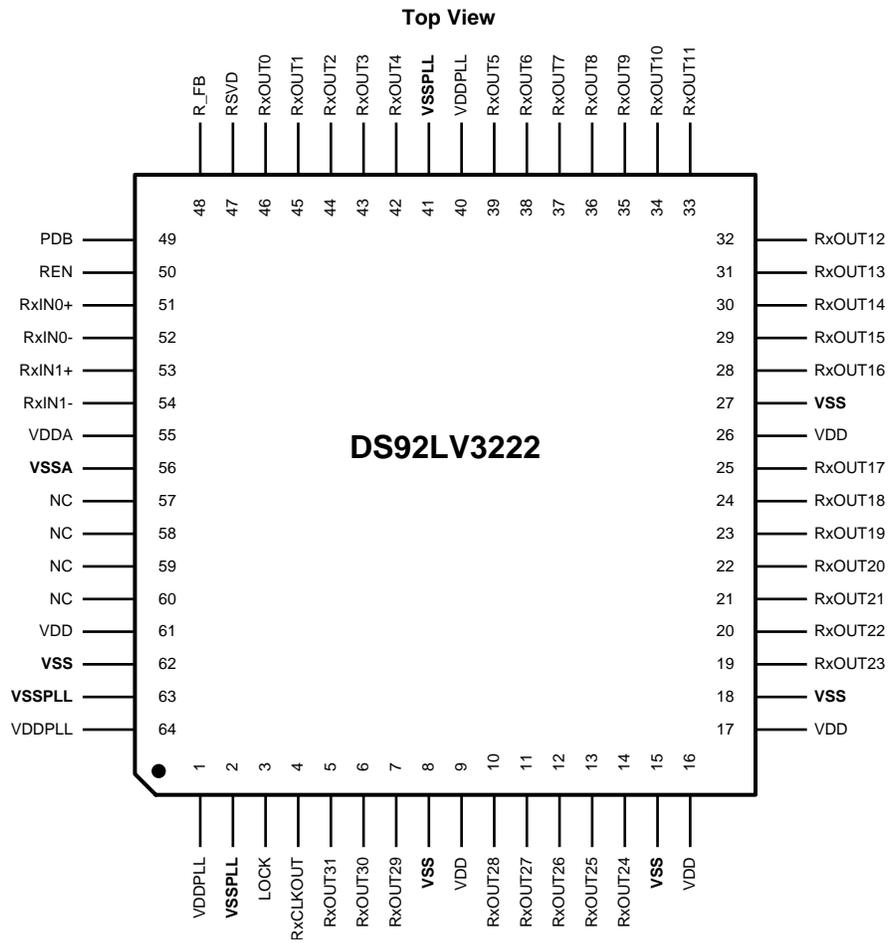
**Figure 2. DS92LV3222 Pin Diagram
64-Pin TQFP (PAG Package)**

DS92LV3222 DESERIALIZER PIN DESCRIPTIONS

Pin #	Pin Name	I/O, Type	Description
LVCMOS PARALLEL INTERFACE PINS			
5–7, 10–14, 19–25, 28–32, 33–39, 42–46	RxOUT[31:29], RxOUT[28:24], RxOUT[23:17], RxOUT[16:12], RxOUT[11:5], RxOUT[4:0]	O, LVCMOS	Deserializer Parallel Interface Data Output Pins.
4	RxCLKOUT	O, LVCMOS	Deserializer Recovered Clock Output. Parallel data rate clock recovered from the embedded clock.
3	LOCK	O, LVCMOS	LOCK indicates the status of the receiver PLL LOCK = L; deserializer CDR/PLL is not locked, RxOUT[31:0] and RCLK are TRI-STATED LOCK = H; deserializer CDR/PLL is locked
CONTROL AND CONFIGURATION PINS			
48	R_FB	I, LVCMOS	Rising/Falling Bar Clock Edge Select R_FB = H; RxOUT clocked on rising edge R_FB = L; RxOUT clocked on falling edge
50	REN	I, LVCMOS	Deserializer Enable, DES Output Enable Control Input (ACTIVE HIGH) REN = L; disabled, RxOUT[31:0] and RxCLKOUT TRI-STATED, PLL still operational REN = H; Enabled (ACTIVE HIGH)
49	PDB	I, LVCMOS	Power Down Bar, Control Input Signal (ACTIVE LOW) PDB = L; disabled, RxOUT[31:0], RCLK, and LOCK are TRI-STATED in stand-by mode, PLL is shutdown PDB = H; Enabled
47	RSVD	I, LVCMOS	Reserved — MUST BE TIED LOW
57, 58, 59, 60	NC		Do Not Connect, leave pins floating
LVDS SERIAL INTERFACE PINS			
51, 53	RxIN[0:1]+	I, LVDS	Deserializer LVDS Non-Inverted Inputs(+)
52, 54	RxIN[0:1]-	I, LVDS	Deserializer LVDS Inverted Inputs(-)
POWER / GROUND PINS			
9, 16, 17, 26, 61	VDD	VDD	Digital Voltage supply, 3.3V
8, 15, 18, 27, 62	VSS	GND	Digital Ground
55	VDDA	VDD	Analog LVDS Voltage supply, POWER, 3.3V
56	VSSA	GND	Analog LVDS GROUND
1, 40, 64	VDDPLL	VDD	Analog Voltage supply PLL VCO POWER, 3.3V
2, 41, 63	VSSPLL	GND	Analog ground, PLL VCO GROUND

Product Folder Links: *DS92LV3221 DS92LV3222*

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS[(1)(2)]

Supply Voltage (V_{DD})	−0.3V to +4V
LVCMOS Input Voltage	−0.3V to (V_{DD} +0.3V)
LVCMOS Output Voltage	−0.3V to (V_{DD} +0.3V)
LVDS Deserializer Input Voltage	−0.3V to +3.9V
LVDS Driver Output Voltage	−0.3V to +3.9V
Junction Temperature	+125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	+260°C
Maximum Package Power Dissipation Capacity Package Derating	1/θ_{JA} °C/W above +25°C
θ_{JA}	35.7 °C/W[(3)]
θ_{JC}	12.6 °C/W
ESD Rating (HBM)	>4 kV

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(2) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
(3) 4 Layer JEDEC

RECOMMENDED OPERATING CONDITIONS

		Min	Nom	Max	Units
Supply Voltage (V_{DD})		3.135	3.3	3.465	V
Supply Voltage (IOV_{DD}) (SER ONLY)	3.3V I/O Interface	3.135	3.3	3.465	V
	1.8V I/O Interface	1.71	1.8	1.89	V
Operating Free Air Temperature (T_A)		−40	+25	+85	°C
Input Clock Rate		20		50	MHz
Tolerable Supply Noise				100	mV_{P-P}

ELECTRICAL CHARACTERISTICS

Over recommended operating supply and temperature ranges unless otherwise specified. [(1)(2)]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVCMOS DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage	Tx: IOV_{DD} = 1.71V to 1.89V	0.65 x IOV_{DD}		IOV_{DD} + 0.3	V
		Tx: IOV_{DD} = 3.135V to 3.465V	2.0		V_{DD}	
		Rx				
V_{IL}	Low Level Input Voltage	Tx: IOV_{DD} = 1.71V to 1.89V	GND		0.35 x IOV_{DD}	V
		Tx: IOV_{DD} = 3.135V to 3.465V	GND		0.8	
		Rx				
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		−0.8	−1.5	V
I_{IN}	Input Current	Tx: V_{IN} = 0V or 3.465V(1.89V) IOV_{DD} = 3.465V(1.89V)	−10		+10	μA
		Rx: V_{IN} = 0V or 3.465V	−10		+10	

(1) Typical values represent most likely parametric norms at V_{DD} = 3.3V, T_A = +25°C, and at the Recommended Operating Conditions at the time of product characterization and are not verified.
(2) Current into a the device is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except V_{OD}, ΔV_{OD}, V_{TH}, V_{TL} which are differential voltages.

Product Folder Links: *DS92LV3221 DS92LV3222*

ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	High Level Output Voltage	I_{OH} = −2mA	2.4	3.0	V_{DD}	V
V_{OL}	Low Level Output Voltage	I_{OH} = −2mA	GND	0.33	0.5	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V		−22	−40	mA
I_{OZ}	TRI-STATE Output Current	PDB = 0V, V_{OUT} = 0V or V_{DD}	−10		+10	µA
SERIALIZER LVDS DC SPECIFICATIONS						
V_{OD}	Output Differential Voltage	No pre-emphasis, VSEL = L (VSEL = H)	350 (629)	440 (850)	525 (1000)	mV$_{P-P}$
ΔV_{OD}	Output Differential Voltage Unbalance	VSEL = L, No pre-emphasis		1	50	mV$_{P-P}$
V_{OS}	Offset Voltage	VSEL = L, No pre-emphasis	1.00	1.25	1.50	V
ΔV_{OS}	Offset Voltage Unbalance	VSEL = L, No pre-emphasis		4	50	mV
I_{OS}	Output Short Circuit Current	TxOUT[1:0] = 0V, PDB = V_{DD}, VSEL = L, No pre-emphasis	−2	−5		mA
		TxOUT[1:0] = 0V, PDB = V_{DD}, VSEL = H, No pre-emphasis	−6	−10		
I_{OZ}	TRI-STATE Output Current	PDB = 0V, TxOUT[1:0] = 0V OR V_{DD}	−15	±1	+15	µA
		PDB = V_{DD}, TxOUT[1:0] = 0V OR V_{DD}	−15	±1	+15	µA
R_T	Output Termination	Internal differential output termination between differential pairs	90	100	130	Ω
SERIALIZER SUPPLY CURRENT (DVDD, PVDD AND AVDD PINS)[3]						
I_{DDTD}	Serializer (Tx) Total Supply Current (includes load current)	f= 50 MHz, CHECKER BOARD pattern VSEL = H, PRE = OFF		120	145	mA
		f= 50 MHz, CHECKER BOARD pattern VSEL = H, RPRE = 12 kΩ		120	145	
		f= 50 MHz, RANDOM pattern VSEL = H, PRE = OFF		115	135	
		f= 50 MHz, RANDOM pattern VSEL = H, RPRE = 12 kΩ		115	135	
I_{DDTZ}	Serializer Supply Current Power-down	TPWDNB = 0V (All other LVCMOS Inputs = 0V)		2	50	µA
DESERIALIZER LVDS DC SPECIFICATIONS						
V_{TH}	Differential Threshold High Voltage	V_{CM} = +1.8V			+50	mV
V_{TL}	Differential Threshold Low Voltage		−50			mV
R_T	Input Termination	Internal differential output termination between differential pairs	90	100	130	Ω
I_{IN}	Input Current	V_{IN} = +2.4V, V_{DD} = 3.6V		±100	±250	µA
		V_{IN} = 0V, V_{DD} = 3.6V		±100	±250	µA
DESERIALIZER SUPPLY CURRENT (DVDD, PVDD AND AVDD PINS)[3]						
		f = 50 MHz, C_L = 8 pF, CHECKER BOARD pattern		145	185	mA
		f = 50 MHz, C_L = 8 pF, RANDOM pattern		122	140	
I_{DDRZ}	Deserializer Supply Current Power-down	PDB = 0V (All other LVCMOS Inputs = 0V, RxIN[1:0](P/N) = 0V)			100	µA

(3)   DIGITAL, PLL, AND ANALOG VDDS

SERIALIZER INPUT TIMING REQUIREMENTS FOR TCLK

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{CIP}	TxCLKIN Period		20	t_{CIP}	50	ns
t_{CIH}	TxCLKIN High Time	20 MHz – 50 MHz	0.45 x t_{CIP}	0.5 x t_{CIP}	0.55 x t_{CIP}	ns
t_{TCIL}	TxCLKIN Low Time	20 MHz – 50 MHz Figure 5	0.45 x t_{CIP}	0.5 x t_{CIP}	0.55 x t_{CIP}	ns
t_{CIT}	TxCLKIN Transition Time	20 MHz – 50 MHz Figure 4	0.5		1.2	ns
t_{JIT}	TxCLKIN Jitter				±100	ps_{P-P}

SERIALIZER SWITCHING CHARACTERISTICS

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{LLHT}	LVDS Low-to-High Transition Time	No pre-emphasis Figure 3		350		ps
t_{LHLT}	LVDS High-to-Low Transition Time			350		ps
t_{STC}	TxIN[31:0] Setup to TxCLKIN	IOVDD = 1.71V to 1.89V Figure 5	0			ns
		IOVDD = 3.135V to 3.465V	0			
t_{HTC}	TxIN[31:0] Hold from TxCLKIN	IOVDD = 1.71V to 1.89V	2.5			ns
		IOVDD = 3.135V to 3.465V	2.25			
t_{PLD}	Serializer PLL Lock Time	Figure 7		4400 x t_{CIP}	5000 x t_{CIP}	ns
t_{LZD}	Data Output LOW to TRI-STATE Delay	See[1]		5	10	ns
t_{HZD}	Data Output TRI-STATE to HIGH Delay	See[1]		5	10	ns
t_{SD}	Serializer Propagation Delay - Latency	f = 50 MHz, R_FB = H, PRE = OFF, Figure 6		4.5 t_{CIP} + 6.77		ns
		f = 50 MHz, R_FB = L, PRE = OFF, Figure 6	4.5 t_{CIP} + 5.63	4.5 t_{CIP} + 7.09	4.5 t_{CIP} + 9.29	
		f = 20 MHz, R_FB = H, PRE = OFF,	4.5 t_{CIP} + 6.57	4.5 t_{CIP} + 8.74	4.5 t_{CIP} + 10.74	
t_{LVSKD}	LVDS Output Skew	LVDS differential output channel-to-channel skew		30	500	ps
$Λ_{STXBW}$	Jitter Transfer Function -3 dB Bandwidth	f = 50 MHz Figure 13		2.8		MHz
$δ_{STX}$	Serializer Jitter Transfer Function Peaking	f = 50 MHz		0.3		dB

(1) When the Serializer output is at TRI-STATE the Deserializer will lose PLL lock. Resynchronization MUST occur before data transfer.

Product Folder Links: *DS92LV3221 DS92LV3222*

DESERIALIZER SWITCHING CHARACTERISTICS

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{ROCP}	Receiver Output Clock Period	$t_{ROCP} = t_{CIP}$ Figure 9	20	t_{ROCP}	50	ns
t_{RODC}	RxCLKOUT Duty Cycle		45	50	55	%
t_{ROTR}	LVCMOS Low-to-High Transition Time	C_L = 8pF (lumped load) Figure 8		3.2		ns
t_{ROTF}	LVCMOS High-to-Low Transition Time			3.5		ns
t_{ROSC}	RxOUT[31:0] Setup to RxCLKOUT	f = 50 MHz	5.6	0.5 x t_{ROCP}		ns
t_{ROHC}	RxOUT[31:0] Hold to RxCLKOUT		7.4	0.5 x t_{ROCP}		ns
t_{HZR}	Data Output High to TRI-STATE Delay	Figure 11		5	10	ns
t_{LZR}	Data Output Low to TRI-STATE Delay			5	10	ns
t_{ZHR}	Data Output TRI-STATE to High Delay			5	10	ns
t_{ZLR}	Data Output TRI-STATE to Low Delay			5	10	ns
t_{RD}	Deserializer Porpagation Delay – Latency	f = 20 MHz Figure 10		5.5 x t_{ROCP} + 3.35		ns
		f = 50 MHz		5.5 x t_{ROCP} + 6.00		ns
t_{RPLLS}	Deserializer PLL Lock Time	20 MHz – 50 MHz Figure 11 See[1]			128k x t_{ROCP}	ns
TOL_{JIT}	Deserializer Input Jitter Tolerance			0.25		UI
t_{LVSKR}	LVDS Differential Input Skew Tolerance	20 MHz – 50 MHz Figure 15			0.4 x t_{ROCP}	ns

(1) t_{RPLLS} is the time required by the Deserializer to obtain lock when exiting power-down mode.

AC Timing Diagrams and Test Circuits
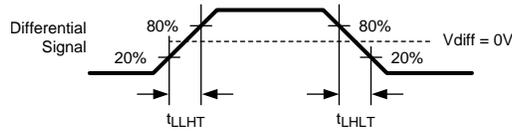
Figure 3. Serializer LVDS Transition Times
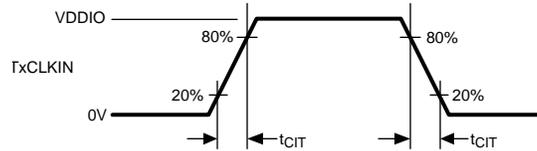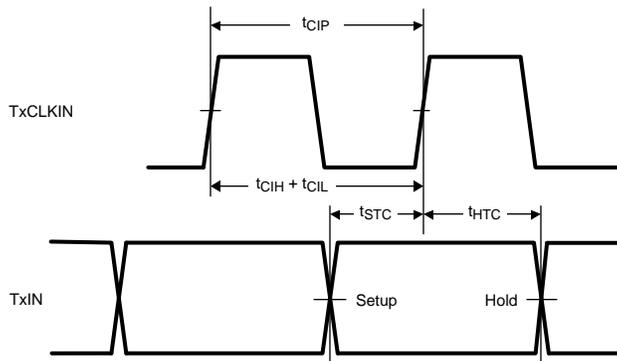

Figure 4. Serializer Input Clock Transition Time

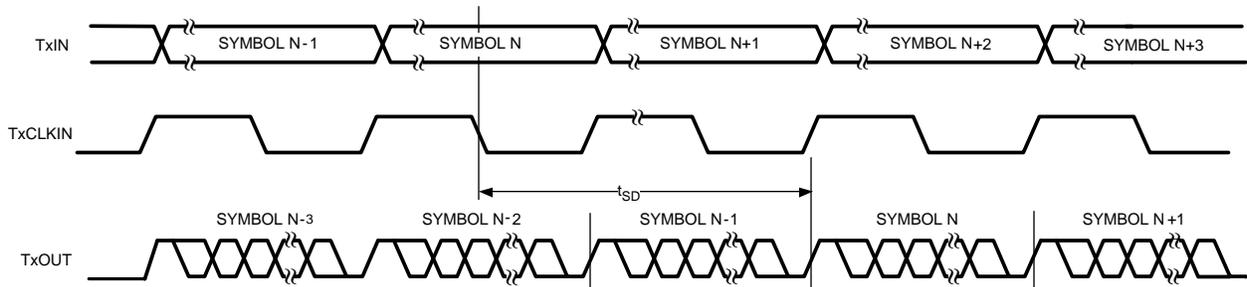**Figure 5. Serializer Setup/Hold and High/Low Times**

Figure 6. Serializer Propagation Delay

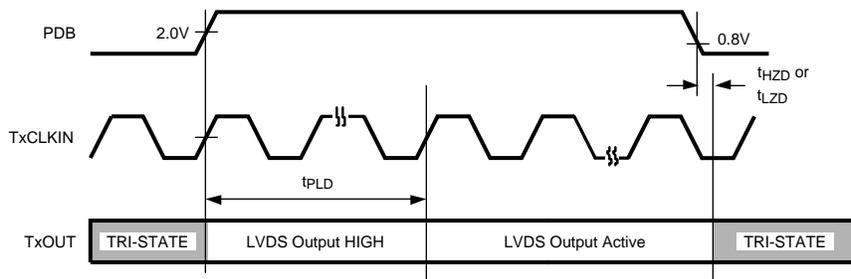Product Folder Links: *DS92LV3221 DS92LV3222*

Figure 7. Serializer PLL Lock Time
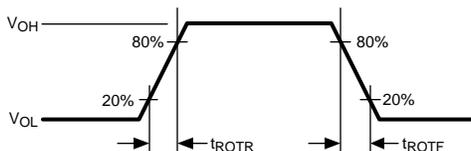
Figure 8. Deserializer LVCMOS Output Transition Time
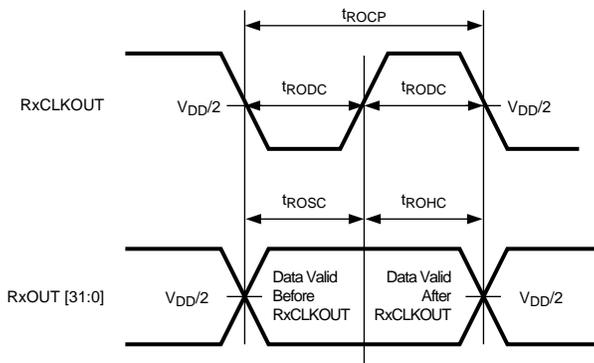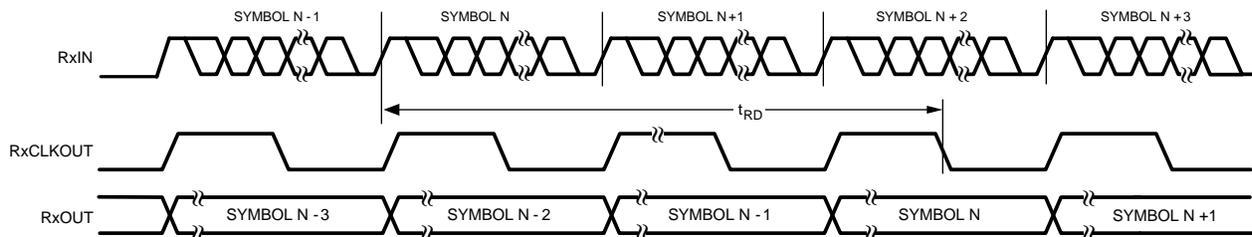

Figure 9. Deserializer Setup and Hold times

Figure 10. Deserializer Propagation Delay
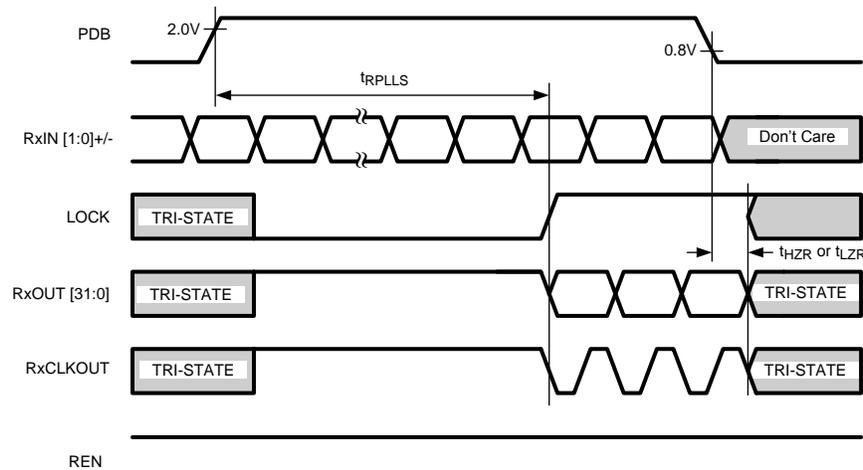
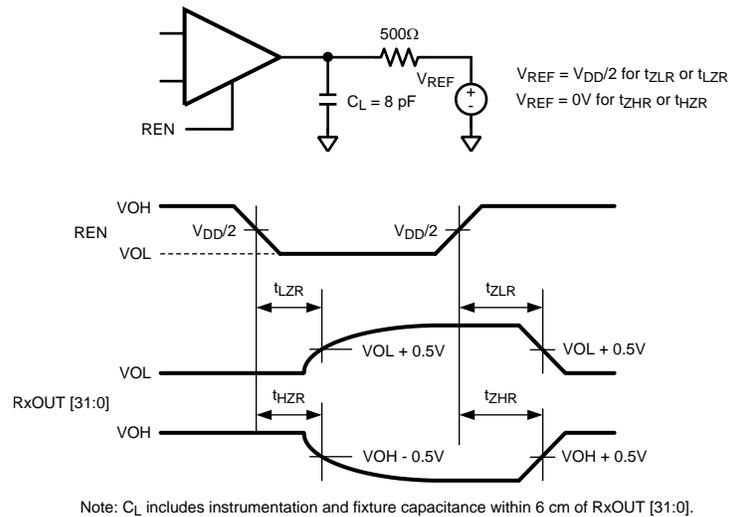**Figure 11. Deserializer PLL Lock Time and PDB TRI-STATE Delay**

Note: C_L includes instrumentation and fixture capacitance within 6 cm of RxOUT [31:0].

Figure 12. Deserializer TRI_STATE Test Circuit and Timing
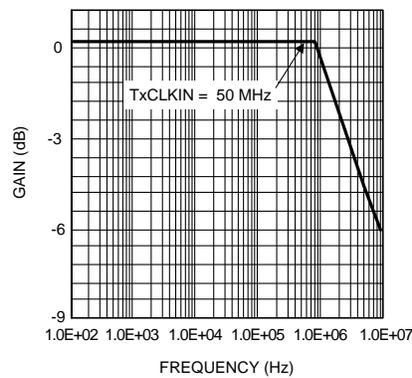
Figure 13. Serializer Jitter Transfer

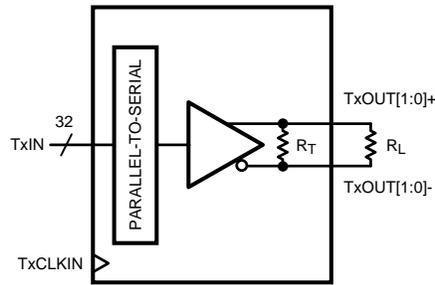Product Folder Links: *DS92LV3221 DS92LV3222*

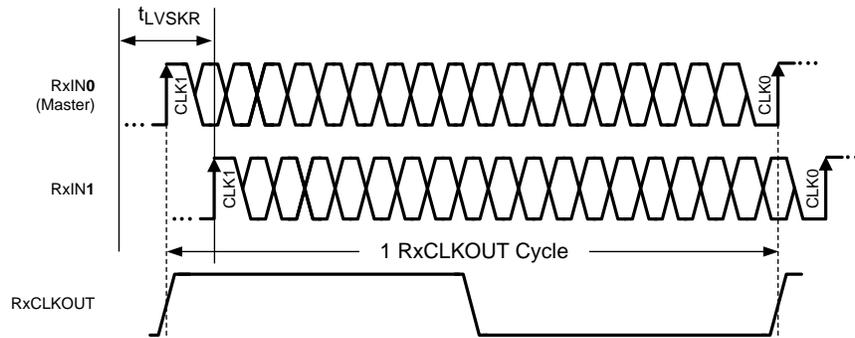**Figure 14. Serializer V$_{OD}$ Test Circuit Diagram**

Figure 15. LVDS Deserializer Input Skew

FUNCTIONAL DESCRIPTION

The DS92LV3221 Serializer (SER) and DS92LV3222 Deserializer (DES) chipset is a flexible SER/DES chipset that translates a 32-bit parallel LVCMOS data bus into 2 pairs of LVDS serial links with embedded clock. The DS92LV3221 serializes the 32-bit wide parallel LVCMOS word into two high-speed LVDS serial data streams with embedded clock, scrambles and DC Balances the data to support AC coupling and enhance signal quality. The DS92LV3222 receives the dual LVDS serial data streams and converts it back into a 32-bit wide parallel data with a recovered clock. The dual LVDS serial data stream reduces cable size, the number of connectors, and eases skew concerns.

Parallel clocks between 20 MHz to 50 MHz are supported. The embedded clock LVDS serial streams have an effective data payload of 640 Mbps (20MHz x 32-bit) to 1.6 Gbps (50MHz x 32- bit). The SER/DES chipset is designed to transmit data over long distances through standard twisted pair (TWP) cables. The differential inputs and outputs are internally terminated with 100 ohm resistors to provide source and load termination, minimize stub length, to reduce component count and further minimize board space.

The DES can attain lock to a data stream without the use of a separate reference clock source; greatly simplifying system complexity and reducing overall cost. The DES synchronizes to the SER regardless of data pattern, delivering true automatic "plug-and-lock" performance. It will lock to the incoming serial stream without the need of special training patterns or special sync characters. The DES recovers the clock and data by extracting the embedded clock information, deskews the serial data channels and then deserializes the data. The DES also monitors the incoming clock information, determines lock status, and asserts the LOCK output high when lock occurs. In addition the DES also supports an optional AT-SPEED BIST (Built In Self Test) mode, BIST error flag, and LOCK status reporting pin. The SER and the DES have a power down control signal to enable efficient operation in various applications.

DESKEW AND CHANNEL ALIGNMENT

The DES automatically provides a clock alignment and deskew function without the need for any special training patterns. During the locking phase, the embedded clock information is recovered on all channels and the serial links are internally synchronized, de-skewed, and auto aligned. The internal CDR circuitry will dynamically compensate for up to 0.4 times the parallel clock period of per channel phase skew (channel-to-channel) between the recovered clocks of the serial links. This provides skew phase tolerance from mismatches in interconnect wires such as PCB trace routing, cable pair-to-pair length differences, and connector imbalances.

DATA TRANSFER

After SER lock is established (SER PLL to TxCLKIN), the inputs TxIN0–TxIN31 are latched into the encoder block. Data is clocked into the SER by the TxCLKIN input. The edge of TxCLKIN used to strobe the data is selectable via the R_FB (SER) pin. R_FB (SER) high selects the rising edge for clocking data and low selects the falling edge. The SER outputs (TxOUT[1:0]+/-) are intended to drive a AC Coupled point-to-point connections.

The SER latches 32-bit parallel data bus and performs several operations to it. The 32-bit parallel data is internally encoded and sequentially transmitted over the two high-speed serial LVDS channels. For each serial channel, the SER transmits 20 bits of information per payload to the DES. This results in a per channel throughput of 400 Mbps to 1.0 Gbps (20 bits x clock rate).

When all of the DES channels obtain lock , the LOCK pin is driven high and synchronously delivers valid data and recovered clock on the output. The DES locks to the clock, uses it to generate multiple internal data strobes, and then drives the recovered clock to the RxCLKOUT pin. The recovered clock (RxCLKOUT) is synchronous to the data on the RxOUT[31:0] pins. While LOCK is high, data on RxOUT[31:0] is valid. Otherwise, RxOUT[31:0] is invalid. The polarity of the RxCLKOUT edge is controlled by its R_FB (DES) input. RxOUT[31:0], LOCK and RxCLKOUT outputs will each drive a maximum of 8 pF load. REN controls TRI-STATE for RxOUT0–RxOUT31 and the RxCLKOUT pin on the DES.

RESYNCHRONIZATION

In the absence of data transitions on one of the channels into the DES (e.g. a loss of the link), it will automatically try to resynchronize and re-establish lock using the standard lock sequence on the master channel (Channel 0). For example, if the embedded clock is not detected one time in succession on either of the serial links, the LOCK pin is driven low. The DES then monitors the master channel for lock, once that is obtained, the second channel is locked and aligned. The logic state of the LOCK signal indicates whether the data on RxOUT is valid; when it is high, the data is valid. The system may monitor the LOCK pin to determine whether data on the RxOUT is valid.

POWERDOWN

The Powerdown state is a low power sleep mode that the SER and DES may use to reduce power when no data is being transferred. The respective PDB pins are used to set each device into power down mode, which reduces supply current into the µA range. The SER enters Powerdown when the SER PDB pin is driven low. In Powerdown, the PLL stops and the outputs go into TRI-STATE, disabling load current and reducing current supply. To exit Powerdown, SER PDB must be driven high. When the SER exits Powerdown, its PLL must lock to TxCLKIN before it is ready for sending data to the DES. The system must then allow time for the DES to lock before data can be recovered.

The DES enters Powerdown mode when DES PDB is driven low. In Powerdown mode, the PLL's stop and the outputs enter TRI-STATE. To bring the DES block out of the Powerdown state, the system drives DES PDB high. Both the SER and DES must relock before data can be transferred from Host and received by the Target. The DES will startup and assert LOCK high when it is locked to the embedded clocks. See also Figure 11.

TRI-STATE

For the SER, TRI-STATE is entered when the SER PDB pin is driven low. This will TRI-STATE the driver output pins on TxOUT[1:0]+/-.

When you drive the REN or DES PDB pin low, the DES output pins (RxOUT[31:0]) and RxCLKOUT will enter TRI-STATE. The LOCK output remains active, reflecting the state of the PLL. The DES input pins are high impedance during receiver Powerdown (DES PDB low) and power-off (VDD = 0V). See also Figure 11.

TRANSMIT PARALLEL DATA AND CONTROL INPUTS

The DS92LV3221 operates on a core supply voltage of 3.3V with an optional digital supply voltage for 1.8V, low-swing, input support. The SER single-ended (32-bit parallel data and control inputs) pins are 1.8V and 3.3V LVCMOS logic level compatible and is configured through the IOVDD input supply rail. If 1.8V is required, the IOVDD pin must be connected to a 1.8V supply rail. Also when power is applied to the transmitter, IOVDD pin must be applied before or simultaneously with other power supply pins (3.3V). If 1.8V input swing is not required, this pin should be tied to the common 3.3V rail. During normal operation, the voltage level on the IOVDD pins must not change.

PRE-EMPHASIS

The SER LVDS Line Driver features a Pre-Emphasis function used to compensate for extra long or lossy transmission media. The same amount of Pre-Emphasis is applied on all of the differential output channels. Cable drive is enhanced with a user selectable Pre-Emphasis feature that provides additional output current during transitions to counteract cable loading effects. The transmission distance will be limited by the loss characteristics and quality of the media.

To enable the Pre-Emphasis function, the "PRE" pin requires one external resistor (Rpre) to VSS (GND) in order to set the pre-emphasized current level. Options include:
1. Normal Output (no Pre-emphasis) – Leave the PRE pin open, include an R pad, do not populate.
2. Enhanced Output (Pre-emphasis enabled) – connect a resistor on the PRE pin to Vss.

Values of the Rpre Resistor should be between 12K Ohm and 100K Ohm. Values less than 6K Ohm should not be used. The amount of Pre-Emphasis for a given media will depend on the transmission distance and Fmax of the application. In general, too much Pre-Emphasis can cause over or undershoot at the receiver input pins. This can result in excessive noise, crosstalk, reduced Fmax, and increased power dissipation. For shorter cables or distances, Pre-Emphasis is typically not be required. Signal quality measurements should be made at the end of the application cable to confirm the proper amount of Pre-Emphasis for the specific application.

The Pre-Emphasis circuit increases the drive current to I = 48 / (R_{PRE}). For example if R_{PRE} = 15 kOhms, then the current is increased by an additional 3.2 mA. To calculate the expected increase in V_{OD}, multiply the increase in current by 50 ohms. So for the case of R_{PRE} = 15 kOhms, the boost to V_{OD} would be 3.2 mA x 50 Ohms = 160 mV. The duration of the current is controlled to one bit by time. If more than one bit value is repeated in the next cycle(s), the Pre-Emphasis current is turned off (back to the normal output current level) for the next bit(s). To boost high frequency data and pre-equalize teh data patternreduce ISI (Inter-Symbol Interference) improving the resulting eye pattern.

V_{OD} SELECT

The SER Line Driver Differential Output Voltage (V_{OD}) magnitude is selectable. Two levels are provided and are selected by the VSEL pin. When this pin is LOW, normal output levels are obtained. For most application set the VSEL pin LOW. When this pin is HIGH, the output current is increased to double the V_{OD} level. Use this setting only for extra long cables or high-loss interconnects.

Table 1. V_{OD} Control

VSEL Pin Setting	Effect
LOW	Small V_{OD}, typ 440 mV_{P-P}
HIGH	Large V_{OD}, typ 850 mV_{P-P}

SERIAL INTERFACE

The serial links between the DS92LV3221 and the DS92LV3222 are intended for a balanced 100 Ohm interconnects. The links **must** be configured as an AC coupled interface.

The SER and DES support AC-coupled interconnects through an integrated DC balanced encoding/decoding scheme. An external AC coupling capacitors must be placed, in series, in the LVDS signal path. The DES input stage is designed for AC-coupling by providing a built-in AC bias network which sets the internal common mode voltage (VCM) to +1.8V.

For the high-speed LVDS transmission, small footprint packages should be used for the AC coupling capacitors. This will help minimize degradation of signal quality due to package parasitics. NPO class 1 or X7R class 2 type capacitors are recommended. 50 WVDC should be the minimum used for best system-level ESD performance. The most common used capacitor value for the interface is 100 nF (0.1 uF) capacitor. One set of capacitors may be used for isolation. Two sets (both ends) may also be used for maximum isolation of both the SER and DES from cable faults.

The DS92LV3221 and the DS92LV3222 differential I/O's are internally terminated with 100 Ohm resistance between the inverting and non-inverting pins and do not require external termination. The internal resistance value will be between 90 ohm and 130 ohm. The integrated terminations improve signal integrity, reduce stub lengths, and decrease the external component count resulting in space savings.

AT-SPEED BIST FEATURE

The DS92LV3221/ DS92LV3222 serial link is equipped with built-in self-test (BIST) capability to support both system manufacturing and field diagnostics. BIST mode is intended to check the entire high-speed serial interface at full link-speed without the use of specialized and expensive test equipment. This feature provides a simple method for a system host to perform diagnostic testing of both SER and DES. The BIST function is easily configured through the SER BISTEN pin. When the BIST mode is activated, the SER generates a PRBS (pseudo-random bit sequence) pattern (2^7-1). This pattern traverses each lane to the DES input. The DS92LV3222 includes an on-chip PRBS pattern verification circuit that checks the data pattern for bit errors and reports any errors on the data output pins of the DES.

The AT-Speed BIST feature is enabled by setting the BISTEN to High on SER. The BISTEN input must be High or Low for 4 or more TxCLKIN clock cycles in order to activate or deactivate the BIST mode. An input clock signal for the Serializer TxCLKIN must also be applied during the entire BIST operation. Once BIST is enabled, all the Serializer data inputs (TxIN[31:0]) are ignored and the DES outputs (RxOUT[31:0]) are not available. Next, the internal test pattern generator for each channel starts transmission of the BIST pattern from SER to DES. The DES BIST mode will be automatically activated by this sequence. A maximum of 128 consecutives clock symbols on DS92LV3222 DES is needed to detect BIST enable function. The BIST is implemented with independent transmit and receive paths for the two serial links. Each channel on the DES will be individually compared against the expected bit sequence of the BIST pattern.
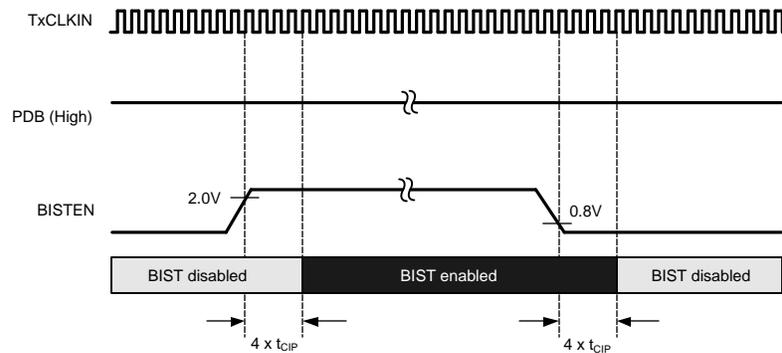
Figure 16. BIST Test Enabled/Disabled

Under the BIST mode, the DES parallel outputs on RxOUT[31:0] are multiplexed to represent BIST status indicators. The pass/fail status of the BIST is represented by a Pass flag along with an Error counter. The Pass flag output is designated on DES RxOUT0 for Channel 0, and RxOUT16 for Channel 1. The DES's PLL must first be locked to ensure the Pass status is valid. The output Pass status pin will stay LOW and then transition to High once $44*10^6$ symbols are achieved across each of the respective transmission links. The total time duration of the test is defined by the following: $44*10^6$ x tCIP . After the Pass output flags reach a HIGH state, it will not drop to LOW even if subsequent bit errors occurred after the BIST duration period. Errors will be reported if the input test pattern comparison does not match. If an error (miss-compare) occurs, the status bit is latched on RxOUT[7:1] for Channel 0, and RxOUT[23:17] for Channel 1; reflecting the number of errors detected. Whenever a data bit contains an error, the Error counter bit output for that corresponding channel goes HIGH. Each counter for the serial link utilizes a 7-bit counter to store the number of errors detected (0 to 127 max).
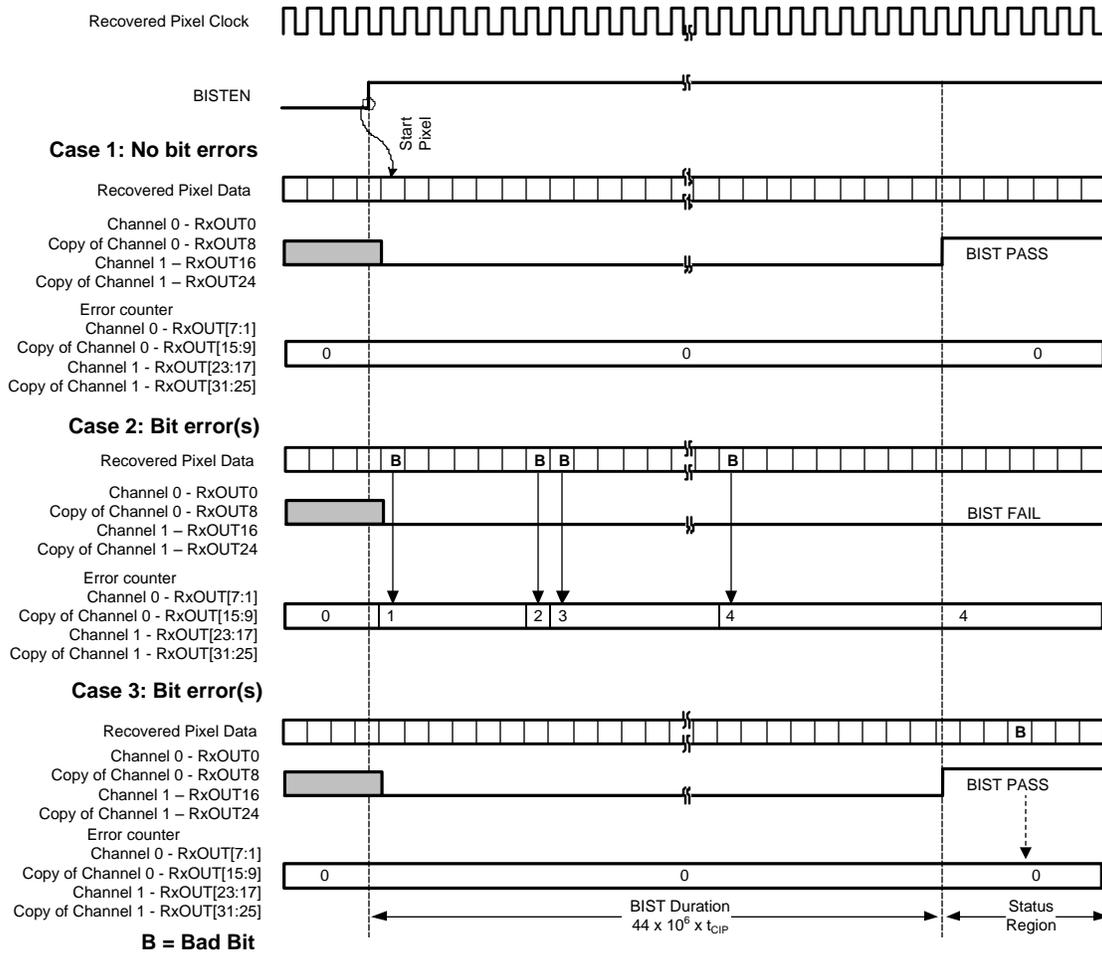
Product Folder Links: *DS92LV3221 DS92LV3222*

**Figure 17. BIST Diagram for Different Bit Error Cases**

TYPICAL APPLICATION CONNECTION

Figure 18 shows a typical application of the DS92LV3221 Serializer (SER). The differential outputs utilize 100nF coupling capacitors to the serial lines. Bypass capacitors are placed near the power supply pins. A system GPO (General Purpose Output) controls the PDB and BISTEN pins. In this application the R_FB (SER) pin is tied Low to latch data on the falling edge of the TxCLKIN. In this application the link is short, therefore the VSEL pin is tied LOW for the standard output swing level. The Pre-emphasis input utilizes a resistor to ground to set the amount of pre-emphasis desired by the application.

Configuration pins for the typical application are shown for SER:

- PDB – Power Down Control Input – Connect to host or tie HIGH (always ON)
- BISTEN – Mode Input - tie LOW if BIST mode is not used, or connect to host
- VSEL – tie LOW for normal VOD (application dependant)
- PRE – Leave open if not required (have a R pad option on PCB)
- RSVD1 & RSVD2 – tie LOW

There are eight power pins for the device. These may be bussed together on a common 3.3V plane (3.3V LVCMOS I/O interface). If 1.8V input swing level for parallel data and control pins are required, connect the IOVDD pin to 1.8V. At a minimum, eight 0.1uF capacitors should be used for local bypassing.
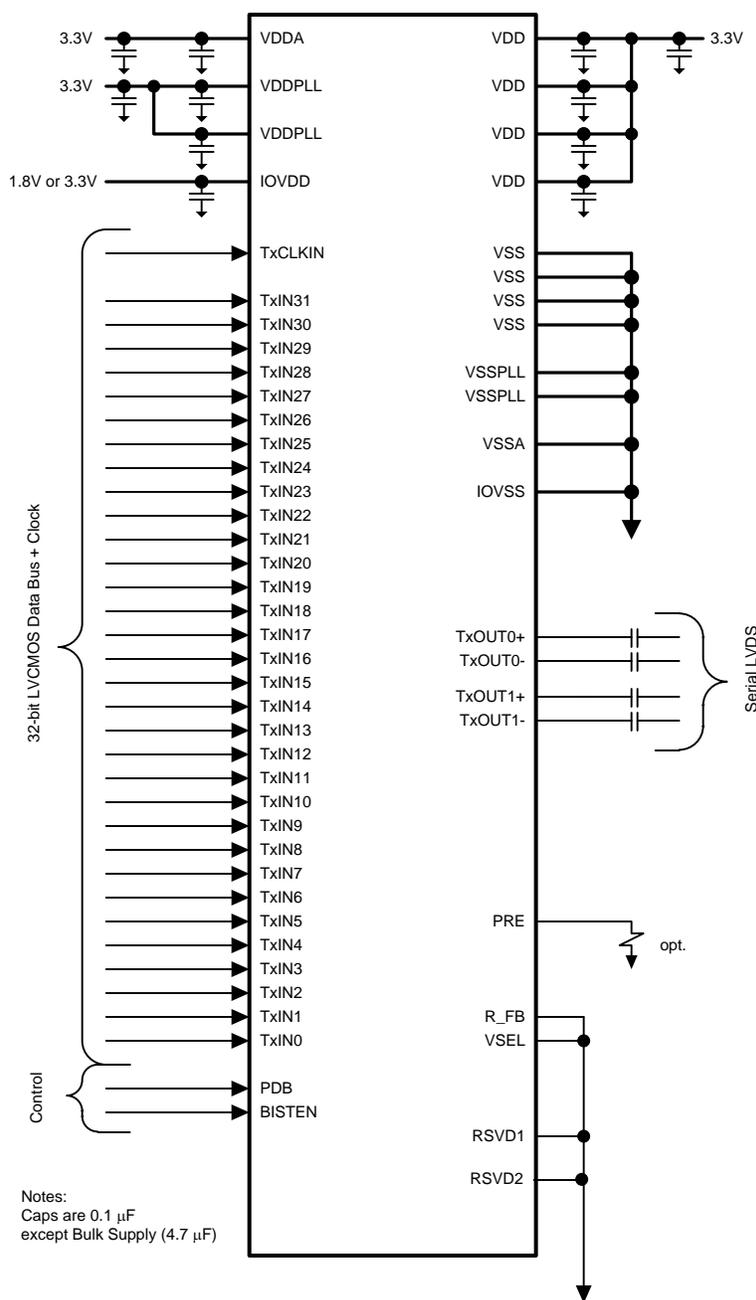
Figure 18. DS92LV3221 Typical Connection Diagram

Figure 19 shows a typical application of the DS92LV3222 Deserializer (DES). The differential inputs utilize 100nF coupling capacitors in the serial lines. Bypass capacitors are placed near the power supply pins. A system GPO (General Purpose Output) controls the PDB pin. In this application the R_FB (DES) pin is tied Low to strobe the data on the falling edge of the RxCLKOUT. The REN signal is not used and is tied High also.

Configuration pins for the typical application are shown for DES:

- PDB – Power Down Control Input – Connect to host or tie HIGH
- REN – tie HIGH if not used (used to MUX two DES to one target device)
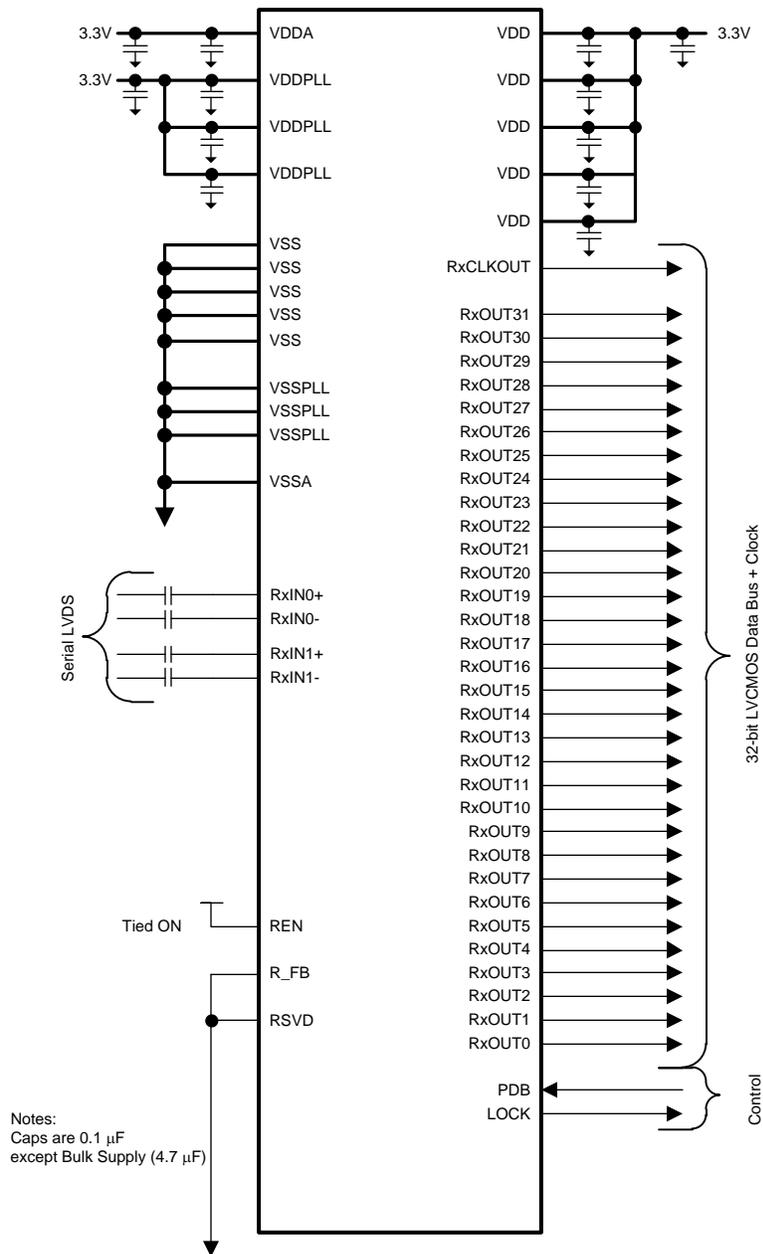- RSVD – tie LOW

Figure 19. DS92LV3222 Typical Connection Diagram

APPLICATIONS INFORMATION

TRANSMISSION MEDIA

The SER and DES are used in AC-coupled point-to-point configurations, through a PCB trace, or through twisted pair cables. Interconnect for LVDS typically has a differential impedance of 100 Ohms. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. In most applications that involve cables, the transmission distance will be determined on data rates involved, acceptable bit error rate and transmission medium.

PCB LAYOUT AND POWER SYSTEM CONSIDERATIONS

Circuit board layout and stack-up for the LVDS SER/DES devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 uF to 0.1 uF. Tantalum capacitors may be in the 2.2 uF to 10 uF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommended at the point of power entry. This is typically in the 50uF to 100uF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with vias on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz range. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely-coupled differential lines of 100 Ohms are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise will appear as common mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

PLUG AND GO

The Serializer and Deserializer devices support hot plugging of the serial interconnect. The automatic receiver lock to random data "plug & go" capability allows the DS92LV3222 to obtain lock to the active data stream during a live insertion event.

LVDS INTERCONNECT GUIDELINES

For full details, see the *Channel-Link PCB and Interconnect Design-In Guidelines* (literature number SNLA008) and the *Transmission Line RAPIDESIGNER Operation and Applications Guide* (literature number SNLA035).

- Use 100 Ohm coupled differential pairs
- Use the S/2S/3S rule in spacings
  - S = space between the pair
  - 2S = space between pairs
  - 3S = space to LVCMOS signal
- Minimize the number of vias
- Use differential connectors when operating above 500 Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair
- Terminate as close to the TX outputs and RX inputs as possible

Additional general guidance can be found in the *LVDS Owner's Manual* (literature number SNLA187), which is available in PDF format from the TI LVDS & CML Solutions web site.

The waveforms below illustrate the typical performance of the DS92LV3221. The SER was given a PCLK and configured as described below each picture. In all of the pictures the SER was configured with BISTEN pin set to logic HIGH. Each waveform was taken by using a high impedance low capacitance differential probe to probe across a 100 ohm differential termination resistor within one inch of TxOUT0+/-.
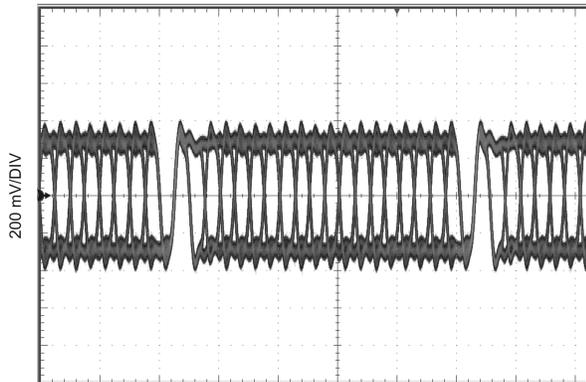
**Figure 20. Serial Output, 50 MHz, VSEL = H,
No Pre-Emphasis**
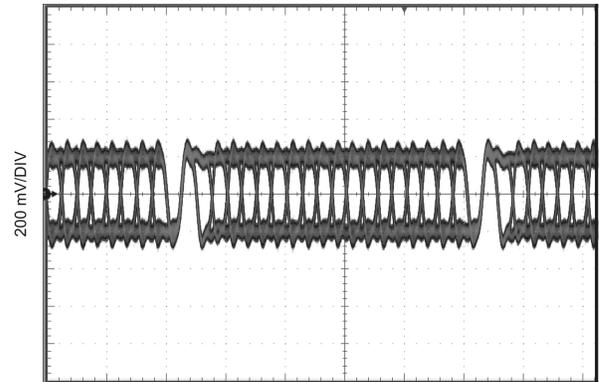
**Figure 21. Serial Output, 50 MHz, VSEL = L,
No Pre-Emphasis**

Product Folder Links: *DS92LV3221 DS92LV3222*

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C   **Page**

Product Folder Links: *DS92LV3221 DS92LV3222*

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS92LV3221TVS/NOPB	ACTIVE	TQFP	PAG	64	160	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	DS92LV3221 TVS	Samples
DS92LV3221TVSX/NOPB	ACTIVE	TQFP	PAG	64	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	DS92LV3221 TVS	Samples
DS92LV3222TVS/NOPB	ACTIVE	TQFP	PAG	64	160	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	DS92LV3222 TVS	Samples
DS92LV3222TVSX/NOPB	ACTIVE	TQFP	PAG	64	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	DS92LV3222 TVS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS92LV3221TVSX/NOPB	TQFP	PAG	64	1000	330.0	24.4	13.0	13.0	1.45	16.0	24.0	Q2
DS92LV3222TVSX/NOPB	TQFP	PAG	64	1000	330.0	24.4	13.0	13.0	1.45	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS92LV3221TVSX/NOPB	TQFP	PAG	64	1000	367.0	367.0	45.0
DS92LV3222TVSX/NOPB	TQFP	PAG	64	1000	367.0	367.0	45.0

![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TRAY

L - Outer tray length without tabs

KO - Outer tray height

W - Outer tray width

P1 - Tray unit pocket pitch

CW - Measurement for tray edge (Y direction) to corner pocket center

CL - Measurement for tray edge (X direction) to corner pocket center
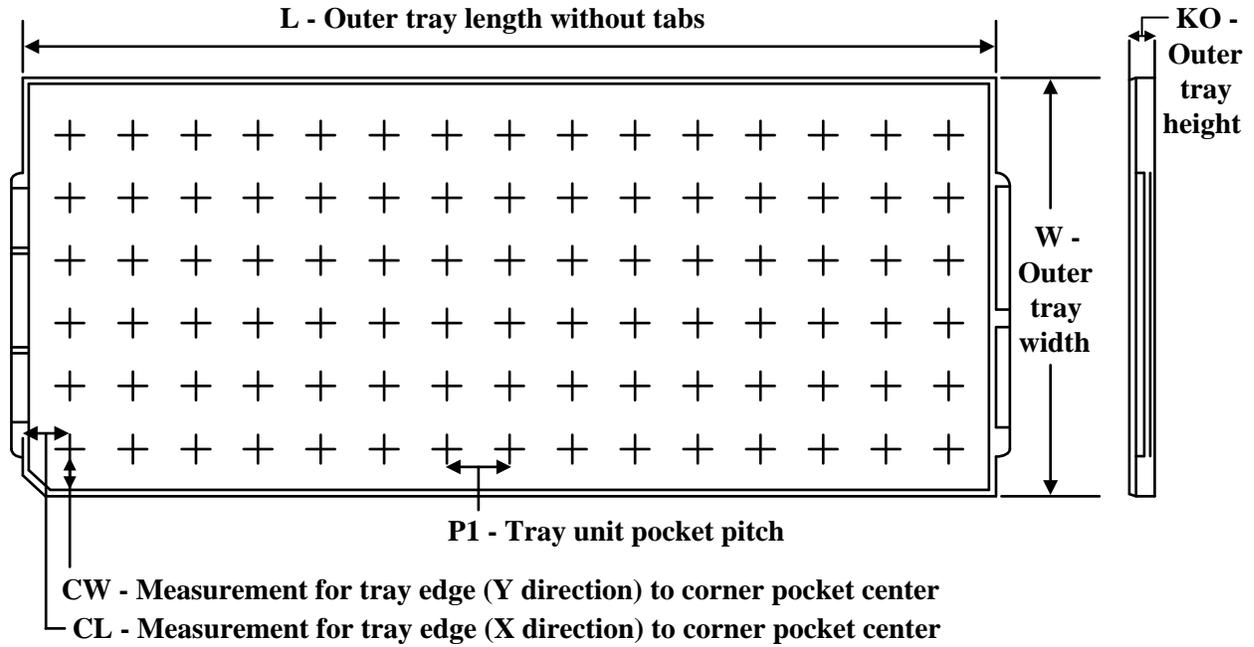
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DS92LV3221TVS/NOPB	PAG	TQFP	64	160	8 X 20	150	322.6	135.9	7620	15.2	13.1	13
DS92LV3222TVS/NOPB	PAG	TQFP	64	160	8 X 20	150	322.6	135.9	7620	15.2	13.1	13

PAG (S-PQFP-G64)   **PLASTIC QUAD FLATPACK**

4040282/C 11/96
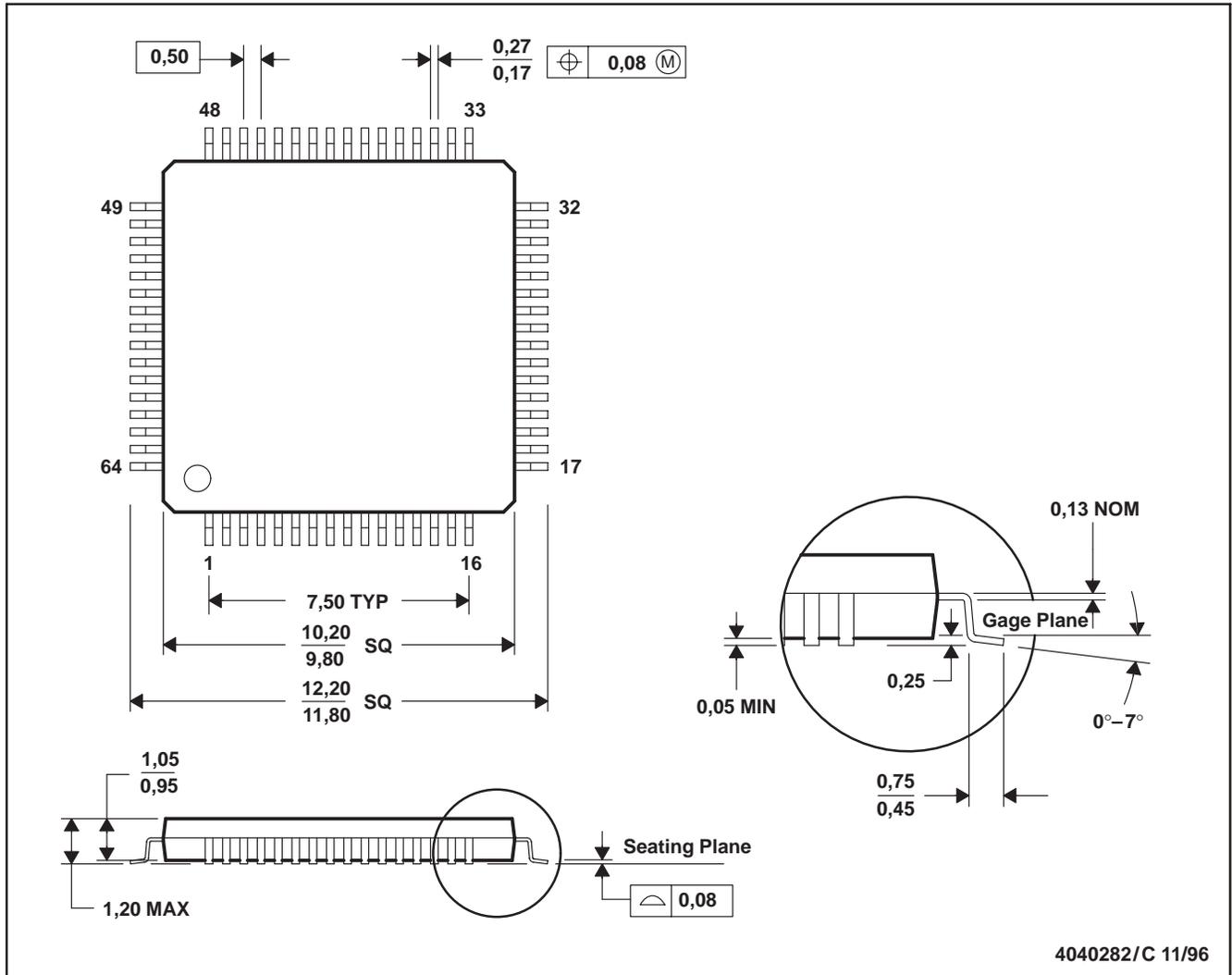
NOTES: A. All linear dimensions are in millimeters.
            B. This drawing is subject to change without notice.
            C. Falls within JEDEC MS-026

![Texas Instruments logo] **TEXAS INSTRUMENTS**

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

IMPORTANT NOTICE AND DISCLAIMER