INA317 微功耗 (50μA)、零漂移、轨至轨输出仪表放大器

1 特性

- 低失调电压：75μV（最大值），G ≥ 100
- 低温漂：0.3μV/°C，G ≥ 100
- 低噪声：50nV/√Hz，G ≥ 100
- 高共模抑制比 (CMRR)：100dB（最小值），G ≥ 10
- 低输入偏置电流：200pA（最大值）
- 电源范围：1.8V 至 5.5V
- 输入电压：(V–) 0.1V 至 (V+) –0.1V
- 电压范围：(V–) 0.05V 至 (V+) –0.05V
- 低静态电流：50μA
- 工作温度范围：-40°C 至 +125°C
- 已过滤射频干扰 (RFI) 的输入
- 8 引脚 VSSOP 封装

2 应用

- 桥式放大器
- 心电图 (ECG) 放大器
- 压力传感器
- 医疗仪表
- 便携式仪表
- 衡器
- 热电偶放大器
- 电阻式温度检测器 (RTD) 传感器放大器
- 数据采集

3 说明

INA317 是一款具备出色精度的低功耗精密仪表放大器。INA317 采用 3 种多功能运算放大器设计，尺寸小巧，功耗较低，适用于各种便携式 应用。

单个外部电阻器可根据行业标准增益等式 G = 1 + (100 kΩ / R_G) 的定义，设置 1 至 1000 范围内的任意增益。

该仪表放大器提供低失调电压（75μV，G ≥ 100）、出色的失调电压漂移
（0.3 μV/°C，G ≥ 100）和高共模抑制（G ≥ 10 时为 100dB）。INA317 采用低至 1.8V (±0.9V) 电压和 50μA 静态电流的电源供电，因而该器件适用于电池供电系统。INA317 器件采用自动校准技术确保广泛工业温度范围内的精度，可提供可扩展到直流的低噪声密度 (50nV/√Hz)。

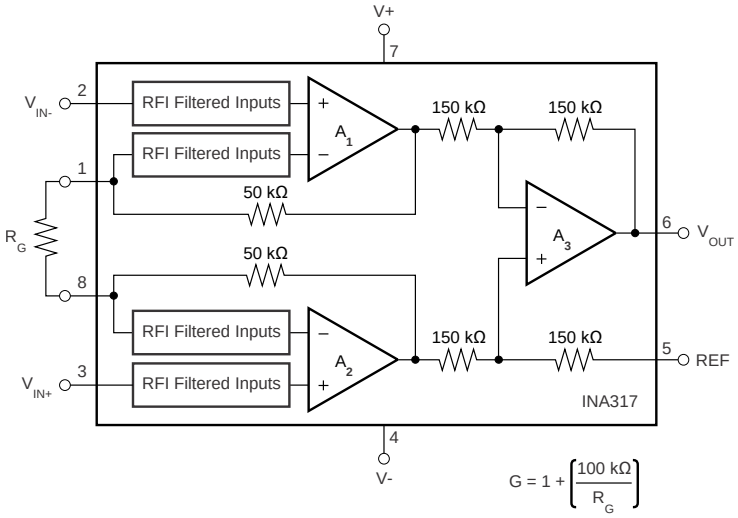
INA317 采用 8 引脚 VSSOP 表面贴装式封装，额定温度范围为 T_A = –40°C 至 +125°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
INA317	VSSOP (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2017 年 11 月	*	初始发行版

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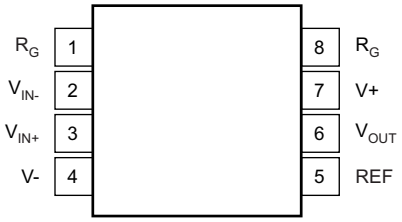
5 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
REF	5	I	Reference input. This pin must be driven by low impedance or connected to ground.
R_G	1, 8	—	Gain setting pins. For gains greater than 1, place a gain resistor between pins 1 and 8.
V_+	7	—	Positive supply
$V_–$	4	—	Negative supply
V_{IN+}	3	I	Positive input
$V_{IN–}$	2	I	Negative input
V_{OUT}	6	O	Output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply voltage	7		V
Analog input voltage (2)	(V–) – 0.3	(V+) + 0.3	V
Output short-circuit (3)	Continuous		
Operating temperature, T_A	–40	150	°C
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	
	Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VS	Supply voltage	1.8	5.5	V
	Specified temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC (1)		INA317 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	169.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	90.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	88.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

for V_S = 1.8 V to 5.5 V at T_A = 25°C, R_L = 10 kΩ, V_{REF} = V_S / 2, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT(1)						
V_{OSI}	Offset voltage, RTI(2)			±10 ±25 / G	±75 ±75 / G	µV
PSR		vs temperature, T_A = –40°C to 125°C			±0.3 ±0.5 / G	µV/°C
		vs power supply,1.8 V ≤ V_S ≤ 5.5 V		±1 ±5 / G	±5 ±15 / G	µV/V
		Long-term stability		See (3)		
	Turnon time to specified V_{OSI}	T_A = –40°C to 125°C		See *Typical Characteristics*		
	Impedance					
Z_{IN}	Differential			100 || 3		GΩ || pF
Z_{IN}	Common-mode			100 || 3		GΩ || pF
V_{CM}	Common-mode voltage range	V_O = 0 V	(V–) + 0.1		(V+) – 0.1	V
CMR	Common-mode rejection	DC to 60 Hz				
		V_{CM} = (V–) + 0.1 V to (V+) – 0.1 V, G = 1	80	90		dB
		V_{CM} = (V–) + 0.1 V to (V+) – 0.1 V, G = 10	100	110		dB
		V_{CM} = (V–) + 0.1 V to (V+) – 0.1 V, G = 100,	100	115		dB
		V_{CM} = (V–) + 0.1 V to (V+) – 0.1 V, G = 1000	100	115		dB
INPUT BIAS CURRENT						
I_B	Input bias current			±70	±200	pA
	vs temperature	T_A = –40°C to 125°C		See 图 26		pA/°C
I_{OS}	Input offset current			±50	±200	pA
	vs temperature	T_A = –40°C to 125°C		See 图 28		pA/°C
INPUT VOLTAGE NOISE						
e_{NI}	Input voltage noise	G = 100, R_S = 0 Ω, f = 10 Hz		50		nV/√Hz
		G = 100, R_S = 0 Ω, f = 100 Hz		50		nV/√Hz
		G = 100, R_S = 0 Ω, f = 1 kHz		50		nV/√Hz
		G = 100, R_S = 0 Ω, f = 0.1 Hz to 10 Hz		1		$µV_{PP}$
i_N	Input current noise	f = 10 Hz		100		fA/√Hz
		f = 0.1 Hz to 10 Hz		2		pA_{PP}
GAIN						
G	Gain equation			1 + (100 kΩ / R_G)		V/V
	Range of gain		1		1000	V/V
	Gain error	V_S = 5.5 V, (V–) + 100 mV ≤ V_O ≤ (V+) – 100 mV				
		G = 1		±0.01%	±0.1%	
		G = 10		±0.05%	±0.25%	
		G = 100		±0.07%	±0.25%	
		G = 1000		±0.25%	±0.5%	
	Gain vs temperature, G = 1	T_A = –40°C to 125°C		±1	±5	ppm/°C
	Gain vs temperature, G > 1(4)	T_A = –40°C to 125°C		±15	±50	ppm/°C
	Gain nonlinearity	V_S = 5.5 V, (V–) + 100 mV ≤ V_O ≤ (V+) – 100 mV				
	Gain nonlinearity, G = 1 to 1000	R_L = 10 kΩ		10		ppm
OUTPUT						
	Output voltage swing from rail	V_S = 5.5 V, R_L = 10 kΩ		See 图 29	50	mV
	Capacitive load drive			500		pF

(1) Total V_{OS}, referred-to-input = (V_{OSI}) + (V_{OSO} / G)
(2) RTI = Referred-to-input
(3) 300-hour life test at 150°C demonstrated randomly distributed variation of approximately 1 µV
(4) Does not include effects of external resistor R_G

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Electrical Characteristics (continued)

for V_S = 1.8 V to 5.5 V at T_A = 25°C, R_L = 10 kΩ, V_{REF} = V_S / 2, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SC}	Short-circuit current	Continuous to common		–40, 5		mA
FREQUENCY RESPONSE						
	Bandwidth, –3 dB	G = 1		150		kHz
		G = 10		35		kHz
		G = 100		3.5		kHz
		G = 1000		350		Hz
SR	Slew rate	V_S = 5 V, V_O = 4-V step, G = 1		0.16		V/µs
		V_S = 5 V, V_O = 4-V step, G = 100		0.05		V/µs
t_S	Settling time to 0.01%	V_{STEP} = 4 V, G = 1		50		µs
		V_{STEP} = 4 V, G = 100		400		µs
t_S	Settling time to 0.001%	V_{STEP} = 4 V, G = 1		60		µs
		V_{STEP} = 4 V, G = 100		500		µs
	Overload recovery	50% overdrive		75		µs
REFERENCE INPUT						
	R_{IN}			300		kΩ
	Voltage range		V–		V+	V
POWER SUPPLY						
	Voltage range	Single voltage range	1.8		5.5	V
		Dual voltage range	±0.9		±2.75	V
I_Q	Quiescent current vs temperature	V_{IN} = V_S / 2		50	75	µA
		T_A = –40°C to 125°C			80	µA
TEMPERATURE RANGE						
	Specified temperature range		–40		125	°C
	Operating temperature range		–40		150	°C

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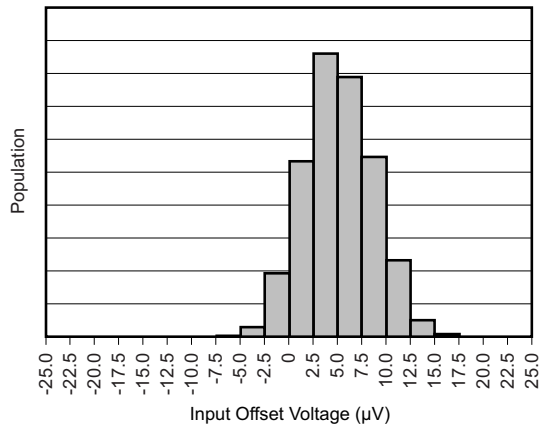
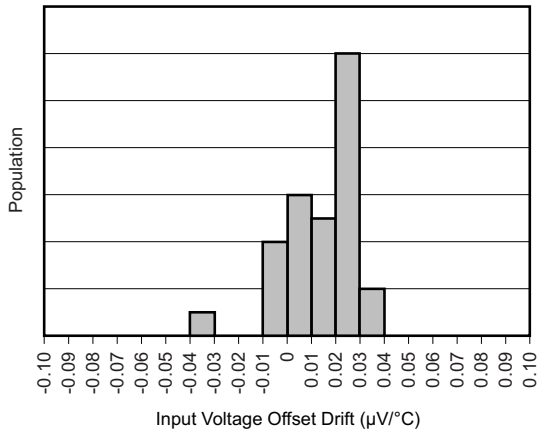
6.6 Typical Characteristics

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1, (unless otherwise noted)



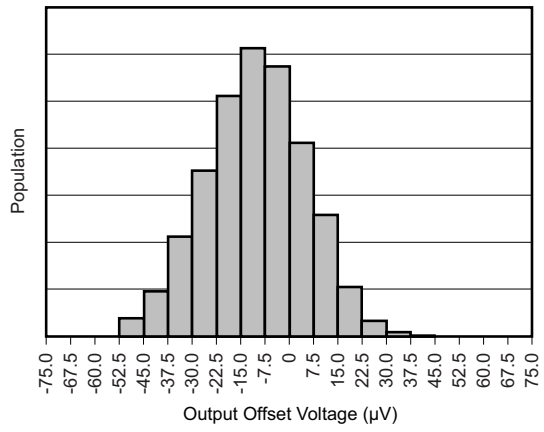
V_S = 5.5 V

图 1. Input Offset Voltage



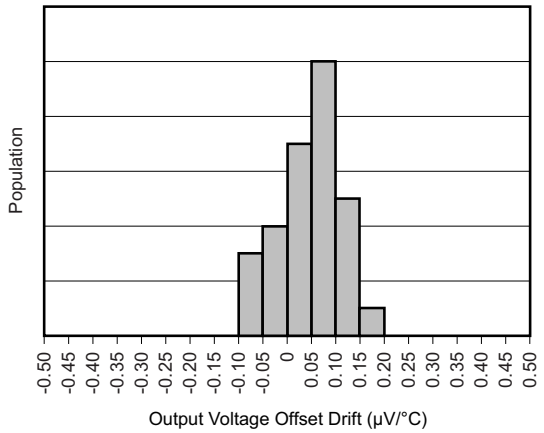
V_S = 5.5 V T_A = –40°C to +125°C

图 2. Input Voltage Offset Drift



V_S = 5.5 V

图 3. Output Offset Voltage



V_S = 5.5 V T_A = –40°C to +125°C

图 4. Output Voltage Offset Drift

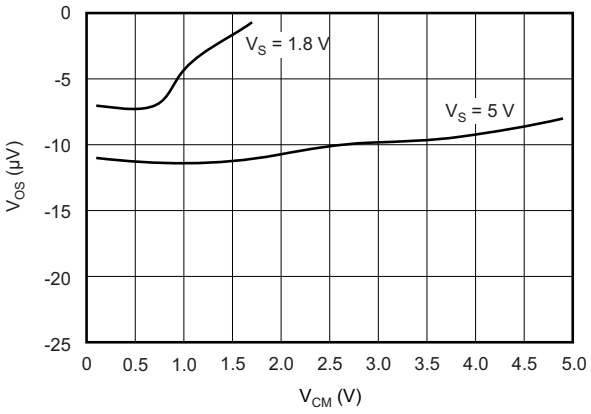
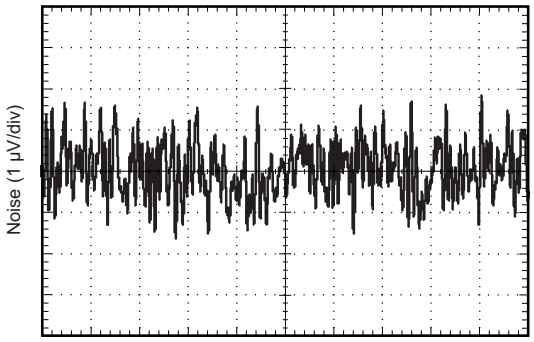


图 5. Offset Voltage vs Common-Mode Voltage



Gain = 1

图 6. 0.1-Hz to 10-Hz Noise

Typical Characteristics (接下页)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1, (unless otherwise noted)

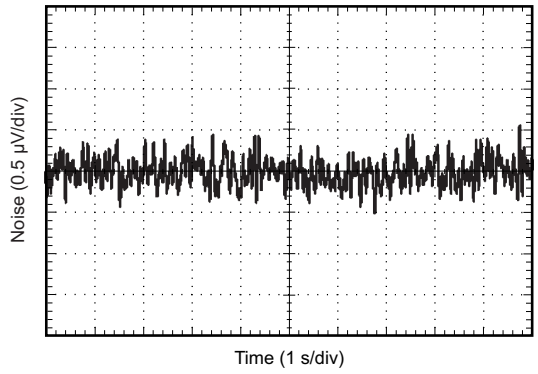


图 7. 0.1-Hz to 10-Hz Noise

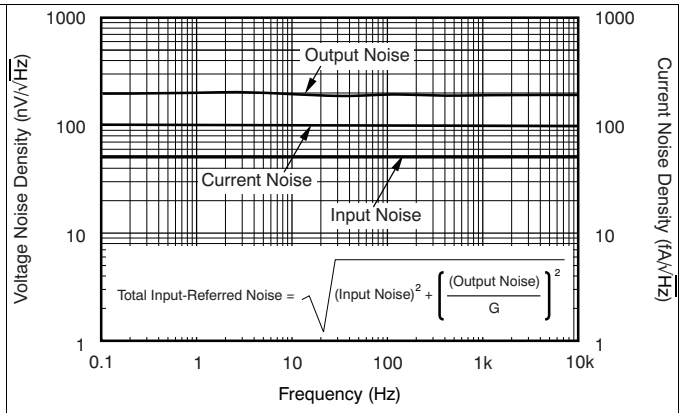


图 8. Spectral Noise Density

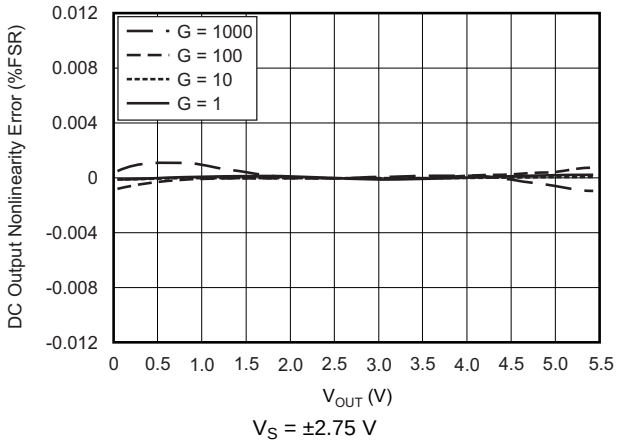


图 9. Nonlinearity Error

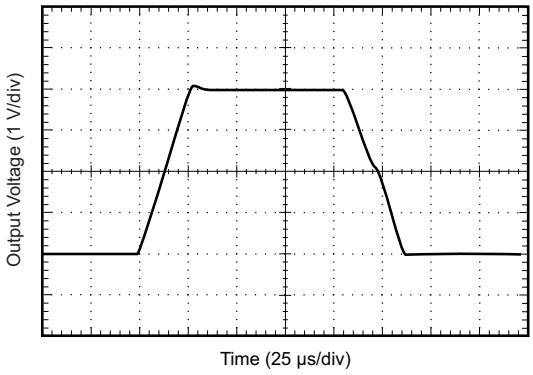


图 10. Large Signal Response

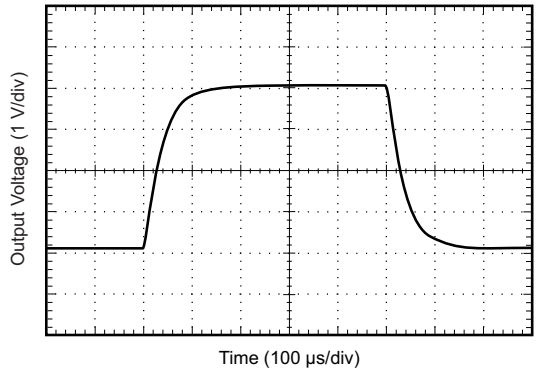


图 11. Large-Signal Step Response

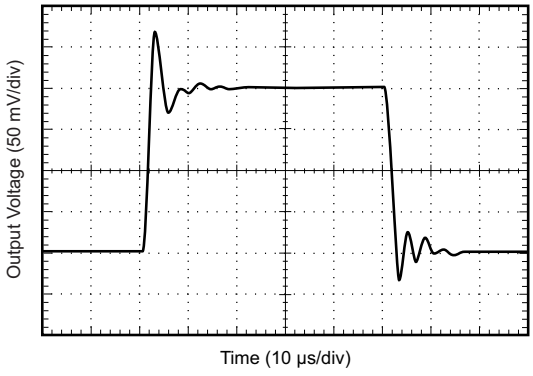


图 12. Small-Signal Step Response

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Typical Characteristics (接下页)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1, (unless otherwise noted)

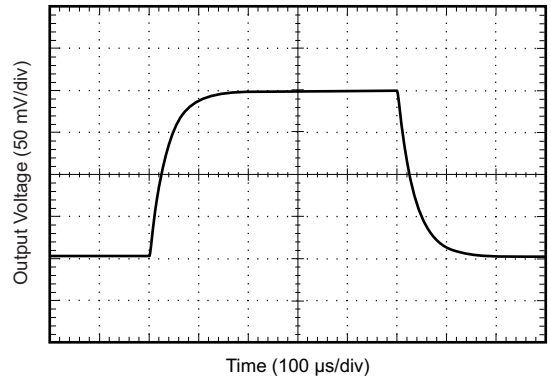


图 13. Small-Signal Step Response

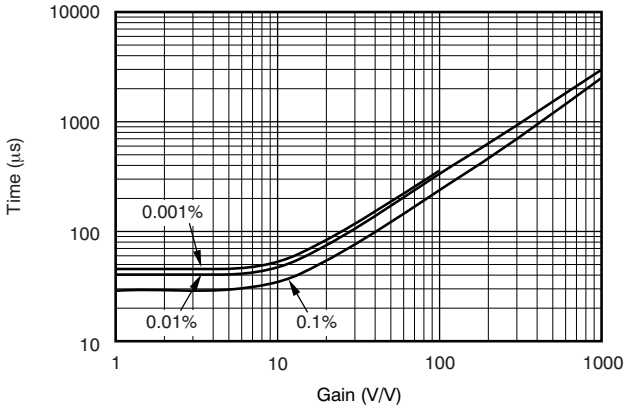


图 14. Settling Time vs Gain

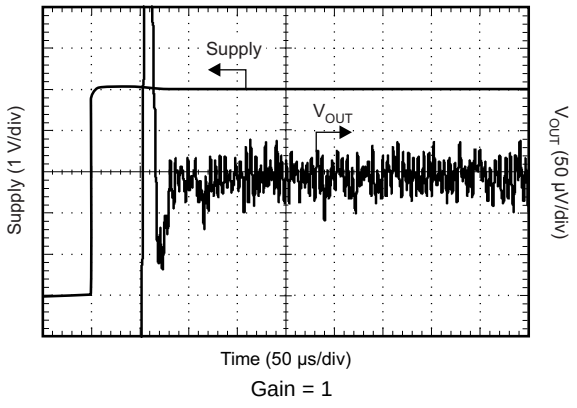


图 15. Start-Up Settling Time

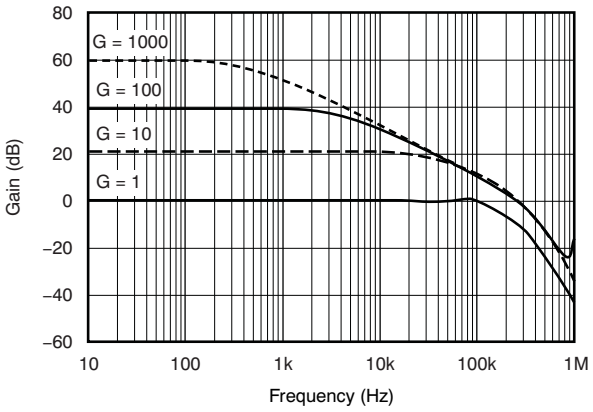


图 16. Gain vs Frequency

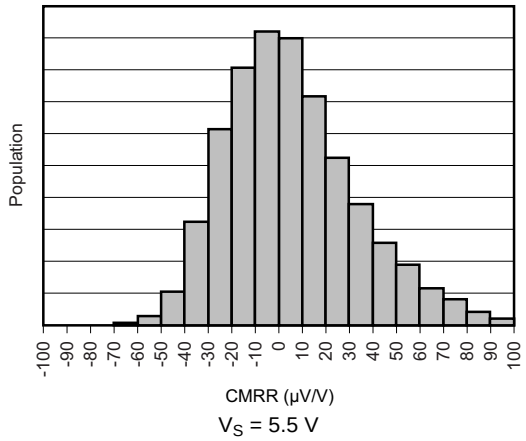


图 17. Common-Mode Rejection Ratio

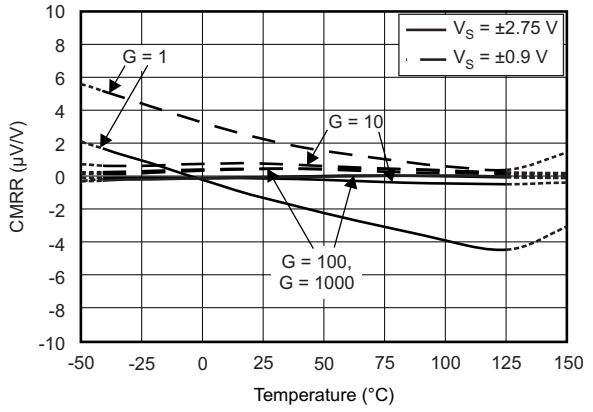


图 18. Common-Mode Rejection Ratio vs Temperature

Typical Characteristics (接下页)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1, (unless otherwise noted)

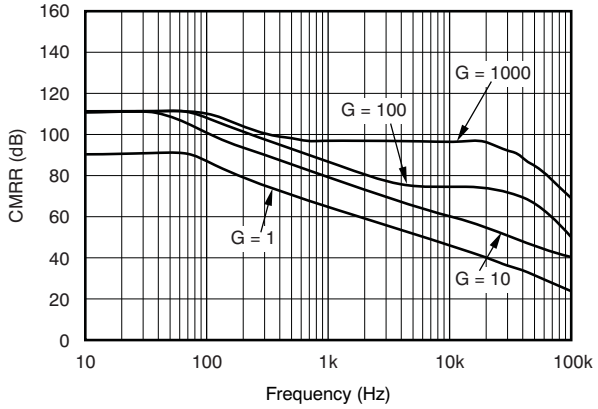
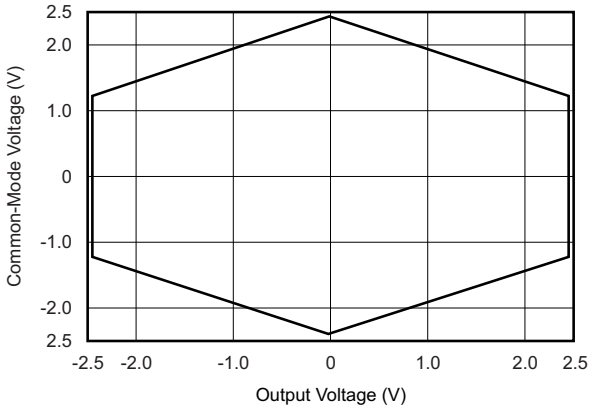
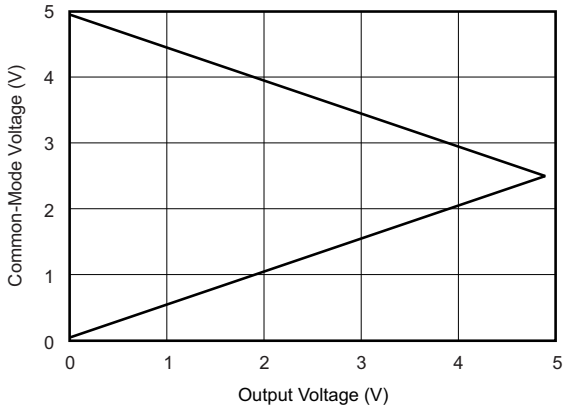


图 19. Common-Mode Rejection Ratio vs Frequency



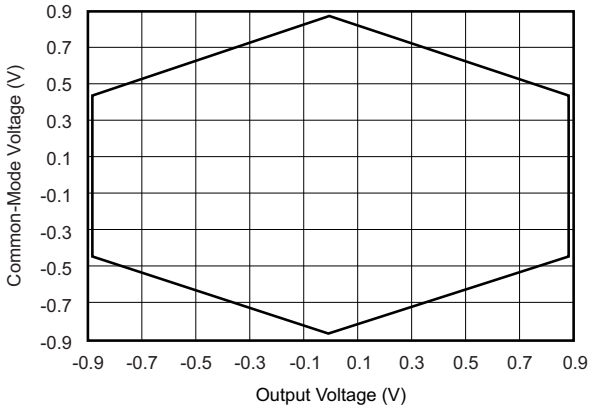
V_S = ±2.5 V V_{REF} = 0 All gains

图 20. Typical Common-Mode Range vs Output Voltage



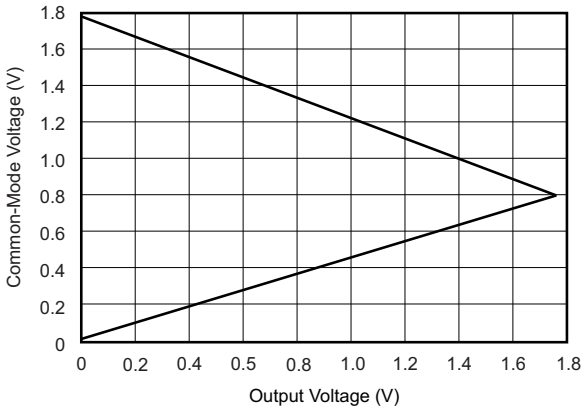
V_S = 5 V V_{REF} = 0 All gains

图 21. Typical Common-Mode Range vs Output Voltage



V_S = ±0.9 V V_{REF} = 0 All gains

图 22. Typical Common-Mode Range vs Output Voltage



V_S = 1.8 V V_{REF} = 0

图 23. Typical Common-Mode Range vs Output Voltage

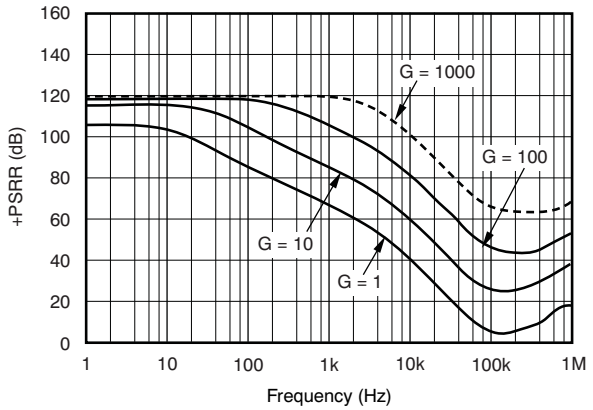


图 24. Positive Power-Supply Rejection Ratio

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Typical Characteristics (接下页)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1, (unless otherwise noted)

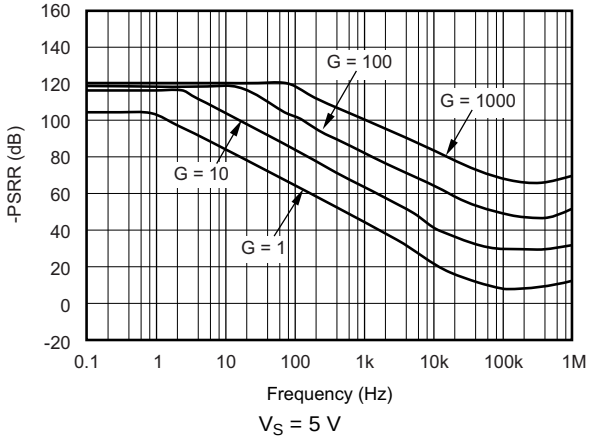

图 25. Negative Power-Supply Rejection Ratio

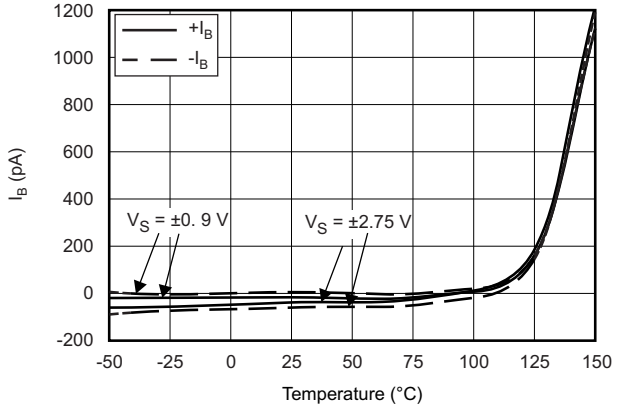

图 26. Input Bias Current vs Temperature

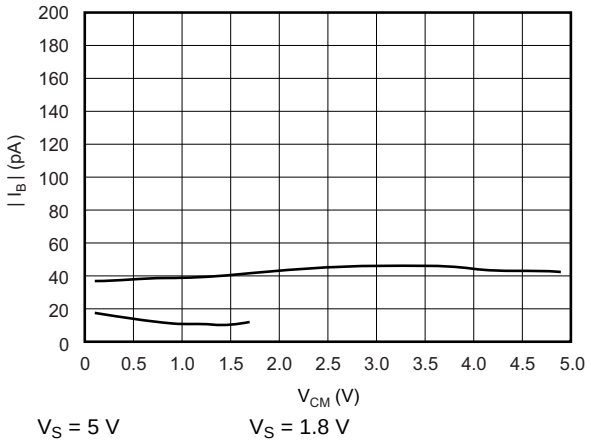

图 27. Input Bias Current vs Common-Mode Voltage

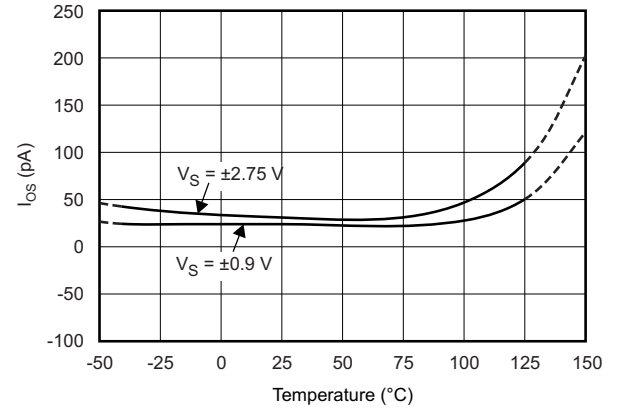

图 28. Input Offset Current vs Temperature

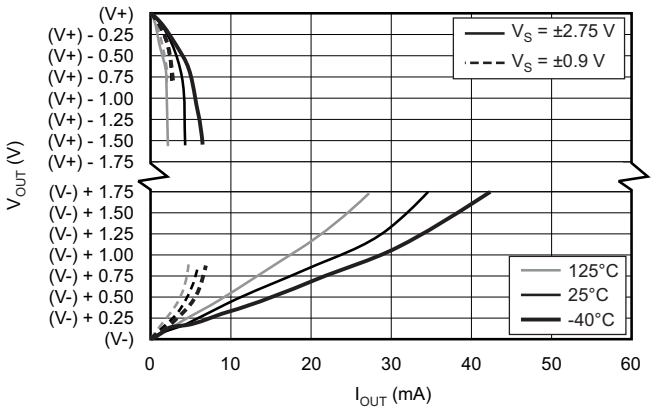

图 29. Output Voltage Swing vs Output Current

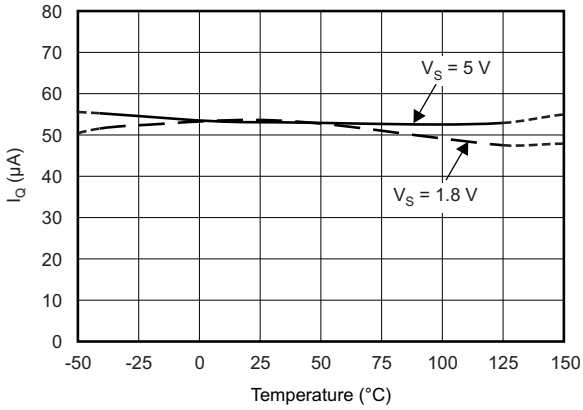

图 30. Quiescent Current vs Temperature

Typical Characteristics (接下页)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1, (unless otherwise noted)

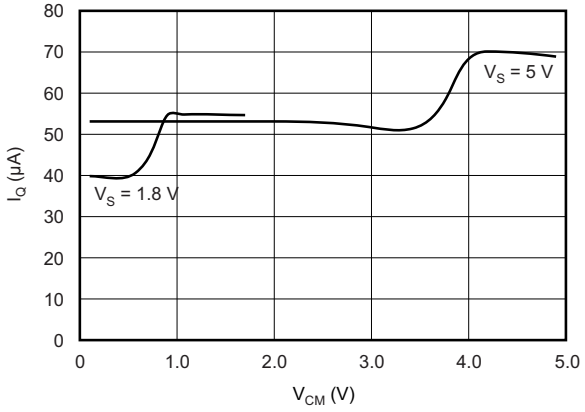

图 31. Quiescent Current vs Common-Mode Voltage

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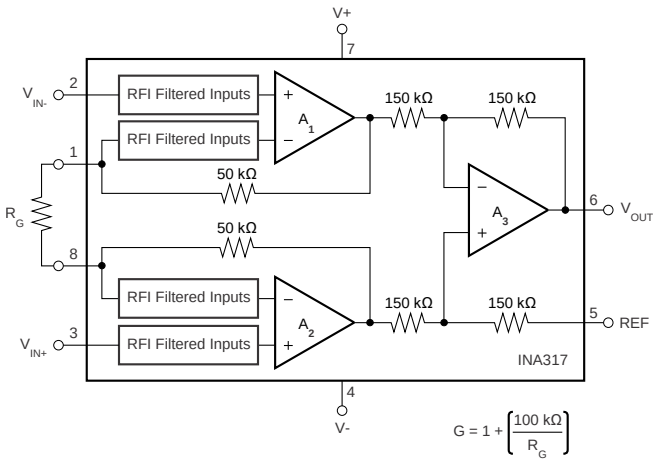
7 Detailed Description

7.1 Overview

The INA317 is a monolithic instrumentation amplifier (INA) based on the precision zero-drift OPA333 (operational amplifier) core. The INA317 integrates laser-trimmed resistors to ensure excellent common-mode rejection and low gain error. The combination of the zero-drift amplifier core and the precision resistors allows this device to achieve outstanding DC precision and is designed for 3.3-V and 5-V industrial applications.

7.2 Functional Block Diagram



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7.3 Feature Description

The INA317 is a low-power, zero-drift instrumentation amplifier that offers accuracy. The versatile three-operational-amplifier design and small size makes the amplifier designed for a wide range of applications. Zero-drift chopper circuitry provides DC specifications. A single external resistor sets any gain from 1 to 10,000. The INA317 is laser trimmed for high common-mode rejection (100 dB at G ≥ 100). Typically, the INA317 operates with power supplies as low as 1.8 V and quiescent current of 50 µA.

7.4 Device Functional Modes

7.4.1 Internal Offset Correction

INA317 internal operational amplifiers use an autocalibration technique with a time-continuous 350-kHz operational amplifier in the signal path. The amplifier is zero-corrected every 8 µs using a proprietary technique. Upon power up, the amplifier requires approximately 100 µs to achieve specified VOS accuracy. This design has no aliasing or flicker noise.

7.4.2 Input Common-Mode Range

The linear input voltage range of the input circuitry of the INA317 is from approximately 0.1 V below the positive supply voltage to 0.1 V above the negative supply. However, as a differential input voltage causes the output voltage to increase, the output voltage swing of amplifiers A1 and A2 limits the linear input range. As a result, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior depends on supply voltage; see 图 20.

Input overload conditions can produce an output voltage that appears normal. For example, if an input overload condition drives the input amplifiers to the respective positive output swing limit, the difference voltage measured by the output amplifier is approximately zero. The output of the INA317 is approximately 0 V even though the inputs are overloaded.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The INA317 measures small differential voltage with high common-mode voltage that develops between the noninverting and inverting input. The high input impedance makes the INA317 designed for a wide range of applications. The ability to set the reference pin to adjust the functionality of the output signal offers additional flexibility that is practical for multiple configurations.

8.2 Typical Application

图 32 shows the basic connections required for operation of the INA317 device. Good layout practice mandates the use of bypass capacitors placed close to the device pins as shown.

The output of the INA317 device is referred to the output reference (REF) pin, which is normally grounded. This connection must be low-impedance to ensure good common-mode rejection. Although 15 Ω or less of stray resistance is tolerated while maintaining specified CMRR, small stray resistances of tens of ohms in series with the REF pin causes noticeable degradation in CMRR.

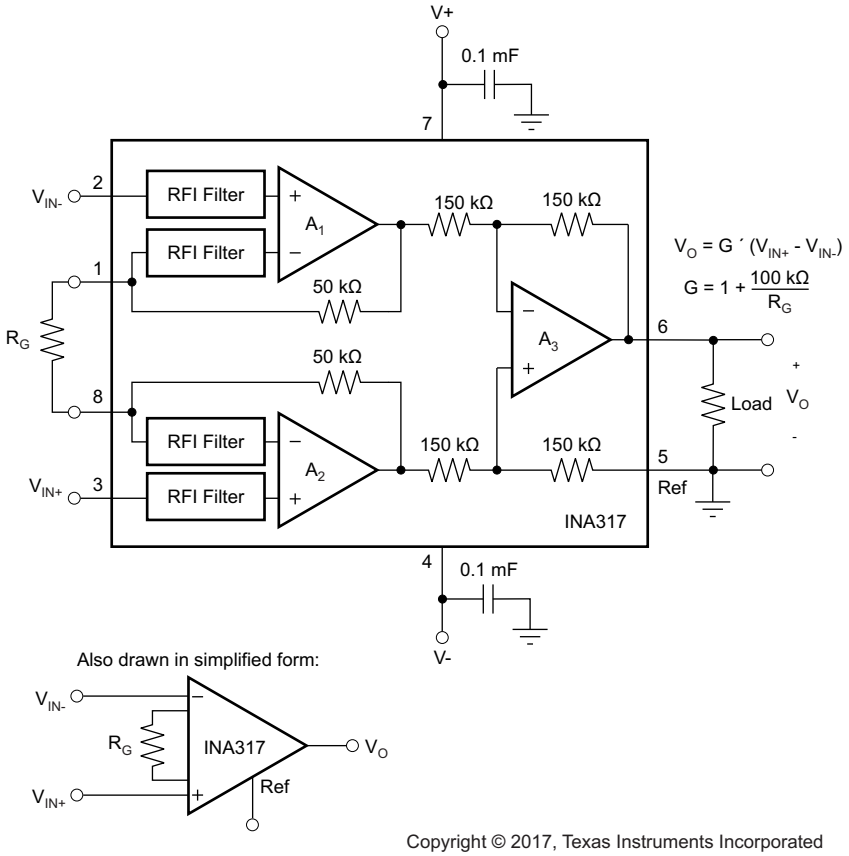

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图 32. Basic Connections

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Typical Application (接下页)

8.2.1 Design Requirements

The device is configured to monitor the input differential voltage when the gain of the external resistor R_G sets the input signal. The output signal references to the REF pin. The most common application is where the output is referenced to ground when no input signal is present by connecting the REF pin to ground. When the input signal increases, the output voltage at the OUT pin increases.

8.2.2 Detailed Design Procedure

8.2.2.1 Setting the Gain

A single external resistor (R_G) that is connected between pins 1 and 8 sets the gain of the INA317. The value of R_G is selected according to 公式 1:

$$G = 1 + (100\ k\Omega / R_G) \quad (1)$$

表 1 lists several commonly-used gains and resistor values. The 100 kΩ in 公式 1 is a result of the sum of the two internal feedback resistors (A_1 and A_2.) These on-chip resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA317 device.

The stability and temperature drift of the external gain setting resistor (R_G) also affects gain. The contribution of R_G to gain accuracy and drift is inferred from the gain in公式 1. Low resistor values required for high gain make wiring resistance important. Sockets add to the wiring resistance and contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater. To ensure stability, avoid parasitic capacitance of more than a few picofarads at the R_G connections. Careful matching of any parasitics on R_G pins maintains optimal CMRR over frequency.

表 1. Commonly-Used Gains and Resistor Values

DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	NC(1)	NC
2	100 k	100 k
5	25 k	24.9 k
10	11.1 k	11 k
20	5.26 k	5.23 k
50	2.04 k	2.05
100	1.01 k	1 k
200	502.5	499
500	200.4	200
1000	100.1	100

(1) NC denotes no connection. When using the SPICE model, the simulation does not converge unless a resistor is connected to the R_G pins; use a large resistor value.

8.2.2.2 Internal Offset Correction

The INA317 device internal operational amplifiers use an autocalibration technique with a time-continuous 350-kHz operational amplifier in the signal path. The amplifier is zero-corrected every 8 µs using a proprietary technique. At power-up, the amplifier requires approximately 100 µs to achieve specified V_{OS} accuracy. This design has no aliasing or flicker noise.

8.2.2.3 Offset Trimming

Most applications require no external offset adjustment. However, apply a voltage to the REF pin to make adjustments if necessary. 图 33 shows an optional circuit for trimming the output offset voltage. The voltage applied to REF pin is added at the output. The operational amplifier buffer provides low impedance at the REF pin to preserve good common-mode rejection.

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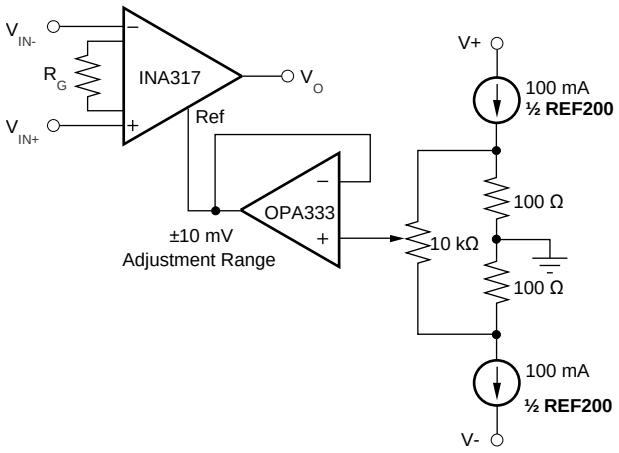

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图 33. Optional Trimming of Output Offset Voltage

8.2.2.4 Noise Performance

The autocalibration technique used by the INA317 device results in reduced low-frequency noise, typically only 50 nV/√Hz (G = 100). The spectral noise density is shown in 图 8. Low-frequency noise of the INA317 device is approximately 1 μV_{PP} measured from 0.1 Hz to 10 Hz (G = 100).

8.2.2.5 Input Bias Current Return Path

The input impedance of the INA317 device is extremely high(approximately 100 GΩ.) However, a path must be provided for the input bias current of the inputs. This input bias current is typically ±70 pA. High-input impedance means that this input bias current changes very little with varying input voltage.

For proper operation, input circuitry must provide a path for the input bias current. 图 34 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA317 device, and the input amplifiers saturate. If the differential source resistance is low, the bias current return path connects to one input (see the thermocouple example in 图 34). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage as a result of bias current and better high-frequency common-mode rejection.

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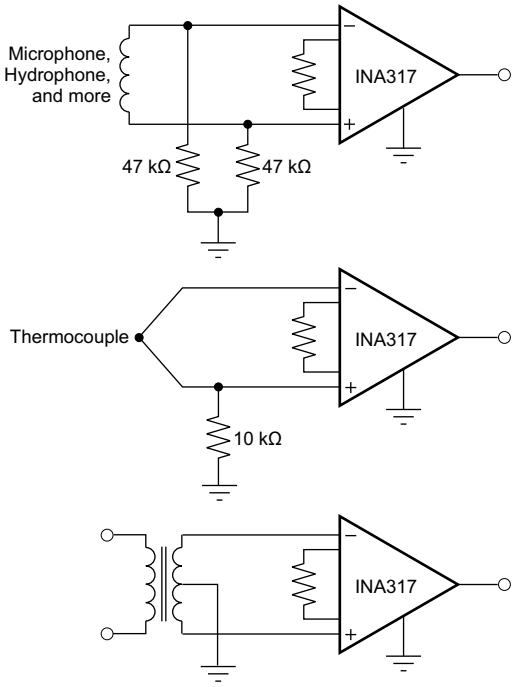

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图 34. Providing an Input Common-Mode Current Path

8.2.2.6 Input Common-Mode Range

The linear input voltage range of the input circuitry of the INA317 device is from approximately 0.1 V below the positive supply voltage to 0.1 V above the negative supply. As a differential input voltage causes the output voltage to increase, however, the linear input range is limited by the output voltage swing of amplifiers A_1 and A_2. The linear common-mode input range is related to the output voltage of the complete amplifier. This behavior depends on supply voltage(see 图 20 to 图 23 in the *Typical Characteristics* section.)

Input overload conditions can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to the respective positive output swing limit, the difference voltage measured by the output amplifier is near zero. The output of the INA317 is near 0 V even though both inputs are overloaded.

8.2.2.7 Operating Voltage

The INA317 operates over a power-supply range of 1.8 V to 5.5 V (±0.9 V to ±2.75 V). Supply voltages higher than 7 V (absolute maximum) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in the *Typical Characteristics* section of this data sheet.

8.2.2.8 Low Voltage Operation

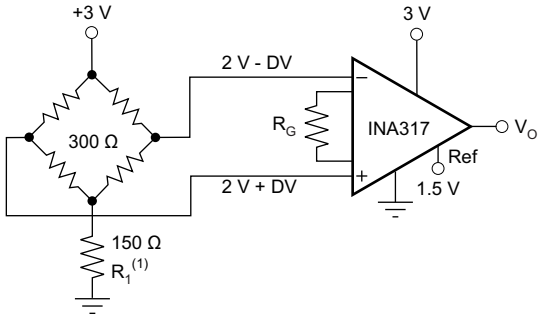
The INA317 device operates on power supplies as low as ±0.9 V. Most parameters vary only slightly throughout this supply voltage range; see the *Typical Characteristics* section. Operation at very low supply voltage requires careful attention to ensure that the input voltages remain within the linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power supply voltage. 图 20 to 图 23 show the range of linear operation for various supply voltages and gains.

8.2.2.9 Single-Supply Operation

The INA317 device can be used on single power supplies of 1.8 V to 5.5 V. 图 35 shows a basic single-supply circuit. The output REF pin is connected to midsupply. Zero differential input voltage demands an output voltage of midsupply. Actual output voltage swing is limited to approximately 50 mV more than ground when the load is referred to ground as shown. 图 29 shows how the output voltage swing varies with output current.

With single-supply operation, V_{IN+} and $V_{IN–}$ must be 0.1 V more than ground for linear operation. For instance, the inverting input cannot connect to ground to measure a voltage that is connected to the noninverting input.

To show the issues affecting low voltage operation, see 图 35. 图 35 shows the INA317 device operating from a single 3-V supply. A resistor in series with the low side of the bridge ensures that the bridge output voltage is within the common-mode range of the amplifier inputs.



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(1) R_1 creates proper common-mode voltage only for low-voltage operation; see *Single-Supply Operation*.

图 35. Single-Supply Bridge Amplifier

8.2.2.10 Input Protection

The input pins of the INA317 device are protected with internal diodes that are connected to the power-supply rails. These diodes clamp the applied signal to prevent the signal from damaging the input circuitry. If the input signal voltage exceeds the power supplies by more than 0.3 V, the input signal current must be limited to less than 10 mA to protect the internal clamp diodes. Limit the current with a series input resistor. Some signal sources are inherently current limited and do not require limiting resistors.

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8.2.3 Application Curves

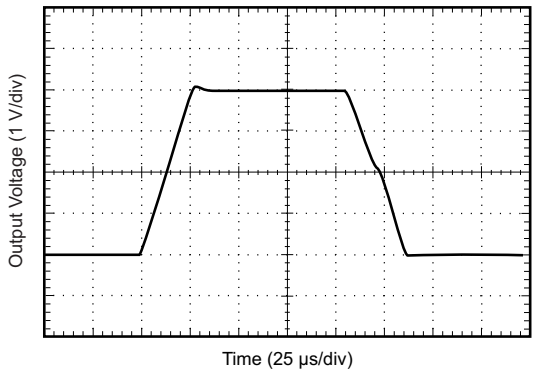

图 36. Large Signal Response

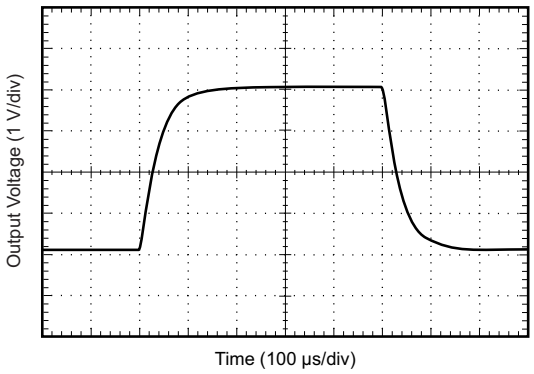

图 37. Large-Signal Step Response

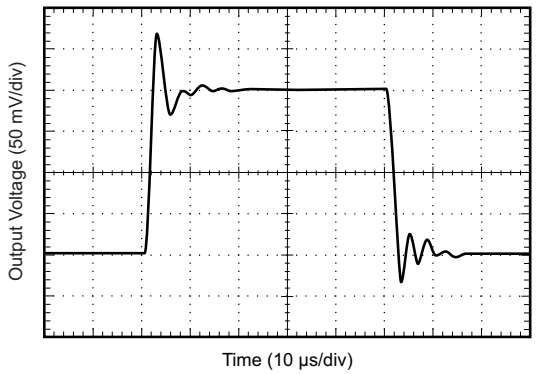

图 38. Small-Signal Step Response

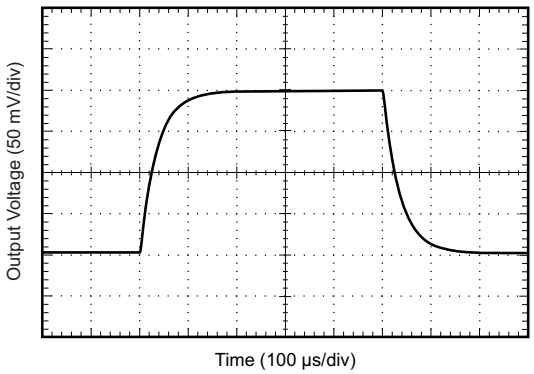

图 39. Small-Signal Step Response

9 Power Supply Recommendations

The minimum power supply voltage for INA317 is 1.8 V and the maximum power supply voltage is 5.5 V. For optimum performance, 3.3 V to 5 V is recommended. TI recommends adding a bypass capacitor at the input to compensate for the layout and power supply source impedance.

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10 Layout

10.1 Layout Guidelines

TI recommends paying attention to good layout practices. Keep traces short and use a printed-circuit-board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-µF bypass capacitor as close as possible the supply pins. Apply these guidelines throughout the analog circuit to improve performance and reduce electromagnetic interference (EMI) susceptibility.

Instrumentation amplifiers vary in the susceptibility to radio-frequency interference (RFI). RFI is identified as a variation in offset voltage or DC signal levels with changes in the interfering RF signal. The INA317 device is designed to minimize susceptibility to RFI by incorporating passive RC filters with an 8-MHz corner frequency at the V_{IN+} and $V_{IN–}$ inputs. As a result, the INA317 device demonstrates low sensitivity compared to previous generation devices. However, strong RF fields can cause varied offset levels and may require additional shielding.

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10.2 Layout Example

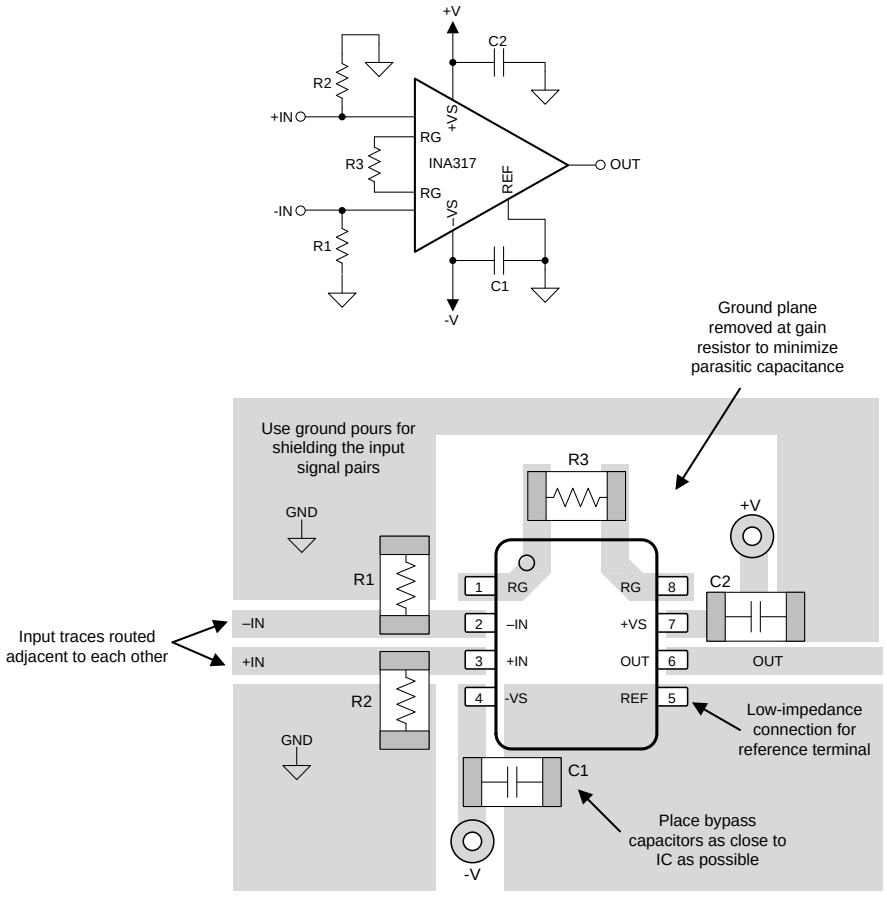

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图 40. INA317 Layout

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 TINA-TI（免费下载软件）

针对 **INA317** 使用基于 **SPICE** 的 **TINA-TI** 模拟仿真程序

TINA 是一款简单、功能强大且易于使用的电路仿真程序，此程序基于 SPICE 引擎。TINA-TI 是 TINA 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。它提供所有传统的 SPICE 直流 (DC)、瞬态和频域分析以及其他设计功能。

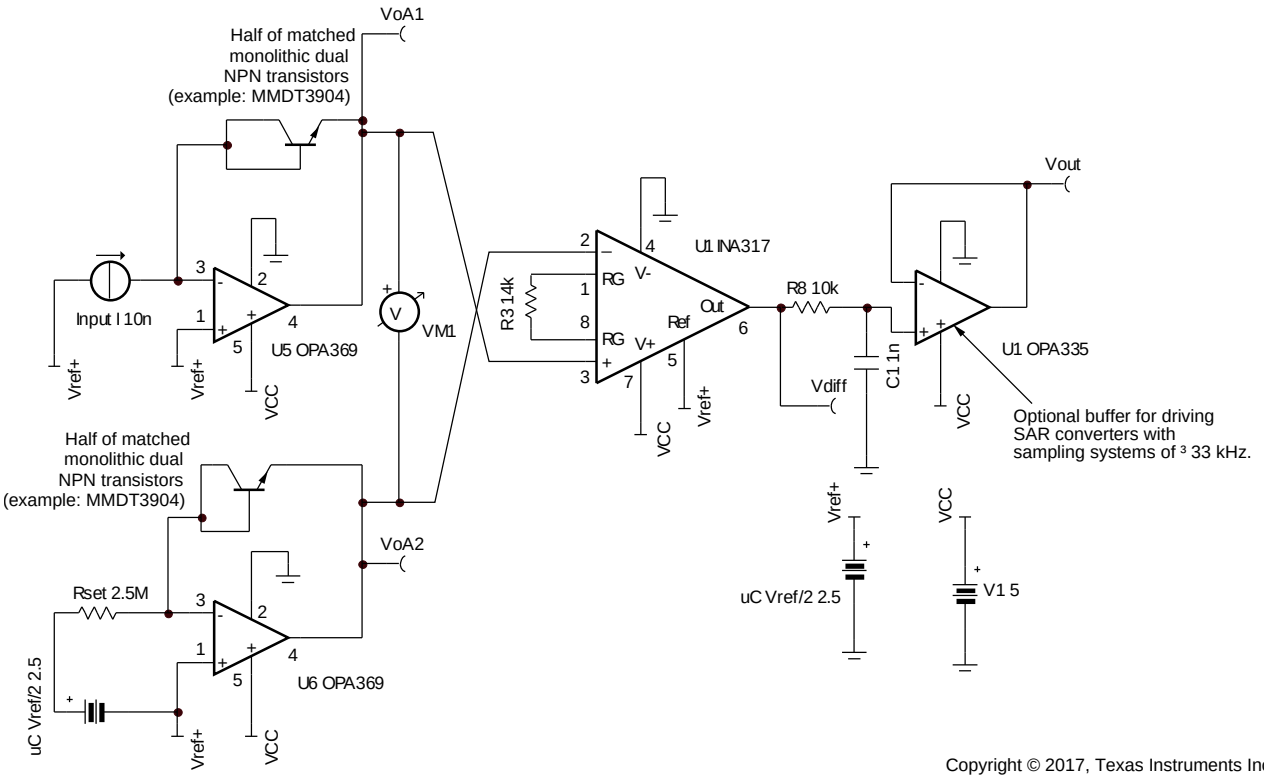
TINA-TI 可从 Analog eLab Design Center（模拟电子实验室设计中心）免费下载，它提供全面的后续处理能力，使得用户能够以多种方式形成结果。

虚拟仪器为用户提供选择输入波形和探测电路节点、电压和波形的功能，从而创建一个动态的快速入门工具。

图 41 和图 42 给出了适用于 INA317 器件的 TINA-TI 电路示例，可用于开发、修改和评估特定 应用的电路设计。。下面给出了这些仿真文件的下载链接。

注

必须安装 TINA 软件（从 DesignSoft）或者 TINA-TI 软件后才能使用这些文件。请从 TINA-TI 文件夹中下载免费的 TINA-TI 软件。



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(1) 如下链接会打开 TI 对数放大器网页：对数放大器产品主页

(2) 未显示对数晶体管的温度补偿。

(3) 对于单片对数放大器（例如 LOG112 或 LOG114），请参阅注 1 中的链接。

图 41. 便携式电池供电类系统的低功耗对数函数电路（例如血糖仪）

要下载包含此电路 TINA-TI 仿真文件的压缩文件，请点击如下链接：对数电路。

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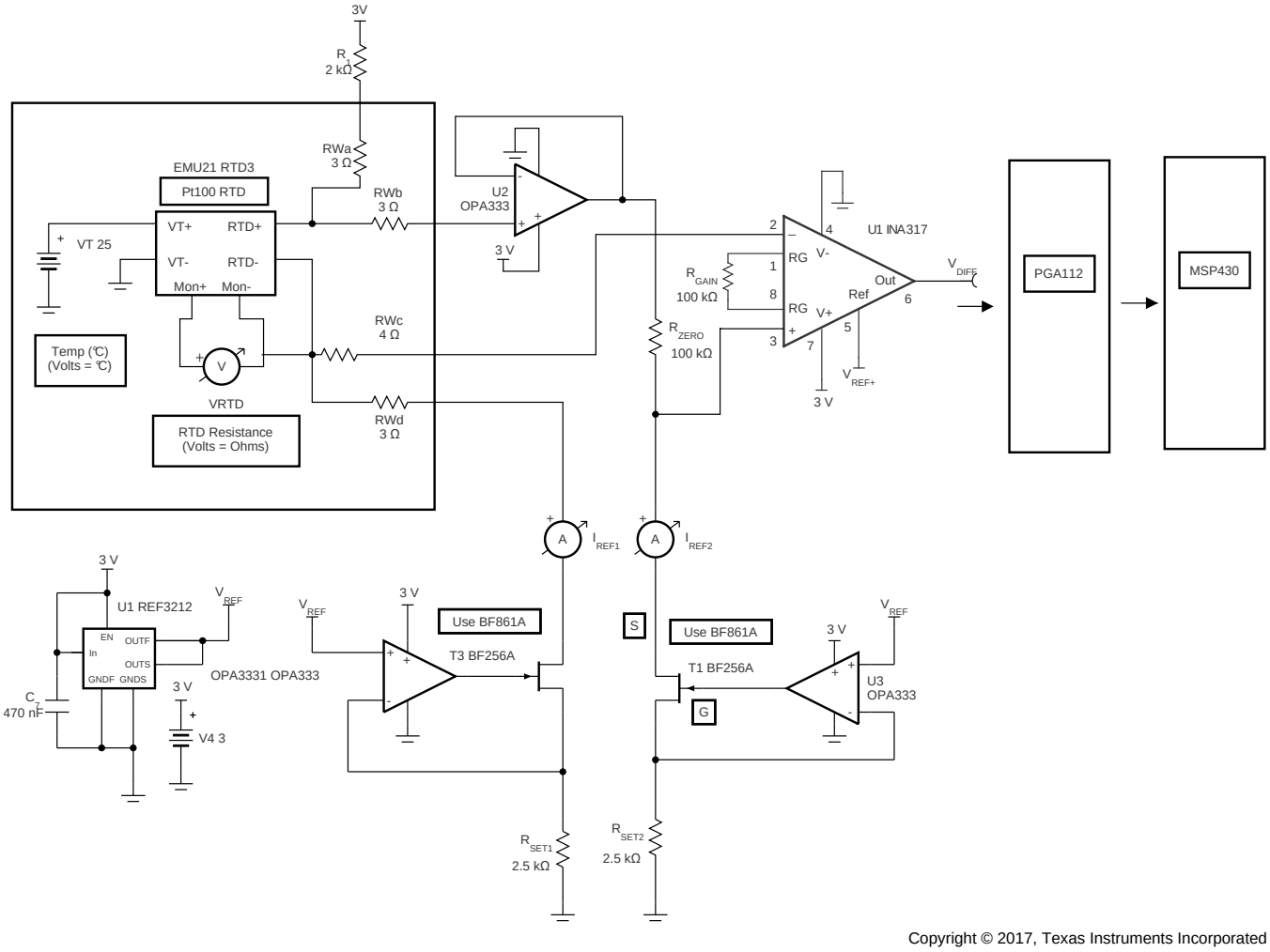
器件支持 (接下页)



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RWa、RWb、RWc 和 RWd 用于仿真线电阻。包含这些电阻以展示 4 线感应技术对线路失配的抗扰性。这种方法假定使用 4 线 RTD。

图 **42.** 带有可编程增益采集系统的适用于 **PT100 RTD** 的 **4** 线、**3V** 调节器

要下载包含此电路 TINA-TI 仿真文件的压缩文件，请点击如下链接：PT100 RTD。

11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档：

- *精密、低噪声、轨至轨输出，36V，零漂移运算放大器*
- *50μV VOS、0.25μV/°C、35μA CMOS 运算放大器零漂移系列*
- *4ppm/°C、100μA、SOT23-6 系列电压基准*
- *《电路板布局布线技巧》*

11.3 商标

All trademarks are the property of their respective owners.

11.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA317IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	I317	Samples
INA317IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	I317	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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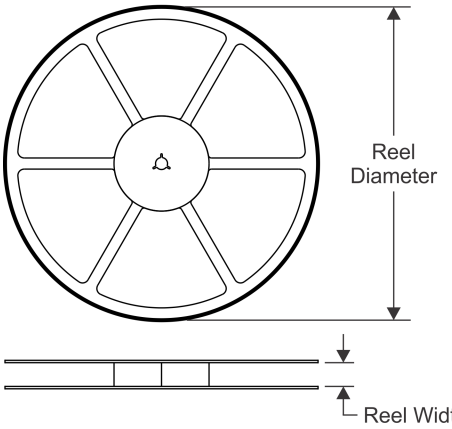
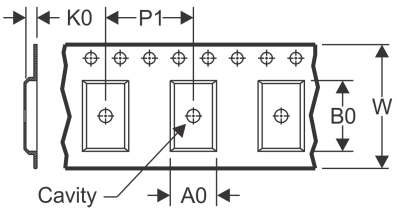
TAPE AND REEL INFORMATION

REEL DIMENSIONS

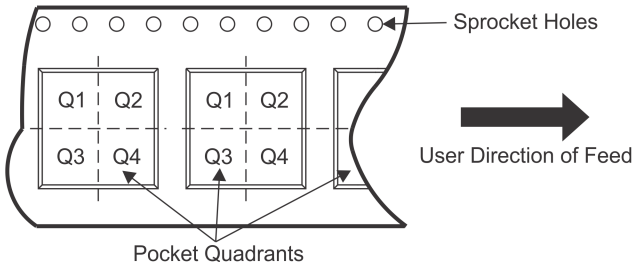


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

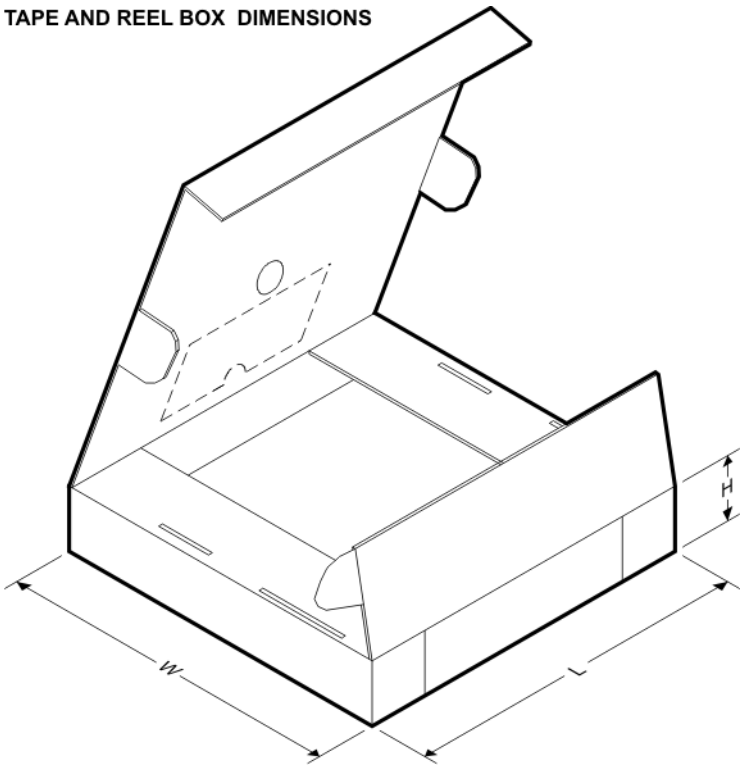
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA317IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA317IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

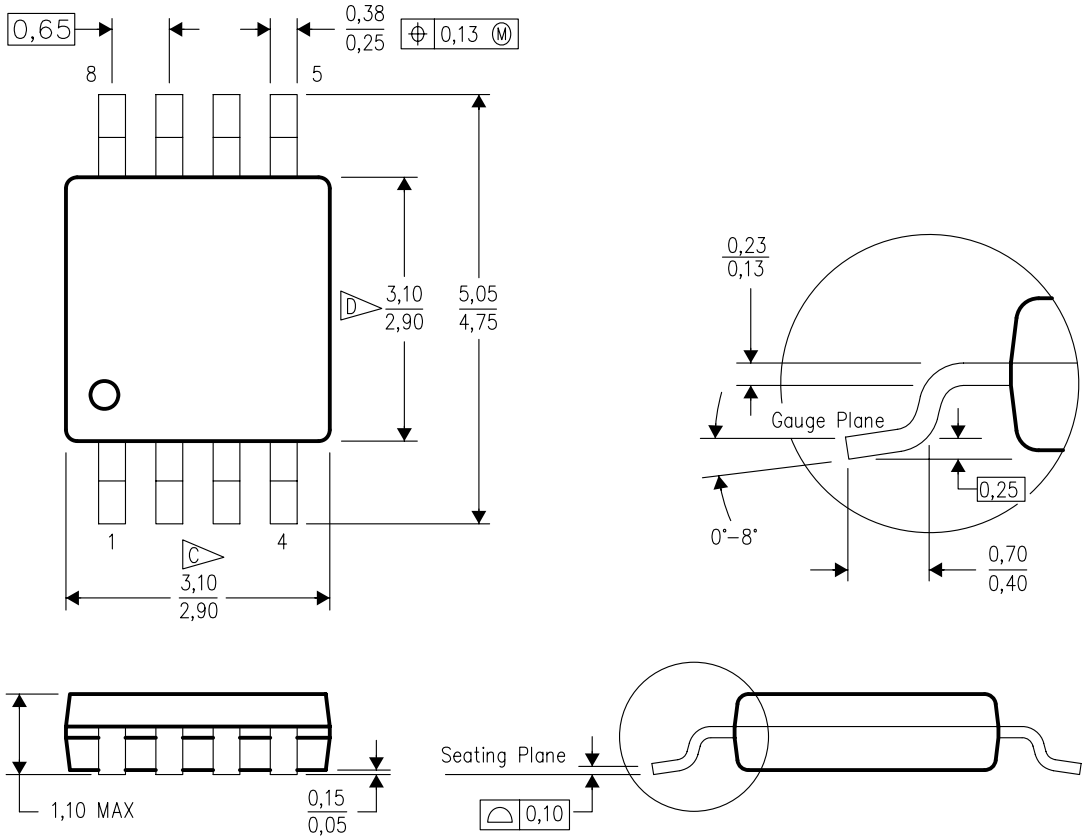
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA317IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA317IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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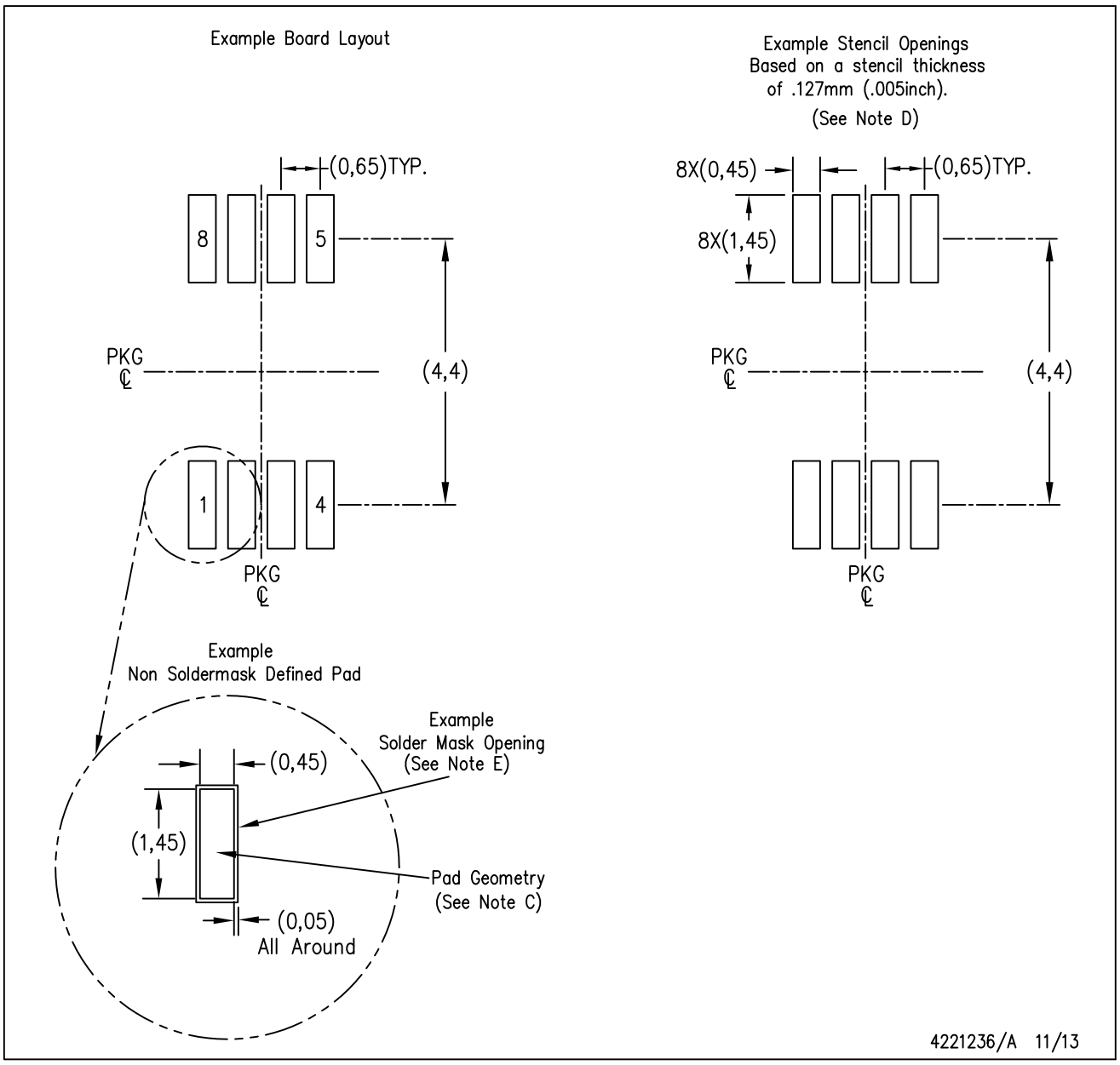
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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