VOLTAGE OUTPUT, UNIDIRECTIONAL MEASUREMENT CURRENT-SHUNT MONITOR

Check for Samples: INA271-HT

FEATURES

- **Wide Common-Mode Range: –16V to +80V**
- **CMRR: 78dB**
- **Accuracy:**
  ±10mV Offset (max)
  ±7.5% Gain Error (max)
  100µV/°C Offset Drift (max)
- **Bandwidth: Up to 130kHz**
- **Transfer Function: 20V/V**
- **Quiescent Current: 1600µA (max)**
- **Power Supply: +2.7V to +18V**
- **Provision for Filtering**

APPLICATIONS

- **Down-Hole Drilling**
- **High Temperature Environments**

SUPPORTS EXTREME TEMPERATURE APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Extreme (–55°C/210°C) Temperature Range** (1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**
- **Texas Instruments high temperature products utilize highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.**

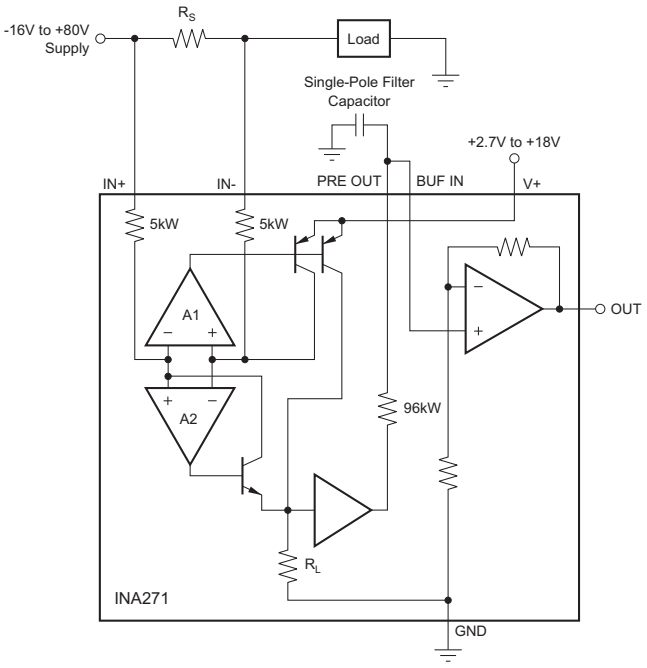
(1) Custom temperature ranges available

DESCRIPTION

The INA271 is a current-shunt monitor with voltage output and can sense drops across current shunts at common-mode voltages from –16V to +80V, independent of the supply voltage. The INA271 pinouts readily enable filtering.

The INA271 is available with a 20V/V output voltage scale. The 130kHz bandwidth simplifies use in current-control loops.

The INA271 operates from a single +2.7V to +18V supply, drawing a maximum of 1600µA of supply current. This device is specified over the extended operating temperature range of –55°C to +210°C.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
11 mils.	Silicon with backgrind	GND	Al-Cu (0.5%)	598 nm

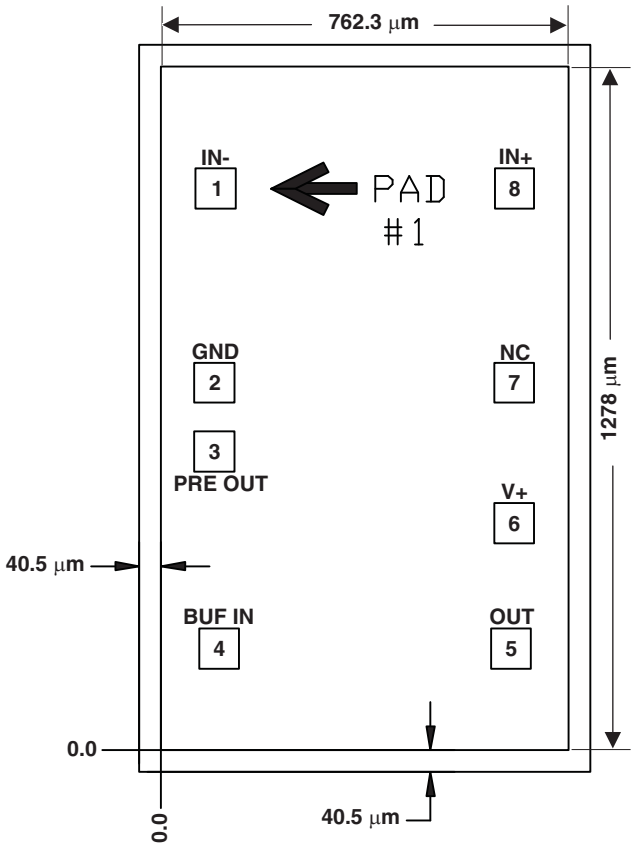


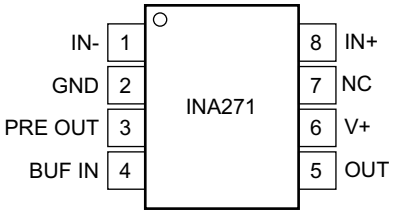
Table 1. Bond Pad Coordinates in Microns

DISCRIPTION	PAD NUMBER	X min	Y min	X max	Y max
IN-	1	64.35	1012.41	139.41	1087.47
GND	2	61.83	648.81	136.89	723.87
PRE OUT	3	61.83	520.29	136.89	595.35
BUF IN	4	70.92	152.37	145.98	227.43
OUT	5	616.32	152.37	691.38	227.43
V+	6	621.99	386.55	697.05	461.61
NC	7	622.44	648.81	697.5	723.87
IN+	8	622.89	1012.41	697.95	1087.47

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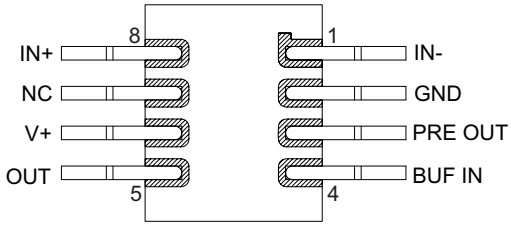
PIN CONFIGURATION

AHD OR HKJ PACKAGE
(TOP VIEW)



NC denotes no internal connection

HKQ PACKAGE
(TOP VIEW)



HKQ as formed or HKJ mounted dead bug

ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 175°C	AHD	INA271AHD	INA271AHD
–55°C to 210°C	KGD (bare die)	INA271SKGD1	NA
		INA271SKGD2	
	HKJ	INA271SHKJ	INA271SHKJ
	HKQ	INA271SHKQ	INA271SHKQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)

		UNIT
Supply Voltage (V_S)	+18	V
Analog Inputs, V_{IN+}, $V_{IN–}$:		
Differential, (V_{IN+}) – ($V_{IN–}$)	–18 to +18	V
Common-Mode	–16 to +80	V
Analog Output:		
OUT and PRE OUT Pins	GND – 0.3 to (V+) + 0.3	V
Input Current Into Any Pin	5	mA
Operating Temperature	–55 to +210	°C
Storage Temperature	–65 to +210	°C
Junction Temperature	+210	°C
ESD Ratings:		
Human Body Model	3000	V
Charged-Device Model	750	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

THERMAL CHARACTERISTICS FOR HKJ OR HKQ PACKAGE

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
θ_{JC}	Junction-to-case thermal resistance	to ceramic side of case			5.7	°C/W
		to top of case lid (metal side of case)			13.7	

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ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_S = +5V, V_{CM} = +12V, V_{SENSE} = 100mV, and PRE OUT connected to BUF IN, unless otherwise noted.

PARAMETER		CONDITIONS	T_A = –55°C to 125°C			T_A = –55°C to 175°C			T_A = 210°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT												
Full-Scale Input Voltage	V_{SENSE}	$V_{SENSE} = (V_{IN+}) + (V_{IN–})$		0.15	(V_S – 0.2)/Gain					0.15	(V_S – 0.2)/Gain	V
Common-Mode Input Range	V_{CM}		–16		80				–16		80	V
Common-Mode Rejection Ratio	CMRR	V_{IN+} = –16V to +80V	80	120					70	78		dB
		V_{IN+} = +12V to +80V	100	120					81	89		
Offset Voltage, RTI[1]	V_{OS}			±0.6	±3					±5	±10	mV
vs Temperature	dV_{OS}/dT			3.3	20					42	100	µV/°C
vs Power-Supply	PSR	V_S = +2.7V to +18V, V_{CM} = +18V		5	100					130	320	µV/V
Input Bias Current, $V_{IN–}$ Pin	I_B			±8	±16					±16	±25	µA
PRE OUT Output Impedance[2]				96						96		kΩ
Buffer Input Bias Current				–50						–50		nA
Buffer Input Bias Current Temperature Coefficient				±0.03						±0.03		nA/°C
OUTPUT (V_{SENSE} ≥ 20mV)[3]												
Gain: INA271 Total Gain	G			20						20		V/V
Output Buffer Gain	G_{BUF}			2						2		V/V
Total Gain Error		V_{SENSE} = 20mV to 100mV		±0.2	±2					±1	±7.5	%
vs Temperature					50					300		ppm/°C
Total Output Error[4]				±1	±3					±4.6	±11.5	%
Nonlinearity Error		V_{SENSE} = 20mV to 100mV		±0.002						±0.002		%
Output Impedance	R_O			1.5						1.5		Ω
Maximum Capacitive Load		No Sustained Oscillation		10						10		nF
VOLTAGE OUTPUT[5]		**R_L = 10kΩ to GND**										
Swing to V+ Power-Supply Rail				(V+) – 0.05	(V+) – 0.2					(V+) – 0.13	(V+) – 0.2	V
Swing to GND[6]				V_{GND} + 0.003	V_{GND} + 0.05					V_{GND} + 0.22	V_{GND} + 0.42	V
FREQUENCY RESPONSE												
Bandwidth	BW	C_{LOAD} = 5pF		130						130		kHz
Phase Margin		C_{LOAD} < 10nF		40						40		degrees
Slew Rate	SR			1						1		V/µs
Settling Time (1%)	t_S	V_{SENSE} = 10mV to 100mV_{PP}, C_{LOAD} = 5pF		2						2		µs

(1) RTI means *Referred-to-Input*.
(2) Initial resistor variation is ±30% with an additional –2200ppm/°C temperature coefficient.
(3) For output behavior when V_{SENSE} < 20mV, see the Application Information section *Accuracy Variations as A Result of V_{SENSE} and Common-Mode Voltage*.
(4) Total output error includes effects of gain error and V_{OS}.
(5) See typical characteristic curve *Output Swing vs Output Current* and Application Information section *Accuracy Variations as A Result of V_{SENSE} and Common-Mode Voltage*.
(6) Ensured by design; not production tested.

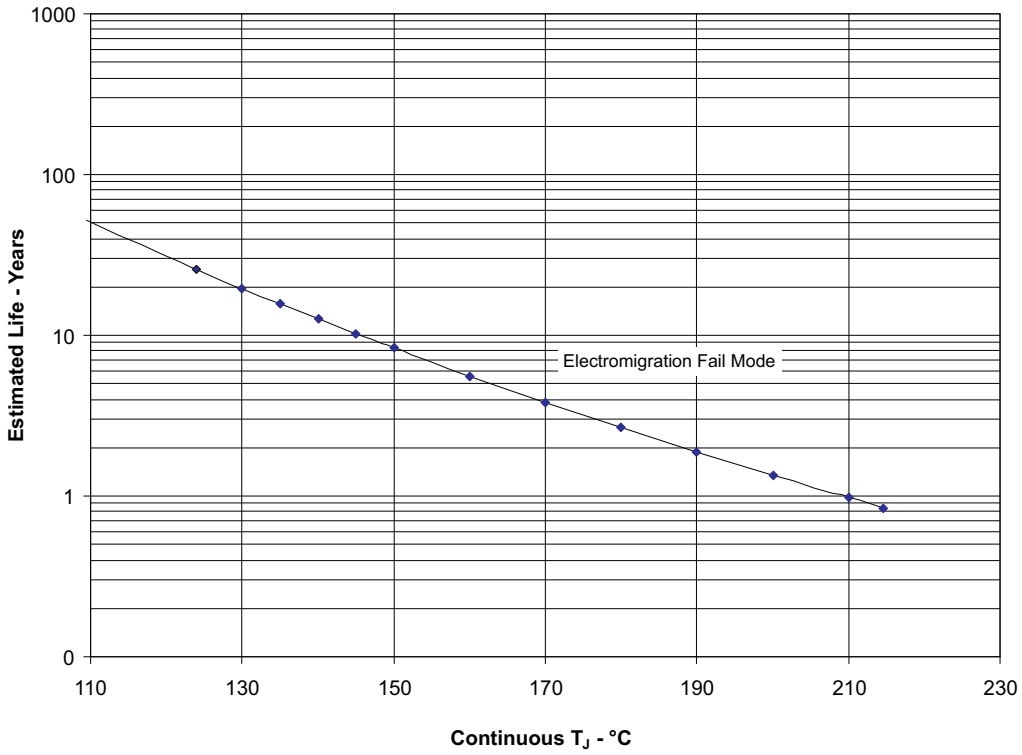
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ELECTRICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +5V, V_{CM} = +12V, V_{SENSE} = 100mV, and PRE OUT connected to BUF IN, unless otherwise noted.

PARAMETER		CONDITIONS	T_A = –55°C to 125°C			T_A = –55°C to 175°C			T_A = 210°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
NOISE < RTI(7)												
Voltage Noise Density	e_n			40						40		nV/√Hz
POWER SUPPLY												
Operating Range	V_S		2.7		18				2.7		18	V
Quiescent Current	I_Q	VOUT = 2V		740	1200					1160	1600	µA
		V_{SENSE} = 0mV		350	950					895	1600	
TEMPERATURE RANGE												
Specified Temperature Range			–55		125				–55		210	°C
Operating Temperature Range			–55		125				–55		210	°C

(7) RTI means *Referred-to-Input*.



(1) See datasheet for absolute maximum and minimum recommended operating conditions.

(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

Figure 1. INA271SKGD1/INA271SKGD2/INA271SHKJ/INA271SHKQ Operating Life Derating Chart

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TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = +12V, V_{CM} = 12V, and V_{SENSE} = 100mV, unless otherwise noted.

GAIN vs FREQUENCY

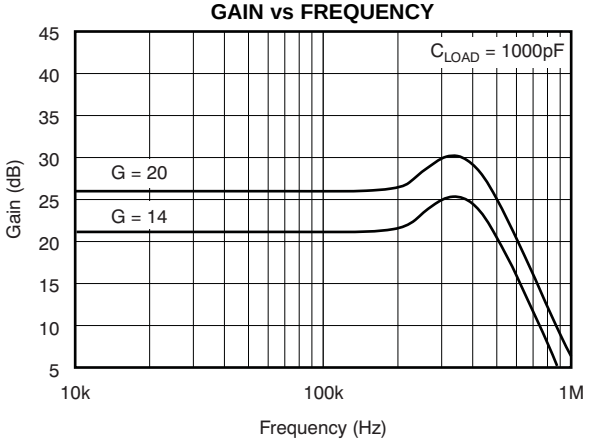


Figure 2.

GAIN vs FREQUENCY

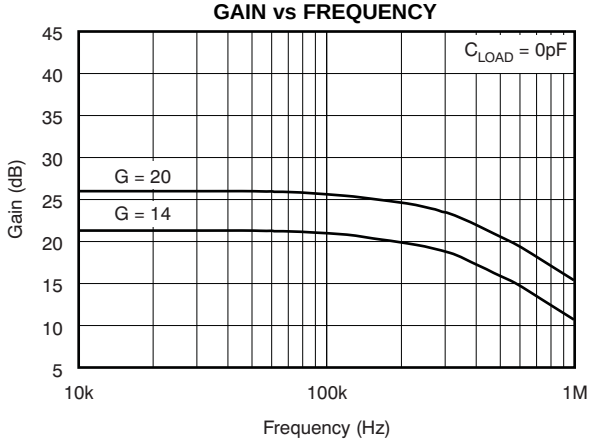


Figure 3.

GAIN PLOT

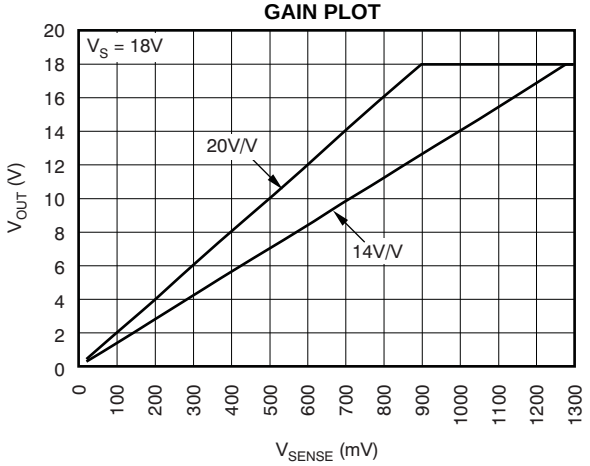


Figure 4.

COMMON-MODE AND POWER-SUPPLY REJECTION vs FREQUENCY

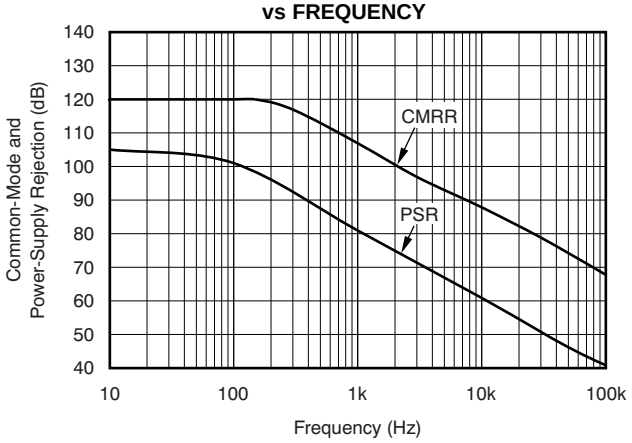


Figure 5.

TOTAL OUTPUT ERROR vs V_{SENSE}

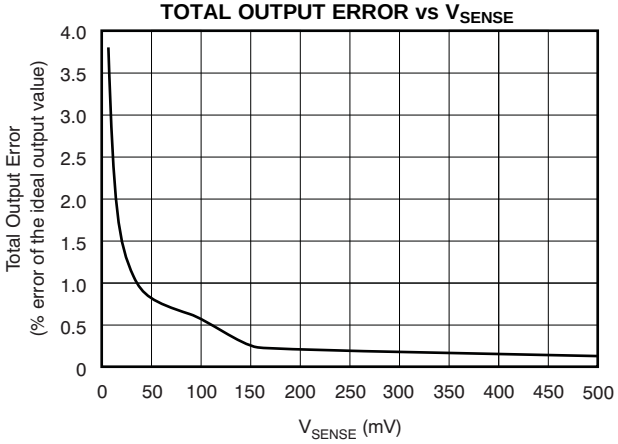


Figure 6.

OUTPUT ERROR vs COMMON-MODE VOLTAGE

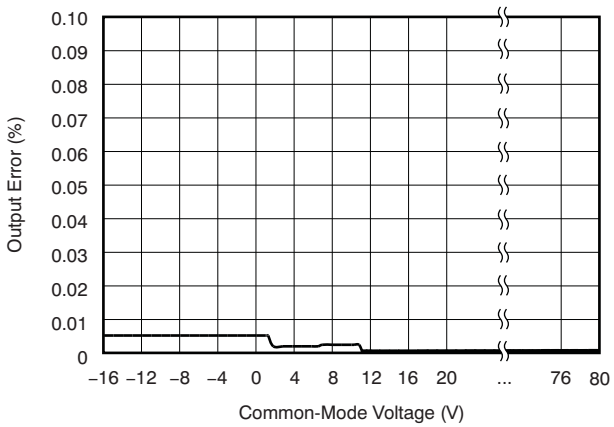


Figure 7.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +12V, V_{CM} = 12V, and V_{SENSE} = 100mV, unless otherwise noted.

POSITIVE OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

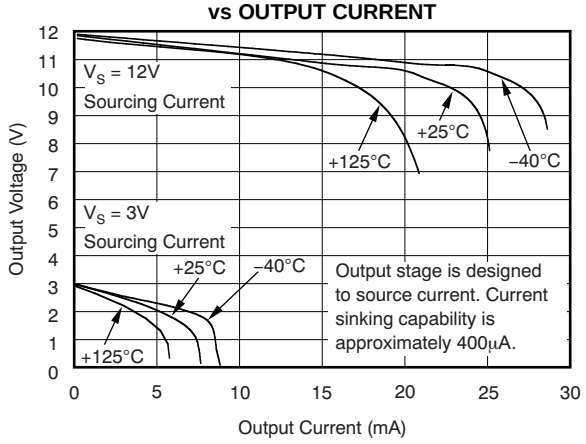


Figure 8.

QUIESCENT CURRENT vs OUTPUT VOLTAGE

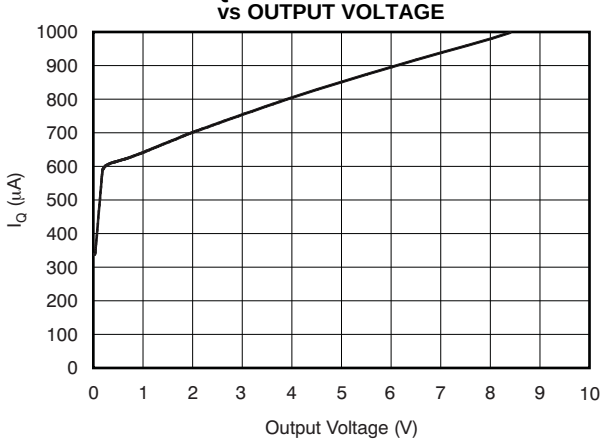


Figure 9.

QUIESCENT CURRENT vs COMMON-MODE VOLTAGE

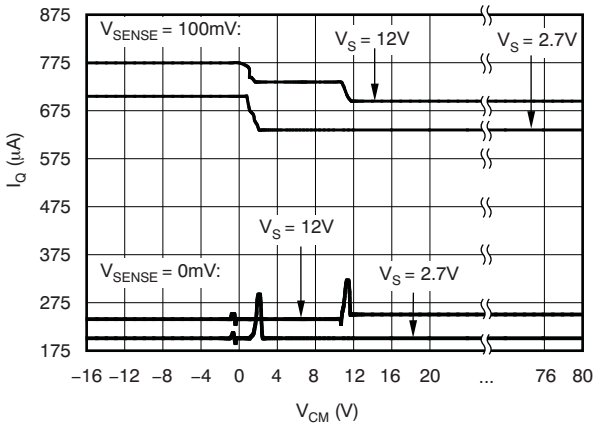


Figure 10.

OUTPUT SHORT-CIRCUIT CURRENT vs SUPPLY VOLTAGE

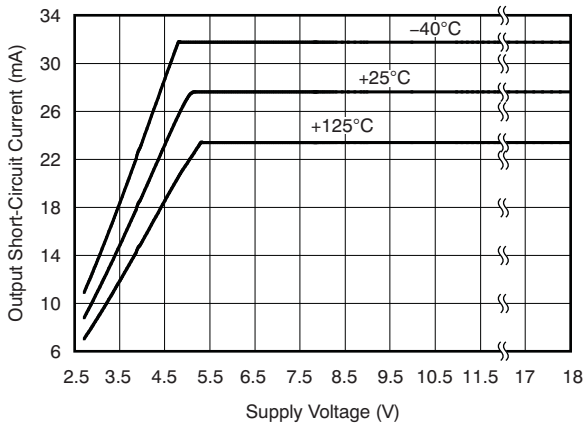


Figure 11.

PREOUT OUTPUT RESISTANCE PRODUCTION DISTRIBUTION

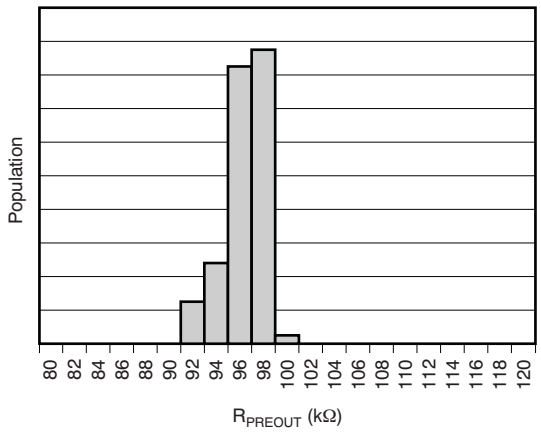


Figure 12.

BUFFER GAIN vs FREQUENCY

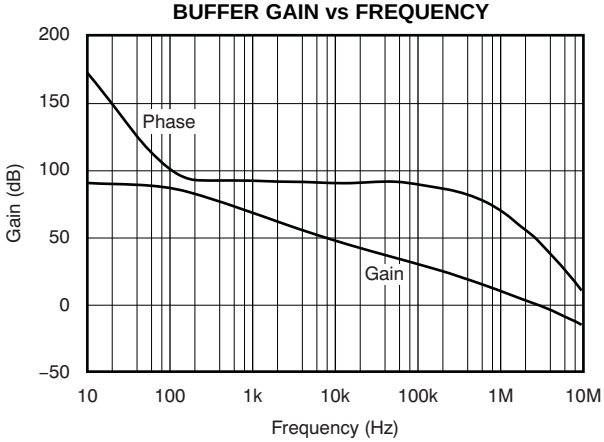


Figure 13.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +12V, V_{CM} = 12V, and V_{SENSE} = 100mV, unless otherwise noted.

SMALL-SIGNAL STEP RESPONSE
10mV TO 20mV INPUT

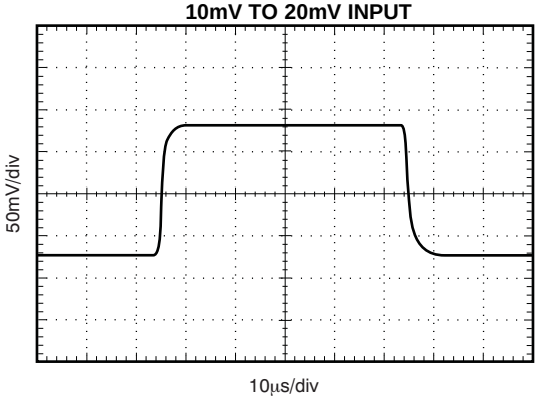


Figure 14.

LARGE-SIGNAL STEP RESPONSE
10mV TO 100mV INPUT

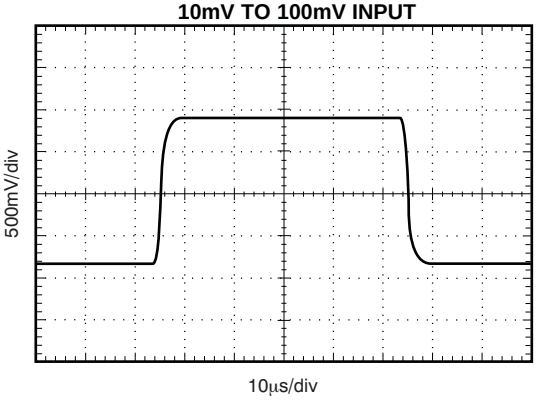


Figure 15.

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APPLICATIONS INFORMATION

BASIC CONNECTION

Figure 16 shows the basic connection of the IINA271. The input pins, IN+ and IN–, should be connected as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistance.

Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Minimum bypass capacitors of 0.01µF and 0.1µF in value should be placed close to the supply pins. Although not mandatory, an additional 10mF electrolytic capacitor placed in parallel with the other bypass capacitors may be useful in applications with particularly noisy supplies.

POWER SUPPLY

The input circuitry of the INA271 can accurately measure beyond its power-supply voltage, V+. For example, the V+ power supply can be 5V, whereas the load power-supply voltage is up to +80V. The output voltage range of the OUT terminal, however, is limited by the voltages on the power-supply pin.

SELECTING R_S

The value chosen for the shunt resistor, R_S, depends on the application and is a compromise between small-signal accuracy and maximum permissible voltage loss in the measurement line. High values of R_S provide better accuracy at lower currents by minimizing the effects of offset, while low values of R_S minimize voltage loss in the supply line. For most applications, best performance is attained with an R_S value that provides a full-scale shunt voltage range of 50mV to 100mV. Maximum input voltage for accurate measurements is (V_S – 0.2)/Gain.

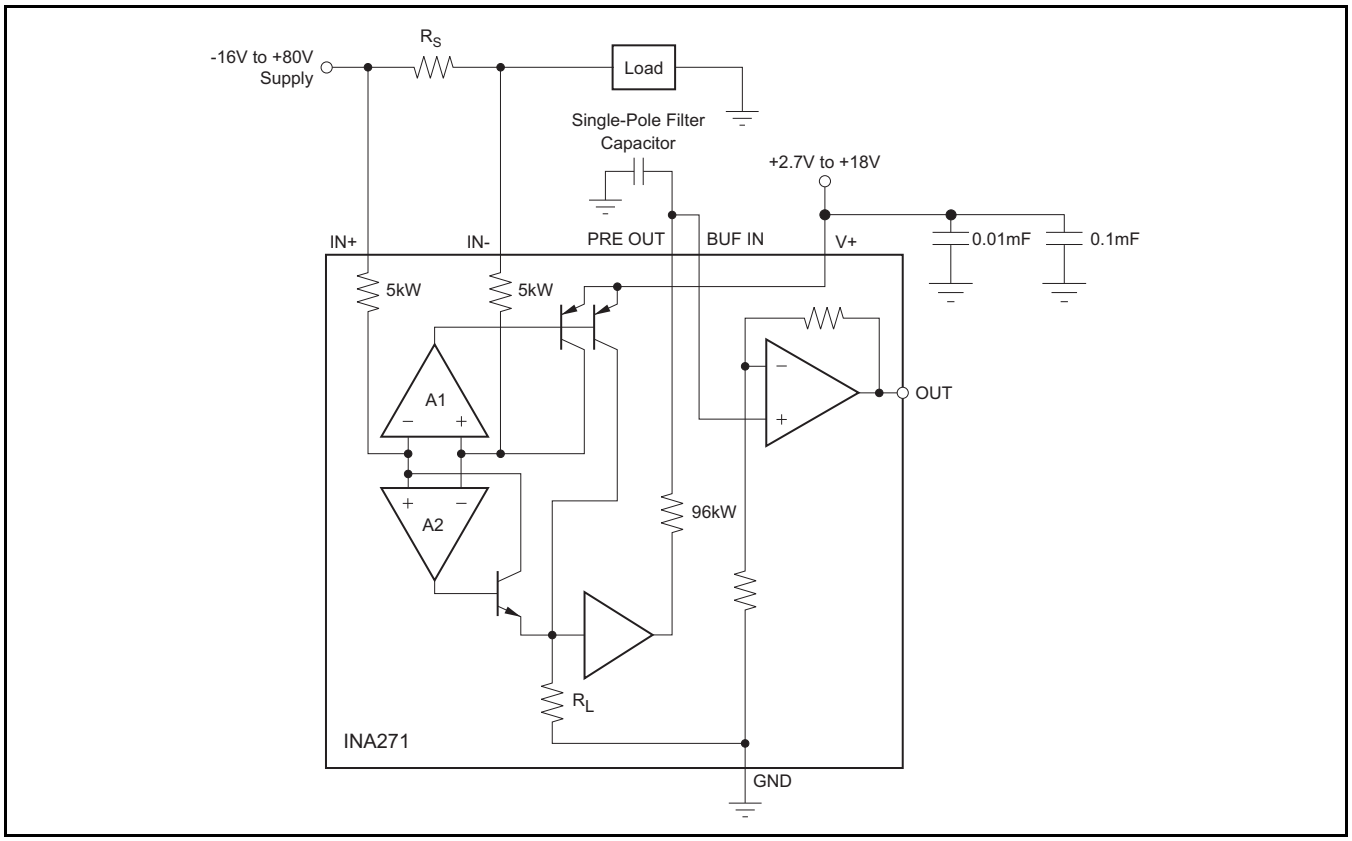


Figure 16. INA271 Basic Connections

TRANSIENT PROTECTION

The –16V to +80V common-mode range of the INA271 is ideal for withstanding automotive fault conditions ranging from 12V battery reversal up to +80V transients, since no additional protective components are needed up to those levels. In the event that the INA271 is exposed to transients on the inputs in excess of their ratings, external transient absorption with semiconductor transient absorbers (zeners or Transzorbs) will be necessary.

Use of MOVs or VDRs is not recommended except when they are used in addition to a semiconductor transient absorber. Select the transient absorber such that it will never allow the INA271 to be exposed to transients greater than 80V (that is, allow for transient absorber tolerance, as well as additional voltage because of transient absorber dynamic impedance). Despite the use of internal zener-type ESD protection, the INA271 is not suited to using external resistors in series with the inputs since the internal gain resistors can vary up to ±30%, but is tightly matched (if gain accuracy is not important, then resistors can be added in series with the INA271 inputs with two equal resistors on each input).

OUTPUT VOLTAGE RANGE

The output of the INA271 is accurate within the output voltage swing range set by the power-supply pin, V+.

The INA271 readily enables the inclusion of filtering between the preamp output and buffer input. Single-pole filtering can be accomplished with a single capacitor because of the 96kΩ output impedance at PRE OUT on pin 3, as shown in Figure 17a.

The INA271 readily lends itself to second-order Sallen-Key configurations, as shown in Figure 17b. When designing these configurations consider that the PRE OUT 96kΩ output impedance exhibits an initial variation of ±30% with the addition of a –2200ppm/°C temperature coefficient.

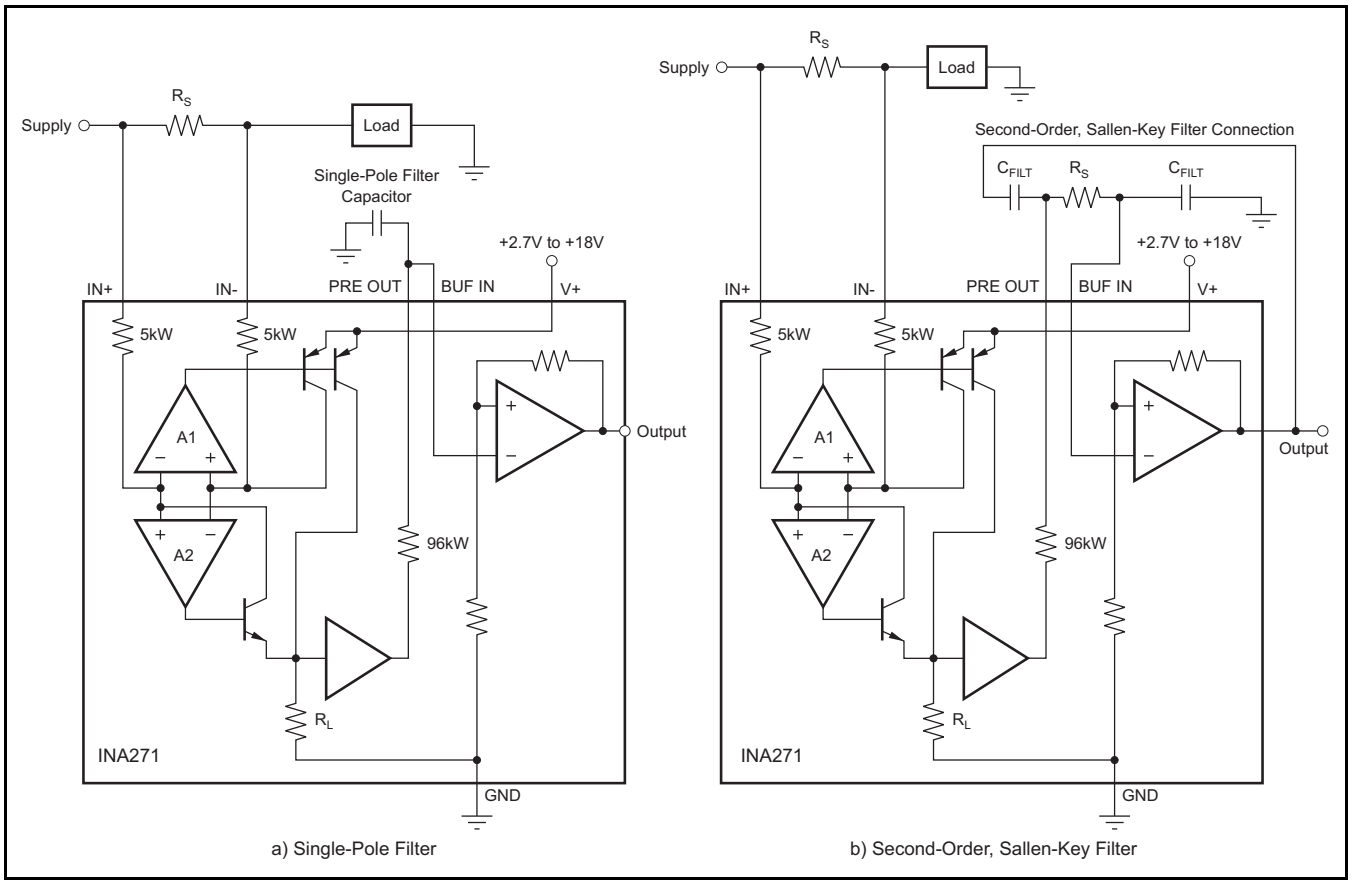


Figure 17. The INA271 can be easily connected for first- or second-order filtering. Remember to use the appropriate buffer gain of 2 when designing Sallen-Key configurations.

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ACCURACY VARIATIONS AS A RESULT OF V_{SENSE} AND COMMON-MODE VOLTAGE

The accuracy of the INA271 current shunt monitor is a function of two main variables: V_{SENSE} ($V_{IN+} - V_{IN-}$) and common-mode voltage, V_{CM}, relative to the supply voltage, V_S. V_{CM} is expressed as ($V_{IN+} + V_{IN-}$)/2; however, in practice, V_{CM} is seen as the voltage at V_{IN+} because the voltage drop across V_{SENSE} is usually small.

This section addresses the accuracy of these specific operating regions:

Normal Case 1: $V_{SENSE} \geq 20mV$, $V_{CM} \geq V_S$
Normal Case 2: $V_{SENSE} \geq 20mV$, $V_{CM} < V_S$
Low V_{SENSE} Case 1:
$V_{SENSE} < 20mV$, $-16V \leq V_{CM} < 0$
Low V_{SENSE} Case 2:
$V_{SENSE} < 20mV$, $0V \leq V_{CM} \leq V_S$
Low V_{SENSE} Case 3:
$V_{SENSE} < 20mV$, $V_S < V_{CM} \leq 80V$

Normal Case 1: $V_{SENSE} \geq 20mV$, $V_{CM} \geq V_S$

This region of operation provides the highest accuracy. Here, the input offset voltage is characterized and measured using a two-step method. First, the gain is determined by Equation 1.

$$G = \frac{V_{OUT1} - V_{OUT2}}{100mV - 20mV} \quad (1)$$

where:

V_{OUT1} = Output Voltage with V_{SENSE} = 100mV
V_{OUT2} = Output Voltage with V_{SENSE} = 20mV

Then the offset voltage is measured at V_{SENSE} = 100mV and referred to the input (RTI) of the current shunt monitor, as shown in Equation 2.

$$V_{OS}RTI\ (Referred\text{-}To\text{-}Input) = \left[\frac{V_{OUT1}}{G}\right] - 100mV \quad (2)$$

In the Typical Characteristics, the *Output Error vs Common-Mode Voltage* curve (Figure 7) shows the highest accuracy for the this region of operation. In this plot, V_S = 12V; for $V_{CM} \geq 12V$, the output error is at its minimum. This case is also used to create the $V_{SENSE} \geq 20mV$ output specifications in the Electrical Characteristics table.

Normal Case 2: $V_{SENSE} \geq 20mV$, $V_{CM} < V_S$

This region of operation has slightly less accuracy than Normal Case 1 as a result of the common-mode operating area in which the part functions, as seen in the *Output Error vs Common-Mode Voltage* curve (Figure 7). As noted, for this graph V_S = 12V; for V_{CM} < 12V, the Output Error increases as V_{CM} becomes less than 12V, with a typical maximum error of 0.005% at the most negative V_{CM} = –16V.

Low V_{SENSE} Case 1: $V_{SENSE} < 20mV$, $-16V \leq V_{CM} < 0$; and Low V_{SENSE} Case 3: $V_{SENSE} < 20mV$, $V_S < V_{CM} \leq 80V$

Although the INA271 is not designed for accurate operation in either of these regions, some applications are exposed to these conditions. For example, when monitoring power supplies that are switched on and off while V_S is still applied to the INA271, it is important to know what the behavior of the device will be in these regions.

As V_{SENSE} approaches 0mV, in these V_{CM} regions, the device output accuracy degrades. A larger-than-normal offset can appear at the current shunt monitor output with a typical maximum value of V_{OUT} = 60mV for V_{SENSE} = 0mV. As V_{SENSE} approaches 20mV, V_{OUT} returns to the expected output value with accuracy as specified in the Electrical Characteristics. Figure 18 shows this effect (Gain = 20).

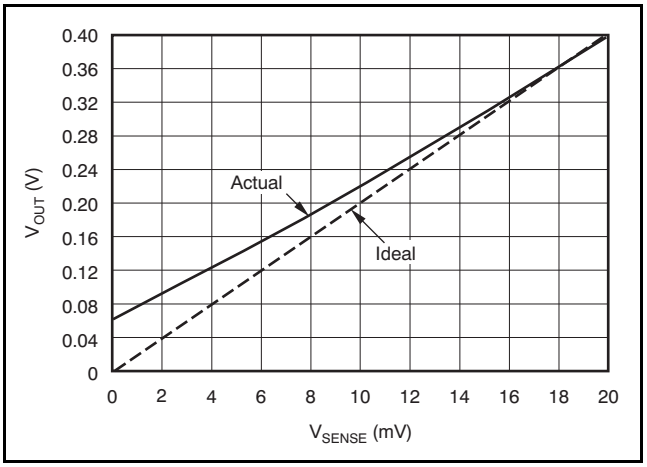


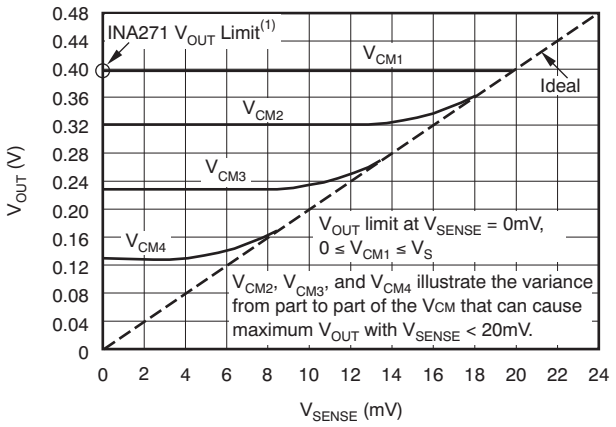
Figure 18. Example for Low V_{SENSE} Cases 1 and 3 (Gain = 20)

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Low V_{SENSE} Case 2: V_{SENSE} < 20mV, 0V ≤ V_{CM} ≤ V_S

This region of operation is the least accurate for the INA271. To achieve the wide input common-mode voltage range, this device uses two op amp front ends in parallel. One op amp front end operates in the positive input common-mode voltage range, and the other in the negative input region. For this case, neither of these two internal amplifiers dominates and overall loop gain is very low. Within this region, V_{OUT} approaches voltages close to linear operation levels for Normal Case 2.

This deviation from linear operation becomes greatest the closer V_{SENSE} approaches 0V. Within this region, as V_{SENSE} approaches 20mV, device operation is closer to that described by Normal Case 2. Figure 19 illustrates this behavior for the INA271. The V_{OUT} maximum peak for this case is determined by maintaining a constant V_S, setting V_{SENSE} = 0mV, and sweeping V_{CM} from 0V to V_S. The exact V_{CM} at which V_{OUT} peaks during this case varies from part to part. The maximum peak voltage for the INA271 is 0.4V.



NOTE: (1) INA271 V_{OUT} Limit = 0.4V. INA270 V_{OUT} Limit = 0.28V.

Figure 19. Example for Low V_{SENSE} Case 2 (Gain = 20)

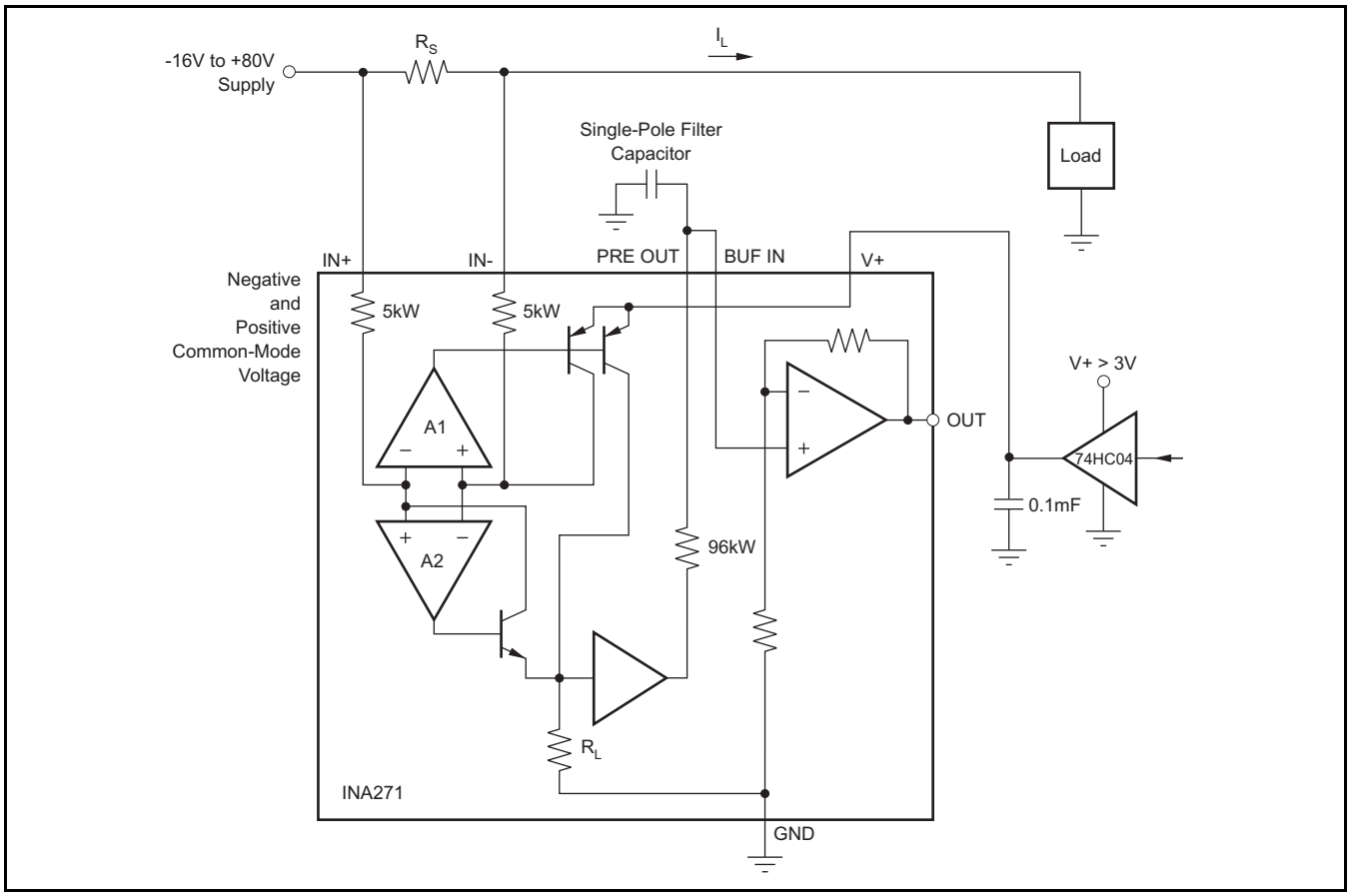
SHUTDOWN

The INA271 does not provide a shutdown pin; however, because it consumes a quiescent current less than 1mA, it can be powered by either the output of logic gates or by transistor switches to supply power. Driving the gate low shuts down the INA271. Use a totem-pole output buffer or gate that can provide sufficient drive along with 0.1µF bypass capacitor, preferably ceramic with good high-frequency characteristics. This gate should have a supply voltage of 3V or greater because the INA271 requires a minimum supply greater than 2.7V. In addition to eliminating quiescent current, this gate also turns off the 10µA bias current present at each of the inputs. Note that the IN+ and IN– inputs are able to withstand full common-mode voltage under all powered and under-powered conditions. An example shutdown circuit is illustrated in Figure 20.

RFI/EMI

Attention to good layout practices is always recommended. Keep traces short and, when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Small ceramic capacitors placed directly across amplifier inputs can reduce RFI/EMI sensitivity. PCB layout should locate the amplifier as far away as possible from RFI sources. Sources can include other components in the same system as the amplifier itself, such as inductors (particularly switched inductors handling a lot of current and at high frequencies). RFI can generally be identified as a variation in offset voltage or dc signal levels with changes in the interfering RF signal. If the amplifier cannot be located away from sources of radiation, shielding may be needed. Twisting wire input leads makes them more resistant to RF fields. The difference in input pin location of the INA271 versus the INA193–INA198 may provide different EMI performance.

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(1) 74HC04 is not tested or characterized at 210°C.

Figure 20. INA271 Example Shutdown Circuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA271SHKJ	ACTIVE	CFP	HKJ	8	25	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 210	INA271 SHKJ	Samples
INA271SHKQ	ACTIVE	CFP	HKQ	8	25	RoHS & Green	AU	N / A for Pkg Type	-55 to 210	INA271S HKQ	Samples
INA271SKGD1	ACTIVE	XCEPT	KGD	0	252	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 210		Samples
INA271SKGD2	ACTIVE	XCEPT	KGD	0	10	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 210		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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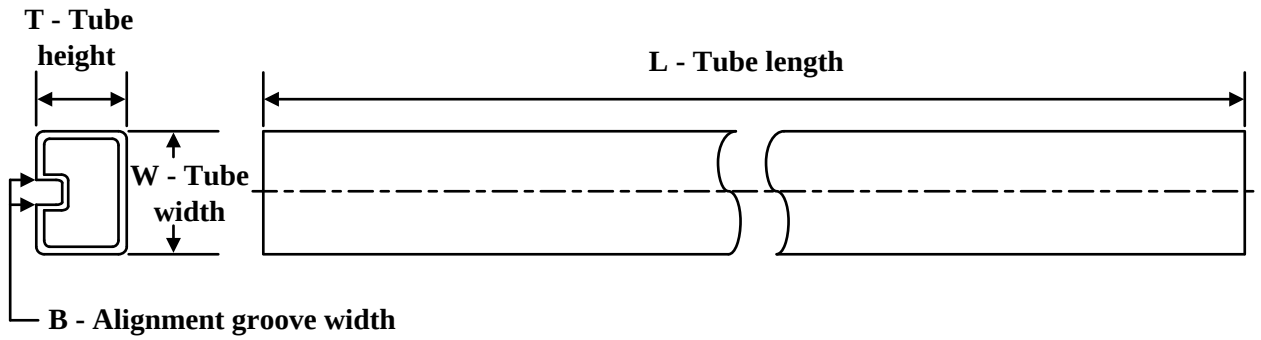
OTHER QUALIFIED VERSIONS OF INA271-HT :

- Catalog : INA271

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

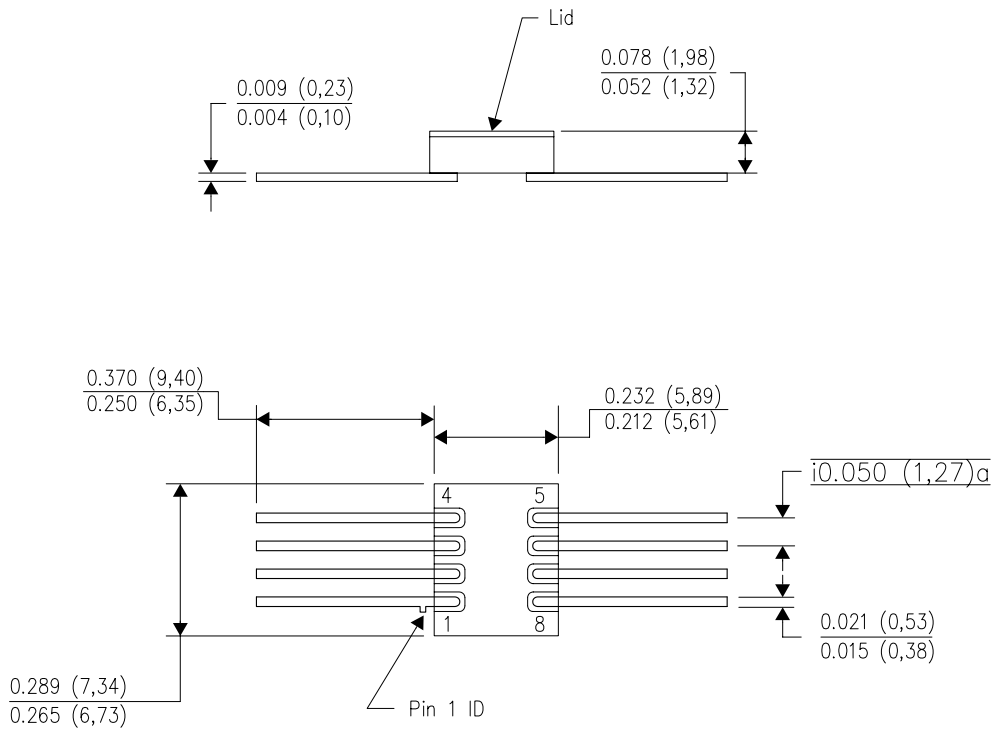
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA271SHKJ	HKJ	CFP	8	25	506.98	26.16	6220	NA
INA271SHKQ	HKQ	CFP	8	25	506.98	26.16	6220	NA

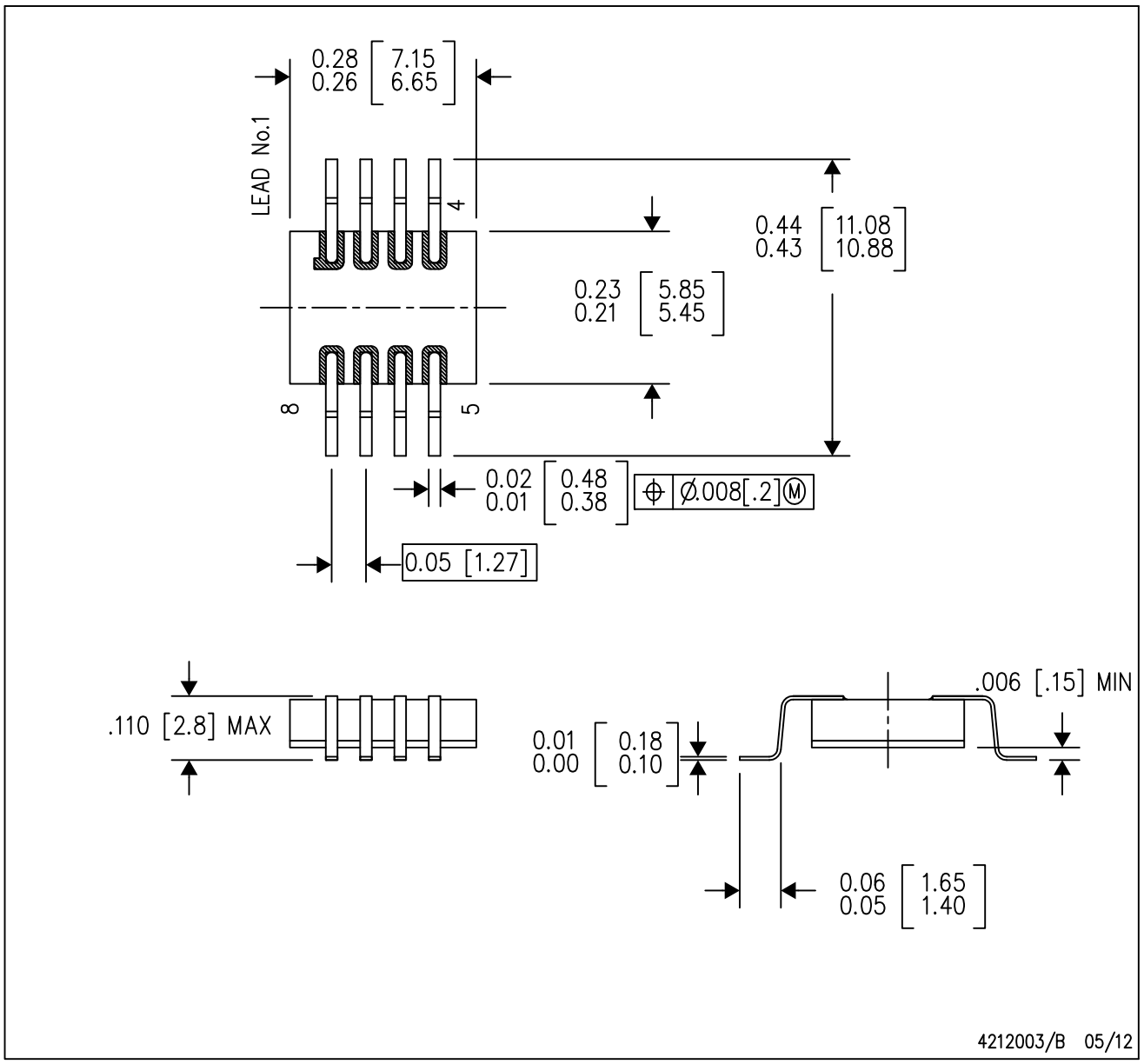
HKJ (R–CDFP–F8) CERAMIC DUAL FLATPACK



4209892/A 10/08

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.

HKQ (R–CDFP–G8) CERAMIC GULL WING



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.
E. Lid is not connected to any lead.

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