TEXAS INSTRUMENTS

ISO721, ISO721M, ISO722, ISO722M

SLLS629L – JANUARY 2006 – REVISED OCTOBER 2015

ISO72x Single Channel High-Speed Digital Isolators

1 Features

- 100 and 150-Mbps Signaling Rate Options
- Low Propagation Delay
- Low Pulse Skew
- Low-Power Sleep Mode
- High Electromagnetic Immunity
- Low Input-Current Requirement
- Failsafe Output
- Drop-In Replacement for Most Opto and Magnetic Isolators
- Operates from 3.3 V and 5 V Supplies
- -40°C to 125°C Operating Temperature Range
- 50 kV/µs Transient Immunity, Typical
- Safety and Regulatory Approvals
  - VDE Basic Insulation with 4000-V_{PK} V_{IOTM}, 560 V_{PK} V_{IORM}
  - 2500 V_{RMS} Isolation per UL 1577
  - CSA Approved for Component Acceptance Notice 5A and IEC 60950-1

2 Applications

- Industrial Fieldbus
  - Modbus
  - Profibus
  - DeviceNet™ Data Buses
  - Smart Distributed Systems (SDS™)
- Computer Peripheral Interface
- Servo Control Interface
- Data Acquisition

3 Description

The ISO721, ISO721M, ISO722, and ISO722M are digital isolators with a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier. This barrier provides galvanic isolation of up to 4000 V_{PK} per VDE. Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuits from entering the local ground, and interfering with or damaging sensitive circuitry.

A binary input signal is conditioned, translated to a balanced signal, then differentiated by the capacitive isolation barrier. Across the isolation barrier, a differential comparator receives the logic transition information, then sets or resets a flip-flop and the output circuit accordingly. A periodic update pulse is sent across the barrier to ensure the proper dc level of the output. If this dc-refresh pulse is not received for more than 4 µs, the input is assumed to be unpowered or not being actively driven, and the failsafe circuit drives the output to a logic-high state.

The symmetry of the dielectric and capacitor within the integrated circuitry provides for close capacitive matching, and allows fast transient voltage changes between the input and output grounds without corrupting the output. The small capacitance and resulting time constant provide for fast operation with signaling rates from 0 Mbps (DC) to 100 Mbps for the ISO721 and the ISO722 devices, and 0 Mbps to 150 Mbps with the ISO721M and the ISO722M devices.

These devices require two supply voltages of 3.3 V, 5 V, or any combination. All inputs are 5-V tolerant when supplied from a 3.3-V supply and all outputs are 4 mA CMOS.

The ISO722 and ISO722M devices include an active-low output enable that when driven to a high logic level, places the output in a high-impedance state and turns off internal bias circuitry to conserve power.

Both the ISO721 and ISO722 devices have TTL input thresholds and a noise filter at the input that prevent transient pulses of up to 2 ns in duration from being passed to the output of the device.

The ISO721M and ISO722M devices have CMOS V_{CC} / 2 input thresholds, but do not have the noise-filter and the additional propagation delay. These features of the ISO721M device also provide for reduced-jitter operation.

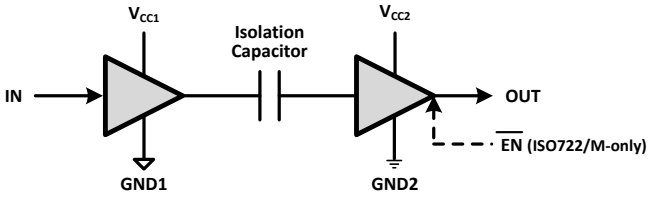
The ISO721, ISO721M, ISO722, and ISO722M devices are characterized for operation over the ambient temperature range of –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO721	SOP (8)	9.50mm x 6.57mm
ISO721	SOIC (8)	4.90mm x 3.91mm
ISO721M		
ISO722		
ISO722M		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision K (February 2012) to Revision L — **Page**

- Moved Power Dissipation metric into new table, called Power Dissipation ... 8
- Added header row above "V_{IORM}" row with the text "DIN V VDE V 0884-10 (VDE V 0884-10):2006-12" in the Insulation Characteristics table. ... 19
- Added "UL 1577" header row over "V_{ISO}" row in the Insulation Characteristics table. ... 19
- Moved "V_{ISO}" row to the bottom of the Insulation Characteristics table. ... 19
- Deleted "per UL" in "Isolation voltage" in the Insulation Characteristics table. ... 19
- Changed the D-8 MIN value of L(101) from "4.8" to "4" in the Package Insulation Characteristics table. ... 20
- Changed the D-8 MIN value of L(102) from "4.3" to "4" in the Package Insulation Characteristics table. ... 20
- Changed Test Condition "DIN IEC 60112/VDE 0303 Part 1" to "DIN EN 60112 (VDE 0303-11); IEC 60112" in the Package Insulation Characteristics table. ... 20
- Deleted bottom row of the Package Insulation Characteristics table. ... 20

Changes from Revision J (July 2010) to Revision K — **Page**

- Added *ESD Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and Mechanical, Packaging, and Orderable Information. ... 1
- Changed the Title From: 3.3-V / 5-V High-Speed Digital Isolators To: ISO72x Single Channel High-Speed Digital Isolators ... 1
- Changed the *Features* List ... 1
- Changed the second paragraph of the *Description* From: "4000 V" To: "4000 V_{PK} per VDE..." ... 1
- Changed the *Thermal Information* table ... 6
- Changed Figure 1 ... 13
- Changed the Basic isolation group Specification From: IIIa To: II in *IEC 60664-1 Ratings Table* ... 19

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- Changed VDE text From: "DIN EN 60747-5-5 (VDE 0884-5)" To: "DIN V VDE V 0884-10 (VDE V 0884-10):2006-12" in the *Regulatory Information* table 19
- Changed CSA File number: 1698195 To: 220991 in the *Regulatory Information* table 19
- Changed the C_{TI} MIN value From: ≥ 175 V To: 400 V in the *Package Insulation Characteristics* table. 20
- Changed R_{IO} Test Condition From: T_A < 100°C To: T_A = 25°C in *Package Insulation Characteristics* 20
- Moved the R_{IO} values from the TYP column to the MIN column of *Package Insulation Characteristics* 20
- Changed the title of Figure 16 From: θ_{JC} Thermal Derating Curve per DIN EN 60747-5-5 To: θ_{JC} Thermal Derating Curve per VDE 20
- Changed Table 1, added row X, PD, X, Undetermined 21
- Changed Table 2, added row X, PD, X, Undetermined 21
- Changed Figure 17 21

Changes from Revision I (February 2010) to Revision J **Page**

- Changed Note 1 of the *Electrical Characteristics, 5 V* table 6
- Changed Note 1 of the *Electrical Characteristics, 5 V, 3.3 V* table 7
- Changed Note 1 of the *Electrical Characteristics, 3.3 V, 5 V* table 7
- Changed Note 1 of the *Electrical Characteristics, 3.3 V* table 8
- Changed V to Vpeak in UNIT column of IEC *Insulation Characteristics* table 19
- Added row for V_{ISO} to *Insulation Characteristics* table 19
- Changed the title From: Package Characteristics To: *Package Insulation Characteristics* 20

Changes from Revision H (June 2009) to Revision I **Page**

- Changed *Features* From: 50 kV/s Transient Immunity, Typical To: 50 kV/µs Transient Immunity, Typical 1

Changes from Revision G (December 2008) to Revision H **Page**

- Changed the first paragraph of the *Description* From: "silicon oxide (SiO_2).." To: "silicon dioxide (SiO_2).." 1
- Added the DUB 8 pin package to the *Pin Configuration and Functions* 4
- Added package designators D-8 and DUB-8 to the table Descriptions/Test Conditions of the *Package Insulation Characteristics* table 20

Changes from Revision F (November 2008) to Revision G **Page**

- Changed the *Features* List From: 4000-$V_{(peak)}$ Isolation To: 4000-$V_{(peak)}$ Isolation, 560-V_{peak} V_{IORM} 1

Changes from Revision E (May 2008) to Revision F **Page**

- Changed Figure 19 text From: 20 mm max. from V_{CC1} To: 2 mm max. from V_{CC1} 23
- Changed Note in Table 3 From: The ISO72x pin 1 and pin 3 are internally connected together. Either or both may be used as V_{CC1}. To: Pin 1 should be used as V_{CC1}. Pin 3 may also be used as V_{CC1} or left open as long as Pin 1 is connected to V_{CC1} 23
- Changed Note in Table 3 From: The ISO721 and ISO721M pin 5 and pin 7 are internally connected together. Either or both may be used as GND2. To: Pin 5 should be used as GND2. Pin 7 may also be used as GND2 or left open as long as Pin 5 is connected to GND2. 23

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Changes from Revision D (February 2007) to Revision E **Page**

- Changed changed the V_{CC} MIN value From: 4.5 V To: 3 V in the *Recommended Operating Conditions* table 5
- Added Note 1 to the *Recommended Operating Conditions* table 5
- Added Note 1 to the *Electrical Characteristics, 5 V* table..... 6
- Added Note 1 to the *Electrical Characteristics, 5 V, 3.3 V* table 7
- Added Note 1 to the *Electrical Characteristics, 3.3 V, 5 V* table 7
- Added Note 1 to the *Electrical Characteristics, 3.3 V* table..... 8

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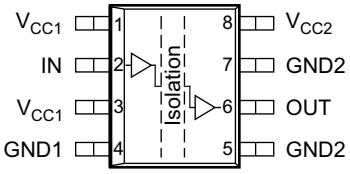
5 Device Comparison Table

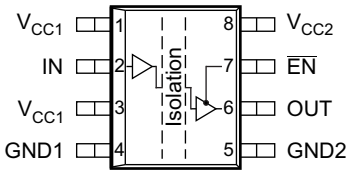
PRODUCT	SIGNALING RATE	OUTPUT ENABLED	INPUT THRESHOLDS	NOISE FILTER
ISO721	100 Mbps	NO	TTL	YES
ISO721M	150 Mbps	NO	CMOS	NO
ISO722	100 Mbps	YES	TTL	YES
ISO722M	150 Mbps	YES	CMOS	NO

6 Pin Configuration and Functions

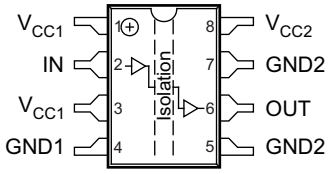
ISO721, ISO721M
SOIC (D) Package
Top View



ISO722, ISO722M
SOIC (D) Package
Top View



ISO721
SOP (DUB) Package
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	ISO721x NO.	ISO722x NO.		
V_{CC1}	1, 3	1, 3	-	Power supply, V_{CC1}
V_{CC2}	8	8	-	Power supply, V_{CC2}
IN	2	2	I	Input
OUT	6	6	O	Output
$\overline{EN}$	-	7	I	Output enable. OUT is enabled when $\overline{EN}$ is low or disconnected and disabled when $\overline{EN}$ is high.
GND1	4	4	-	Ground connection for V_{CC1}
GND2	5, 7	5	-	Ground connection for V_{CC2}

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	V_{CC1}, V_{CC2}	–0.5	6	V
V_I	Input voltage	IN, OUT, or $\overline{EN}$	–0.5	V_{CC} + 0.5(2)	V
I_O	Output current			±15	mA
T_J	Maximum junction temperature			170	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Maximum voltage must not exceed 6 V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage(1), V_{CC1}, V_{CC2}		3		5.5	V
I_{OH}	Output current				4	mA
I_{OL}			–4			mA
t_{ui}	Input pulse duration	ISO72x	10			ns
		ISO72xM	6.67			
1 / t_{ui}	Signaling Rate	ISO72x	0		100	Mbps
		ISO72xM	0		150	
V_{IH}	High-level input voltage (IN, $\overline{EN}$)	ISO72x	2		5.5	V
V_{IL}	Low-level input voltage (IN, $\overline{EN}$)		0		0.8	V
V_{IH}	High-level input voltage (IN, $\overline{EN}$)	IOS72xM	0.7 V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage (IN, $\overline{EN}$)		0		0.3 V_{CC}	V
T_A	Ambient temperature		–40	25	125	°C
T_J	Junction temperature	See *Thermal Information*			150	°C
H	External magnetic field intensity per IEC 61000-4-8 and IEC 61000-4-9 certification				1000	A/m

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V. For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

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7.4 Thermal Information

THERMAL METRIC[1]			ISO721 DUB 8 PINS	ISO72x D 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	High-K Board	86.6	114.7	°C/W
		Low-K Board	N/A	263	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		70.3	63	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		50.2	54.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter		34.3	18.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter		49.8	54.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics, 5 V

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	Quiescent	V_I = V_{CC} or 0 V, no load			0.5	1	mA
		25 Mbps				2	4	
I_{CC2}	V_{CC2} supply current	ISO722/722M Sleep Mode	V_I = V_{CC} or 0 V, No load	$\overline{EN}$ at V_{CC}			200	µA
		Quiescent		$\overline{EN}$ at 0 V or ISO721/721M		8	12	mA
		25 Mbps	V_I = V_{CC} or 0 V, no load			10	14	
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 10		V_{CC} – 0.8	4.6		V
			I_{OH} = –20 µA, See Figure 10		V_{CC} – 0.1	5		
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 10			0.2	0.4	V
			I_{OL} = 20 µA, See Figure 10			0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		$\overline{EN}$, IN at 2 V				10	µA
I_{IL}	Low-level input current		$\overline{EN}$, IN at 0.8 V		–10			
I_{OZ}	High-impedance output current	ISO722, ISO722M	$\overline{EN}$, IN at V_{CC}				1	µA
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4 × 10^6πt)			1		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 14		25	50		kV/µs

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7.6 Electrical Characteristics, 5 V, 3.3 V

V_{CC1} at 5 V ± 10%, V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	Quiescent	V_I = V_{CC} or 0 V, no load			0.5	1	mA
		25 Mbps				2	4	
I_{CC2}	V_{CC2} supply current	ISO722/722M Sleep mode	V_I = V_{CC} or 0 V, No load	$\overline{EN}$ at V_{CC}			150	µA
		Quiescent		$\overline{EN}$ at 0 V or ISO721/721M		4	6.5	mA
		25 Mbps	V_I = V_{CC} or 0 V, no load			5	7.5	
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 10		V_{CC} – 0.4	3		V
			I_{OH} = –20 µA, See Figure 10		V_{CC} – 0.1	3.3		
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 10			0.2	0.4	V
			I_{OL} = 20 µA, See Figure 10			0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		$\overline{EN}$, IN at 2 V				10	µA
I_{IL}	Low-level input current		$\overline{EN}$, IN at 0.8 V		–10			µA
I_{OZ}	High-impedance output current	ISO722, ISO722M	$\overline{EN}$, IN at V_{CC}				1	µA
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4 × 10^6πt)			1		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 14		25	40		kV/µs

7.7 Electrical Characteristics, 3.3 V, 5 V

V_{CC1} at 3.3 V ± 10%, V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	Quiescent	V_I = V_{CC} or 0 V, no load			0.3	0.5	mA
		25 Mbps				1	2	
I_{CC2}	V_{CC2} supply current	ISO722/722M Sleep mode	V_I = V_{CC} or 0 V, No load	$\overline{EN}$ at V_{CC}			200	µA
		Quiescent		$\overline{EN}$ at 0 V or ISO721/721M		8	12	mA
		25 Mbps	V_I = V_{CC} or 0 V, No load			10	14	
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 10		V_{CC} – 0.8	4.6		V
			I_{OH} = –20 µA, See Figure 10		V_{CC} – 0.1	5		
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 10			0.2	0.4	V
			I_{OL} = 20 µA, See Figure 10			0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		$\overline{EN}$, IN at 2 V				10	µA
I_{IL}	Low-level input current		$\overline{EN}$, IN at 0.8 V		–10			µA
I_{OZ}	High-impedance output current	ISO722, ISO722M	$\overline{EN}$, IN at V_{CC}				1	µA
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4 × 10^6πt)			1		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 14		25	40		kV/µs

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7.8 Electrical Characteristics, 3.3 V

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	Quiescent	V_I = V_{CC} or 0 V, no load			0.3	0.5	mA
		25 Mbps				1	2	
I_{CC2}	V_{CC2} supply current	ISO722/722M Sleep Mode	V_I = V_{CC} or 0 V, No load	$\overline{EN}$ at V_{CC}			150	µA
		Quiescent		$\overline{EN}$ at 0 V or ISO721/721M		4	6.5	mA
		25 Mbps	V_I = V_{CC} or 0 V, no load			5	7.5	
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 10		V_{CC} – 0.4	3		V
			I_{OH} = –20 µA, See Figure 10		V_{CC} – 0.1	3.3		
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 10			0.2	0.4	V
			I_{OL} = 20 µA, See Figure 10			0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		$\overline{EN}$, IN at 2 V				10	µA
I_{IL}	Low-level input current		$\overline{EN}$, IN at 0.8 V		–10			µA
I_{OZ}	High-impedance output current	ISO722, ISO722M	$\overline{EN}$, IN at V_{CC}				1	µA
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4 × 10^6πt)			1		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V, See Figure 14		25	40		kV/µs

7.9 Power Dissipation

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	ISO721 DUB 8 PINS	ISO72x D 8 PINS	UNIT
P_D	Power Dissipation	ISO72x	VCC1 = VCC2 = 5.5 V, TJ = 150°C, CL = 15 pF, Input a 100-Mbps 50% duty-cycle square wave		159	mW
		ISO72xM	VCC1 = VCC2 = 5.5 V, TJ = 150°C, CL = 15 pF, Input a 100-Mbps 50% duty-cycle square wave		195	mW
		ISO721	VCC1 = VCC2 = 5.5 V, TJ = 150°C, CL = 15 pF, Input a 100-Mbps 50% duty-cycle square wave	159		mW

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7.10 Switching Characteristics, 5 V

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high-level output	ISO72x	$\overline{EN}$ at 0 V, See Figure 10	13	17	24	ns
t_{PHL}	Propagation delay, high-to-low-level output	ISO72x	$\overline{EN}$ at 0 V, See Figure 10	13	17	24	ns
$t_{sk(p)}$	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$	ISO72x	$\overline{EN}$ at 0 V, See Figure 10		0.5	2	ns
t_{PLH}	Propagation delay, low-to-high-level output	ISO72xM	$\overline{EN}$ at 0 V, See Figure 10	8	10	16	ns
t_{PHL}	Propagation delay, high-to-low-level output	ISO72xM	$\overline{EN}$ at 0 V, See Figure 10	8	10	16	ns
$t_{sk(p)}$	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$	ISO72xM	$\overline{EN}$ at 0 V, See Figure 10		0.5	1	ns
$t_{sk(pp)}$ (1)	Part-to-part skew				0	3	ns
t_r	Output signal rise time		$\overline{EN}$ at 0 V, See Figure 10		1		ns
t_f	Output signal fall time		$\overline{EN}$ at 0 V, See Figure 10		1		ns
t_{pHZ}	Sleep-mode propagation delay, high-level-to-high-mpedance output	ISO722 ISO722M	See Figure 11	6	8	15	ns
t_{pZH}	Sleep-mode propagation delay, high-impedance-to-high-level output	ISO722 ISO722M	See Figure 11	3.5	4	8	µs
t_{pLZ}	Sleep-mode propagation delay, low-level-to-high-impedance output	ISO722 ISO722M	See Figure 12	5.5	8	15	ns
t_{pZL}	Sleep-mode propagation delay, high-impedance-to-low-level output	ISO722 ISO722M	See Figure 12	4	5	8	µs
t_{fs}	Failsafe output delay time from input power loss		See Figure 13		3		µs
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter	ISO72x	100-Mbps NRZ data input, See Figure 15		2		ns
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter	ISO72x	100-Mbps unrestricted bit run length data input, See Figure 15		3		ns
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter	ISO72xM	150-Mbps NRZ data input, See Figure 15		1		ns
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter	ISO72xM	150-Mbps unrestricted bit run length data input, See Figure 15		2		ns

(1) $t_{sk(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

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7.11 Switching Characteristics, 5 V, 3.3 V

V_{CC1} at 5 V ± 10%, V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high-level output	ISO72x	$\overline{EN}$ at 0 V, See Figure 10	15	19	30	ns
t_{PHL}	Propagation delay , high-to-low-level output	ISO72x	$\overline{EN}$ at 0 V, See Figure 10	15	19	30	ns
$t_{sk(p)}$	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$	ISO72x	$\overline{EN}$ at 0 V, See Figure 10		0.5	3	ns
t_{PLH}	Propagation delay, low-to-high-level output	ISO72xM	$\overline{EN}$ at 0 V, See Figure 10	10	12	20	ns
t_{PHL}	Propagation delay, high-to-low-level output	ISO72xM	$\overline{EN}$ at 0 V, See Figure 10	10	12	20	ns
$t_{sk(p)}$	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$	ISO72xM	$\overline{EN}$ at 0 V, See Figure 10		0.5	1	ns
$t_{sk(pp)}$ (1)	Part-to-part skew				0	5	ns
t_r	Output signal rise time		$\overline{EN}$ at 0 V, See Figure 10		2		ns
t_f	Output signal fall time		$\overline{EN}$ at 0 V, See Figure 10		2		ns
t_{pHZ}	Sleep-mode propagation delay, high-level-to-high-mpedance output	ISO722 ISO722M	See Figure 11	7	11	25	ns
t_{pZH}	Sleep-mode propagation delay, high-impedance-to-high-level output	ISO722 ISO722M	See Figure 11	4.5	6	8	µs
t_{pLZ}	Sleep-mode propagation delay, low-level-to-high-impedance output	ISO722 ISO722M	See Figure 12	7	13	25	ns
t_{pZL}	Sleep-mode propagation delay, high-impedance-to-low-level output	ISO722 ISO722M	See Figure 12	4.5	6	8	µs
t_{fs}	Failsafe output delay time from input power loss		See Figure 13		3		µs
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter	ISO72x	100-Mbps NRZ data input, See Figure 15		2		ns
		ISO72x	100-Mbps unrestricted bit run length data input, See Figure 15		3		ns
		ISO72xM	150-Mbps NRZ data input, See Figure 15		1		ns
		ISO72xM	150-Mbps unrestricted bit run length data input, See Figure 15		2		ns

(1) $t_{sk(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

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7.12 Switching Characteristics, 3.3 V, 5 V

V_{CC1} at 3.3 V ± 10%, V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high-level output	ISO72x	$\overline{EN}$ at 0 V, See Figure 10	15	17	30	ns
t_{PHL}	Propagation delay , high-to-low-level output	ISO72x	$\overline{EN}$ at 0 V, See Figure 10	15	17	30	ns
$t_{sk(p)}$	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$	ISO72x	$\overline{EN}$ at 0 V, See Figure 10		0.5	2	ns
t_{PLH}	Propagation delay, low-to-high-level output	ISO72xM	$\overline{EN}$ at 0 V, See Figure 10	10	12	21	ns
t_{PHL}	Propagation delay, high-to-low-level output	ISO72xM	$\overline{EN}$ at 0 V, See Figure 10	10	12	21	ns
$t_{sk(p)}$	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$	ISO72xM	$\overline{EN}$ at 0 V, See Figure 10		0.5	1	ns
$t_{sk(pp)}$ (1)	Part-to-part skew				0	5	ns
t_r	Output signal rise time		$\overline{EN}$ at 0 V, See Figure 10		1		ns
t_f	Output signal fall time		$\overline{EN}$ at 0 V, See Figure 10		1		ns
t_{pHZ}	Sleep-mode propagation delay, high-level-to-high-mpedance output	ISO722 ISO722M	See Figure 11	7	9	15	ns
t_{pZH}	Sleep-mode propagation delay, high-impedance-to-high-level output	ISO722 ISO722M	See Figure 11	4.5	5	8	µs
t_{pLZ}	Sleep-mode propagation delay, low-level-to-high-impedance output	ISO722 ISO722M	See Figure 12	7	9	15	ns
t_{pZL}	Sleep-mode propagation delay, high-impedance-to-low-level output	ISO722 ISO722M	See Figure 12	4.5	5	8	µs
t_{fs}	Failsafe output delay time from input power loss		See Figure 13		3		µs
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter	ISO72x	100-Mbps NRZ data input, See Figure 15		2		ns
		ISO72x	100-Mbps unrestricted bit run length data input, See Figure 15		3		ns
		ISO72xM	150-Mbps NRZ data input, See Figure 15		1		ns
		ISO72xM	150-Mbps unrestricted bit run length data input, See Figure 15		2		ns

(1) $t_{sk(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

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7.13 Switching Characteristics, 3.3 V

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high-level output	ISO72x	$\overline{EN}$ at 0 V, See Figure 10	17	20	34	ns
t_{PHL}	Propagation delay , high-to-low-level output	ISO72x	$\overline{EN}$ at 0 V, See Figure 10	17	20	34	ns
$t_{sk(p)}$	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$	ISO72x	$\overline{EN}$ at 0 V, See Figure 10		0.5	3	ns
t_{PLH}	Propagation delay, low-to-high-level output	ISO72xM	$\overline{EN}$ at 0 V, See Figure 10	10	12	25	ns
t_{PHL}	Propagation delay, high-to-low-level output	ISO72xM	$\overline{EN}$ at 0 V, See Figure 10	10	12	25	ns
$t_{sk(p)}$	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$	ISO72xM	$\overline{EN}$ at 0 V, See Figure 10		0.5	1	ns
$t_{sk(pp)}$ (1)	Part-to-part skew				0	5	ns
t_r	Output signal rise time		$\overline{EN}$ at 0 V, See Figure 10		2		ns
t_f	Output signal fall time		$\overline{EN}$ at 0 V, See Figure 10		2		ns
t_{pHZ}	Sleep-mode propagation delay, high-level-to-high-mpedance output	ISO722 ISO722M	See Figure 11	7	13	25	ns
t_{pZH}	Sleep-mode propagation delay, high-impedance-to-high-level output	ISO722 ISO722M	See Figure 11	5	6	8	µs
t_{pLZ}	Sleep-mode propagation delay, low-level-to-high-impedance output	ISO722 ISO722M	See Figure 12	7	13	25	ns
t_{pZL}	Sleep-mode propagation delay, high-impedance-to-low-level output	ISO722 ISO722M	See Figure 12	5	6	8	µs
t_{fs}	Failsafe output delay time from input power loss		See Figure 13		3		µs
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter	ISO72x	100-Mbps NRZ data input, See Figure 15		2		ns
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter	ISO72x	100-Mbps unrestricted bit run length data input, See Figure 15		3		ns
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter	ISO72xM	150-Mbps NRZ data input, See Figure 15		1		ns
$t_{jit(PP)}$	Peak-to-peak eye-pattern jitter	ISO72xM	150-Mbps unrestricted bit run length data input, See Figure 15		2		ns

(1) $t_{sk(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

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7.14 Typical Characteristics

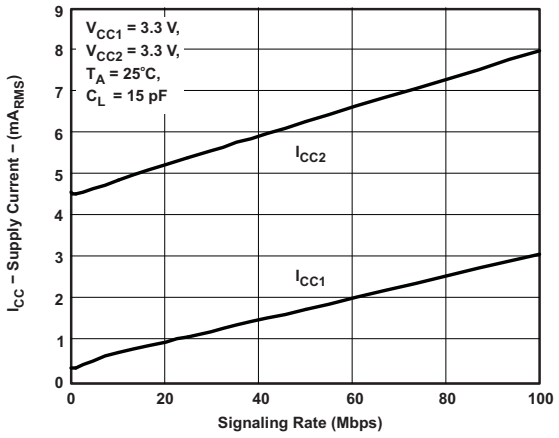

Figure 1. RMS Supply Current vs Signaling Rate

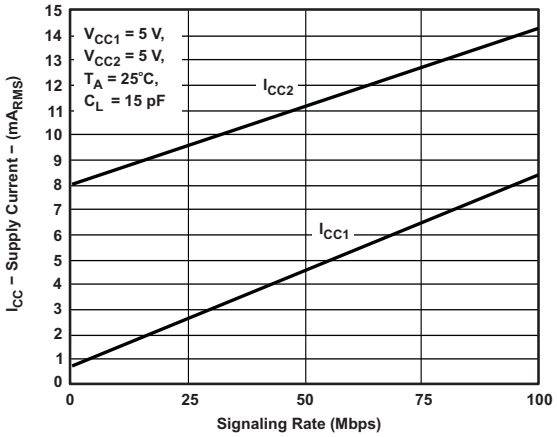

Figure 2. RMS Supply Current vs Signaling Rate

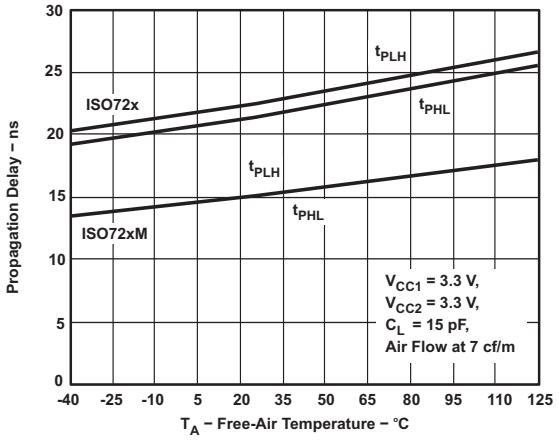

Figure 3. Propagation Delay vs Free-Air Temperature

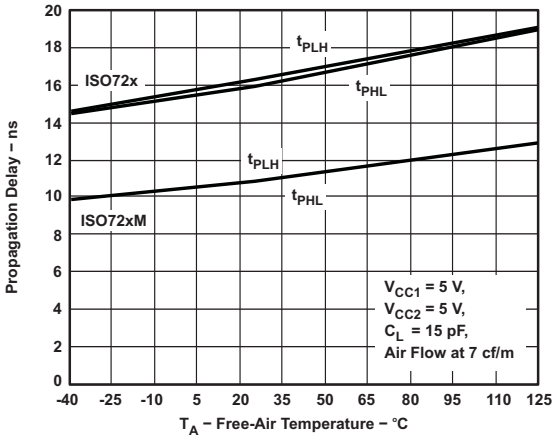

Figure 4. Propagation Delay vs Free-Air Temperature

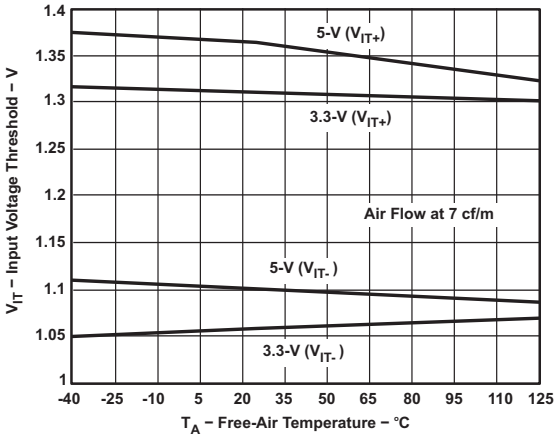

Figure 5. ISO72x Input Threshold Voltage vs Free-Air Temperature

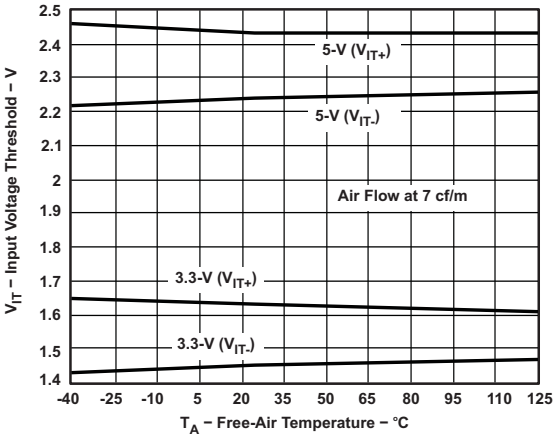

Figure 6. ISO72xM Input Threshold Voltage vs Free-Air Temperature

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Typical Characteristics (continued)

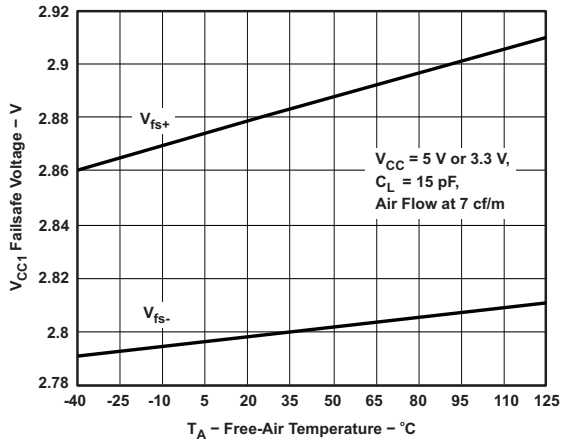

Figure 7. V_{CC1} Failsafe Threshold Voltage vs Free-Air Temperature

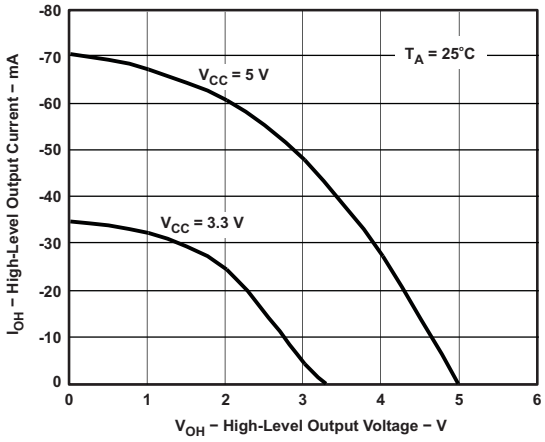

Figure 8. High-Level Output Current vs High-Level Output Voltage

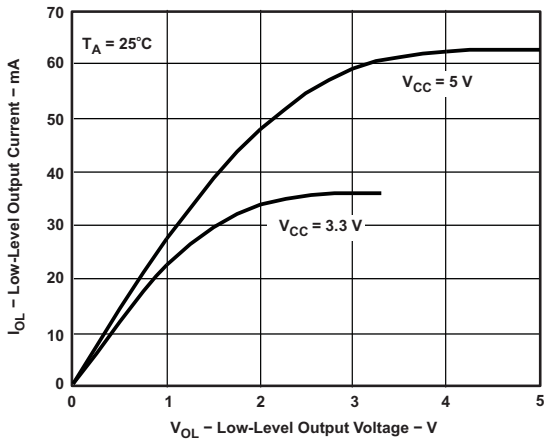

Figure 9. Low-Level Output Current vs Low-Level Output Voltage

8 Parameter Measurement Information

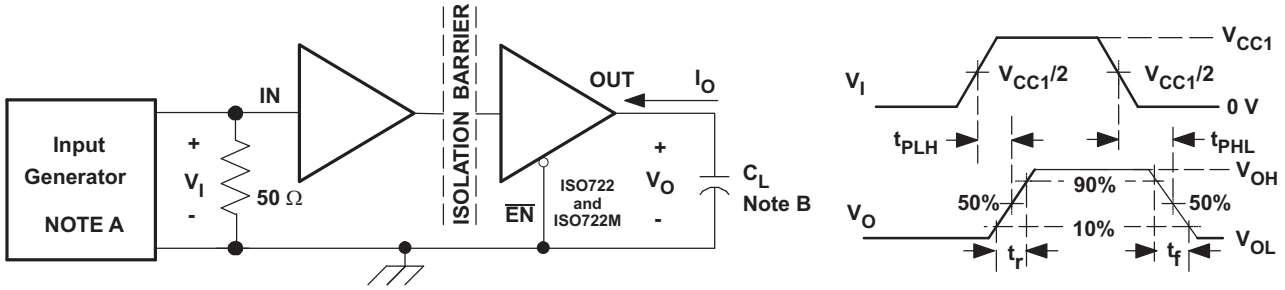

Figure 10. Switching Characteristic Test Circuit and Voltage Waveforms

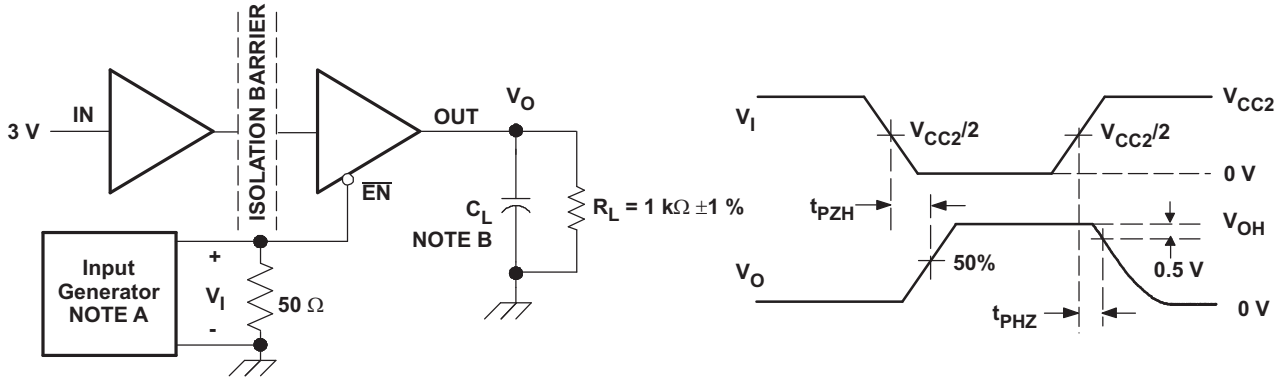

Figure 11. ISO722 Sleep-Mode High-Level Output Test Circuit and Voltage Waveforms

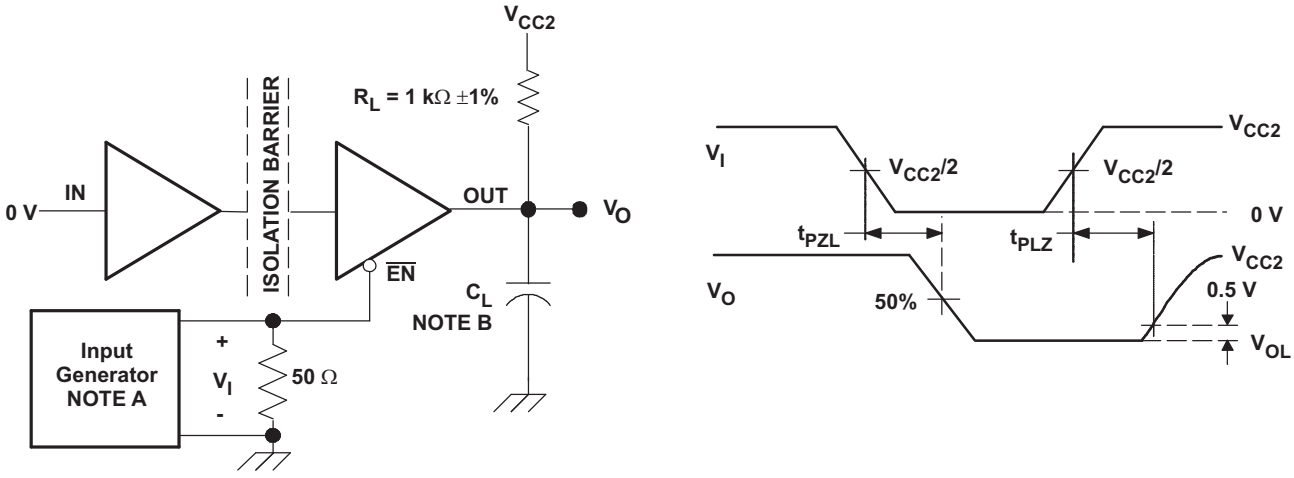

Figure 12. ISO722 Sleep-Mode Low-Level Output Test Circuit and Voltage Waveforms

NOTE

A: The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B: C_L = 15 pF ± 20% and includes instrumentation and fixture capacitance.

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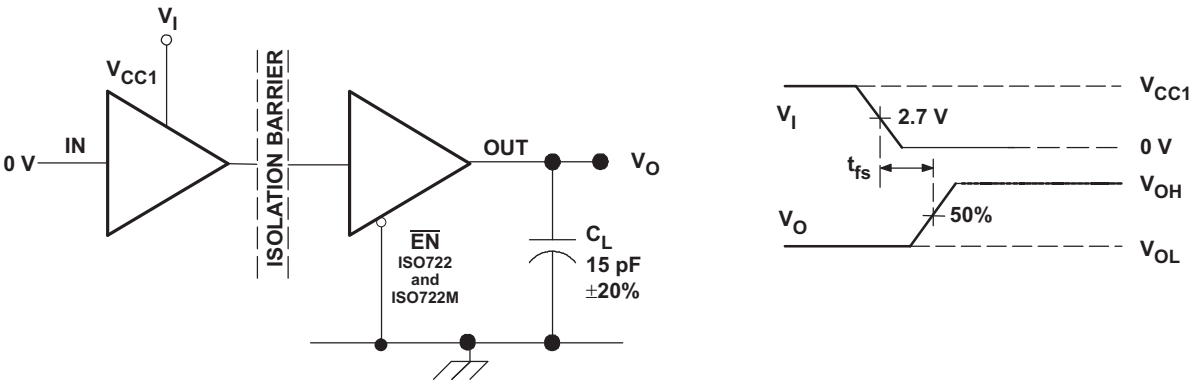
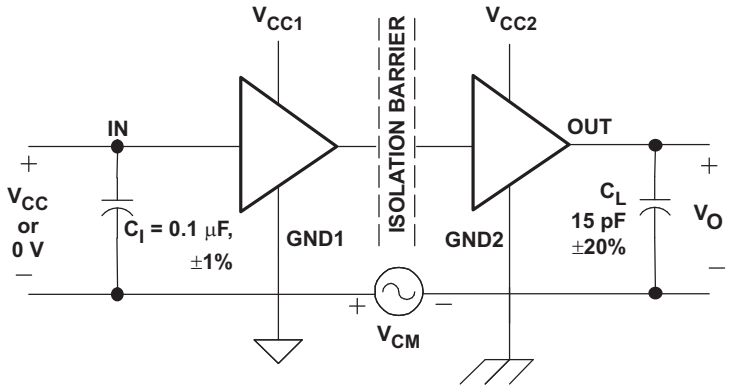
Parameter Measurement Information (continued)



NOTE: V_I transition time is 100 ns.

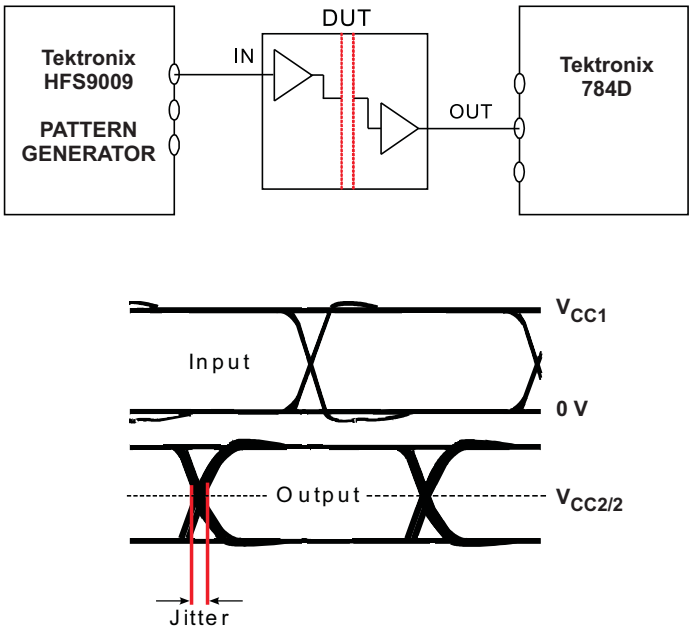
Figure 13. Failsafe Delay Time Test Circuit and Voltage Waveforms



NOTE: Pass/fail criterion is no change in V_O.

Figure 14. Common-Mode Transient-Immunity Test Circuit and Voltage Waveform

Parameter Measurement Information (continued)



NOTE: Bit pattern run length is $2^{16} - 1$. Transition time is 800 ps. NRZ data input has no more than five consecutive 1s or 0s.

Figure 15. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform

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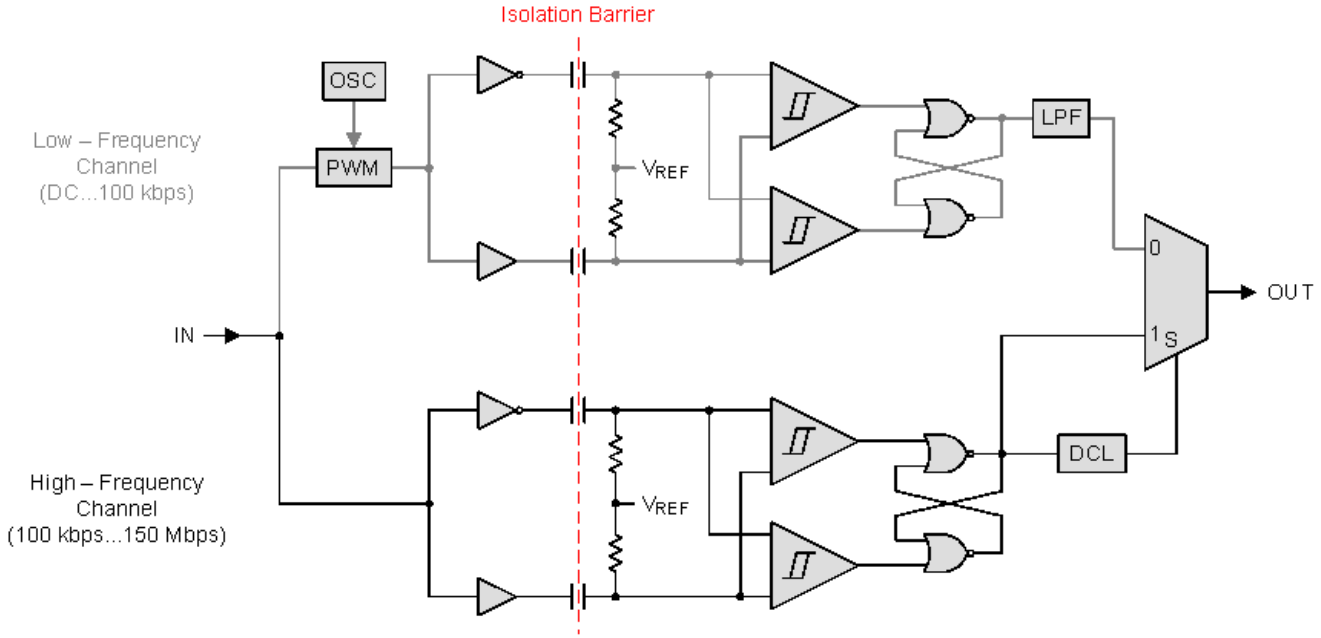
9 Detailed Description

9.1 Overview

The isolator in the *Functional Block Diagram* is based on a capacitive isolation barrier technique. The I/O channel of the device consists of two internal data channels, a high-frequency channel (HF) with a bandwidth from 100 kbps up to 150 Mbps, and a low-frequency channel (LF) covering the range from 100 kbps down to DC. In principle, a single ended input signal entering the HF-channel is split into a differential signal via the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transients, which then are converted into differential pulses by two comparators. The comparator outputs drive a NOR-gate flip-flop whose output feeds an output multiplexer. A decision logic (DCL) at the driving output of the flip-flop measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, (as in the case of a low-frequency signal), the DCL forces the output-multiplexer to switch from the high-frequency to the low-frequency channel.

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, creating a sufficiently high-frequency signal capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before passing the carrier on to the output multiplexer.

9.2 Functional Block Diagram



9.3 Features Description

Insulation characteristics and regulatory information of ISO72x family is provided in this section.

9.3.1 Insulation Characteristics

over recommended operating conditions (unless otherwise noted.)

PARAMETER		TEST CONDITIONS	SPECIFICATIONS	UNIT
DIN V VDE V 0884-10 (VDE V 0884-10):2006-12(1)				
V_{IORM}	Maximum working insulation voltage		560	Vpeak
V_{PR}	Input to output test voltage	After Input/Output Safety Test Subgroup 2/3 $V_{PR} = V_{IORM} \times 1.2$, t = 10 s, Partial discharge < 5 pC	672	Vpeak
		Method a, $V_{PR} = V_{IORM} \times 1.6$, Type and sample test with t = 10 s, Partial discharge < 5 pC	896	Vpeak
		Method b1, $V_{PR} = V_{IORM} \times 1.875$, 100% production test with t = 1 s, Partial discharge < 5 pC	1050	Vpeak
V_{IOTM}	Transient overvoltage	t = 60 s	4000	Vpeak
R_S	Insulation resistance	V_{IO} = 500 V at T_S	> 10^9	Ω
	Pollution degree		2	
UL 1577				
V_{ISO}	Isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification)	3535 / 2500	Vpeak/Vrms
		$V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)(2)	4242 / 3000	

(1) Climatic classification 40/125/21
(2) Based on lifetime curve (see the *High-Voltage Lifetime of the ISO72x Family of Digital Isolators* application report, SLLA197); these devices can withstand 4242 Vpeak / 3000 Vrms for > 10,000 s at 150°C.

9.3.2 IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage ≤150 VRMS	I-IV
	Rated mains voltage ≤300 VRMS	I-III

9.3.3 Regulatory Information

VDE	CSA	UL
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 61010-1 (VDE 0411-1)	Approved according to CSA Component Acceptance Notice 5A and IEC 60950-1	Recognized under UL 1577 Component Recognition Program
Basic Insulation Maximum Transient Overvoltage, 4000 V_{PK} Maximum Working Voltage, 560 V_{PK} Maximum Surge Voltage, 4000 V_{PK}	Evaluated to CSA 60950-1-07 and IEC 60950-1 (2nd Ed) with 2000 V_{RMS} Isolation rating for products with working voltages ≤ 125 V_{RMS} for reinforced insulation and ≤ 390 V_{RMS} for basic insulation	Single Protection, 2500 V_{RMS}(1)
Certificate number: 40016131	Master contract number: 220991	File number: E181974

(1) Production tested ≥ 3000 V_{RMS} for 1 second in accordance with UL 1577.

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9.3.4 Package Insulation Characteristics

PARAMETER		DESCRIPTIONS / TEST CONDITIONS		MIN	TYP	MAX	UNIT
L(101)	Minimum air gap (clearance)(1)	Shortest terminal-to-terminal distance through air	D-8	4			mm
			DUB-8	6.1			
L(102)	Minimum external tracking (creepage)(1)	Shortest terminal-to-terminal distance across the package surface	D-8	4			mm
			DUB-8	6.8			
CTI	Tracking resistance (comparative tracking index)	DIN EN 60112 (VDE 0303-11); IEC 60112		400			V
DTI	Distance through insulation	Minimum internal gap (internal clearance)		0.008			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V; all pins on each side of the barrier tied together, creating a two-terminal device; T_A = 25°C		10^{12}			Ω
		Input to output, V_{IO} = 500 V, 100°C ≤ T_A < T_A max.		10^{11}			Ω
C_{IO}	Barrier capacitance Input-to-output	V_I = 0.4 sin (4 × 10^6πt)			1		pF

(1) Creepage and clearance requirements are applied according to the specific equipment isolation standards of an application. Maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance.
Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the *Isolation Glossary* in the *Related Documentation* section. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

9.3.5 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply, and without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	θ_{JA} = 263°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C			100	mA
		θ_{JA} = 263°C/W, V_I = 3.6 V, T_J = 170°C, T_A = 25°C			153	
T_S	Maximum case temperature				150	°C

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed in the JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages and is conservative.

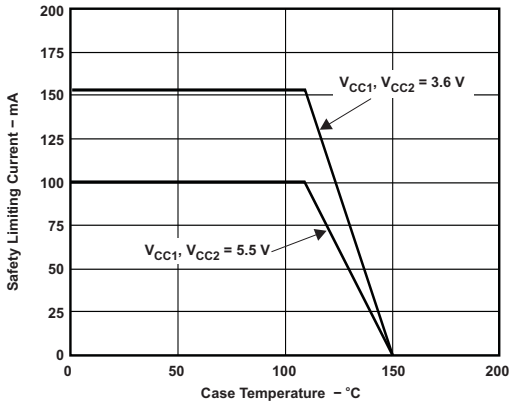

Figure 16. θ_{JC} Thermal Derating Curve per VDE

9.4 Device Functional Modes

Functional modes of ISO72x are shown in Table 1 and Table 2.

Table 1. ISO721 Functional Table

V_{CC1}	V_{CC2}	INPUT (IN)	OUTPUT (OUT)
PU	PU	H	H
		L	L
		Open	H
PD	PU	X	H
X	PD	X	Undetermined

Table 2. ISO722 Functional Table

V_{CC1}	V_{CC2}	INPUT (IN)	OUTPUT ENABLE ($\overline{EN}$)	OUTPUT (OUT)
PU	PU	H	L or open	H
		L	L or open	L
		X	H	Z
		Open	L or open	H
PD	PU	X	L or open	H
PD	PU	X	H	Z
X	PD	X	X	Undetermined

9.4.1 Device I/O Schematic

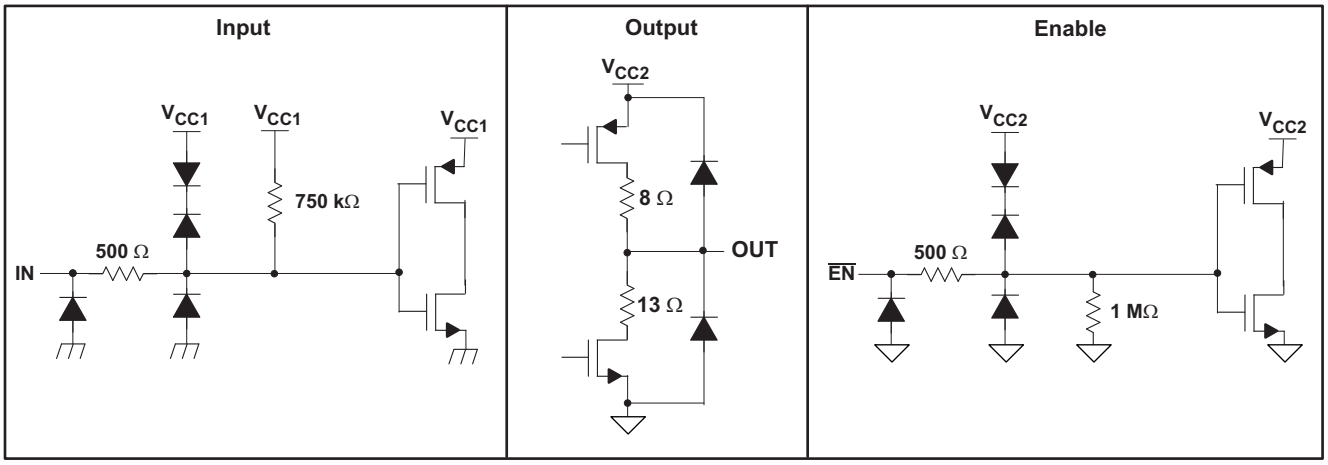

Figure 17. Equivalent Input and Output Schematic Diagrams

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10 Application and Implementation

NOTE

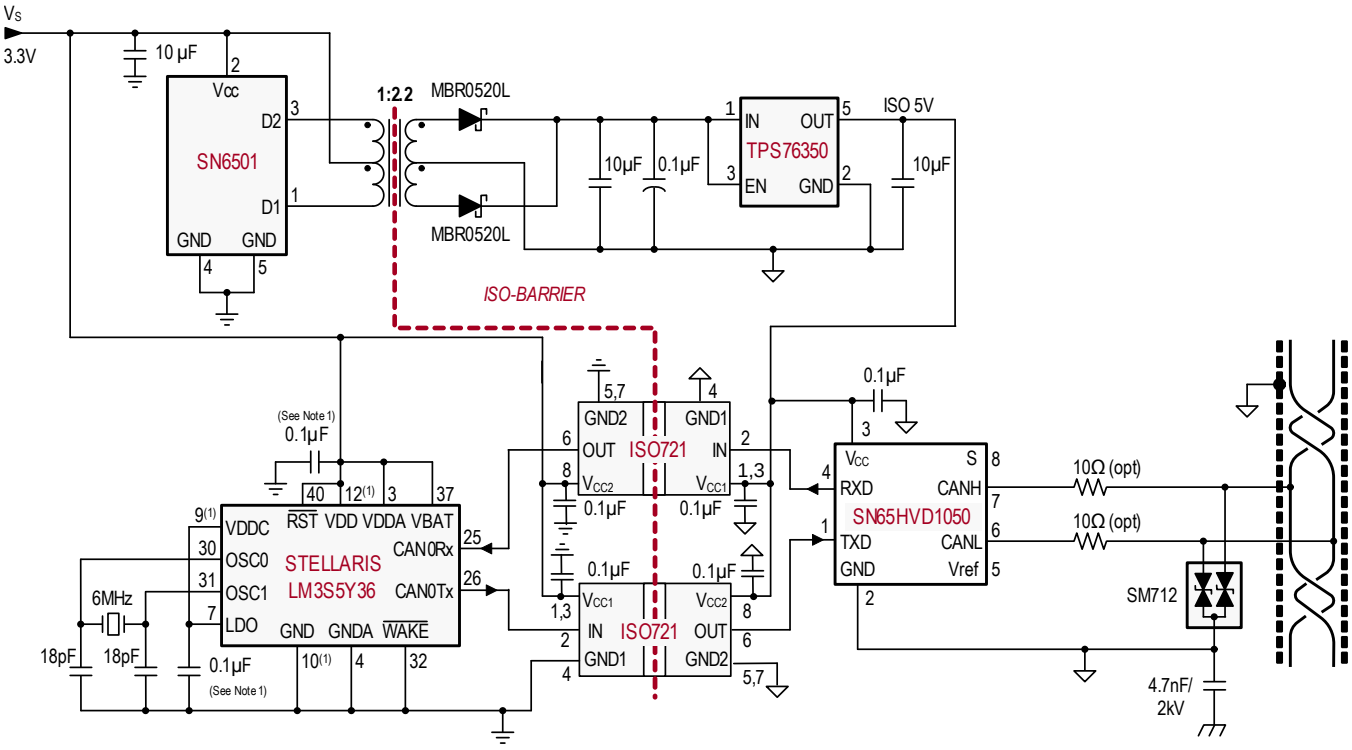
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The ISO72x devices use single-ended TTL or CMOS-logic-switching technology. The supply voltage range of the devices is from 3 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, due to the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

10.2 Typical Application

The ISO721 device can be used with Texas Instruments' microcontroller, CAN transceiver, transformer driver, and low-dropout voltage regulator to create an Isolated CAN Interface as shown in Figure 18.



(1) Multiple pins and capacitors omitted for clarity purpose.

Figure 18. Isolated CAN Interface

Typical Application (continued)

10.2.1 Design Requirements

Unlike optocouplers which need external components to improve performance and provide bias (or limit current), the ISO72x devices need only two external bypass capacitors to operate.

10.2.2 Detailed Design Procedure

Typical ISO721 circuit hook-up is shown in Figure 19.

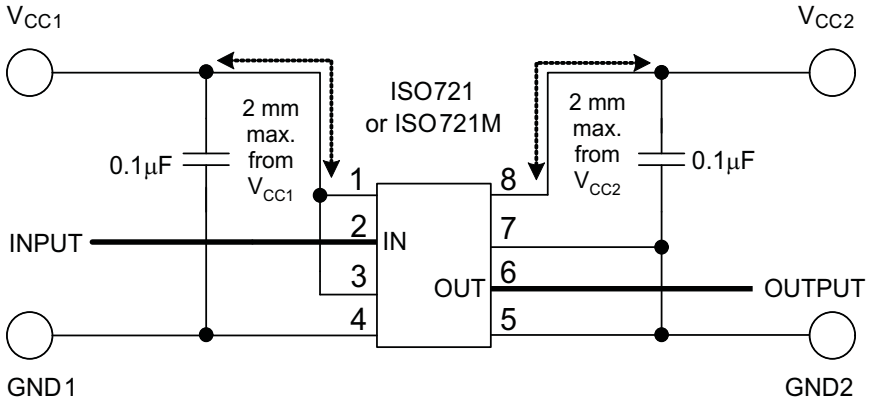


Figure 19. Typical ISO721 Circuit Hook-up

The ISO72x isolators have the same functional pinout as those of most other vendors as shown in Figure 20, and they are often pin-for-pin drop-in replacements. The notable differences in the products are propagation delay, signaling rate, power consumption, and transient protection rating. Table 3 is used as a guide for replacing other isolators with the ISO72x family of single channel isolators.

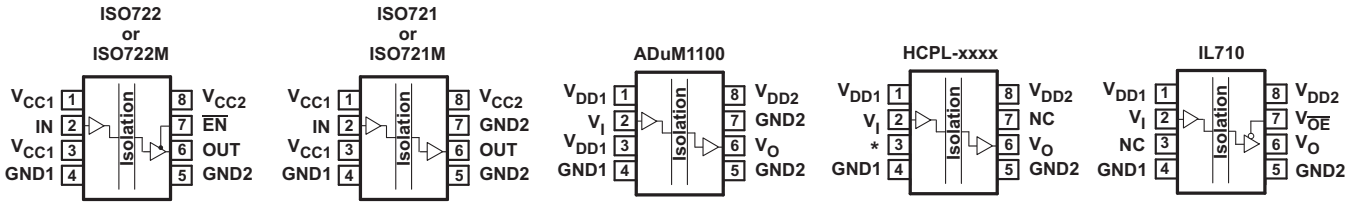


Figure 20. Pin Cross Reference

Table 3. Cross Reference

ISOLATOR	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7		PIN 8
							ISO721 OR ISO721M	ISO722 OR ISO722M	
ISO721 (1)(2)	V_{CC1}	IN	V_{CC1}	GND1	GND2	OUT	GND2	$\overline{EN}$	V_{CC2}
ADuM1100 (1)(2)	V_{DD1}	V_I	V_{DD1}	GND1	GND2	V_O	GND2		V_{DD2}
HCPL-xxxx	V_{DD1}	V_I	*Leave Open (3)	GND1	GND2	V_O	NC (4)		V_{DD2}
IL710	V_{DD1}	V_I	NC (5)	GND1	GND2	V_O	$V_{\overline{OE}}$		V_{DD2}

(1) Pin 1 should be used as V_{CC1}. Pin 3 can also be used as V_{CC1} or left open, as long as pin 1 is connected to V_{CC1}.
(2) Pin 5 should be used as GND2. Pin 7 can also be used as GND2 or left open, as long as pin 5 is connected to GND2.
(3) Pin 3 of the HCPL devices must be left open. This is not a problem when substituting an ISO72x device, because the extra V_{CC1} on pin 3 can be left an open circuit as well.
(4) An HCPL device pin 7 must be left floating (open) or grounded when an ISO722 or ISO722M device is to be used as a drop-in replacement. If pin 7 of the ISO722 or ISO722M device is placed in a high logic state, the output of the device is disabled.
(5) Pin 3 of the IL710 must not be tied to ground on the circuit board because this shorts the ISO72x V_{CC1} to ground. The IL710 pin 3 can only be tied to V_{CC} or left open to drop in an ISO72x device.

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10.2.3 Application Curves

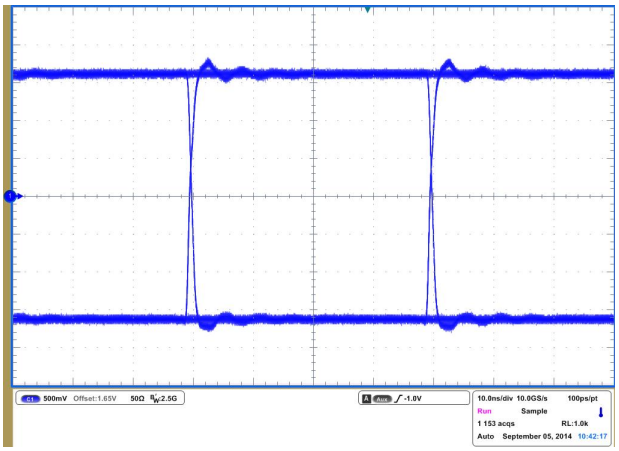

Figure 21. ISO721M Eye Diagram at 25 Mbps, 3.3 V and 25°C

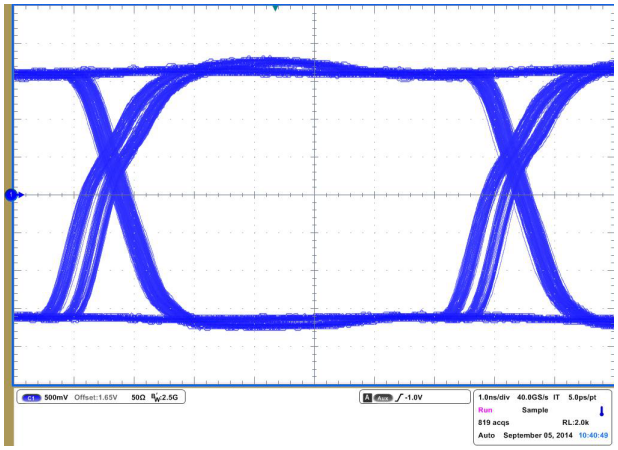

Figure 22. ISO721M Eye Diagram at 150 Mbps, 3.3 V and 25°C

11 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, a 0.1-µF bypass capacitor should be placed at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments SN6501 data sheet. For such applications, detailed power supply design and transformer selection recommendations are available in the data sheet, SN6501 *Transformer Driver for Isolated Power Supplies* (SLLSEA0).

12 Layout

12.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design as shown in Figure 23. Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane, and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power/ground plane system to the stack to keep it symmetrical. Adding a second plane system makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly. For detailed layout recommendations, see the Application Note *Digital Isolator Design Guide* (SLLA284).

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Layout Guidelines (continued)

12.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 epoxy-glass as PCB material. FR-4 (Flame Retardant 4) meets the requirements of Underwriters Laboratories UL94-V0, and is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and its self-extinguishing flammability-characteristics.

12.2 Layout Example

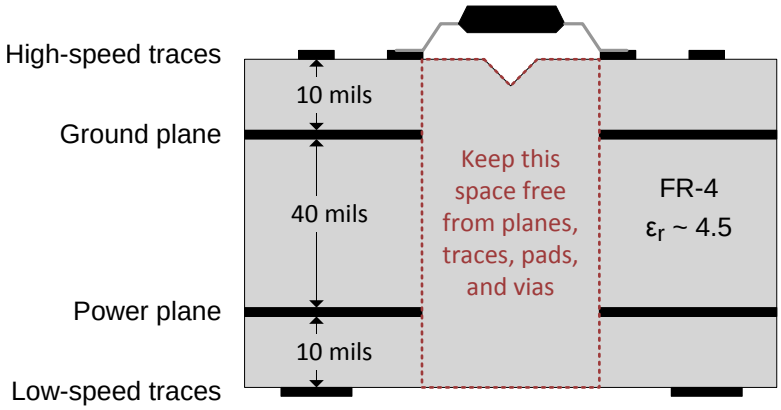

Figure 23. Recommended Layer Stack

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13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

Transformer Driver for Isolated Power Supplies, SLLSEA0.

Digital Isolator Design Guide, SLLA284.

Isolation Glossary, SLLA353

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO721	Click here	Click here	Click here	Click here	Click here
ISO721M	Click here	Click here	Click here	Click here	Click here
ISO722	Click here	Click here	Click here	Click here	Click here
ISO722M	Click here	Click here	Click here	Click here	Click here

13.3 Trademarks

SDS is a trademark of Honeywell.
DeviceNet is a trademark of Open Devicenet Vendors Association, Inc.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO721D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ISO721	Samples
ISO721DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ISO721	Samples
ISO721DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ISO721	Samples
ISO721DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ISO721	Samples
ISO721MD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IS721M	Samples
ISO721MDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IS721M	Samples
ISO721MDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IS721M	Samples
ISO722D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ISO722	Samples
ISO722DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ISO722	Samples
ISO722DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ISO722	Samples
ISO722MD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IS722M	Samples
ISO722MDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IS722M	Samples
ISO722MDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IS722M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF ISO721, ISO721M, ISO722 :

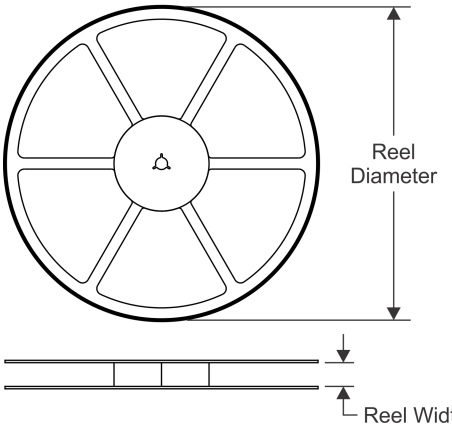
- Automotive : ISO721-Q1, ISO721-Q1, ISO722-Q1
- Enhanced Product : ISO721M-EP
- Military : ISO721M

NOTE: Qualified Version Definitions:

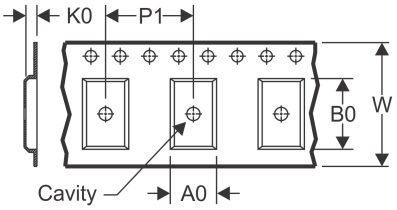
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

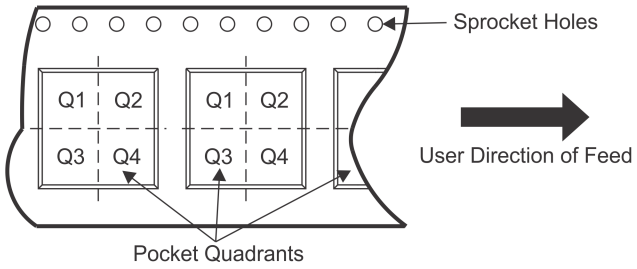


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

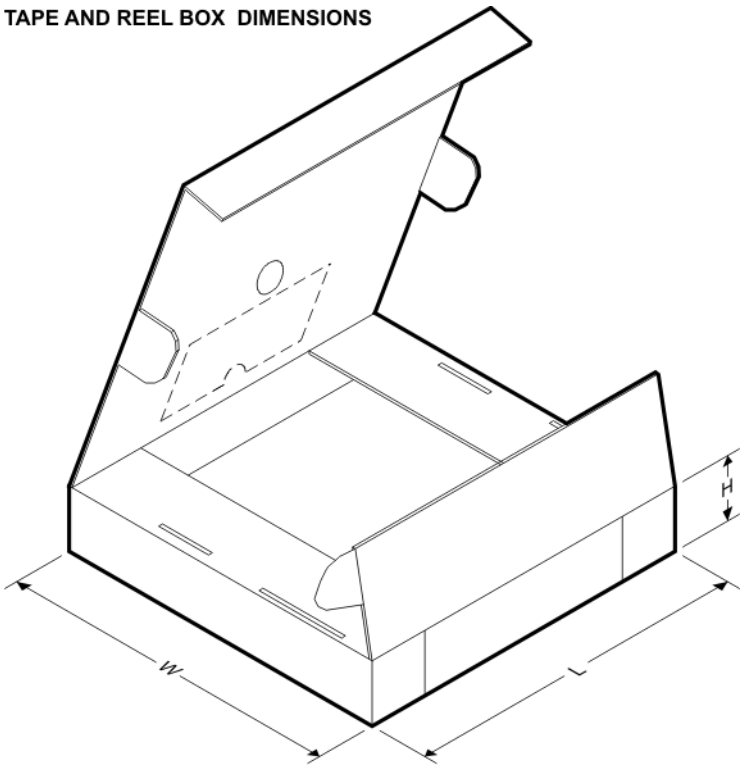
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO721DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO721MDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO722DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO722MDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

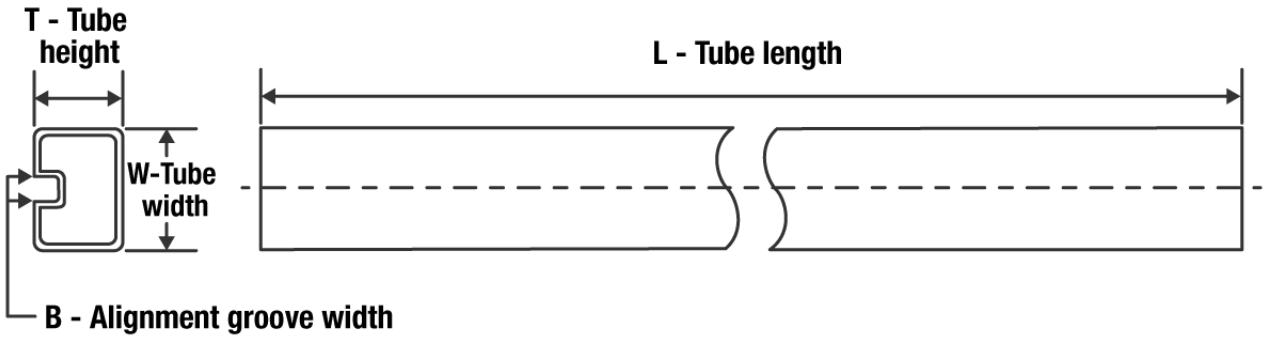
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

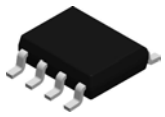
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO721DR	SOIC	D	8	2500	350.0	350.0	43.0
ISO721MDR	SOIC	D	8	2500	350.0	350.0	43.0
ISO722DR	SOIC	D	8	2500	350.0	350.0	43.0
ISO722MDR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO721D	D	SOIC	8	75	505.46	6.76	3810	4
ISO721DG4	D	SOIC	8	75	505.46	6.76	3810	4
ISO721MD	D	SOIC	8	75	505.46	6.76	3810	4
ISO721MDG4	D	SOIC	8	75	505.46	6.76	3810	4
ISO722D	D	SOIC	8	75	505.46	6.76	3810	4
ISO722MD	D	SOIC	8	75	505.46	6.76	3810	4

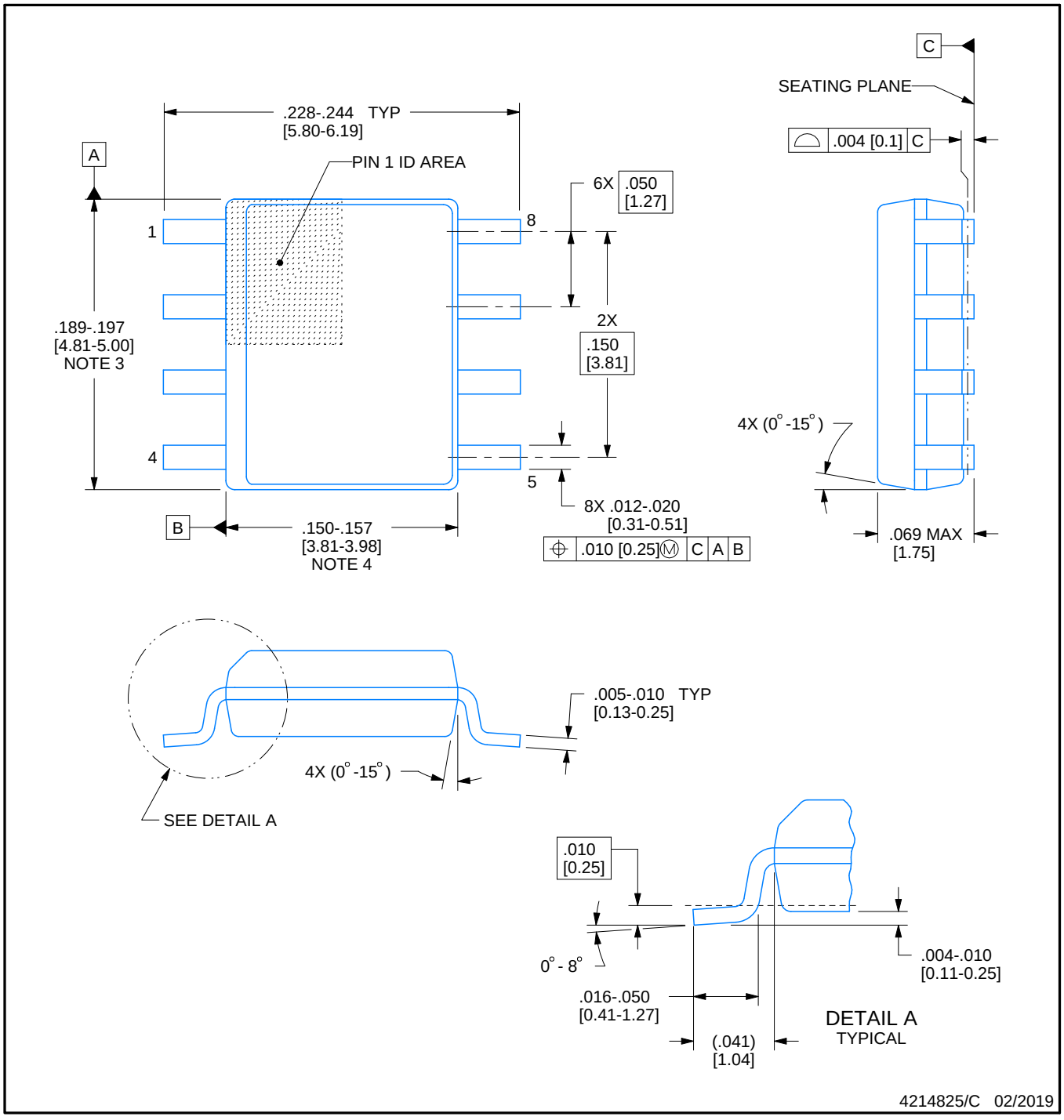


PACKAGE OUTLINE

D0008A

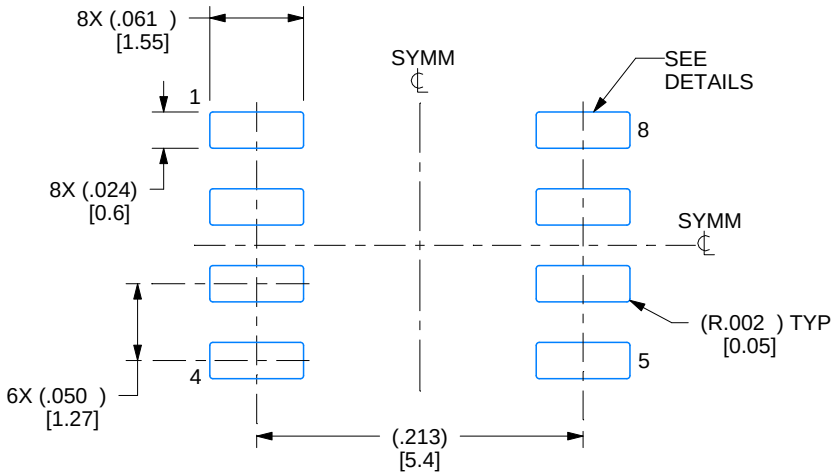
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

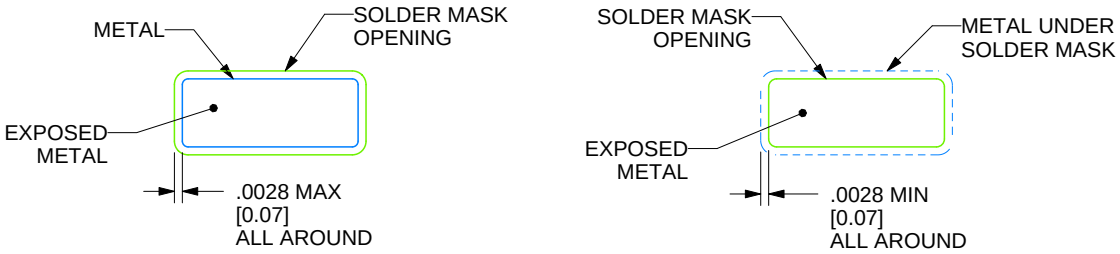


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

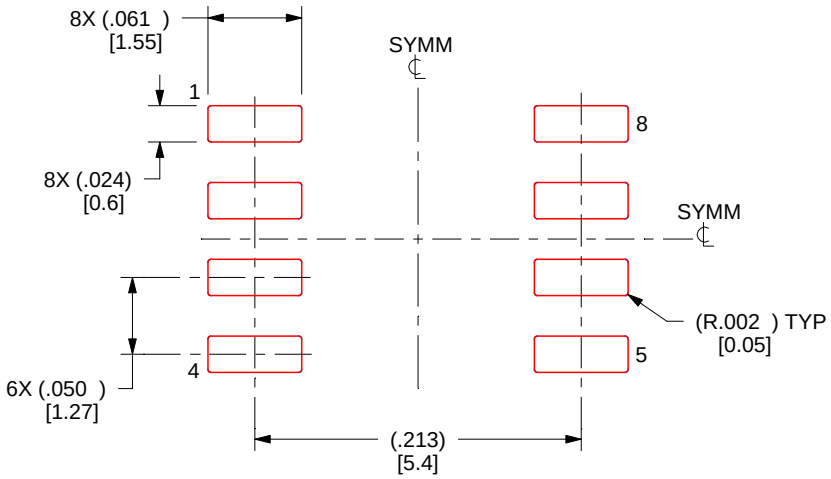
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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