ISO722x 双通道数字隔离器

1 特性

- 1、5、25 和 150Mbps 信号传输速率选项
  - 低通道到通道输出偏斜；最大值为 1ns
  - 低脉宽失真度 (PWD)；最大值为 1ns
  - 低抖动；在速率为 150Mbps 时的典型值为 1ns
- 50kV/μs 典型瞬态抗扰度
- 使用 2.8V（C 级）、3.3V 或 5V 电源工作
- 4kV 静电放电 (ESD) 保护
- 高电磁抗扰度
- 工作温度范围 –40°C 至 +125°C
- 额定电压下正常使用寿命为 28 年（请参阅 *ISO72x 系列数字隔离器高压使用寿命*和隔离电容寿命图）
- 安全相关认证
  - 符合 DIN VDE V 0884-11:2017-01 和 DIN EN 61010-1 (VDE 0411-1) 标准的 4000 V_{PK} V_{IOTM}、560 V_{PK} V_{IORM} VDE 基本绝缘
  - 符合 UL 1577 标准的 2500 V_{RMS} 隔离
  - CSA 批准的 IEC 60950-1 和 IEC 62368-1

2 应用

- 工业现场总线
  - Modbus
  - Profibus™
  - DeviceNet™数据总线
- 计算机外设接口
- 伺服器控制接口
- 数据采集

3 说明

ISO7220x 和 ISO7221x 系列器件是双通道数字隔离器。为了方便 PCB 布局，各通道在 ISO7220x 中方向相同，在 ISO7221x 中方向相反。这些器件具有逻辑输入和输出缓冲器，二者由 TI 的二氧化硅 (SiO_2) 绝缘栅相隔离，提供4000 V_{PK}。当与隔离电源配合使用时，这些器件可阻止高电压和隔离接地，并可防止数据总线或其他电路上的噪声电流进入本地接地或对敏感电路造成干扰或损坏。

对二进制输入信号进行调理并转换为平衡的信号，然后由电容式隔离层进行差分。跨越该隔离层，差分比较器可接收逻辑转换信息，然后相应地设置或重置触发器和输出电路。电路将跨越隔离层发送定期更新脉冲，以确保直流电平输出正常。如果每 4μs 没有收到此直流更新脉冲，则会假定输入未通电，或者未主动驱动，故障保护电路会将输出驱动至逻辑高电平状态。

低容值电容和生成的时间常数提供高速运行，其信号传输速率范围为 0Mbps（直流）到 150Mbps（线路上的信号传输速率是每秒进行的电压转换次数，以单位 bps 来表示）。A 选项、B 选项和 C 选项器件具有 TTL 输入阈值，并且在输入上具有噪声滤波器，可防止将瞬态脉冲传递到器件的输出。M 选项器件具有 CMOS $V_{CC}/2$ 输入阈值，没有输入噪声滤波器以及额外的传播延迟。

ISO7220x 和 ISO7221x 系列器件需要两个 2.8V（C 级）、3.3V、5V 电源或这些电源的任意组合。通过 2.8V 或 3.3V 电源供电时，所有输入均可耐受 5V 电压，所有输出均为 4mA CMOS。

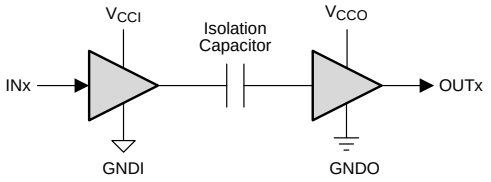
ISO7220x 和 ISO7221x 系列器件在 –40°C 至 +125°C 的环境温度范围内运行。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ISO7220x	SOIC (8)	4.90mm × 3.91mm
ISO7221x		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



V_{CCI} 和 GNDI 分别是输入通道的电源和接地连接引脚。

V_{CCO} 和 GNDO 分别是输出通道的电源和接地连接引脚。

目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision O (April 2017) to Revision P **Page**

- 已更改 *通篇将"(VDE V 0884-10):2006-12"更改为"DIN VDE V 0884-11:2017-01"* ... 1
- 已更改 通篇将*"CSA 批准的组件验收通知 5A 和 IEC 60950-1"更改为"CSA 批准的 IEC 60950-1 和 IEC 62368-1"* ... 1
- Added the basic insulation working voltage for CSA in the *Safety-Related Certifications* table ... 9
- Changed the VDE certification number from 40016131 to 40047657 in the *Safety-Related Certifications* table ... 9
- Changed the maximum propagation delay and pulse-width distortion in each *Switching Characteristics* table ... 14
- Added ± 10% for the V_{CC1} and V_{CC2} voltages in the condition statement of the *Switching Characteristics—5-V V_{CC1} and V_{CC2} Supplies* table ... 14
- Changed ISO722x to ISO7220 for all part numbers for the Channel-to-channel output skew parameter in each *Switching Characteristic* table ... 14

Changes from Revision N (September 2015) to Revision O **Page**

- Changed the *Dissipation Characteristics* table to *Power Ratings*. Combined the *DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 Insulation Characteristics* table *IEC Package Characteristics*, and *IEC 60664-1 Ratings Table* in the *Insulation Specifications* table. Changed the *Regulatory Information* table to *Safety-Related Certifications* ... 7
- Deleted the maximum surge voltage, 4000 V_{PK} for VDE in the *Safety-Related Certifications* table ... 9
- Changed the CSA information in the *Safety-Related Certifications* table ... 9

- 已添加 *接收文档更新通知* 部分 28
- 已更改 *静电放电注意事项* 部分 28

Changes from Revision M (October 2014) to Revision N **Page**

- 已更改 通篇将 VDE 认证从“DIN EN 60747-5-5 (VDE 0884-5)”更改为“DIN V VDE V 0884-10 (VDE V 0884-10):2006-12”.. 1
- 将*简化原理图*更新为较高质量版本。 1
- Changed the max value of the IN and OUT voltage from 6 to V_{CC} + 0.5 in the *Absolute Maximum Ratings* table. 6
- Changed L(I01) MIN value from 4.8 to 4 in the *IEC Package Characteristics* table. 8
- Added the JEDEC package dimensions note in the *IEC Package Characteristics* table 8
- Changed L(I01) MIN value from 4.8 to 4 in the *IEC Package Characteristics* table. 8
- Added the DTI parameter to the *IEC Package Characteristics* table. 8
- Changed the DTI test condition From: IEC 60112 / VDE 0303 Part 1 To: DIN EN 60112 (VDE 0303-11); IEC 60112 8
- Added = 150°C to insulation resistance test condition in the *DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 Insulation Characteristics* table. 8
- Added table row with input side V_{CC} = X to the *ISO7220x or ISO7221x Function* table. 24

Changes from Revision L (January 2012) to Revision M **Page**

- 已更改 将此数据表的标题更改为 *ISO722x 双通道数字隔离器* 1
- 已添加 *引脚配置和功能* 部分、*处理额定值* 表、*功耗额定值* 表、*特性* *说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分，将*热性能信息* 表 1
- 更新了 特性 部分 1
- 已添加 在“说明”部分的第二句中添加了符合 VDE 标准的 4000 V_{PK} 电压 符合 VDE 标准的 1
- Updated the *Regulatory Information* Table 6
- Added the min and max values to the Storage temperature parameter in the *Absolute Maximum Ratings* table. 6
- Changed in ROC table Max col, V_{IH} row from VCC to 5.5 7
- Changed the L(I01) parameter name to external clearance (CLR) and L(I02) to external creepage (CPG). Also changed the input-to-output test voltage (V_{PR}) parameter name to apparent charge (q_{pd}) 8
- Changed the Device Options table, Input Threshold column from ≠ symbol to ~ symbol 6 places 24
- 已更改 *隔离相关术语* 28

Changes from Revision K (January 2010) to Revision L **Page**

- 将特性从“使用 3.3V 或 5V 电源工作”更改为“使用 2.8V（C 级）、3.3V 或 5V 电源工作” 1
- 将特性从“4000 V_{peak} 绝缘，560 V_{peak} V_{IORM}”更改为“4000 V_{PK} V_{IOTM}，560 V_{PK} V_{IORM}，符合 IEC 60747-5-2 (VDE 0884, Rev2)” 1
- Added device options to V_{CC} in the RECOMMENDED OPERATING CONDITIONS table 7
- Changed Note: (1) in the RECOMMENDED OPERATING CONDITIONS table 7
- Changed the CTI MIN value From: ≥175 V To: ≥400 V 8
- Updated the *Regulatory Information* table 9
- Changed I_{CC1} and I_{CC2} test conditions in the 5-V table 10
- Changed Table Note: (1) 10
- Changed I_{CC1} and I_{CC2} test conditions in the V_{CC1} at 5 V, V_{CC2} at 3.3 V table 11
- Changed Table Note: (1) 11
- Changed I_{CC1} and I_{CC2} test conditions in the V_{CC1} at 3.3 V, V_{CC2} at 5 V table 12
- Changed Table Note (1) 12
- Changed I_{CC1} and I_{CC2} test conditions in the V_{CC1} and V_{CC2} at 3.3 V table 13
- Changed Table Note (1) 13

- Added ELECTRICAL and Switching CHARACTERISTICS table for V_{CC1} and V_{CC2} at 2.8 V (ISO722xC-Only) 13
- Changed *V_{CC} Undervoltage Threshold vs Free-Air Temperature* 19
- Changed *Failsafe Delay Time Test Circuit and Voltage Waveforms* 21

Changes from Revision J (May 2009) to Revision K **Page**

- Changed the RECOMMENDED OPERATING CONDITIONS so that Note (2) is associated with all device options in the Input pulse width and Signaling rate 7
- Changed Note (2) From: Typical signaling rate under ideal conditions at 25°C. To: Typical signaling rate and Input pulse width are measured at ideal conditions at 25°C. 7
- Changed column 2 of the AVAILABLE OPTIONS table From: Signaling Rate To: Max Signaling Rate 24

Changes from Revision I (December 2008) to Revision J **Page**

- Changed ISO7221C Marked As column From: TI7221C To: I7221C in the AVAILABLE OPTIONS table 24

Changes from Revision H (May 2008) to Revision I **Page**

- 已添加 将“IEC 61010-1、IEC 60950-1 和 CSA 批准”添加到了 UL 1577 特性 要点 1

Changes from Revision G (March 2008) to Revision H **Page**

- Added Note: (1) to the RECOMMENDED OPERATING CONDITIONS table 7
- Added Note: (1) to the ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V table 10
- Added Note: (1) to the ELECTRICAL CHARACTERISTICS: V_{CC1} at 5 V, V_{CC2} at 3.3 V table 11
- Added Note (1): to the ELECTRICAL CHARACTERISTICS: V_{CC1} at 3.3 V, V_{CC2} at 5 V table 12
- Added Note (1): to the ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3 V 13

Changes from Revision F (August 2007) to Revision G **Page**

- 已添加 在数据表中添加了器件型号 ISO7220B 和 ISO7221B 1
- 已添加 5Mbps 信号传输速率更改为 特性 列表 1
- Added Part Numbers ISO7220B and ISO7221B to the ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V table . 10
- Added Part Numbers ISO7220B and ISO7221B to the ELECTRICAL CHARACTERISTICS: V_{CC1} at 5 V, V_{CC2} at 3.3 V table 11
- Added Part Numbers ISO7220B and ISO7221B to the ELECTRICAL CHARACTERISTICS: V_{CC1} at 3.3 V, V_{CC2} at 5 V table 12
- Added Part Numbers ISO7220B and ISO7221B to the ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3 V 13
- Added PROPAGATION DELAY vs FREE-AIR TEMPERATURE, ISO722xB, *Propagation Delay vs Free-Air Temperature, ISO722xB* 19
- Added Part Numbers ISO7220B and ISO7221B to the AVAILABLE OPTIONS table 24

Changes from Revision E (July 2007) to Revision F **Page**

- Added $t_{sk(pp)}$ footnote to the SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V OPERATION table 14
- Added $t_{sk(o)}$ footnote to the SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V OPERATION table 14
- Added $t_{sk(pp)}$ footnote to the SWITCHING CHARACTERISTICS: V_{CC1} at 5 V, V_{CC2} at 3.3 V OPERATION table 15
- Added $t_{sk(o)}$ footnote to the SWITCHING CHARACTERISTICS: V_{CC1} at 5 V, V_{CC2} at 3.3 V OPERATION table 15
- Added $t_{sk(pp)}$ footnote to the SWITCHING CHARACTERISTICS: V_{CC1} at 3.3 V, V_{CC2} at 5 V OPERATION table 16
- Added $t_{sk(o)}$ footnote to the SWITCHING CHARACTERISTICS: V_{CC1} at 3.3 V, V_{CC2} at 5 V OPERATION table 16

- Added $t_{sk(pp)}$ footnote to the SWITCHING CHARACTERISTICS table ... 17
- Changed *3.3-V_{RMS} Supply Current vs Signaling Rate* - Re-scaled the Y-axis ... 19
- Changed *5-V_{RMS} Supply Current vs Signaling Rate* - New Curves ... 19

Changes from Revision D (June 2007) to Revision E **Page**

- Changed *3.3-V_{RMS} Supply Current vs Signaling Rate* - New Curves ... 19
- Changed *5-V_{RMS} Supply Current vs Signaling Rate* - Re-scaled the Y-axis ... 19

Changes from Revision C (May 2007) to Revision D **Page**

- Changed *Typical ISO7220x Circuit Hook-Up* - Pin 2 (INA) label From: OUTPUT to INPUT ... 26

Changes from Revision B (May 2007) to Revision C **Page**

- Added the Signaling rate values to the RECOMMENDED OPERATING CONDITIONS table ... 7
- Changed the IEC 60664-1 RATINGS TABLE - Specification I-III test conditions From: Rated mains voltage ≤150 VRMS To: Rated mains voltage ≤300 VRMS. Added a row for the I-II specifications ... 8
- Added *ISO722xM Jitter vs Signaling Rate* cross reference to the Peak-to-peak eye-pattern jitter of the SWITCHING CHARACTERISTICS table ... 14
- Added *Time-Dependent Dielectric Breakdown Test Results* ... 26

Changes from Revision A (August 2006) to Revision B **Page**

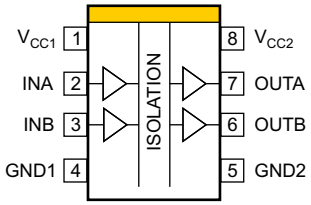
- Added the TYPICAL CHARACTERISTIC CURVES to the data sheet. ... 19
- Added the PARAMETER MEASUREMENT INFORMATION to the data sheet ... 21
- Added the APPLICATION INFORMATION section to the data sheet ... 25
- 已添加 在数据表中添加了“隔离相关术语”部分 ... 28

Changes from Original (July 2006) to Revision A **Page**

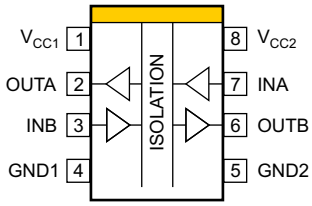
- 已删除 从 UL 1577 特性 要点中删除了“CSA 批准” ... 1
- Added option A to the AVAILABLE OPTIONS table ... 24

5 Pin Configuration and Functions

ISO7220x D Package
8-Pin SOIC
Top View



ISO7221x D Package
8-Pin SOIC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	ISO7220x	ISO7221x		
INA	2	7	I	Input, channel A
INB	3	3	I	Input, channel B
GND1	4	4	—	Ground connection for V_{CC1}
GND2	5	5	—	Ground connection for V_{CC2}
OUTA	7	2	O	Output, channel A
OUTB	6	6	O	Output, channel B
V_{CC1}	1	1	—	Power supply, V_{CC1}
V_{CC2}	8	8	—	Power supply, V_{CC2}

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}	–0.5	6	V
V_I	Voltage at IN, OUT	–0.5	V_{CC} + 0.5(3)	V
I_O	Output current	–15	15	mA
T_J	Maximum junction temperature		170	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under A*bsolute Maximum Ratings* can cause permanent damage to the device. These ratings are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to network ground pin and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	V
		Machine Model, ANSI/ESDS5.2-1996	±200	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage(1), V_{CC1}, V_{CC2}	ISO722xA, ISO722xB, ISO722xM	3		5.5	V
		ISO722xC	2.8		5.5	
I_{OH}	High-level output current		–4			mA
I_{OL}	Low-level output current				4	mA
t_{ui}	Input pulse width(2)	ISO722xA	1	0.67		µs
		ISO722xB	200	100		ns
		ISO722xC	40	33		
		ISO722xM	6.67	5		
$1/t_{ui}$	Signaling rate(2)	ISO722xA	0	1500	1000	kbps
		ISO722xB	0	10	5	Mbps
		ISO722xC	0	30	25	
		ISO722xM	0	200	150	
V_{IH}	High-level input voltage	ISO722xA, ISO722xB, ISO722xC	2		5.5	V
V_{IL}	Low-level input voltage	ISO722xA, ISO722xB, ISO722xC	0		0.8	V
V_{IH}	High-level input voltage	ISO722xM	0.7 V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage	ISO722xM	0		0.3 V_{CC}	V
T_J	Junction temperature		–40		150	°C
H	External magnetic field-strength immunity per IEC 61000-4-8 and IEC 61000-4-9 certification				1000	A/m

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.
For the 2.8-V operation, V_{CC1} or V_{CC2} is specified at 2.8 V.
(2) Typical signaling rate and Input pulse width are measured at ideal conditions at 25°C.

6.4 Thermal Information

THERMAL METRIC(1)			ISO7220x ISO7221x	UNIT
			D (SOIC)	
			8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Low-K Thermal Resistance(2)	212	°C/W
		High-K Thermal Resistance	122	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		69.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		47.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter		15.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter		47.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

6.5 Power Ratings

$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L = 15$ pF, Input a 150 Mbps 50% duty cycle square wave

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Device power dissipation, ISO722xM				390	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	4	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	0.008	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	400	V
	Material group		II	
	Overvoltage category	Rated mains voltage ≤150 V_{RMS}	I-IV	
		Rated mains voltage ≤300 V_{RMS}	I-III	
		Rated mains voltage ≤400 V_{RMS}	I-II	
DIN VDE V 0884-11:2017-01(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	560	V_{PK}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$ t = 60 s (qualification), t = 1 s (100% production)	4000	V_{PK}
q_{pd}	Apparent charge(3)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.3 \times V_{IORM}$, t_m = 10 s	≤5	
		Method b1: At routine test (100% production) and preconditioning (type test) $V_{ini} = V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1 s	≤5	
C_{IO}	Barrier capacitance, input to output(4)	V_{IO} = 0.4 sin (4E6πt)	1	pF
R_{IO}	Isolation resistance, input to output(4)	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ = 2500 V_{RMS}, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$ = 3000 V_{RMS}, t = 1 s (100% production)	2500	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *basic electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier tied together creating a two-terminal device

6.7 Safety-Related Certifications

VDE	CSA	UL
Certified according to DIN VDE V 0884-11:2017-01 and DIN EN 61010-1 (VDE 0411-1):2011-07	Certified according to IEC 60950-1 and IEC 62368-1	Recognized under UL 1577 Component Recognition Program
Basic Insulation Maximum Transient Overvoltage, 4000 V_{PK}; Maximum Repetitive Peak Isolation Voltage, 560 V_{PK}	2000 V_{RMS} Isolation rating 400 V_{RMS} Basic insulation and 148 V_{RMS} Reinforced insulation working voltage per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed. +A1+A2. 300 V_{RMS} Basic insulation working voltage per CSA 62369-1-14 and IEC 62368-1:2014 Ed. 2.	Single protection, 2500 V_{RMS}
Certificate number: 40047657	Master contract number: 220991	File number: E181974

6.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 212°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C, see Figure 1			124	mA
		$R_{\theta JA}$ = 212°C/W, V_I = 3.6 V, T_J = 170°C, T_A = 25°C, see Figure 1			190	
T_S	Safety temperature				150	°C

(1) The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

6.9 Electrical Characteristics—5-V V_{CC1} and V_{CC2} Supplies

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	ISO7220x quiescent, V_I = V_{CC} or 0 V, no load		1	2	mA
		ISO7221 quiescent, V_I = V_{CC} or 0 V, no load		8.5	17	
		ISO7220A and ISO7220B 1 Mbps, 0.5-MHz input clock signal, no load		2	3	mA
		ISO7221A, ISO7221B 1 Mbps, 0.5-MHz input clock signal, no load		10	18	
		ISO7220C, ISO7220M 25 Mbps, 12.5-MHz input clock signal, no load		4	9	mA
		ISO7221C and ISO7221M 25 Mbps, 12.5-MHz input clock signal, no load		12	22	
I_{CC2}	V_{CC2} supply current	ISO7220x quiescent, V_I = V_{CC} or 0 V, no load		16	31	mA
		ISO7221x quiescent, V_I = V_{CC} or 0 V, no load		8.5	17	
		ISO7220A and ISO7220B 1 Mbps, 0.5-MHz input clock signal, no load		17	32	mA
		ISO7221A, ISO7221B 1 Mbps, 0.5-MHz input clock signal, no load		10	18	
		ISO7220C, ISO7220M 25 Mbps, 12.5-MHz input clock signal, no load		20	34	mA
		ISO7221C and ISO7221M 25 Mbps, 12.5-MHz input clock signal, no load		12	22	
V_{OH}	High-level output voltage	I_{OH} = –4 mA, See Figure 14	V_{CC} – 0.8	4.6		V
		I_{OH} = –20 μA, See Figure 14	V_{CC} – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 14		0.2	0.4	V
		I_{OL} = 20 μA, See Figure 14		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis			150		mV
I_{IH}	High-level input current	IN from 0 V to V_{CC}			10	μA
I_{IL}	Low-level input current	IN from 0 V to V_{CC}	–10			μA
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See Figure 16	25	50		kV/μs

6.10 Electrical Characteristics—5-V V_{CC1} and 3.3-V V_{CC2} Supply

V_{CC1} at 5 V ± 10%, V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	ISO7220x quiescent, V_I = V_{CC} or 0 V, no load		1	2	mA
		ISO7221x quiescent, V_I = V_{CC} or 0 V, no load		8.5	17	
		ISO7220A and ISO7220B 1 Mbps, 0.5-MHz input clock signal, no load		2	3	mA
		ISO7221A and ISO7221B 1 Mbps, 0.5-MHz input clock signal, no load		10	18	
		ISO7220C and ISO7220M 25 Mbps, 12.5-MHz input clock signal, no load		4	9	mA
		ISO7221C and ISO7221M 25 Mbps, 12.5-MHz input clock signal, no load		12	22	
I_{CC2}	V_{CC2} supply current	ISO7220x quiescent, V_I = V_{CC} or 0 V, no load		8	18	mA
		ISO7221x quiescent, V_I = V_{CC} or 0 V, no load		4.3	9.5	
		ISO7220A and ISO7220B 1 Mbps, 0.5-MHz input clock signal, no load		9	19	mA
		ISO7221A and ISO7221B 1 Mbps, 0.5-MHz input clock signal, no load		5	11	
		ISO7220C and ISO7220M 25 Mbps, 12.5-MHz input clock signal, no load		10	20	mA
		ISO7221C and ISO7221M 25 Mbps, 12.5-MHz input clock signal, no load		6	12	
V_{OH}	High-level output voltage	ISO7220x, ISO7221x (3.3-V side), I_{OH} = –4 mA, See Figure 14	V_{CC} – 0.4			V
		ISO7221x (5-V side), I_{OH} = –4 mA, See Figure 14	V_{CC} – 0.8			
		All devices, I_{OH} = –20 μA, See Figure 14	V_{CC} – 0.1			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 14			0.4	V
		I_{OL} = 20 μA, See Figure 14			0.1	
$V_{I(HYS)}$	Input voltage hysteresis			150		mV
I_{IH}	High-level input current	IN from 0 V to V_{CC}			10	μA
I_{IL}	Low-level input current	IN from 0 V to V_{CC}	–10			μA
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See Figure 16	15	40		kV/μs

6.11 Electrical Characteristics—3.3-V V_{CC1} and 5-V V_{CC2} Supply

V_{CC1} at 3.3 V ± 10%, V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	ISO7220x quiescent, V_I = V_{CC} or 0 V, no load		0.6	1	mA
		ISO7221x quiescent, V_I = V_{CC} or 0 V, no load		4.3	9.5	
		ISO7220A and ISO7220B 1 Mbps, 0.5-MHz input clock signal, no load		1	2	mA
		ISO7221A and ISO7221B 1 Mbps, 0.5-MHz input clock signal, no load		5	11	
		ISO7220C and ISO7220M 25 Mbps, 12.5-MHz input clock signal, no load		2	4	mA
		ISO7221C and ISO7221M 25 Mbps, 12.5-MHz input clock signal, no load		6	12	
I_{CC2}	V_{CC2} supply current	ISO7220x quiescent, V_I = V_{CC} or 0 V, no load		16	31	mA
		ISO7221x quiescent, V_I = V_{CC} or 0 V, no load		8.5	17	
		ISO7220A and ISO7220B 1 Mbps, 0.5-MHz input clock signal, no load		18	32	mA
		ISO7221A and ISO7221B 1 Mbps, 0.5-MHz input clock signal, no load		10	18	
		ISO7220C and ISO7220M 25 Mbps, 12.5-MHz input clock signal, no load		20	34	mA
		ISO7221C and ISO7221M 25 Mbps, 12.5-MHz input clock signal, no load		12	22	
V_{OH}	High-level output voltage	ISO7220x and ISO7221x (5-V side), I_{OH} = –4 mA, See Figure 14	V_{CC} – 0.8			V
		ISO7221x (3.3-V side), I_{OH} = –4 mA, See Figure 14	V_{CC} – 0.4			
		All devices, I_{OH} = –20 μA, See Figure 14	V_{CC} – 0.1			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 14			0.4	
		I_{OL} = 20 μA, See Figure 14		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			150		mV
I_{IH}	High-level input current	IN from 0 V or V_{CC}			10	μA
I_{IL}	Low-level input current	IN from 0 V or V_{CC}	–10			μA
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See Figure 16	15	40		kV/μs

6.12 Electrical Characteristics—3.3-V V_{CC1} and V_{CC2} Supplies

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted.)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC2} supply current	ISO7220x quiescent, V_I = V_{CC} or 0 V, no load		0.6	1	mA
		ISO7221x quiescent, V_I = V_{CC} or 0 V, no load		4.3	9.5	
		ISO7220A and ISO7220B 1 Mbps, 0.5-MHz input clock signal, no load		1	2	mA
		ISO7221A and ISO7221B 1 Mbps, 0.5-MHz input clock signal, no load		5	11	
		ISO7220C and ISO7220M 25 Mbps, 12.5-MHz input clock signal, no load		2	4	mA
		ISO7221C and ISO7221M 25 Mbps, 12.5-MHz input clock signal, no load		6	12	
I_{CC2}	V_{CC2} supply current	ISO7220x quiescent, V_I = V_{CC} or 0 V, no load		8	18	mA
		ISO7221x quiescent, V_I = V_{CC} or 0 V, no load		4.3	9.5	
		ISO7220A and ISO7220B 1 Mbps, 0.5-MHz input clock signal, no load		9	19	mA
		ISO7221A and ISO7221B 1 Mbps, 0.5-MHz input clock signal, no load		5	11	
		ISO7220C and ISO7220M 25 Mbps, 12.5-MHz input clock signal, no load		10	20	mA
		ISO7221C and ISO7221M 25 Mbps, 12.5-MHz input clock signal, no load		6	12	
V_{OH}	High-level output voltage	I_{OH} = –4 mA, See Figure 14	V_{CC} – 0.4	3		V
		I_{OH} = –20 μA, See Figure 14	V_{CC} – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 14		0.2	0.4	
		I_{OL} = 20 μA, See Figure 14		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis			150		mV
I_{IH}	High-level input current	IN from 0 V or V_{CC}			10	μA
I_{IL}	Low-level input current	IN from 0 V or V_{CC}	–10			μA
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See Figure 16	15	40		kV/μs

(1) For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

6.13 Electrical Characteristics—2.8-V V_{CC1} and V_{CC2} Supplies

V_{CC1} and V_{CC2} at 2.8 V (over recommended operating conditions unless otherwise noted.) 2.8-V operation is only specified for ISO722xC with production screening starting in January 2012. The first two digits of the Lot Trace Code (YMSLLLLG4) written on top of each device can be used to identify year and month of production respectively.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	ISO7220C quiescent, V_I = V_{CC} or 0 V, no load		0.4	0.9	mA
		ISO7221C quiescent, V_I = V_{CC} or 0 V, no load		3.7	7.5	
		ISO7220C 25 Mbps, 12.5-MHz input clock signal, no load		1.5	3.5	mA
		ISO7221C 25 Mbps, 12.5-MHz input clock signal, no load		4.5	10	
I_{CC2}	V_{CC2} supply current	ISO7220C quiescent, V_I = V_{CC} or 0 V, no load		6.8	15	mA
		ISO7221C quiescent, V_I = V_{CC} or 0 V, no load		3.7	7.5	
		ISO7220C 25 Mbps, 12.5-MHz input clock signal, no load		9	17	mA
		ISO7221C 25 Mbps, 12.5-MHz input clock signal, no load		4.5	10	
V_{OH}	High-level output voltage	I_{OH} = –4 mA, See Figure 14	V_{CC} – 0.6	2.55		V
		I_{OH} = –20 μA, See Figure 14	V_{CC} – 0.1	2.8		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 14		0.25	0.6	
		I_{OL} = 20 μA, See Figure 14		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis			150		mV
I_{IH}	High-level input current	IN from 0 V or V_{CC}			10	μA
I_{IL}	Low-level input current	IN from 0 V or V_{CC}	–10			μA
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See Figure 16	10	30		kV/μs

6.14 Switching Characteristics—5-V V_{CC1} and V_{CC2} Supplies

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO722xA, see Figure 14	280	405	600	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			1	18	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xB, see Figure 14	42	55	70	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			1	3	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xC, see Figure 14	22	32	42	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			1	2	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xM, see Figure 14	6	10	16	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			0.5	1	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xA			180	ns
		ISO722xB			17	
		ISO722xC			10	
		ISO722xM			3	
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO7220A		3	15	ns
		ISO7220B		0.6	3	
		ISO7220C, ISO7220M		0.2	1	
t_r	Output signal rise time	See Figure 14		1		ns
t_f	Output signal fall time			1		ns
t_{fs}	Failsafe output delay time from input power loss	See Figure 15		3		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO722xM, 150 Mbps PRBS NRZ data, 5-bit max same polarity input, both channels, See Figure 17, Figure 13		1		ns
		ISO722xM, 150 Mbps unrestricted bit run length data input, both channels, See Figure 17		2		

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified pins of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

6.15 Switching Characteristics—5-V V_{CC1} and 3.3-V V_{CC2} Supply

V_{CC1} at 5 V ± 10%, V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO722xA, see Figure 14	285	410	585	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			1	18	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xB, see Figure 14	45	58	75	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			1	3	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xC, see Figure 14	25	36	48	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			1	2	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xM, see Figure 14	7	12	20	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			0.5	1	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xA			180	ns
		ISO722xB			17	
		ISO722xC			10	
		ISO722xM			5	
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO7220A		3	15	ns
		ISO7220B		0.6	3	
		ISO7220C, ISO7220M		0.2	1	
t_r	Output signal rise time	See Figure 14		2		ns
t_f	Output signal fall time			2		ns
t_{fs}	Failsafe output delay time from input power loss	See Figure 15		3		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO722xM, 150 Mbps PRBS NRZ data, 5-bit max same polarity input, both channels, See Figure 17, Figure 13		1		ns
		ISO722xM, 150 Mbps unrestricted bit run length data input, both channels, See Figure 17		2		

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified pins of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

6.16 Switching Characteristics—3.3-V $_{CC1}$ and 5-V V_{CC2} Supplies

V_{CC1} at 3.3 V ± 10%, V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO722xA, see Figure 14	285	395	605	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			1	22	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xB, see Figure 14	45	58	75	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			1	4	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xC, see Figure 14	25	36	48	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			1	3	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xM, see Figure 14	7	12	21	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			0.5	1	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xA			190	ns
		ISO722xB			17	
		ISO722xC			10	
		ISO722xM			5	
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO7220A		3	15	ns
		ISO7220B		0.6	3	
		ISO7220C, ISO7220M		0.2	1	
t_r	Output signal rise time	See Figure 14		1		ns
t_f	Output signal fall time			1		ns
t_{fs}	Failsafe output delay time from input power loss	See Figure 15		3		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO722xM, 150 Mbps PRBS NRZ data, 5-bit max same polarity input, both channels, see Figure 17, Figure 13		1		ns
		ISO722xM, 150 Mbps unrestricted bit run length data input, both channels, see Figure 17		2		

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified pins of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

6.17 Switching Characteristics—3.3-V V_{CC1} and V_{CC2} Supplies

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO722xA, see Figure 14	290	400	610	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			1	22	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xB, see Figure 14	46	62	78	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			1	4	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xC, see Figure 14	26	40	52	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			1	3	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO722xM, see Figure 14	8	16	25	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			0.5	1	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xA			190	ns
		ISO722xB			17	
		ISO722xC			10	
		ISO722xM			5	
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO7220A		3	15	ns
		ISO7220B		0.6	3	
		ISO7220C, ISO7220M		0.2	1	
t_r	Output signal rise time	See Figure 14		2		ns
t_f	Output signal fall time			2		ns
t_{fs}	Failsafe output delay time from input power loss	See Figure 15		3		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO722xM, 150 Mbps PRBS NRZ data, 5-bit max same polarity input, both channels, See Figure 17, Figure 13		1		ns
		ISO722xM, 150 Mbps unrestricted bit run length data input, both channels, See Figure 17		2		

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified pins of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

6.18 Switching Characteristics—2.8-V V_{CC1} and V_{CC2} Supplies

V_{CC1} and V_{CC2} at 2.8 V (over recommended operating conditions unless otherwise noted.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO722xC, see Figure 14	26	45	65	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)			1.5	5	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xC			12	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO7220C		0.2	5	ns
t_r	Output signal rise time	See Figure 14		2		ns
t_f	Output signal fall time			2		ns
t_{fs}	Failsafe output delay time from input power loss	See Figure 15		4.6		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified pins of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

6.19 Insulation Characteristics Curves

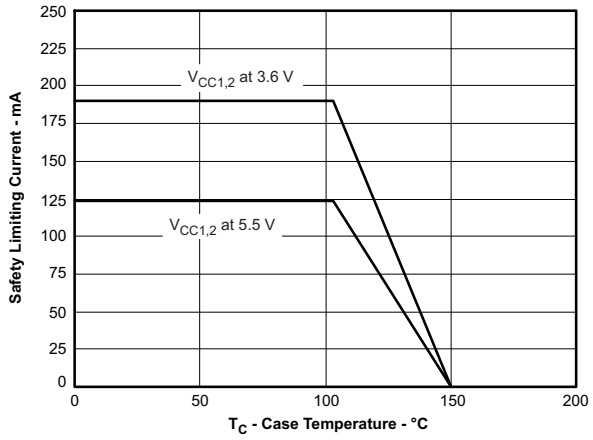


Figure 1. Thermal Derating Curve for Limiting Current per VDE

6.20 Typical Characteristics

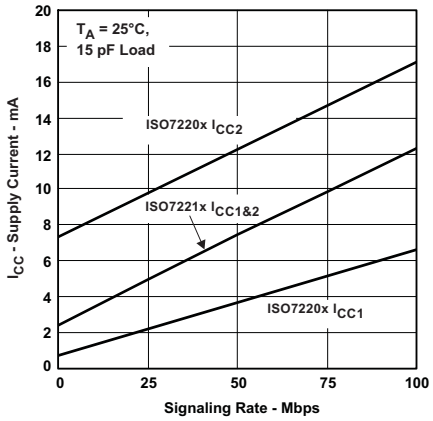


Figure 2. 3.3-V_{RMS} Supply Current vs Signaling Rate (Mbps)

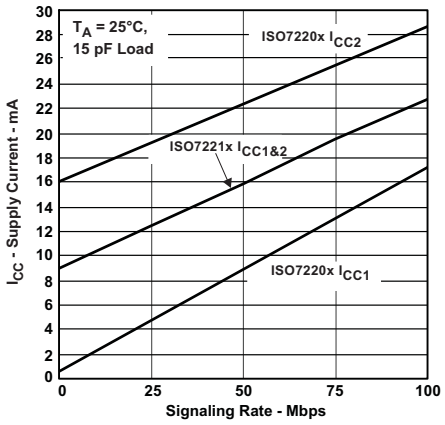


Figure 3. 5-V_{RMS} Supply Current vs Signaling Rate (Mbps)

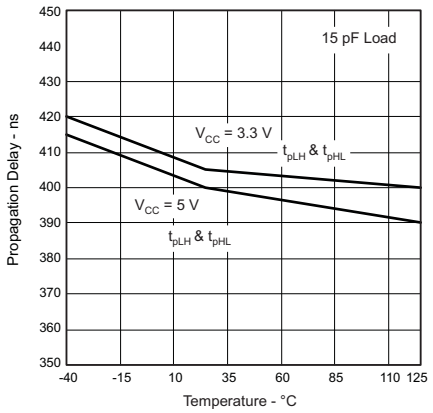


Figure 4. Propagation Delay vs Free-Air Temperature, ISO722xA

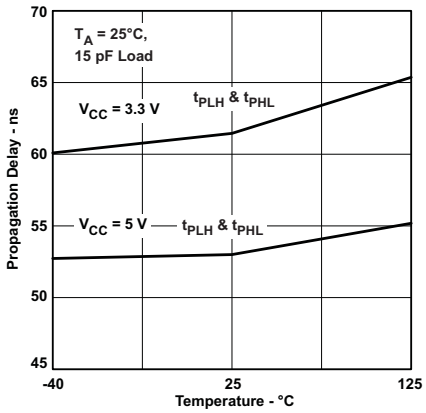


Figure 5. Propagation Delay vs Free-Air Temperature, ISO722xB

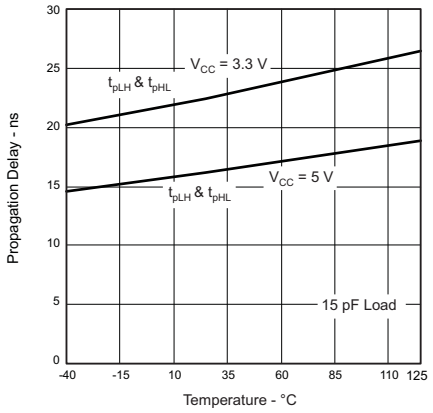


Figure 6. Propagation Delay vs Free-Air Temperature, ISO722xC

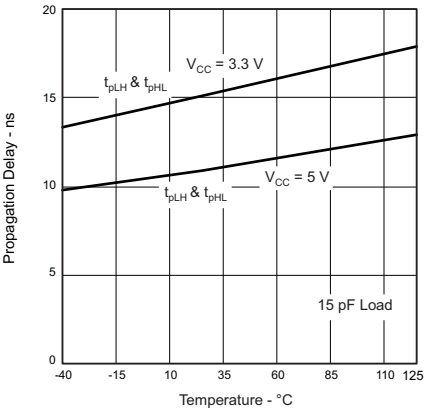


Figure 7. Propagation Delay vs Free-Air Temperature, ISO722xM

Typical Characteristics (continued)

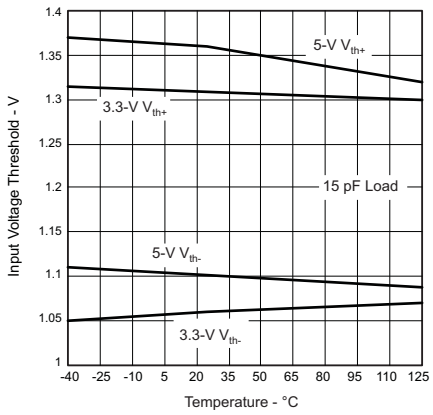


Figure 8. ISO722xA, ISO722xB and ISO722xC Input Voltage Low-to-High Switching Threshold vs Free-Air Temperature

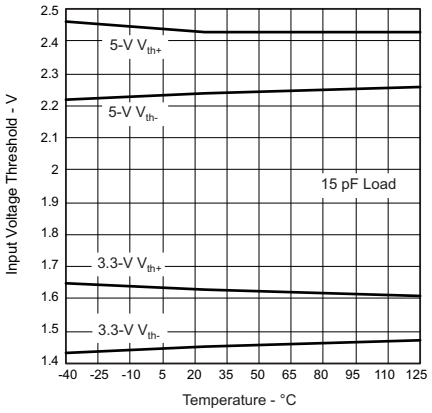


Figure 9. ISO722xM Input Voltage High-to-Low vs Free-Air Temperature

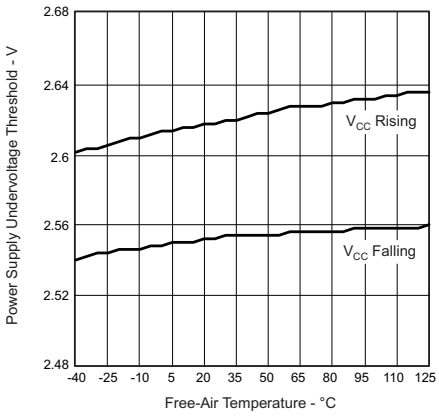


Figure 10. V_{CC} Undervoltage Threshold vs Free-Air Temperature

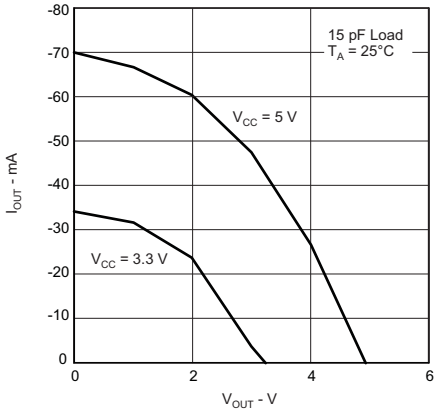


Figure 11. High-Level Output Current vs High-Level Output Voltage

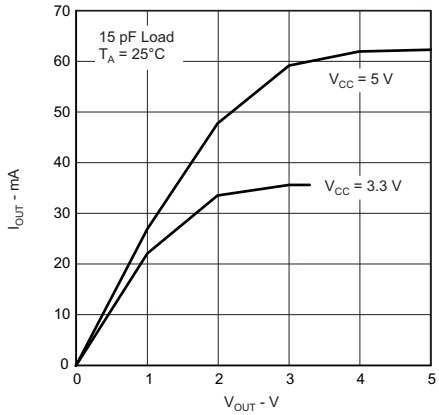


Figure 12. Low-Level Output Current vs Low-Level Output Voltage

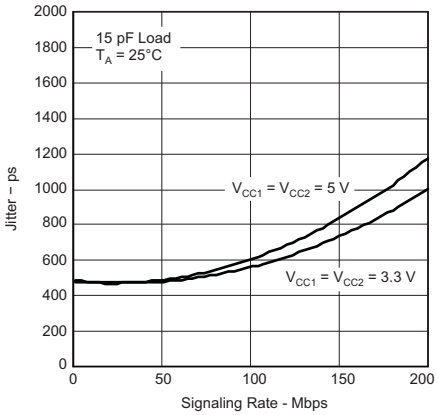
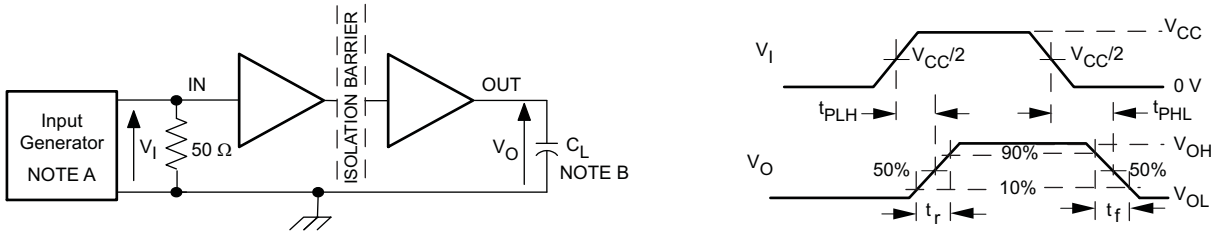


Figure 13. ISO722xM Jitter vs Signaling Rate

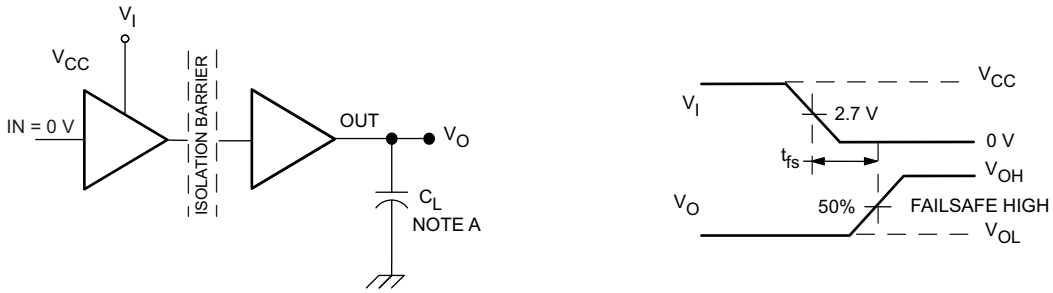
7 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

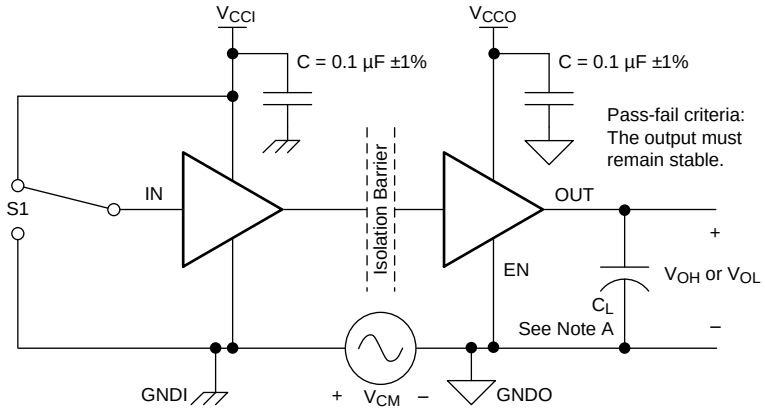
B. C_L = 15 pF and includes instrumentation and fixture capacitance within ± 20%.

Figure 14. Switching Characteristic Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ± 20%.

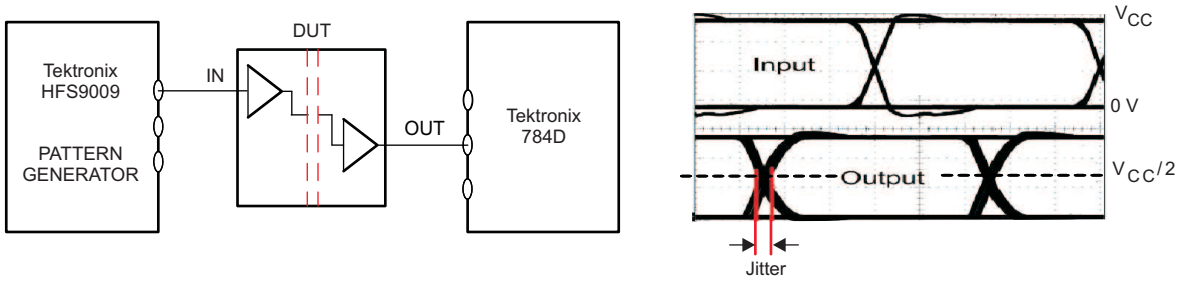
Figure 15. Failsafe Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ± 20%.

Figure 16. Common-Mode Transient Immunity Test Circuit

Parameter Measurement Information (continued)



NOTE: PRBS bit pattern run length is $2^{16} - 1$. Transition time is 800 ps.

Figure 17. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform

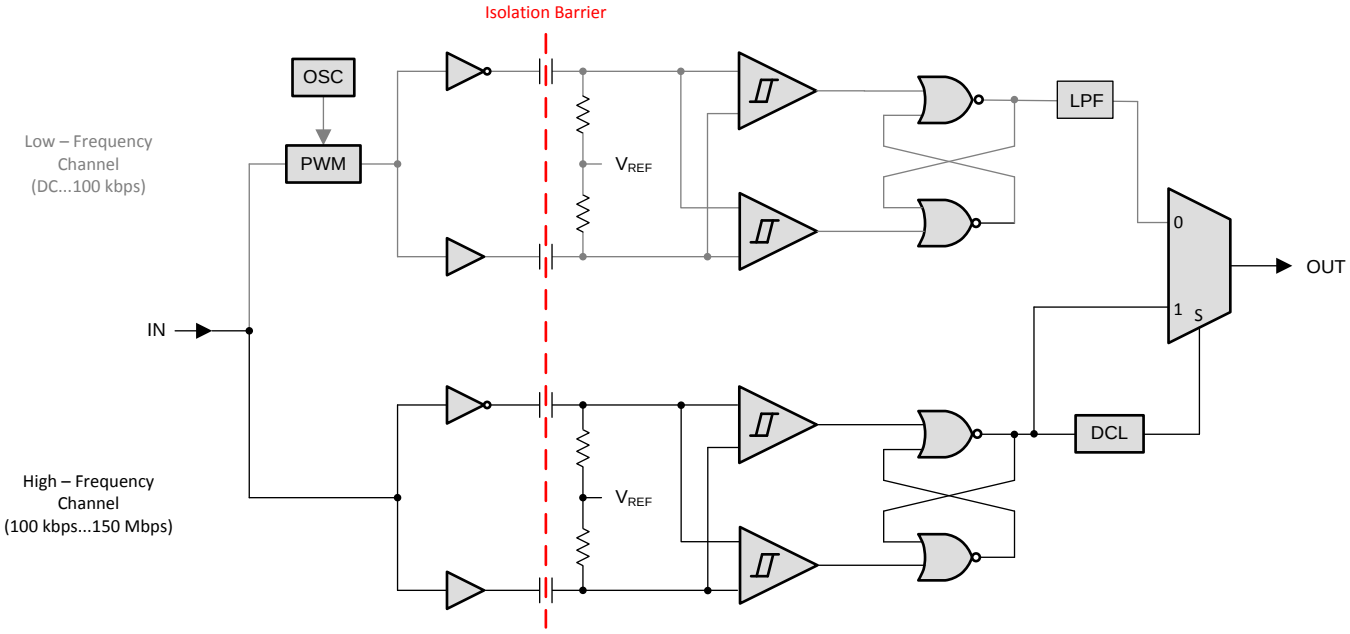
8 Detailed Description

8.1 Overview

The isolator in the*Functional Block Diagram* is based on a capacitive isolation barrier technique. The I/O channel of the ISO7220x and ISO7221x family of devices consists of two internal data channels, a high-frequency channel (HF) with a bandwidth from 100 kbps up to 150 Mbps, and a low-frequency channel (LF) covering the range from 100 kbps down to DC. In principle, a single-ended input signal entering the HF-channel is split into a differential signal via the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transients, which then are converted into differential pulses by two comparators. The comparator outputs drive a NOR-gate flip-flop whose output feeds an output multiplexer. A decision logic (DCL) at the driving output of the flip-flop measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, (as in the case of a low-frequency signal), the DCL forces the output-multiplexer to switch from the high-frequency to the low-frequency channel.

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency signal, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.

8.2 Functional Block Diagram



8.3 Feature Description

Table 1 provides an overview of the device features.

Table 1. Device Features

PART NUMBER	MAXIMUM SIGNALING RATE	INPUT THRESHOLD	CHANNEL DIRECTION
ISO7220A	1 Mbps	≈ 1.5 V (TTL) (CMOS compatible)	Same direction
ISO7220B	5 Mbps	≈ 1.5 V (TTL) (CMOS compatible	
ISO7220C	25 Mbps	≈ 1.5 V (TTL) (CMOS compatible)	
ISO7220M	150 Mbps	V_{CC}/ 2 (CMOS)	
ISO7221A	1 Mbps	≈ 1.5 V (TTL) (CMOS compatible)	Opposite directions
ISO7221B	5 Mbps	≈ 1.5 V (TTL) (CMOS compatible)	
ISO7221C	25 Mbps	≈ 1.5 V (TTL) (CMOS compatible)	
ISO7221M	150 Mbps	V_{CC}/ 2 (CMOS)	

8.4 Device Functional Modes

The ISO7220x and ISO7221x family of devices functional modes are listed in Table 2.

Table 2. ISO7220x or ISO7221x Function Table(1)

INPUT SIDE V_{CC}	OUTPUT SIDE V_{CC}	INPUT (IN)	OUTPUT (OUT)
PU	PU	H	H
		L	L
		Open	H
PD	PU	X	H
X	PD	X	Undetermined

(1) PU = Powered Up (V_{CC} ≥ 3.0 V), PD = Powered Down (V_{CC} ≤ 2.5 V), X = Irrelevant, H = High Level, L = Low Level

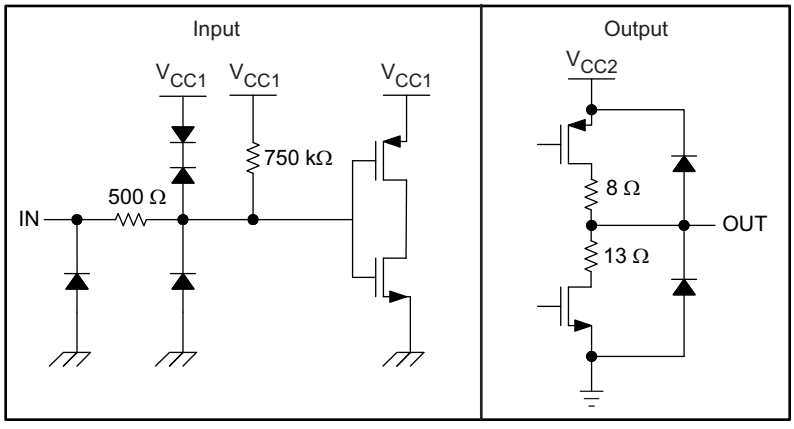


Figure 18. Device I/O Schematics

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO7220x and ISO7221x family devices use single-ended TTL or CMOS-logic switching technology. The supply voltage range is from 3 V (2.8 V for C-grade) to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, μC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

The ISO7221x family of devices can be used with Texas Instruments' mixed signal micro-controller, digital-to-analog converter, transformer driver, and voltage regulator to create an isolated 4- to 20-mA current loop.

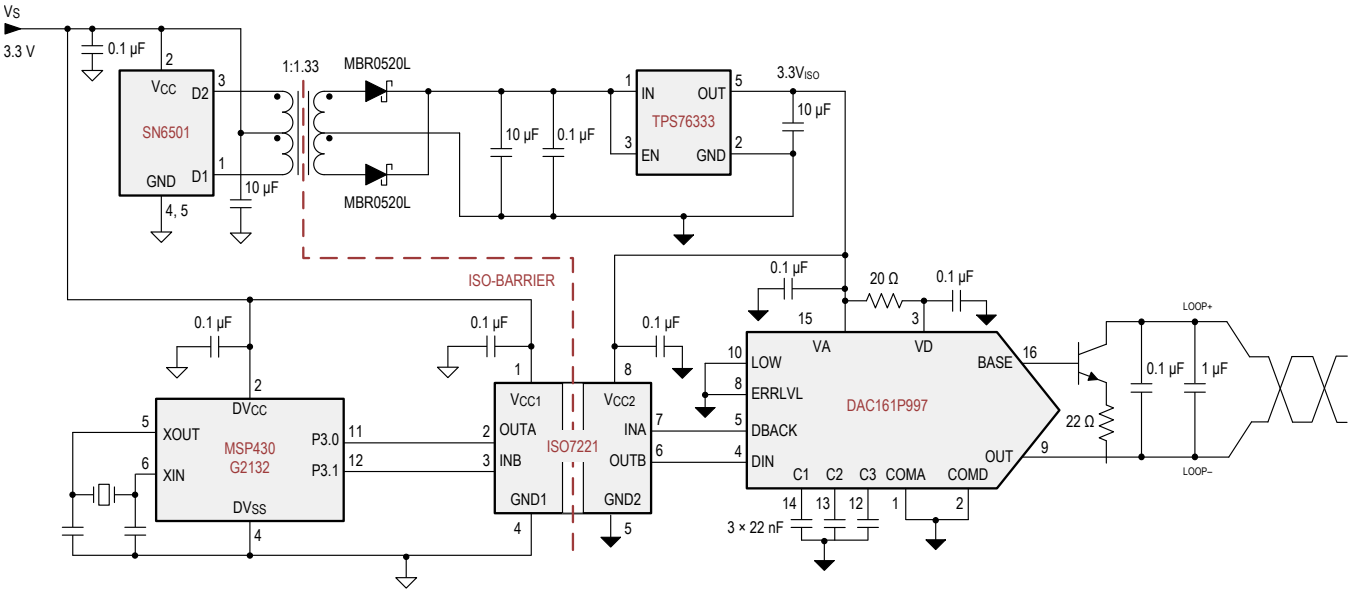


Figure 19. Isolated 4- to 20-mA Current Loop

9.2.1 Design Requirements

Unlike optocouplers, which require external components to improve performance, provide bias (or limit current), the ISO7220x and ISO7221x devices require only two external bypass capacitors to operate.

Typical Application (continued)

9.2.2 Detailed Design Procedure

Figure 20 and Figure 21 show the hookup of a typical ISO7220x and ISO7221x circuit. The only external components are two bypass capacitors.

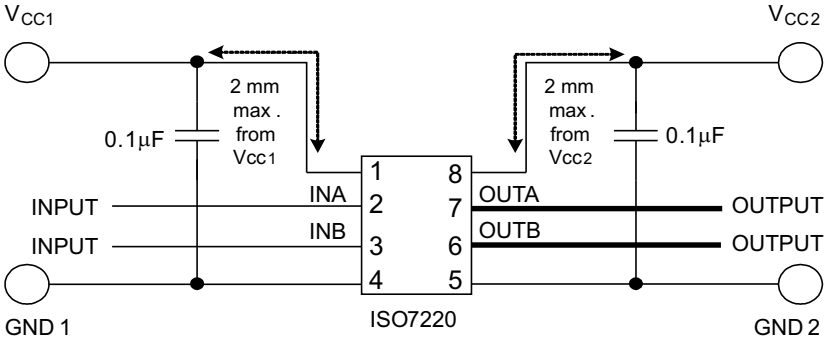


Figure 20. Typical ISO7220x Circuit Hook-Up

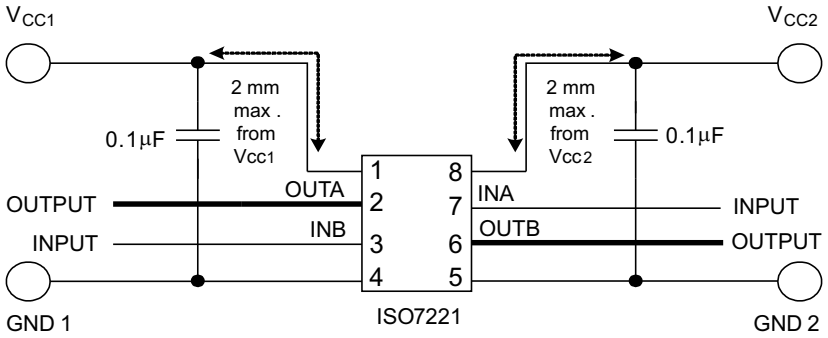


Figure 21. Typical ISO7221x Circuit Hook-Up

9.2.3 Application Curve

At maximum working voltage, the isolation barrier of the ISO7220x and ISO7221x family of devices has more than 28 years of life.

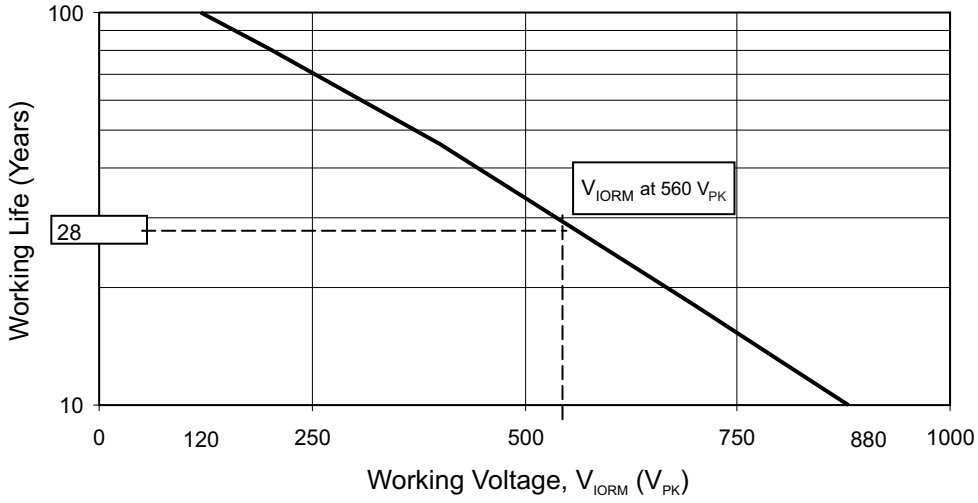


Figure 22. Time-Dependent Dielectric Breakdown Test Results

10 Power Supply Recommendations

To help ensure reliable operation at all data rates and supply voltages, a 0.1-μF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments SN6501 device. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501 Transformer Driver for Isolated Power Supplies*.

11 Layout

11.1 Layout Guidelines

A minimum of four layers are required to accomplish a low EMI PCB design (see Figure 23). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Route the high-speed traces on the top layer to avoid the use of vias (and the introduction of the inductances) and allow for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Place a solid ground plane next to the high-speed signal layer to establish controlled impedance for transmission line interconnects and provide an excellent low-inductance path for the return current flow.
- Place the power plane next to the ground plane to create additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Route the slower speed control signals on the bottom layer to allow for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. Adding a second plane system to the stack makes the stack mechanically stable and prevents it from warping. The power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the *Digital Isolator Design Guide*.

11.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

11.2 Layout Example

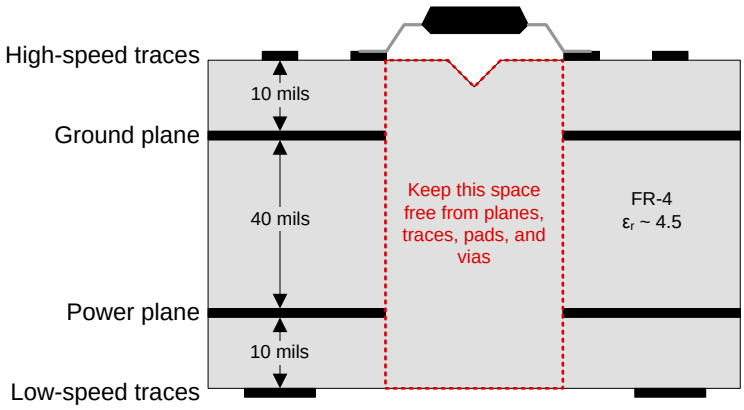


Figure 23. Recommended Layer Stack

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

有关开发支持，请参阅：

- 带 DALI DMX512 与电力线通信的交流电源 LED 照明参考设计
- 工业伺服驱动器和交流逆变器驱动器参考设计
- 低成本单相/两相隔离式电量测量参考设计
- 抗噪电容式触摸屏 HMI 参考设计
- 2 类 PoE PSE、6kV 雷电浪涌参考设计

12.2 文档支持

12.2.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《适用于 4mA 至 20mA 回路的 DAC161P997 单线 16 位 DAC》数据表*
- 德州仪器 (TI)，*《数字隔离器设计指南》*
- 德州仪器 (TI)，*《ISO72x 系列数字隔离器高压使用寿命》应用报告*
- 德州仪器 (TI)，*隔离相关术语*
- 德州仪器 (TI)，*《MSP430G2x32 混合信号微控制器》数据表*
- 德州仪器 (TI)，*《SN6501 用于隔离式电源的变压器驱动器》数据表*
- 德州仪器 (TI)，*《TPS763xx 低功耗 150mA 低压降线性稳压器》数据表*

12.3 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 3. 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
ISO7220A	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ISO7220B	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ISO7220C	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ISO7220M	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ISO7221A	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ISO7221B	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ISO7221C	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ISO7221M	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.4 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.5 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

12.6 商标

E2E is a trademark of Texas Instruments.
DeviceNet is a trademark of Open DeviceNet Vendors Association.
Profibus is a trademark of Profibus.
All other trademarks are the property of their respective owners.

12.7 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.8 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7220AD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220A	Samples
ISO7220ADG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220A	Samples
ISO7220ADR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220A	Samples
ISO7220ADRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220A	Samples
ISO7220BD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220B	Samples
ISO7220BDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220B	Samples
ISO7220BDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220B	Samples
ISO7220BDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220B	Samples
ISO7220CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220C	Samples
ISO7220CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220C	Samples
ISO7220MD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220M	Samples
ISO7220MDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220M	Samples
ISO7220MDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220M	Samples
ISO7220MDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7220M	Samples
ISO7221AD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221A	Samples
ISO7221ADG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221A	Samples
ISO7221ADR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221A	Samples
ISO7221ADRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221A	Samples
ISO7221BD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221B	Samples
ISO7221BDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7221BDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221B	Samples
ISO7221CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221C	Samples
ISO7221CDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221C	Samples
ISO7221CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221C	Samples
ISO7221CDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221C	Samples
ISO7221MD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221M	Samples
ISO7221MDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221M	Samples
ISO7221MDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221M	Samples
ISO7221MDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	I7221M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF ISO7220A, ISO7221A, ISO7221C :

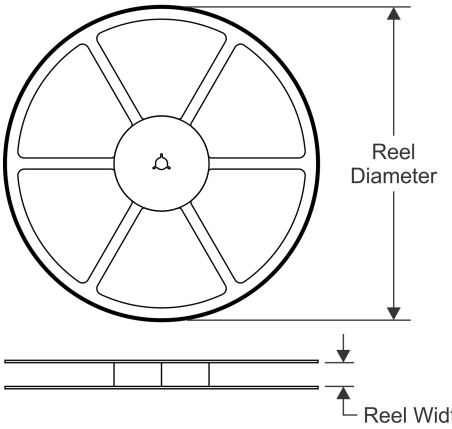
- Automotive : ISO7220A-Q1, ISO7221A-Q1, ISO7221C-Q1

NOTE: Qualified Version Definitions:

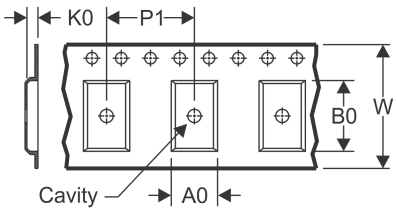
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

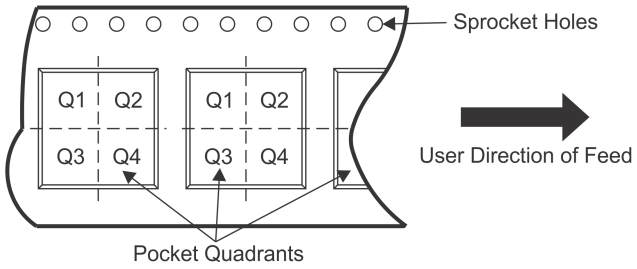


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

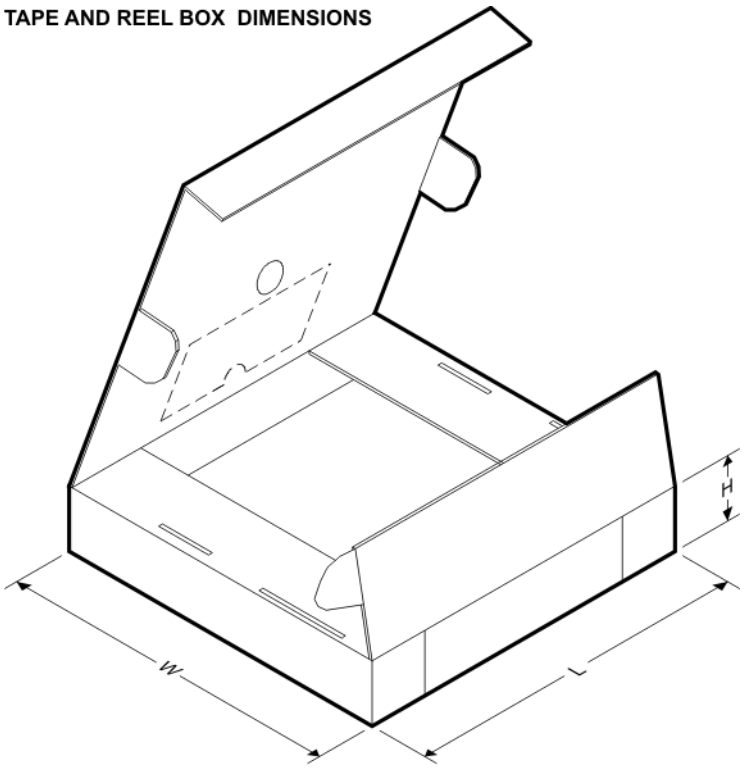
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7220ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7220BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7220CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7220MDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7221ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7221BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7221CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7221MDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

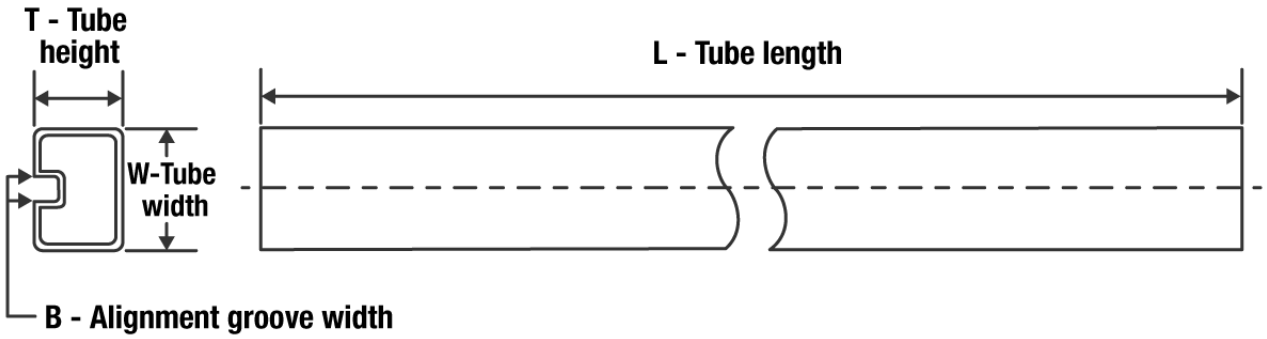
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

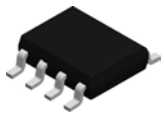
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7220ADR	SOIC	D	8	2500	350.0	350.0	43.0
ISO7220BDR	SOIC	D	8	2500	350.0	350.0	43.0
ISO7220CDR	SOIC	D	8	2500	350.0	350.0	43.0
ISO7220MDR	SOIC	D	8	2500	350.0	350.0	43.0
ISO7221ADR	SOIC	D	8	2500	350.0	350.0	43.0
ISO7221BDR	SOIC	D	8	2500	350.0	350.0	43.0
ISO7221CDR	SOIC	D	8	2500	350.0	350.0	43.0
ISO7221MDR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO7220AD	D	SOIC	8	75	505.46	6.76	3810	4
ISO7220ADG4	D	SOIC	8	75	505.46	6.76	3810	4
ISO7220BD	D	SOIC	8	75	505.46	6.76	3810	4
ISO7220BDG4	D	SOIC	8	75	505.46	6.76	3810	4
ISO7220CD	D	SOIC	8	75	505.46	6.76	3810	4
ISO7220MD	D	SOIC	8	75	505.46	6.76	3810	4
ISO7220MDG4	D	SOIC	8	75	505.46	6.76	3810	4
ISO7221AD	D	SOIC	8	75	505.46	6.76	3810	4
ISO7221ADG4	D	SOIC	8	75	505.46	6.76	3810	4
ISO7221BD	D	SOIC	8	75	505.46	6.76	3810	4
ISO7221CD	D	SOIC	8	75	505.46	6.76	3810	4
ISO7221CDG4	D	SOIC	8	75	505.46	6.76	3810	4
ISO7221MD	D	SOIC	8	75	505.46	6.76	3810	4
ISO7221MDG4	D	SOIC	8	75	505.46	6.76	3810	4

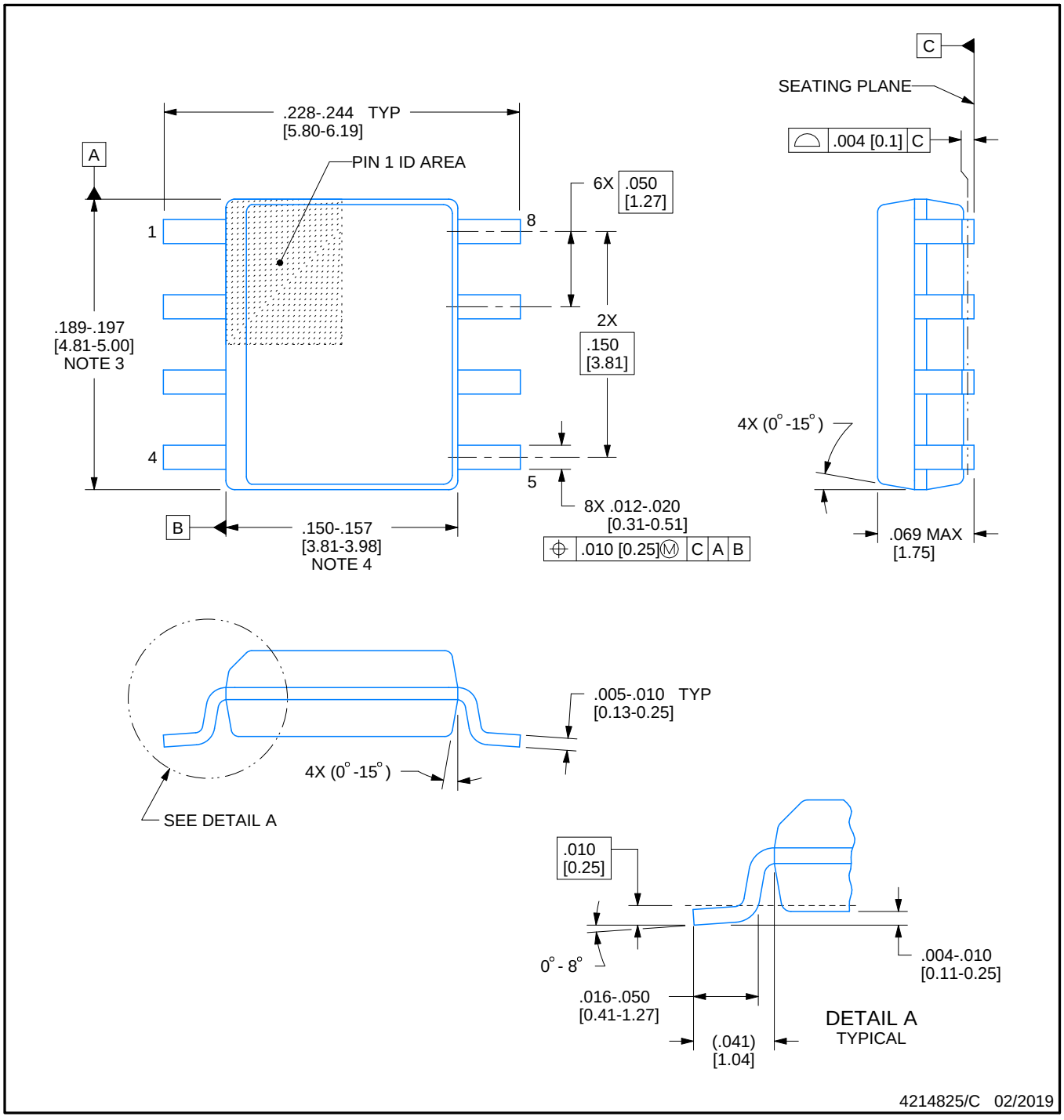


PACKAGE OUTLINE

D0008A

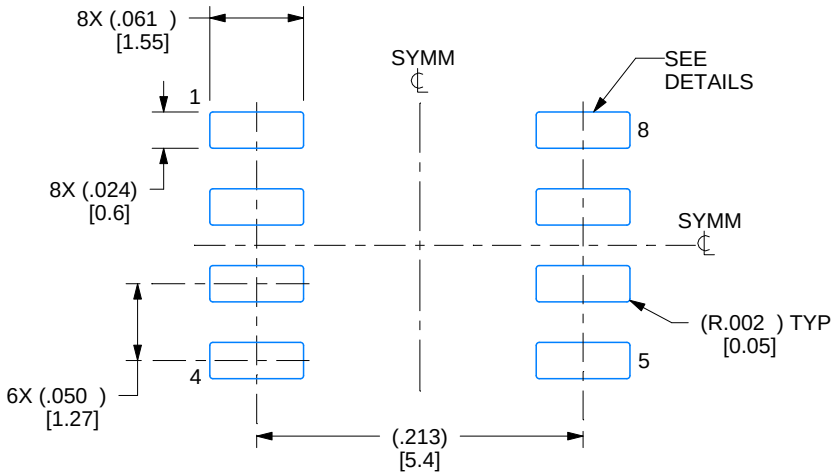
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

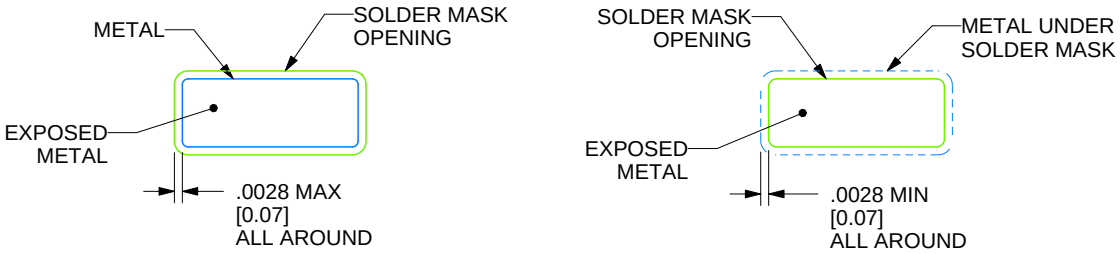


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

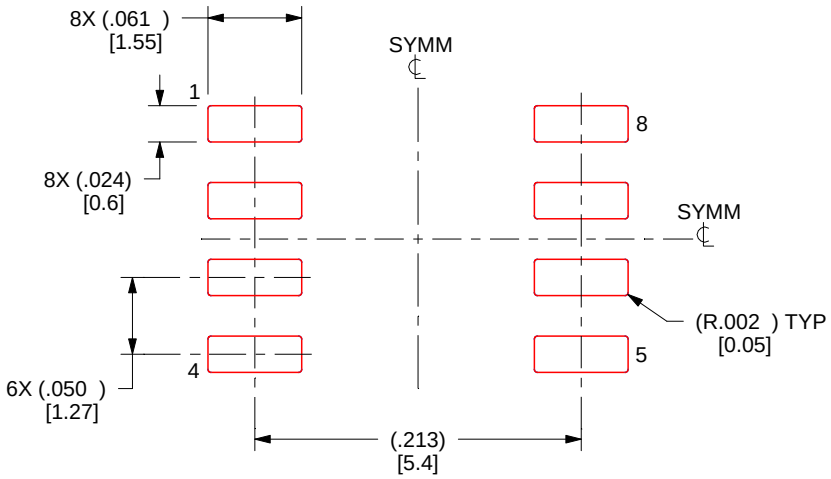
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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