ISO7841x 高性能、8000V_{PK} 增强型四通道数字隔离器

1 特性

- 信号传输速率：高达 100Mbps
- 宽电源电压范围：2.25V 至 5.5V
- 2.25V 至 5.5V 电平转换
- 宽温度范围：–55°C 至 +125°C
- 低功耗：电流典型值为 1.7mA/通道（1Mbps 时）
- 低传播延迟：典型值为 11ns（5V 电源供电时）
- 行业领先的 CMTI（最小值）：±100 kV/μs
- 优异的电磁兼容性 (EMC)
- 系统级静电放电 (ESD)、瞬态放电 (EFT) 以及抗浪涌保护
- 低辐射
- 隔离层寿命：40 年以上
- 宽体 SOIC-16 封装和超宽体 SOIC-16 封装选项
- 安全及管理批准：中的“安全及管理批准”列表中的“安全及管理批准”列表
  - 8000 V_{PK} 增强型隔离，符合 DIN V VDE V 0884-10 (VDE V 0884-10)：2006-12
  - 符合 UL 1577 标准且长达 1 分钟的 5.7kV_{RMS} 隔离
  - CSA 组件验收通知 5A，IEC 60950-1 和 IEC 60601-1 终端设备标准
  - 符合 GB4943.1-2011 标准的 CQC 认证
  - 符合 EN 61010-1 和 EN 60950-1 标准的 TUV 认证
  - 完成了所有 DW 封装认证；完成了符合 UL、VDE、TUV 标准的 DWW 封装认证并且已针对 CSA 和 CQC 进行了规划

2 应用

- 工业自动化
- 电机控制
- 电源
- 太阳能逆变器
- 医疗设备
- 混合动力电动汽车

3 说明

ISO7841x 器件是一款高性能四通道数字隔离器，隔离电压为 8000V_{PK}。该器件已通过符合 VDE、CSA、CQC 和 TUV 标准的增强型隔离认证。在隔离互补金属氧化物半导体 (CMOS) 或者低电压互补金属氧化物半导体 (LVCMOS) 数字 I/O 时，该隔离器可提供高电磁抗扰度和低辐射，同时具备低功耗特性。每个隔离通道都有一个由二氧化硅 (SiO_2) 绝缘隔栅分开的逻辑输入和输出缓冲器。

该器件配有使能引脚，可用于将多个主驱动应用中的相应输出置于 高阻抗状态， 也可用于降低功耗。ISO7841 器件具有 3 个正向通道和 1 个反向通道。如果出现输入功率或信号丢失，ISO7841 器件默认输出高电平，ISO7841F 器件默认输出低电平。有关更多详细信息，请参阅 *Device Functional Modes*器件功能模式部分。

与隔离式电源结合使用时，该器件有助于防止数据总线或者其他电路中的噪声电流进入本地接地，进而干扰或损坏敏感电路。凭借创新的芯片设计和布线技术，ISO7841 器件的电磁兼容性得到了显著增强，可确保提供系统级 ESD、EFT 和浪涌保护并符合辐射标准。

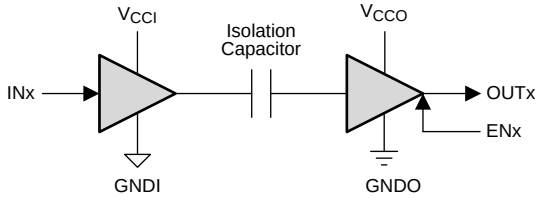
ISO7841 器件采用 16 引脚 SOIC 宽体 (DW) 和超宽体 (DWW) 封装。

器件信息(1)

产品型号	封装	封装尺寸（标称值）
ISO7841 ISO7841F	DW (16)	10.30mm x 7.50mm
	DWW (16)	10.30mm x 14.0mm

(1) 要了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化电路原理图



V_{CCI} 和 GNDI 分别是输入通道的电源和接地连接。

V_{CCO} 和 GNDO 分别是输出通道的电源和接地连接。

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision F (April 2016) to Revision G **Page**

- Changed part numbers in the *Power Ratings* table (previously *Power Dissipation Characteristics*) ... 7
- Changed the input-to-output test voltage parameter to apparent charge in the *Insulation Specifications* ... 8
- 已添加 *接收文档更新通知*部分 ... 26

Changes from Revision E (March 2016) to Revision F **Page**

- 已更改 隔离层寿命年数（*特性*部分） ... 1
- VDE 认证现在已完成 ... 1
- Changed V_{CCO} to V_{CCI} for the minimum value of the input threshold voltage hysteresis parameter in all electrical characteristics tables ... 10
- Added V_{CM} to the test condition of the common-mode transient immunity parameter in all electrical characteristics tables ... 10
- Added the lifetime projection graphs for DW and DWW packages to the *Safety Limiting Values* section ... 15

Changes from Revision D (December 2015) to Revision E **Page**

- 更改了“安全及管理批准”列表*特性* ... 1
- 在*特性*中添加了“符合 EN 61010-1 和 EN 60950-1 标准的 TUV 认证” ... 1
- 将*说明*的第一段中的文本从“符合 VDE、CSA 和 CQC 的认证” 更改为“符合 VDE、CSA、CQC 和 TUV 的认证。” ... 1
- Added Note 1 to *Insulation Characteristics* ... 8
- Changed *IEC 60664-1 Ratings Table* ... 8

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- Added TUV to the *Regulatory Information* section and Regulatory Information. Deleted Note 1 in Regulatory Information 9
- Changed *Device I/O Schematics* 21

Changes from Revision C (July 2015) to Revision D **Page**

- 在*特性*中添加了“完成了 DW 封装认证；规划了 DWW 认证”..... 1
- 向*说明*部分添加了文本：“和超宽体 (DWW) 封装”。..... 1
- 已将封装“超宽 SOIC、DWW (16)”添加至*器件信息*表..... 1
- Added the 16-DWW Package to *Package Insulation and Safety-Related Specifications*..... 8
- Added the DWW package information to *Package Insulation and Safety-Related Specifications* 8
- Added the DWW package information to *Regulatory Information*..... 9
- Changed the MIN value of CMTI in *Electrical Characteristics—5-V Supply*, 5 V table From: 70 To: 100 kV/μs, deleted the TYP value of 100 kV/μs..... 10
- Added the Supply Current - ISO7841DW and ISO7841FDW section to the *Supply Current Characteristics—5-V Supply* 10
- Added the Supply Current - ISO7841DWW and ISO7841FDWW section to the *Supply Current Characteristics—5-V Supply* 10
- Changed the MIN value of CMTI in *Electrical Characteristics—3.3-V Supply*, 5 V table From: 70 To: 100 kV/μs, deleted the TYP value of 100 kV/μs..... 11
- Added the Supply Current - ISO7841DW and ISO7841FDW section to the *Electrical Characteristics—3.3-V Supply*..... 11
- Added the Supply Current - ISO7841DWW and ISO7841FDWW section to the *Electrical Characteristics—3.3-V Supply* 11
- Changed the MIN value of CMTI in *Electrical Characteristics—2.5-V Supply*, 5 V table From: 70 To: 100 kV/μs, deleted the TYP value of 100 kV/μs..... 12
- Added the Supply Current - ISO7841DW and ISO7841FDW section to the *Supply Current Characteristics—2.5-V Supply*..... 12
- Added the Supply Current - ISO7841DWW and ISO7841FDWW section to the *Supply Current Characteristics—2.5-V Supply* 12
- Added text to the *Application Information* section: " isolation voltage per UL 1577." 22

Changes from Revision B (January 2015) to Revision C **Page**

- 已添加器件 ISO7481F 至数据表..... 1
- 已更改 *说明*以包含“ISO7841 器件默认输出为“高”，ISO7841F 器件默认输出为“低””。 1
- Changed From: t_{PLH} and t_{PHL}at 5.5V To: t_{PLH} and t_{PHL} at 5.0 V 16
- Changed *Default Output Delay Time Test Circuit and Voltage Waveforms*..... 18
- Added the *Device I/O Schematics* section 21

Changes from Revision A (January 2015) to Revision B **Page**

- 已将文档标题从“四通道数字隔离器”更改为“四通道 3/1 数字隔离器” 1
- 在*特性*部分添加了“2.25V 至 5.5V 电平转换”..... 1
- 将*特性*中的“宽体 SOIC-16 封装”更改为“宽体和超宽体 SOIC-16 封装选项”..... 1
- 更改了*特性*..... 1
- VDE 认证现在已完成 1
- 更改了简化电路原理图并增加了注释 1 和注释 2 1
- Added the *Power Dissipation Characteristics* table..... 7
- Changed *Package Insulation and Safety-Related Specifications* title From: *IEC Insulation and Safety-Related Specifications for DW-16 Package* To: *Package Insulation and Safety-Related Specifications* 8
- Changed *Package Insulation and Safety-Related Specifications* 8

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- Changed *Insulation Characteristics* title From: *DIN V VDE 0884-10 (VDE V 0884-10) and UL 1577 Insulation Characteristics* To: *Insulation Characteristics* 8
- Changed *Insulation Characteristics* 8
- Changed the Test Condition of CTI of the table in *Package Insulation and Safety-Related Specifications* 8
- Changed the MIN value of CTI From" > 600 V To: 600 V 8
- Changed title From: *Regulatory Information (All Certifications Planned)Regulatory Information (All Certifications Planned)* To: *Regulatory Information* 9
- Changed the table in *Regulatory Information* 9
- Changed *Safety Limiting Values*, added I_S DW-16 package options 9
- Changed *Switching Characteristics Test Circuit and Voltage Waveforms* 17
- Changed *Enable/Disable Propagation Delay Time Test Circuit and Waveform* 17
- Changed From: V_{CC1} To: V_{CCI} in *Default Output Delay Time Test Circuit and Voltage Waveforms* 18
- Changed *Common-Mode Transient Immunity Test Circuit* 18
- Deleted INPUT-SIDE and OUTPUT-SIDE from columns 1 and 2 of *Function Table* 21
- Changed the *Application Information* section 22
- Changed the *Application Information* section 22

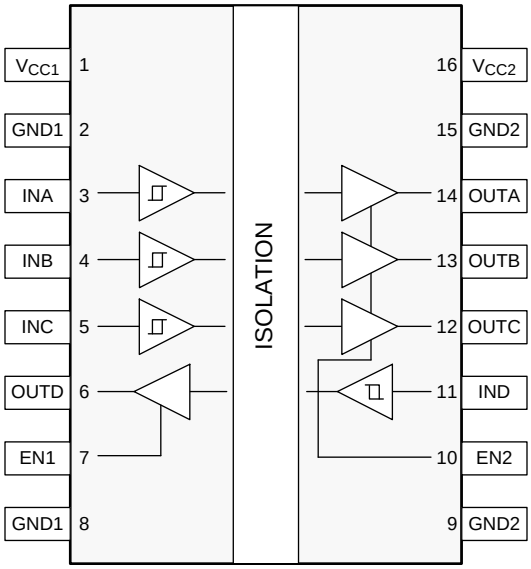
Changes from Original (November 2014) to Revision A **Page**

- 已将器件状态从“产品预览”更新为“量产数据” 1

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5 Pin Configuration and Functions

DW and DWW Packages
16-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN1	7	I	Output enable 1. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low.
EN2	10	I	Output enable 2. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.
GND1	2	—	Ground connection for V_{CC1}
	8		
GND2	9	—	Ground connection for V_{CC2}
	15		
INA	3	I	Input, channel A
INB	4	I	Input, channel B
INC	5	I	Input, channel C
IND	11	I	Input, channel D
OUTA	14	O	Output, channel A
OUTB	13	O	Output, channel B
OUTC	12	O	Output, channel C
OUTD	6	O	Output, channel D
V_{CC1}	1	—	Power supply, V_{CC1}
V_{CC2}	16	—	Power supply, V_{CC2}

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6 Specifications

6.1 Absolute Maximum Ratings

See (1)

			MIN	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage(2)		–0.5	6	V
	Voltage	INx	–0.5	V_{CCX} + 0.5(3)	V
		OUTx	–0.5	V_{CCX} + 0.5(3)	
		ENx	–0.5	V_{CCX} + 0.5(3)	
I_O	Output current		–15	15	mA
	Surge immunity			12.8	kV
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6 V

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±6000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage		2.25		5.5	V
I_{OH}	High-level output current	V_{CCO}(1) = 5 V	–4			mA
		V_{CCO}(1) = 3.3 V	–2			
		V_{CCO}(1) = 2.5 V	–1			
I_{OL}	Low-level output current	V_{CCO}(1) = 5 V			4	mA
		V_{CCO}(1) = 3.3 V			2	
		V_{CCO}(1) = 2.5 V			1	
V_{IH}	High-level input voltage		0.7 × V_{CCI} (1)		V_{CCI} (1)	V
V_{IL}	Low-level input voltage		0		0.3 × V_{CCI}(1)	V
DR	Signaling rate		0		100	Mbps
T_J	Junction temperature(2)		–55		150	°C
T_A	Ambient temperature		–55	25	125	°C

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.
(2) To maintain the recommended operating conditions for T_J, see *Thermal Information*.

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6.4 Thermal Information

THERMAL METRIC(1)		ISO7841		UNIT
		DW (SOIC)	DWW (SOIC)	
		16 Pins	16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	78.9	78.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	41.6	41.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.6	49.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.5	15.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.1	48.8	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Power Ratings

$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150°C$, $C_L = 15$ pF, input a 50 MHz 50% duty cycle square wave

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation by ISO7841x				200	mW
P_{D1}	Maximum power dissipation by side-1 of ISO7841x				50	mW
P_{D2}	Maximum power dissipation by side-2 of ISO7841x				150	mW

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6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATION		UNIT
			DW	DWW	
GENERAL					
CLR	External clearance(1)	Shortest pin-to-pin distance through air	>8	>14.5	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface*High Voltage Feature Description*	>8	>14.5	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>21	>21	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A	>600	>600	V
	Material group		I	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V_{RMS}	I–IV	I–IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I–III	I–IV	
DIN V VDE V 0884-10 (VDE V 0884-10):2006-12(2)					
V_{IORM}	Maximum repetitive peak isolation voltage		2121	2828	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); Time dependent dielectric breakdown (TDDB) Test, see Figure 1 and Figure 2	1500	2000	V_{RMS}
		DC voltage	2121	2828	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$ t = 60 s (qualification) t= 1 s (100% production)	8000	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 60065, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 12800\ V_{PK}$ (qualification)	8000	8000	V_{PK}
q_{pd}	Apparent charge(4)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM} = 2545\ V_{PK}$ (DW) and 3394 V_{PK} (DWW), t_m = 10 s	≤5	≤5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM} = 3394\ V_{PK}$ (DW) and 4525 V_{PK} (DWW), t_m = 10 s	≤5	≤5	
		Method b1: At routine test (100% production) and preconditioning (type test) $V_{ini} = V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM} = 3977\ V_{PK}$ (DW) and 5303 V_{PK} (DWW), t_m = 1 s	≤5	≤5	
C_{IO}	Barrier capacitance, input to output(5)	$V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1 MHz	2	2	pF
R_{IO}	Isolation resistance, input to output(5)	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^9$	$>10^9$	
	Pollution degree		2	2	
	Climatic category		55/125/21	55/125/21	
UL 1577					
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 5700\ V_{RMS}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO} = 6840\ V_{RMS}$, t = 1 s (100% production)	5700	5700	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.

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6.7 Safety-Related Certifications

Certifications for the DW package are complete. DWW package certifications are complete for UL, VDE and TUV and planned for CSA and CQC.

VDE	CSA	UL	CQC	TUV
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 60950-1 (VDE 0805 Teil 1):2011-01	Approved under CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 60601-1	Certified according to UL 1577 Component Recognition Program	Certified according to GB 4943.1-2011	Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013
Reinforced insulation Maximum transient isolation voltage, 8000 V_{PK}; Maximum repetitive peak isolation voltage, 2121 V_{PK} (DW), 2828 V_{PK} (DWW); Maximum surge isolation voltage, 8000 V_{PK}	Reinforced insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed., 800 V_{RMS} (DW package) and 1450 V_{RMS} (DWW package) max working voltage (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3.1, 250 V_{RMS} (354 V_{PK}) max working voltage (DW package)	Single protection, 5700 V_{RMS}	Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage	5700 V_{RMS} Reinforced insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 600 V_{RMS} (DW package) and 1000 V_{RMS} (DWW package) 5700 V_{RMS} Reinforced insulation per EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013 up to working voltage of 800 V_{RMS} (DW package) and 1450 V_{RMS} (DWW package)
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certificate number: CQC15001121716	Client ID number: 77311

6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 78.9°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			288	mA
		$R_{\theta JA}$ = 78.9°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			440	
		$R_{\theta JA}$ = 78.9°C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C			576	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 78.9°C/W, T_J = 150°C, T_A = 25°C			1584	mW
T_S	Maximum safety temperature				150	°C

The maximum safety temperature is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

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6.9 Electrical Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 11	V_{CCO}(1) – 0.4	V_{CCO}(1) – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 11		0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CCI}(1)			V
I_{IH}	High-level input current	V_{IH} = V_{CCI}(1) at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI}(1) or 0 V, V_{CM} = 1500 V; see Figure 14	100			kV/µs
C_I	Input capacitance	V_I = V_{CC}/2 + 0.4 × sin (2πft), f = 1 MHz, V_{CC} = 5 V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

6.10 Supply Current Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7841DW AND ISO7841FDW							
Supply current	Disable	EN1 = EN2 = 0 V, V_I = 0 V (ISO7841F), V_I = V_{CCI}(1) (ISO7841)	I_{CC1}		1.1	1.8	mA
			I_{CC2}		0.8	1.3	
		EN1 = EN2 = 0 V, V_I = V_{CCI}(1) (ISO7841F), V_I = 0 V (ISO7841)	I_{CC1}		4.5	6.6	mA
			I_{CC2}		2	2.9	
	DC signal	V_I = 0 V (ISO7841F), V_I = V_{CCI}(1) (ISO7841)	I_{CC1}		1.5	2.4	mA
			I_{CC2}		2.1	3.1	
		V_I = V_{CCI}(1) (ISO7841F), V_I = 0 V (ISO7841)	I_{CC1}		5	7.3	mA
			I_{CC2}		3.4	4.9	
	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		3.3	4.9	mA
			I_{CC2}		2.9	4.2	
		10 Mbps	I_{CC1}		3.9	5.5	mA
			I_{CC2}		4.4	5.7	
		100 Mbps	I_{CC1}		9.2	11.6	mA
			I_{CC2}		19	21.9	
ISO7841DWW AND ISO7841FDWW							
Supply current	Disable	EN1 = EN2 = 0 V, V_I = 0 V (ISO7841F), V_I = V_{CCI}(1) (ISO7841)	I_{CC1}		1.1	1.8	mA
			I_{CC2}		0.8	1.3	
		EN1 = EN2 = 0 V, V_I = V_{CCI}(1) (ISO7841F), V_I = 0 V (ISO7841)	I_{CC1}		4.5	6.6	mA
			I_{CC2}		2	2.9	
	DC signal	V_I = 0 V (ISO7841F), V_I = V_{CCI}(1) (ISO7841)	I_{CC1}		1.5	2.4	mA
			I_{CC2}		2.1	3.3	
		V_I = V_{CCI}(1) (ISO7841F), V_I = 0 V (ISO7841)	I_{CC1}		5	7.5	mA
			I_{CC2}		3.4	5.2	
	All channels switching with square wave clock input;C_L = 15 pF	1 Mbps	I_{CC1}		3.4	5	mA
			I_{CC2}		3	4.4	
		10 Mbps	I_{CC1}		4	5.6	mA
			I_{CC2}		4.5	6.1	
		100 Mbps	I_{CC1}		9.4	12.1	mA
			I_{CC2}		19.5	22.6	

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

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6.11 Electrical Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA; see Figure 11	V_{CCO}(1) – 0.4	V_{CCO}(1) – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA; see Figure 11		0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CCI}(1)			V
I_{IH}	High-level input current	V_{IH} = V_{CCI}(1) at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	-10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI}(1) or 0 V, V_{CM} = 1500 V; see Figure 14	100			kV/µs

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

6.12 Electrical Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7841DW AND ISO7841FDW							
Supply current	Disable	EN1 = EN2 = 0 V, V_I = 0 V (ISO7841F), V_I = V_{CCI}(1) (ISO7841)	I_{CC1}		1.1	1.8	mA
			I_{CC2}		0.8	1.3	
		EN1 = EN2 = 0 V, V_I = V_{CCI}(1) (ISO7841F), V_I = 0 V (ISO7841)	I_{CC1}		4.5	6.6	mA
			I_{CC2}		1.9	2.9	
	DC signal	V_I = 0 V (ISO7841F), V_I = V_{CCI}(1) (ISO7841)	I_{CC1}		1.5	2.4	mA
			I_{CC2}		2.1	3.1	
		V_I = V_{CCI}(1) (ISO7841F), V_I = 0 V (ISO7841)	I_{CC1}		5	7.3	mA
			I_{CC2}		3.3	4.9	
	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		3.3	4.9	mA
			I_{CC2}		2.8	4.1	
		10 Mbps	I_{CC1}		3.7	5.3	mA
			I_{CC2}		3.9	5.2	
		100 Mbps	I_{CC1}		7.4	9.3	mA
			I_{CC2}		14.5	16.9	
ISO7841DWW AND ISO7841FDWW							
Supply current	Disable	EN1 = EN2 = 0 V, V_I = 0 V (ISO7841F), V_I = V_{CCI}(1) (ISO7841)	I_{CC1}		1.1	1.8	mA
			I_{CC2}		0.8	1.3	
		EN1 = EN2 = 0 V, V_I = V_{CCI}(1) (ISO7841F), V_I = 0 V (ISO7841)	I_{CC1}		4.5	6.6	mA
			I_{CC2}		2	2.9	
	DC signal	V_I = 0 V (ISO7841F), V_I = V_{CCI}(1) (ISO7841)	I_{CC1}		1.5	2.4	mA
			I_{CC2}		2.1	3.3	
		V_I = V_{CCI}(1) (ISO7841F), V_I = 0 V (ISO7841)	I_{CC1}		5	7.5	mA
			I_{CC2}		3.4	5.2	
	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		3.4	5	mA
			I_{CC2}		2.9	4.4	
		10 Mbps	I_{CC1}		3.8	5.4	mA
			I_{CC2}		4	5.5	
		100 Mbps	I_{CC1}		7.5	9.9	mA
			I_{CC2}		14.8	17.2	

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

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6.13 Electrical Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA; see Figure 11	V_{CCO}(1) – 0.4	V_{CCO}(1) – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA; see Figure 11		0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CCI}(1)			V
I_{IH}	High-level input current	V_{IH} = V_{CCI}(1) at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI}(1) or 0 V, V_{CM} = 1500 V; see Figure 14	100			kV/µs

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

6.14 Supply Current Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7841DW AND ISO7841FDW							
Supply current	Disable	EN1 = EN2 = 0 V, V_I = 0 V (ISO7841F), V_I = V_{CCI}(1) (ISO7841)	I_{CC1}		1.1	1.7	mA
			I_{CC2}		0.8	1.2	
		EN1 = EN2 = 0 V, V_I = V_{CCI}(1) (ISO7841F), V_I = 0 V (ISO7841)	I_{CC1}		4.5	6.5	mA
			I_{CC2}		1.9	2.8	
	DC signal	V_I = 0 V (ISO7841F), V_I = V_{CCI}(1) (ISO7841)	I_{CC1}		1.6	2.3	mA
			I_{CC2}		2.2	3.1	
		V_I = V_{CCI}(1) (ISO7841F), V_I = 0 V (ISO7841)	I_{CC1}		5.1	7.2	mA
			I_{CC2}		3.5	4.8	
	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		3.4	4.8	mA
			I_{CC2}		2.9	4	
		10 Mbps	I_{CC1}		3.7	5.1	mA
			I_{CC2}		3.7	4.8	
		100 Mbps	I_{CC1}		6.8	8.1	mA
			I_{CC2}		12	14.2	
ISO7841DWW AND ISO7841FDWW							
Supply current	Disable	EN1 = EN2 = 0 V, V_I = 0 V (ISO7841F), V_I = V_{CCI}(1) (ISO7841)	I_{CC1}		1.1	1.7	mA
			I_{CC2}		0.8	1.2	
		EN1 = EN2 = 0 V, V_I = V_{CCI}(1) (ISO7841F), V_I = 0 V (ISO7841)	I_{CC1}		4.5	6.5	mA
			I_{CC2}		1.9	2.8	
	DC signal	V_I = 0 V (ISO7841F), V_I = V_{CCI}(1) (ISO7841)	I_{CC1}		1.6	2.4	mA
			I_{CC2}		2.2	3.3	
		V_I = V_{CCI}(1) (ISO7841F), V_I = 0 V (ISO7841)	I_{CC1}		5.1	7.5	mA
			I_{CC2}		3.5	5.2	
	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		3.5	5	mA
			I_{CC2}		3	4.3	
		10 Mbps	I_{CC1}		3.8	5.3	mA
			I_{CC2}		3.8	5.2	
		100 Mbps	I_{CC1}		6.9	8.8	mA
			I_{CC2}		12.3	14.2	

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

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6.15 Switching Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 11	6	11	16	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.55	4.1	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			2.5	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.5	ns
t_r	Output signal rise time	See Figure 11		1.7	3.9	ns
t_f	Output signal fall time			1.9	3.9	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 12		12	20	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			12	20	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO7841			10	20	ns
	Enable propagation delay, high impedance-to-high output for ISO7841F			2	2.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO7841			2	2.5	µs
	Enable propagation delay, high impedance-to-low output for ISO7841F			10	20	ns
t_{fs}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 13		0.2	9	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.90		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.16 Switching Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 11	6	10.8	16	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.7	4.2	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			2.2	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.5	ns
t_r	Output signal rise time	See Figure 11		0.8	3	ns
t_f	Output signal fall time			0.8	3	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 12		17	32	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			17	32	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO7841			17	32	ns
	Enable propagation delay, high impedance-to-high output for ISO7841F			2	2.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO7841			2	2.5	µs
	Enable propagation delay, high impedance-to-low output for ISO7841F			17	32	ns
t_{fs}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 13		0.2	9	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.91		ns

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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6.17 Switching Characteristics—2.5-V Supply

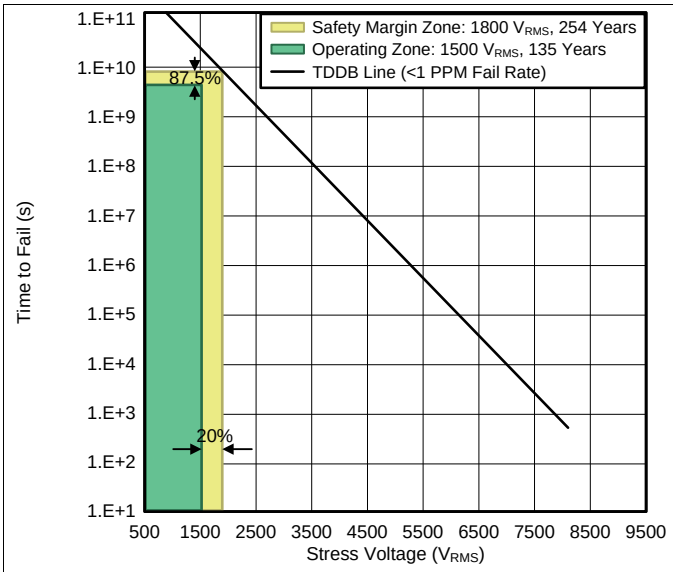
V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 11	7.5	11.7	17.5	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.66	4.2	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction Channels			2.2	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.5	ns
t_r	Output signal rise time	See Figure 11		1	3.5	ns
t_f	Output signal fall time			1.2	3.5	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 12		22	45	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			22	45	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO7841			18	45	ns
	Enable propagation delay, high impedance-to-high output for ISO7841F			2	2.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO7841			2	2.5	µs
	Enable propagation delay, high impedance-to-low output for ISO7841F			18	45	ns
t_{fs}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 13		0.2	9	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.91		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

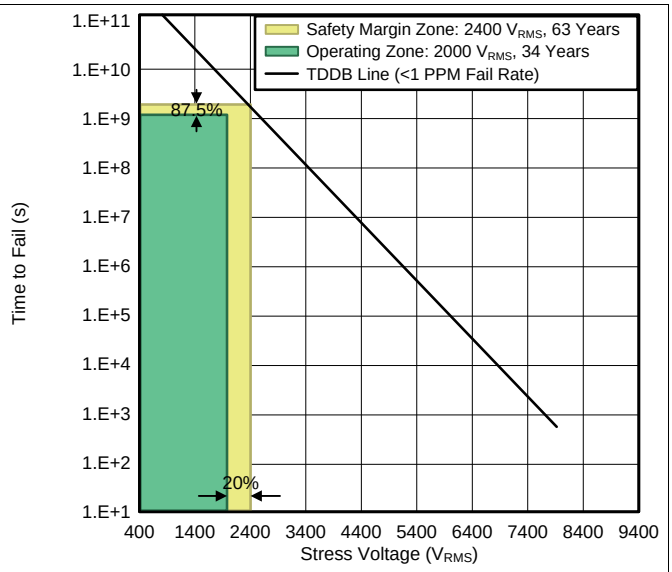
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6.18 Insulation Characteristics Curves



T_A upto 150°C
Operating lifetime = 135 years
Stress-voltage frequency = 60 Hz
Isolation working voltage = 1500 V_{RMS}

Figure 1. Reinforced Isolation Capacitor Life Time Projection for Devices in DW Package



T_A upto 150°C
Operating lifetime = 34 years
Stress-voltage frequency = 60 Hz
Isolation working voltage = 2000 V_{RMS}

Figure 2. Reinforced Isolation Capacitor Life Time Projection for Devices in DWW Package

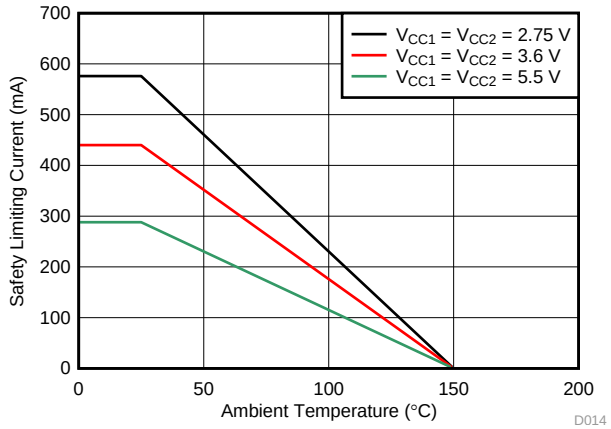


Figure 3. Thermal Derating Curve for Limiting Current per VDE

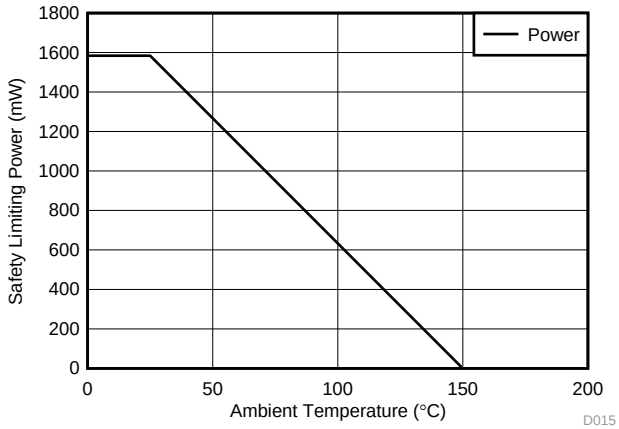
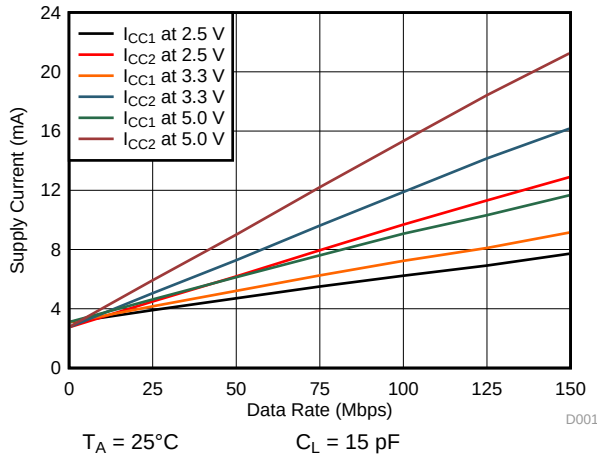


Figure 4. Thermal Derating Curve for Limiting Power per VDE

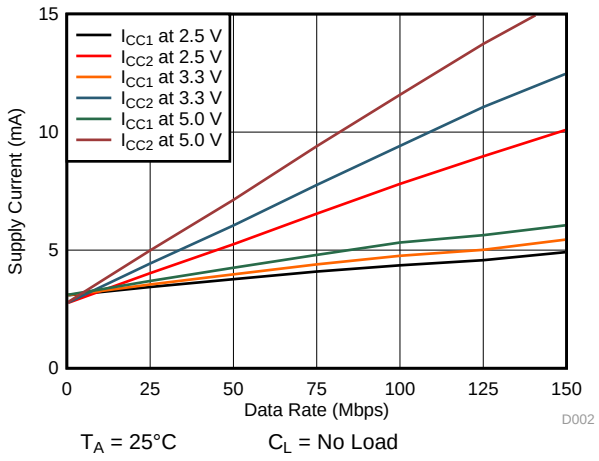
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6.19 Typical Characteristics



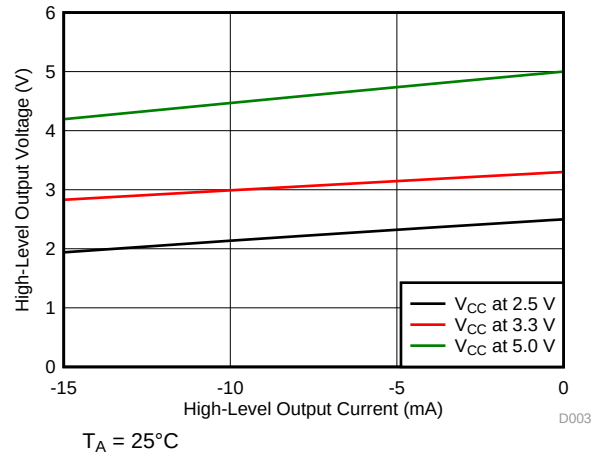
T_A = 25°C C_L = 15 pF

Figure 5. Supply Current vs Data Rate (With 15-pF Load)



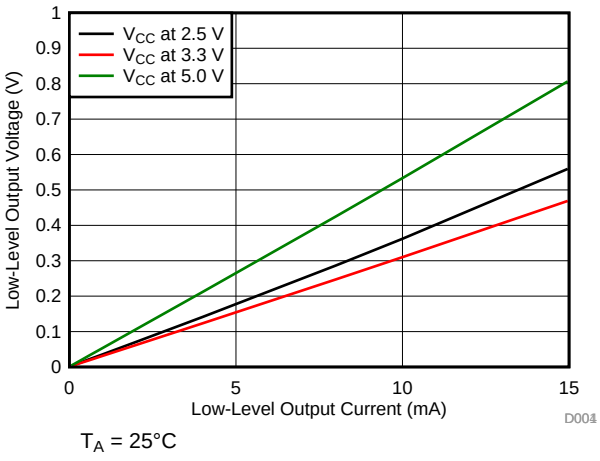
T_A = 25°C C_L = No Load

Figure 6. Supply Current vs Data Rate (With No Load)



T_A = 25°C

Figure 7. High-Level Output Voltage vs High-level Output Current



T_A = 25°C

Figure 8. Low-Level Output Voltage vs Low-Level Output Current

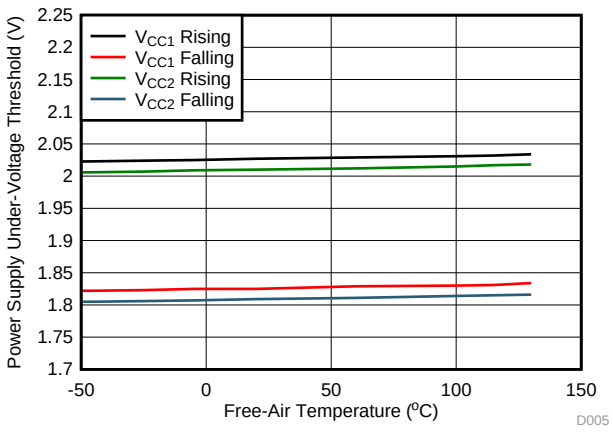


Figure 9. Power Supply Undervoltage Threshold vs Free-Air Temperature

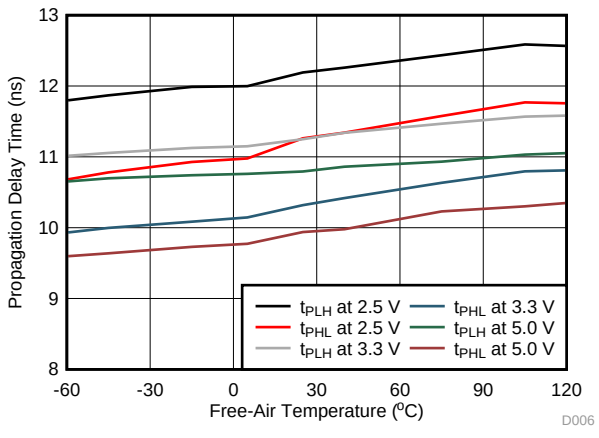
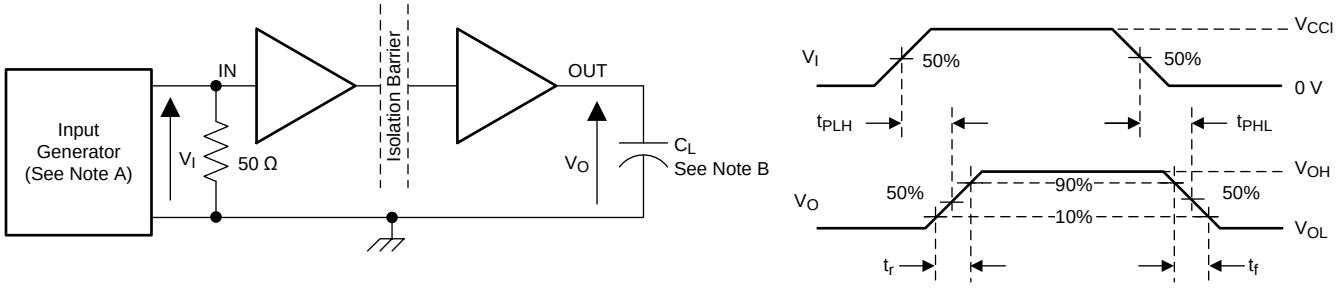


Figure 10. Propagation Delay Time vs Free-Air Temperature

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7 Parameter Measurement Information

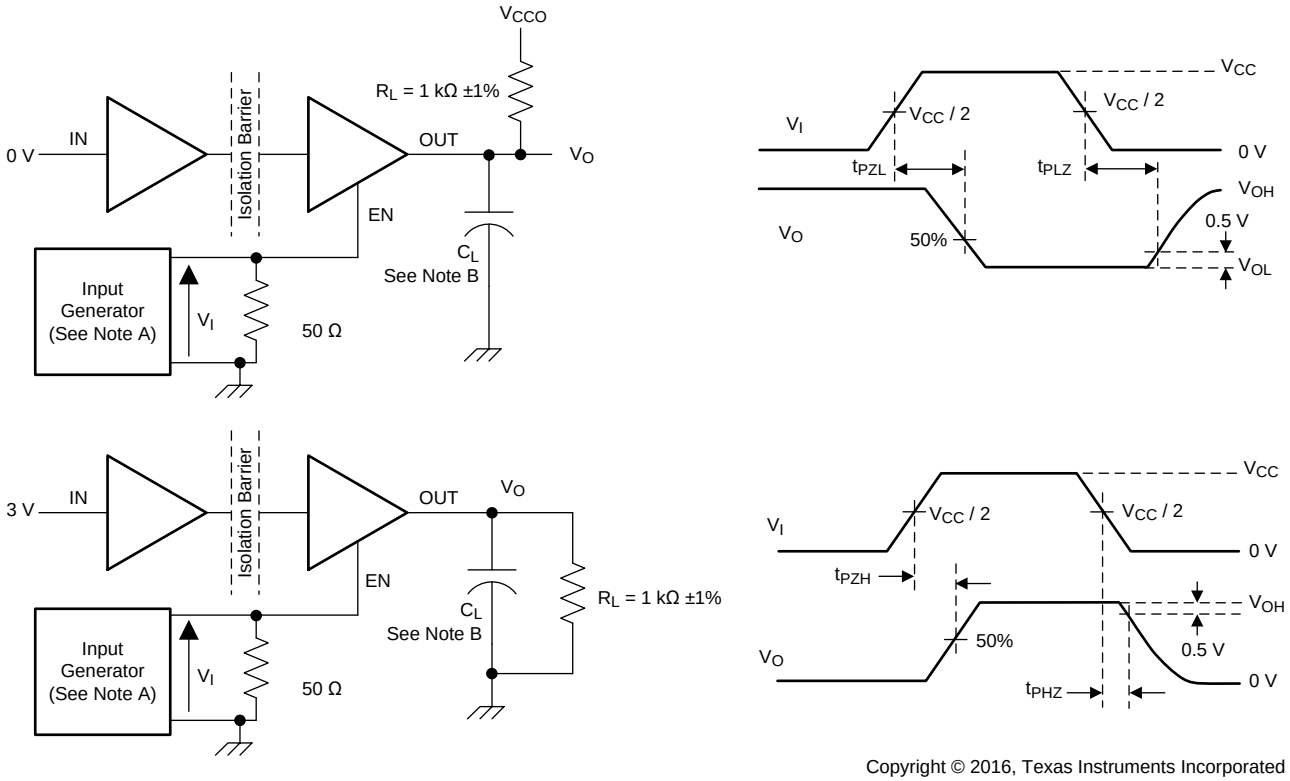


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A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 11. Switching Characteristics Test Circuit and Voltage Waveforms



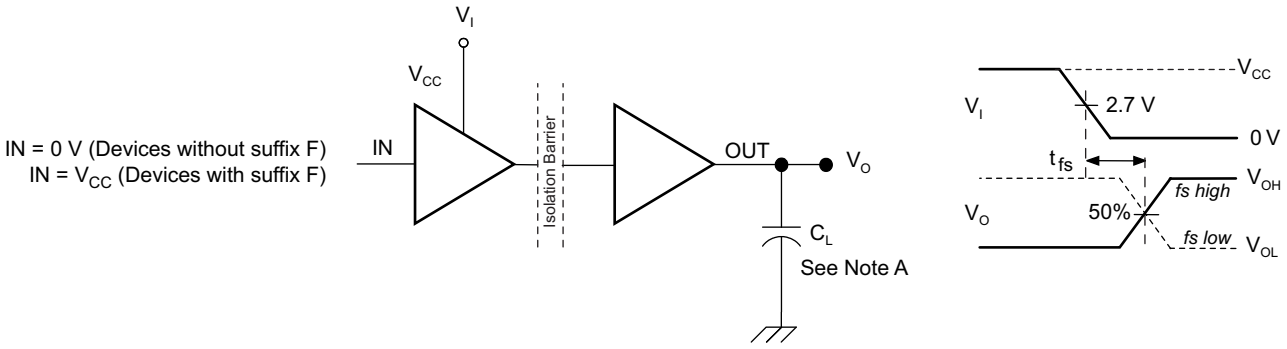
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A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 12. Enable/Disable Propagation Delay Time Test Circuit and Waveform

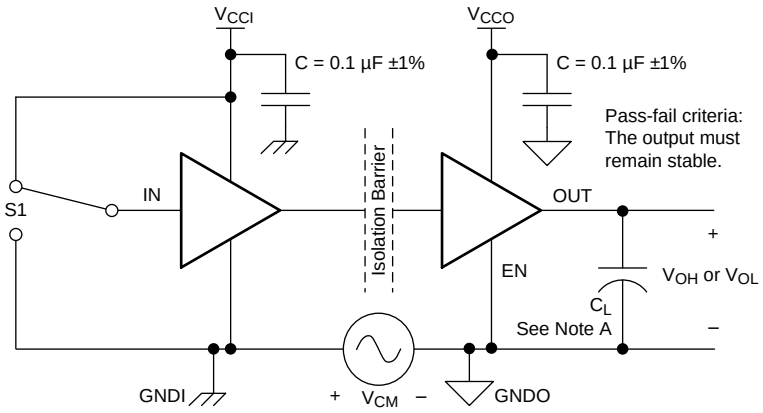
Parameter Measurement Information (continued)



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A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 13. Default Output Delay Time Test Circuit and Voltage Waveforms



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A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 14. Common-Mode Transient Immunity Test Circuit

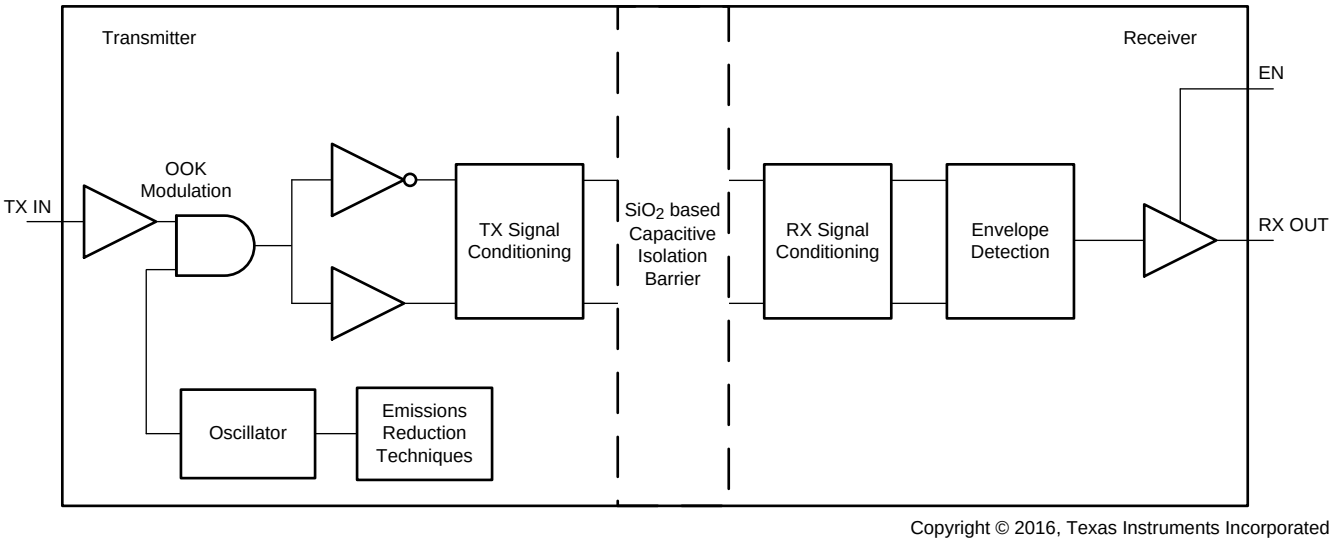
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8 Detailed Description

8.1 Overview

The ISO7841 device uses an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon-dioxide based isolation barrier. The transmitter sends a high-frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. If the EN pin is low then the output goes to high impedance. The ISO7841 device also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions because of the high-frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 15, shows a functional block diagram of a typical channel.

8.2 Functional Block Diagram



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Figure 15. Conceptual Block Diagram of a Digital Capacitive Isolator

Figure 16 shows a conceptual detail of how the ON-OFF keying scheme works.

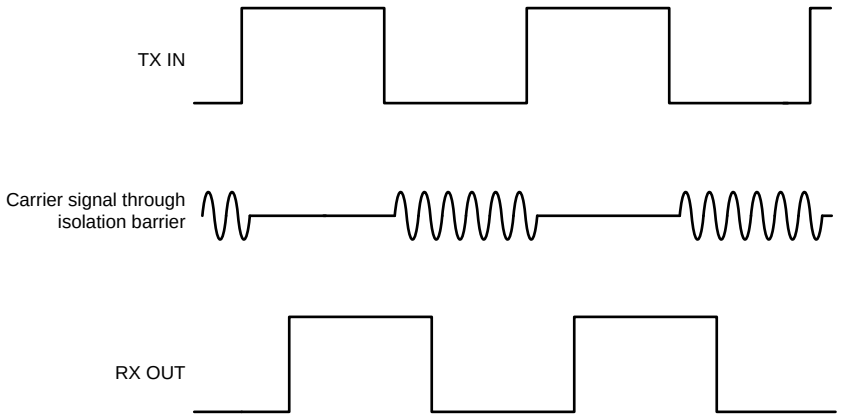


Figure 16. On-Off Keying (OOK) Based Modulation Scheme

8.3 Feature Description

Table 1 lists the device features.

Table 1. Device Features

PART NUMBER	CHANNEL DIRECTION	RATED ISOLATION	MAXIMUM DATA RATE	DEFAULT OUTPUT
ISO7841	3 Forward, 1 Reverse	5700 V_{RMS} / 8000 V_{PK} (1)	100 Mbps	High
ISO7841F	3 Forward, 1 Reverse	5700 V_{RMS} / 8000 V_{PK} (1)	100 Mbps	Low

(1) See for detailed isolation ratings.

8.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge, and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO7841 device incorporates many chip-level design improvements for overall system robustness. Some of these improvements include

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

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8.4 Device Functional Modes

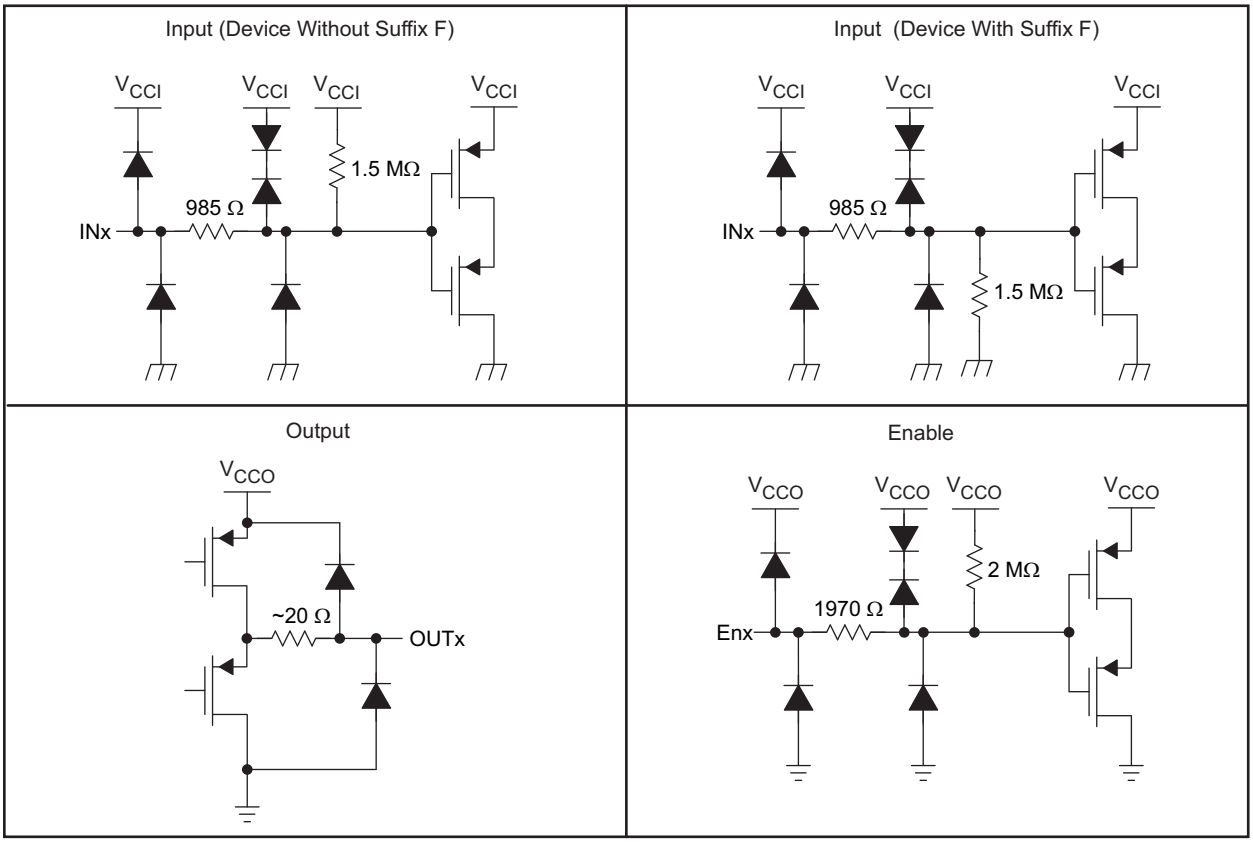
Table 2 lists the ISO7841 functional modes.

Table 2. Function Table(1)

V_{CCI}	V_{CCO}	INPUT (INx)(2)	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H or open	H	Normal Operation: A channel output assumes the logic state of its input.
		L	H or open	L	
		Open	H or open	Default	Default mode: When INx is open, the corresponding channel output goes to its default logic state. Default= High for ISO7841 and Low for ISO7841F.
X	PU	X	L	Z	A low value of Output Enable causes the outputs to be high-impedance
PD	PU	X	H or open	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default= High for IISO7841 and Low for ISO7841F. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of its input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined (3). When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of its input

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up (V_{CC} ≥ 2.25 V); PD = Powered down (V_{CC} ≤ 1.7 V); X = Irrelevant; H = High level; L = Low level ; Z = High Impedance
(2) A strongly driven input signal can weakly power the floating V_{CC} through an internal protection diode and cause undetermined output.
(3) The outputs are in undetermined state when 1.7 V < V_{CCI}, V_{CCO} < 2.25 V.

8.4.1 Device I/O Schematics



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Figure 17. Device I/O Schematics

9 Application and Implementation

NOTE

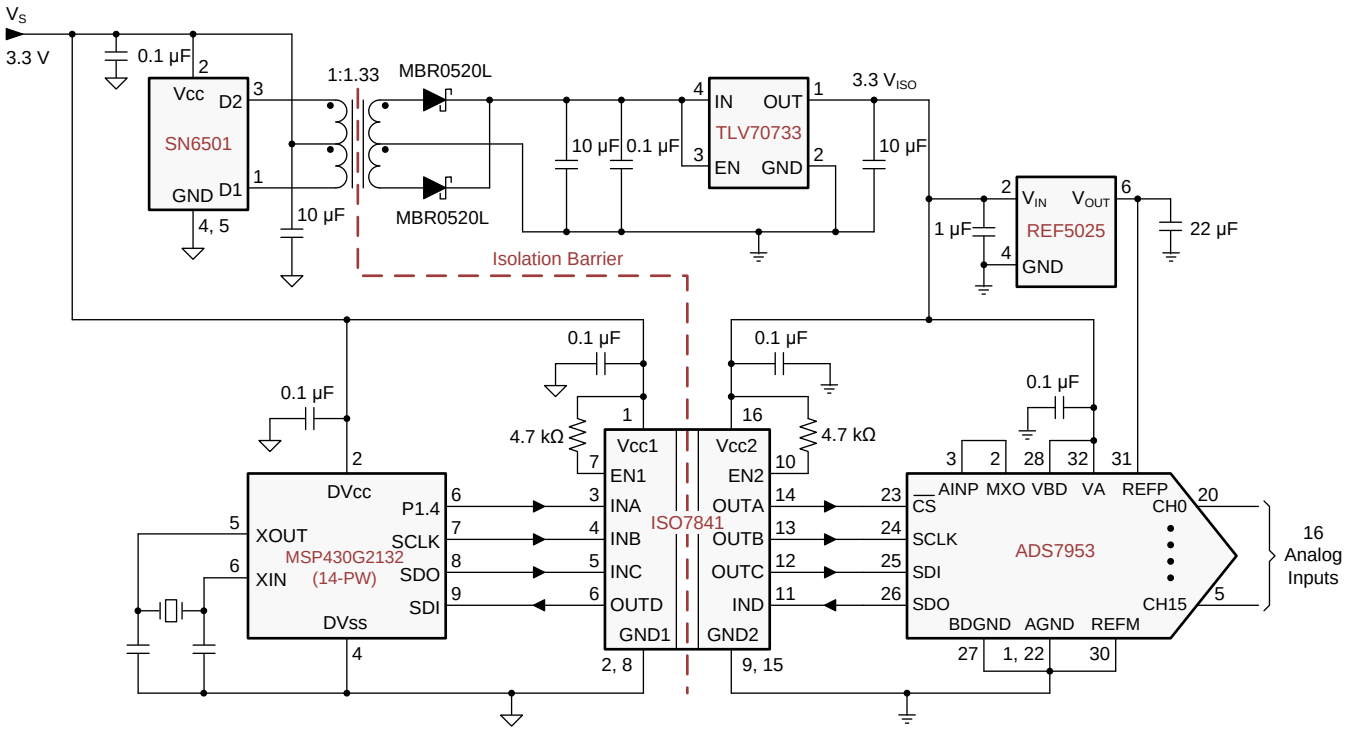
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO7841 device is a high-performance, quad-channel digital isolator with a 5.7-kV_{RMS} isolation voltage per UL 1577. The device comes with enable pins on each side that can be used to put the respective outputs in high impedance for multi-master driving applications and reduce power consumption. The ISO7841 device uses single-ended CMOS-logic switching technology. The supply voltage range is from 2.25 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, μC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

Figure 18 shows the isolated SPI.



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Figure 18. Isolated SPI for an Analog Input Module With 16 Input

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Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the parameters shown in Table 3.

Table 3. Design Parameters

PARAMETER	VALUE
Supply voltage	2.25 to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 µF
Decoupling capacitor from V_{CC2} and GND2	0.1 µF

9.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO7841 device only requires two external bypass capacitors to operate.

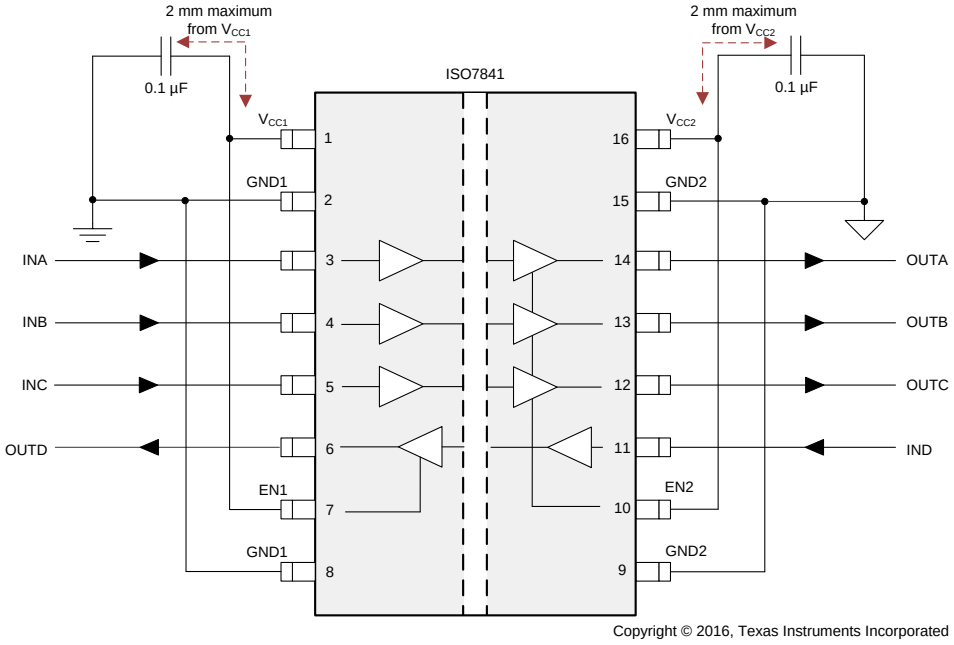


Figure 19. Typical ISO7841 Circuit Hook-Up

9.2.3 Application Curve

The typical eye diagram of the ISO7841 device indicates low jitter and wide open eye at the maximum data rate of 100 Mbps.

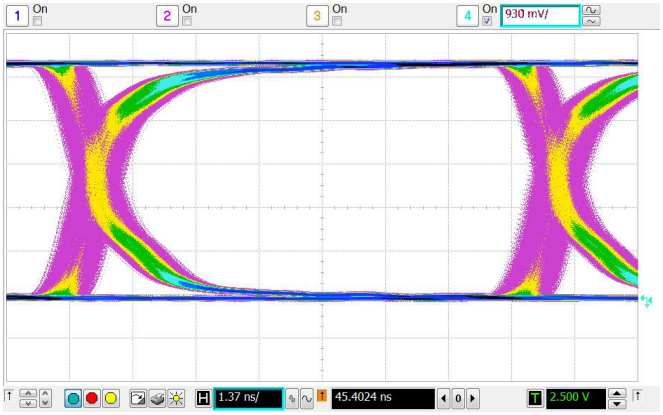


Figure 20. Eye Diagram at 100 Mbps PRBS, 5 V and 25°C

10 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1-μF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas InstrumentsSN6501. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 Transformer Driver for Isolated Power Supplies.

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11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 21). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/inch^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to *Digital Isolator Design Guide*.

11.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

11.2 Layout Example

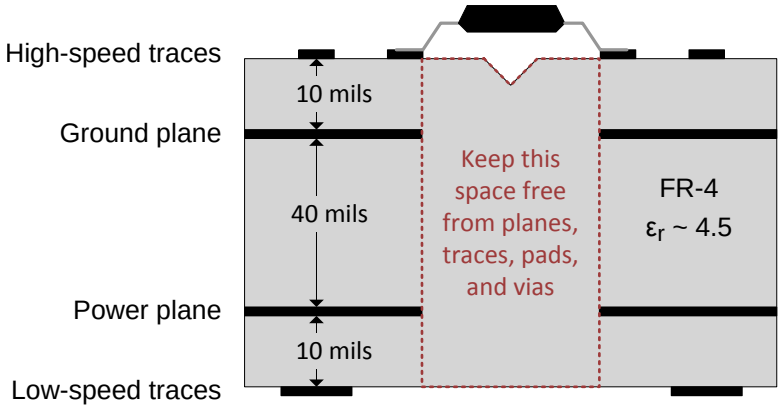


Figure 21. Layout Example Schematic

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

相关文档如下：

- *《ADS79xx- 8 位、10 位和 12 位，1MSPS，4 通道、8 通道、12 通道和 16 通道，单端，微功耗，串行接口 ADC》*
- *数字隔离器设计指南*
- *隔离相关术语*
- *《MSP430G2x32、MSP430G2x02 混合信号微控制器》*
- *《REF50xx 低噪声、极低漂移、高精度电压基准》*
- *《SN6501 用于隔离电源的变压器驱动器》*
- *《用于便携式设备的 TLV707、TLV707P 200mA、低 IQ、低噪声、低压降稳压器》*

12.2 相关链接

以下表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **4.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持与社区
ISO7841	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ISO7841F	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 静电放电警告



这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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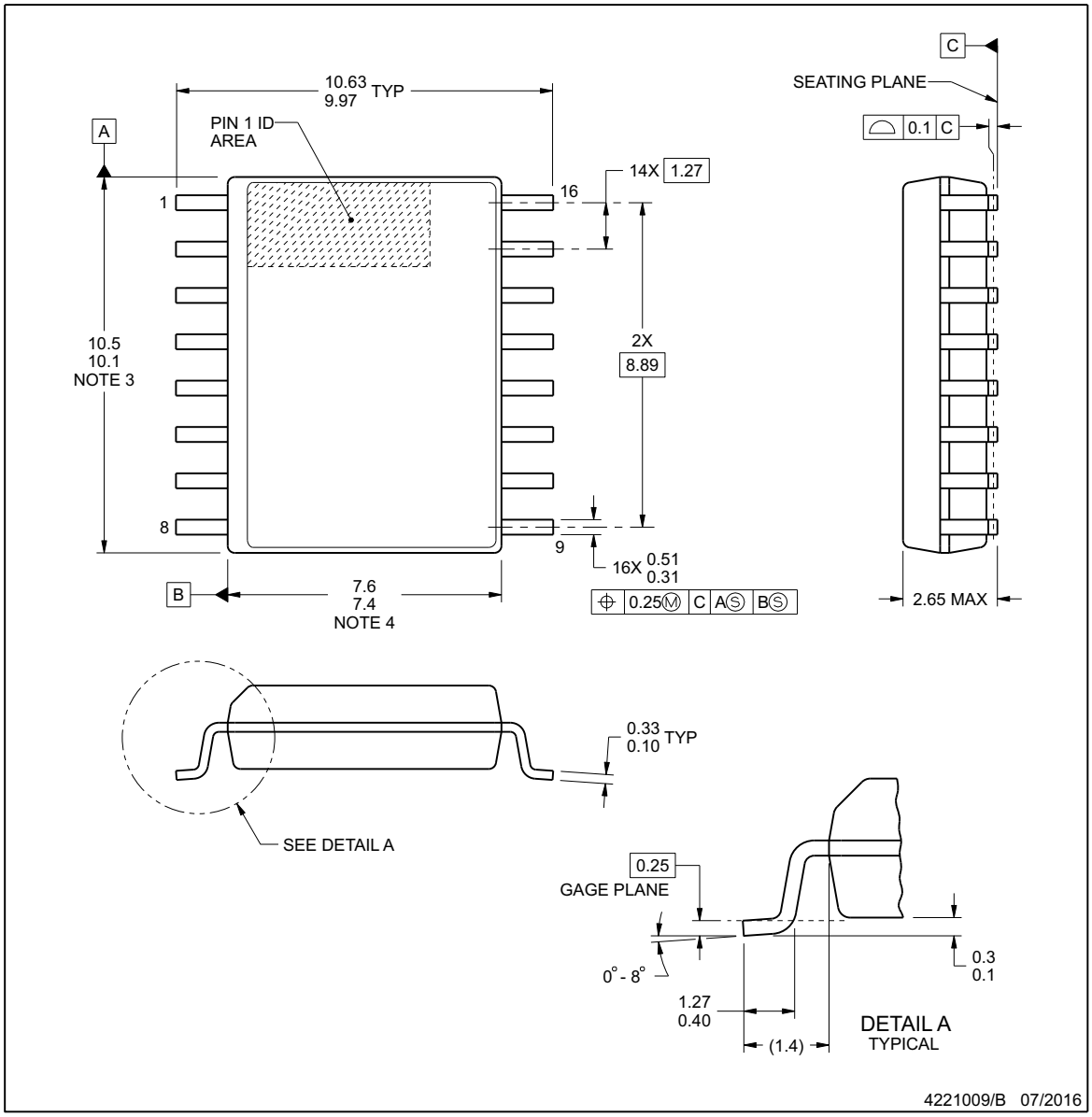


PACKAGE OUTLINE

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES:

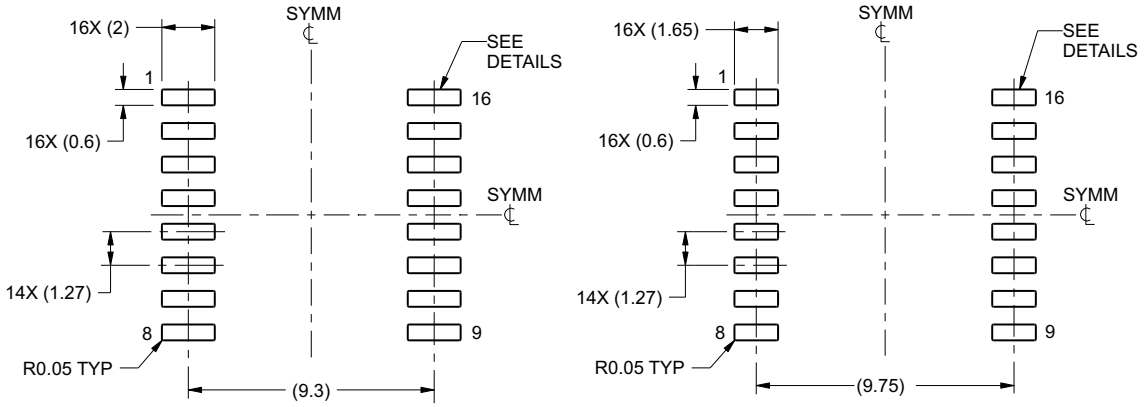
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

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EXAMPLE BOARD LAYOUT

DW0016B — **SOIC - 2.65 mm max height**

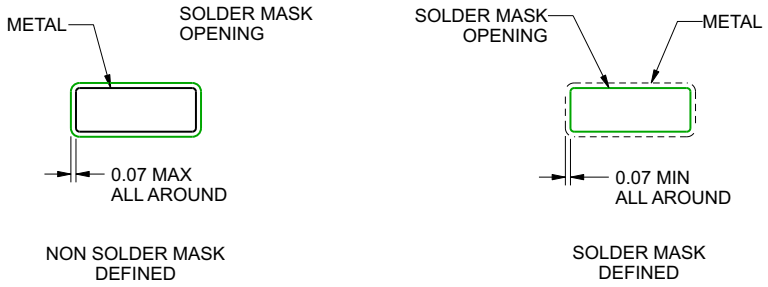
SOIC



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

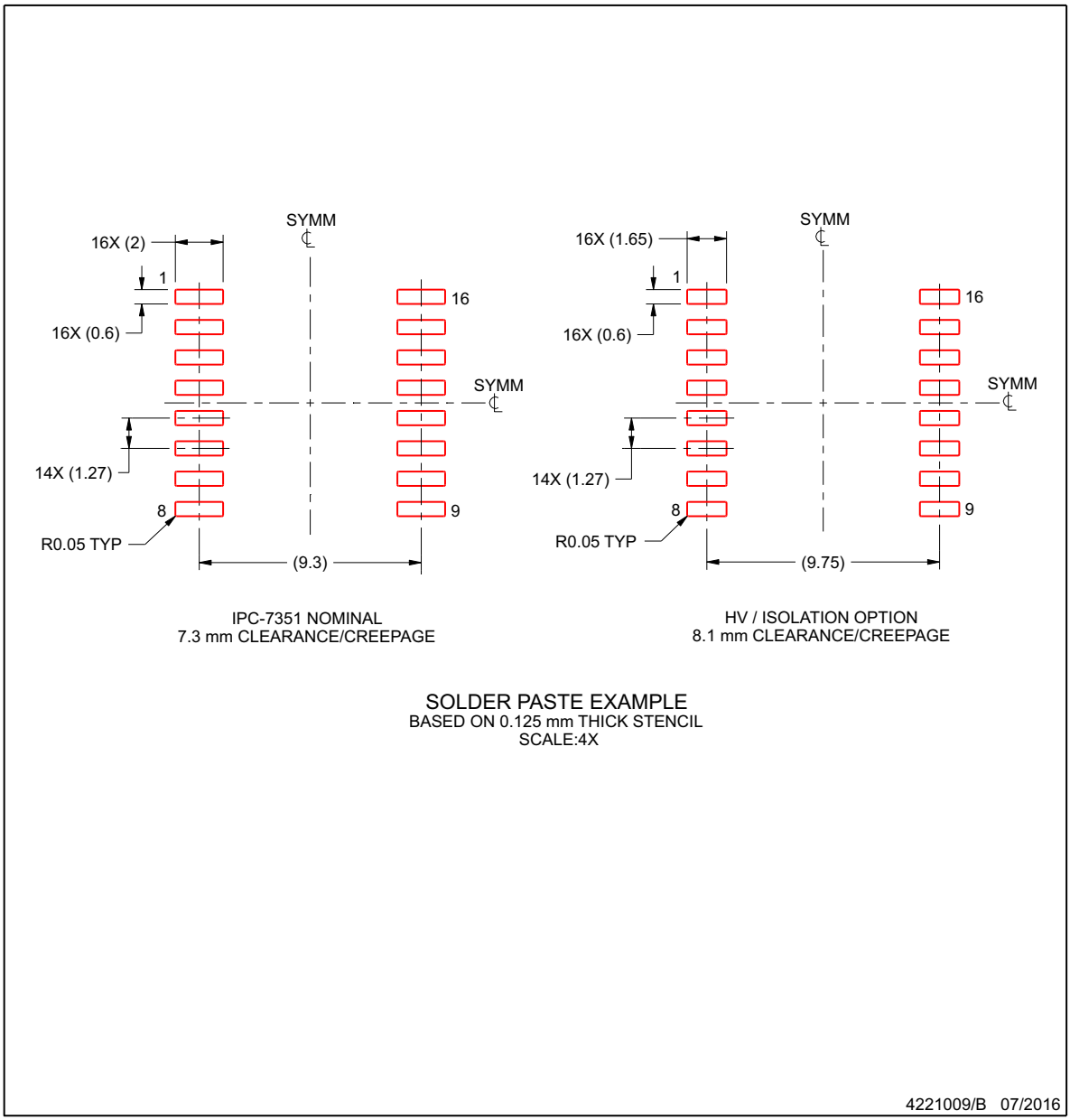
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EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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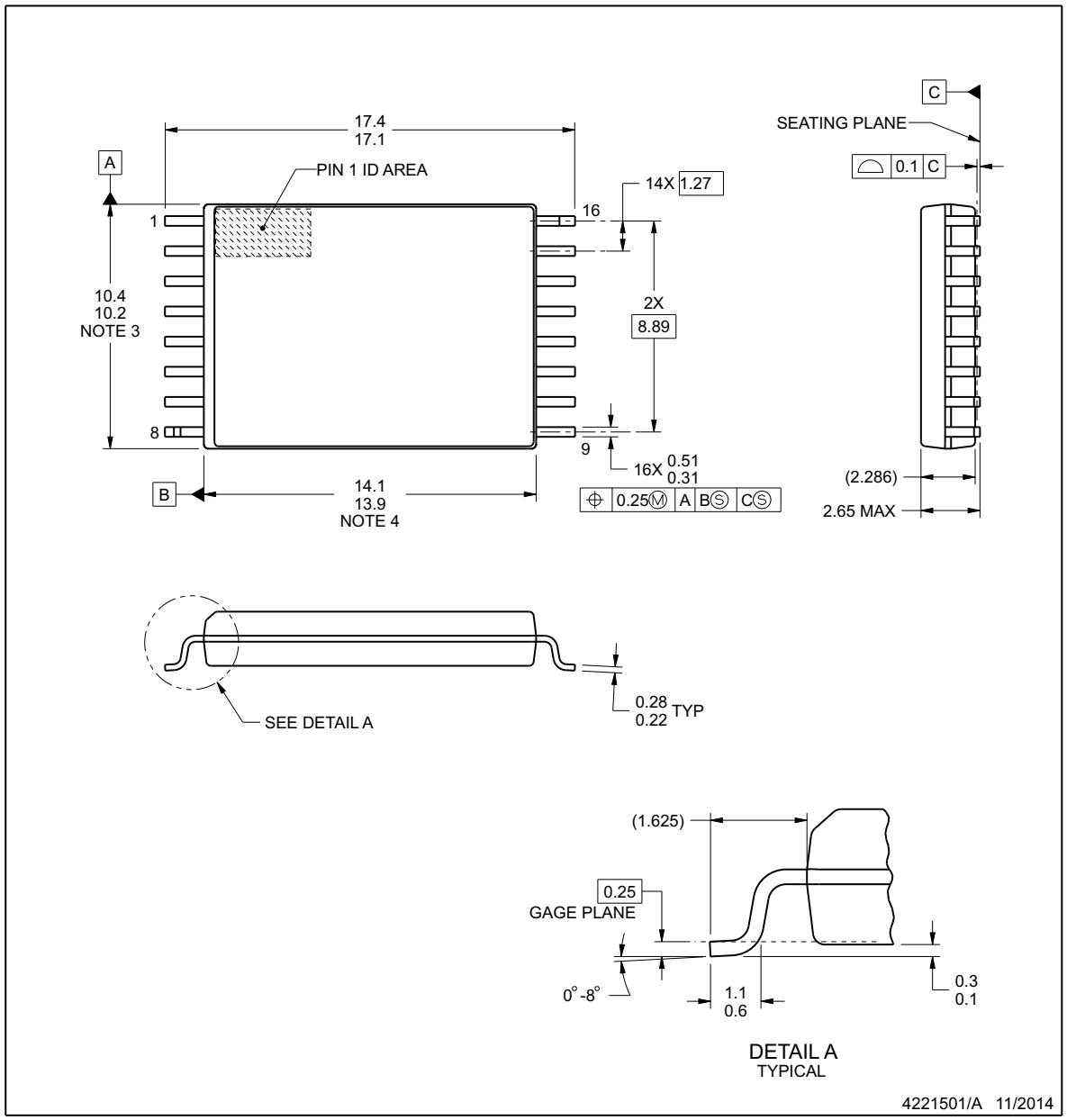


PACKAGE OUTLINE

DWW0016A

SOIC - 2.65 mm max height

PLASTIC SMALL OUTLINE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 mm per side.
4. This dimension does not include interlead flash.

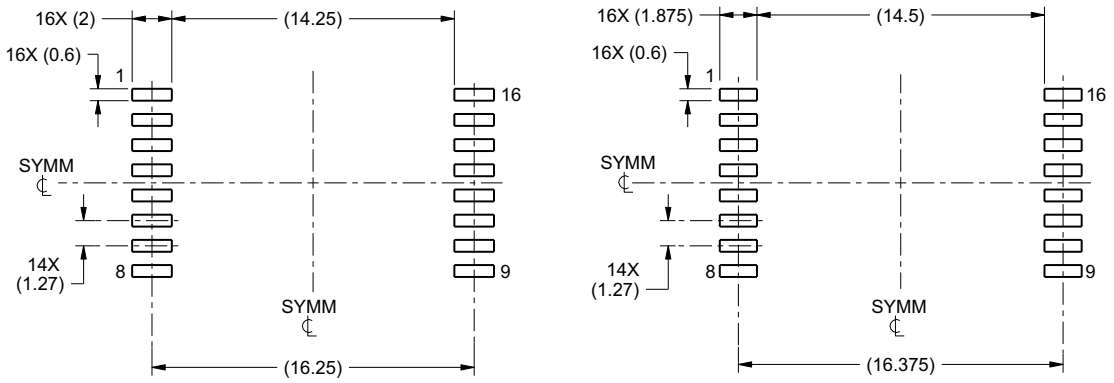
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EXAMPLE BOARD LAYOUT

DWW0016A

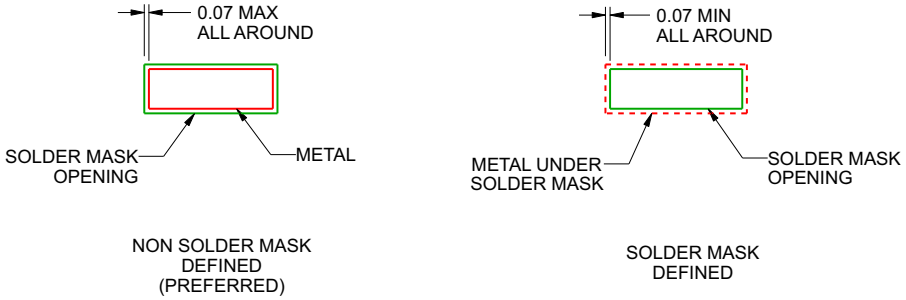
SOIC - 2.65 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
STANDARD
SCALE:3X

LAND PATTERN EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
SCALE:3X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4221501/A 11/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

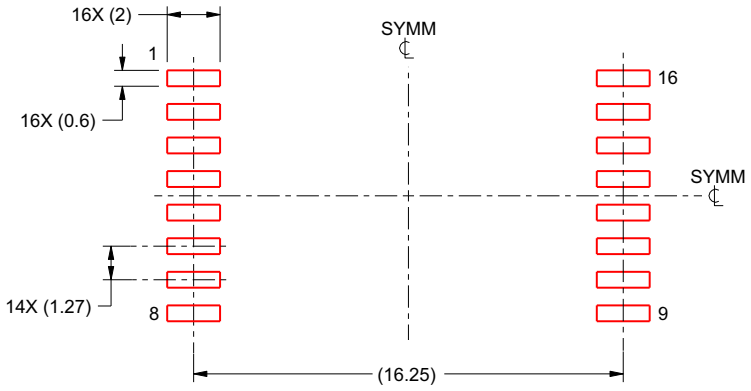
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EXAMPLE STENCIL DESIGN

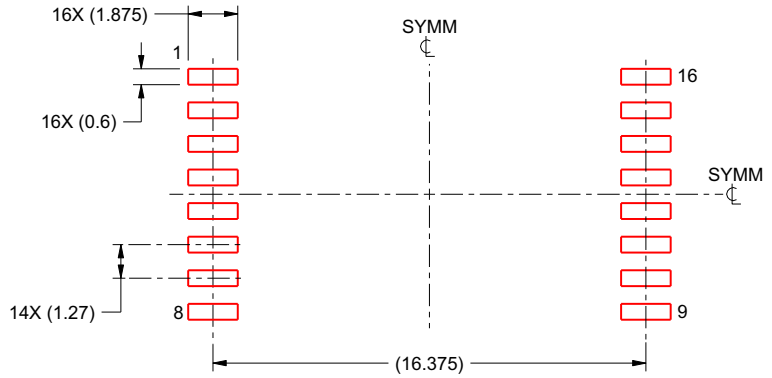
DWW0016A

SOIC - 2.65 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
STANDARD
BASED ON 0.125 mm THICK STENCIL
SCALE:4X



SOLDER PASTE EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221501/A 11/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7841DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7841	Samples
ISO7841DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7841	Samples
ISO7841DWW	ACTIVE	SOIC	DWW	16	45	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7841	Samples
ISO7841DWWR	ACTIVE	SOIC	DWW	16	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7841	Samples
ISO7841FDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7841F	Samples
ISO7841FDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7841F	Samples
ISO7841FDWW	ACTIVE	SOIC	DWW	16	45	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7841F	Samples
ISO7841FDWWR	ACTIVE	SOIC	DWW	16	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7841F	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

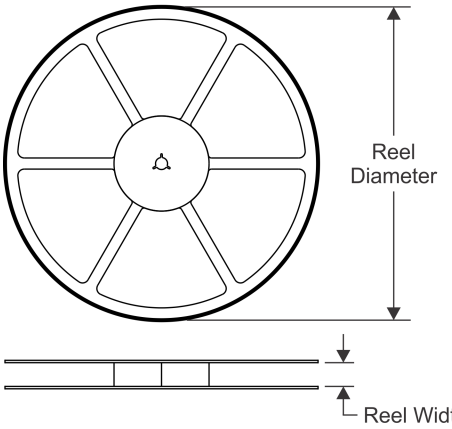
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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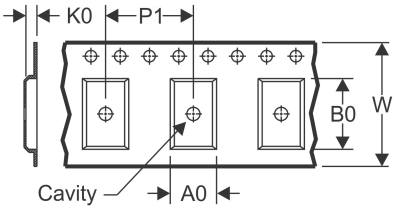
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

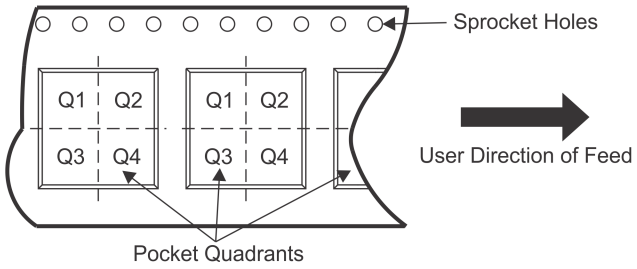


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

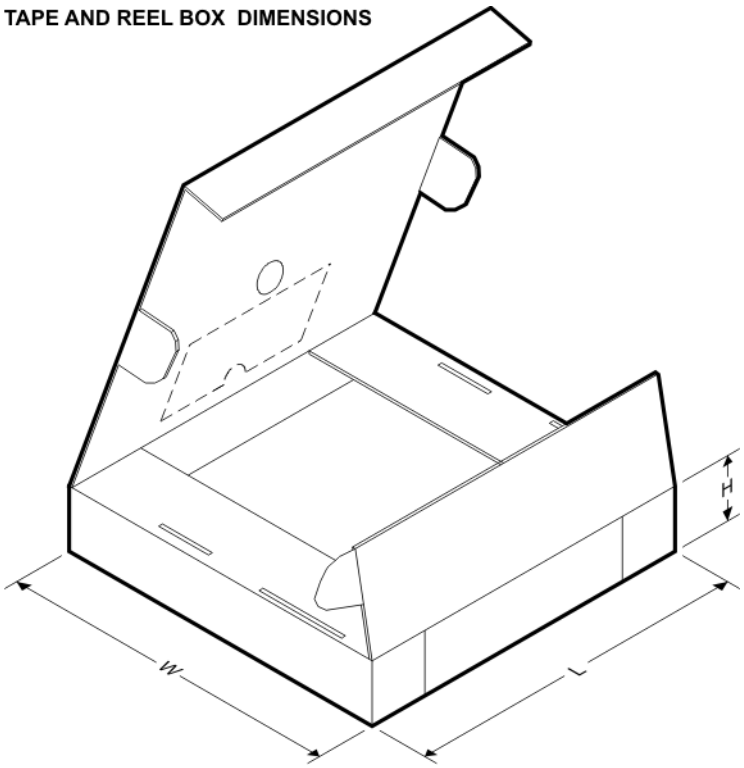
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7841DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7841DWWR	SOIC	DWW	16	1000	330.0	24.4	18.0	10.0	3.0	20.0	24.0	Q1
ISO7841FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7841FDWWR	SOIC	DWW	16	1000	330.0	24.4	18.0	10.0	3.0	20.0	24.0	Q1

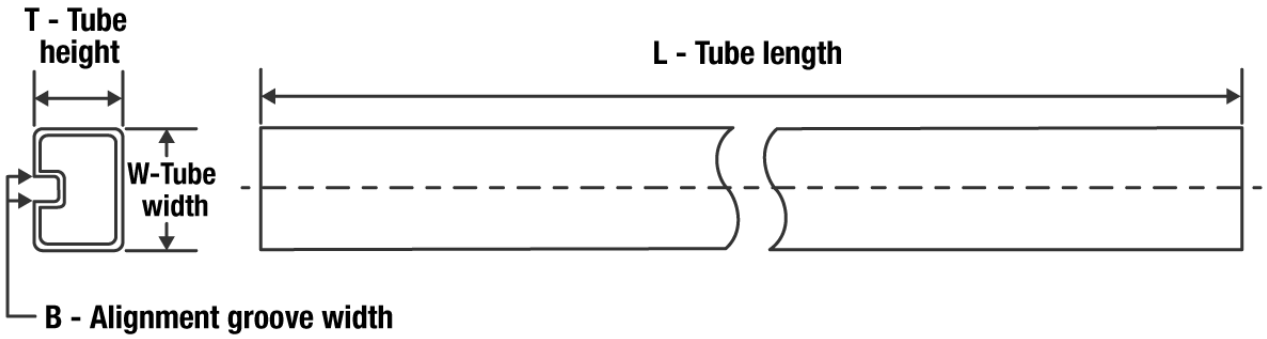
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7841DWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7841DWWR	SOIC	DWW	16	1000	350.0	350.0	43.0
ISO7841FDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7841FDWWR	SOIC	DWW	16	1000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO7841DW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7841DWW	DWW	SOIC	16	45	507	20	5000	9
ISO7841FDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7841FDWW	DWW	SOIC	16	45	507	20	5000	9

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