ISOW7841A-Q1 Automotive High-Performance, 5000-V_{RMS} Reinforced Quad-Channel Digital Isolator With Integrated High-Efficiency, Low-Emissions DC-DC Converter

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device temperature Grade 1: –40°C to 125°C Ambient Operating Temperature
- 100 Mbps data rate
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Robust isolation barrier:
  - >100-Year projected lifetime at 1 kV_{RMS} working voltage
  - Up to 5000 V_{RMS} isolation rating
  - Up to 10 kV_{PK} surge capability
  - ±100 kV/µs minimum CMTI
- Integrated high-efficiency DC-DC converter with on-chip transformer
- 3-V to 5.5-V Wide input supply range
- Regulated 5-V or 3.3-V output
- Up to 0.65-W output power
- 5 V to 5 V; 5 V to 3.3 V: Available load current ≥ 130 mA
- 3.3 V to 3.3 V: Available load current ≥ 75 mA ; 3.3 V to 5 V: Available load current ≥ 40 mA
- Soft-start to limit inrush current
- Overload and short-circuit protection
- Thermal shutdown
- Default output: *High* and *Low* options
- Low propagation delay: 13 ns Typ (5-V supply)
- Robust electromagnetic compatibility (EMC)
  - System-level ESD, EFT, and surge immunity
  - ±8 kV IEC 61000-4-2 contact discharge protection across isolation barrier
  - Low emissions
- 16-pin wide SOIC package
- Safety-related certifications:
  - 7071-V_{PK} reinforced isolation per DIN V VDE V 0884-11:2017-01
  - 5000-V_{RMS} isolation for 1 minute per UL 1577
  - CSA Certification per IEC 60950-1, IEC 62368-1 and IEC 60601-1 end equipment standards
  - CQC Approval per GB4943.1-2011
  - TUV Certification according to EN 60950-1 and EN 61010-1
  - All certifications are planned

2 Applications

- Battery Management System (BMS)
- On-Board Charger (OBC)
- Traction Inverter
- DC/DC Converter

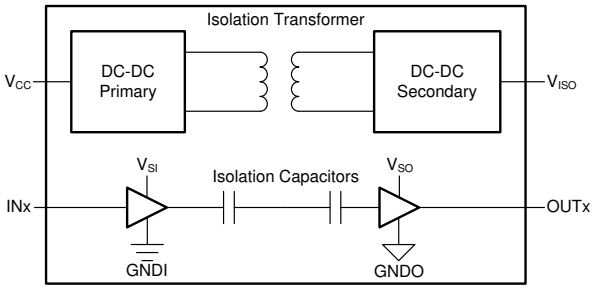
3 Description

The ISOW7841A-Q1 is an automotive qualified high-performance, quad-channel reinforced digital isolator with an integrated high-efficiency power converter. The low emissions integrated DC-DC converter provides up to 650 mW of isolated power at high efficiency and can be configured for various input and output voltage configurations. Therefore this device eliminates the need for a separate isolated power supply in space-constrained isolated designs.

Device Information 1

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISOW7841A-Q1	SOIC (16)	10.30 mm × 7.50 mm

1. For all available packages, see the orderable addendum at the end of the data sheet.



1. V_{CC} is the primary supply voltage referenced to GND1. V_{ISO} is the isolated supply voltage referenced to GND2.
2. V_{SI} and V_{SO} can be either V_{CC} or V_{ISO} depending on the channel direction
3. V_{SI} is the input-side supply voltage referenced to GNDI and V_{SO} is the output-side supply voltage referenced to GNDO.

Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2020) to Revision B (December 2020)	Page
• Added Function Saftey bullet to Features	1

Changes from Revision * (February 2020) to Revision A (June 2020)	Page
• Updated device status to Production Data	1
• Changed the maximum limit for output signal rise and fall times from 3 to 4 ns in the //Switching Characteristics—5-V Input, 3.3-V Output// table	13

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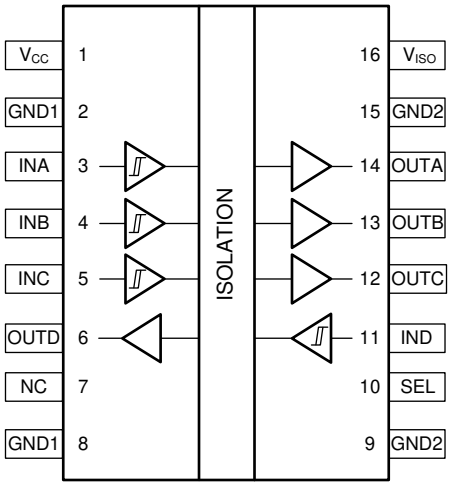
5 Description Continued

The ISOW7841A-Q1 device provides high electromagnetic immunity and low emissions while isolating CMOS or LVCMOS digital I/Os. The signal-isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide (SiO_2) insulation barrier, whereas, power isolation uses on-chip transformers separated by thin film polymer as insulating material. If the input signal is lost, the default output is high for the ISOW7841A-Q1 without the F suffix and low for the device with the F suffix.

These devices help prevent noise currents on data buses, such as CAN, or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. Through innovative chip design and layout techniques, electromagnetic compatibility of the device has been significantly enhanced to ease system-level ESD, EFT, surge and emissions compliance. The high-efficiency of the power converter allows operation at a higher ambient temperature. The device is available in a 16-pin SOIC wide-body (SOIC-WB) DWE package.

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6 Pin Configuration and Functions



ISOW7841A-Q1 DWE Package. 16-Pin SOIC-WB. Top View.

Table 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
	ISOW7841A-Q1		
GND1	2, 8	—	Ground connection for V_{CC}
GND2	9, 15	—	Ground connection for V_{ISO}
INA	3	I	Input channel A
INB	4	I	Input channel B
INC	5	I	Input channel C
IND	11	I	Input channel D
NC	7	—	Not connected
OUTA	14	O	Output channel A
OUTB	13	O	Output channel B
OUTC	12	O	Output channel C
OUTD	6	O	Output channel D
SEL	10	I	V_{ISO} selection pin. V_{ISO} = 5 V when SEL shorted to V_{ISO}. V_{ISO} = 3.3 V, when SEL shorted to GND2 or when left floating. For more information see *Section 9.4*.
V_{CC}	1	—	Supply voltage
V_{ISO}	16	—	Isolated supply voltage determined by SEL pin

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7 Specifications

7.1 Absolute Maximum Ratings

See (1) (2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.5	6	V
V_{ISO}	Isolated supply voltage	–0.5	6	V
V_{IO}	Voltage at INx, OUTx, SEL pins	–0.5	V_{CC} + 0.5, V_{ISO} + 0.5 (3)	V
I_O	Maximum output current through data channels	–15	15	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values except differential I/O bus voltages are with respect to the local ground pin (GND1 or GND2) and are peak voltage values.

(3) This value depends on whether the pin is located on the V_{CC} or V_{ISO} side. The maximum voltage at the I/O pins should not exceed 6 V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1) HBM ESD Classification Level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1000	
		Contact discharge per IEC 61000-4-2 (2) Isolation barrier withstand test	±8000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

(2) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.

7.3 Recommended Operating Conditions

See 1

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		5.5	V
I_{OH}	High level output current 2	V_{SO} = 5 V	–4			mA
		V_{SO} = 3.3 V	–2			
I_{OL}	Low level output current 2	V_{SO} = 5 V			4	mA
		V_{SO} = 3.3 V			2	
V_{IH}	High-level input voltage		0.7 × V_{SI}		V_{SI}	V
V_{IL}	Low-level input voltage		0		0.3 × V_{SI}	V
DR	Data rate				100	Mbps
T_A	Ambient temperature		–40		125	°C

1. V_{SI} is the input side supply, V_{SO} is the output side supply
2. This current is for data output channel.

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7.4 Thermal Information

THERMAL METRIC[1]		ISOW7841A-Q1 DWE (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	56.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	28.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	V_{CC} = 5.5 V, I_{ISO} = 110 mA, T_J = 150°C, T_A ≤ 80°C, C_L = 15 pF, input a 50-MHz 50% duty-cycle square wave			1.02	W
P_{D1}	Maximum power dissipation (side-1)				0.51	W
P_{D2}	Maximum power dissipation (side-2)				0.51	W

7.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	>8	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance – capacitive signal isolation)	> 21	µm
		Minimum internal gap (internal clearance – transformer power isolation)	>120	
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN V VDE 0884-11:2017-01[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test ; See Figure 10-5	1000	V_{RMS}
		DC voltage	1414	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}; t = 60 s (qualification); V_{TEST} = 1.2 × V_{IOTM}; t = 1 s (100% production)	7071	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	Test method per IEC 62368-1, 1.2/50 µs waveform, V_{TEST} = 1.6 × V_{IOSM} = 10000 V_{PK}(qualification)	6250	V_{PK}

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PARAMETER		TEST CONDITIONS	VALUE	UNIT
q_{pd}	Apparent charge(4)	Method a, after input/output safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), V_{ini} = 1.2 × V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 × V_{IORM}, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~3.5	pF
R_{IO}	Insulation resistance(5)	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V, T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
$V_{ISO(UL)}$	Withstand isolation voltage	V_{TEST} = $V_{ISO(UL)}$= 5000 V_{RMS}, t = 60 s (qualification), V_{TEST} = 1.2 × $V_{ISO(UL)}$ = 6000 V_{RMS}, t = 1 s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.

(2) This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.

(4) Apparent charge is electrical discharge caused by a partial discharge (pd).

(5) All pins on each side of the barrier tied together creating a two-terminal device.

7.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Plan to certify according to DIN V VDE V 0884-11:2017-01	Plan to certify according to IEC 60950-1, IEC 62368-1, and IEC 60601-1	Plan to certify under UL 1577 Component Recognition Program	Plan to certify according to GB 4943.1-2011	Plan to certify according to EN 61010-1:2010 and EN 60950- 1:2006/A2:2013
Reinforced insulation; Maximum transient isolation voltage, 7071 V_{PK}; Maximum repetitive peak isolation voltage, 1414 V_{PK}; Maximum surge isolation voltage, 6250 V_{PK}	Reinforced insulation per CSA 60950-1-07+A1+A2, IEC 60950-1 2nd Ed.+A1+A2, CSA 62368-1-14 and IEC 62368-1 2nd Ed., 800 V_{RMS} maximum working voltage (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3+A1, 250 V_{RMS} maximum working voltage; Temperature rating is 90°C for reinforced insulation and 125°C for basic insulation; see certificate for details.	Single protection, 5000 V_{RMS}	Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V_{RMS} maximum working voltage;	5000 V_{RMS} Reinforced insulation per EN 61010-1:2010 up to working voltage of 600 V_{RMS}; 5000 V_{RMS} Reinforced insulation per EN 60950-1:2006/A2:2013 up to working voltage of 800 V_{RMS}
Certification planned	Certification planned	Certification planned	Certification planned	Certification planned

7.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current(1)	$R_{\theta JA}$ = 56.8°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see Thermal Derating Curve for Safety Limiting Current per VDE			400	mA
		$R_{\theta JA}$ = 56.8°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see Thermal Derating Curve for Safety Limiting Current per VDE			611	
P_S	Safety input, output, or total power(1)	$R_{\theta JA}$ = 56.8°C/W, T_J = 150°C, T_A = 25°C, see Thermal Derating Curve for Safety Limiting Power per VDE			2200	mW
T_S	Maximum safety temperature(1)				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use the following equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

7.9 Electrical Characteristics—5-V Input, 5-V Output

V_{CC} = 5 V ±10%, SEL shorted to V_{ISO} (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ISO}	Isolated supply voltage	External I_{ISO} = 0 to 50 mA	4.75	5.07	5.43	V
		External I_{ISO} = 0 to 130 mA	4.5	5.07	5.43	
$V_{ISO(LINE)}$	DC line regulation	I_{ISO} = 50 mA, V_{CC} = 4.5 V to 5.5 V		2		mV/V
$V_{ISO(LOAD)}$	DC load regulation	I_{ISO} = 0 to 130 mA		1%		
EFF	Efficiency at maximum load current	I_{ISO} = 130 mA, C_{LOAD} = 0.1 µF || 10 µF; V_I = V_{SI} (ISOW7841A-Q1); V_I =0 V (ISOW7841A-Q1 with F suffix)		53%		
$V_{CC+(UVLO)}$	Positive-going UVLO threshold on V_{CC}, V_{ISO}				2.7	V
$V_{CC-(UVLO)}$	Negative-going UVLO threshold on V_{CC}, V_{ISO}		2.1			V
$V_{HYS\ (UVLO)}$	UVLO threshold hysteresis on V_{CC}, V_{ISO}			0.2		V
V_{ITH}	Input pin rising threshold				0.7	V_{SI}
V_{ITL}	Input pin falling threshold		0.3			V_{SI}
$V_{I(HYS)}$	Input pin threshold hysteresis (INx)		0.1			V_{SI}
I_{IL}	Low level input current	V_{IL} = 0 at INx or SEL	–10			µA
I_{IH}	High level input current	V_{IH} = V_{SI}>(1) at INx or SEL			10	µA
V_{OH}	High level output voltage	I_O = –4 mA, see Figure 8-1	V_{SO} (1) – 0.4	V_{SO} – 0.2		V
V_{OL}	Low level output voltage	I_O = 4 mA, see Figure 8-1		0.2	0.4	V
CMTI	Common mode transient immunity	V_I = V_{SI} or 0 V, V_{CM} = 1000 V; see Figure 8-2	100			kV/us
I_{CC_SC}	DC current from supply under short circuit on V_{ISO}	V_{ISO} shorted to GND2		137		mA
$V_{ISO(RIP)}$	Output ripple on isolated supply (pk-pk)	20-MHz bandwidth, C_{LOAD} = 0.1 µF || 20 µF, I_{ISO} = 130 mA		100		mV

(1) V_{SI} = input side supply; V_{SO} = output side supply

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7.10 Supply Current Characteristics—5-V Input, 5-V Output

V_{CC} = 5 V ±10%, SEL shorted to V_{ISO} (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (ISOW7841A-Q1); V_I = V_{SI} (1) (ISOW7841A-Q1 with F suffix)		23		mA
		No external I_{LOAD}; V_I = V_{SI} (ISOW7841A-Q1); V_I = 0V (ISOW7841A-Q1 with F suffix)		17		
		All channels switching with square wave clock input of 1 Mbps; C_L = 15 pF, No external I_{LOAD}		20		
		All channels switching with square wave clock input of 10 Mbps; C_L = 15 pF, No external I_{LOAD}		24		
		All channels switching with square wave clock input of 100 Mbps; C_L = 15 pF, No external I_{LOAD}		54		
$I_{ISO(OUT)}$ (2)	Current available to isolated supply	V_I = 0 V (ISOW7841A-Q1); V_I = V_{SI} (ISOW7841A-Q1 with F suffix)	128			mA
		V_I = V_{SI} (ISOW7841A-Q1); V_I = 0V (ISOW7841A-Q1 with F suffix)	130			
		All channels switching with square wave clock input of 1 Mbps; C_L = 15 pF	128			
		All channels switching with square wave clock input of 10 Mbps; C_L = 15 pF	127			
		All channels switching with square wave clock input of 100 Mbps; C_L = 15 pF	112			

(1) V_{SI} = input side supply; V_{SO} = output side supply
(2) Current available to load should be derated by 2 mA/°C for T_A > 80°C.

7.11 Electrical Characteristics—3.3-V Input, 5-V Output

V_{CC} = 3.3 V ±10%, SEL shorted to V_{ISO} (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ISO}	Isolated supply voltage	External I_{ISO} = 0 to 40 mA	4.5	5.07	5.43	V
$V_{ISO(LINE)}$	DC line regulation	I_{ISO} = 20 mA, V_{CC} = 4.5 V to 5.5 V		2		mV/V
$V_{ISO(LOAD)}$	DC load regulation	I_{ISO} = 0 to 40 mA		1%		
EFF	Efficiency at maximum load current	I_{ISO} = 40 mA, C_{LOAD} = 0.1 µF || 10 µF; V_I = V_{SI} (ISOW7841A-Q1); V_I =0 V (ISOW7841A-Q1 with F suffix)		42%		
$V_{CC+(UVLO)}$	Positive-going UVLO threshold on V_{CC}, V_{ISO}				2.7	V
$V_{CC-(UVLO)}$	Negative-going UVLO threshold on V_{CC}, V_{ISO}		2.1			V
$V_{HYS\ (UVLO)}$	UVLO threshold hysteresis on V_{CC}, V_{ISO}			0.2		V
V_{ITH}	Input pin rising threshold				0.7	V_{SI}
V_{ITL}	Input pin falling threshold		0.3			V_{SI}
$V_{I(HYS)}$	Input pin threshold hysteresis (INx)		0.1			V_{SI}
I_{IL}	Low level input current	V_{IL} = 0 at INx or SEL	–10			µA
I_{IH}	High level input current	V_{IH} = V_{SI} (1) at INx or SEL			10	µA
V_{OH}	High level output voltage	I_O = –4 mA, see Figure 8-1	V_{SO} (1) – 0.4	V_{SO} – 0.2		V
V_{OL}	Low level output voltage	I_O = 4 mA, see Figure 8-1		0.2	0.4	V
CMTI	Common mode transient immunity	V_I = V_{SI} or 0 V, V_{CM} = 1000 V; see Figure 8-2	100			kV/us

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC_SC}	DC current from supply under short circuit on V_{ISO}	V_{ISO} shorted to GND2		137		mA
$V_{ISO(RIP)}$	Output ripple on isolated supply (pk-pk)	20-MHz bandwidth, C_{LOAD} = 0.1 µF || 20 µF, I_{ISO} = 40 mA		90		mV

(1) V_{SI} = input side supply; V_{SO} = output side supply

7.12 Supply Current Characteristics—3.3-V Input, 5-V Output

V_{CC} = 3.3 V ±10%, SEL shorted to V_{ISO} (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (ISOW7841A-Q1); V_I = V_{SI} (1) (ISOW7841A-Q1 with F suffix)		31		mA
		No external I_{LOAD}; V_I = V_{SI} (ISOW7841A-Q1); V_I = 0V (ISOW7841A-Q1 with F suffix)		24		
		All channels switching with square wave clock input of 1 Mbps; C_L = 15 pF, No external I_{LOAD}		28		
		All channels switching with square wave clock input of 10 Mbps; C_L = 15 pF, No external I_{LOAD}		33		
		All channels switching with square wave clock input of 100 Mbps; C_L = 15 pF, No external I_{LOAD}		80		
$I_{ISO(OUT)}$ (2)	Current available to isolated supply	V_I = 0 V (ISOW7841A-Q1); V_I = V_{SI} (ISOW7841A-Q1 with F suffix)	38			mA
		V_I = V_{SI} (ISOW7841A-Q1); V_I = 0V (ISOW7841A-Q1 with F suffix)	40			
		All channels switching with square wave clock input of 1 Mbps; C_L = 15 pF	38			
		All channels switching with square wave clock input of 10 Mbps; C_L = 15 pF	37			
		All channels switching with square wave clock input of 100 Mbps; C_L = 15 pF	22			

(1) V_{SI} = input side supply; V_{SO} = output side supply
(2) Current available to load should be derated by 2 mA/°C for T_A > 80°C.

7.13 Electrical Characteristics—5-V Input, 3.3-V Output

V_{CC} = 5 V ±10%, SEL shorted to GND2 (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ISO}	Isolated supply voltage	External I_{ISO} = 0 to 50 mA	3.13	3.34	3.56	V
		External I_{ISO} = 0 to 130 mA	3	3.34	3.56	
$V_{ISO(LINE)}$	DC line regulation	I_{ISO} = 50 mA, V_{CC} = 4.5 V to 5.5 V		2		mV/V
$V_{ISO(LOAD)}$	DC load regulation	I_{ISO} = 10 to 130 mA		1%		
EFF	Efficiency at maximum load current	I_{ISO} = 130 mA, C_{LOAD} = 0.1 µF || 10 µF; V_I = V_{SI} (ISOW7841A-Q1); V_I = 0 V (ISOW7841A-Q1 with F suffix)		48%		
$V_{CC+(UVLO)}$	Positive-going UVLO threshold on V_{CC}, V_{ISO}				2.7	V
$V_{CC-(UVLO)}$	Negative-going UVLO threshold on V_{CC}, V_{ISO}		2.1			V
$V_{HYS\ (UVLO)}$	UVLO threshold hysteresis on V_{CC}, V_{ISO}			0.2		V
V_{ITH}	Input pin rising threshold				0.7	V_{SI}
V_{ITL}	Input pin falling threshold		0.3			V_{SI}
$V_{I(HYS)}$	Input pin threshold hysteresis (INx)		0.1			V_{SI}

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IL}	Low level input current	V_{IL} = 0 at INx or SEL	–10			µA
I_{IH}	High level input current	V_{IH} = V_{SI} (1) at INx or SEL			10	µA
V_{OH}	High level output voltage	I_O = –2 mA, see Figure 8-1	V_{SO} (1) – 0.3	V_{SO} – 0.1		V
V_{OL}	Low level output voltage	I_O = 2 mA, see Figure 8-1		0.1	0.3	V
CMTI	Common mode transient immunity	V_I = V_{SI} or 0 V, V_{CM} = 1000 V; see Figure 8-2	100			kV/us
I_{CC_SC}	DC current from supply under short circuit on V_{ISO}	V_{ISO} shorted to GND2		137		mA
$V_{ISO(RIP)}$	Output ripple on isolated supply (pk-pk)	20-MHz bandwidth, C_{LOAD} = 0.1 µF || 20 µF, I_{ISO} = 130 mA		100		mV

(1) V_{SI} = input side supply; V_{SO} = output side supply

7.14 Supply Current Characteristics—5-V Input, 3.3-V Output

V_{CC} = 5 V ±10%, SEL shorted to GND2 (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (ISOW7841A-Q1); V_I = V_{SI} (1) (ISOW7841A-Q1 with F suffix)		20		mA
		No external I_{LOAD}; V_I = V_{SI} (ISOW7841A-Q1); V_I = 0 V (ISOW7841A-Q1 with F suffix)		14		
		All channels switching with square wave clock input of 1 Mbps; C_L = 15 pF, No external I_{LOAD}		17		
		All channels switching with square wave clock input of 10 Mbps; C_L = 15 pF, No external I_{LOAD}		20		
		All channels switching with square wave clock input of 100 Mbps; C_L = 15 pF, No external I_{LOAD}		40		
$I_{ISO(OUT)}$ (2)	Current available to isolated supply	V_I = 0 V (ISOW7841A-Q1); V_I = V_{SI} (ISOW7841A-Q1 with F suffix)	128			mA
		V_I = V_{SI} (ISOW7841A-Q1); V_I = 0 V (ISOW7841A-Q1 with F suffix)	130			
		All channels switching with square wave clock input of 1 Mbps; C_L= 15 pF	129			
		All channels switching with square wave clock input of 10 Mbps; C_L = 15 pF	128			
		All channels switching with square wave clock input of 100 Mbps; C_L = 15 pF	118			

(1) V_{SI} = input side supply; V_{SO} = output side supply
(2) Current available to load should be derated by 2 mA/°C for T_A > 105°C.

7.15 Electrical Characteristics—3.3-V Input, 3.3-V Output

V_{CC} = 3.3 V ±10%, SEL shorted to GND2 (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ISO}	Isolated supply voltage	External I_{ISO} = 0 to 30 mA	3.13	3.34	3.58	V
		External I_{ISO} = 0 to 75 mA	3	3.34	3.58	
$V_{ISO(LINE)}$	DC line regulation	I_{ISO} = 30 mA, V_{CC} = 3 V to 3.6 V		2		mV/V
$V_{ISO(LOAD)}$	DC load regulation	I_{ISO} = 0 to 75 mA		1%		
EFF	Efficiency at maximum load current	I_{ISO} = 75 mA, C_{LOAD} = 0.1 µF || 10 µF; V_I = V_{SI} (ISOW7841A-Q1); V_I = 0 V (ISOW7841A-Q1 with F suffix)		47%		
$V_{CC+(UVLO)}$	Positive-going UVLO threshold on V_{CC}, V_{ISO}				2.7	V

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CC–(UVLO)}$	Negative-going UVLO threshold on V_{CC}, V_{ISO}		2.1			V
$V_{HYS\ (UVLO)}$	UVLO threshold hysteresis on V_{CC}, V_{ISO}			0.2		V
V_{ITH}	Input pin rising threshold				0.7	V_{SI}
V_{ITL}	Input pin falling threshold		0.3			V_{SI}
$V_{I(HYS)}$	Input pin threshold hysteresis (INx)		0.1			V_{SI}
I_{IL}	Low level input current	V_{IL} = 0 at INx or SEL	–10			µA
I_{IH}	High level input current	V_{IH} = V_{SI} (1) at INx or SEL			10	µA
V_{OH}	High level output voltage	I_O = –2 mA, see Figure 8-1	V_{SO} (1) – 0.3	V_{SO} – 0.1		V
V_{OL}	Low level output voltage	I_O = 2 mA, see Figure 8-1		0.1	0.3	V
CMTI	Common mode transient immunity	V_I = V_{SI} or 0 V, V_{CM} = 1000 V; see Figure 8-2	100			kV/us
I_{CC_SC}	DC current from supply under short circuit on V_{ISO}	V_{ISO} shorted to GND2		143		mA
$V_{ISO(RIP)}$	Output ripple on isolated supply (pk-pk)	20-MHz bandwidth, C_{LOAD} = 0.1 µF || 20 µF, I_{ISO} = 75 mA		90		mV

(1) V_{SI}= input side supply; V_{SO} = output side supply

7.16 Supply Current Characteristics—3.3-V Input, 3.3-V Output

V_{CC} = 3.3 V ±10%, SEL shorted to GND2 (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Current drawn from supply	No external I_{LOAD}; V_I = 0 V (ISOW7841A-Q1); V_I = V_{SI} (1) (ISOW7841A-Q1 with F suffix)		26		mA
		No external I_{LOAD}; V_I = V_{SI} (ISOW7841A-Q1); V_I = 0 V (ISOW7841A-Q1 with F suffix)		20		
		All channels switching with square wave clock input of 1 Mbps; C_L = 15 pF, No external I_{LOAD}		23		
		All channels switching with square wave clock input of 10 Mbps; C_L = 15 pF, No external I_{LOAD}		26		
		All channels switching with square wave clock input of 100 Mbps; C_L = 15 pF, No external I_{LOAD}		53		
$I_{ISO(OUT)}$ (2)	Current available to isolated supply	V_I = 0 V (ISOW7841A-Q1); V_I = V_{SI} (ISOW7841A-Q1 with F suffix)	73			mA
		V_I = V_{SI}(ISOW7841A-Q1); V_I = 0V (ISOW7841A-Q1 with F suffix)	75			
		All channels switching with square wave clock input of 1 Mbps; C_L = 15 pF	74			
		All channels switching with square wave clock input of 10 Mbps; C_L = 15 pF	73			
		All channels switching with square wave clock input of 100 Mbps; C_L = 15 pF	61			

(1) V_{SI} = input side supply; V_{SO} = output side supply
(2) Current available to load should be derated by 2 mA/°C for T_A > 115°C.

7.17 Switching Characteristics—5-V Input, 5-V Output

V_{CC} = 5 V ±10%, SEL shorted to V_{ISO} (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 8-1		13	17.6	ns

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.6	4.7	ns
$t_{SK(o)}$	Channel-channel output skew time(2)	Same-direction channels			2.5	ns
$t_{SK(p-p)}$	Part-part skew time(3)				4.5	ns
t_r, t_f	Output signal rise and fall times			2	4	ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

7.18 Switching Characteristics—3.3-V Input, 5-V Output

V_{CC} = 3.3 V ±10%, SEL shorted to V_{ISO} (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 8-1		13.5	19.6	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.6	4.7	ns
$t_{SK(o)}$	Channel-channel output skew time(2)	Same-direction channels			2.5	ns
$t_{SK(p-p)}$	Part-part skew time(3)				4.5	ns
t_r, t_f	Output signal rise and fall times			2	4	ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

7.19 Switching Characteristics—5-V Input, 3.3-V Output

V_{CC} = 5 V ±10%, SEL shorted to GND2 (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 8-1		14	19.7	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.6	4.4	ns
$t_{SK(o)}$	Channel-channel output skew time(2)	Same-direction channels			2	ns
$t_{SK(p-p)}$	Part-part skew time(3)				4.5	ns
t_r, t_f	Output signal rise and fall times			1	4	ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

7.20 Switching Characteristics—3.3-V Input, 3.3-V Output

V_{CC} = 3.3 V ±10%, SEL shorted to GND2 (over recommended operating conditions, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 8-1		14.5	20.2	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.6	4.4	ns
$t_{SK(o)}$	Channel-channel output skew time(2)	Same-direction channels			2.2	ns
$t_{SK(p-p)}$	Part-part skew time(3)				4.5	ns
t_r, t_f	Output signal rise and fall times			1	3	ns

(1) Also known as pulse skew.

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(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

7.21 Insulation Characteristics Curves

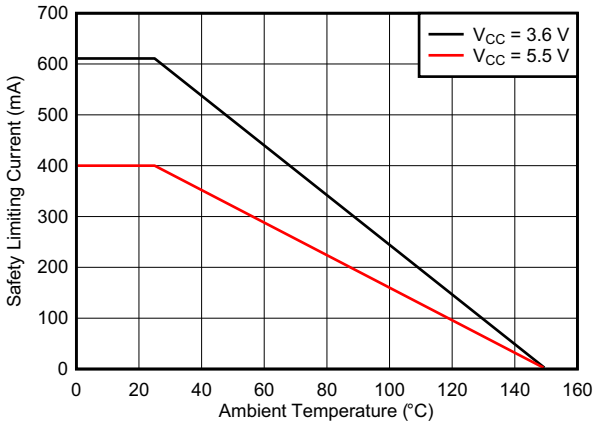


Figure 7-1. Thermal Derating Curve for Safety Limiting Current per VDE

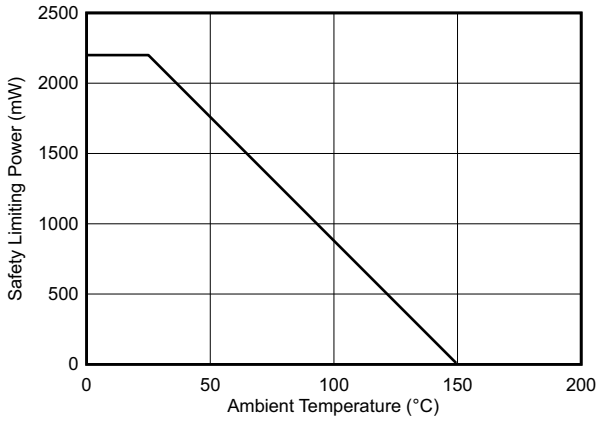
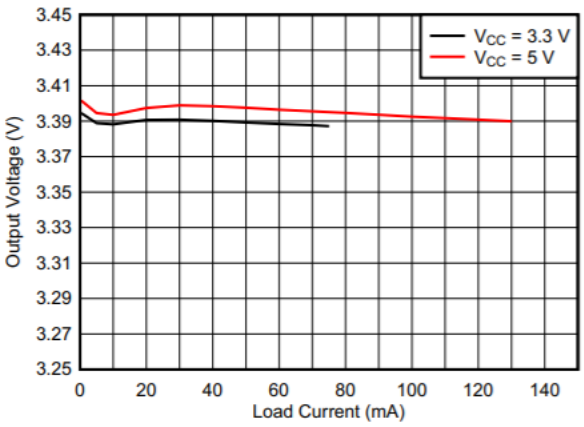


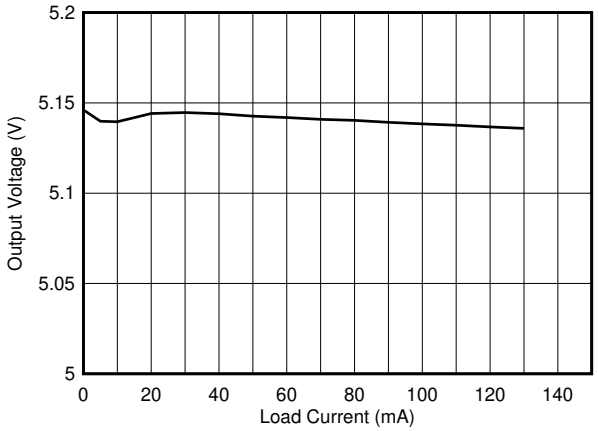
Figure 7-2. Thermal Derating Curve for Safety Limiting Power per VDE

7.22 Typical Characteristics



V_{ISO} = 3.3 V T_A = 25°C

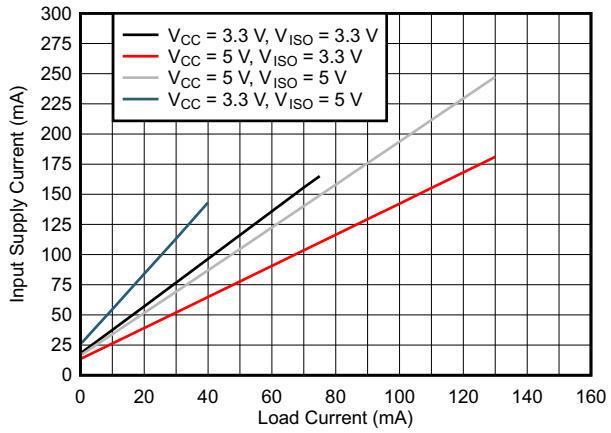
Figure 7-3. Isolated Supply Voltage (V_{ISO}) vs Load Current (I_{ISO})



V_{ISO} = 5 V T_A = 25°C

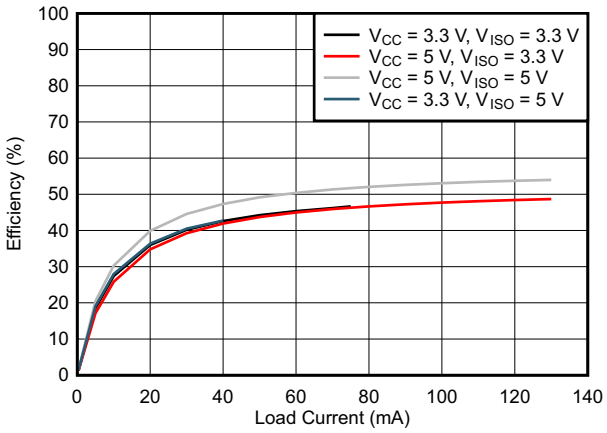
Figure 7-4. Isolated Supply Voltage (V_{ISO}) vs Load Current (I_{ISO})

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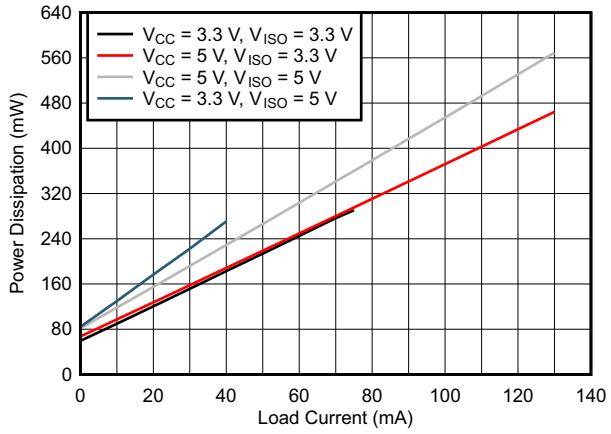
T_A = 25°C

Figure 7-5. ISOW7841 Supply Current (I_{CC}) vs Load Current (I_{ISO})



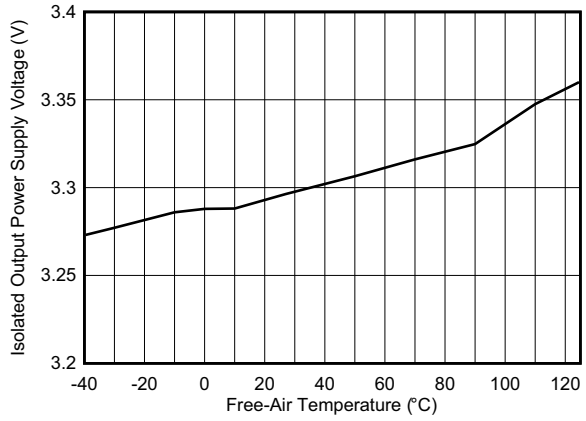
T_A = 25°C

Figure 7-6. ISOW7841 Efficiency vs Load Current (I_{ISO})



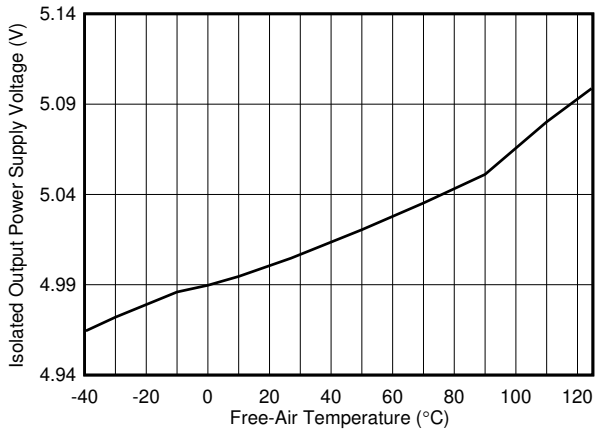
T_A = 25°C

Figure 7-7. ISOW7841 Power Dissipation vs Load Current (I_{ISO})



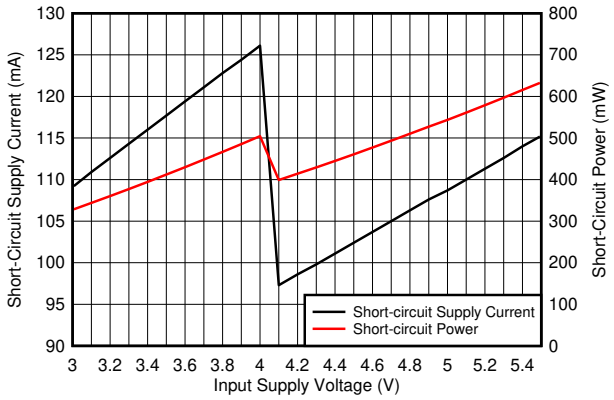
No I_{ISO} load V_{CC} = 5 V V_{ISO} = 3.3 V

Figure 7-8. 3.3-V Isolated Supply Voltage (V_{ISO}) vs Free-Air Temperature



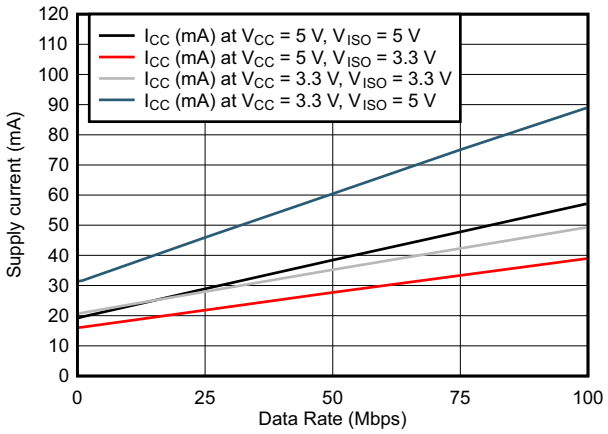
No I_{ISO} load V_{CC} = 5 V V_{ISO} = 5 V

Figure 7-9. 5-V Isolated Supply Voltage (V_{ISO}) vs Free-Air Temperature



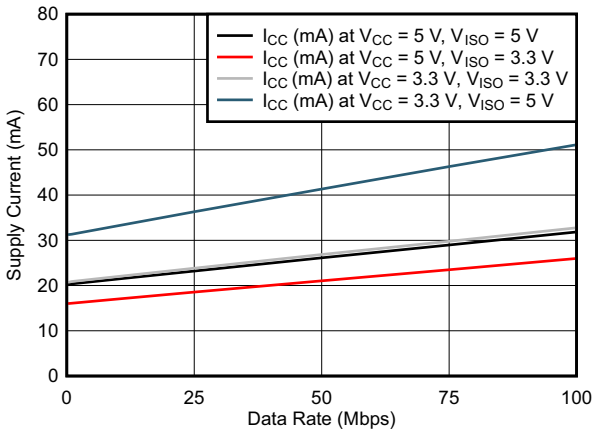
V_{ISO} shorted to GND2 T_A = 25°C

Figure 7-10. Short-Circuit Supply Current (I_{CC}) and Power (P) vs Supply Voltage (V_{CC})



C_L = 15 pF T_A = 25°C No I_{ISO} load

Figure 7-11. ISOW7841A-Q1 Supply Current vs Data Rate



C_L = no load T_A = 25°C No I_{ISO} load

Figure 7-12. ISOW7841A-Q1 Supply Current vs Data Rate

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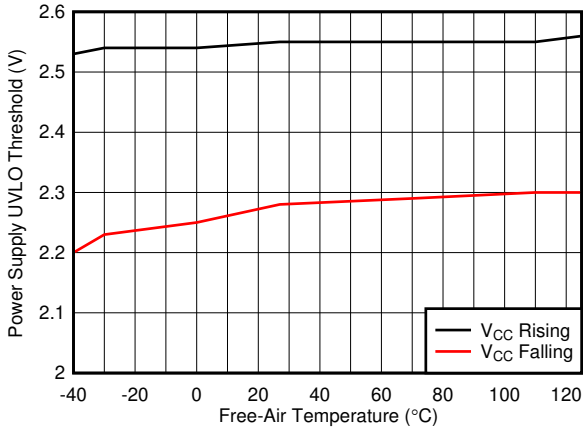


Figure 7-13. Power-Supply Undervoltage Threshold vs Free Air Temperature

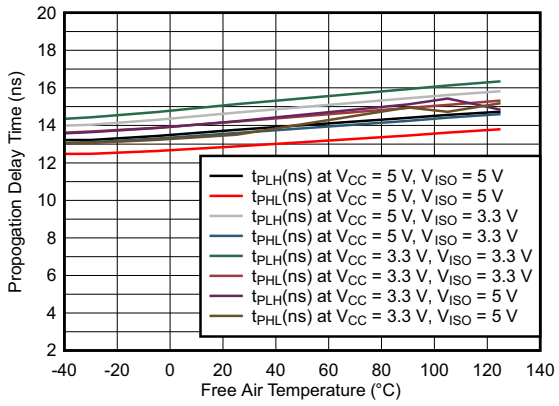
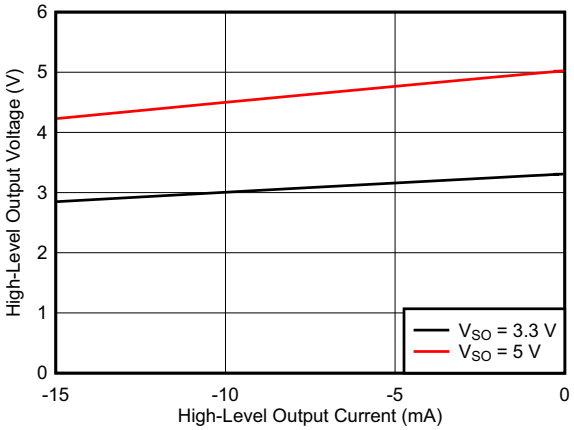
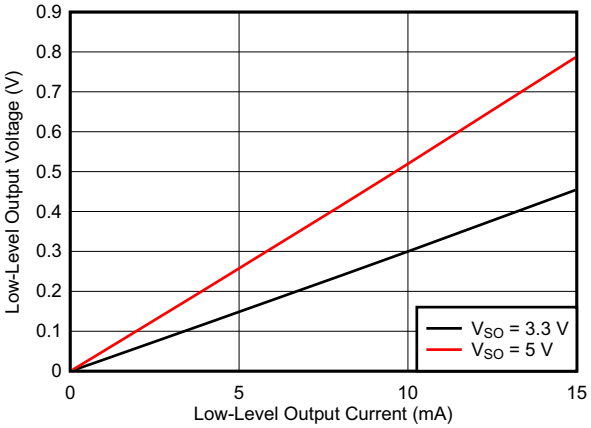


Figure 7-14. Propagation Delay Time vs Free-Air Temperature



T_A = 25°C

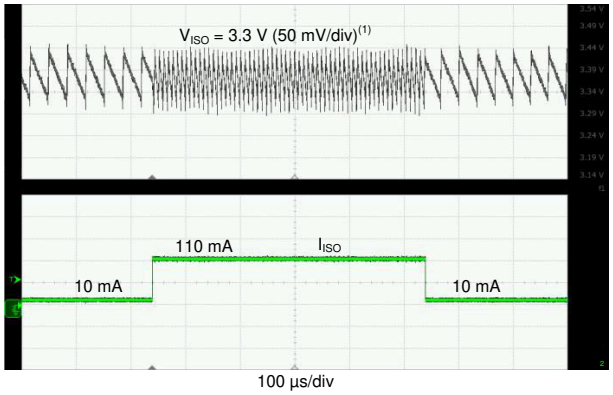
Figure 7-15. High-Level Output Voltage vs High-Level Output Current



T_A = 25°C

Figure 7-16. Low-Level Output Voltage vs Low-Level Output Current

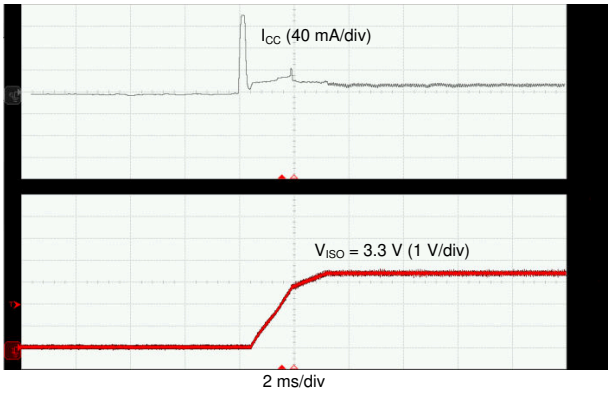
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V_{CC} = 5 V V_{ISO} = 3.3 V

Negligible undershoot and overshoot because of load transient

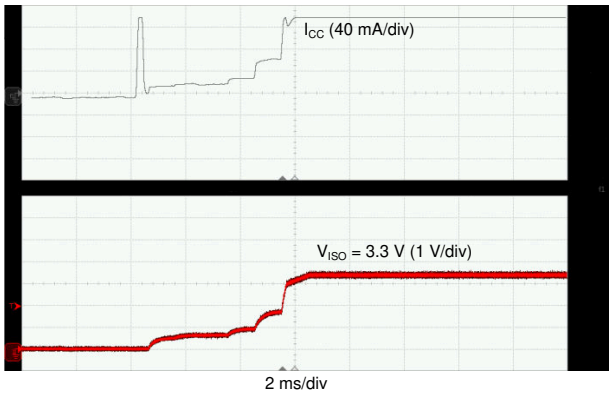
Figure 7-17. 10-mA to 110-mA Load Transient Response



V_{CC} = 5 V V_{ISO} = 3.3 V

Current spike is because of charging the input supply capacitor

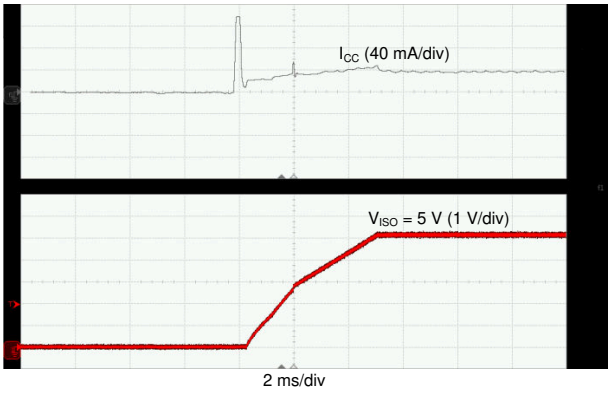
Figure 7-18. Soft Start at 10-mA Load



V_{CC} = 5 V V_{ISO} = 3.3 V

Input current spike is because of charging the input supply decoupling capacitor

Figure 7-19. Soft Start at 120-mA Load

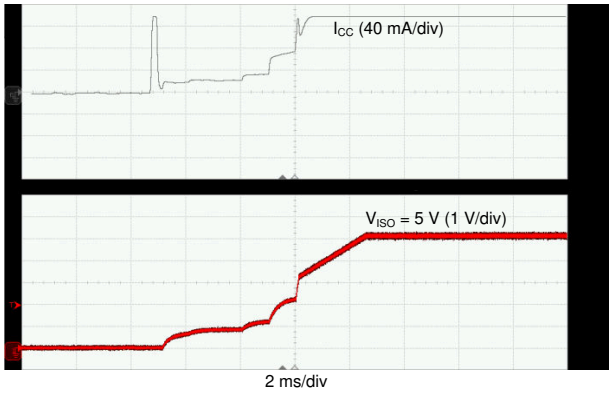


V_{CC} = 5 V V_{ISO} = 5 V

Input current spike is because of charging the input supply decoupling capacitor

Figure 7-20. Soft Start at 10-mA Load

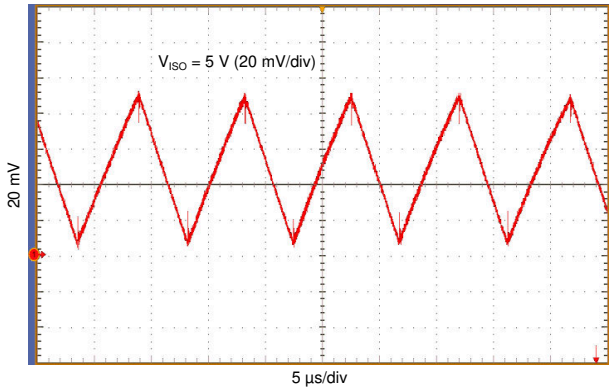
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V_{CC} = 5 V V_{ISO} = 5 V

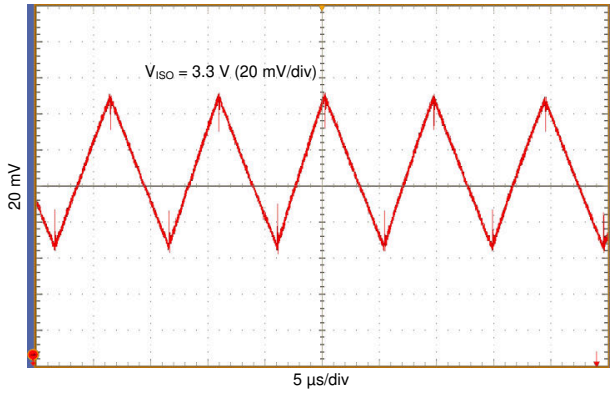
Input current spike is because of charging the input supply decoupling capacitor

Figure 7-21. Soft Start at 130-mA Load



V_{CC} = 5 V V_{ISO} = 5 V

Figure 7-22. V_{ISO} Ripple Voltage at 130 mA

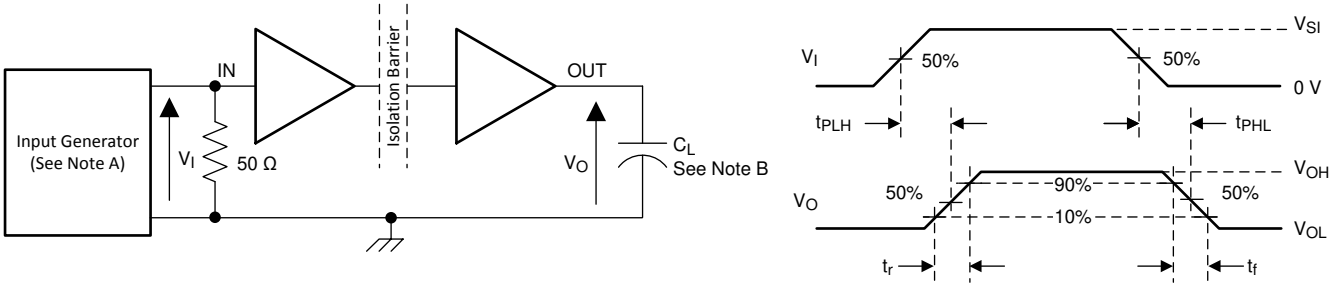


V_{CC} = 5 V V_{ISO} = 3.3 V

Figure 7-23. V_{ISO} Ripple Voltage at 130 mA

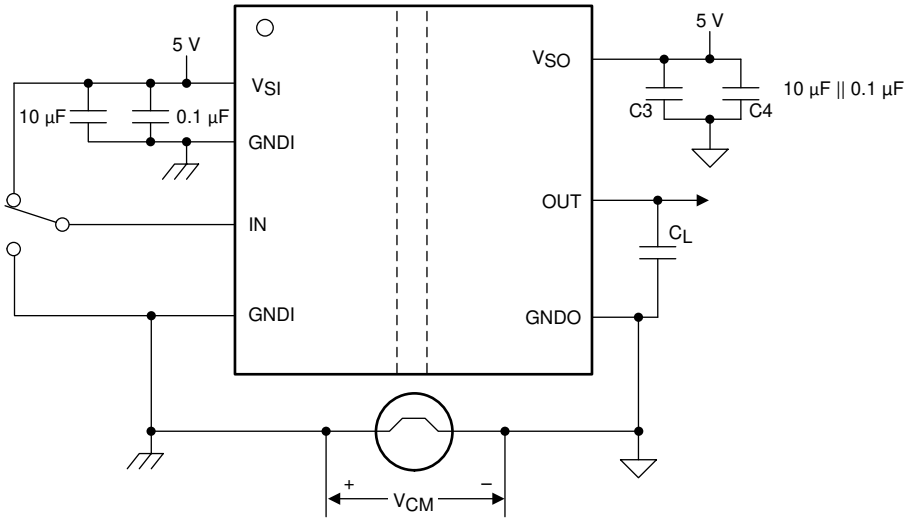
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8 Parameter Measurement Information



1. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω. At the input, 50-Ω resistor is required to terminate the input generator signal. The resistor is not required in the actual application.
2. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 8-1. Switching Characteristics Test Circuit and Voltage Waveforms



1. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.
2. Pass-fail criteria: Outputs must remain stable.

Figure 8-2. Common-Mode Transient Immunity Test Circuit

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9 Detailed Description

9.1 Overview

The ISOW7841A-Q1 has a high-efficiency, low-emissions isolated DC-DC converter, and four high-speed isolated data channels. Block Diagram shows the functional block diagram of the ISOW7841A-Q1.

The integrated DC-DC converter uses switched mode operation and proprietary circuit techniques to reduce power losses and boost efficiency. Specialized control mechanisms, clocking schemes, and the use of a high-Q on-chip transformer provide high efficiency and low radiated emissions. The integrated transformer uses thin film polymer as the insulation barrier.

The V_{CC} supply is provided to the primary power controller that switches the power stage connected to the integrated transformer. Power is transferred to the secondary side, rectified and regulated to either 3.3 V or 5 V, depending on the SEL pin. The output voltage, V_{ISO}, is monitored and feedback information is conveyed to the primary side through a dedicated isolation channel. The duty cycle of the primary switching stage is adjusted accordingly. The fast feedback control loop of the power converter ensures low overshoots and undershoots during load transients. Undervoltage lockout (UVLO) with hysteresis is integrated on the V_{CC} and V_{ISO} supplies which ensures robust system performance under noisy conditions. An integrated soft-start mechanism ensures controlled inrush current and avoids any overshoot on the output during power up.

The integrated signal-isolation channels employ an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon-dioxide based isolation barrier. The transmitter sends a high-frequency carrier across the barrier to represent one state and sends no signal to represent the other state. The receiver demodulates the signal after signal conditioning and produces the output through a buffer stage. The signal-isolation channels incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions from the high frequency carrier and IO buffer switching. Figure 9-2 shows a functional block diagram of a typical signal isolation channel.

The ISOW7841A-Q1 is suitable for applications that have limited board space and require more integration. This device is also suitable for very-high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive.

9.2 Functional Block Diagram

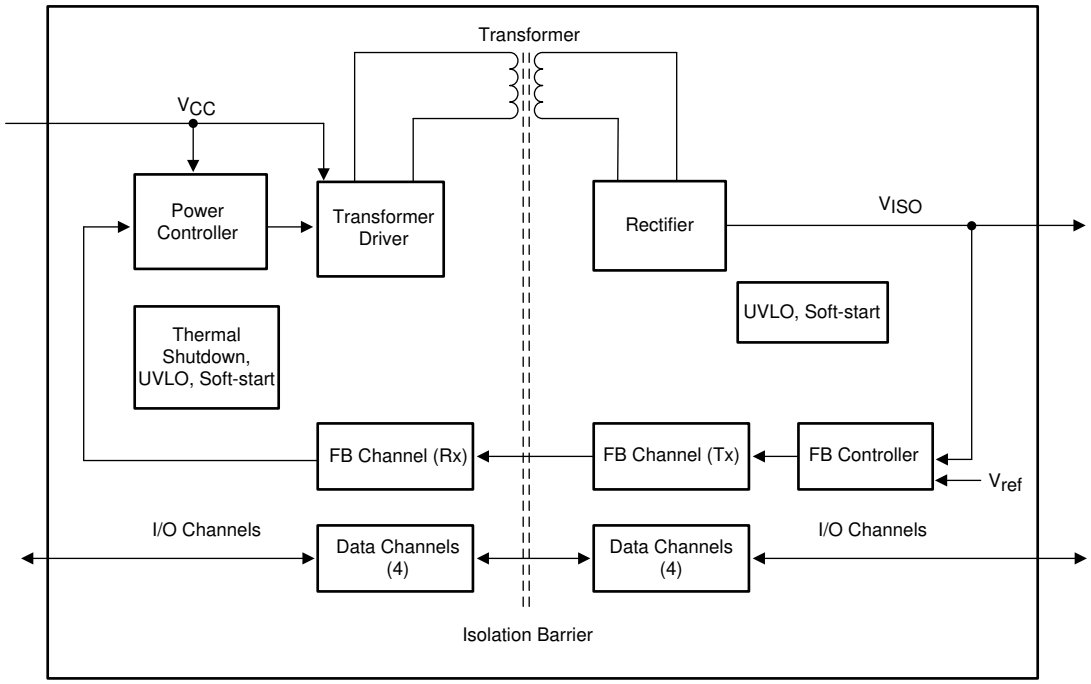


Figure 9-1. Block Diagram

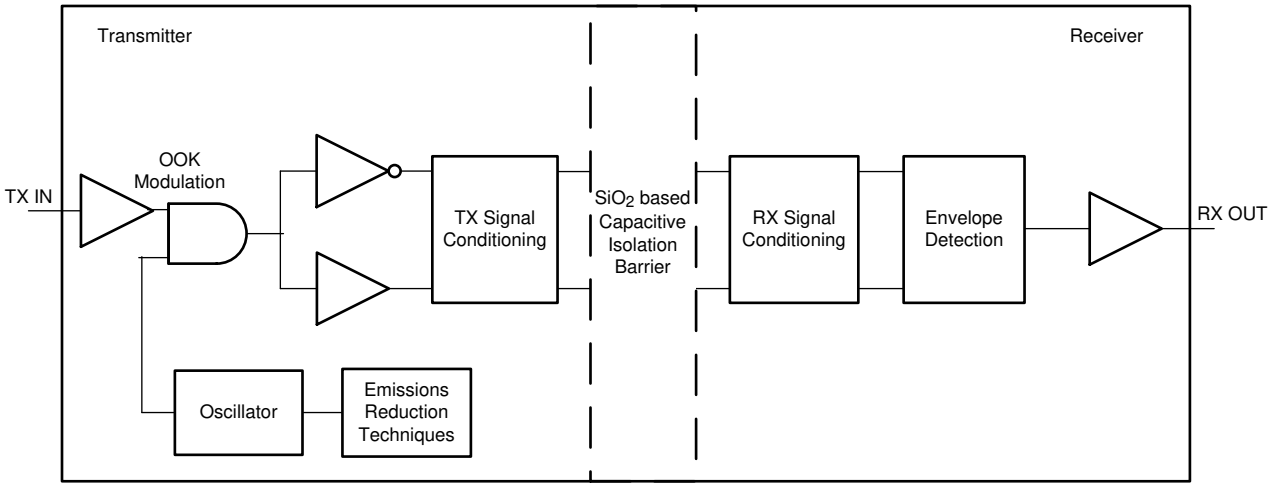


Figure 9-2. Conceptual Block Diagram of a Capacitive Data Channel

Figure 9-3 shows a conceptual detail of how the OOK scheme works.

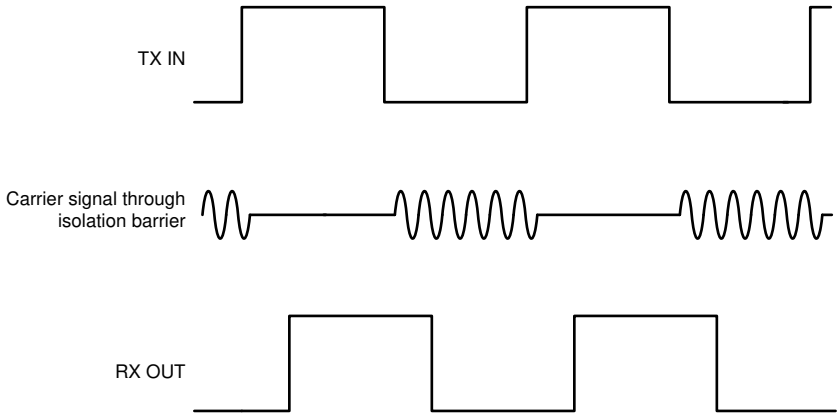


Figure 9-3. On-Off Keying (OOK) Based Modulation Scheme

9.3 Feature Description

Table 9-1 shows an overview of the device features.

Table 9-1. Device Features

PART NUMBER(1)	CHANNEL DIRECTION	MAXIMUM DATA RATE	DEFAULT OUTPUT STATE	RATED ISOLATION(2)
ISOW7841A-Q1	3 forward, 1 reverse	100 Mbps	High	5 kV_{RMS} / 7071 V_{PK}
ISOW7841FA-Q1			Low	

(1) The F suffix is part of the orderable part number. See the section for the full orderable part number.
(2) For detailed isolation ratings, see the table.

9.3.1 Electromagnetic Compatibility (EMC) Considerations

The ISOW7841A-Q1 uses emissions reduction schemes for the internal oscillator and advanced internal layout scheme to minimize radiated emissions at the system level.

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level

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performance and reliability depends, to a large extent, on the application board design and layout, the ISOW7841A-Q1 incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

9.3.2 Power-Up and Power-Down Behavior

The ISOW7841A-Q1 has built-in UVLO on the V_{CC} and V_{ISO} supplies with positive-going and negative-going thresholds and hysteresis. When the V_{CC} voltage crosses the positive-going UVLO threshold during power-up, the DC-DC converter initializes and the power converter duty cycle is increased in a controlled manner. This soft-start scheme limits primary peak currents drawn from the V_{CC} supply and charges the V_{ISO} output in a controlled manner, avoiding overshoots. Outputs of the isolated data channels are in an indeterminate state until the V_{CC} or V_{ISO} voltage crosses the positive-going UVLO threshold. When the UVLO positive-going threshold is crossed on the secondary side V_{ISO} pin, the feedback data channel starts providing feedback to the primary controller. The regulation loop takes over and the isolated data channels go to the normal state defined by the respective input channels or their default states. Design should consider a sufficient time margin (typically 10 ms with 10-µF load capacitance) to allow this power up sequence before valid data channels are accounted for system functionality.

When V_{CC} power is lost, the primary side DC-DC controller turns off when the UVLO lower threshold is reached. The V_{ISO} capacitor then discharges depending on the external load. The isolated data outputs on the V_{ISO} side are returned to the default state for the brief time that the V_{ISO} voltage takes to discharge to zero.

9.3.3 Current Limit, Thermal Overload Protection

The ISOW7841A-Q1 is protected against output overload and short circuit. Output voltage starts dropping when the power converter is not able to deliver the current demanded during overload conditions. For a V_{ISO} short-circuit to ground, the duty cycle of the converter is limited to help protect against any damage.

Thermal protection is also integrated to help prevent the device from getting damaged during overload and short-circuit conditions on the isolated output. Under these conditions, the device temperature starts to increase. When the temperature goes above 180°C, thermal shutdown activates and the primary controller turns off which removes the energy supplied to the V_{ISO} load, which causes the device to cool off. When the junction temperature goes below 150°C, the device starts to function normally. If an overload or output short-circuit condition prevails, this protection cycle is repeated. Care should be taken in the design to prevent the device junction temperatures from reaching such high values.

9.4 Device Functional Modes

Table 9-2 lists the supply configurations for these devices.

Table 9-2. Supply Configurations

SEL INPUT	V_{CC}	V_{ISO}
Shorted to V_{ISO}	5 V	5 V
Shorted to V_{ISO}	3.3 V	5 V
Shorted to GND2 or floating	5 V	3.3 V
Shorted to GND2 or floating	3.3 V	3.3 V(1)

(1) The SEL pin has a weak pulldown internally. Therefore for V_{ISO} = 3.3 V, the SEL pin should be strongly connected to the GND2 pin in noisy system scenarios.

Table 9-3 lists the functional modes for ISOW7841A-Q1.

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Table 9-3. Function Table

INPUT SUPPLY (V_{CC})	INPUT (INx)	OUTPUT (OUTx)	COMMENTS
PU	H	H	Output channel assumes the logic state of its input
	L	L	
	Open	Default	Default mode(1): When INx is open, the corresponding output channel assumes logic based on default output mode of selected version
PD	X	Undetermined(2)	

(1) In the default condition, the output is high for ISOW7841A-Q1 and low for ISOW7841A-Q1 with the F suffix.
(2) The outputs are in an undetermined state when V_{CC} < 2.1 V.

9.4.1 Device I/O Schematics

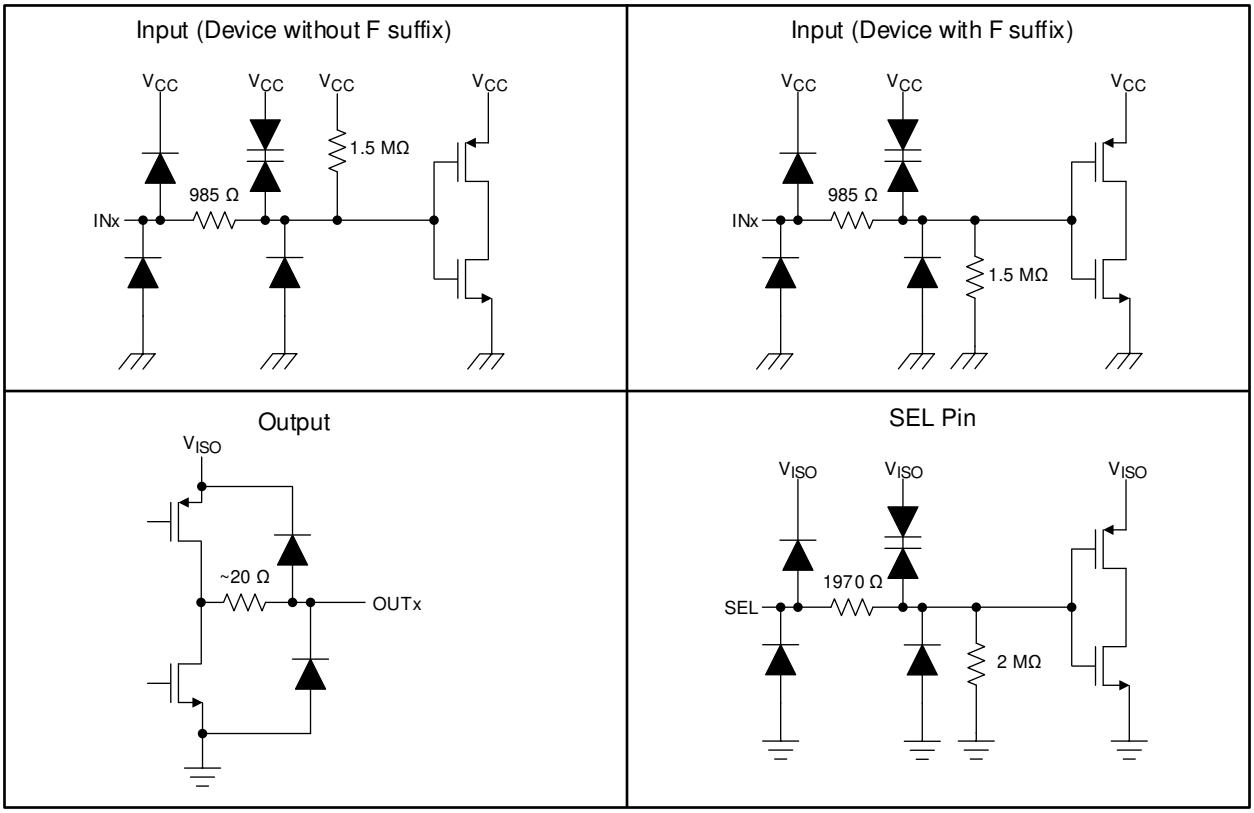


Figure 9-4. Device I/O Schematics

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10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The device is a high-performance, quad channel digital isolator with integrated DC-DC converter. Typically digital isolators require two power supplies isolated from each other to power up both sides of device. Due to the integrated DC-DC converter in the device, the isolated supply is generated inside the device that can be used to power isolated side of the device and peripherals on isolated side, thus saving board space. The device uses single-ended CMOS-logic switching technology. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is Microcontroller or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

The device is suitable for applications that have limited board space and desire more integration. The device is also suitable for very high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive.

10.2 Typical Application

Figure 10-1 shows the typical schematic for SPI isolation. Typically, an ADC is used to monitor HV battery to chassis insulation resistance.

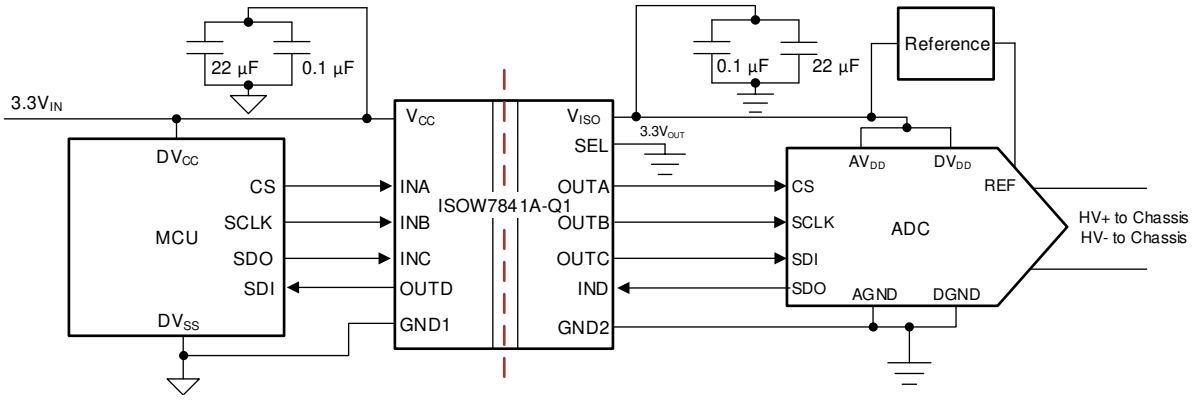


Figure 10-1. Isolated Power and SPI for Automotive BMS Insulation monitoring Application with ISOW7841A-Q1

10.2.1 Design Requirements

To design with this device, use the parameters listed in Table 10-1.

Table 10-1. Design Parameters

PARAMETER	VALUE
Input voltage	3 V to 5.5 V
Decoupling capacitor between V_{CC} and GND1	0.1 µF to 10 µF
Decoupling capacitor between V_{ISO} and GND2	0.1 µF to 10 µF

Because of very-high current flowing through the ISOW7841A-Q1 device V_{CC} and V_{ISO} supplies, higher decoupling capacitors typically provide better noise and ripple performance. Although a 10-µF capacitor is

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adequate, higher decoupling capacitors (such as 22 µF or 47 µF) on both the V_{CC} and V_{ISO} pins to the respective grounds are strongly recommended to achieve the best performance.

10.2.2 Detailed Design Procedure

The devices requires only external bypass capacitors to operate. These low-ESR ceramic bypass capacitors must be placed as close to the chip pads as possible.

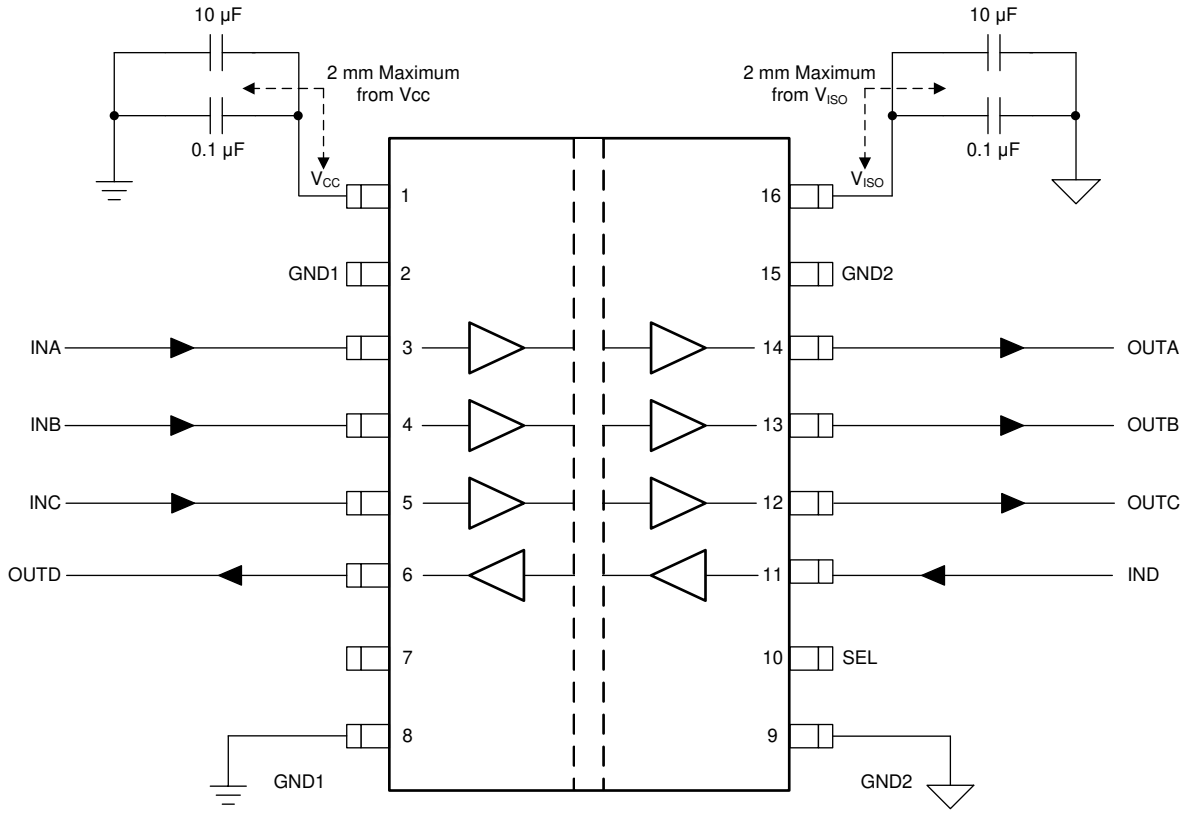


Figure 10-2. Typical ISOW7841A-Q1 Circuit Hook-Up

The V_{CC} power-supply input provides power to isolated data channels and to the isolated DC-DC converter. Use Equation 1 to calculate the total power budget on the primary side.

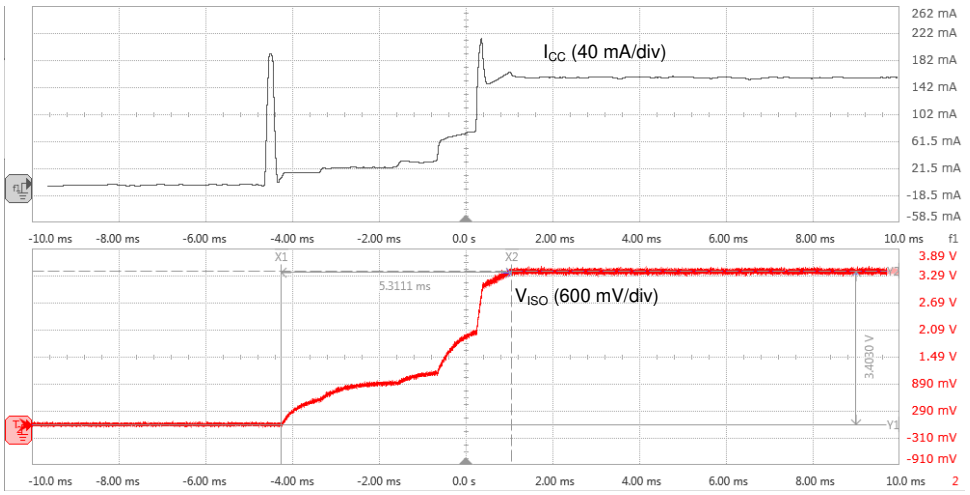
$$I_{CC} = (V_{ISO} \times I_{ISO}) / (\eta \times V_{CC}) + I_{inpx} \quad (1)$$

where

- I_{CC} is the total current required by the primary supply.
- V_{ISO} is the isolated supply voltage.
- I_{ISO} is the external load on the isolated supply voltage.
- η is the efficiency.
- V_{CC} is the supply voltage.
- I_{inpx} is the total current drawn for the isolated data channels and power converter when data channels are toggling at a specific data rate. This data is shown in the Section 7.9 table.

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10.2.3 Application Curve



V_{CC} = 3.3 V I_{ISO} = 70 mA

Input current spike is because of charging the input supply decoupling capacitor

Figure 10-3. Soft-Start Waveform

10.2.3.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See Figure 10-4 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 87.5% for lifetime which translates into minimum required insulation lifetime of 37.5 years at a working voltage that's 20% higher than the specified value.

Figure 10-5 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 1000 V_{RMS} with a lifetime of 1184 years.

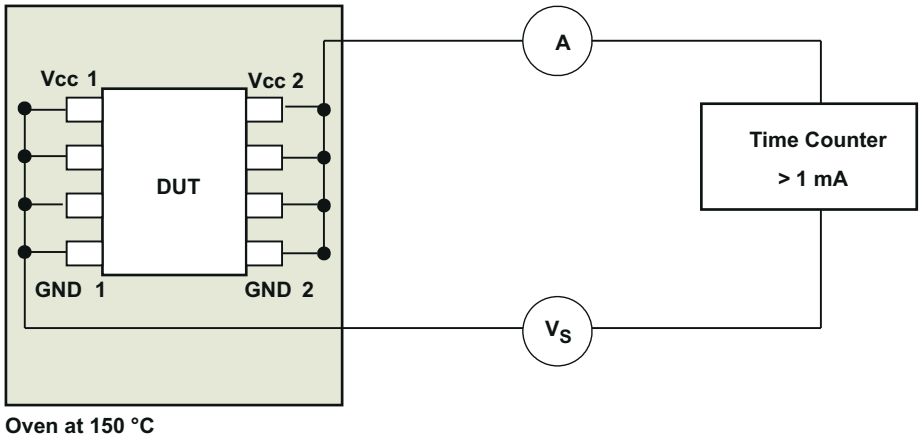


Figure 10-4. Test Setup for Insulation Lifetime Measurement

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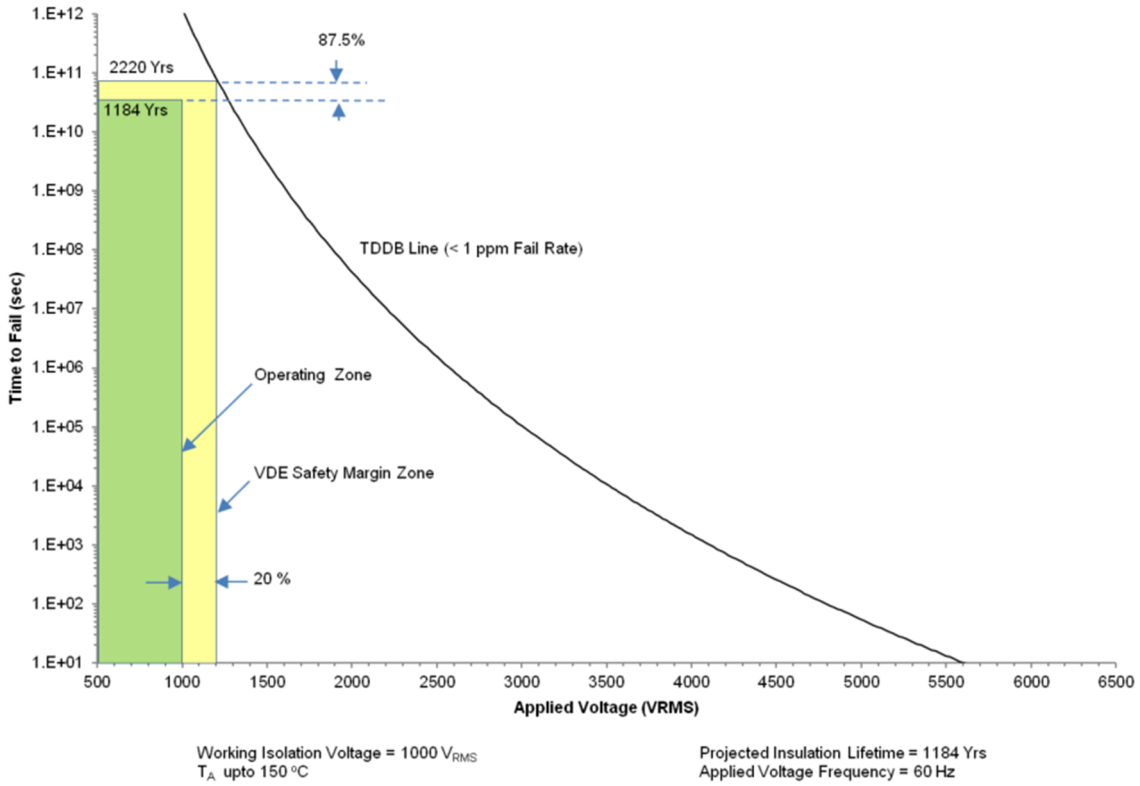


Figure 10-5. Insulation Lifetime Projection Data

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Power Supply Recommendations

To help make sure that operation is reliable at data rates and supply voltages, adequate decoupling capacitors must be located as close to supply pins as possible. The input supply (V_{CC}) must have an appropriate current rating to support output load and switching at the maximum data rate required by the end application. For more information, refer to the *Detailed Design Procedure* section.

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11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low-EMI PCB design (see Figure 11-1). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane, and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.
- Keep decoupling capacitors as close as possible to the V_{CC} and V_{ISO} pins.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

Because the device has no thermal pad to dissipate heat, the device dissipates heat through the respective GND pins. Ensure that enough copper is present on both GND pins to prevent the internal junction temperature of the device from rising to unacceptable levels.

The integrated signal and power isolation device simplifies system design and reduces board area. The use of low-inductance micro-transformers in the device necessitates the use of high frequency switching, resulting in higher radiated emissions compared to discrete solutions. The device uses on-chip circuit techniques to reduce emissions compared to competing solutions. For further reduction in radiated emissions at system level, refer to the *Low-Emission Designs With ISOW7841 Integrated Signal and Power Isolator* application report.

11.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

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11.2 Layout Example

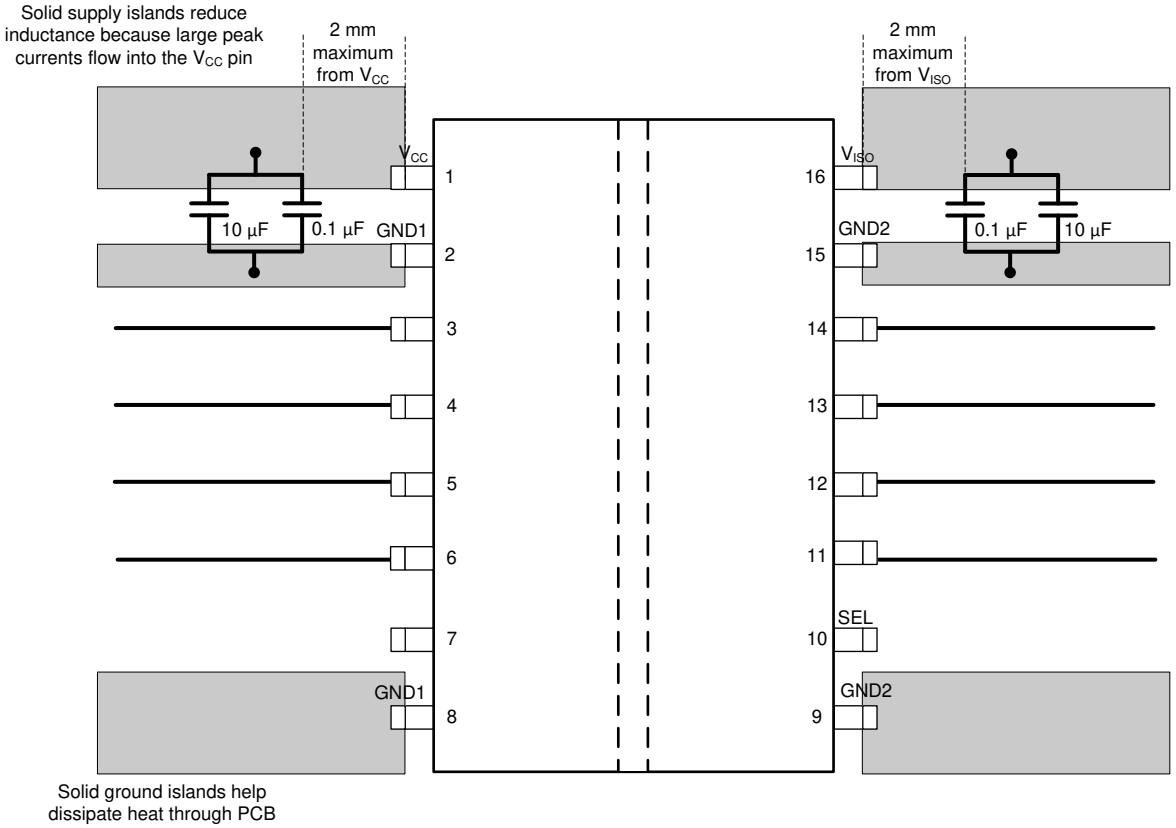


Figure 11-1. Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

For development support, refer to:

- 8-ch Isolated High Voltage Analog Input Module with ISOW7841 Reference Design
- Isolated CAN Module With Integrated Power Reference Design

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *Isolation Glossary*
- Texas Instruments, *ISOW784x Quad-Channel Digital Isolator With Integrated DC-DC Converter Evaluation Module* user's guide
- Texas Instruments, *Low-Emission Designs With ISOW7841 Integrated Signal and Power Isolator* application report

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI ™E2E Online Community	TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.
Design Support	TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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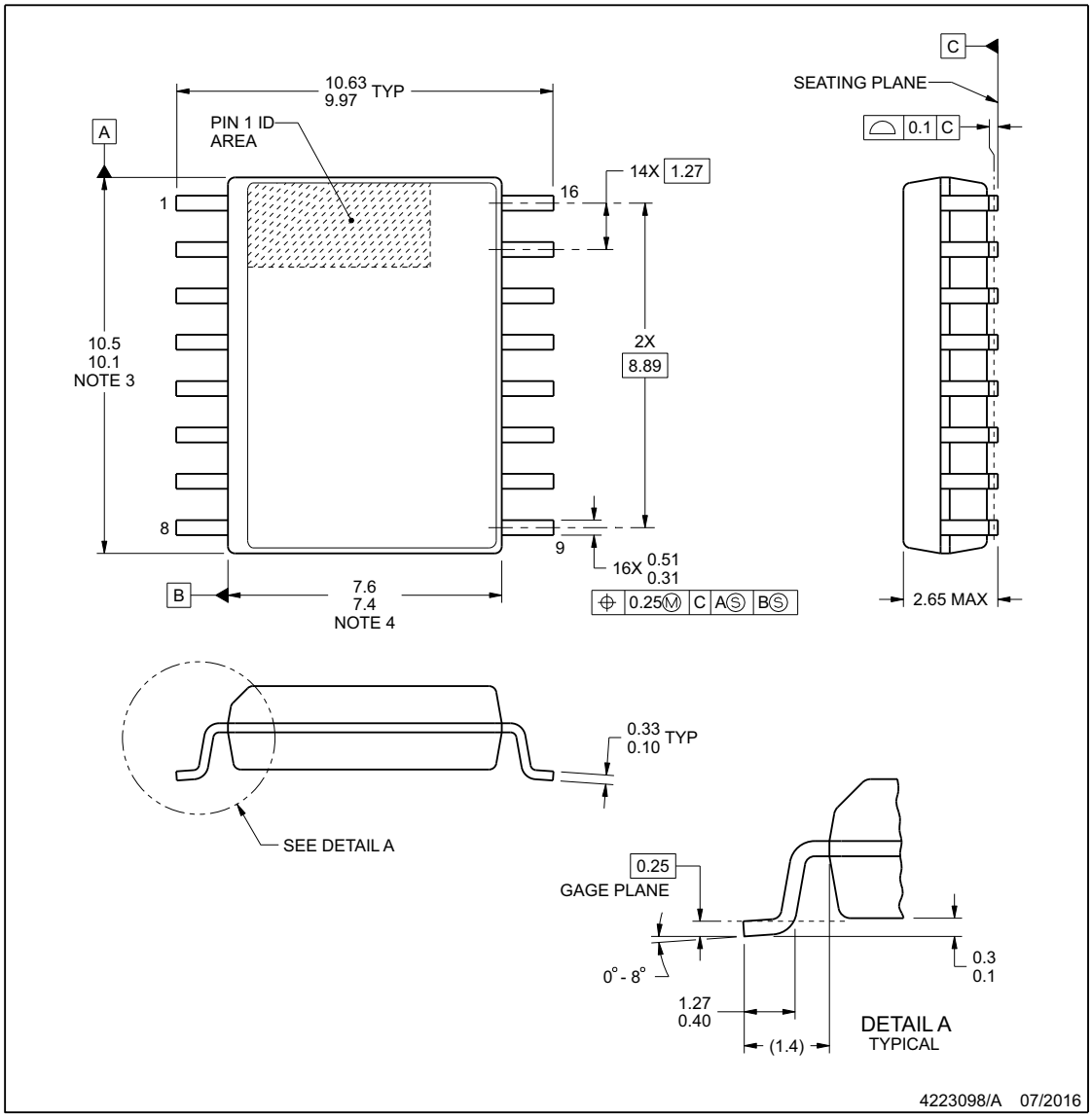


PACKAGE OUTLINE

DWE0016A

SOIC - 2.65 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

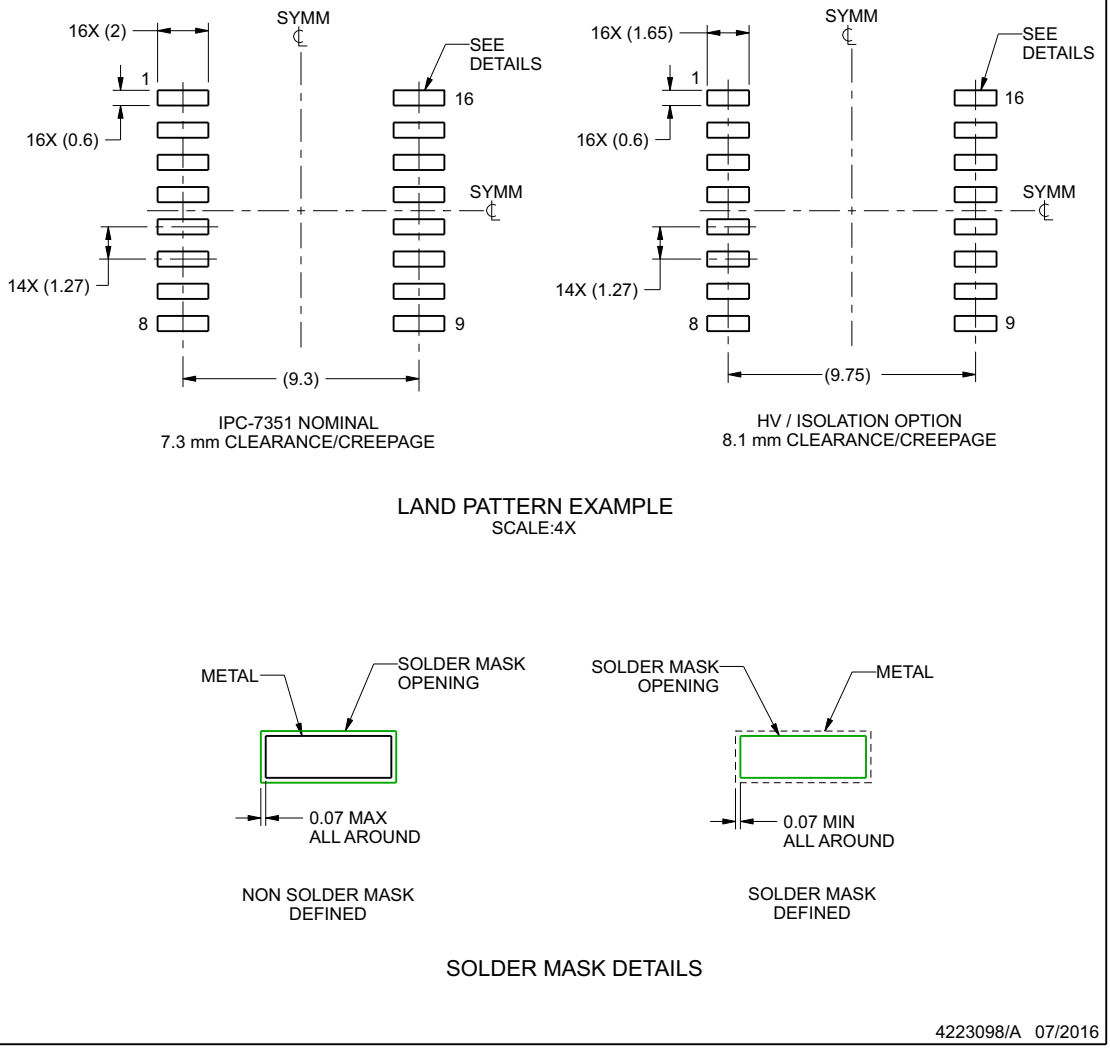
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EXAMPLE BOARD LAYOUT

DWE0016A

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

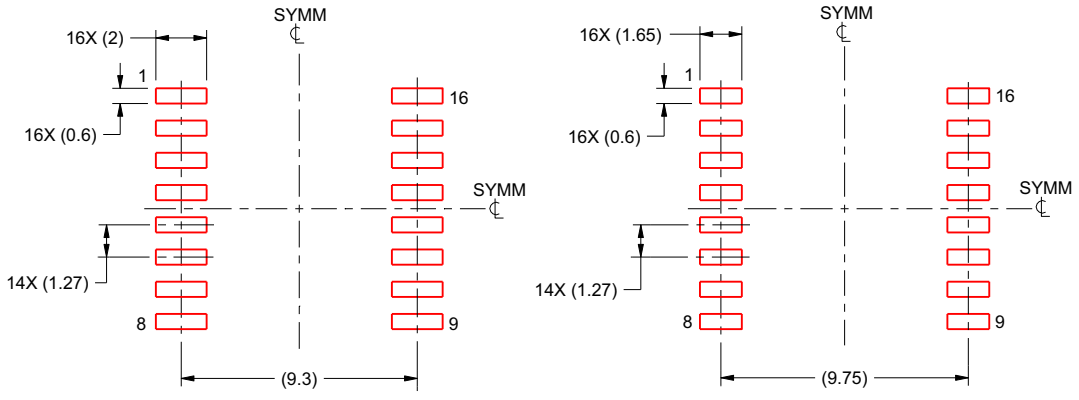
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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EXAMPLE STENCIL DESIGN

DWE0016A — **SOIC - 2.65 mm max height**

SOIC



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4223098/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISOW7841AQDWEQ1	ACTIVE	SOIC	DWE	16	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	W7841A Q1	Samples
ISOW7841AQDWERQ1	ACTIVE	SOIC	DWE	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	W7841A Q1	Samples
ISOW7841FAQDWEQ1	ACTIVE	SOIC	DWE	16	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	W7841FA Q1	Samples
ISOW7841FAQDWERQ1	ACTIVE	SOIC	DWE	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	W7841FA Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

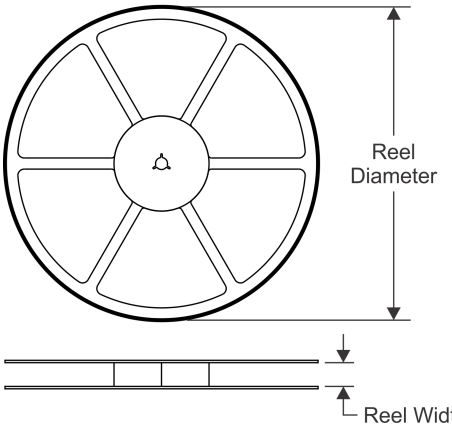
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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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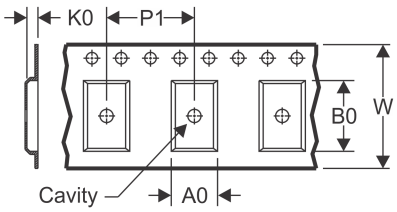
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

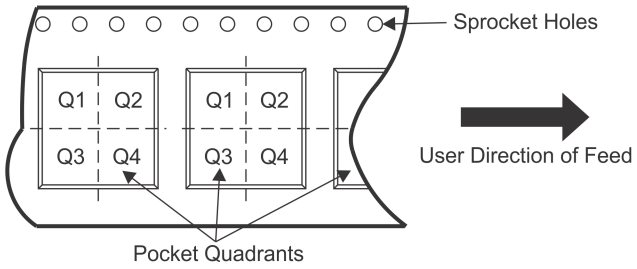


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

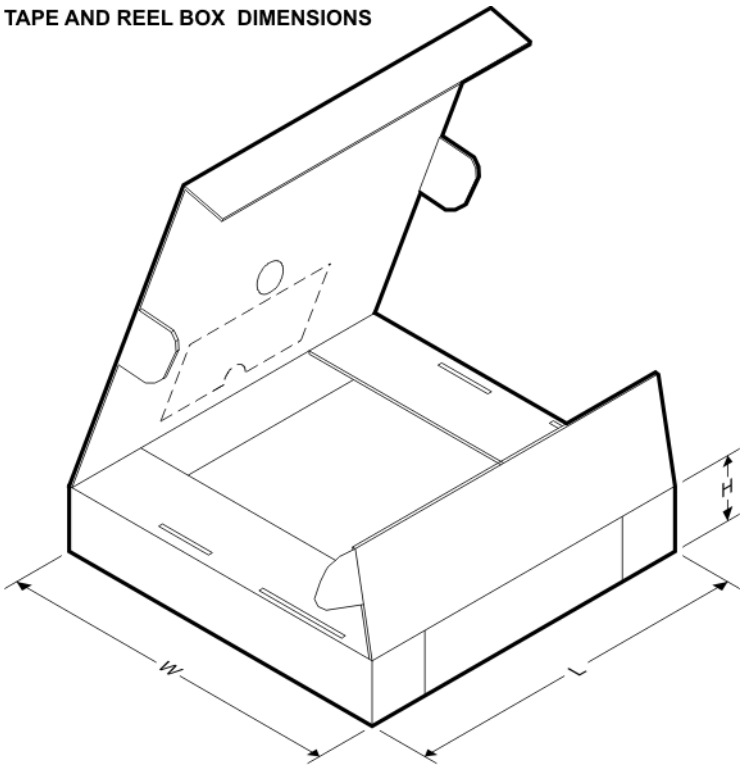
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISOW7841AQDWERQ1	SOIC	DWE	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISOW7841FAQDWERQ1	SOIC	DWE	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

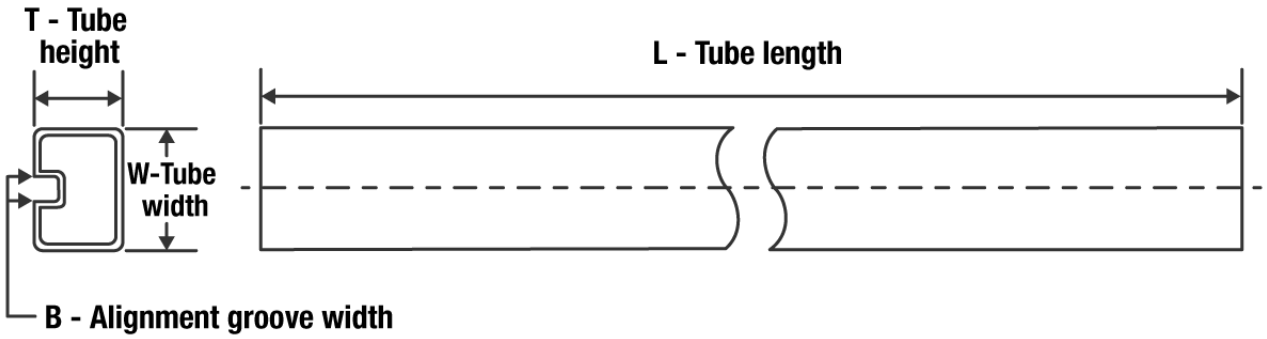
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

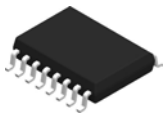
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISOW7841AQDWERQ1	SOIC	DWE	16	2000	350.0	350.0	43.0
ISOW7841FAQDWERQ1	SOIC	DWE	16	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISOW7841AQDWEQ1	DWE	SO-MOD	16	40	506.98	12.7	4826	6.6
ISOW7841FAQDWEQ1	DWE	SO-MOD	16	40	506.98	12.7	4826	6.6

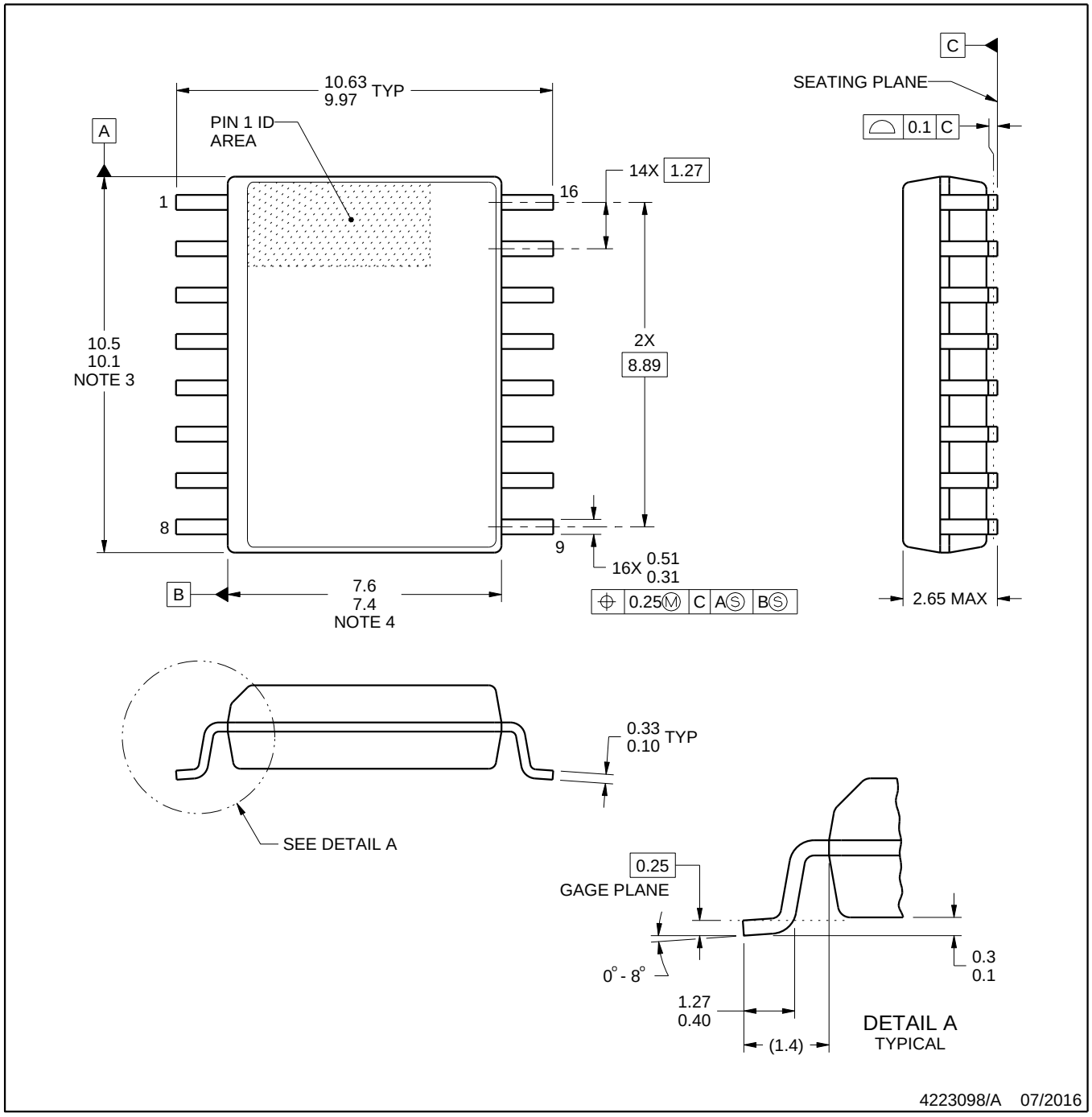


PACKAGE OUTLINE

DWE0016A

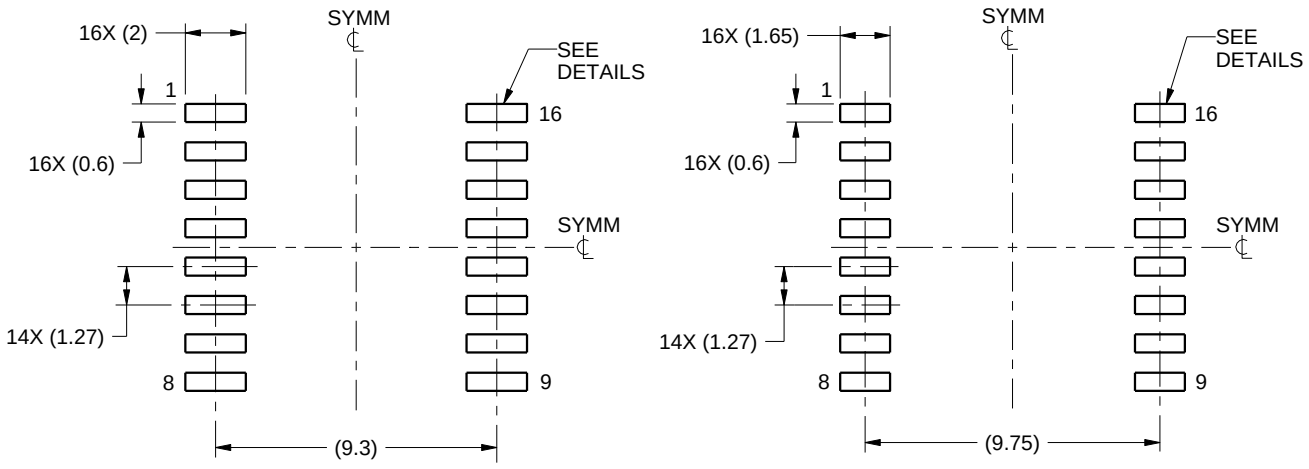
SOIC - 2.65 mm max height

SOIC



NOTES:

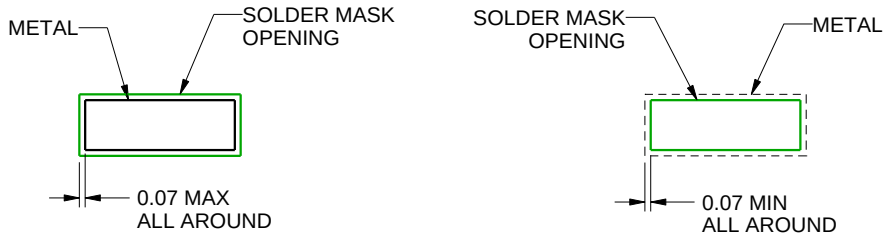
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

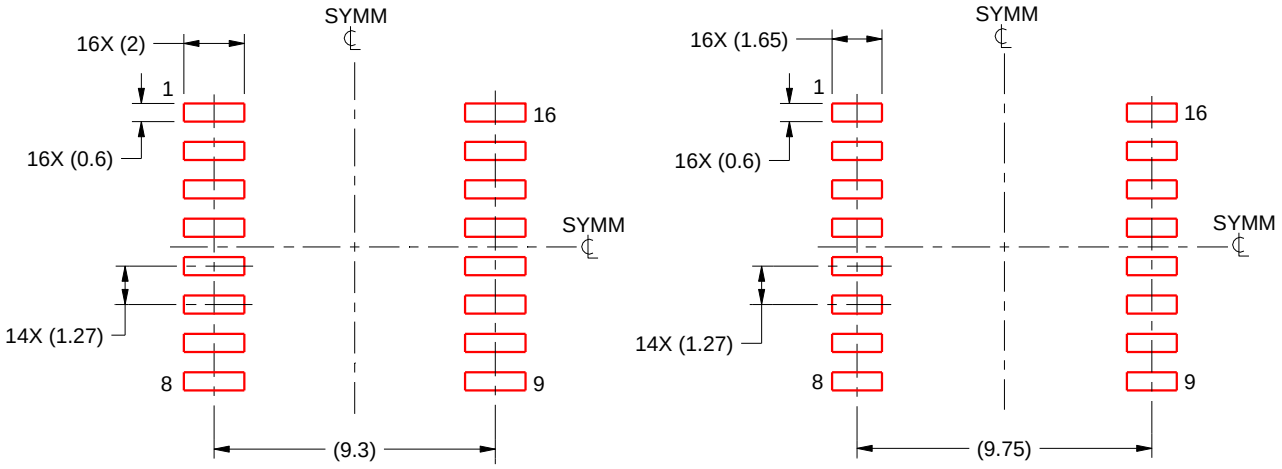
SOLDER MASK DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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