适合低功耗 HMI 按钮应用的 LDC2112/LDC2114 电感应触控解决 方案

1 特性

- 低功耗：
  - 一个按钮：6μA（速率为 0.625SPS 时）
  - 两个按钮：72μA（速率为 20SPS 时）
- 可配置按钮扫描频率：
  - 0.625SPS 至 80SPS
- 触摸按钮的应力水平测量
- 独立通道运算：
  - 适用于 LDC2112 的双通道
  - 适用于 LDC2114 的四通道
- 集成算法，可支持：
  - 调节每个按钮的力阈值
  - 环境变化补偿
  - 同步按钮按压检测
- 支持独立运算，无需 MCU
- 强大的 EMI 性能：
  - 支持 CISPR 22 和 CISPR 24 合规性
- 工作电压范围：1.8V ± 5%
- 温度范围：-40°C 至 +85°C
- 接口：
  - I^2C
  - 每个通道的专用逻辑输出

2 应用

以下产品的触控按钮及其所用不同材料（包括金属、塑料和玻璃材料）的应力水平测量：

- 消费类电子产品：
  - 智能手机
  - 智能手表及其他可穿戴设备
  - 智能扬声器
  - 平板电脑/PC
  - 虚拟现实耳机
  - 条形音箱
- 工业 应用：
  - 电视
  - 手持设备
  - 家用电器
  - HMI 面板和键盘

3 说明

借助电感式传感技术，设计人员可以测量导电目标的小幅偏移，从而在金属、玻璃、塑料和木材等各种材料上实现人机界面 (HMI) 的触控按钮设计。电感应触控系统的传感器是一款可在小型 PCB 上实现的线圈，该 PCB 位于面板后方，以免受外界环境影响。电感式传感解决方案不受湿度或油污和灰尘等非导电污染物的干扰。它能够自动更正导电目标出现的任何变形。

LDC2112/LDC2114 是一款多通道、低噪声电感数字转换器，采用集成算法，可实现电感应触控 应用。该器件采用创新型 LC 谐振器，可高度抑制噪音和干扰。即使材料偏移不足 200nm，LDC2112/LDC2114 也能够可靠地检测出来。

LDC2112/LDC2114 还提供了超低功耗模式，专供电池供电类应用中的开通/关断按钮 使用。

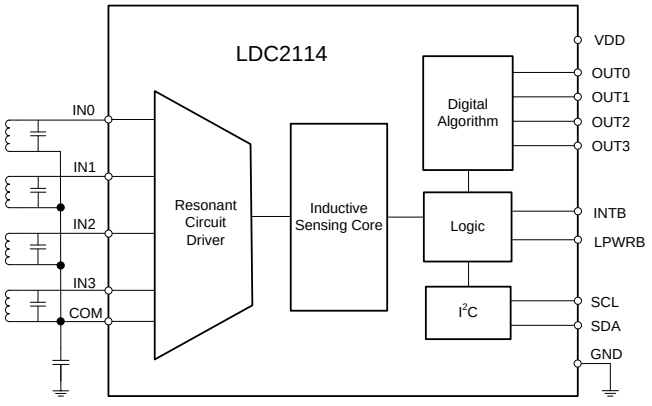
LDC2112/LDC2114 采用 16 引脚 DSBGA 或 TSSOP 封装。DSBGA 封装（间距为 0.4mm）的标称封装尺寸非常小，仅为 1.6 × 1.6mm，其最大高度为 0.4mm。TSSOP 封装（间距为 0.65mm）的标称封装尺寸为 5.0 × 4.4mm，其最大高度为 1.2mm。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LDC2112/LDC2114	DSBGA (16)	1.6mm x 1.6mm
LDC2112/LDC2114	TSSOP (16)	5.0mm × 4.4mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

简化原理图



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4 修订历史记录

Changes from Revision A (January 2017) to Revision B **Page**

- Changed unit of Data set-up time from µs to ns (typo) ... 7
- 已更改 Multi-Channel and Single-Channel Operation ... 11
- 已添加 LDC2112 to Register EN – Address 0x0C Table ... 19

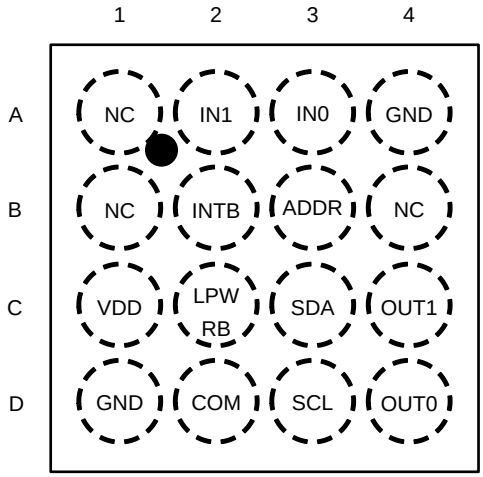
Changes from Original (December 2016) to Revision A **Page**

- 已更改 将“高级信息”更改成了“生产数据发布” ... 1

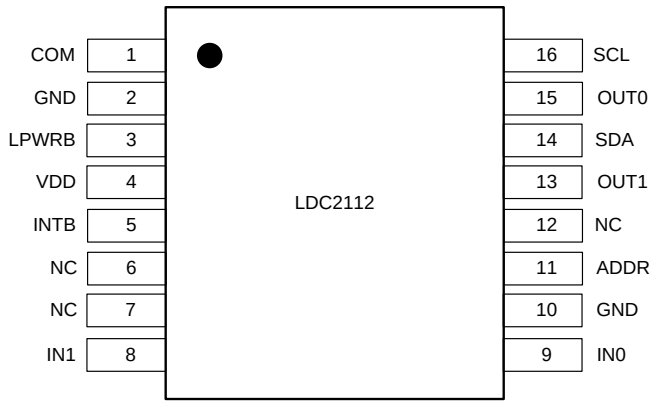
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5 Pin Configuration and Functions

LDC2112
16-Pin DSBGA
Top View (Bumps Down)



LDC2112
16-Pin TSSOP
Top View



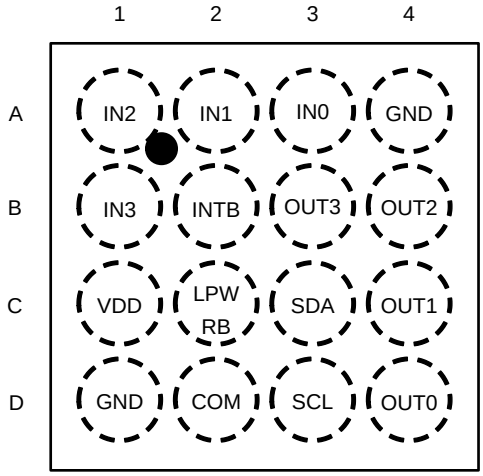
Pin Functions - LDC2112

PIN			I/O(1)	DESCRIPTION
NAME	DSBGA NO.	TSSOP NO.		
VDD	C1	4	P	Power supply
GND	D1	2	G	Ground(2)
	A4	10		
INTB	B2	5	O	Interrupt output Polarity can be configured in Register 0x11.
LPWRB	C2	3	I	Normal / Low Power Mode select Set LPWRB to V_{DD} for Normal Power Mode or ground for Low Power Mode.
COM	D2	1	A	Common return current path for all LC resonator sensors A capacitor should be connected from this pin to GND. Refer to *Setting COM Pin Capacitor*.
IN0	A3	9	A	Channel 0 LC sensor input
IN1	A2	8	A	Channel 1 LC sensor input
OUT0	D4	15	O	Channel 0 logic output Polarity can be configured in Register 0x1C.
OUT1	C4	13	O	Channel 1 logic output Polarity can be configured in Register 0x1C.
ADDR	B3	11	I	I^2C address When ADDR = Ground, I^2C address = 0x2A. When ADDR = V_{DD}, I^2C address = 0x2B.
SCL	D3	16	I	I^2C clock
SDA	C3	14	I/O	I^2C data
NC	A1	7	—	No connect Leave them floating.
	B1	6		
	B4	12		

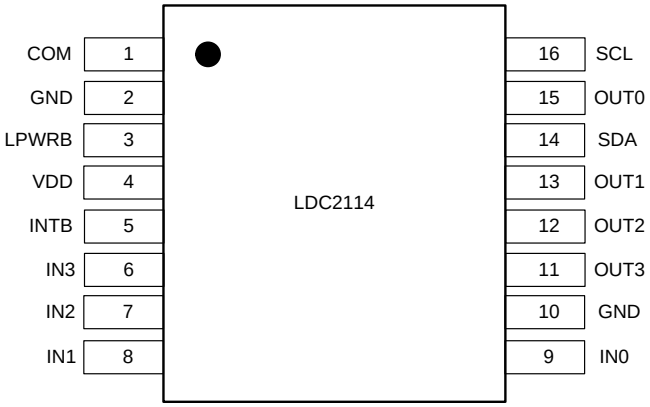
(1) I = Input, O = Output, P=Power, G=Ground, A=Analog
(2) Both pins should be connected to the system ground on the PCB.

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LDC2114
16-Pin DSBGA
Top View (Bumps Down)



LDC2114
16-Pin TSSOP
Top View



Pin Functions - LDC2114

PIN			I/O(1)	DESCRIPTION
NAME	DSBGA NO.	TSSOP NO.		
VDD	C1	4	P	Power supply
GND	D1	2	G	Ground(2)
	A4	10		
INTB	B2	5	O	Interrupt output Polarity can be configured in Register 0x11.
LPWRB	C2	3	I	Normal / Low Power Mode select Set LPWRB to V_{DD} for Normal Power Mode or ground for Low Power Mode.
COM	D2	1	A	Common return current path for all LC resonator sensors A capacitor should be connected from this pin to GND. Refer to *Setting COM Pin Capacitor*.
IN0	A3	9	A	Channel 0 LC sensor input
IN1	A2	8	A	Channel 1 LC sensor input
IN2	A1	7	A	Channel 2 LC sensor input
IN3	B1	6	A	Channel 3 LC sensor input
OUT0	D4	15	O	Channel 0 logic output Polarity can be configured in Register 0x1C.
OUT1	C4	13	O	Channel 1 logic output Polarity can be configured in Register 0x1C.
OUT2	B4	12	O	Channel 2 logic output Polarity can be configured in Register 0x1C.
OUT3	B3	11	O	Channel 3 logic output Polarity can be configured in Register 0x1C.
SCL	D3	16	I	I^2C clock
SDA	C3	14	I/O	I^2C data I^2C address = 0x2A.

(1) I = Input, O = Output, P=Power, G=Ground, A=Analog
(2) Both pins should be connected to the system ground on the PCB.

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating temperature range unless otherwise noted.(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage		2.2	V
V_I	Voltage on SCL, SDA	–0.3	3.6	V
	Voltage on any other pin	–0.3	2.2(2)	V
T_J	Junction temperature	–40	85	℃
T_{STG}	Storage temperature	–65	125	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Maximum voltage across any two pins (not including SCL or SDA) is V_{DD} + 0.3 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating temperature range unless otherwise noted.

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	1.71		1.89	V
T_J	Junction temperature	–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		LDC2112/LDC2114		UNIT
		DSBGA	TSSOP	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	81.8	105.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.4	40.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.2	50.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	3.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	18	49.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

Over operating temperature range unless otherwise noted. V_{DD} = 1.8 V, T_J = 25 °C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
V_{DD}	Supply voltage		1.71	1.8	1.89	V
I_{DDNP}	Normal power mode supply current (4 channels)(1)(2)(3)	4 channels, 40 SPS per channel, 1 ms sampling window per channel, LPWRB = V_{DD}		0.49		mA
I_{DDNP}	Normal power mode supply current (2 channels)(1)(2)	2 channels, 40 SPS per channel, 1 ms sampling window per channel, LPWRB = V_{DD}		0.26		mA
I_{DDLP}	Low power mode supply current(1)(2)	1 channel, 1.25 SPS per channel, 1 ms sampling window per channel, LPWRB = Ground		9		µA
I_{DDSB}	Standby supply current	No button active (EN = 0x00)		5	7	µA
SENSOR						
$I_{SENSOR, MAX}$	Sensor maximum current drive	Registers SENSOR*n*_CONFIG: RP*n* = 0 (4)		2.5		mA
$R_{P, MIN}$	Sensor minimum parallel resonant impedance			350		Ω
$R_{P, MAX}$	Sensor maximum parallel resonant impedance			10		kΩ
f_{SENSOR}	Sensor resonant frequency		1		30	MHz
$Q_{SENSOR, MIN}$	Sensor minimum quality factor			5		
$Q_{SENSOR, MAX}$	Sensor maximum quality factor			30		
$V_{SENSOR, PP}$	Sensor oscillation peak-to-peak voltage	Measured on the IN*n*(4) pins with reference to COM.		0.9		V
C_{IN}	Sensor input pin capacitance			17		pF
CONVERTER						
$SR_{NP, MIN}$	Minimum normal power mode scan rate(5)	LPWRB = V_{DD}	7	10	13	SPS
$SR_{NP, MAX}$	Maximum normal power mode scan rate(5)	LPWRB = V_{DD}	56	80	104	SPS
$SR_{LP, MIN}$	Minimum low power mode scan rate(5)	LPWRB = Ground	0.438	0.625	0.813	SPS
$SR_{LP, MAX}$	Maximum low power mode scan rate(5)	LPWRB = Ground	3.5	5	6.5	SPS
Resolution	Data code width			12		Bits

(1) Sensor configuration: L_{SENSOR} = 0.85 µH, C_{SENSOR} = 58 pF, Q_{SENSOR} = 11, R_P = 0.7 kΩ.
(2) I^2C communication and pull-up resistors current is not included.
(3) Four-channel supply current is applicable to LDC2114 only.
(4) The italic *n* is the channel index, i.e., *n* = 0 or 1 for LDC2112; *n* = 0, 1, 2, or 3 for LDC2114.
(5) For typical distribution of the scan rates, refer to 图 9.

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6.6 Digital Interface

Over operating temperature range unless otherwise noted. V_{DD} = 1.8 V, T_J = 25 °C. Pins: LPWRB, INTB, OUT0, OUT1, OUT2, OUT3, and ADDR.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE LEVELS						
V_{IH}	Input high voltage		0.8 × V_{DD}			V
V_{IL}	Input low voltage				0.2 × V_{DD}	V
V_{OH}	Output high voltage	I_{SOURCE} = 400 µA	0.8 × V_{DD}			V
V_{OL}	Output low voltage	I_{SINK} = 400 µA			0.2 × V_{DD}	V
I_L	Digital input leakage current		–500		500	nA

6.7 I²C Interface

			MIN	TYP	MAX	UNIT
VOLTAGE LEVELS						
V_{IH}	Input high voltage		0.7 × V_{DD}			V
V_{IL}	Input low voltage				0.3 × V_{DD}	V
V_{OL}	Output low voltage	3 mA sink current			0.2 × V_{DD}	V
HYS	Hysteresis(1)		0.05 × V_{DD}			V
I²C TIMING CHARACTERISTICS						
f_{SCL}	Clock frequency				400	kHz
t_{LOW}	Clock low time		1.3			µs
t_{HIGH}	Clock high time		0.6			µs
$t_{HD;STA}$	Hold time repeated START condition	After this period, the first clock pulse is generated.	0.6			µs
$t_{SU;STA}$	Set-up time for a repeated START condition		0.6			µs
$t_{HD;DAT}$	Data hold time		0			µs
$t_{SU;DAT}$	Data set-up time		100			ns
$t_{SU;STO}$	Set-up time for STOP condition		0.6			µs
t_{BUF}	Bus free time between a STOP and START condition		1.3			µs
$t_{VD;DAT}$	Data valid time				0.9	µs
$t_{VD;ACK}$	Data valid acknowledge time				0.9	µs
t_{SP}	Pulse width of spikes that must be suppressed by the input filter(1)				50	ns

(1) This parameter is specified by design and/or characterization and is not tested in production.

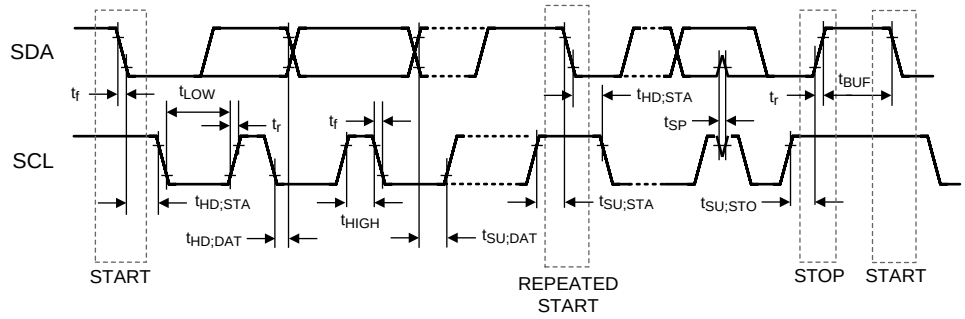


图 1. I²C Timing Diagram

6.8 Typical Characteristics

Over recommended operating conditions unless specified otherwise. V_{DD} = 1.8 V, T_J = 25 °C.

One channel enabled with a button sampling window of 1 ms unless specified otherwise.

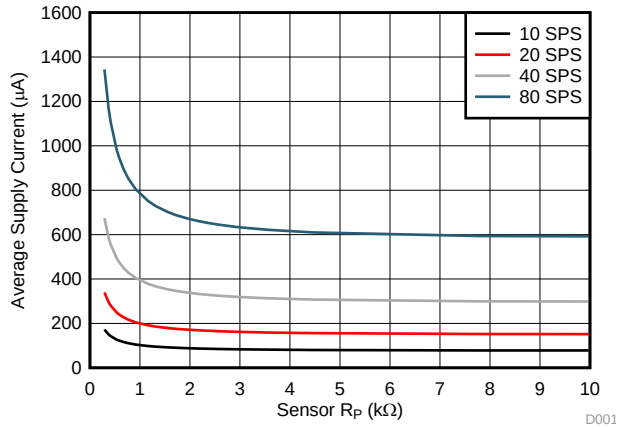


图 2. Supply Current vs Sensor R_P for Normal Power Mode. Sensor Frequency = 3.6 MHz. Four Channels Enabled.

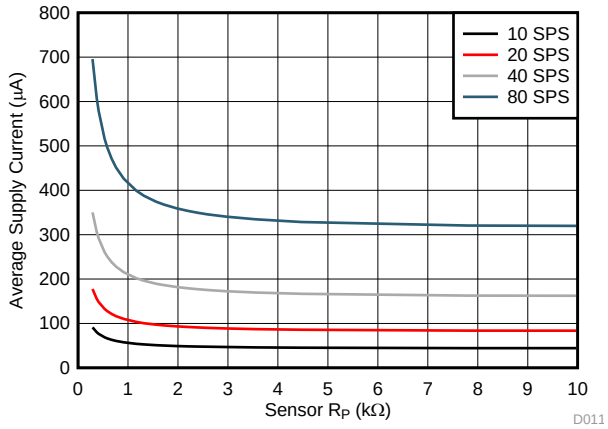


图 3. Supply Current vs Sensor R_P for Normal Power Mode. Sensor Frequency = 3.6 MHz. Two Channels Enabled.

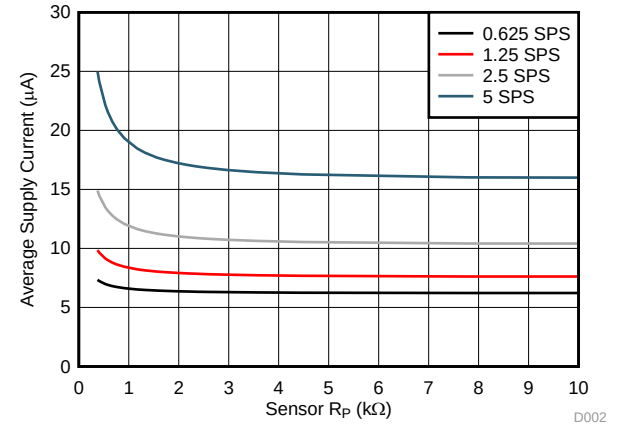


图 4. Supply Current vs Sensor R_P for Low Power Mode. Sensor Frequency = 3.6 MHz.

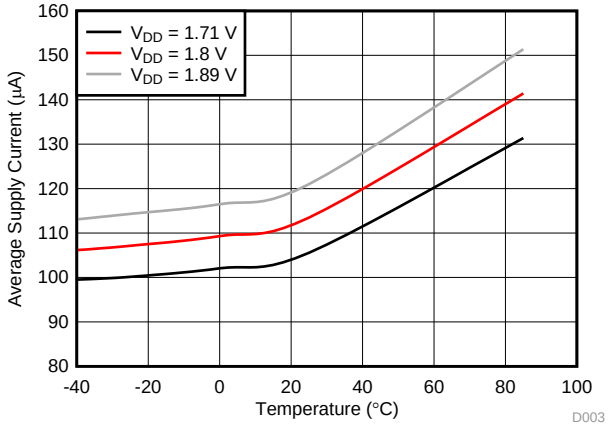


图 5. Supply Current vs Temperature. Sensor R_P = 650 Ω, Scan Rate = 40 SPS.

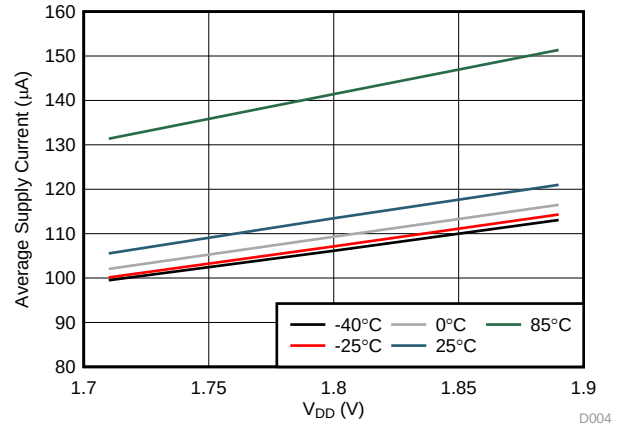


图 6. Supply Current vs V_{DD}. Sensor R_P = 650 Ω, Scan Rate = 40 SPS.

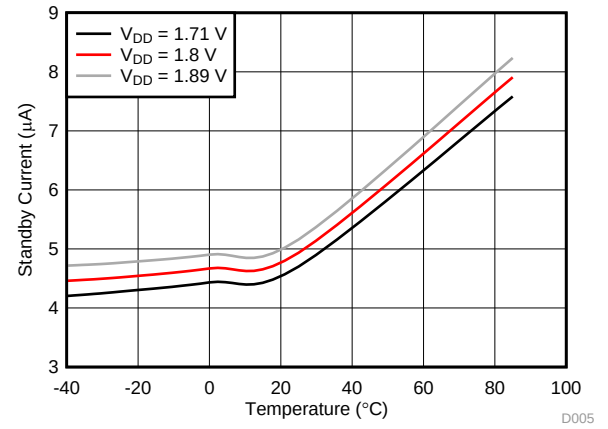


图 7. Standby Current vs Temperature

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Typical Characteristics (接下页)

One channel enabled with a button sampling window of 1 ms unless specified otherwise.

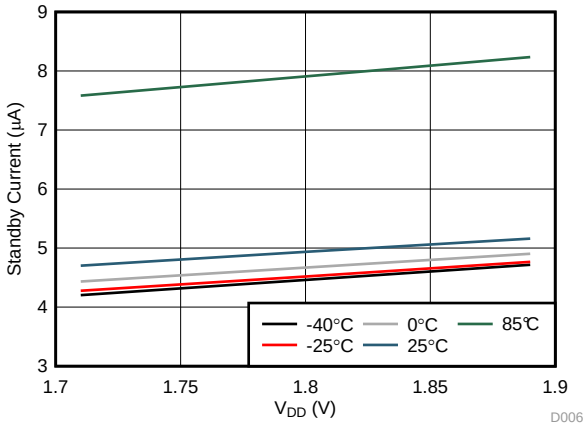


图 8. Standby Current vs V_{DD}

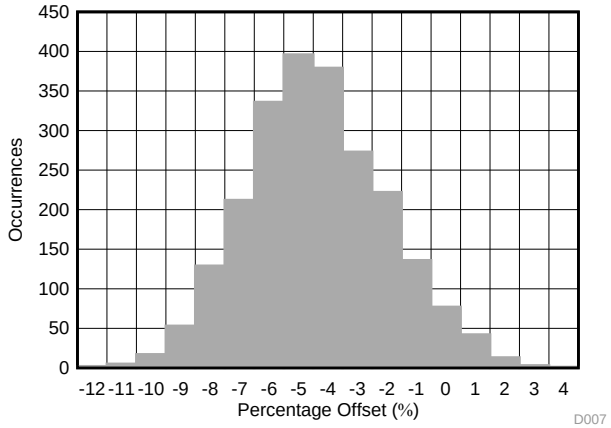


图 9. Scan Rate Distribution at 30 °C

7 Detailed Description

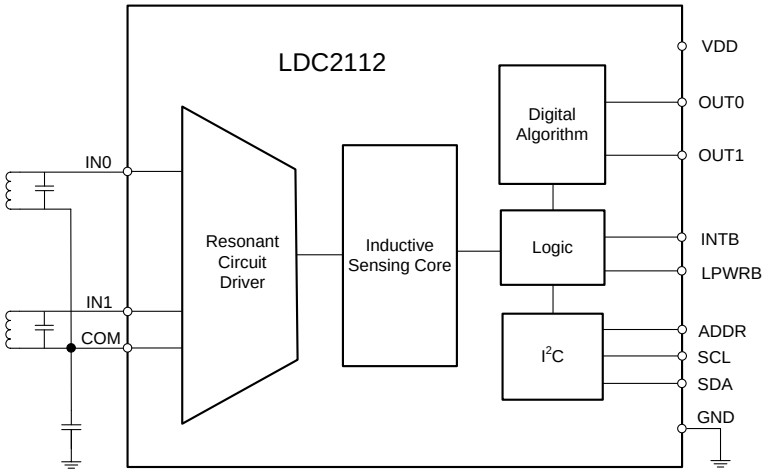
7.1 Overview

The LDC2112/LDC2114 is a multi-channel, low-noise, high-resolution inductance to digital converter (LDC) optimized for inductive touch applications. Button presses form micro-deflections in the conductive targets which cause frequency shifts in the resonant sensors. The LDC2112/LDC2114 can measure such frequency shifts and determine when button presses have occurred. With adjustable sensitivity per input channel, the LDC2112/LDC2114 can reliably operate with a wide range of physical button structures and materials. The high resolution measurement enables the implementation of force level buttons. The LDC2112/LDC2114 incorporates customizable post-processing algorithms for enhanced robustness.

The LDC2112/LDC2114 can operate in an ultra-low power mode for optimal battery life, or can be toggled into a higher scan rate for more responsive button press detection for game play or other low latency applications. The LDC2112/LDC2114 is operational from –40 °C to +85 °C with a 1.8 V ± 5% power supply voltage.

The LDC2112/LDC2114 is configured through 400 kHz I^2C. Button presses can be reported through the I^2C interface or with configurable polarity dedicated push-pull outputs. Besides the LC resonant sensors, the only external components necessary for operation are supply bypassing capacitors and a COM pin capacitor to ground.

7.2 Functional Block Diagram

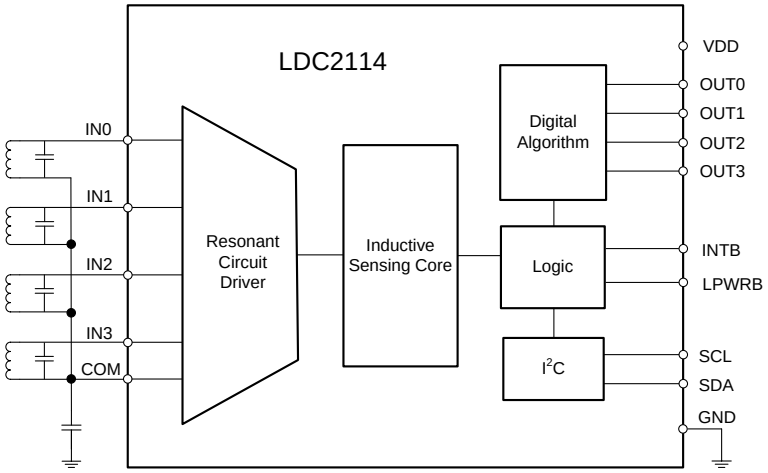


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图 10. Block Diagram of LDC2112

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Functional Block Diagram (接下页)



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图 11. Block Diagram of LDC2114

7.3 Feature Description

7.3.1 Multi-Channel and Single-Channel Operation

The LDC2112 provides two independent sensing channels; the LDC2114 provides four independent sensing channels. In the following sections, some parameters, such as DATA*n* and SENSOR*n*_CONFIG, contain a channel index *n*. In those instances, *n* = 0 or 1 for LDC2112, and *n* = 0, 1, 2, or 3 for LDC2114.

The LDC2112's two available channels are always enabled in Normal Power Mode. The LDC2112 sequentially samples both channels at the configured scan rate. Either channel can be independently enabled in Low Power Mode by setting the LPEN*n* (*n* = 0 or 1) bit fields in *Register EN (Address 0x0C)*.

Any of the LDC2114's four available channels can be independently enabled by setting the EN*n* and LPEN*n* (*n* = 0, 1, 2, or 3) bit fields in *Register EN (Address 0x0C)*. The low-power-enable bit LPEN*n* only takes effect if the corresponding EN*n* bit is also set. If only one channel is set active, the LDC2114 periodically samples the single active channel at the configured scan rate. When several channels are set active, the LDC2114 operates in multi-channel mode, and it sequentially samples the active channels at the configured scan rate. Each channel of the LDC2114 can be independently enabled in Low Power Mode and Normal Power Mode.

7.3.2 Button Output Interfaces

Button events may be reported by using two methods. The first method is to monitor the OUT*n* pins (*n* = 0, 1, 2, or 3), which are push-pull outputs and can be used as interrupts to a micro-controller. The polarities of these pins are programmable through *Register OPOL_DPOL (Address 0x1C)*. Any button press or error condition is also reported by the push-pull interrupt pin, INTB. Its polarity is configurable through *Register INTPOL (Address 0x11)*. Any assertion of INTB is cleared upon reading *Register STATUS (Address 0x00)*. Each push-pull output must be assigned to a dedicated general-purpose input pin on the micro-controller to avoid potential current fights.

The second method is by use of the LDC2112/LDC2114's I^2C interface. The *Register OUT (Address 0x01)* contains the fields OUT0, OUT1, OUT2, and OUT3, which indicate when a button press has been detected. For more advanced button press measurements, the output DATA*n* registers (*n* = 0, 1, 2, or 3, *Addresses 0x02 through 0x09*), which are 12-bit two's complements, can be retrieved for all active buttons, and processed on a micro-controller. A valid button push is represented by a positive value. The polarity is configurable in *Register OPOL_DPOL (Address 0x1C)*. The DATA*n* values can be used to implement multi-level buttons, where the data value is correlated to the amount of force applied to the button.

Feature Description (接下页)

7.3.3 Programmable Button Sensitivity

The GAIN*n* registers (Addresses *0x0E*, *0x10*, *0x12*, and *0x14*) enable sensitivity enhancement of individual buttons to ensure consistent behavior of different mechanical structures. The sensitivity has a 64-level gain factor for a normalized gain between 1 and 232. Each gain step increases the gain by an average of 9%.

The gain required for an application is primarily determined by the mechanical rigidity of each individual button. The individual gain steps are listed in the *Gain Table*.

7.3.4 Baseline Tracking

The LDC2112/LDC2114 incorporates a baseline tracking algorithm to automatically compensate for any slow change in the sensor output caused by environmental variations, such as temperature drift. The baseline tracking is configured independently for Normal Power Mode and Low Power Mode. For more information, refer to *Tracking Baseline*.

7.3.5 Integrated Button Algorithms

The LDC2112/LDC2114 features several algorithms that can mitigate false button detections due to mechanical non-idealities. The algorithms look for correlated button responses, for example, similar or opposite responses between two neighboring buttons, to determine if there is any undesirable mechanical crosstalk. For more information, refer to *Mitigating False Button Detections*.

7.3.6 I^2C Interface

The LDC2112/LDC2114 features an I^2C Interface that can be used to program the internal registers and read channel data. Before reading the OUT (Address 0x01) or channel DATA*n* (*n* = 0, 1, 2 or 3, Addresses 0x02 through 0x05) registers, the user should always read *Register STATUS (Address 0x00)* first to lock the data. The LDC2112/LDC2114 supports burst mode with auto-incrementing register addresses.

For the write sequence, there is a special handshake process that has to take place to ensure data integrity. The sequence of register write is illustrated as follows:

- Set CONFIG_MODE (*Register RESET, Address 0x0A*) bit = 1 to start the register write session
- Poll for RDY_TO_WRITE (*Register STATUS, Address 0x00*) bit = 1
- I^2C write to configure registers
- Set CONFIG_MODE (*Register RESET, Address 0x0A*) bit = 0 to terminate the register write session

After CONFIG_MODE is de-asserted, the new scan cycle will start in less than 1 ms. The waveform of the above process is shown in 图 12.

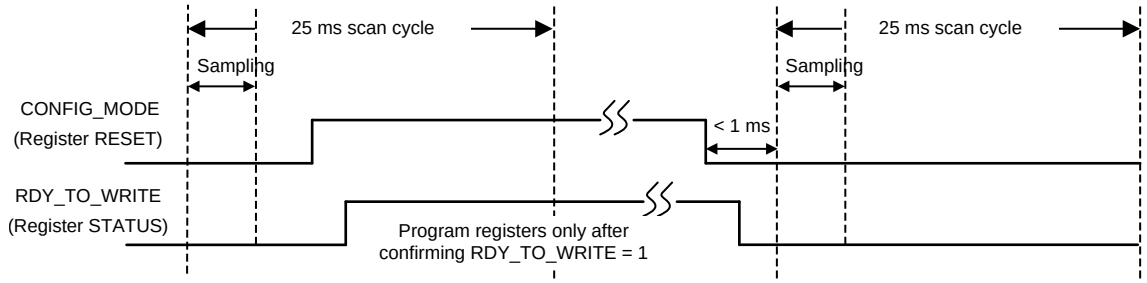


图 12. Timing Diagram Representing the States of the CONFIG_MODE and RDY_TO_WRITE Bits for an I^2C Write Handshake

7.3.6.1 Selectable I^2C Address (LDC2112 Only)

The LDC2112 provides an I^2C address select pin, ADDR. Connecting this pin to ground will set the LDC2112 I^2C address to 0x2A. Connecting ADDR to V_{DD} will set the LDC2112 I^2C address to 0x2B.

The LDC2114 has a fixed I^2C address of 0x2A.

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Feature Description (接下页)

7.3.6.2 I²C Interface Specifications

The maximum speed of the I²C interface is 400 kHz. This sequence uses the standard I²C 7-bit slave address followed by an 8-bit pointer to set the register address. For both write and read, the address pointer will auto-increment as long as the master acknowledges.

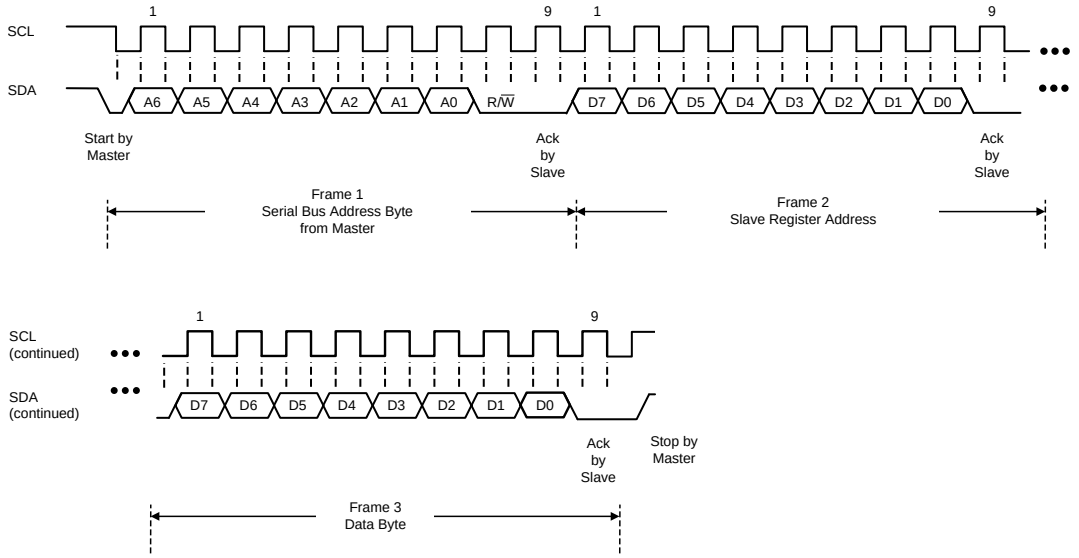


图 13. I²C Sequence of Writing a Single Register

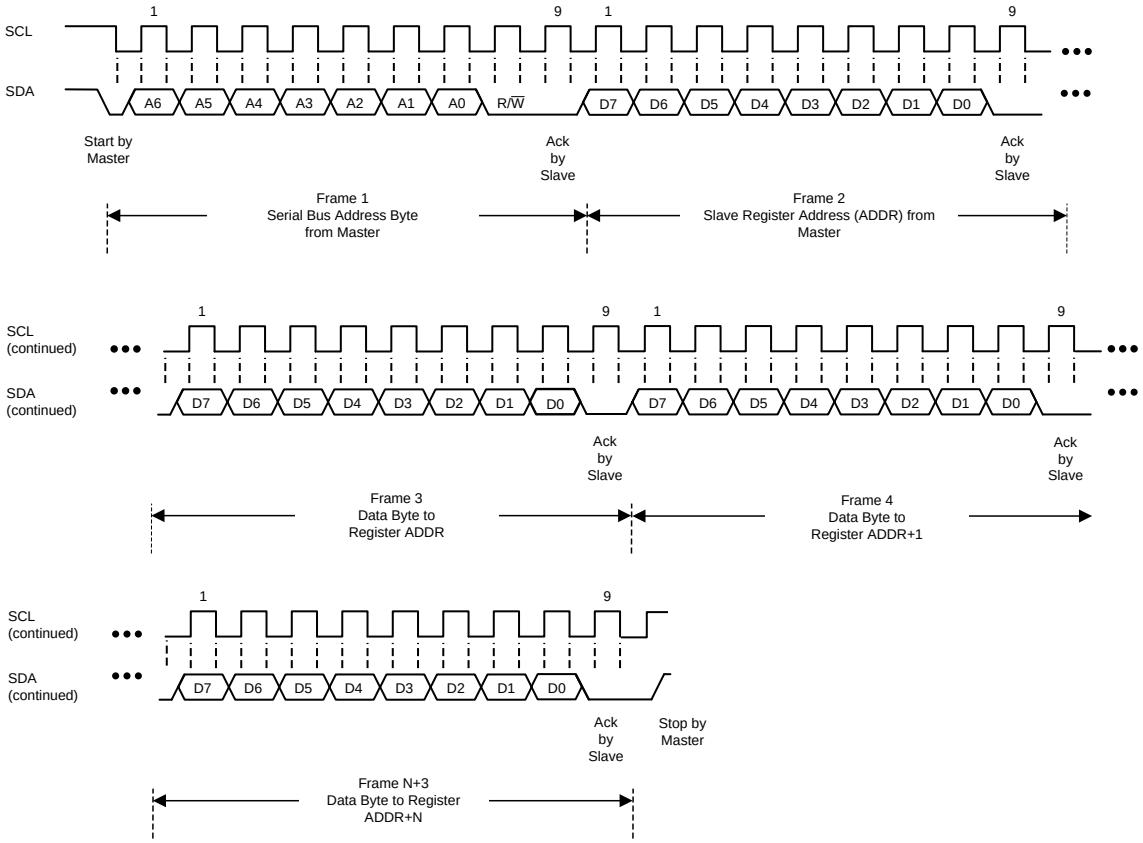


图 14. I²C Sequence of Writing Consecutive Registers

Feature Description (接下页)

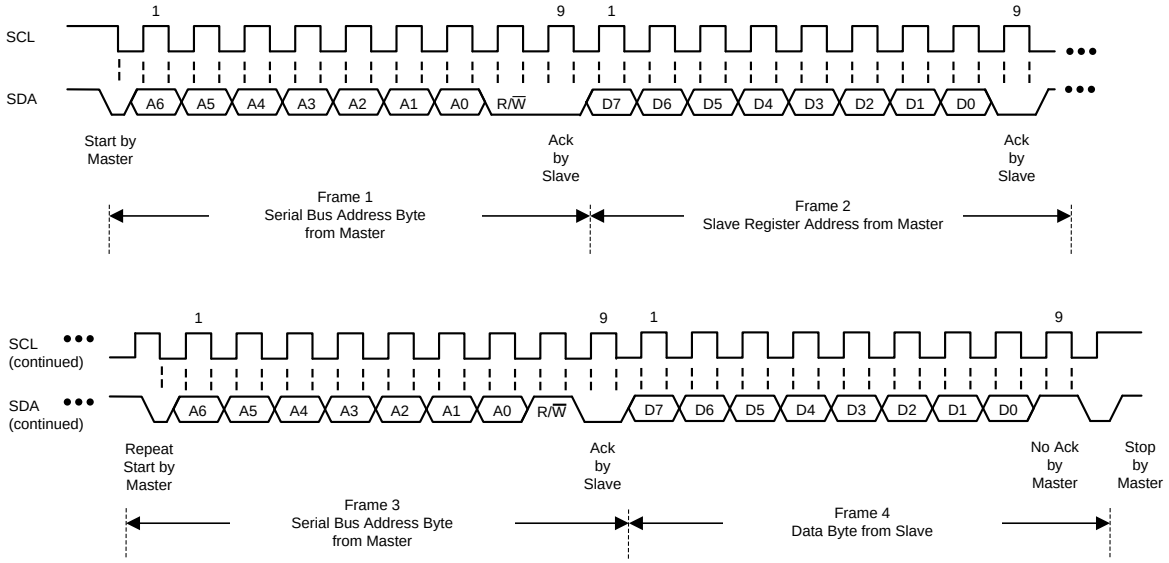


图 15. I²C Sequence of Reading a Single Register

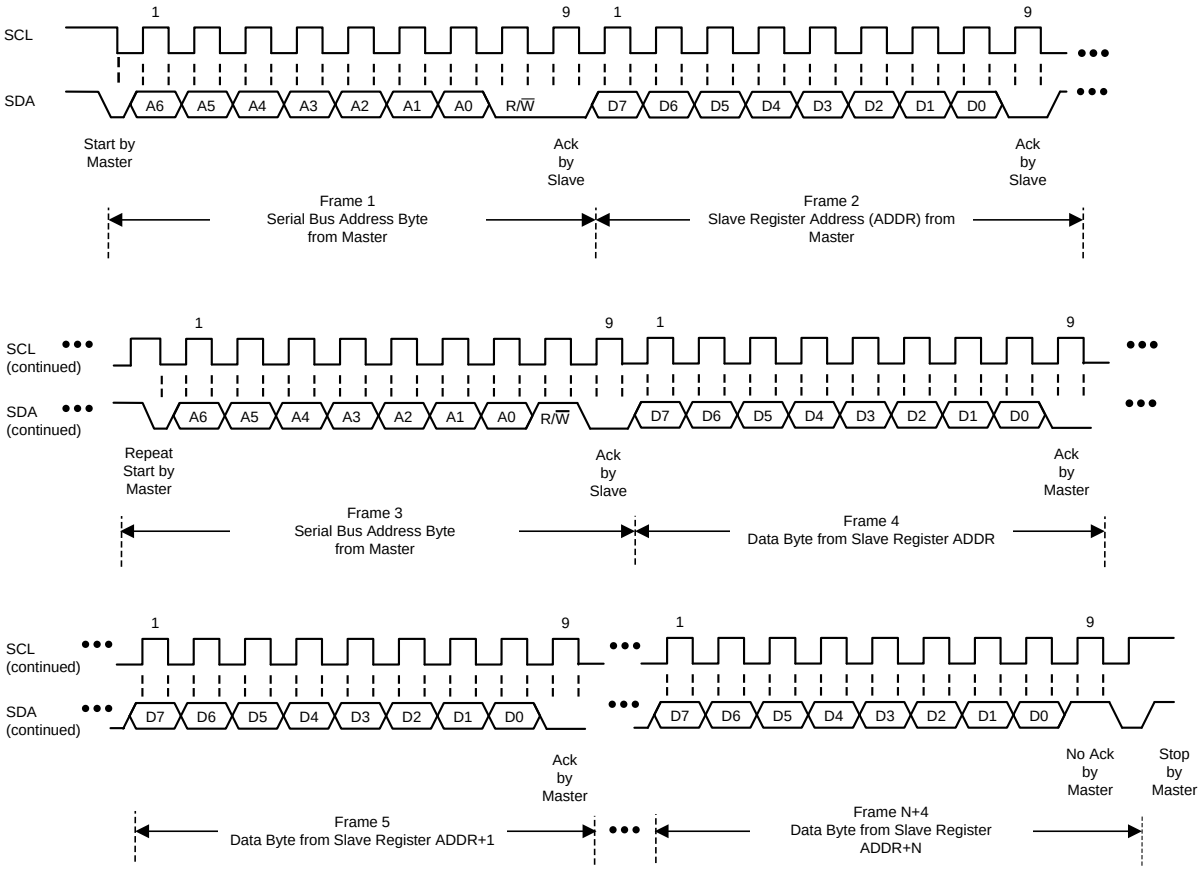


图 16. I²C Sequence of Reading Consecutive Registers

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Feature Description (接下页)

7.3.6.3 I²C Bus Control

The LDC2112/LDC2114 cannot drive the I²C clock (SCL), i.e. it does not support clock stretching. In the unlikely event where the SCL is stuck LOW, power cycle any device that is holding the SCL to activate its internal Power-On Reset (POR) circuit. If the LDC is connected to the same power supply as that device, there will be about 66 ms set-up time before the LDC becomes active again. For more information, refer to *Defining Power-On Timing*. If the data line (SDA) is stuck LOW, the I²C master should send nine clock pulses. The device that is holding the bus LOW should release it sometime within those nine clocks. If not, then power cycle to clear the bus.

The LDC2112/LDC2114 has built-in monitors to check that the device is currently working. In the unlikely event of a device fault, the device state will be reset internally, and all the registers will be reset with default settings. For system robustness, it is recommended to check the value of a modified register periodically to monitor the device status and reload the register settings if needed.

7.4 Device Functional Modes

The LDC2112/LDC2114 supports two power modes of operation, a Normal Power Mode for active sampling at 10, 20, 40, or 80 SPS, and a Low Power Mode for reduced current consumption at 0.625, 1.25, 2.5, or 5 SPS. Refer to *Configuring Button Scan Rate* for details.

7.4.1 Normal Power Mode

When the LPWRB input pin is set to V_{DD}, all enabled channels operate in Normal Power Mode. Each channel can be enabled independently through *Register EN (Address 0x0C)*. For the electrical specification of Normal Power Mode Scan Rate, refer to *Electrical Characteristics*.

7.4.2 Low Power Mode

When the LPWRB input pin is set to Ground, only the low-power-enabled channels are active. Each channel can be enabled independently to operate in Low Power Mode through *Register EN (Address 0x0C)*. For a channel to operate in the Low Power Mode, both the LPEN*n* and EN*n* bits (*n* is the channel index) must be set to 1. The Low Power Mode allows for energy-saving monitoring of button activity. In this mode, the device is in an inactive power-saving state for the majority of the time. Lower scan rates correspond to lower current consumption. In addition, the individual button sampling window should be set to the lowest effective setting (this is system dependent, but typically 0.8 to 1 ms). For the electrical specification of the configurable Low Power Mode Scan Rate, refer to *Electrical Characteristics*.

If a channel is operational in both Low Power Mode and Normal Power Mode, it is recommended to toggle the LPWRB pin only after the button associated with that channel is released.

7.4.3 Configuration Mode

Before configuring any register settings, the device must be put into the configuration mode first. Setting CONFIG_MODE = 1 through *Register RESET (Address 0x0A)* stops data conversion and holds the device in configuration mode. Any device configuration changes can then be made. The current consumption in this mode is typically 0.3 mA. After all changes have been written, set CONFIG_MODE = 0 for normal operation. Refer to *I²C Interface* for more information.

7.5 Register Maps

Registers indicated with Reserved must be written only with indicated values. Improper device operation may occur otherwise.

表 1. Register List

ADDRESS	NAME	DEFAULT VALUE	DESCRIPTION
0x00	STATUS	0x00	Device status
0x01	OUT	0x00	Channel output logic states
0x02	DATA0_LSB	0x00	The lower 8 bits of the Button 0 data (Two's complement)
0x03	DATA0_MSB	0x00	The upper 4 bits of the Button 0 data (Two's complement)
0x04	DATA1_LSB	0x00	The lower 8 bits of the Button 1 data (Two's complement)

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Register Maps (接下页)

表 1. Register List (接下页)

ADDRESS	NAME	DEFAULT VALUE	DESCRIPTION
0x05	DATA1_MSB	0x00	The upper 4 bits of the Button 1 data (Two's complement)
0x06	DATA2_LSB	0x00	The lower 8 bits of the Button 2 data (Two's complement)
0x07	DATA2_MSB	0x00	The upper 4 bits of the Button 2 data (Two's complement)
0x08	DATA3_LSB	0x00	The lower 8 bits of the Button 3 data (Two's complement)
0x09	DATA3_MSB	0x00	The upper 4 bits of the Button 3 data (Two's complement)
0x0A	RESET	0x00	Reset device and register configurations
0x0B	RESERVED	0x00	Reserved. Set to 0x00
0x0C	EN	0x10 (LDC2112) 0x1F (LDC2114)	Enable channels and low power modes
0x0D	NP_SCAN_RATE	0x01	Normal Power Mode scan rate
0x0E	GAIN0	0x28	Gain for Channel 0 sensitivity adjustment
0x0F	LP_SCAN_RATE	0x02	Low Power Mode scan rate
0x10	GAIN1	0x28	Gain for Channel 1 sensitivity adjustment
0x11	INTPOL	0x01	Interrupt polarity
0x12	GAIN2	0x28	Gain for Channel 2 sensitivity adjustment
0x13	LP_BASE_INC	0x05	Low power base increment
0x14	GAIN3	0x28	Gain for Channel 3 sensitivity adjustment
0x15	NP_BASE_INC	0x03	Normal power base increment
0x16	BTPAUSE_MAXWIN	0x00	Baseline tracking pause and Max-win
0x17	LC_DIVIDER	0x03	LC oscillation frequency divider
0x18	HYST	0x08	Hysteresis for threshold
0x19	TWIST	0x00	Anti-twist
0x1A	COMMON_DEFORM	0x00	Anti-common and anti-deformation
0x1B	RESERVED	0x00	Reserved. Set to 0x00
0x1C	OPOL_DPOL	0x0F	Output polarity
0x1D	RESERVED	0x00	Reserved. Set to 0x00
0x1E	CNTSC	0x55	Counter scale
0x1F	RESERVED	0x00	Reserved. Set to 0x00
0x20	SENSOR0_CONFIG	0x04	Sensor 0 cycle count, frequency, R_P range
0x21	RESERVED	0x00	Reserved. Set to 0x00
0x22	SENSOR1_CONFIG	0x04	Sensor 1 cycle count, frequency, R_P range
0x23	RESERVED	0x00	Reserved. Set to 0x00
0x24	SENSOR2_CONFIG	0x04	Sensor 2 cycle count, frequency, R_P range
0x25	FTF0	0x02	Sensor 0 fast tracking factor
0x26	SENSOR3_CONFIG	0x04	Sensor 3 cycle count, frequency, R_P range
0x27	RESERVED	0x00	Reserved. Set to 0x00
0x28	FTF1_2	0x50	Sensors 1 and 2 fast tracking factors
0x29	RESERVED	0x00	Reserved. Set to 0x00
0x2A	RESERVED	0x00	Reserved. Set to 0x00
0x2B	FTF3	0x01	Sensor 3 fast tracking factor
0xFC	MANUFACTURER_ID_LSB	0x49	Manufacturer ID lower byte
0xFD	MANUFACTURER_ID_MSB	0x54	Manufacturer ID upper byte
0xFE	DEVICE_ID_LSB	0x01 (LDC2112) 0x00 (LDC2114)	Device ID lower byte
0xFF	DEVICE_ID_MSB	0x20	Device ID upper byte

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7.5.1 Individual Register Listings

Fields indicated with 'Reserved' must be written only with indicated values. Improper device operation may occur otherwise. The R/W column indicates the Read-Write status of the corresponding field. An 'R/W' entry indicates read and write capability, an 'R' indicates read-only, and a 'W' indicates write-only.

Before reading the OUT (Address 0x01) or channel DATA*n* registers (*n* = 0, 1, 2, or 3, Addresses 0x02 through 0x09), the user should always read the STATUS register (Address 0x00) first to lock the data. The LDC2112/LDC2114 supports burst mode with auto-incrementing register addresses.

表 2. Register STATUS – Address 0x00

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	OUT_STATUS	R	0	**Output Status** Logic OR of output bits from *Register OUT (Address 0x01)*. This field is cleared by reading this register.
6	CHIP_READY	R	1	**Chip Ready Status** b0: Chip not ready after internal reset. b1: Chip ready after internal reset.
5	RDY_TO_WRITE	R	0	**Ready to Write** Indicates if registers are ready to be written. See *I^2C Interface* for more information. b0: Registers not ready. b1: Registers ready.
4	MAXOUT	R	0	**Maximum Output Code** Indicates if any channel output data reaches the maximum value (+0x7FF or –0x800). Cleared by a read of the status register. b0: No maximum output code. b1: Maximum output code.
3	FSM_WD	R	0	**Finite-State Machine Watchdog Error** Reports an error has occurred and conversions have been halted. Cleared by a read of the status register. b0: No error in finite-state machine. b1: Error in finite-state machine.
2	LC_WD	R	0	**LC Sensor Watchdog Error** Reports an error when any LC oscillator fails to start. Cleared by a read of the status register. b0: No error in LC oscillator initialization. b1: Error in LC oscillator initialization.
1	TIMEOUT	R	0	**Button Timeout** Reports when any button is asserted for more than 50 seconds. Cleared by a read of the status register. b0: no timeout error. b1: timeout error.
0	REGISTER_FLAG	R	0	**Register Integrity Flag** Reports if any register's value has an unexpected change. Cleared by a read of the status register. b0: No unexpected register change. b1: Unexpected register change.

表 3. Register OUT – Address 0x01

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:4	RESERVED	R	0000	Reserved. Set to b0000.
3	OUT3	R	0	**Output Logic State for Channel 3 (LDC2114 Only)** b0: No button press detected on Channel 3. b1: Button press detected on Channel 3.
2	OUT2	R	0	**Output Logic State for Channel 2 (LDC2114 Only)** b0: No button press detected on Channel 2. b1: Button press detected on Channel 2.
1	OUT1	R	0	**Output Logic State for Channel 1** b0: No button press detected on Channel 1. b1: Button press detected on Channel 1.
0	OUT0	R	0	**Output Logic State for Channel 0** b0: No button press detected on Channel 0. b1: Button press detected on Channel 0.

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表 4. Register DATA0_LSB – Address 0x02

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:0	DATA0[7:0]	R	0000 0000	The lower 8 bits of Channel 0 data (Two's complement).

表 5. Register DATA0_MSB – Address 0x03

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:4	RESERVED	R	0000	Reserved.
3:0	DATA0[11:8]	R	0000	The upper 4 bits of Channel 0 data (Two's complement).

表 6. Register DATA1_LSB – Address 0x04

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:0	DATA1[7:0]	R	0000 0000	The lower 8 bits of Channel 1 data (Two's complement).

表 7. Register DATA1_MSB – Address 0x05

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:4	RESERVED	R	0000	Reserved.
3:0	DATA1[11:8]	R	0000	The upper 4 bits of Channel 1 data (Two's complement).

表 8. Register DATA2_LSB – Address 0x06

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:0	DATA2[7:0]	R	0000 0000	The lower 8 bits of Channel 2 data (Two's complement). (LDC2114 Only)

表 9. Register DATA2_MSB – Address 0x07

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:4	RESERVED	R	0000	Reserved.
3:0	DATA2[11:8]	R	0000	The upper 4 bits of Channel 2 data (Two's complement). (LDC2114 Only)

表 10. Register DATA3_LSB – Address 0x08

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:0	DATA3[7:0]	R	0000 0000	The lower 8 bits of Channel 3 data (Two's complement). (LDC2114 Only)

表 11. Register DATA3_MSB – Address 0x09

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:4	RESERVED	R	0000	Reserved.
3:0	DATA3[11:8]	R	0000	The upper 4 bits of Channel 3 data (Two's complement). (LDC2114 Only)

表 12. Register RESET – Address 0x0A

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:5	RESERVED	R/W	000	Reserved. Set to b000.
4	FULL_RESET	R/W	0	**Device Reset** b0: Normal operation. b1: Resets the device and register configurations. All registers will be returned to default values. Normal operation will not resume until STATUS:CHIP_READY = 1.
3:1	RESERVED	R/W	000	Reserved. Set to b000.
0	CONFIG_MODE	R/W	0	**Configuration Mode** b0: Normal operation. b1: Holds the device in configuration mode (no data conversion), but maintains current register configurations. Any device configuration changes should be made with this bit set to 1. After all configuration changes have been written, set this bit to 0 for normal operation.

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表 13. Register EN – Address 0x0C

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	LPEN3	R/W	0	**Channel 3 Low-Power-Enable (LDC2114 Only)** b0: Disable Channel 3 in Low Power Mode. b1: Enable Channel 3 in Low Power Mode. EN3 must also be set to 1.
6	LPEN2	R/W	0	**Channel 2 Low-Power-Enable (LDC2114 Only)** b0: Disable Channel 2 in Low Power Mode. b1: Enable Channel 2 in Low Power Mode. EN2 must also be set to 1.
5	LPEN1	R/W	0	**Channel 1 Low-Power-Enable** b0: Disable Channel 1 in Low Power Mode. b1: Enable Channel 1 in Low Power Mode. EN1 must also be set to 1.
4	LPEN0	R/W	1	**Channel 0 Low-Power-Enable** b0: Disable Channel 0 in Low Power Mode. b1: Enable Channel 0 in Low Power Mode. EN0 must also be set to 1.
3	EN3 (LDC2114)	R/W	1	**Channel 3 Enable (LDC2114 Only)** b0: Disable Channel 3. b1: Enable Channel 3.
	RESERVED (LDC2112)	R	0	Reserved. Set to b0. (LDC2112 Only)
2	EN2 (LDC2114)	R/W	1	**Channel 2 Enable (LDC2114 Only)** b0: Disable Channel 2. b1: Enable Channel 2.
	RESERVED (LDC2112)	R	0	Reserved. Set to b0. (LDC2112 Only)
1	EN1 (LDC2114)	R/W	1	**Channel 1 Enable (LDC2114 Only)** b0: Disable Channel 1. b1: Enable Channel 1.
	RESERVED (LDC2112)	R	0	Reserved. Set to b0. (LDC2112 Only) For LDC2112, Channel 1 is always enabled.
0	EN0 (LDC2114)	R/W	1	**Channel 0 Enable (LDC2114 Only)** b0: Disable Channel 0. b1: Enable Channel 0.
	RESERVED (LDC2112)	R	0	Reserved. Set to b0. (LDC2112 Only) For LDC2112, Channel 0 is always enabled.

表 14. Register NP_SCAN_RATE – Address 0x0D

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:2	RESERVED	R/W	b00 0000	Reserved. Set to b00 0000.
1:0	NPSR	R/W	01	**Normal Power Mode Scan Rate** Refer to *Configuring Button Scan Rate* for more information. b00: 80 SPS b01: 40 SPS (Default) b10: 20 SPS b11: 10 SPS

表 15. Register GAIN0 – Address 0x0E

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:6	RESERVED	R/W	00	Reserved. Set to b00.
5:0	GAIN0	R/W	b10 1000	**Gain for Channel 0** Refer to the *Gain Table* for detailed configuration.

表 16. Register LP_SCAN_RATE – Address 0x0F

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:2	RESERVED	R/W	b00 0000	Reserved. Set to b00 0000.
1:0	LPSR	R/W	10	**Low Power Mode Scan Rate** Refer to *Configuring Button Scan Rate* for more information. b00: 5 SPS b01: 2.5 SPS b10: 1.25 SPS (Default) b11: 0.625 SPS

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表 17. Register GAIN1 – Address 0x10

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:6	RESERVED	R/W	00	Reserved. Set to b00.
5:0	GAIN1	R/W	b10 1000	**Gain for Channel 1** Refer to the *Gain Table* for detailed configuration.

表 18. Register INTPOL – Address 0x11

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:3	RESERVED	R/W	b0 0000	Reserved. Set to b0 0000.
2	INTPOL	R/W	0	**Interrupt Polarity** b0: Set INTB pin polarity to active low. b1: Set INTB pin polarity to active high.
1:0	RESERVED	R/W	01	Reserved. Set to b01.

表 19. Register GAIN2 – Address 0x12

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:6	RESERVED	R/W	00	Reserved. Set to b00.
5:0	GAIN2	R/W	b10 1000	**Gain for Channel 2 (LDC2114 Only)** Refer to the *Gain Table* for detailed configuration.

表 20. Register LP_BASE_INC – Address 0x13

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:3	RESERVED	R/W	b0 0000	Reserved. Set to b0 0000.
2:0	LPBI	R/W	b101	**Baseline Tracking Increment in Low Power Mode** Refer to *Tracking Baseline* for more information. Valid values: [b000:b111]. b101: LPBI = 5 (Default)

表 21. Register GAIN3 – Address 0x14

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:6	RESERVED	R/W	00	Reserved. Set to b00.
5:0	GAIN3	R/W	b10 1000	**Gain for Channel 3 (LDC2114 Only)** Refer to the *Gain Table* for detailed configuration.

表 22. Register NP_BASE_INC – Address 0x15

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:3	RESERVED	R/W	b0 0000	Reserved. Set to b0 0000.
2:0	NPBI	R/W	b011	**Baseline Tracking Increment in Normal Power Mode** Refer to *Tracking Baseline* for more information. Valid values: [b000:b111]. b011: NPBI = 3 (Default)

表 23. Register BTPAUSE_MAXWIN – Address 0x16

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	BTPAUSE3	R/W	0	**Baseline Tracking Pause for Channel 3 (LDC2114 Only)** Pauses baseline tracking for Channel 3 when OUT3 is asserted. Refer to *Tracking Baseline* for more information. b0: Normal baseline tracking for Channel 3 regardless of OUT3 status. (Default) b1: Pauses baseline tracking for Channel 3 when OUT3 is asserted.
6	BTPAUSE2	R/W	0	**Baseline Tracking Pause for Channel 2 (LDC2114 Only)** Pauses baseline tracking for Channel 2 when OUT2 is asserted. Refer to *Tracking Baseline* for more information. b0: Normal baseline tracking for Channel 2 regardless of OUT2 status. (Default) b1: Pauses baseline tracking for Channel 2 when OUT2 is asserted.

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表 23. Register BTPAUSE_MAXWIN – Address 0x16 (接下页)

BIT	FIELD	TYPE	RESET	DESCRIPTION
5	BTPAUSE1	R/W	0	**Baseline Tracking Pause for Channel 1** Pauses baseline tracking for Channel 1 when OUT1 is asserted. Refer to *Tracking Baseline* for more information. b0: Normal baseline tracking for Channel 1 regardless of OUT1 status. (Default) b1: Pauses baseline tracking for Channel 1 when OUT1 is asserted.
4	BTPAUSE0	R/W	0	**Baseline Tracking Pause for Channel 0** Pauses baseline tracking for Channel 0 when OUT0 is asserted. Refer to *Tracking Baseline* for more information. b0: Normal baseline tracking for Channel 0 regardless of OUT0 status. (Default) b1: Pauses baseline tracking for Channel 0 when OUT0 is asserted.
3	MAXWIN3	R/W	0	**Max-Win Algorithm Setting for Channel 3 (LDC2114 Only)** Refer to *Resolving Simultaneous Button Presses (Max-Win)* for more information. b0: Exclude Channel 3 from the max-win group. (Default) b1: Include Channel 3 in the max-win group.
2	MAXWIN2	R/W	0	**Max-Win Algorithm Setting for Channel 2 (LDC2114 Only)** Refer to *Resolving Simultaneous Button Presses (Max-Win)* for more information. b0: Exclude Channel 2 from the max-win group. (Default) b1: Include Channel 2 in the max-win group.
1	MAXWIN1	R/W	0	**Max-Win Algorithm Setting for Channel 1** Refer to *Resolving Simultaneous Button Presses (Max-Win)* for more information. b0: Exclude Channel 1 from the max-win group. (Default) b1: Include Channel 1 in the max-win group.
0	MAXWIN0	R/W	0	**Max-Win Algorithm Setting for Channel 0** Refer to *Resolving Simultaneous Button Presses (Max-Win)* for more information. b0: Exclude Channel 0 from the max-win group. (Default) b1: Include Channel 0 in the max-win group.

表 24. Register LC_DIVIDER – Address 0x17

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:3	RESERVED	R/W	b0 0000	Reserved. Set to b0 0000.
2:0	LCDIV	R/W	b011	**LC Oscillation Frequency Divider** The frequency divider sets the button sampling window in conjunction with SENCYC*n*. Valid values: [b000:b111]. Refer to *Programming Button Sampling Window* for more information. b011: LCDIV = 3 (Default)

表 25. Register HYST – Address 0x18

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:4	RESERVED	R/W	b0000	Reserved. Set to b0000.
3:0	HYST	R/W	b1000	**Hysteresis** Defines the hysteresis for button triggering threshold. Valid values: [b0000:b1111]. Hysteresis = HYST × 4 b1000: HYST = 8, Hysteresis = 32 (Default) Refer to *Setting Button Triggering Threshold* for more information.

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表 26. Register TWIST – Address 0x19

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:3	RESERVED	R/W	b0 0000	Reserved. Set to b0 0000.
2:0	ANTITWIST	R/W	b000	**Anti-Twist** When set to 0, the anti-twist algorithm is not enabled. When greater than 0, all buttons are enabled for the anti-twist algorithm. The validation of all buttons is void if any button's DATA is negative by a threshold. Anti-twist Threshold = ANTITWIST × 4. Refer to *Overcoming Case Twisting (Anti-Twist)* for more information.

表 27. Register COMMON_DEFORM – Address 0x1A

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	ANTICOM3	R/W	0	**Anti-Common Algorithm Setting for Channel 3 (LDC2114 Only)** Refer to *Eliminating Common-Mode Change (Anti-Common)* for more information. b0: Exclude Channel 3 from the anti-common group. (Default) b1: Include Channel 3 in the anti-common group.
6	ANTICOM2	R/W	0	**Anti-Common Algorithm Setting for Channel 2 (LDC2114 Only)** Refer to *Eliminating Common-Mode Change (Anti-Common)* for more information. b0: Exclude Channel 2 from the anti-common group. (Default) b1: Include Channel 2 in the anti-common group.
5	ANTICOM1	R/W	0	**Anti-Common Algorithm Setting for Channel 1** Refer to *Eliminating Common-Mode Change (Anti-Common)* for more information. b0: Exclude Channel 1 from the anti-common group. (Default) b1: Include Channel 1 in the anti-common group.
4	ANTICOM0	R/W	0	**Anti-Common Algorithm Setting for Channel 0** Refer to *Eliminating Common-Mode Change (Anti-Common)* for more information. b0: Exclude Channel 0 from the anti-common group. (Default) b1: Include Channel 0 in the anti-common group.
3	ANTIDFORM3	R/W	0	**Anti-Deform Algorithm Setting for Channel 3 (LDC2114 Only)** Refer to *Mitigating Metal Deformation (Anti-Deform)* for more information. b0: Exclude Channel 3 from the anti-deform group. (Default) b1: Include Channel 3 in the anti-deform group.
2	ANTIDFORM2	R/W	0	**Anti-Deform Algorithm Setting for Channel 2 (LDC2114 Only)** Refer to *Mitigating Metal Deformation (Anti-Deform)* for more information. b0: Exclude Channel 2 from the anti-deform group. (Default) b1: Include Channel 2 in the anti-deform group.
1	ANTIDFORM1	R/W	0	**Anti-Deform Algorithm Setting for Channel 1** Refer to *Mitigating Metal Deformation (Anti-Deform)* for more information. b0: Exclude Channel 1 from the anti-deform group. (Default) b1: Include Channel 1 in the anti-deform group.
0	ANTIDFORM0	R/W	0	**Anti-Deform Algorithm Setting for Channel 0** Refer to *Mitigating Metal Deformation (Anti-Deform)* for more information. b0: Exclude Channel 0 from the anti-deform group. (Default) b1: Include Channel 0 in the anti-deform group.

表 28. Register OPOL_DPOL – Address 0x1C

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	OPOL3	R/W	0	**Output Polarity for OUT3 Pin (LDC2114 Only)** b0: Active low (Default) b1: Active high
6	OPOL2	R/W	0	**Output Polarity for OUT2 Pin (LDC2114 Only)** b0: Active low (Default) b1: Active high

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表 28. Register OPOL_DPOL – Address 0x1C (接下页)

BIT	FIELD	TYPE	RESET	DESCRIPTION
5	OPOL1	R/W	0	**Output Polarity for OUT1 Pin** b0: Active low (Default) b1: Active high
4	OPOL0	R/W	0	**Output Polarity for OUT0 Pin** b0: Active low (Default) b1: Active high
3	DPOL3	R/W	1	**Data Polarity for Channel 3 (LDC2114 Only)** b0: DATA3 decreases as $f_{SENSOR3}$ increases. b1: DATA3 increases as $f_{SENSOR3}$ increases. (Default)
2	DPOL2	R/W	1	**Data Polarity for Channel 2 (LDC2114 Only)** b0: DATA2 decreases as $f_{SENSOR2}$ increases. b1: DATA2 increases as $f_{SENSOR2}$ increases. (Default)
1	DPOL1	R/W	1	**Data Polarity for Channel 1** b0: DATA1 decreases as $f_{SENSOR1}$ increases. b1: DATA1 increases as $f_{SENSOR1}$ increases. (Default)
0	DPOL0	R/W	1	**Data Polarity for Channel 0** b0: DATA0 decreases as $f_{SENSOR0}$ increases. b1: DATA0 increases as $f_{SENSOR0}$ increases. (Default)

表 29. Register CNTSC – Address 0x1E(1)

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:6	CNTSC3	R/W	01	**Counter Scale for Channel 3 (LDC2114 Only)** Refer to *Scaling Frequency Counter Output* for more information. b00: CNTSC3 = 0 b01: CNTSC3 = 1 (Default) b10: CNTSC3 = 2 b11: CNTSC3 = 3
5:4	CNTSC2	R/W	01	**Counter Scale for Channel 2 (LDC2114 Only)** Refer to *Scaling Frequency Counter Output* for more information. b00: CNTSC2 = 0 b01: CNTSC2 = 1 (Default) b10: CNTSC2 = 2 b11: CNTSC2 = 3
3:2	CNTSC1	R/W	01	**Counter Scale for Channel 1** Refer to *Scaling Frequency Counter Output* for more information. b00: CNTSC1 = 0 b01: CNTSC1 = 1 (Default) b10: CNTSC1 = 2 b11: CNTSC1 = 3
1:0	CNTSC0	R/W	01	**Counter Scale for Channel 0** Refer to *Scaling Frequency Counter Output* for more information. b00: CNTSC0 = 0 b01: CNTSC0 = 1 (Default) b10: CNTSC0 = 2 b11: CNTSC0 = 3

(1) The Counter Scale sets a scaling factor for the internal frequency counter to avoid data overflow. The formula for calculating counter scale is CNTSC*n* = LCDIV + ceiling($\log_2$ (0.0861×(SENCYC*n*+1)/$f_{SENSORn}$)), *n* = 0, 1, 2, or 3, where LCDIV and SENCYC*n* are the exponential and linear scalers that set the number of sensor oscillation cycles, $f_{SENSORn}$ is the sensor frequency in MHz.

表 30. Register SENSOR0_CONFIG – Address 0x20

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	RP0	R/W	0	**Channel 0 Sensor R_P Range Select** Set based on the actual sensor R_P physical parameter. $R_P = 1/R_S \times L/C$ where R_S is the AC series resistance in the LC resonator, L is the inductance, and C is the capacitance. Refer to *Designing Sensor Parameters* for more information. b0: 350Ω ≤ R_P ≤ 4kΩ (Default) b1: 800Ω ≤ R_P ≤ 10kΩ

表 30. Register SENSOR0_CONFIG – Address 0x20 (接下页)

BIT	FIELD	TYPE	RESET	DESCRIPTION
6:5	FREQ0	R/W	00	**Channel 0 Sensor Frequency Range Select** Refer to *Designing Sensor Parameters* for more information. b00: 1 MHz to 3.3 MHz (Default) b01: 3.3 MHz to 10 MHz b10: 10 MHz to 30 MHz b11: Reserved
4:0	SENCYC0	R/W	b0 0100	**Channel 0 Sensor Cycle Count** SENCYC0 sets the Channel 0 button sampling window in conjunction with LCDIV. Refer to *Programming Button Sampling Window* for more information.

表 31. Register SENSOR1_CONFIG – Address 0x22

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	RP1	R/W	0	**Channel 1 Sensor R_P Range Select** Set based on the actual sensor R_P physical parameter. $R_P = 1/R_S \times L/C$ where R_S is the AC series resistance in the LC resonator, L is the inductance, and C is the capacitance. Refer to *Designing Sensor Parameters* for more information. b0: 350 Ω ≤ R_P ≤ 4 kΩ (Default) b1: 800 Ω ≤ R_P ≤ 10 kΩ
6:5	FREQ1	R/W	00	**Channel 1 Sensor Frequency Range Select** Refer to *Designing Sensor Parameters* for more information. b00: 1 MHz to 3.3 MHz (Default) b01: 3.3 MHz to 10 MHz b10: 10 MHz to 30 MHz b11: Reserved
4:0	SENCYC1	R/W	b0 0100	**Channel 1 Sensor Cycle Count** SENCYC1 sets the Channel 1 button sampling window in conjunction with LCDIV. Refer to *Programming Button Sampling Window* for more information.

表 32. Register SENSOR2_CONFIG – Address 0x24

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	RP2	R/W	0	**Channel 2 Sensor R_P Range Select (LDC2114 Only)** Set based on the actual sensor R_P physical parameter. $R_P = 1/R_S \times L/C$ where R_S is the AC series resistance in the LC resonator, L is the inductance, and C is the capacitance. Refer to *Designing Sensor Parameters* for more information. b0: 350 Ω ≤ R_P ≤ 4 kΩ (Default) b1: 800 Ω ≤ R_P ≤ 10 kΩ
6:5	FREQ2	R/W	00	**Channel 2 Sensor Frequency Range Select (LDC2114 Only)** Refer to *Designing Sensor Parameters* for more information. b00: 1 MHz to 3.3 MHz (Default) b01: 3.3 MHz to 10 MHz b10: 10 MHz to 30 MHz b11: Reserved
4:0	SENCYC2	R/W	b0 0100	**Channel 2 Sensor Cycle Count (LDC2114 Only)** SENCYC2 sets the Channel 2 button sampling window in conjunction with LCDIV. Refer to *Programming Button Sampling Window* for more information.

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表 33. Register FTF0 – Address 0x25

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:3	RESERVED	R/W	b0 0000	Reserved. Set to b0 0000.
2:1	FTF0	R/W	01	**Fast Tracking Factor for Channel 0** Defines baseline tracking speed for negative values of DATA0. Refer to *Tracking Baseline* for more information. b00: FTF0 = 0 b01: FTF0 = 1 (Default) b10: FTF0 = 2 b11: FTF0 = 3
0	RESERVED	R/W	0	Reserved. Set to b0.

表 34. Register SENSOR3_CONFIG – Address 0x26

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	RP3	R/W	0	**Channel 3 Sensor R_P Range Select (LDC2114 Only)** Set based on the actual sensor R_P physical parameter. $R_P = 1/R_S \times L/C$ where R_S is the AC series resistance in the LC resonator, L is the inductance, and C is the capacitance. Refer to *Designing Sensor Parameters* for more information. b0: 350 Ω ≤ R_P ≤ 4 kΩ (Default) b1: 800 Ω ≤ R_P ≤ 10 kΩ
6:5	FREQ3	R/W	00	**Channel 3 Sensor Frequency Range Select (LDC2114 Only)** Refer to *Designing Sensor Parameters* for more information. b00: 1 MHz to 3.3 MHz (Default) b01: 3.3 MHz to 10 MHz b10: 10 MHz to 30 MHz b11: Reserved
4:0	SENCYC3	R/W	b0 0100	**Channel 3 Sensor Cycle Count (LDC2114 Only)** SENCYC3 sets the Channel 3 button sampling window in conjunction with LCDIV. Refer to *Programming Button Sampling Window* for more information.

表 35. Register FTF1_2 – Address 0x28

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:6	FTF2	R/W	01	**Fast Tracking Factor for Channel 2 (LDC2114 Only)** Defines baseline tracking speed for negative values of DATA2. Refer to *Tracking Baseline* for more information. b00: FTF2 = 0 b01: FTF2 = 1 (Default) b10: FTF2 = 2 b11: FTF2 = 3
5:4	FTF1	R/W	01	**Fast Tracking Factor for Channel 1** Defines baseline tracking speed for negative values of DATA1. Refer to *Tracking Baseline* for more information. b00: FTF1 = 0 b01: FTF1 = 1 (Default) b10: FTF1 = 2 b11: FTF1 = 3
3:0	RESERVED	R/W	b0000	Reserved. Set to b0000.

表 36. Register FTF3 – Address 0x2B

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:2	RESERVED	R/W	b00 0000	Reserved. Set to b00 0000.
1:0	FTF3	R/W	01	**Fast Tracking Factor for Channel 3 (LDC2114 Only)** Defines baseline tracking speed for negative values of DATA3. Refer to *Tracking Baseline* for more information. b00: FTF3 = 0 b01: FTF3 = 1 (Default) b10: FTF3 = 2 b11: FTF3 = 3

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表 37. Register MANUFACTURER_ID_LSB – Address 0xFC

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:0	MANUFACTURER_ID [7:0]	R	0x49	**Manufacturer ID [7:0]**

表 38. Register MANUFACTURER_ID_MSB – Address 0xFD

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:0	MANUFACTURER_ID [15:8]	R	0x54	**Manufacturer ID [15:8]**

表 39. Register DEVICE_ID_LSB – Address 0xFE

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:0	DEVICE_ID [7:0]	R	0x01 (LDC2112)	**Device ID [7:0]**
			0x00 (LDC2114)	

表 40. Register DEVICE_ID_MSB – Address 0xFF

BIT	FIELD	TYPE	RESET	DESCRIPTION
7:0	DEVICE_ID [15:8]	R	0x20	**Device ID [15:8]**

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7.5.1.1 Gain Table for Registers GAIN0, GAIN1, GAIN2, and GAIN3

表 41. GAIN*n* Bit Values in Decimal and Corresponding Normalized Gain Factors

BIT VALUE IN DECIMAL	NORMALIZED GAIN FACTOR	BIT VALUE IN DECIMAL	NORMALIZED GAIN FACTOR
0	1.0	32	16
1	1.0625	33	17
2	1.1875	34	19
3	1.3125	35	21
4	1.4375	36	23
5	1.5625	37	25
6	1.6875	38	27
7	1.8125	39	29
8	2.0	40	32
9	2.125	41	34
10	2.375	42	38
11	2.625	43	42
12	2.875	44	46
13	3.125	45	50
14	3.375	46	54
15	3.625	47	58
16	4.0	48	64
17	4.25	49	68
18	4.75	50	76
19	5.25	51	84
20	5.75	52	92
21	6.25	53	100
22	6.75	54	108
23	7.25	55	116
24	8.0	56	128
25	8.5	57	136
26	9.5	58	152
27	10.5	59	168
28	11.5	60	184
29	12.5	61	200
30	13.5	62	216
31	14.5	63	232

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8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LDC2112/LDC2114 supports multiple buttons. Each button can be configured in various ways for optimal operation.

8.1.1 Theory of Operation

An AC current flowing through an inductor will generate an AC magnetic field. If a conductive material, such as a metal object, is in close proximity to the inductor, the magnetic field will induce circulating eddy currents on the surface of the conductor. The eddy currents are a function of the distance, size, and composition of the conductor. If the conductor is deflected toward the inductor as shown in 图 17, more eddy currents will be generated.

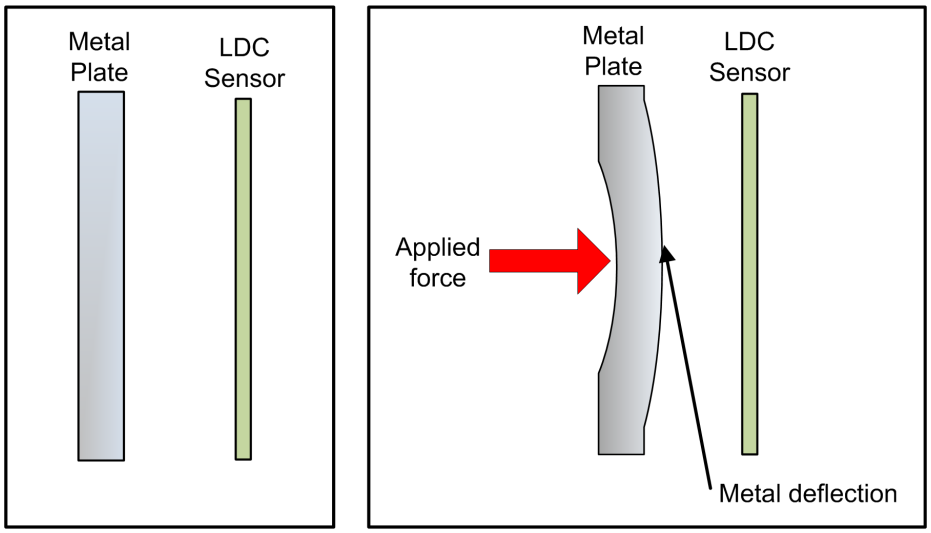


图 17. Metal Deflection

The eddy currents create their own magnetic field, which opposes the original field generated by the inductor. This effect reduces the effective inductance of the system, resulting in an increase in sensor frequency. 图 18 shows the inductance and frequency response of an example sensor with a diameter of 14 mm. As the sensitivity of an inductive sensor increases with closer targets, the conductive plate should be placed quite close to the sensor—typically 10% of the sensor diameter for circular coils. For rectangular or race-track-shaped coils, the target to sensor distance should typically be less than 10% of the shorter side of the coil.

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Application Information (接下页)

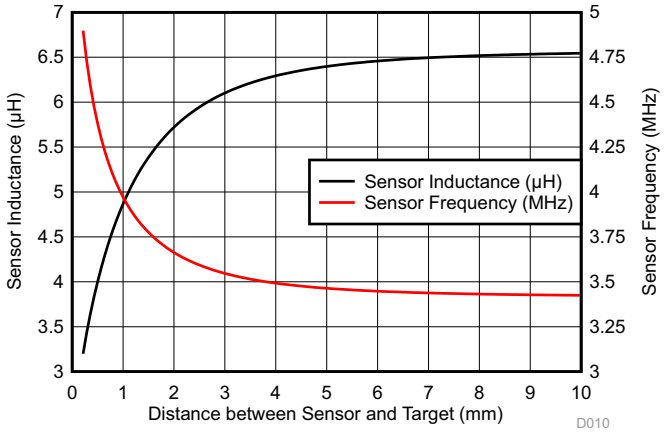


图 18. Sensor Inductance and Frequency vs Target Distance. Sensor Diameter = 14 mm

The output DATA*n* registers (Addresses 0x02 through 0x09) of the LDC2112/LDC2114 contain the processed values of the changes in sensor frequencies.

8.1.2 Designing Sensor Parameters

Each inductive touch button uses an LC resonator sensor, as illustrated in 图 19, where L is the inductor, C is the capacitor, and R_S is the AC series resistance of the sensor at the frequency of operation. The key parameters of the LC sensor include frequency, effective parallel resistance R_P, and quality factor Q. These parameters must be within the ranges as specified in the Sensor section of the *Electrical Characteristics* table. Note that the effective R_P and Q changes when the conductive target is in place.

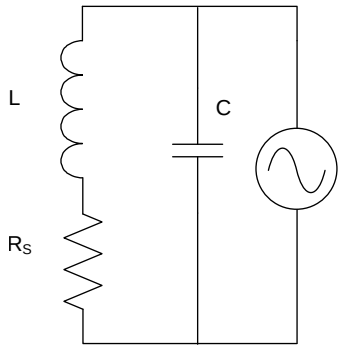


图 19. LC Resonator

The LC sensor frequency, as defined by the equation below, must be between 1 MHz and 30 MHz.

$$f_{SENSOR} = \frac{1}{2\pi\sqrt{LC}} \quad (1)$$

The sensor quality factor, as defined by the equation below, must be between 5 and 30.

$$Q_{SENSOR} = \frac{1}{R_S}\sqrt{\frac{L}{C}} \quad (2)$$

The series resistance can be represented as an equivalent parallel resistance, R_P, which is given by

$$R_P = \frac{L}{R_S C} \quad (3)$$

Application Information (接下页)

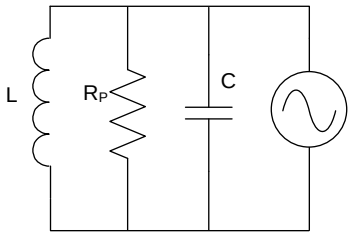


图 20. Equivalent Parallel Circuit

R_P can be viewed as the load on the sensor driver. This load corresponds to the current drive needed to maintain the oscillation amplitude. R_P must be between 350 Ω and 10 kΩ.

In summary, the LDC2112/LDC2114 requires that the sensor parameters are within the following ranges when the conductive target is present:

- 1 MHz ≤ f_{SENSOR} ≤ 30 MHz
- 5 ≤ Q ≤ 30
- 350 Ω ≤ R_P ≤ 10 kΩ

8.1.3 Setting COM Pin Capacitor

The COM pin requires a bypass capacitor to ground. The capacitor should be a low ESL, low ESR type. C_{COM} must be sized so that the following relationship is valid for all channels.

$$100 \times C_{SENSORn} / Q_{SENSORn} < C_{COM} < 1250 \times C_{SENSORn} / Q_{SENSORn} \quad (4)$$

The value of $Q_{SENSORn}$ when the sensor is at the minimum target distance should be used. The maximum acceptable value for C_{COM} is 20 nF. The C_{COM} range for a particular sensor configuration can be obtained with the Spiral_Inductor_Designer tab of the *LDC Calculations Tool*.

8.1.4 Defining Power-On Timing

The low power architecture of the LDC2112/LDC2114 makes it possible for the device to be active all the time. When not being used, the LDC2112/LDC2114 can operate in Low Power Mode with a single standby power button, which typically consumes less than 10 µA. If additional power-saving is desired, or in the rare event where a power-on reset becomes necessary (see *I^2C Interface*), the output data will become ready after 50 ms startup time, about 1 ms optional register loading time, and two sampling windows for all active channels. The power-on timing of the LDC2112/LDC2114 is illustrated in 图 21 below.

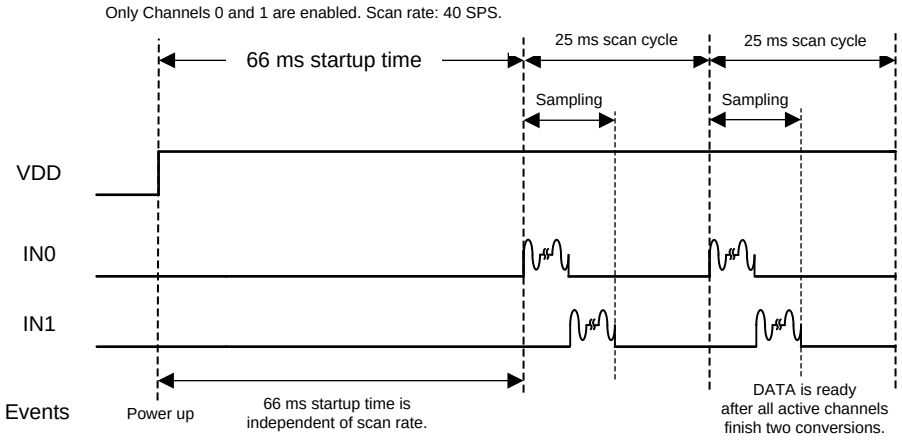


图 21. Power-On Timing

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Application Information (接下页)

8.1.5 Configuring Button Scan Rate

The LDC2112/LDC2114 periodically samples all active channels at the selected scan rate. The device can operate at eight different scan rates to meet various power consumption requirements, where a lower scan rate achieves lower power consumption. In Normal Power Mode, the scan rate can be programmed to 80, 40, 20, or 10 SPS through *Register NP_SCAN_RATE (Address 0x0D)*. In Low Power Mode, the scan rate can be programmed to 5, 2.5, 1.25, or 0.625 SPS through *Register LP_SCAN_RATE (Address 0x0F)*. The mode is selected by setting the LPWRB pin to VDD (Normal Power) or ground (Low Power). In either mode, each button can be independently enabled through a bit in *Register EN (Address 0x0C)*. For typical distribution of the scan rates, refer to 图 9.

表 42. Button Scan Rates

SCAN RATE (SPS)	LPSR (0x0F) SETTING	NPSR (0x0D) SETTING	LPWRB PIN SETTING
0.625	b11	Not Applicable	Ground
1.25	b10	Not Applicable	Ground
2.5	b01	Not Applicable	Ground
5	b00	Not Applicable	Ground
10	Not Applicable	b11	V_{DD}
20	Not Applicable	b10	V_{DD}
40	Not Applicable	b01	V_{DD}
80	Not Applicable	b00	V_{DD}

8.1.6 Programming Button Sampling Window

The button sampling window is the actual duration per scan cycle for active data sampling of the sensor frequency. It is programmed with the exponential parameter, LCDIV, in *Register LC_DIVIDER (Address 0x17)*, and the individual linear sensor cycle counter SENCYC*n* (*n* = 0, 1, 2, or 3) in Registers SENSOR*n*_CONFIG (*n* = 0, 1, 2, or 3, Addresses *0x20*, *0x22*, *0x24*, *0x26*). For most touch button applications, the button sampling window should be set to between 1 ms and 8 ms. The recommended minimum sensor conversion time is 1 ms. Longer conversion time can be used to achieve better signal-to-noise ratio if needed. If multiple channels are enabled, the active channels will sample sequentially, as illustrated in 图 22.

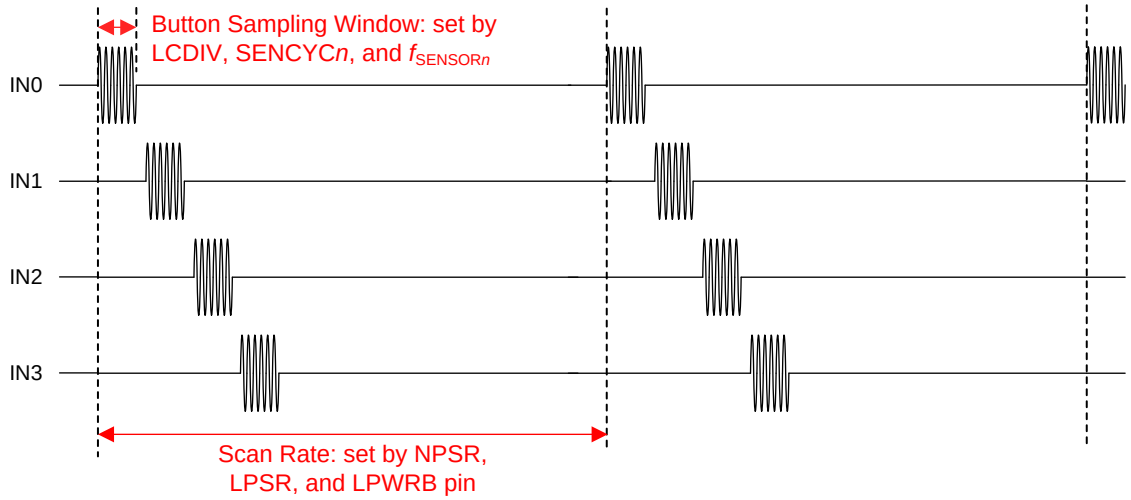


图 22. Configurable Scan Rate and Button Sampling Window

The LDC2112/LDC2114 is designed to work with LC resonator sensors with oscillation frequencies ranging from 1 MHz to 30 MHz. The exact definition of the button sampling window is given by the equation below.

$$\text{Button Sampling Window} = \frac{\text{Number of Sensor Oscillation Cycles}}{\text{Sensor Frequency}}$$

$$t_{SAMPLE} = \frac{128 \times (SENCYC n + 1) \times 2^{LCDIV}}{f_{SENSOR n}}, n = 0, 1, 2, \text{or } 3 \quad (5)$$

where:

- t_{SAMPLE} is the button sampling window in µs,
- SENCYC*n* and LCDIV are the linear and exponential scalers that set the number of sensor oscillation cycles, and
- $f_{SENSOR n}$ is the sensor frequency in MHz.

In the equation above, LCDIV (0 to 7, default 3) is the exponential LC divider that sets the approximate ranges for all channels, and SENCYC*n* (0 to 31, default 4) is the linear sensor cycle scaler that fine-tunes each individual channel. Together they set the number of sensor oscillation cycles used to determine the button sampling window.

For example, if the LC sensor frequency is 9.2 MHz, and it is desirable to get 1 ms button sampling window, then this can be achieved by setting SENCYC*n* = 17 and LCDIV = 2.

Alternatively, from the button sampling window and sensor frequency, the LCDIV can be read off from *图 23*. For example, 1 ms button sampling window and 9.2 MHz sensor frequency intersect at the region where LCDIV = 2. Then SENCYC*n* can be calculated accordingly.

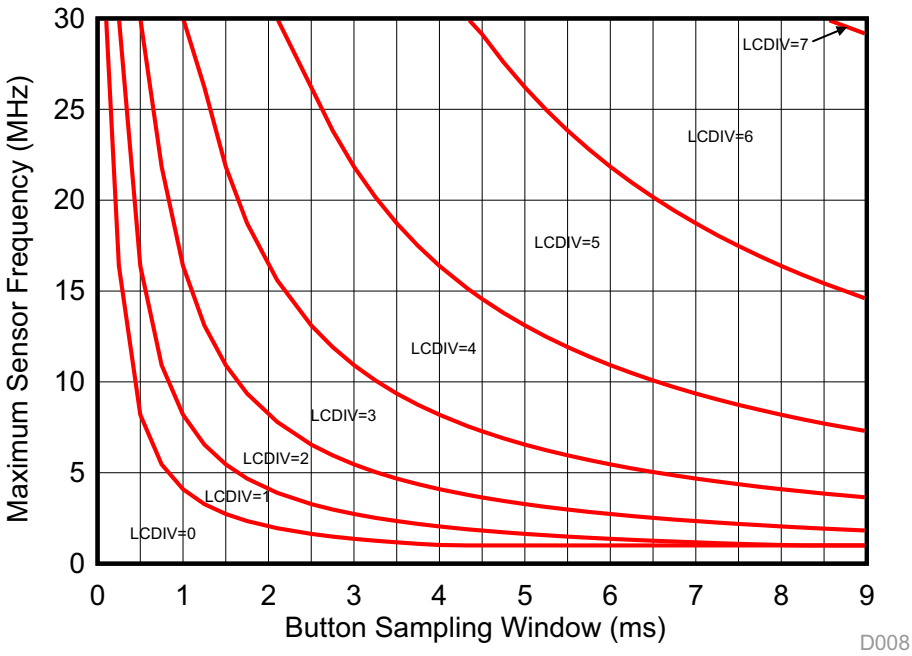


图 23. LCDIV as a Function of Sensor Frequency and Button Sampling Window

8.1.7 Scaling Frequency Counter Output

The LDC2112/LDC2114 requires this internal frequency counter scaler to be set based on the button sampling window to avoid data overflow. The scaler in *Register CNTSC (Address 0x1E)* must be set by the following formula:

$$CNTSC n = LCDIV + \text{ceiling}\left(\log_2 \frac{0.0861 \times (SENCYC n + 1)}{f_{SENSOR n}} \right), (n = 0, 1, 2, \text{or } 3)$$

where:

- CNTSC*n* is the internal frequency counter scaler,
- SENCYC*n* and LCDIV are the linear and exponential scalers that set the number of sensor oscillation cycles, and
- $f_{SENSOR n}$ is the sensor frequency in MHz.

(6)

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8.1.8 Setting Button Triggering Threshold

Every material shows some hysteresis when it deforms then returns to the original state. The amount of hysteresis is a function of material properties and physical parameters, such as size and thickness. This feature modifies the hysteresis of the button signal threshold according to different materials and various button shapes and sizes. Hysteresis can be programmed in *Register HYST (Address 0x18)*. By default, the button triggering hysteresis is set to 32. The nominal button triggering threshold is 128. With hysteresis, the effective on-threshold is 128 + 32 = 160. This means if the DATA*n* (*n* = 0, 1, 2, or 3) reaches 160, the LDC considers that as a button press. When the DATA*n* decreases to 128 – 32 = 96, the LDC considers the button to be released.

$$\text{Threshold}_{ON} = 128 + \text{Hysteresis} \quad (7)$$

$$\text{Threshold}_{OFF} = 128 - \text{Hysteresis} \quad (8)$$

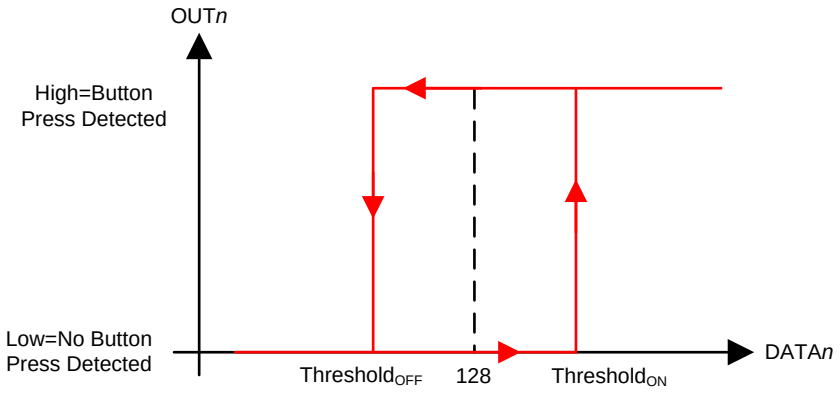


图 24. Button Triggering Threshold with Hysteresis. Output Polarity: Active High

8.1.9 Tracking Baseline

The LDC2112/LDC2114 automatically tracks slow changes in the baseline signal and compensates for environmental drifts and variations. In Normal Power Mode, the effective baseline increment per scan cycle ($BINC_{NP}$) can be determined by 公式 9:

$$BINC_{NP} = \frac{2^{NPBI}}{72} \quad (9)$$

where:

- NPBI is the Normal Power Baseline Increment index that can be configured in *Register NP_BASE_INC (Address 0x15)*.

In Low Power Mode, the effective baseline increment per scan cycle ($BINC_{LP}$) can be determined by 公式 10:

$$BINC_{LP} = \frac{2^{LPBI}}{9} \quad (10)$$

where:

- LPBI the Low Power Baseline Increment index that can be configured in *Register LP_BASE_INC (Address 0x13)*.

As a result of baseline tracking, a button press with a constant force only lasts for a finite amount of time. The duration of a button press is defined by 公式 11 (DATA*n* > Threshold_{ON}).

$$\text{Duration of Button Press} = \frac{\text{DATA}n - \text{Threshold}_{OFF}}{BINC} \quad (11)$$

where:

- Duration of Button Press is the number of scan cycles that the channel is asserted,
- DATA*n* is the button signal at the beginning of a press, and
- BINC is the baseline increment per scan cycle.

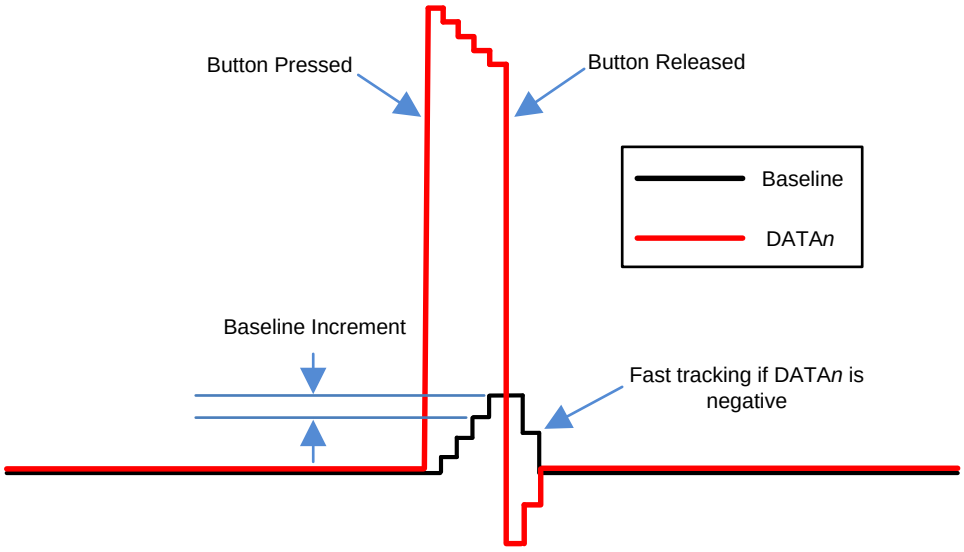


图 25. Baseline Tracking in the Presence of a Button Press

The baseline tracking for a particular channel can be paused when the channel output is asserted. This is achieved by setting the corresponding BTPAUSE bit in *Register BTPAUSE_MAXWIN (Address 0x16)* to b1.

If DATA*n* is negative, the tracking speed will be scaled by the fast tracking factor as specified in Registers *FTF0 (Address 0x25)*, *FTF1_2 (Address 0x28)*, or *FTF3 (Address 0x2B)*. The scaling factors for various FTF*n* settings are shown in 表 43.

$$BINC\ (DATAn < 0) = Fast_Tracking_Factor_n \times BINC\ (DATAn > 0) \quad (12)$$

表 43. Fast Tracking Factor Settings

FTF*n* Setting	Fast Tracking Factor
b00	1
b01	4
b10	8
b11	16

8.1.10 Mitigating False Button Detections

The LDC2112/LDC2114 offers several algorithms that can mitigate false button detections due to mechanical non-idealities associated with groups of buttons. These are listed below.

8.1.10.1 Eliminating Common-Mode Change (Anti-Common)

This algorithm eliminates false detection when a user presses the middle of two or more buttons, which could lead to a common-mode response on multiple buttons. All the buttons can be individually enabled to have this feature by programming *Register COMMON_DEFORM (Address 0x1A)*.

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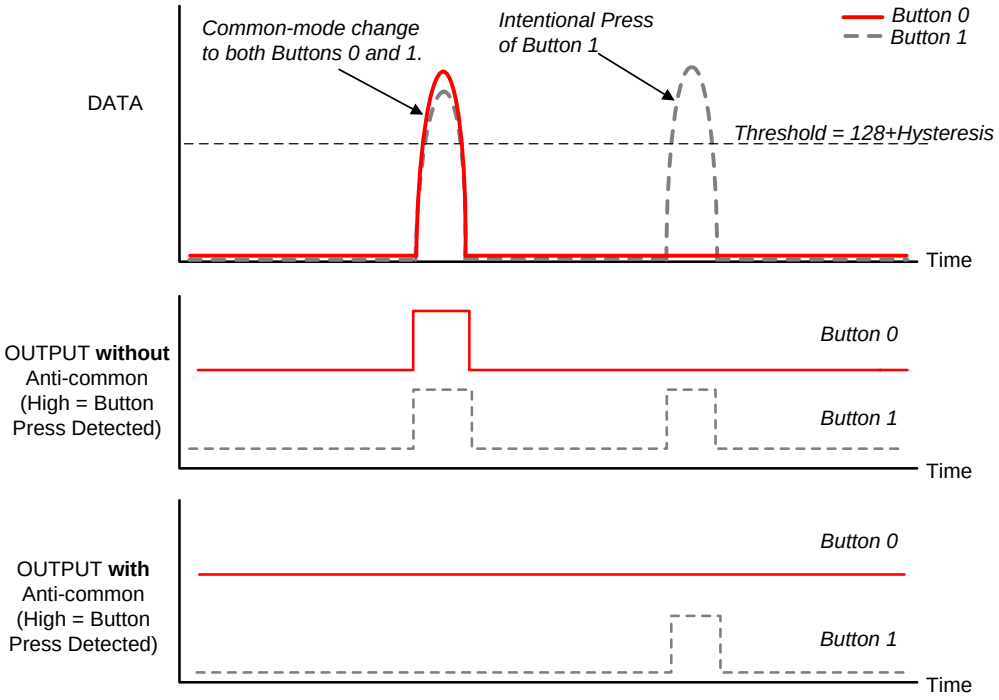


图 26. Illustration of the Anti-Common Feature

8.1.10.2 Resolving Simultaneous Button Presses (Max-Win)

This algorithm enables the system to select the button pressed with maximum force when multiple buttons are pressed at the same time. This could happen when two buttons are physically very close to each other, and pressing one causes a residual reaction on the other. Buttons can be individually enabled to join the “max-win” group by configuring *Register BTPAUSE_MAXWIN (Address 0x16)*.

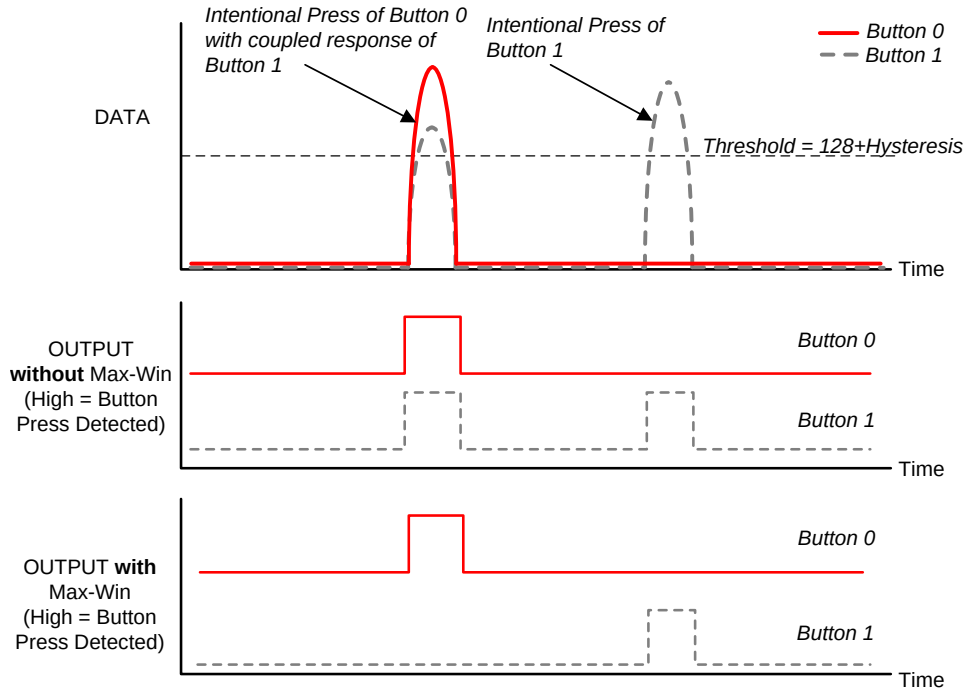


图 27. Illustration of the Max-Win Feature

8.1.10.3 Overcoming Case Twisting (Anti-Twist)

The anti-twist algorithm reduces the likelihood of false detection when the case is twisted, which could cause unintended mechanical activation of the buttons, or an opposite reaction in two adjacent buttons. When this algorithm is enabled, detection of button presses is suppressed if any button's output data is negative by a configurable threshold. The anti-twist algorithm can be enabled by configuring *Register TWIST (Address 0x19)*.

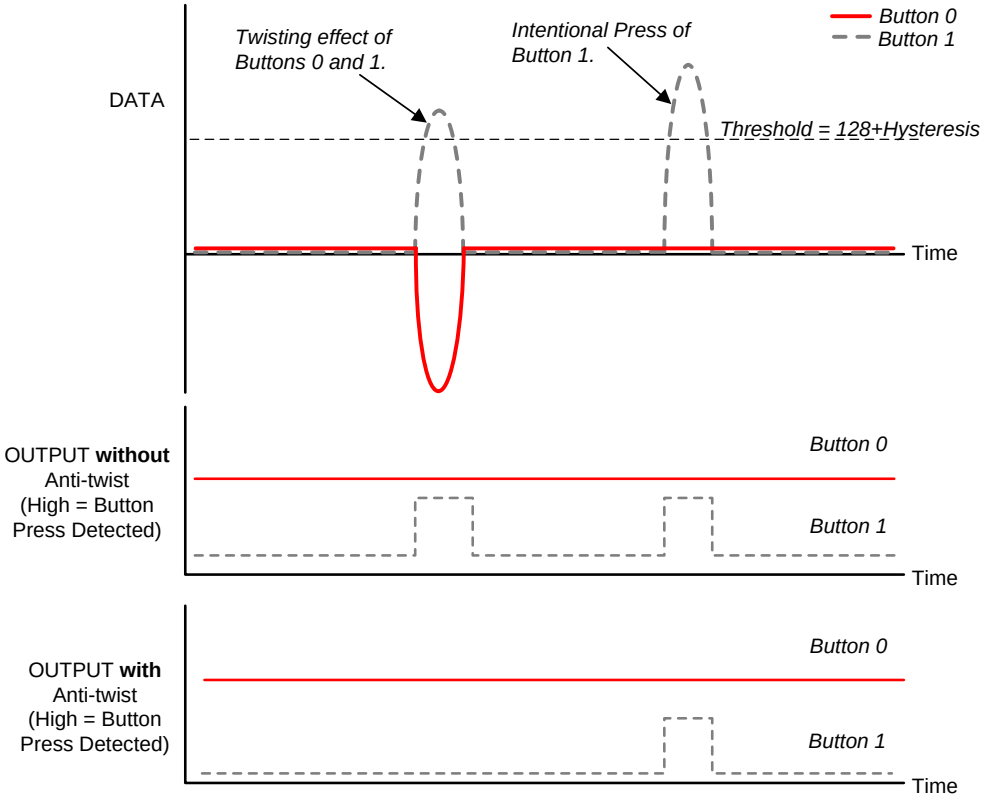


图 28. Illustration of the Anti-Twist Feature

8.1.10.4 Mitigating Metal Deformation (Anti-Deform)

This function filters changes due to metal deformation in the vicinity of one or more buttons. Such metal deformation can be accidentally caused by pressing a neighboring button that does not have sufficient mechanical isolation. The user can specify which buttons to join the anti-deform group by configuring *Register COMMON_DEFORM (Address 0x1A)*.

8.1.11 Reporting Interrupts for Button Presses and Error Conditions

INTB, the LDC2112/LDC2114 interrupt pin, is asserted when a button press or an error condition occurs. The default polarity is active low and can be configured through *Register INTPOL (Address 0x11)*.

图 29 shows the LDC2112/LDC2114 response to a single button press on Channel 0. At the end of the button sampling window following a press of Button 0, the OUT0 pin and INTB pin are asserted. The OUT_STATUS bit changes from 0 to 1, and remains so until a read of the STATUS register clears it. The OUT*n* (*n* = 0, 1, 2, or 3) and INTB pins are asserted until the end of the button sampling window following the release of the button.

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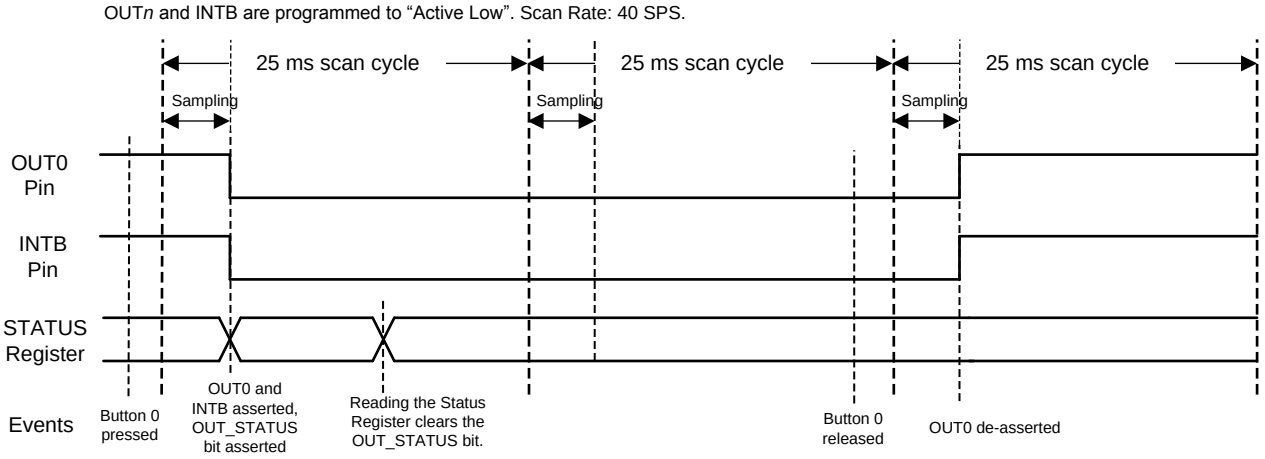


图 29. Timing Diagram of a Single Button Press

图 30 shows the LDC2112/LDC2114 response to multiple button presses. In this example, after Button 0 is pressed, the OUT0 pin is asserted. After that, Button 1 is also pressed, following which Button 0 is released. The OUT0 pin is de-asserted and OUT1 pin asserted at the end of the next button sampling window. The INTB pin remains continuously asserted as long as at least one of the buttons is pressed. The OUT_STATUS bit only changes from 0 to 1 after the first button assertion.

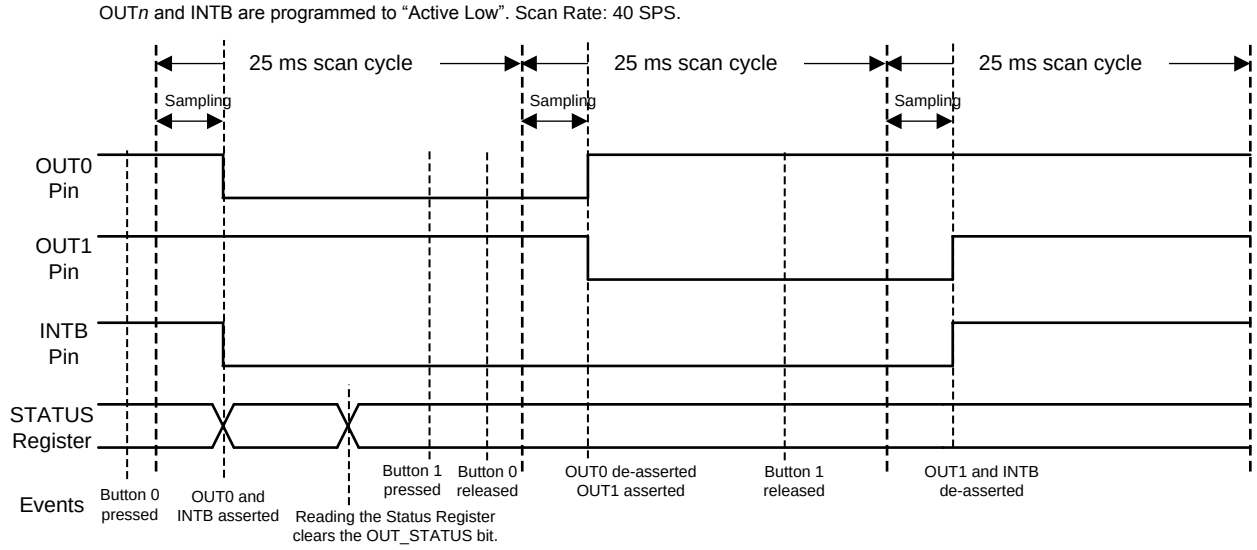


图 30. Timing Diagram of Multiple Button Presses

The INTB pin also reports any error event. If an error occurs, the INTB pin is asserted and the error is reported in the STATUS register (Address 0x00). Refer to *Register STATUS (Address 0x00)* for possible error events.

8.1.12 Estimating Supply Current

When the LDC2112/LDC2114 is active (in either Normal Power Mode or Low Power Mode), its current can be characterized by 公式 13:

$$I_{ACTIVEn} = 1.6 + \frac{12}{1 + 16 \times R_{Pn}^{1.21}} + 0.011 \times f_{SENSORn}$$

where

- $I_{ACTIVEn}$ is the supply current in mA during active sampling,
- R_{Pn} is the sensor parallel resonant impedance in kΩ,
- $f_{SENSORn}$ is the sensor frequency in MHz, and
- n is the channel index, i.e. n = 0 or 1 for LDC2112; n = 0, 1, 2, or 3 for LDC2114. (13)

The LDC2112/LDC2114 is only actively sampling the enabled channels during a fraction of the scan window. So the average supply current is:

$$I_{DD} = \frac{1}{t_{SCAN}} \times \left(\sum_{n} I_{ACTIVEn} \times t_{SAMPLEn} \right) + 0.005$$

where

- I_{DD} is the average supply current in mA,
- t_{SCAN} is the scan window (set by the scan rate) in ms,
- $I_{ACTIVEn}$ is the supply current when the device is active as defined by 公式 13, and
- t_{SAMPLE} is the button sampling window in ms. (14)

8.2 Typical Application

8.2.1 Touch Button Design

The low power architecture of LDC2112/LDC2114 makes them suitable for driving button sensors in consumer electronics, such as mobile phones. Most mobile phones today have three buttons along the edges, namely the power button, volume up, and volume down. The LDC2112 can support two buttons, and LDC2114 can support four.

On a typical smartphone, the two volume buttons are next to each other, so they may be susceptible to false detections such as simultaneous button presses. To prevent such mis-triggers, they can be grouped together to take advantage of the various features that mitigate false detections as explained in *Mitigating False Button Detections*. For example, if Max-win is applied to the two volume buttons, only the one with the greater force will be triggered.

The inductive touch solution does not require any mechanical cutouts at the button locations. This can support reduced manufacturing cost for the phone case and enhance the case's resistance to moisture, dust, and dirt. This is a great advantage compared to mechanical buttons in the market today.

8.2.1.1 Design Requirements

The sensor parameters, including frequency, R_P, and Q factor have to be within the design space of the LDC2112/LDC2114 as specified in *Electrical Characteristics*.

8.2.1.2 Detailed Design Procedure

The LDC2112/LDC2114 is a multi-channel device. The italic n in the parameters below refers to the channel index, i.e., n = 0 or 1 for LDC2112, and n = 0, 1, 2, or 3 for LDC2114.

1. Select system-based options:

- Select Normal or Low Power Mode of operation by setting the LPWRB pin to V_{DD} or Ground, respectively. Configure the enable bits for all channels in *Register EN (Address 0x0C)*.
- Select the polarities of OUTn and INTB pins by configuring *Register OPOL_DPOL (Address 0x1C)* and *Register INTPOL (Address 0x11)*.

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Typical Application (接下页)

- Configure the sensor frequency setting in Registers SENSOR*n*_CONFIG (Addresses *0x20*, *0x22*, *0x24*, *0x26*).

2. Choose the sampling rate (80, 40, 20, 10, 5, 2.5, 1.25, or 0.625 SPS) based on system power consumption requirement, and configure *Register NP_SCAN_RATE (Address 0x0D)* or *Register LP_SCAN_RATE (Address 0x0F)*.

3. Choose the button sampling window based on power consumption and noise requirements (recommended: 1 ms to 8 ms). While a longer button sampling window provides better noise performance, 1 ms is typically sufficient for most applications. Set SENCYC*n* and LCDIV in Registers SENSOR*n*_CONFIG (Addresses *0x20*, *0x22*, *0x24*, *0x26*) and *Register LC_DIVIDER (Address 0x17)* in the following steps:

- Calculate LCDIV = ceiling ($\log_2$ ($f_{SENSORn}$ × $t_{SAMPLEn}$) – 12), where $f_{SENSORn}$ is the sensor frequency in MHz, $t_{SAMPLEn}$ is the button sampling window in µs
- If LCDIV < 0, set it to 0
- Adjust SENCYC*n* to get desired $t_{SAMPLEn}$ according to $t_{SAMPLEn} = 128 \times (SENCYCn + 1) \times 2^{LCDIV} / f_{SENSORn}$

4. Calibrate gain in the appropriate Registers GAIN*n* (Addresses *0x0E*, *0x10*, *0x12*, *0x14*). The gain setting can be used to tune the sensitivity of the touch button. GAIN*n* is a 6-bit field with 64 different gain levels corresponding to normalized gains between 1 and 232. A good mechanical and sensor design typically requires a gain level of around 32 to 50, corresponding to relative gains of 16 to 76 (normalized to gain level of 0). Use the following sequence to determine the appropriate gain for each button:

- Apply minimum desired force to the button.
- Read initial DATA*n* value after the button press. Note that the baseline tracking will affect this value.
- Calculate gain factor needed to increase DATA*n* to the programmed threshold (default is 160).
- Look up the *Gain Table* to find the required gain setting.

5. Enable special features to mitigate button interference if there is any. Registers BTPAUSE_MAXWIN, TWIST, COMMON_DEFORM (Addresses *0x16*, *0x19*, *0x1A*).

For more information on inductive touch system design, including mechanical design and sensor electrical design, refer to *Inductive Touch System Design Guide*.

8.2.1.3 Application Curves

图 31 shows a sequence of button presses of 150 grams force, two presses to Channel 0, then two presses to Channel 1. Each button press response is greater than the threshold.

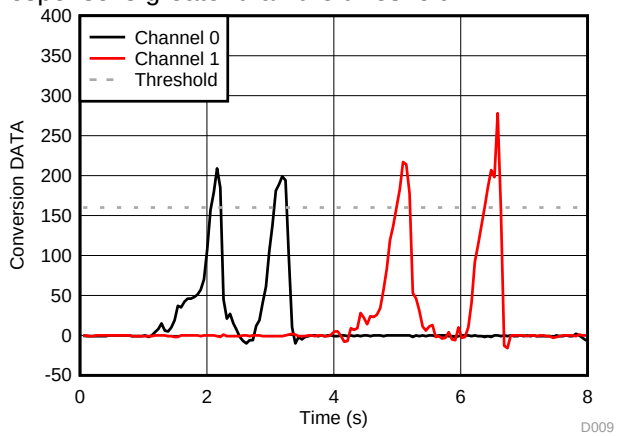


图 31. Conversion DATA vs Time for Channels 0 and 1

9 Power Supply Recommendations

The LDC2112/LDC2114 power supply should be bypassed with a 1 µF and a 0.1 µF pair of capacitors in parallel to ground. The capacitors should be placed as close to the LDC as possible. The smaller value 0.1 µF capacitor should be placed closer to the VDD pin than the 1 µF capacitor. The capacitors should be a low ESL, low ESR type. To enable close positioning of the capacitors, use of 0201 footprint devices for the bypass capacitors is recommended for the DSBGA package.

Refer to *Recommended Operating Conditions* for more details.

10 Layout

10.1 Layout Guidelines

The COM pin must be bypassed to ground with an appropriate value capacitor. For details of how to choose the capacitor value, refer to *Setting COM Pin Capacitor*. C_{COM} should be placed as close as possible to the COM pin. The COM signal should be tied to a small copper fill placed underneath the IN*n* signals. The IN*n* signals should stay clear of other high frequency traces.

Each active channel needs to have an LC resonator connected to the corresponding IN*n* pins. The sensor capacitor should be placed within 10 mm of the corresponding IN*n* pin, and the inductor (NOT shown in 图 32) should be placed at the appropriate location next to (but not touching) the metal target. The IN*n* traces should be at least 6 mil (0.15 mm) wide to minimize parasitic inductances.

For the DSBGA package, the inner four device pads (INTB, OUT3, LPWRB, and SDA) should be routed out on an inner layer through vias, with the traces offset to reduce coupling with other signals. These four vias may need to use blind vias or microvias to bring the signals out. The PCB layer stack should use a thinner (4 mil or 0.1 mm thickness) dielectric between the top copper and next copper layer so that microvias can be used.

10.2 Layout Example

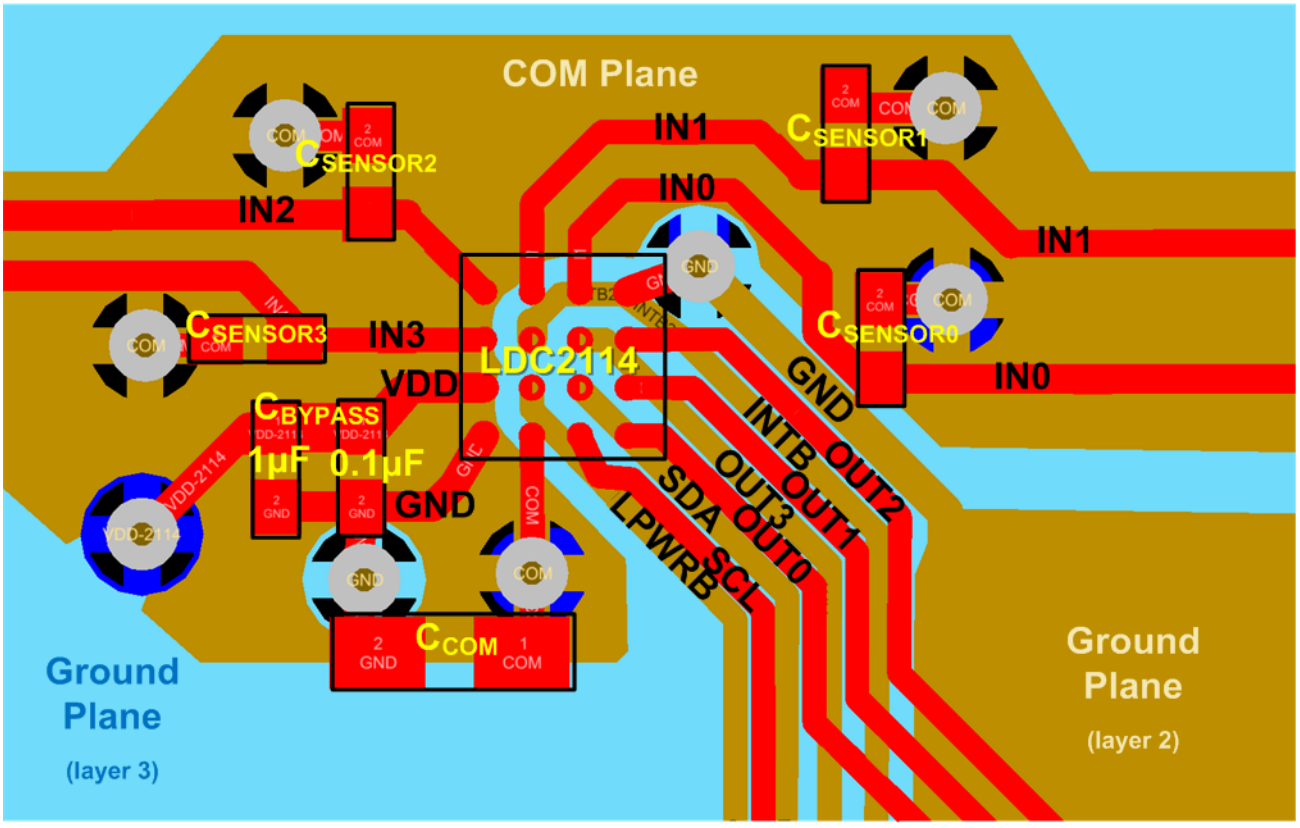


图 32. Layout of LDC2114 (DSBGA-16) With Decoupling Capacitors and Sensor Capacitors

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Layout Example (接下页)

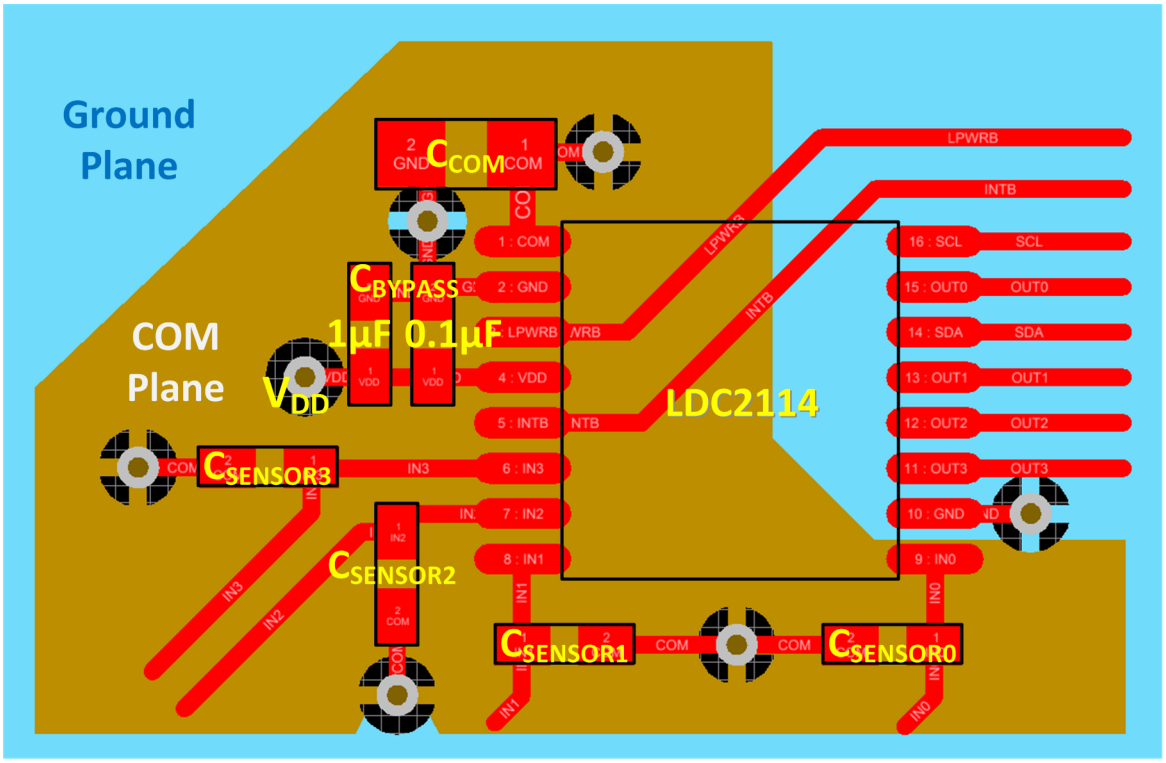


图 33. Layout of LDC2114 (TSSOP-16) With Decoupling Capacitors and Sensor Capacitors

10.3 DSBGA Light Sensitivity

Exposing the DSBGA device to direct light may cause incorrect operation of the device. Light sources such as halogen lamps can affect electrical performance if they are situated in proximity to the device. Light with wavelengths in the red and infrared part of the spectrum have the most detrimental effect.

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

- *LDC 计算工具*
- *《电感应触控系统设计指南》*

11.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即购买的快速链接。

表 **44.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
LDC2112	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
LDC2114	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.3 接收文档更新通知

要接收文档更新通知，请导航至德州仪器 TI.com.cn 上的器件产品文件夹。请单击右上角的*通知我* 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

11.4 社区资源

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

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11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LDC2112PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LDC2112	Samples
LDC2112PWT	ACTIVE	TSSOP	PW	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LDC2112	Samples
LDC2112YFDR	ACTIVE	DSBGA	YFD	16	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	17M	Samples
LDC2112YFDT	ACTIVE	DSBGA	YFD	16	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	17M	Samples
LDC2114PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LDC2114	Samples
LDC2114PWT	ACTIVE	TSSOP	PW	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LDC2114	Samples
LDC2114YFDR	ACTIVE	DSBGA	YFD	16	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	14G	Samples
LDC2114YFDT	ACTIVE	DSBGA	YFD	16	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	14G	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

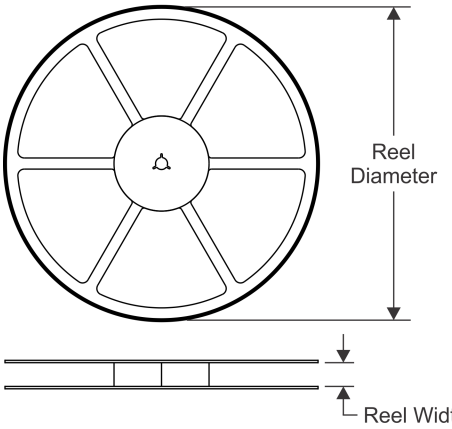
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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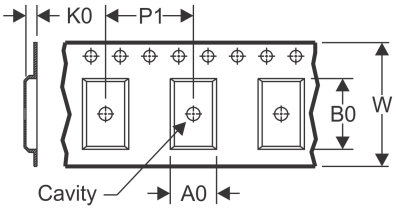
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

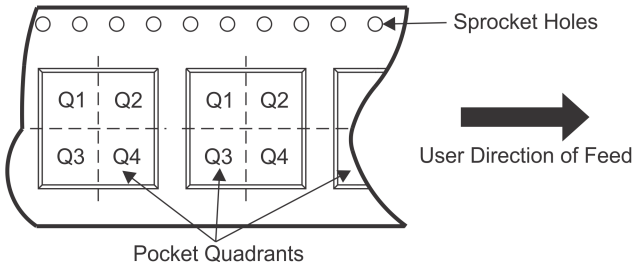


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

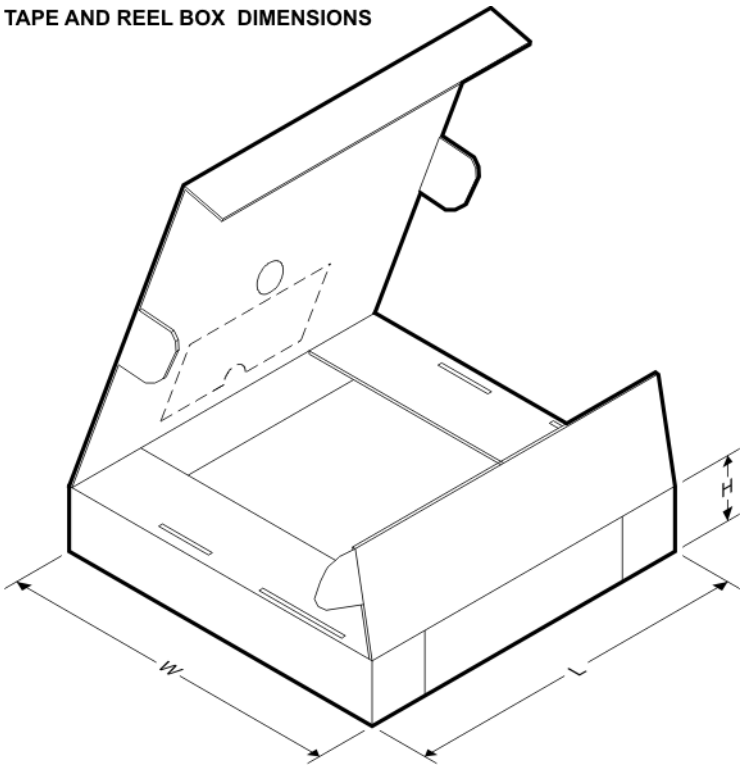
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LDC2112PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LDC2112YFDR	DSBGA	YFD	16	3000	180.0	8.4	1.69	1.69	0.46	4.0	8.0	Q1
LDC2112YFDT	DSBGA	YFD	16	250	180.0	8.4	1.69	1.69	0.46	4.0	8.0	Q1
LDC2114PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LDC2114YFDR	DSBGA	YFD	16	3000	180.0	8.4	1.69	1.69	0.46	4.0	8.0	Q1
LDC2114YFDT	DSBGA	YFD	16	250	180.0	8.4	1.69	1.69	0.46	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

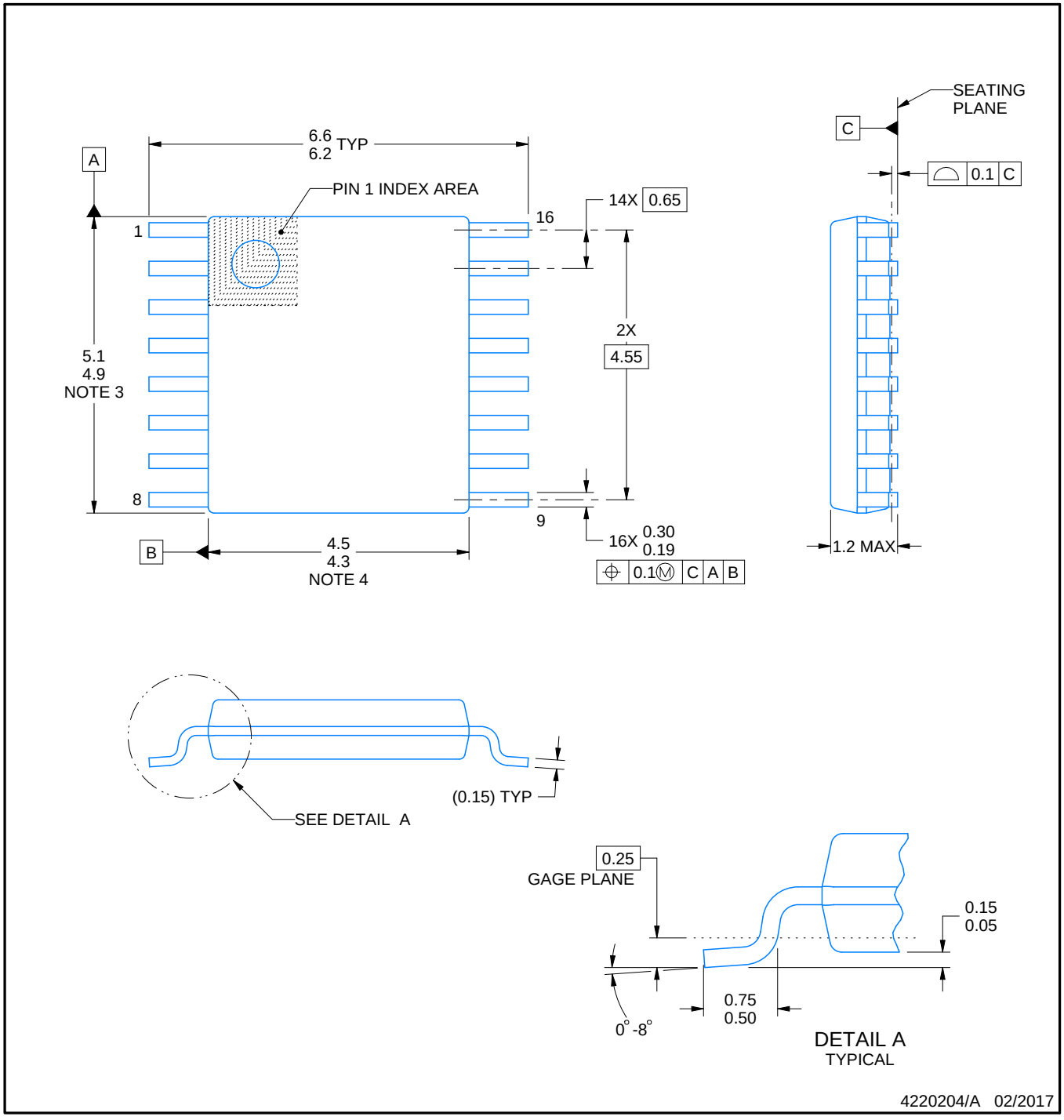
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LDC2112PWR	TSSOP	PW	16	2000	350.0	350.0	43.0
LDC2112YFDR	DSBGA	YFD	16	3000	182.0	182.0	20.0
LDC2112YFDT	DSBGA	YFD	16	250	182.0	182.0	20.0
LDC2114PWR	TSSOP	PW	16	2000	350.0	350.0	43.0
LDC2114YFDR	DSBGA	YFD	16	3000	182.0	182.0	20.0
LDC2114YFDT	DSBGA	YFD	16	250	182.0	182.0	20.0

PACKAGE OUTLINE

PW0016A

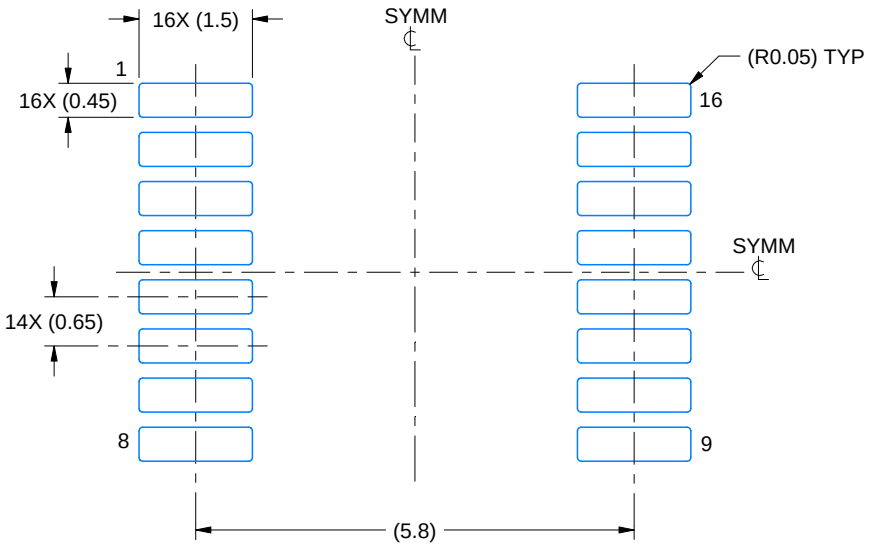
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

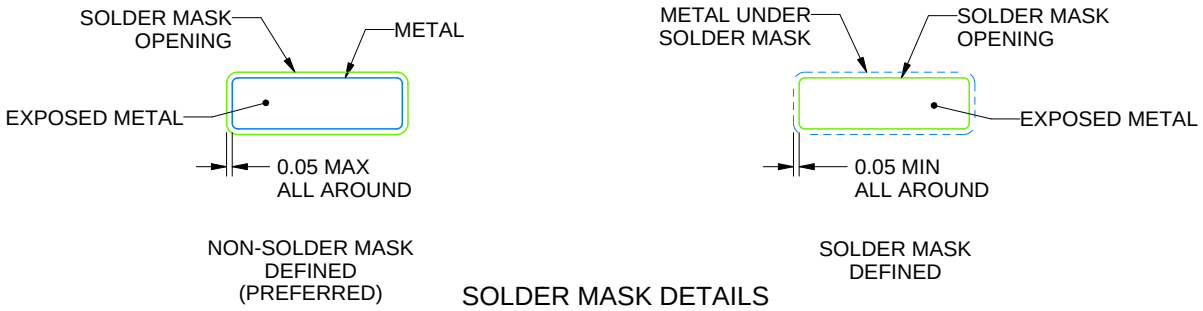


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

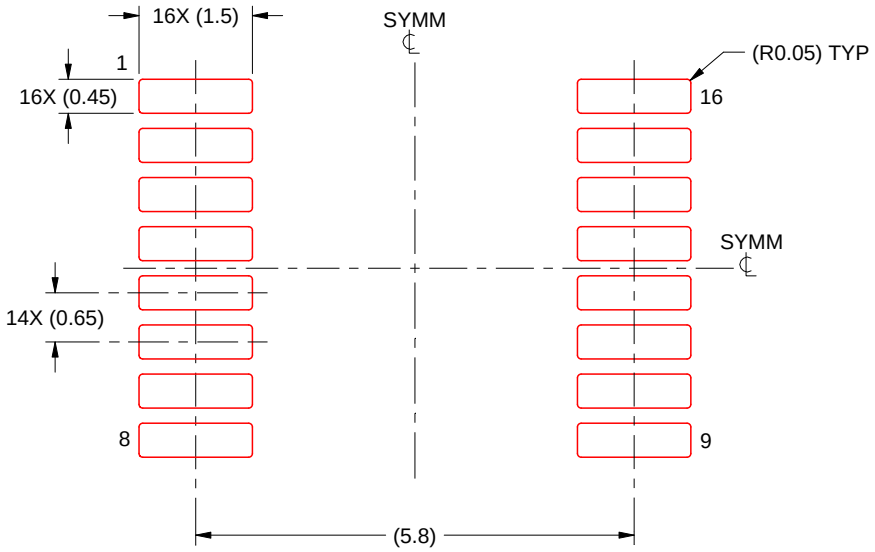


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

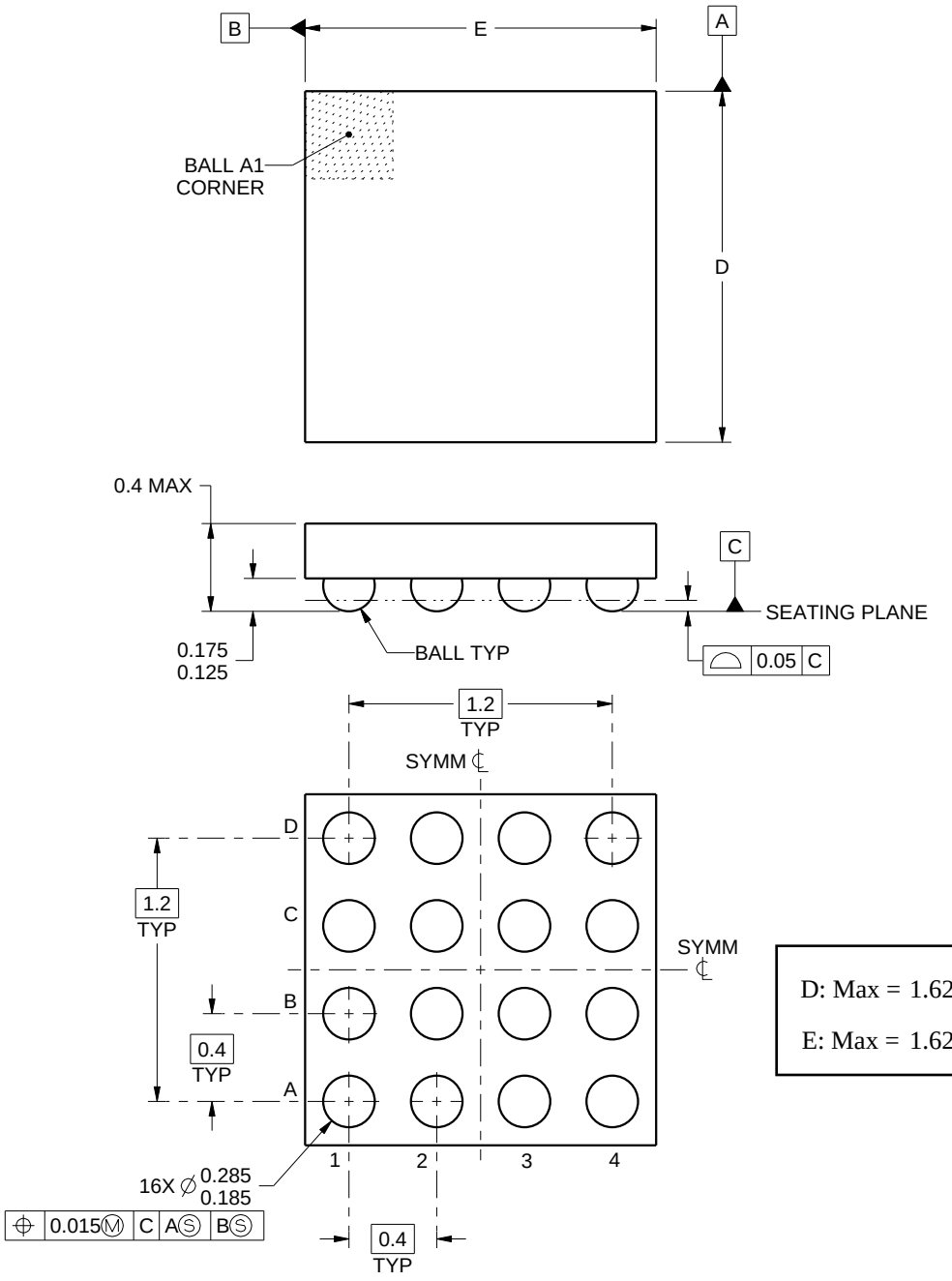
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

YFD0016

DSBGA - 0.4 mm max height

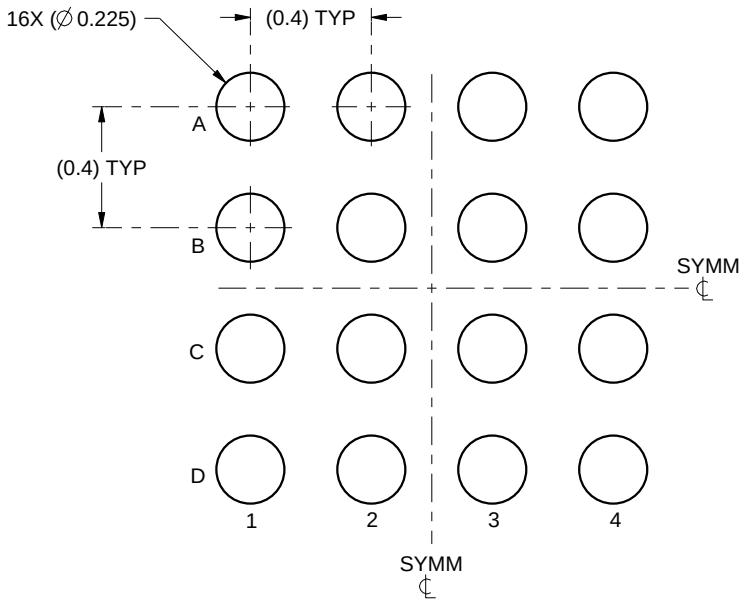
DIE SIZE BALL GRID ARRAY



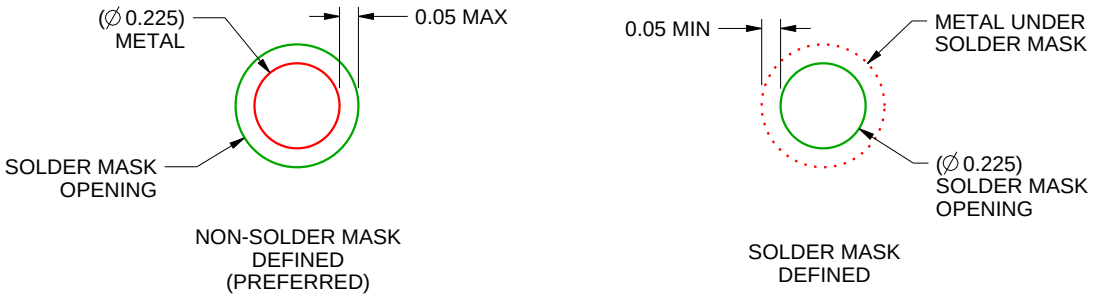
4222547/A 12/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4222547/A 12/2015

NOTES: (continued)

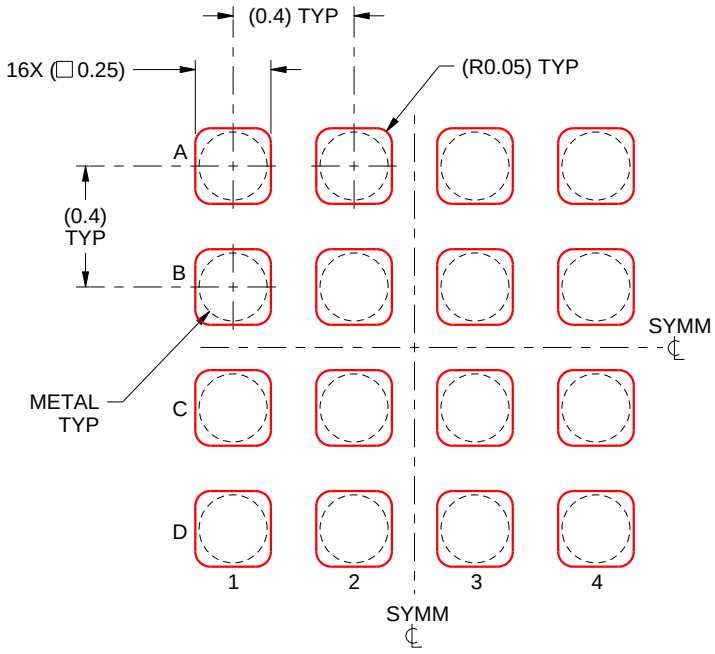
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
Refer to Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFD0016

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4222547/A 12/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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