# LM15851 超宽带射频采样子系统

## 1 特性

- 出色的噪声和线性性能，最高可达 $F_{IN}$ = 3GHz 以上
- 可配置数字下变频器 (DDC)
- 抽取因数范围为 4 至 32（复杂基带输出）
- 在 4x 抽取率和 4000MSPS 条件下，可用输出带宽为 800MHz
- 在 32x 抽取率和 4000MSPS 条件下，可用输出带宽为 100MHz
- 低引脚数目 JESD204B 子类 1 接口
- 自动优化输出通道计数
- 嵌入式低延迟信号范围指示
- 低功耗
- 主要规格：
  - 最大采样率：4000MSPS
  - 最小采样率：1000MSPS
  - DDC 输出字大小：15 位复数（共 30 位）
  - 三阶互调失真 (IMD3)：−64dBc（−13dBFS 时，$F_{IN}$ = 2140MHz ± 30MHz）
  - 全功率带宽 (FPBW) (–3dB)：3.2GHz））
  - 电源电压：1.9V 和 1.2V
  - 功耗
    - 10 倍抽取率 (4000MSPS)：2W
    - 断电模式：< 50mW

## 2 应用

- 无线基础设施
- RF 采样软件定义无线电
- 宽带微波回程
- 电缆数据服务接口规范 (DOCSIS)/电缆基础设施

## 3 说明

LM15851 器件为宽带采样和数字调谐器件。德州仪器 (TI) 的千兆次采样模数转换器 (ADC) 技术支持采用射频直接对大范围频谱采样。集成 DDC（数字下变频器）可进行数字滤波和下变频转换。所选频率块适用于 JESD204B 串行接口。数据以基带 15 位复数信息形式输出，以减轻下游处理压力。根据数字下变频器 (DDC) 抽取率和链接输出率设置，该数据将通过串行接口的 1 至 5 通道输出。

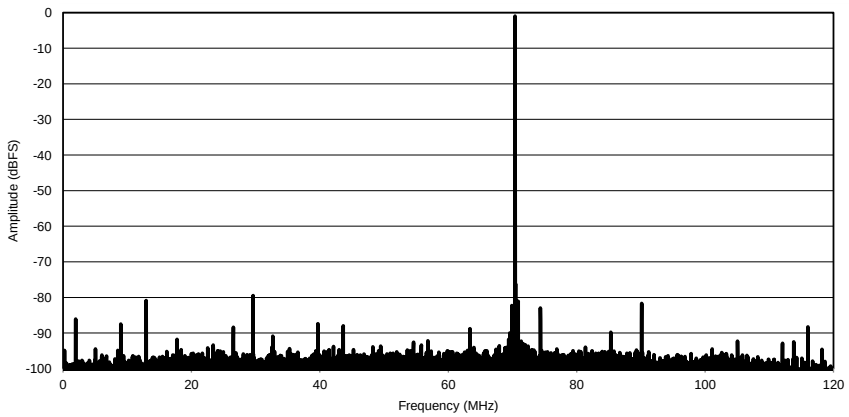
LM15851 器件采用68 引脚超薄四方扁平无引线 (VQFN) 封装。该器件的工业环境运行温度范围为 –40°C ≤ $T_A$ ≤ 85°C。

器件信息(1)

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| LM15851 | VQFN (68) | 10.00mm x 10.00mm |

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

**16 倍抽取率 — 频谱响应**
**$f_S$ = 4GHz，$F_{IN}$ = 1897MHz（–1dBFS 时），$f_{(NCO_x)}$ = 1827MHz**




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

# 目录

**1 特性** ... 1
**2 应用** ... 1
**3 说明** ... 1
**4 修订历史记录** ... 2
**5 Pin Configuration and Functions** ... 4
**6 Specifications** ... 9
6.1 Absolute Maximum Ratings ... 9
6.2 ESD Ratings ... 9
6.3 Recommended Operating Conditions ... 10
6.4 Thermal Information ... 10
6.5 Electrical Characteristics ... 10
6.6 Timing Requirements ... 14
6.7 Internal Characteristics ... 16
6.8 Switching Characteristics ... 17
6.9 Typical Characteristics ... 19
**7 Detailed Description** ... 24
7.1 Overview ... 24
7.2 Functional Block Diagram ... 24
7.3 Feature Description ... 25
7.4 Device Functional Modes ... 43
7.5 Programming ... 46
7.6 Register Map ... 48
**8 Application and Implementation** ... 73
8.1 Application Information ... 73
8.2 Typical Application ... 73
8.3 Initialization Set-Up ... 75
8.4 Dos and Don'ts ... 75
**9 Power Supply Recommendations** ... 76
9.1 Supply Voltage ... 76
**10 Layout** ... 77
10.1 Layout Guidelines ... 77
10.2 Layout Example ... 77
10.3 Thermal Management ... 80
**11 器件和文档支持** ... 80
11.1 器件支持 ... 80
11.2 文档支持 ... 81
11.3 社区资源 ... 81
11.4 商标 ... 82
11.5 静电放电警告 ... 82
11.6 Glossary ... 82
**12 机械、封装和可订购信息** ... 82

## 4 修订历史记录

| Changes from Revision D (July 2015) to Revision E | Page |
|---|---|
| • Changed reset value of address 0x006 from 0x03 to 0x13 in *Memory Map* table | 48 |
| • Changed reset value of address 0x006 from 0x03 to 0x13 in *Standard SPI-3.0 Registers* table | 51 |
| • Changed 0x03 to 0x13 in reset value and description of bits 7-0 and changed 0000 0011 to 0001 0011 in *Chip Version Register* section | 52 |

| Changes from Revision C (September 2014) to Revision D | Page |
|---|---|
| • Deleted references to time stamp including pin names (TMST+, TMST–). | 7 |
| • Added additional voltage difference parameters to the *Absolute Maximum Ratings* table | 9 |
| • Added junction temperature to the *Absolute Maximum Ratings* table | 9 |
| • Added common mode voltage parameter to the *Recommended Operating Conditions* table. Changed CLK to SYSREF, and ~SYNC | 10 |
| • Deleted the *Differential Analog Input Connection* image in *The Analog Inputs* section | 25 |
| • Added note about offset adjust in Background Calibration Mode to the *Offset Adjust* section and I/O offset register tables | 29 |
| • Added the *Calibration Cycle Timing for Different Calibration Modes and Options* table in the *Timing Calibration Mode* section | 44 |
| • Changed 0x004-0x005 to RESERVED in the *Standard SPI-3.0 Registers* summary table | 51 |
| • Changed the name of bit 0 in the Clock Generator Control 0 Register from DC_LVPECL_TS_EN to DC_LVPECL_SYNC_en | 56 |

| Changes from Revision B (February 2014) to Revision C | Page |
|---|---|
| • 已更改 器件状态，从产品预览改为量产数据 | 1 |

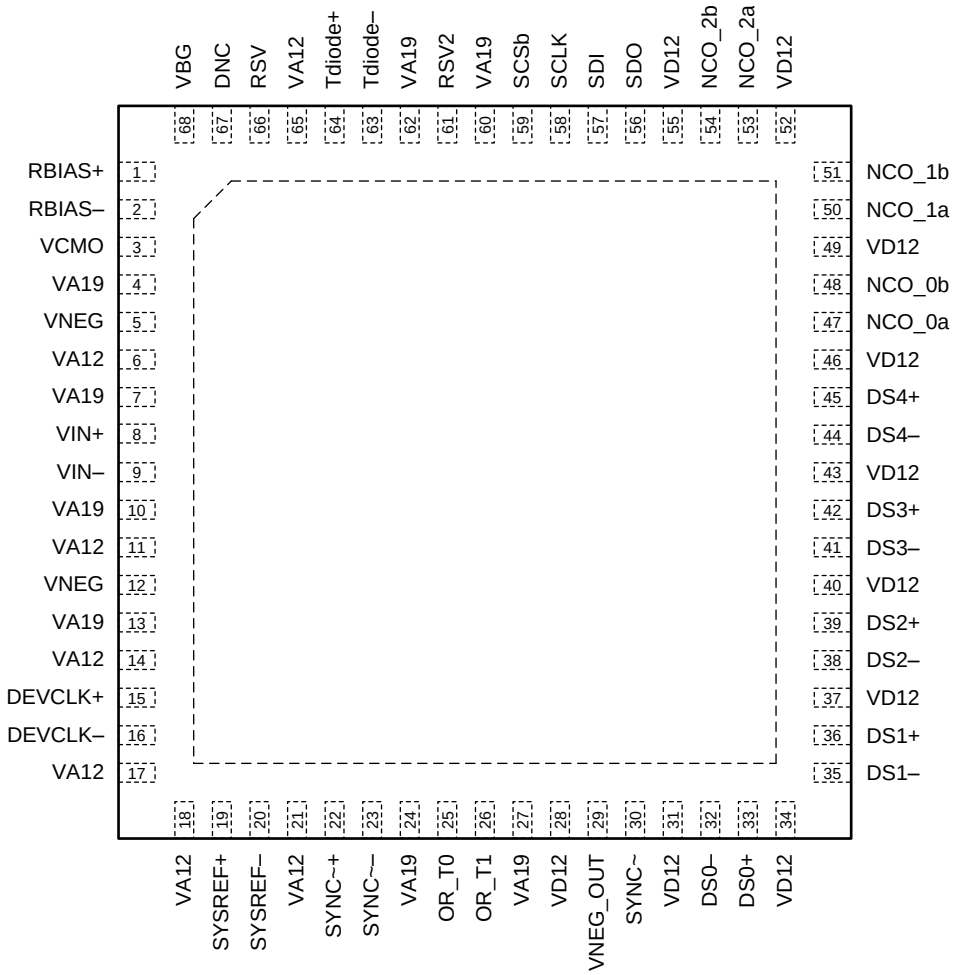

版权 © 2014–2017, Texas Instruments Incorporated

**Changes from Original (January 2014) to Revision A** **Page**

- 已将*主要技术规格*列表移到*特性*列表中 ..... 1
- 已将*其他毛刺：-81dBFS* 特征项替换为*全功率带宽 (FPBW) (–3dB)：3.3GHz*特征项（*主要技术规格特性*列表 ..... 1
- 已删除 *关于处于开发阶段*的声明（*说明部分*） ..... 1
- 已添加 目录（*说明 （续）*部分现列在*修订历史记录*后） ..... 1
- 已添加 *器件信息表* ..... 1
- Moved the pin configuration illustration and pin functions table into a new *Pin and Configurations* section. Changed Symbol column name to NAME column name ..... 7
- 已添加 已更改*器件和文档支持*部分，现包含商标和静电放电注意事项 ..... 82
- 已添加 已更改*机械、封装和可订购产品信息*部分 ..... 82

# 5 Pin Configuration and Functions

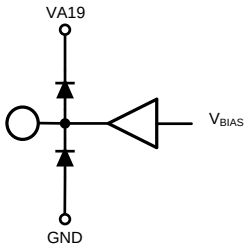
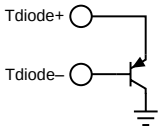
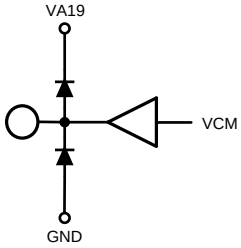
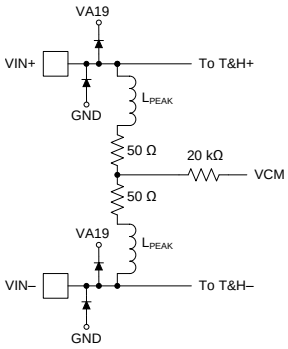
**NKE Package**
**68-Pin VQFN With Thermal Pad**
**Top View**



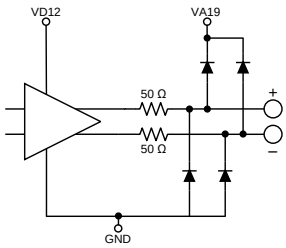
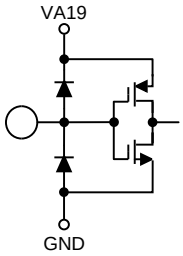
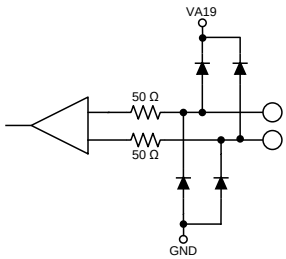
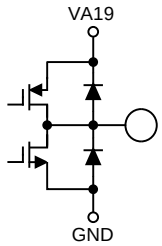

DNC = Make no external connection


Copyright © 2014–2017, Texas Instruments Incorporated

## Pin Functions

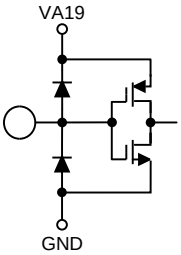
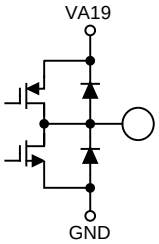
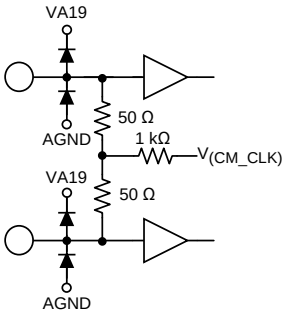
| PIN | | EQUIVALENT CIRCUIT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO. | | | |
| **ANALOG** | | | | |
| RBIAS+ | 1 |  | I/O | **External Bias Resistor Connections**<br>External bias resistor terminals. A 3.3 kΩ (±0.1%) resistor should be connected between RBIAS+ and RBIAS–. The RBIAS resistor is used as a reference for internal circuits which affect the linearity of the converter. The value and precision of this resistor should not be compromised. These pins must be isolated from all other signals and grounds. |
| RBIAS– | 2 | | | |
| TDIODE– | 63 |  | Passive | **Temperature Diode**<br>These pins are the positive (anode) and negative (cathode) diode connections for die temperature measurements. Leave these pins unconnected if they are not used. See the *Built-In Temperature Monitor Diode* section for more details. |
| TDIODE+ | 64 | | | |
| VBG | 68 |  | O | **Bandgap Output Voltage**<br>This pin is capable of sourcing or sinking 100 μA and can drive a load up to 80 pF. Leave this pin unconnected if it is not used in the application. See the *The Reference Voltage* section for more details. |
| VCMO | 3 | | O | **Common Mode Voltage**<br>The voltage output at this pin must be the common-mode input voltage at the VIN+ and VIN– pins when DC coupling is used. This pin is capable of sourcing or sinking 100 μA and can drive a load up to 80 pF. Leave this pin unconnected if it is not used in the application. |
| VIN+ | 8 |  | I | **Signal Input**<br>The differential full-scale input range is determined by the full-scale voltage adjust register. An internal peaking inductor ($L_{PEAK}$) of 5 nH is included for parasitic compensation. |
| VIN– | 9 | | | |

## Pin Functions (continued)

| PIN | | EQUIVALENT CIRCUIT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO. | | | |
| **DATA** | | | | |
| DS0− | 32 |  | O | **Data**<br>**CML** These pins are the high-speed serialized-data outputs with user-configurable pre-emphasis. These outputs must always be terminated with a 100-Ω differential resistor at the receiver. |
| DS0+ | 33 | | | |
| DS1– | 35 | | | |
| DS1+ | 36 | | | |
| DS2– | 38 | | | |
| DS2+ | 39 | | | |
| DS3– | 41 | | | |
| DS3+ | 42 | | | |
| DS4– | 44 | | | |
| DS4+ | 45 | | | |
| **GROUND, RESERVED, DNC** | | | | |
| DNC | 67 | | — | **Do Not Connect**<br>Do not connect DNC to any circuitry, power, or ground signals. |
| RSV | 66 |  | — | **Reserved**<br>**Connect to Ground or Leave Unconnected:** This reserved pin is a logic input for possible future device versions. It is recommended to connect this pin to ground. Floating this pin is also permissible. |
| RSV2 | 61 | | — | **Reserved**<br>**Connect to Ground** Connect this reserved input pin to ground for proper operation. |
| Thermal Pad | | | — | **Ground (GND)**<br>The exposed pad on the bottom of the package is the ground return for all supplies. This pad must be connected with multiple vias to the printed circuit board (PCB) ground planes to ensure proper electrical and thermal performance.<br>The exposed center pad on the bottom of the package must be thermally and electrically connected (soldered) to a ground plane to ensure rated performance. |
| **LVCMOS** | | | | |
| NCO_0 | 47, 48 |  | I | **NCO ConfigSelect**<br>These three pin pairs allow the host device to select the specific NCO frequency or phase accumulator that is active. Each pair must be connected together and driven with a common 1.8-V LVCMOS signal. Connect these inputs to GND if they are not used in the application. |
| NCO_1 | 50, 51 | | | |
| NCO_2 | 53, 54 | | | |
| OR_T0 | 25 |  | O | **Over-Range**<br>Over-range detection status for T0 and T1 thresholds. Leave these pins unconnected if they are not used in the application. |
| OR_T1 | 26 | | | |


Copyright © 2014–2017, Texas Instruments Incorporated

## Pin Functions (continued)

| PIN | | EQUIVALENT CIRCUIT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO. | | | |
| SCLK | 58 |  | I | **Serial Interface Clock**<br>This pin functions as the serial-interface clock input which clocks the serial data in and out. The *Using the Serial Interface* section describes the serial interface in more detail. |
| SDI | 57 | | I | **Serial Data In**<br>This pin functions as the serial-interface data input. The *Using the Serial Interface* section describes the serial interface in more detail. |
| SYNC~ | 30 | | I | **SYNC~**<br>This pin provides the JESD204B-required synchronizing request input. A logic-low applied to this input initiates a lane alignment sequence. The choice of LVCMOS or differential SYNC~ is selected through bit 6 of the configuration register 0x202h. Connect this input to GND or VA19 if differential SYNC~ input is used. |
| $\overline{\text{SCS}}$ | 59 | | I | **Serial Chip Select (active low)**<br>This pin functions as the serial-interface chip select. The *Using the Serial Interface* section describes the serial interface in more detail. |
| SDO | 56 |  | O | **Serial Data Out**<br>This pin functions as the serial-interface data output. The *Using the Serial Interface* section describes the serial interface in more detail. |
| **DIFFERENTIAL INPUT** | | | | |
| DEVCLK+ | 15 |  | I | **Device Clock Input**<br>The differential device clock signal must be AC coupled to these pins. The input signal is sampled on the rising edge of CLK. |
| DEVCLK– | 16 | | | |
| SYSREF+ | 19 | | I | **SYSREF**<br>The differential periodic waveform on these pins synchronizes the device per JESD204B. If JESD204B subclass 1 synchronization is not required and these inputs are not utilized they may be left unconnected. In that case ensure SysRef_Rcvr_En=0 and SysRef_Pr_En=0. |
| SYSREF– | 20 | | | |
| SYNC~+ | 22 | | I | **SYNC~**<br>This differential input provides the JESD204B-required synchronizing request input. A differential logic-low applied to these inputs initiates a lane alignment sequence. For differential SYNC~ usage, leave unconnected if SYNC_DIFFSEL = 0. These inputs may be left unconnected if they are not used for the SYNC~function. |
| SYNC~- | 23 | | | |

## Pin Functions (continued)

| PIN | | EQUIVALENT CIRCUIT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO. | | | |
| **POWER** | | | | |
| VA12 | 6<br>11<br>14<br>17<br>18<br>21<br>65 | | — | **Analog 1.2 V power supply pins**<br>Bypass these pins to ground using one 10-µF capacitor and two 1-µF capacitors for bulk decoupling plus one 0.1-µF capacitor per pin for individual decoupling. |
| VA19 | 4<br>7<br>10<br>13<br>24<br>27<br>60<br>62 | | — | **Analog 1.9 V power supply pins**<br>Bypass these pins to ground using one 10-µF capacitor and two 1-µF capacitors for bulk decoupling plus one 0.1-µF capacitor per pin for individual decoupling. |
| VD12 | 28<br>31<br>34<br>37<br>40<br>43<br>46<br>49<br>52<br>55 | | — | **Digital 1.2 V power supply pins**<br>Bypass these pins to ground using one 10-µF capacitor and two 1-µF capacitors for bulk decoupling plus one 0.1-µF capacitor per pin for individual decoupling. |
| VNEG | 5<br>12 | | I | **VNEG**<br>These pins must be decoupled to ground with a 0.1-µF ceramic capacitor near each pin. These power input pins must be connected to the VNEG_OUT pin with a low resistance path. The connections must be isolated from any noisy digital signals and must also be isolated from the analog input and clock input pins. |
| VNEG_OUT | 29 | | O | **VNEG_OUT**<br>The voltage on this output can range from –1V to +1V. This pin must be decoupled to ground with a 4.7-µF, low ESL, low ESR multi-layer ceramic chip capacitor and connected to the VNEG input pins. This voltage must be isolated from any noisy digital signals, clocks, and the analog input. |


Copyright © 2014–2017, Texas Instruments Incorporated

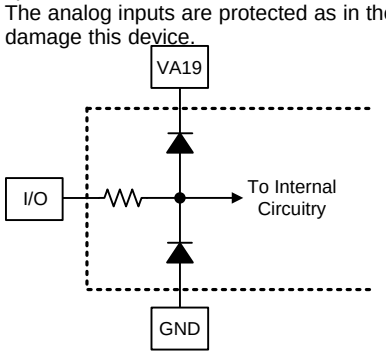
# 6 Specifications

## 6.1 Absolute Maximum Ratings

The soldering process must comply with TI's Reflow Temperature Profile specifications. Refer to www.ti.com/packaging.[(1)(2)(3)]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage | 1.2-V supply | VA12, VD12 | | 1.4 | V |
| | 1.9-V supply | VA19 | | 2.2 | |
| | 1.2-V supply difference between VA12 and VD12 | | –200 | 200 | mV |
| Voltage | On any input pin (except VIN+ or VIN–) | | –0.15 | $V_{(VA19)}$ + 0.15 | V |
| | On VIN+ or VIN– | | 0 | 2 | |
| Voltage difference | \|(VIN+) – (VIN–)\|[(4)] | | | 2 | V |
| | \|(DEVCLK+) – (DEVCLK–)\| | | | 2 | |
| | \|(SYSREF+) – (SYSREF–)\| | | | 2 | |
| | \|(~SYNC+) – (~SYNC–)\| | | | 1 | |
| RF input power, $P_I$ | On VIN+, VIN–, with proper input common mode maintained. $F_{IN}$ ≥ 3 GHz, $Z_{(SOURCE)}$ = 100 Ω, Input_Clamp_EN = 0 or 1 | | | 11.07 | dBm |
| | On VIN+, VIN–, with proper input common mode maintained. $F_{IN}$ = 1 GHz, $Z_{(SOURCE)}$ = 100 Ω, Input_Clamp_EN = 1 | | | 14.95 | |
| | On VIN+, VIN–, with proper input common mode maintained. $F_{IN}$ ≤ 100 MHz, $Z_{(SOURCE)}$ = 100 Ω, Input_Clamp_EN = 1 | | | 20.97 | |
| Input current | At any pin other than VIN+ or VIN–[(5)] | | –25 | 25 | mA |
| | VIN+ or VIN– | | –50 | 50 | mA DC |
| | Package[(5)] (sum of absolute value of all currents forced in or out, not including power supply current) | | | 100 | mA |
| Junction temperature, $T_J$ | Power applied. Verified by High Temperature Operation Life testing to 1000 hours. | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | | –65 | 150 | °C |

(1) Reflow temperature profiles are different for lead-free and non-lead-free packages.
(2) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) The analog inputs are protected as in the following circuit. Input-voltage magnitudes beyond the *Absolute Maximum Ratings* may damage this device.




(5) When the input voltage at any pin (other than VIN+ or VIN–) exceeds the power supply limits (that is, less than GND or greater than VA19), the current at that pin must be limited to 25 mA. The 100-mA maximum package input current rating limits the number of pins that can safely exceed the power supplies. This limit is not placed upon the power pins or thermal pad (GND).

## 6.2 ESD Ratings

| | | VALUE | UNIT |
|---|---|---|---|
| $V_{(ESD)}$ Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)] | ±2000 | V |
| | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)] | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Copyright © 2014–2017, Texas Instruments Incorporated

## 6.3 Recommended Operating Conditions

All voltages are measured with respect to GND = 0 V, unless otherwise specified.

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.2-V supply: VA12, VD12 | 1.14 | 1.26 | V |
| | | 1.9-V supply: VA19 | 1.8 | 2 | |
| | Supply sequence (power-up and power-down) | | | 1.9 supply ≥ 1.2 supply | V |
| $V_{CMI}$ | Analog input common mode voltage | | $V_{(VCMO)}$ – 0.15 | $V_{(VCMO)}$ + 0.15 | V |
| | VIN+, VIN– voltage (maintaining common mode) | | 0 | $V_{(VA19)}$ | V |
| | DEVCLK±, SYSREF±, ~SYNC± pin voltage range | | 0 | $V_{(VA19)}$ | V |
| $V_{ID(CLK)}$ | Differential DEVCLK±, SYSREF±, ~SYNC± amplitude | | 0.4 | 2 | $V_{PP}$ |
| $V_{CM(CLK)}$ | SYSREF±, ~SYNC± Common Mode | | 0.64 | 1.1 | V |
| $T_A$ | Ambient temperature | | –40 | 85 | °C |
| $T_J$ | Junction temperature | | | 135 | °C |

## 6.4 Thermal Information

| THERMAL METRIC[1] | | LM15851 NKE (VQFN) 68 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Thermal resistance, junction-to-ambient | 19.8 | °C/W |
| $R_{\theta JCbot}$ | Thermal resistance, junction-to-case (bottom) | 2.7 | °C/W |
| $\psi_{JB}$ | Characterization parameter, junction-to-board | 9.1 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN full scale range at default setting (725 $mV_{PP}$), VIN = –1 dBFS, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 4 GHz at 0.5 $V_{PP}$ with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a foreground (FG) mode calibration with timing calibration enabled. Typical values are at $T_A$ = 25°C.[1][2]

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **DYNAMIC PERFORMANCE CHARACTERISTICS** | | | | | | | |
| $IMD_3$ | Third-order intermodulation distortion | F1 = 2110 MHz at −13 dBFS<br>F2 = 2170 MHz at −13 dBFS | | | –64 | | dBc |
| **DECIMATE-BY-4 MODE** | | | | | | | |
| SNR1 | Signal-to-noise ratio, integrated across DDC alias protected output bandwidth Input frequency-dependent interleaving spurs included | $F_{IN}$ = 600 MHz, –1 dBFS, decimate-by-4 mode | $T_A$ = 25°C | | 59.9 | | dBFS |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | 56.2 | | | |
| | | | $T_A$ = 25°C, calibration = BG | | 59.2 | | |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$, calibration = BG | 53.3 | | | |
| | | $F_{IN}$ = 2400 MHz, –1 dBFS, decimate-by-4 mode | | | 56.4 | | |
| SNR2 | Signal-to-noise ratio, integrated across DDC alias protected output bandwidth Input frequency-dependent interleaving spurs excluded | $F_{IN}$ = 600 MHz, –1 dBFS, decimate-by-4 mode | $T_A$ = 25°C[3] | | 60.1 | | dBFS |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$[3] | 56.7 | | | |
| | | | $T_A$ = 25°C, calibration = BG [3] | | 60.2 | | |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$, calibration = BG[3] | 56.7 | | | |
| | | $F_{IN}$ = 2400 MHz, –1 dBFS, decimate-by-4 mode[3] | | | 57 | | |

(1) To ensure accuracy, the VA19, VA12, and VD12 pins are required to be well bypassed. Each supply pin must be decoupled with one or more bypass capacitors.
(2) Interleave related fixed frequency spurs at $f_S$ / 4 and $f_S$ / 2 are excluded from all SNR, SINAD, ENOB and SFDR specifications. The magnitude of these spurs is provided separately.
(3) Interleave related spurs at $f_S$ / 2 – $F_{IN}$, $f_S$ / 4 + $F_{IN}$ and $f_S$ / 4 – $F_{IN}$ are excluded from these performance calculations. The magnitude of these spurs is provided separately.


Copyright © 2014–2017, Texas Instruments Incorporated

## Electrical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN full scale range at default setting (725 $mV_{PP}$), VIN = –1 dBFS, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 4 GHz at 0.5 $V_{PP}$ with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a foreground (FG) mode calibration with timing calibration enabled. Typical values are at $T_A$ = 25°C.(1)(2)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| SINAD1 | Signal-to-noise and distortion ratio, integrated across DDC alias protected output bandwidth<br>Input frequency-dependent interleaving spurs included | $F_{IN}$ = 600 MHz, –1 dBFS, decimate-by-4 mode | $T_A$ = 25°C | | 59.9 | | dBFS |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | 55.9 | | | |
| | | | $T_A$ = 25°C, calibration = BG | | 59.2 | | |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$, calibration = BG | 53.1 | | | |
| | | $F_{IN}$ = 2400 MHz, –1 dBFS, decimate-by-4 mode | | | 56.4 | | |
| SINAD2 | Signal-to-noise and distortion ratio, integrated across DDC alias protected output bandwidth<br>Interleaving spurs excluded | $F_{IN}$ = 600 MHz, –1 dBFS, decimate-by-4 mode | $T_A$ = 25°C(3) | | 60.1 | | dBFS |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$(3) | 56.3 | | | |
| | | | $T_A$ = 25°C, calibration = BG (3) | | 60.1 | | |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$, calibration = BG(3) | 56.4 | | | |
| | | $F_{IN}$ = 2400 MHz, –1 dBFS, decimate-by-4 mode(3) | | | 57 | | |
| ENOB1 | Effective number of bits, integrated across DDC alias protected output bandwidth<br>Interleaving spurs included | $F_{IN}$ = 600 MHz, –1 dBFS, Decimate-by-4 mode | $T_A$ = 25°C | | 9.7 | | Bits |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | 9.0 | | | |
| | | | $T_A$ = 25°C, calibration = BG | | 9.5 | | |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$, calibration = BG | 8.5 | | | |
| | | $F_{IN}$ = 2400 MHz, –1 dBFS, decimate-by-4 mode | | | 9.1 | | |
| ENOB2 | Effective number of bits, integrated across DDC alias protected output bandwidth<br>Interleaving spurs excluded | $F_{IN}$ = 600 MHz, –1 dBFS, decimate-by-4 mode | $T_A$ = 25°C(3) | | 9.7 | | Bits |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$(3) | 9.0 | | | |
| | | | $T_A$ = 25°C, calibration = BG (3) | | 9.7 | | |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$, calibration = BG(3) | 9.1 | | | |
| | | $F_{IN}$ = 2400 MHz, –1 dBFS, decimate-by-4 mode(3) | | | 8.5 | | |
| SFDR1 | Spurious-free dynamic range across entire Nyquist bandwidth<br>Interleaving spurs included | $F_{IN}$ = 600 MHz, –1 dBFS, decimate-by-4 mode | $T_A$ = 25°C | | 70.1 | | dBFS |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | 59.2 | | | |
| | | | $T_A$ = 25°C, calibration = BG | | 62.9 | | |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$, calibration = BG | 51.8 | | | |
| | | $F_{IN}$ = 2400 MHz, –1 dBFS, decimate-by-4 mode | | | 66.4 | | |
| SFDR2 | Spurious-free dynamic range across entire Nyquist bandwidth<br>Interleaving spurs excluded | $F_{IN}$ = 600 MHz, –1 dBFS, decimate-by-4 mode | $T_A$ = 25°C(3) | | 71.6 | | dBFS |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$(3) | 60 | | | |
| | | | $T_A$ = 25°C, calibration = BG (3) | | 74.8 | | |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$, calibration = BG(3) | 62.9 | | | |
| | | $F_{IN}$ = 2400 MHz, –1 dBFS, Decimate-by-4 mode(3) | | | 80.4 | | |
| $f_S/2$ | Interleaving offset spur at ½ sampling rate(4) | $F_{IN}$ = 600 MHz, –1 dBFS, decimate-by-4 mode | $T_A$ = 25°C | | –72 | | dBFS |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | –56 | |
| | | | $T_A$ = 25°C, calibration = BG | | –65 | | |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$, calibration = BG | | | –50.5 | |
| $f_S/4$ | Interleaving offset spur at ¼ sampling rate(4) | $F_{IN}$ = 600 MHz, –1 dBFS, decimate-by-4 mode | $T_A$ = 25°C | | –68 | | dBFS |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | –55 | |
| | | | $T_A$ = 25°C, calibration = BG | | –62 | | |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$, calibration = BG | | | –47.4 | |
| $f_S/2 – F_{IN}$ | Interleaving spur at ½ sampling rate – input frequency(4) | $F_{IN}$ = 600 MHz, –1 dBFS, decimate-by-4 mode | $T_A$ = 25°C | | –75 | | dBFS |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | –62.3 | |
| | | | $T_A$ = 25°C, calibration = BG | | –70 | | |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$, calibration = BG | | | –51.5 | |
| $f_S/4 + F_{IN}$ | Interleaving spur at ¼ sampling rate + input frequency(4) | $F_{IN}$ = 600 MHz, –1 dBFS, decimate-by-4 mode | $T_A$ = 25°C | | –73 | | dBFS |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | –58.9 | |
| | | | $T_A$ = 25°C, calibration = BG | | –65 | | |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$, calibration = BG | | | –52.8 | |
| $f_S/4 – F_{IN}$ | Interleaving spur at ¼ sampling rate – input frequency(4) | $F_{IN}$ = 600 MHz, –1 dBFS, Decimate-by-4 mode | $T_A$ = 25°C | | –78 | | dBFS |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | –60.4 | |
| | | | $T_A$ = 25°C, calibration = BG | | –65 | | |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$, calibration = BG | | | –52.3 | |

(4) Magnitude of reported tones in output spectrum of ADC core. This tone will only be present in the DDC output for specific Decimation and NCO settings. Careful frequency planning can be used to intentionally place unwanted tones outside the DDC output spectrum.

Copyright © 2014–2017, Texas Instruments Incorporated

## Electrical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN full scale range at default setting (725 $mV_{PP}$), VIN = –1 dBFS, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 4 GHz at 0.5 $V_{PP}$ with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a foreground (FG) mode calibration with timing calibration enabled. Typical values are at $T_A$ = 25°C.(1)(2)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| THD | Total harmonic distortion(4) | $F_{IN}$ = 600 MHz, –1 dBFS, decimate-by-4 mode | $T_A$ = 25°C | | –70 | | dBFS |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | –59.5 | |
| | | | $T_A$ = 25°C, calibration = BG | | –73 | | |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$, calibration = BG | | | –60 | |
| HD2 | Second harmonic distortion(4) | $F_{IN}$ = 600 MHz, –1 dBFS, decimate-by-4 mode | $T_A$ = 25°C | | –83 | | dBFS |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | –62 | |
| | | | $T_A$ = 25°C, calibration = BG | | –78 | | |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$, calibration = BG | | | –62.5 | |
| HD3 | Third harmonic distortion(4) | $F_{IN}$ = 600 MHz, –1 dBFS, decimate-by-4 mode | $T_A$ = 25°C | | –72 | | dBFS |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | –59.5 | |
| | | | $T_A$ = 25°C, calibration = BG | | –82 | | |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$, calibration = BG | | | –62 | |
| **DECIMATE-BY-8 MODE** | | | | | | | |
| SNR1 | Signal-to-noise ratio, integrated across DDC output bandwidth Interleaving spurs included | $F_{IN}$ = 600 MHz, –1 dBFS, decimate-by-8 mode | | | 63 | | dBFS |
| | | | Calibration = BG | | 61.6 | | |
| | | $F_{IN}$ = 2400 MHz, –1 dBFS, decimate-by-8 mode | | | 54.6 | | |
| SNR2 | Signal-to-noise ratio, integrated across DDC output bandwidth Interleaving spurs excluded | $F_{IN}$ = 600 MHz, –1 dBFS, decimate-by-8 mode(3) | | | 63.3 | | dBFS |
| | | | Calibration = BG | | 63.3 | | |
| SINAD1 | Signal-to-noise and distortion ratio, integrated across DDC output bandwidth Interleaving spurs included | $F_{IN}$ = 600 MHz, –1 dBFS, Decimate-by-8 mode | | | 63 | | dBFS |
| | | | Calibration = BG | | 61.6 | | |
| | | $F_{IN}$ = 2400 MHz, –1 dBFS, decimate-by-8 mode | | | 54.6 | | |
| SINAD2 | Signal-to-noise and distortion ratio, integrated across DDC output bandwidth Interleaving spurs excluded | $F_{IN}$ = 600 MHz, –1 dBFS, decimate-by-8 mode(3) | | | 63.3 | | dBFS |
| | | | Calibration = BG | | 63.3 | | |
| ENOB1 | Effective number of bits, integrated across DDC output bandwidth Interleaving spurs included | $F_{IN}$ = 600 MHz, –1 dBFS, decimate-by-8 mode | | | 10.2 | | Bits |
| | | | Calibration = BG | | 10.0 | | |
| | | $F_{IN}$ = 2400 MHz, –1 dBFS, decimate-by-8 mode | | | 8.8 | | |
| ENOB2 | Effective number of bits, integrated across DDC output bandwidth Interleaving spurs excluded | $F_{IN}$ = 600 MHz, –1 dBFS, decimate-by-8 mode(5) | | | 10.2 | | Bits |
| | | | Calibration = BG | | 10.2 | | |
| SFDR1 | Spurious-free dynamic range Interleaving Spurs Included | $F_{IN}$ = 600 MHz, –1 dBFS, decimate-by-8 mode | | | 74.9 | | dBFS |
| | | | Calibration = BG | | 68.3 | | |
| SFDR2 | Spurious-free dynamic range Interleaving spurs excluded | $F_{IN}$ = 600 MHz, –1 dBFS, decimate-by-8 mode(5) | | | 77.8 | | dBFS |
| | | | Calibration = BG | | 77.8 | | |
| $f_S/2$ | Interleaving offset spur at ½ sampling rate(4) | $F_{IN}$ = 600 MHz, –1 dBFS, decimate-by-8 mode | | | –73 | | dBFS |
| | | | Calibration = BG | | –72 | | |
| $f_S/4$ | Interleaving offset spur at ¼ sampling rate(4) | $F_{IN}$ = 600 MHz, –1 dBFS, decimate-by-8 mode | | | –70 | | dBFS |
| | | | Calibration = BG | | –66 | | |
| $f_S/2 – F_{IN}$ | Interleaving spur at ½ sampling rate – input frequency(4) | $F_{IN}$ = 600 MHz, –1 dBFS, decimate-by-8 mode | | | –76 | | dBFS |
| | | | Calibration = BG | | –67 | | |
| $f_S/4 + F_{IN}$ | Interleaving spur at ¼ sampling rate + input frequency(4) | $F_{IN}$ = 600 MHz, –1 dBFS, decimate-by-8 mode | | | –72 | | dBFS |
| | | | Calibration = BG | | –64 | | |
| $f_S/4 – F_{IN}$ | Interleaving spur at ¼ sampling rate – input frequency(4) | $F_{IN}$ = 600 MHz, –1 dBFS, decimate-by-8 mode | | | –74 | | dBFS |
| | | | Calibration = BG | | –67 | | |
| THD | Total harmonic distortion(6) | $F_{IN}$ = 600 MHz, –1 dBFS, decimate-by-8 mode | | | –70 | | dBFS |
| | | | Calibration = BG | | –72 | | |
| | | $F_{IN}$ = 2400 MHz, –1 dBFS, decimate-by-8 mode | | | –71 | | |
| HD2 | Second harmonic distortion(6) | $F_{IN}$ = 600 MHz, –1 dBFS, decimate-by-8 mode | | | –80 | | dBFS |
| | | | Calibration = BG | | –79 | | |
| | | $F_{IN}$ = 2400 MHz, –1 dBFS, decimate-by-8 mode | | | –78 | | |


Copyright © 2014–2017, Texas Instruments Incorporated

## Electrical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN full scale range at default setting (725 $mV_{PP}$), VIN = –1 dBFS, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 4 GHz at 0.5 $V_{PP}$ with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a foreground (FG) mode calibration with timing calibration enabled. Typical values are at $T_A$ = 25°C.(1)(2)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| HD3 | Third harmonic distortion(6) | $F_{IN}$ = 600 MHz, –1 dBFS, decimate-by-8 mode | | | –74 | | dBFS |
| | | | Calibration = BG | | –80 | | |
| | | $F_{IN}$ = 2400 MHz, –1 dBFS, decimate-by-8 mode | | | –-77 | | |
| **DDC CHARACTERISTICS** | | | | | | | |
| | Alias protection(5) | | | 80 | | | dB |
| | Alias protected bandwidth(5) | | | 80 | | | % of output BW |
| SFDR-DDC | Spurious-free dynamic range of digital down-converter(5) | | | 100 | | | dB |
| | Implementation loss(5) | | | | | 0.5 | dB |
| **ANALOG INPUT CHARACTERISTICS** | | | | | | | |
| $V_{ID(VIN)}$ | Full-scale analog-differential input range | Minimum FSR setting(6) | | | 500 | | $mV_{PP}$ |
| | | Default FSR setting, $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | 650 | 725 | 800 | |
| | | Maximum FSR setting(6) | | | 950 | | |
| $C_{I(VIN)}$ | Analog input capacitance(5) | Differential | | | 0.05 | | pF |
| | | Each input pin to ground | | | 1.5 | | pF |
| $R_{ID(VIN)}$ | Differential input resistance | | | 80 | 95 | 110 | Ω |
| FPBW | Full power bandwidth | –3 dB — calibration = BG | | | 2.8 | | GHz |
| | | –3 dB — calibration = FG | | | 3.2 | | |
| | Gain flatness | DC to 2 GHz | | | 1.2 | | dB |
| | | 2 GHz to 4 GHz | | | 3.8 | | |
| | | DC to 2 GHz — calibration = BG | | | 1.5 | | |
| | | 2 GHz to 4 GHz — calibration = BG | | | 4.5 | | |
| **ANALOG OUTPUT CHARACTERISTICS (VCMO, VBG)** | | | | | | | |
| $V_{(VCMO)}$ | Common-mode output voltage | $I_{(VCMO)}$ = ±100 µA, $T_A$ = 25°C | | | 1.225 | | V |
| | | $I_{(VCMO)}$ = ±100 µA, $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | 1.185 | | 1.265 | |
| $TCV_{O(VCMO)}$ | Common-mode output-voltage temperature coefficient | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | -21 | | ppm/°C |
| $C_{(LOAD_VCMO)}$ | Maximum VCMO output load capacitance | | | | | 80 | pF |
| $V_{O(BG)}$ | Bandgap reference output voltage | $I_{(BG)}$ = ±100 µA, $T_A$ = 25°C | | | 1.248 | | V |
| | | $I_{(BG)}$ = ±100 µA, $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | 1.195 | | 1.3 | |
| $TCV_{ref(BG)}$ | Bandgap reference voltage temperature coefficient | $T_A$ = $T_{MIN}$ to $T_{MAX}$, $I_{(BG)}$ = ±100 µA | | | 0 | | ppm/°C |
| $C_{(LOAD_BG)}$ | Maximum bandgap reference output load capacitance | | | | | 80 | pF |
| **TEMPERATURE DIODE CHARACTERISTICS** | | | | | | | |
| $V_{(TDIODE)}$ | Temperature diode voltage slope | Offset voltage (approx. 0.77 V) varies with process and must be measured for each part. Offset measurement should be done with PowerDown=1 to minimize device self-heating. | 100-µA forward current Device active | | –1.6 | | mV/°C |
| | | | 100-µA forward current Device in power-down | | –1.6 | | mV/°C |

(5) This parameter is specified by design and is not tested in production.
(6) This parameter is specified by design, characterization, or both and is not tested in production.

## Electrical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN full scale range at default setting (725 $mV_{PP}$), VIN = –1 dBFS, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 4 GHz at 0.5 $V_{PP}$ with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a foreground (FG) mode calibration with timing calibration enabled. Typical values are at $T_A$ = 25°C.(1)(2)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **CLOCK INPUT CHARACTERISTICS (DEVCLK±, SYSREF±, SYNC~)** | | | | | | |
| $V_{ID(CLK)}$ | Differential clock input level | Sine wave clock, $T_A$ = $T_{MIN}$ to $T_{MAX}$ | 0.4 | 0.6 | 2 | $V_{PP}$ |
| | | Square wave clock, $T_A$ = $T_{MIN}$ to $T_{MAX}$ | 0.4 | 0.6 | 2 | $V_{PP}$ |
| $I_{I(CLK)}$ | Input current | $V_I$ = 0 or $V_I$ = $V_A$ | | ±1 | | µA |
| $C_{I(CLK)}$ | Input capacitance(5) | Differential | | 0.02 | | pF |
| | | Each input to ground | | 1 | | pF |
| $R_{ID(CLK)}$ | Differential input resistance | $T_A$ = 25°C | | 95 | | Ω |
| | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | 80 | | 110 | Ω |
| **CML OUTPUT CHARACTERISTICS (DS0–DS7±)** | | | | | | |
| $V_{OD}$ | Differential output voltage | Assumes ideal 100-Ω load<br>Measured differentially<br>Default pre-emphasis setting | 280 | 305 | 330 | mV peak |
| $V_{O(ofs)}$ | Output offset voltage | | | 0.6 | | V |
| $I_{OS}$ | Output short-circuit current | Output+ and output– shorted together | | ±6 | | mA |
| | | Output+ or output– shorted to 0 V | | 12 | | |
| $Z_{OD}$ | Differential output impedance | | | 100 | | Ω |
| **LVCMOS INPUT CHARACTERISTICS (SDI, SCLK, $\overline{SCS}$, SYNC~)** | | | | | | |
| $V_{IH}$ | Logic high input voltage | See (6) | 0.83 | | | V |
| $V_{IL}$ | Logic low input voltage | See (6) | | | 0.4 | V |
| $C_I$ | Input capacitance(5)(7) | Each input to ground | | 1 | | pF |
| **LVCMOS OUTPUT CHARACTERISTICS (SDO, OR_T0, OR_T1)** | | | | | | |
| $V_{OH}$ | CMOS H level output | $I_{OH}$ = –400 µA(6) | 1.65 | 1.9 | | V |
| $V_{OL}$ | CMOS L level output | $I_{OH}$ = 400 µA(6) | | 0.01 | 0.15 | V |
| **POWER SUPPLY CHARACTERISTICS** | | | | | | |
| $I_{(VA19)}$ | Analog 1.9-V supply current | PD = 0, calibration = BG, decimate by 8, DDR = 0, P54 = 1 | | 560 | 607 | mA |
| $I_{(VA12)}$ | Analog 1.2-V supply current | PD = 0, calibration = BG, decimate by 8, DDR = 0, P54 = 1 | | 377 | 428 | mA |
| $I_{(VD12)}$ | Digital 1.2-V supply current | PD = 0, calibration = BG, decimate by 8, DDR = 0, P54 = 1 | | 541 | 826 | mA |
| $P_C$ | Power consumption | PD = 0, calibration = BG, decimate by 8, DDR = 0, P54 = 1 | | 2.17 | 2.66 | W |
| | | PD = 1 | | < 50 | | mW |

(7) The digital control pin capacitances are die capacitances only and is in addition to package and bond-wire capacitance of approximately 0.4 pF.

## 6.6 Timing Requirements

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DEVICE (SAMPLING) CLOCK** | | | | | | |
| $f_{(DEVCLK)}$ | Input DEVCLK frequency | Sampling rate is equal to clock input | 1 | | 4 | GHz |
| $t_{d(A)}$ | Sampling (aperture) delay | Input CLK transition to sampling instant | | 0.64 | | ns |
| $t_{(AJ)}$ | Aperture jitter | | | 0.1 | | ps RMS |


Copyright © 2014–2017, Texas Instruments Incorporated

## Timing Requirements (continued)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{(LAT_DDC)}$ | ADC core and DDC latency(1) | Decimation = 4, DDR = 1, P54 = 0 | | 292 | | $t_{(DEVCLK)}$ |
| | | Decimation = 4, DDR = 1, P54 = 1 | | 284 | | |
| | | Decimation = 8, DDR = 0, P54 = 0 | | 384 | | |
| | | Decimation = 8, DDR = 0, P54 = 1 | | 368 | | |
| | | Decimation = 8, DDR = 1, P54 = 0 | | 392 | | |
| | | Decimation = 8, DDR = 1, P54 = 1 | | 368 | | |
| | | Decimation = 10, DDR = 0, P54 = 0 | | 386 | | |
| | | Decimation = 10, DDR = 1, P54 = 0 | | 386 | | |
| | | Decimation = 16, DDR = 0, P54 = 0 | | 608 | | |
| | | Decimation = 16, DDR = 0, P54 = 1 | | 560 | | |
| | | Decimation = 16, DDR = 1, P54 = 0 | | 608 | | |
| | | Decimation = 16, DDR = 1, P54 = 1 | | 560 | | |
| | | Decimation = 20, DDR = 0, P54 = 0 | | 568 | | |
| | | Decimation = 20, DDR = 1, P54 = 0 | | 568 | | |
| | | Decimation = 32, DDR = 0, P54 = 0 | | 1044 | | |
| | | Decimation = 32, DDR = 0, P54 = 1 | | 948 | | |
| | | Decimation = 32, DDR = 1, P54 = 0 | | 1044 | | |
| **JESD204B INTERFACE LINK TIMING CHARACTERISTICS (REFER TO Figure 1)** | | | | | | |
| $t_{d(LMFC)}$ | SYSREF to LMFC delay<br>Functional delay between SYSREF assertion latched and LMFC frame boundary(1) | All decimation modes | | 40 | | $t_{(DEVCLK)}$ |
| $t_{d(TX)}$ | LMFC to frame boundary delay - decimation modes<br>Functional delay from LMFC frame boundary to beginning of next multi-frame in transmitted data(2) | Decimation = 4, DDR = 1, P54 = 0 | | 52.7 | | $t_{(DEVCLK)}$ |
| | | Decimation = 4, DDR = 1, P54 = 1 | | 43.9 | | |
| | | Decimation = 8, DDR = 0, P54 = 0 | | 60.7 | | |
| | | Decimation = 8, DDR = 0, P54 = 1 | | 51.5 | | |
| | | Decimation = 8, DDR = 1, P54 = 0 | | 52.7 | | |
| | | Decimation = 8, DDR = 1, P54 = 1 | | 43.9 | | |
| | | Decimation = 10, DDR = 0, P54 = 0 | | 60.7 | | |
| | | Decimation = 10, DDR = 1, P54 = 0 | | 52.7 | | |
| | | Decimation = 16, DDR = 0, P54 = 0 | | 60.7 | | |
| | | Decimation = 16, DDR = 0, P54 = 1 | | 51.5 | | |
| | | Decimation = 16, DDR = 1, P54 = 0 | | 52.7 | | |
| | | Decimation = 16, DDR = 1, P54 = 1 | | 43.9 | | |
| | | Decimation = 20, DDR = 0, P54 = 0 | | 60.7 | | |
| | | Decimation = 20, DDR = 1, P54 = 0 | | 52.7 | | |
| | | Decimation = 32, DDR = 0, P54 = 0 | | 60.7 | | |
| | | Decimation = 32, DDR = 0, P54 = 1 | | 51.5 | | |
| | | Decimation = 32, DDR = 1, P54 = 0 | | 52.7 | | |
| $t_{su(SYNC\sim F)}$ | SYNC~ to LMFC setup time(3)<br>Required SYNC~ setup time relative to the internal LMFC boundary. | | | 40 | | $t_{(DEVCLK)}$ |
| $t_{h(SYNC\sim F)}$ | SYNC~ to LMFC hold time(3)<br>Required SYNC~ hold time relative to the internal LMFC boundary. | | | –8 | | |
| $t_{(SYNC\sim)}$ | SYNC~ assertion time<br>Required SYNC~ assertion time before deassertion to initiate a link resynchronization. | | | 4 | | Frame clock cycles |
| $t_{d(LMFC)}$ | Delay from SYSREF sampled high by DEVCLK to internal LMFC boundary | | | 40 | | $t_{(DEVCLK)}$ |
| $t_{(ILA)}$ | Duration of initial lane alignment sequence | | | 4 | | Multi-frame clock cycles |

(1) Unless otherwise specified, delays quoted are exact un-rounded functional delays (assuming zero propagation delay).
(2) The values given are functional delays only. Additional propagation delay of 0 to 3 clock cycles will be present.
(3) This parameter must be met to achieve deterministic alignment of the data frame and NCO phase to other similar devices. If this parameter is not met the device will still function correctly but will not be aligned to other devices.

Copyright © 2014–2017, Texas Instruments Incorporated

## Timing Requirements (continued)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SYSREF** | | | | | | |
| $t_{su(SYS)}$ | Setup time SYSREF relative to DEVCLK rising edge[4] | | | 40 | | ps |
| $t_{h(SYS)}$ | Hold time SYSREF relative to DEVCLK rising edge[4] | | | 40 | | ps |
| $t_{(PH_SYS)}$ | SYSREF assertion duration after rising edge event. | | 8 | | | $t_{(DEVCLK)}$ |
| $t_{(PL_SYS)}$ | SYSREF deassertion duration after falling edge event. | | 8 | | | $t_{(DEVCLK)}$ |
| $t_{(SYS)}$ | Period SYSREF± | DDR = 0, P54 = 0 | | K × F × 10 | | $t_{(DEVCLK)}$ |
| | | DDR = 0, P54 = 1 | | K × F × 8 | | |
| | | DDR = 1, P54 = 0 | | K × F × 5 | | |
| | | DDR = 1, P54 = 1 | | K × F × 4 | | |
| **SERIAL INTERFACE (REFER TO Figure 2)** | | | | | | |
| $f_{(SCK)}$ | Serial clock frequency[5] | | | | 20 | MHz |
| $t_{(PH)}$ | Serial clock high time | | 20 | | | ns |
| $t_{(PL)}$ | Serial clock low time | | 20 | | | ns |
| $t_{su}$ | Serial-data to serial-clock rising setup time[5] | | 10 | | | ns |
| $t_h$ | Serial-data to serial clock rising hold time[5] | | 10 | | | ns |
| $t_{(CSS)}$ | $\overline{SCS}$-to-serial clock rising setup time | | 10 | | | ns |
| $t_{(CSH)}$ | $\overline{SCS}$-to-serial clock falling hold time | | 10 | | | ns |
| $t_{(IAG)}$ | Inter-access gap | | 10 | | | ns |

(4) This parameter is specified by design, characterization, or both and is not tested in production.
(5) This parameter is specified by design and is not tested in production.

## 6.7 Internal Characteristics

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DEVICE (SAMPLING) CLOCK** | | | | | | |
| $t_{d(A)}$ | Sampling (aperture) delay | Input CLK transition to sampling instant | | 0.64 | | ns |
| $t_{(AJ)}$ | Aperture jitter | | | 0.1 | | ps RMS |
| **CALIBRATION TIMING CHARACTERISTICS (REFER TO THE *CALIBRATION* SECTION)** | | | | | | |
| $t_{(CAL)}$ | Calibration cycle time | Calibration = FG, T_AUTO=1 | | | $227 \times 10^6$ | $t_{(DEVCLK)}$ |
| | | Calibration = FG, T_AUTO=0 | | | $102 \times 10^6$ | |
| **JESD204B INTERFACE LINK TIMING CHARACTERISTICS (REFER TO Figure 1)** | | | | | | |
| $t_{d(LMFC)}$ | SYSREF to LMFC delay<br>Functional delay between SYSREF assertion latched and LMFC frame boundary[1] | All decimation modes | | 40 | | $t_{(DEVCLK)}$ |

(1) Unless otherwise specified, delays quoted are exact un-rounded functional delays (assuming zero propagation delay).


Copyright © 2014–2017, Texas Instruments Incorporated

## Internal Characteristics (continued)

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{d(TX)}$ | LMFC to frame boundary delay - decimation modes<br>Functional delay from LMFC frame boundary to beginning of next multi-frame in transmitted data(2) | Decimation = 4, DDR = 1, P54 = 0 | | 52.7 | | $t_{(DEVCLK)}$ |
| | | Decimation = 4, DDR = 1, P54 = 1 | | 43.9 | | |
| | | Decimation = 8, DDR = 0, P54 = 0 | | 60.7 | | |
| | | Decimation = 8, DDR = 0, P54 = 1 | | 51.5 | | |
| | | Decimation = 8, DDR = 1, P54 = 0 | | 52.7 | | |
| | | Decimation = 8, DDR = 1, P54 = 1 | | 43.9 | | |
| | | Decimation = 10, DDR = 0, P54 = 0 | | 60.7 | | |
| | | Decimation = 10, DDR = 1, P54 = 0 | | 52.7 | | |
| | | Decimation = 16, DDR = 0, P54 = 0 | | 60.7 | | |
| | | Decimation = 16, DDR = 0, P54 = 1 | | 51.5 | | |
| | | Decimation = 16, DDR = 1, P54 = 0 | | 52.7 | | |
| | | Decimation = 16, DDR = 1, P54 = 1 | | 43.9 | | |
| | | Decimation = 20, DDR = 0, P54 = 0 | | 60.7 | | |
| | | Decimation = 20, DDR = 1, P54 = 0 | | 52.7 | | |
| | | Decimation = 32, DDR = 0, P54 = 0 | | 60.7 | | |
| | | Decimation = 32, DDR = 0, P54 = 1 | | 51.5 | | |
| | | Decimation = 32, DDR = 1, P54 = 0 | | 52.7 | | |
| $t_{d(LMFC)}$ | Delay from SYSREF sampled high by DEVCLK to internal LMFC boundary | | | 40 | | $t_{(DEVCLK)}$ |
| $t_{(ILA)}$ | Duration of initial lane alignment sequence | | | 4 | | Multi-frame clock cycles |

(2) The values given are functional delays only. Additional propagation delay of 0 to 3 clock cycles will be present.

## 6.8 Switching Characteristics

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN FSR (AC coupled) = Default setting, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 4 GHz at 0.5 $V_{PP}$ with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a foreground mode calibration with timing calibration enabled. Typical values are at $T_A$ = 25°C.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SERIAL DATA OUTPUTS** | | | | | | |
| | Serialized output bit rate | | 1 | | 10 | Gbps |
| | Serialized output bit rate | DDR = 0, P54 = 0 | | $f_S$ | | |
| | | DDR = 0, P54 = 1 | | 1.25 × $f_S$ | | |
| | | DDR = 1, P54 = 0 | | 2 × $f_S$ | | |
| | | DDR = 1, P54 = 1 | | 2.5 × $f_S$ | | |
| $t_{TLH}$ | LH transition time — differential | 10% to 90%, 8 Gbps | | 35 | | ps |
| $t_{THL}$ | HL transition time — differential | 10% to 90%, 8 Gbps | | 35 | | ps |
| UI | Unit interval | 8 Gbps serial rate | | 125 | | ps |
| DDJ | Data dependent jitter | 8 Gbps serial rate | | 11.3 | | ps |
| RJ | Random Jitter | 8 Gbps serial rate | | 1.4 | | ps |
| **SERIAL INTERFACE** | | | | | | |
| $t_{(OZD)}$ | SDO tri-state to driven | See Figure 2 | | | 5 | ns |
| $t_{(ODZ)}$ | SDO driven to tri-state | See Figure 2 | 2.5 | | 5 | ns |
| $t_{(OD)}$ | SDO output delay | See Figure 2 | | | 20 | ns |

Copyright © 2014–2017, Texas Instruments Incorporated

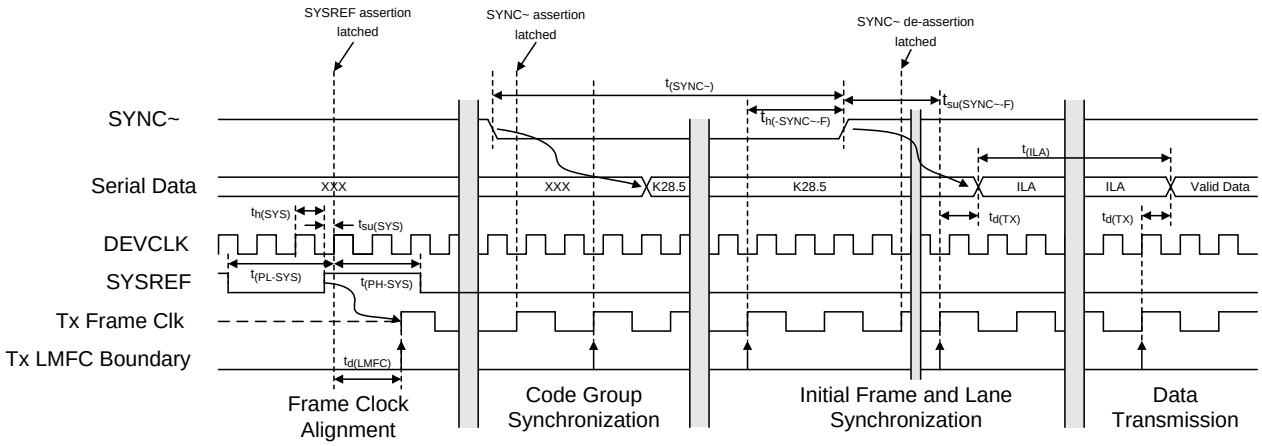



**Figure 1. JESD204 Synchronization**

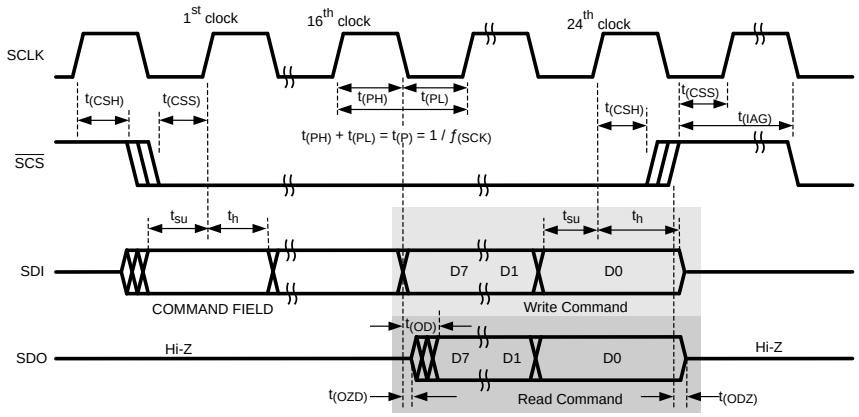
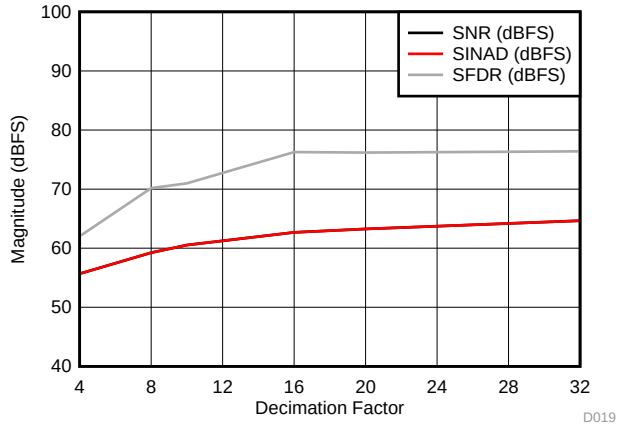



**Figure 2. Serial Interface Timing**


Copyright © 2014–2017, Texas Instruments Incorporated

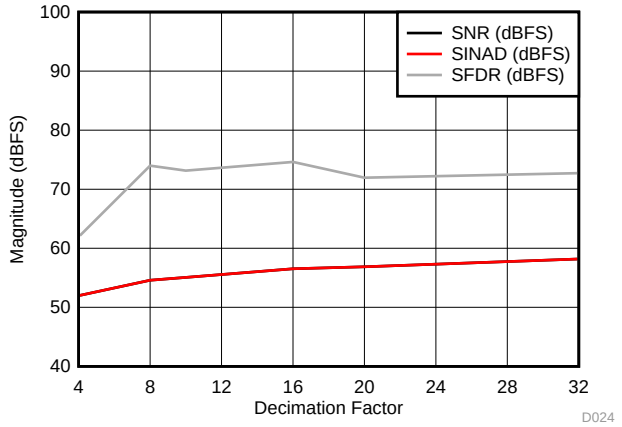
## 6.9 Typical Characteristics

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN FSR (AC coupled) = Default setting, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 4 GHz at 0.5 $V_{PP}$ with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a Foreground mode calibration with Timing Calibration enabled. $T_A$ = 25°C. $V_I$ = –1 dBFS.



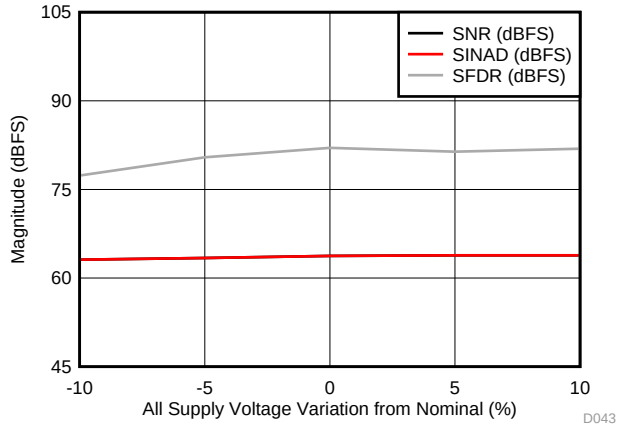

$F_{IN}$ = 608 MHz

**Figure 3. SNR, SINAD, SFDR vs Decimation Setting**



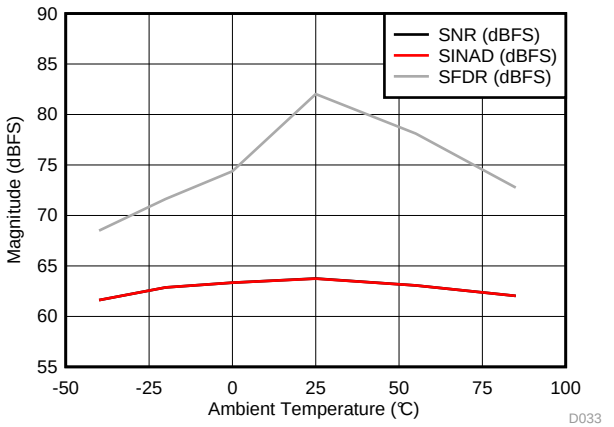

$F_{IN}$ = 2483 MHz

**Figure 4. SNR, SINAD, SFDR vs Decimation Setting**



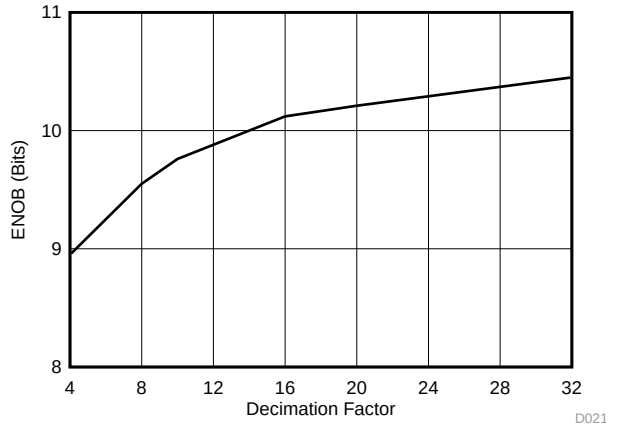

Decimate by 16 mode $F_{IN}$ = 608 MHz

**Figure 5. SNR, SINAD, SFDR vs Supply**



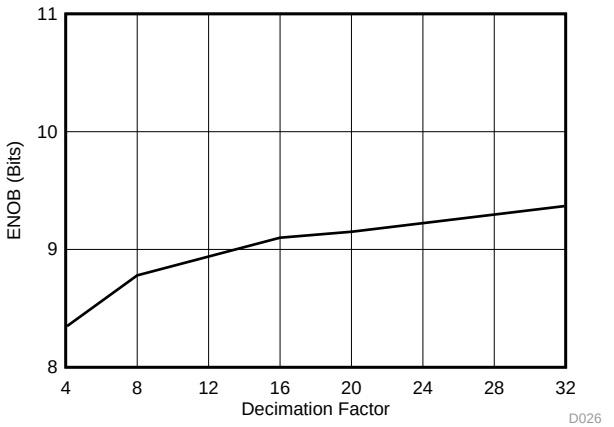

Decimate by 16 mode $F_{IN}$ = 608 MHz

**Figure 6. SNR, SINAD, SFDR vs Temperature**




$F_{IN}$ = 608 MHz

**Figure 7. ENOB vs Decimation Setting**



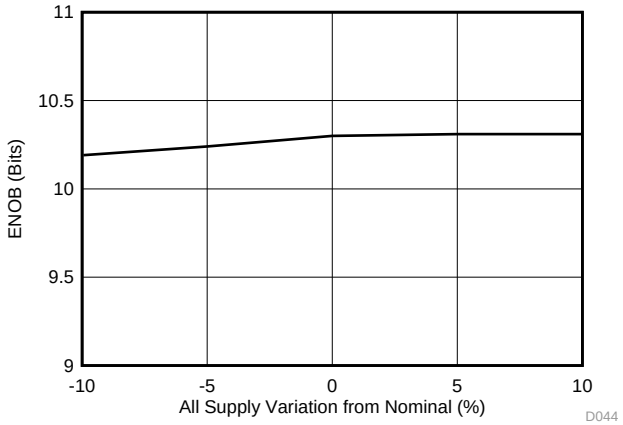

$F_{IN}$ = 2483 MHz

**Figure 8. ENOB vs Decimation Setting**

Copyright © 2014–2017, Texas Instruments Incorporated

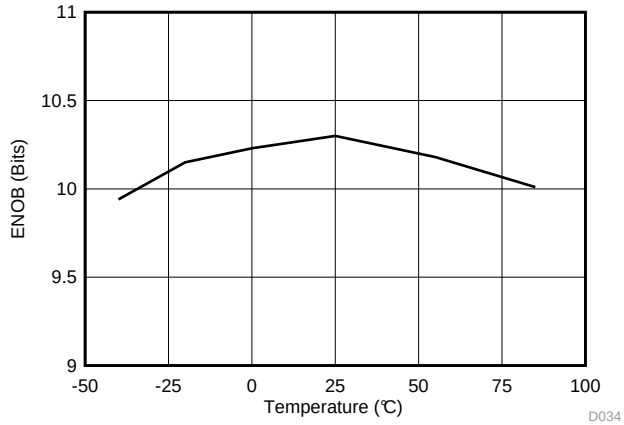
## Typical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN FSR (AC coupled) = Default setting, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 4 GHz at 0.5 $V_{PP}$ with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a Foreground mode calibration with Timing Calibration enabled. $T_A$ = 25°C. $V_I$ = –1 dBFS.



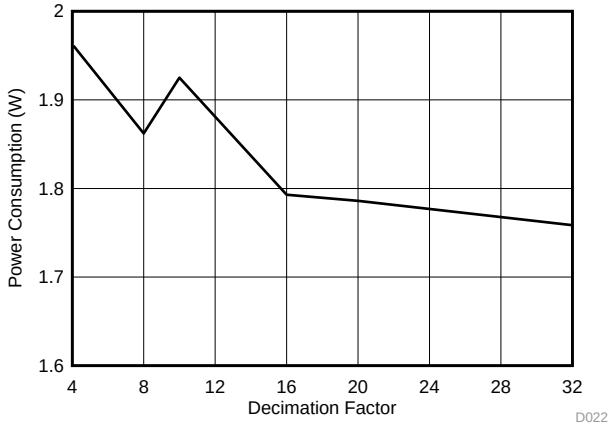

Decimate by 16 mode $F_{IN}$ = 608 MHz

**Figure 9. ENOB vs Supply**



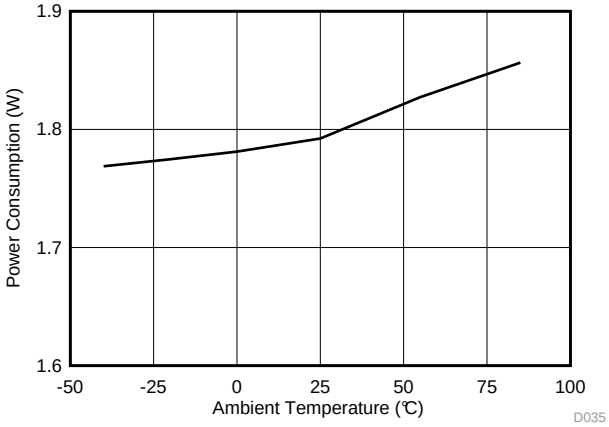

Decimate by 16 mode $F_{IN}$ = 608 MHz

**Figure 10. ENOB vs Temperature**



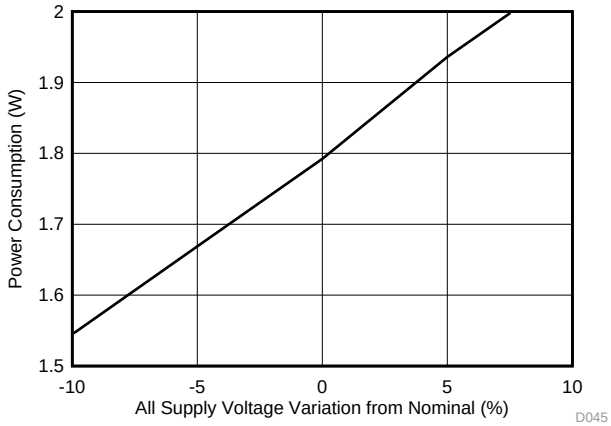

$F_{IN}$ = 608 MHz

**Figure 11. Power Consumption vs Decimation Setting**



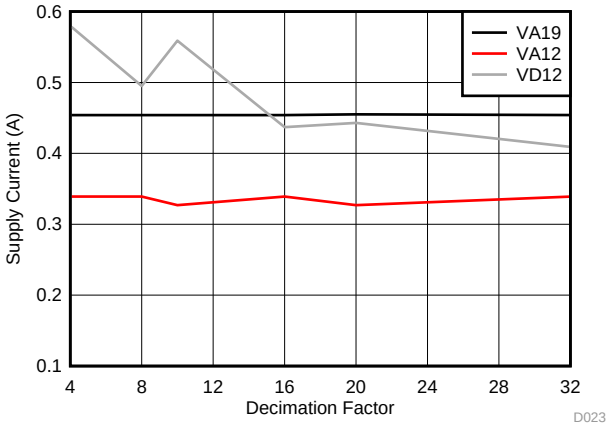

Decimate by 16 mode $F_{IN}$ = 608 MHz

**Figure 12. Power Consumption vs Temperature**




Decimate by 16 mode $F_{IN}$ = 608 MHz

**Figure 13. Power Consumption vs Supply**




$F_{IN}$ = 608 MHz

**Figure 14. Supply Current vs Decimation Setting**


Copyright © 2014–2017, Texas Instruments Incorporated

## Typical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN FSR (AC coupled) = Default setting, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 4 GHz at 0.5 $V_{PP}$ with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a Foreground mode calibration with Timing Calibration enabled. $T_A$ = 25°C. $V_I$ = –1 dBFS.

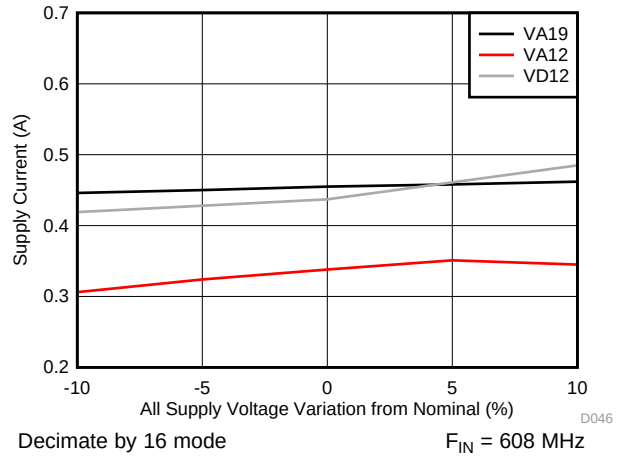



**Figure 15. Supply Current vs Supply Voltage**

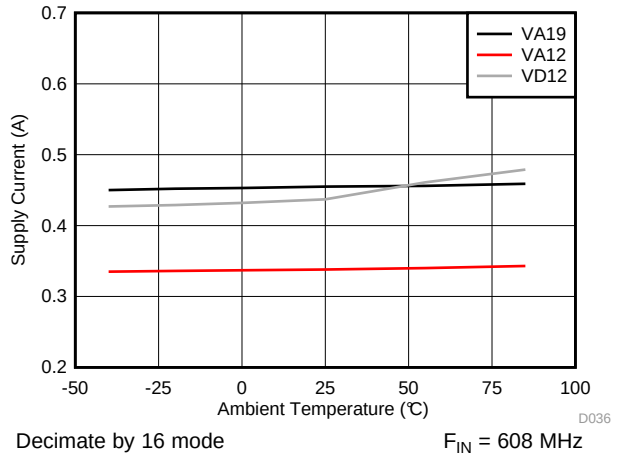



**Figure 16. Supply Current vs Temperature**

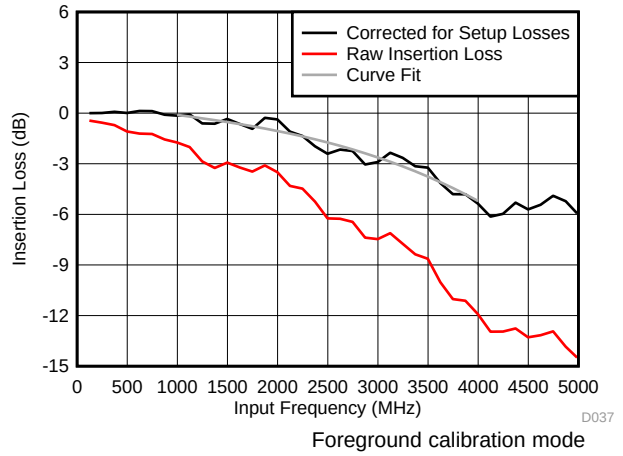



**Figure 17. Insertion Loss vs Input Frequency**

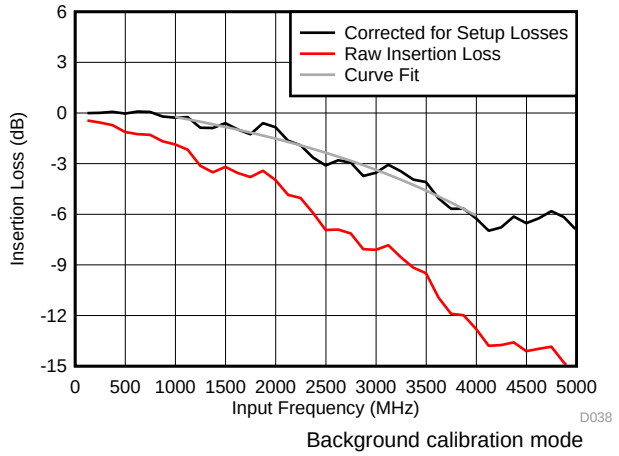



**Figure 18. Insertion Loss vs Input Frequency**

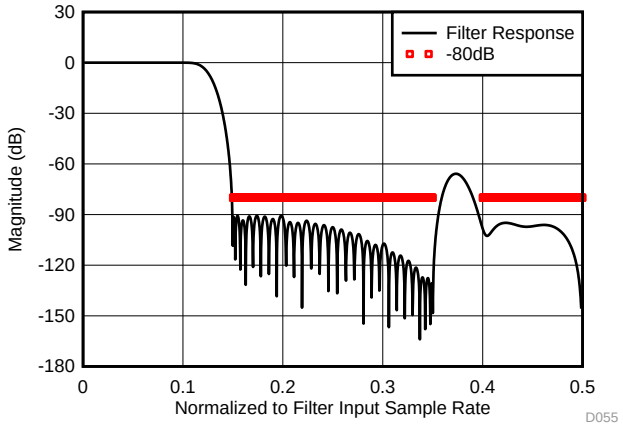



**Figure 19. Decimate by 4 - Stopband Response**

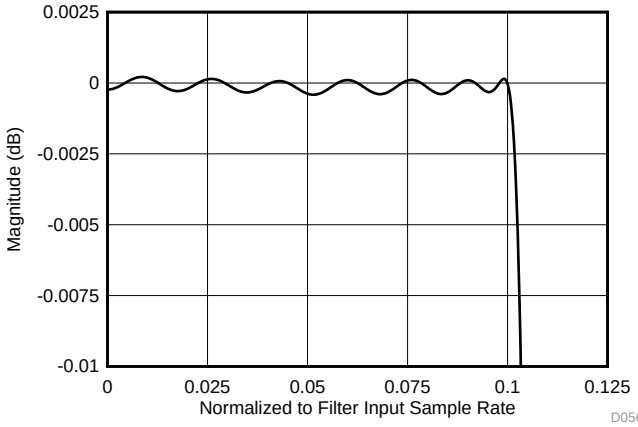



**Figure 20. Decimate by 4 - Passband Response**

Copyright © 2014–2017, Texas Instruments Incorporated

## Typical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN FSR (AC coupled) = Default setting, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 4 GHz at 0.5 $V_{PP}$ with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a Foreground mode calibration with Timing Calibration enabled. $T_A$ = 25°C. $V_I$ = –1 dBFS.

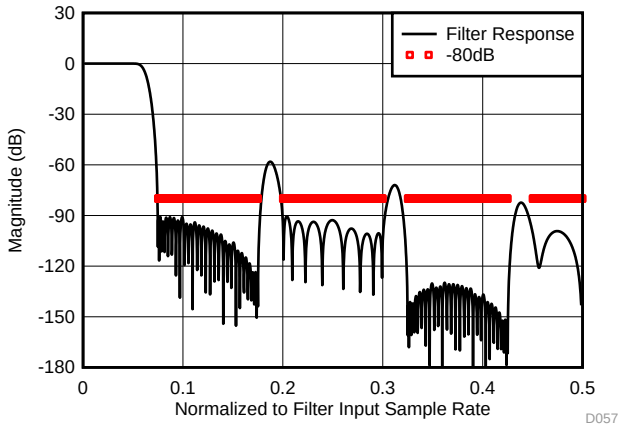



**Figure 21. Decimate by 8 - Stopband Response**

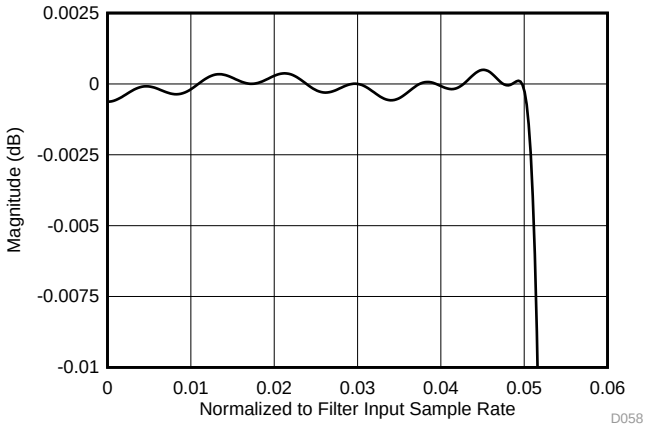



**Figure 22. Decimate by 8 - Passband Response**

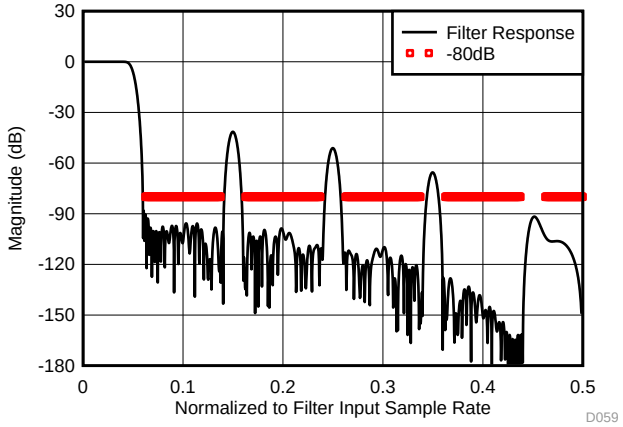



**Figure 23. Decimate by 10 - Stopband Response**

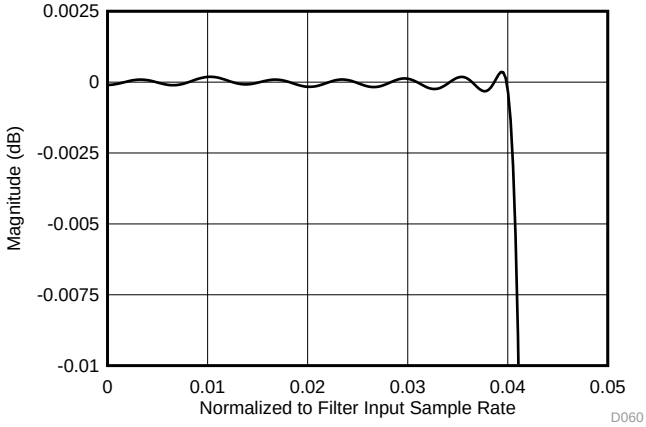



**Figure 24. Decimate by 10 - Passband Response**

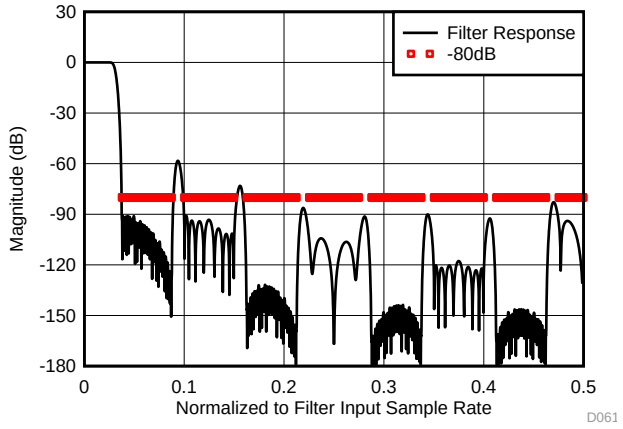



**Figure 25. Decimate by 16 - Stopband Response**

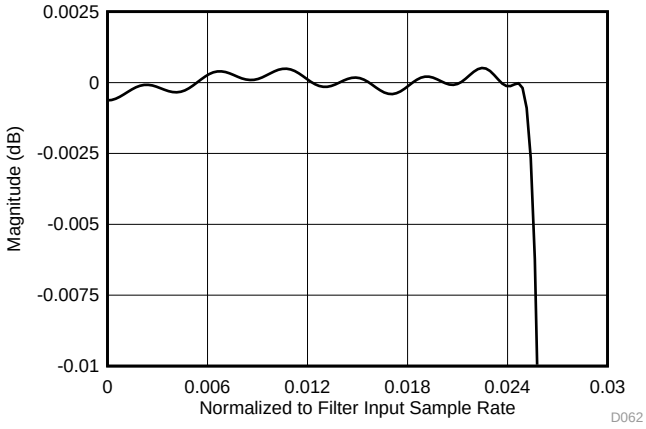



**Figure 26. Decimate by 16 - Passband Response**


Copyright © 2014–2017, Texas Instruments Incorporated

## Typical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN FSR (AC coupled) = Default setting, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 4 GHz at 0.5 $V_{PP}$ with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a Foreground mode calibration with Timing Calibration enabled. $T_A$ = 25°C. $V_I$ = –1 dBFS.

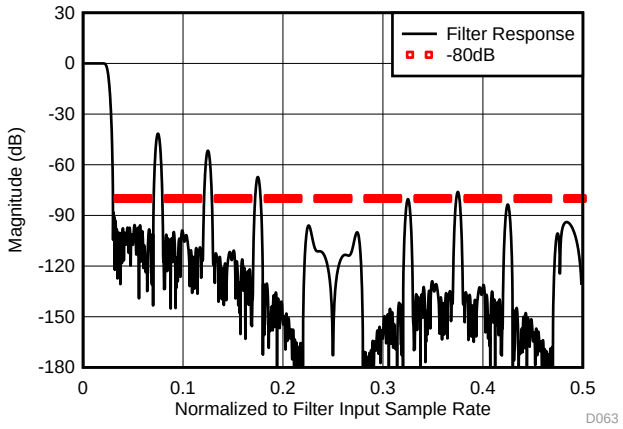



**Figure 27. Decimate by 20 - Stopband Response**

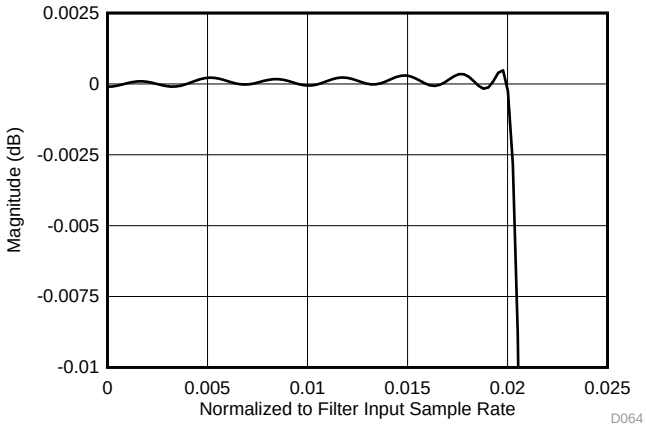



**Figure 28. Decimate by 20 - Passband Response**

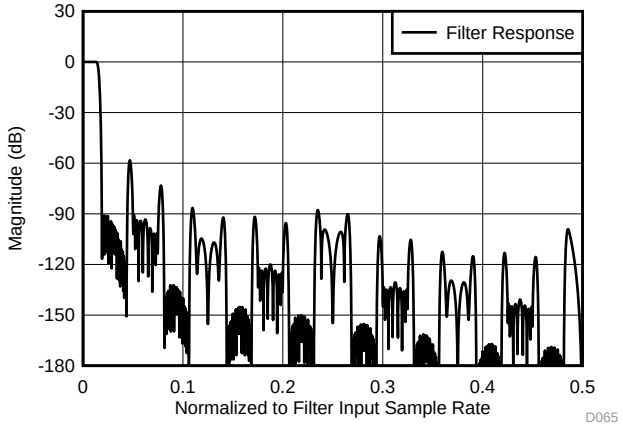



**Figure 29. Decimate by 32 - Stopband Response**

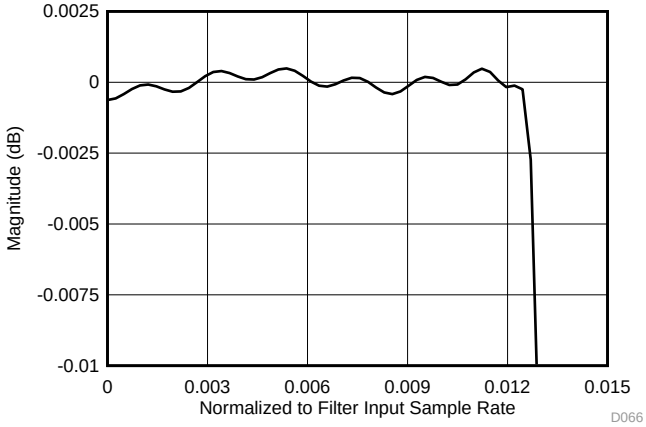



**Figure 30. Decimate by 32 - Passband Response**

Copyright © 2014–2017, Texas Instruments Incorporated

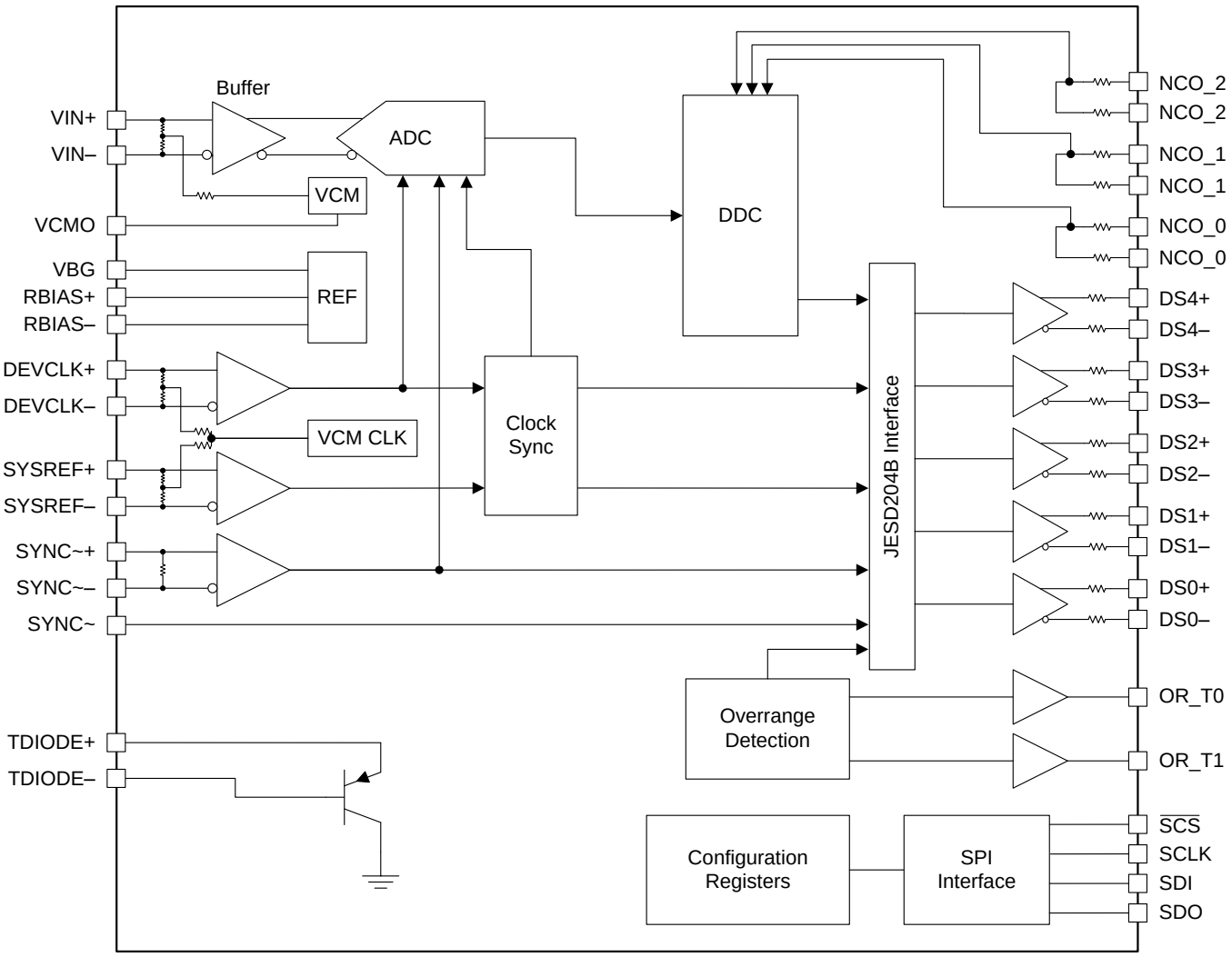
# 7 Detailed Description

## 7.1 Overview

The LM15851 device is an ultra-wideband sampling and digital tuning subsystem. The device combines a very-wideband and high sampling-rate ADC front-end with a configurable digital-down conversion block. This combination provides the necessary features to facilitate the development of flexible software-defined radio products for a wide range of communications applications.

The LM15851 device is based on an ultra high-speed ADC core. The core uses an interleaved calibrated folding and interpolating architecture that results in very high sampling rate, very good dynamic performance, and relatively low-power consumption. This ADC core is followed by a configurable DDC block which is implemented on a small geometry CMOS. The DDC block provides a range of decimation settings that allow the product to work in ultra-wideband, wideband, and more-narrow-band receive systems. The output data from the DDC block is transmitted through a JESD204B-compatible multi-lane serial-output system. This system minimizes the number of data pairs required to convey the output data to the downstream processing circuitry.

## 7.2 Functional Block Diagram





Copyright © 2014–2017, Texas Instruments Incorporated

## Functional Block Diagram (continued)

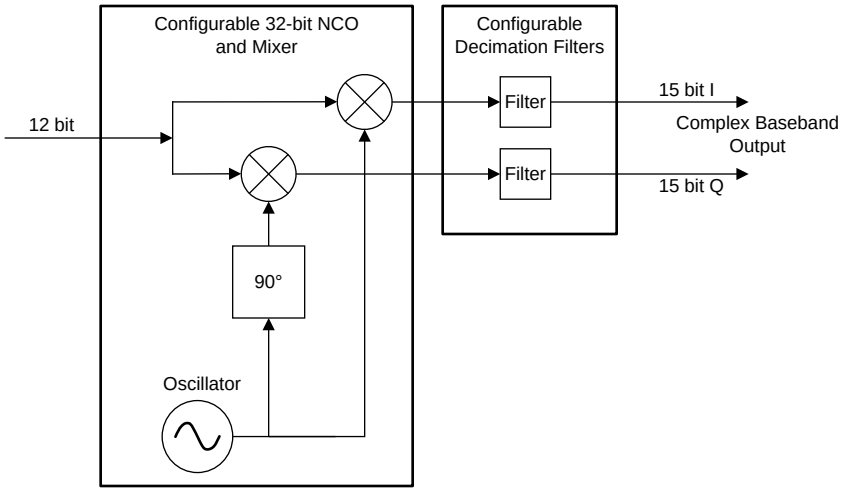



**Figure 31. DDC Details Block Diagram**

## 7.3 Feature Description

### 7.3.1 Signal Acquisition

The analog input is sampled on the rising edge of CLK and the digital equivalent of that data is available in the serialized datastream $t_{(LAT)}$ or $t_{(LAT_DDC)}$ input clock cycles later.

The LM15851 device converts as long as the input clock signal is present. The fully-differential comparator design and the innovative design of the sample-and-hold amplifier, together with calibration, enables very good performance at input frequencies beyond 3 GHz. The LM15851 data is output on a high-speed serial JESD204B interface.

### 7.3.2 The Analog Inputs

A differential input signal must be used to drive the LM15851 device. Operation with a single-ended signal is not recommended as performance suffers. The input signals can be either be AC coupled or DC coupled. The analog inputs are internally connected to the $V_{CMO}$ bias voltage. When DC-coupled input signals are used, the common mode voltage of the applied signal must meet the device Input common mode requirements. See $V_{CMI}$ in the *Recommended Operating Conditions* table.

The full-scale input range for each converter can be adjusted through the serial interface. See the *Full Scale Range Adjust* section.

The buffered analog inputs simplify the task of driving these inputs and the RC pole that is generally used at sampling ADC inputs is not required. If an amplifier circuit before the ADC is desired, use care when selecting an amplifier with adequate noise and distortion performance and adequate gain at the frequencies used for the application. If gain is not required, a balun (balanced-to-unbalanced transformer) is generally used to provide single ended (SE) to differential conversion.

The input impedance of VIN± consists of two 50-Ω resistors in series between the inputs and a capacitance from each of these inputs to ground. A resistance of approximately 20 kΩ exists from the center point of the 50-Ω resistors to the on-chip $V_{CMO}$ providing self-biasing for AC-coupled applications.

Performance is good in both DC-coupled mode and AC coupled mode, provided the common-mode voltage at the analog input is within specifications.

Copyright © 2014–2017, Texas Instruments Incorporated

## Feature Description (continued)

### 7.3.2.1 Input Clamp

The LM15851 maximum DC input voltage is limited to the range 0 to 2 V to prevent damage to the device. To help maintain these limits, an active input clamping circuit is incorporated which sources or sinks input currents up to ±50 mA. The clamping circuit is enabled by default and is controlled via the Input_Clamp_EN bit (register 0x034, bit 5). The protection provided by this circuit is limited as follows:

- Shunt current-clamping is only effective for non-zero source impedances.
- At frequencies above 3 GHz the clamping is ineffective because of the finite turn-on and turn-off time of the switch.

With these limitations in mind, analysis has been done to determine the allowable input signal levels as a function of input frequency when the Input Clamp is enabled, assuming the source impedance matches the input impedance of the device (100-Ω differential). This information is incorporated in the *Absolute Maximum Ratings* table.

### 7.3.2.2 AC Coupled Input Usage

The easiest way to accomplish SE-to-differential conversion for AC-coupled signals is with an appropriate balun.

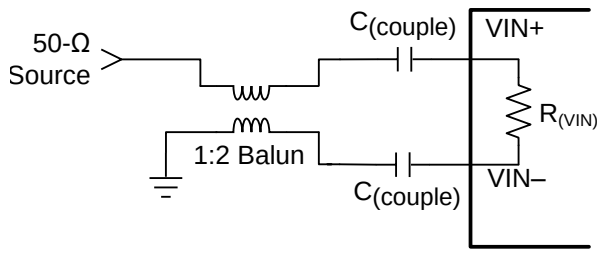



**Figure 32. Single-Ended-to-Differential Signal Conversion With a Balun**

Figure 32 shows a generic depiction of a SE-to-differential signal conversion using a balun. The circuitry specific to the balun depends on the type of balun selected and the overall board layout. TI recommends that the system designer contact the manufacturer of the selected balun to aid in designing the best performing single-ended to differential conversion circuit using that particular balun.

When selecting a balun, understanding the input architecture of the ADC is important. Specific balun parameters must be considered. The balun must match the impedance of the analog source to the on-chip 100-Ω differential input termination of the LM15851 device. The range of this input termination resistor is described in the *Electrical Characteristics* table as the specification $R_{ID}$.

Also, as a result of the ADC architecture, the phase and amplitude balance are important. The lowest possible phase and amplitude imbalance is desired when selecting a balun. The phase imbalance must be no more than ±2.5° and the amplitude imbalance must be limited to less than 1 dB at the desired input frequency range.

Finally, when selecting a balun, the voltage standing-wave ratio (VSWR), bandwidth, and insertion loss of the balun must also be considered. The VSWR aids in determining the overall transmission line termination capability of the balun when interfacing to the ADC input. The insertion loss must be considered so that the signal at the balun output is within the specified input range of the ADC as described in the *Electrical Characteristics* table as the specification $V_{ID}$.

Table 1 lists the recommended baluns for specific signal frequency ranges.

**Table 1. Balun Recommendations**

| MINIMUM FREQUENCY (MHz) | MAXIMUM FREQUENCY (MHz) | IMPEDANCE RATIO | PART NUMBER | MANUFACTURER |
|---|---|---|---|---|
| 4.5 | 3000 | 1:1 | TC1-1-13MA+ | Mini-Circuits |
| 400 | 3000 | 1:2 | B0430J50100AHF | Anaren |
| 30 | 1800 | 1:2 | ADTL2-18+ | Mini-Circuits |
| 10 | 4000 | 1:2 | TCM2-43X+ | Mini-Circuits |


Copyright © 2014–2017, Texas Instruments Incorporated

#### 7.3.2.3 DC Coupled Input Usage

When a DC-coupled signal source is used, the common mode voltage of the applied signal must be within a specified range ($V_{CMI}$). To achieve this range, the common mode of the driver should be based on the VCMO output provided for this purpose.

Full-scale distortion performance degrades as the input common-mode voltage deviates from VCMO. Therefore, maintaining the input common-mode voltage within the $V_{CMI}$ range is important.

Table 2 lists the recommended amplifiers for DC-coupled usage or if AC-coupling with gain is required.

**Table 2. Amplifier Recommendations**

| –3-dB BANDWIDTH (MHz) | MIN GAIN (dB) | MAX GAIN (dB) | GAIN TYPE | PART NUMBER |
|---|---|---|---|---|
| 7000 | 16 | 16 | Fixed | LMH3401 |
| 2800 | 0 | 17 | Resistor set | LMH6554 |
| 2400 | 6 | 26 | Digital programmable | LMH6881 |
| 900 | –1.16 | 38.8 | Digital programmable | LMH6518 |

#### 7.3.2.4 Handling Single-Ended Input Signals

The LM15851 device has no provision to adequately process single-ended input signals. The best way to handle single-ended signals is to convert these signals to balanced differential signals before presenting the signals to the ADC.

### 7.3.3 Clocking

The LM15851 device has a differential clock input, DEVCLK+ and DEVCLK–, that must be driven with an AC-coupled differential clock-signal. The clock inputs are internally terminated and biased. The input clock signal must be capacitively coupled to the clock pins as shown in Figure 33.

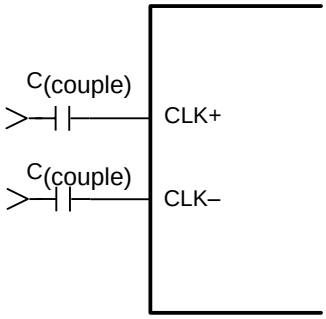



**Figure 33. Differential Sample-Clock Connection**

The differential sample-clock line pair must have a characteristic impedance of 100 Ω and must be terminated at the clock source of that 100-Ω characteristic impedance. The input clock line must be as short and direct as possible. The LM15851 clock input is internally terminated with an untrimmed 100-Ω resistance.

Insufficient input clock levels results in poor dynamic performance. Excessively-high input-clock levels can cause a change in the analog-input offset voltage. To avoid these issues, maintain the input clock level within the range specified in the *Electrical Characteristics* table.

The low times and high times of the input clock signal can affect the performance of any ADC. The LM15851 device features a duty-cycle clock-correction circuit which maintains performance over temperature. The ADC meets the performance specification when the input clock high times and low times are maintained as specified in the *Electrical Characteristics* table.

High-speed high-performance ADCs such as the LM15851 device require a very-stable input clock-signal with minimum phase noise or jitter. ADC jitter requirements are defined by the ADC resolution or ENOB (effective number of bits), maximum ADC input frequency, and the input signal amplitude relative to the ADC input full-scale range. Use Equation 1 to calculate the maximum jitter (the sum of the jitter from all sources) allowed to prevent a jitter-induced reduction in SNR.

Copyright © 2014–2017, Texas Instruments Incorporated

$$RMS_{tot(J)} = \frac{V_{FSR}}{V_{I(PP)}} \times \frac{1}{\left(2^{(n+1)} \times \pi \times F_{IN}\right)}$$

where

- $RMS_{tot(J)}$ is the RMS total of all jitter sources in seconds
- $V_{I(PP)}$ is the peak-to-peak analog input signal
- $V_{FSR}$ is the full-scale range of the ADC
- n is the ADC resolution in bits
- $F_{IN}$ is the maximum input frequency, in Hertz, at the ADC analog input (1)

Note that the maximum jitter previously described is the root sum square (RSS) of the jitter from all sources, including that from the clock source, the jitter added by noise coupling at board level and that added internally by the ADC clock circuitry, in addition to any jitter added to the input signal. Because the effective jitter added by the ADC is beyond user control, the best option is to minimize the jitter from the clock source, the sum of the externally-added input clock jitter and the jitter added by any circuitry to the analog signal.

Input clock amplitudes above those specified in the *Recommended Operating Conditions* table can result in increased input-offset voltage. Increased input-offset voltage causes the converter to produce an output code other than the expected 2048 when both input pins are at the same potential.

### 7.3.4 Over-Range Function

To ensure that system-gain management has the quickest-possible response time, a low-latency configurable over-range function is included. The over-range function works by monitoring the raw 12-bit samples exiting the ADC module. The upper 8 bits of the magnitude of the ADC data are checked against two programmable thresholds, OVR_T0 and OVR_T1. The following table lists how a raw ADC value is converted to an absolute value for a comparison of the thresholds.

| ADC SAMPLE (OFFSET BINARY) | ADC SAMPLE (2's COMPLEMENT) | ABSOLUTE VALUE | UPPER 8 BITS USED FOR COMPARISON |
|---|---|---|---|
| 1111 1111 1111 (4095) | 0111 1111 1111 (+2047) | 111 1111 1111 (2047) | 1111 1111 (255) |
| 1111 1111 0000 (4080) | 0111 1111 0000 (+2032) | 111 1111 0000 (2032) | 1111 1110 (254) |
| 1000 0000 0000 (2048) | 0000 0000 0000 (0) | 000 0000 0000 (0) | 0000 0000 (0) |
| 0000 0001 0000 (16) | 1000 0001 0000 (-2032) | 111 1111 0000 (2032) | 1111 1110 (254) |
| 0000 0000 0000 (0) | 1000 0000 0000 (-2048) | 111 1111 1111 (2047) | 1111 1111 (255) |

If the upper 8 bits of the absolute value equal or exceed the OVR_T0 or OVR_T1 threshold during the monitoring period, then the over-range bit associated with the threshold is set to 1, otherwise the over-range bit is 0. The resulting over-range bits are embedded into the complex output data samples and output on OR_T0 and OR_T1. Table 3 lists the outputs, related data samples, threshold settings and the monitoring period equation.

**Table 3. Threshold and Monitor Period for Embedded OR Bits**

| EMBEDDED OVER-RANGE OUTPUTS | ASSOCIATED THRESHOLD | ASSOCIATED SAMPLES | MONITORING PERIOD (ADC SAMPLES) |
|---|---|---|---|
| OR_T0 | OVR_T0 | In-Phase (I) samples | $2^{OVR_N}$ (1) |
| OR_T1 | OVR_T1 | Quadrature (Q) samples | |

(1) OVR_N is the monitoring period register setting.


Copyright © 2014–2017, Texas Instruments Incorporated

**Table 4. Over-Range Monitoring Period**

| OVR_N | MONITORING PERIOD |
|---|---|
| 0 | 1 |
| 1 | 2 |
| 2 | 4 |
| 3 | 8 |
| 4 | 16 |
| 5 | 32 |
| 6 | 64 |
| 7 | 128 |

Typically, the OVR_T0 threshold can be set near the full-scale value (228 for example). When the threshold is triggered, a typical system can turn down the system gain to avoid clipping. The OVR_T1 threshold can be set much lower. For example, the OVR_T1 threshold can be set to 64 (−12 dBFS). If the input signal is strong, the OVR_T1 threshold is tripped occasionally. If the input is quite weak, the threshold is never tripped. The downstream logic device monitors the OVR_T1 bit. If OVR_T1 stays low for an extended period of time, then the system gain can be increased until the threshold is occasionally tripped (meaning the peak level of the signal is above −12 dBFS).

The OR_T0 threshold is embedded as the LSB along with the upper 15 bits of every complex I sample. The OR_T1 threshold is embedded as the LSB along with the upper 15 bits of every complex Q sample.

### 7.3.5 ADC Core Features

#### *7.3.5.1 The Reference Voltage*

The reference voltage for the LM15851 device is derived from an internal bandgap reference. A buffered version of the reference voltage is available at the VBG pin for user convenience. This output has an output-current capability of ±100 μA. The VBG output must be buffered if more current is required. No provision exists for the use of an external reference voltage, but the full-scale input voltage can be adjusted through the full-scale-range register settings.

#### *7.3.5.2 Common-Mode Voltage Generation*

The internal reference voltage is used to generate a stable common-mode voltage reference for the analog Inputs and the DEVCLK and SYSREF differential-clock inputs.

#### *7.3.5.3 Bias Current Generation*

An external bias resistor, in combination with the on-chip voltage reference is used to provide an accurate and stable source of bias currents for internal circuitry. Using an external accurate resistor minimizes variation in device power consumption and performance.

#### *7.3.5.4 Full Scale Range Adjust*

The ADC input full-scale range can be adjusted through the GAIN_FS register setting (registers 0x022 and 0x023). The adjustment range is approximately 500 $mV_{PP}$ to 950 $mV_{PP}$. The full-scale range adjustment is useful for matching the input-signal amplitude to the ADC full scale, or to match the full-scale range of multiple ADCs when developing a multi-converter system.

#### *7.3.5.5 Offset Adjust*

The ADC-input offset voltage can be adjusted through the OFFSET_FS register setting (registers 0x025 and 0x026). The adjustment range is approximately 28 mV to –28 mV differential.

**NOTE**

Offset adjust has no effect when background calibration mode is enabled.

#### 7.3.5.6 Power-Down

The power-down bit (PD) allows the LM15851 device to be entirely powered down. The serial data output drivers are disabled when PD is high. When the device returns to normal operation, the JESD204 link must be re-established, and the ADC pipeline and decimation filters contain meaningless information and must be flushed.

#### 7.3.5.7 Built-In Temperature Monitor Diode

A built-in thermal monitoring diode junction is made available on the TDIODE+ and TDIODE– pins. This diode facilitates temperature monitoring and characterization of the device in higher ambient temperature environments. While the on-chip diode is not highly characterized, the diode can be used effectively by performing a baseline measurement at a known ambient or board temperature with the device in power-down (PD) mode. Recommended monitoring ICs include the LM95233 device and similar remote-diode temperature monitoring products from Texas Instruments.

### 7.3.6 Digital Down Converter (DDC)

The digitized data is the input to the digital down-converter block. This block provides frequency conversion and decimation filtering to allow a specific range of frequencies to be selected and output in the digital data stream.

#### 7.3.6.1 NCO/Mixer

The DDC contains a complex numerically-controlled oscillator and a complex mixer. The oscillator generates a complex exponential sequence shown in Equation 2.

$$x[n] = e^{j\omega n} \tag{2}$$

The frequency ($\omega$) is specified by the a 32-bit register setting. The complex exponential sequence is multiplied by the real input from the ADC to mix the desired carrier down to 0 Hz.

#### 7.3.6.2 NCO Settings

##### 7.3.6.2.1 NCO Frequency Phase Selection

Within the DDC, eight different frequency and phase settings are always available for use. Each of the eight settings uses a different phase accumulator within the NCO. Because all eight phase accumulators are continuously running independently, rapid switching between different NCO frequencies is possible allowing rapid tuning of different signals.

The specific frequency-phase pair in use is selected through either the NCO_x input pins, or the NCO_SEL configuration bits (register 0x20D, bits 2:0). The CFG_MODE bit (register 0x20C, bit 0) is used to choose whether the input pins or selection bits are used. When the CFG_MODE bit is set to 0, the NCO_x input pins select the active NCO frequency and phase setting. When the CFG_MODE bit is set to 1, the NCO_SEL register settings select the active NCO frequency and phase setting.

The frequency for each phase accumulator is programmed independently through the NCO_FREQn (and optionally NCO_RDIV) settings. The phase offset for each accumulator is programmed independently through the NCO_PHASEn register settings.

##### 7.3.6.2.2 NCO_0, NCO_1, and NCO_2 (NCO_x)

When the CFG_MODE bit is set to 0, the state of these three inputs determines the active NCO frequency and phase accumulator settings.

##### 7.3.6.2.3 NCO_SEL Bits (2:0)

When the CFG_MODE bit is set to 1, the state of these register bits determines the active NCO frequency and phase accumulator settings.


Copyright © 2014–2017, Texas Instruments Incorporated

#### 7.3.6.2.4 NCO Frequency Setting (Eight Total)

##### *7.3.6.2.4.1 Basic NCO Frequency-Setting Mode*

In basic NCO frequency-setting mode, the NCO frequency setting is set by the 32-bit register value, NCO_FREQn (n = preset 0 trough 7, see the *NCO Frequency (Preset x) Register* section).

$$(n = 0 – 7)\ f_{(NCO)} = NCO_FREQn \times 2^{-32} \times f_{(DEVCLK)} \quad (3)$$

**NOTE**

Changing the register setting after the JESD204B interface is running results in non-deterministic NCO phase. If deterministic phase is required, the JESD204B link must be re-initialized after changing the register setting. See the *Multiple ADC Synchronization* section.

##### *7.3.6.2.4.2 Rational NCO Frequency Setting Mode*

In basic NCO frequency mode, the frequency step size is very small and many frequencies can be synthesized, but sometimes an application requires very specific frequencies that fall between two frequency steps. For example with $f_S$ equal to 2457.6 MHz and a desired $f_{(NCO)}$ equal to 5.02 MHz the value for NCO_FREQ is 8773085.867. Truncating the fractional portion results in an $f_{(NCO)}$ equal to 5.0199995 MHz, which is not the desired frequency.

To produce the desired frequency, the NCO_RDIV parameter is used to force the phase accumulator to arrive at specific frequencies without error. First, select a frequency step size ($f_{(STEP)}$) that is appropriate for the NCO frequency steps required. The typical value of $f_{(STEP)}$ is 10 kHz. Next, program the NCO_RDIV value according to Equation 4.

$$NCO_RDIV = \frac{\left(\frac{f_{(DEVCLK)}}{f_{(STEP)}}\right)}{128} \quad (4)$$

The result of Equation 4 must be an integer value. If the value is not an integer, adjust either of the parameters until the result in an integer value.

For example, select a value of 1920 for NCO_RDIV.

**NOTE**

NCO_RDIV values larger than 8192 can degrade the NCO SFDR performance and are not recommended.

Now use Equation 5 to calculate the NCO_FREQ register value.

$$NCO_FREQ = \text{round} \times \left(\frac{2^{25} \times N}{NCO_RDIV}\right) \quad (5)$$

Alternatively, the following equations can be used:

$$N = \frac{f_{(NCO)}}{f_{(STEP)}} \quad (6)$$

$$NCO_FREQ = \text{round} \times \left(\frac{2^{25} \times N}{NCO_RDIV}\right) \quad (7)$$

**Table 5. Common NCO_RDIV Values (For 10-kHz Frequency Steps)**

| $f_{(DEVCLK)}$ (MHz) | NCO_RDIV |
|---|---|
| 3686.4 | 2880 |
| 3072 | 2400 |
| 2949.12 | 2304 |
| 2457.6 | 1920 |
| 1966.08 | 1536 |
| 1474.56 | 1152 |
| 1228.8 | 960 |

#### 7.3.6.2.5 NCO Phase-Offset Setting (Eight Total)

The NCO phase-offset setting is set by the 16-bit register value NCO_PHASEn (n = preset 0 trough 7, see the *NCO Phase (Preset x) Register* section). The value is left-justified into a 32-bit field and then added to the phase accumulator.

Use Equation 8 to calculate the phase offset in radians.

$$\text{NCO_PHASEn} \times 2^{-16} \times 2 \times \pi \tag{8}$$

**NOTE**

Changing the register setting after the JESD204B interface is running results in non-deterministic NCO phase. If deterministic phase is required, the JESD204B link must be re-initialized after changing the register setting. See *Multiple ADC Synchronization*.

#### 7.3.6.2.6 Programmable DDC Delay

The DDC Filter elements incorporate a programmable sample delay. The delay can be programmed from 0 to (decimation setting – 0.5) ADC sample periods. The delay step-size is 0.5 ADC sample periods. The delay settings are programmed through the DDC_DLYn parameter.

**Table 6. Programmable DDC Delay Range**

| D (Decimation Setting) | Min Delay ($t_{(DEVCLK)}$) | Max Delay ($t_{(DEVCLK)}$) |
|---|---|---|
| 4 | 0 | 3.5 |
| 8 | 0 | 7.5 |
| 10 | 0 | 9.5 |
| 16 | 0 | 15.5 |
| 20 | 0 | 19.5 |
| 32 | 0 | 31.5 |


Copyright © 2014–2017, Texas Instruments Incorporated

#### 7.3.6.3 Decimation Filters

The decimation filters are arranged to provide a programmable overall decimation of 4, 8, 10, 16, 20, or 32. The input and output of each filter is complex. The output data consists of 15-bit complex baseband information. Table 7 lists the effective output sample rates.

**Table 7. Output Sample Rates**

| DECIMATION SETTING | COMPLEX SAMPLE OUTPUT RATE AND RESULTING BANDWIDTH (OUTPUT SAMPLE = 15-BIT I + 15-BIT Q + 2-BIT OR) | | | | | |
|---|---|---|---|---|---|---|
| | $f_{(DEVCLK)}$ | | | $f_{(DEVCLK)}$ = 4000 MHz | | |
| | OUTPUT RATE (MSPS) | RAW OUTPUT BANDWIDTH (MHz) | ALIAS PROTECTED BANDWIDTH (MHz) | OUTPUT RATE (MSPS) | RAW OUTPUT BANDWIDTH (MHz) | ALIAS PROTECTED BANDWIDTH (MHz) |
| 4 | $f_{(DEVCLK)}$ / 4 | $f_{(DEVCLK)}$ / 4 | 0.8 × $f_{(DEVCLK)}$ / 4 | 1000 | 1000 | 800 |
| 8 | $f_{(DEVCLK)}$ / 8 | $f_{(DEVCLK)}$N / 8 | 0.8 × $f_{(DEVCLK)}$ / 8 | 500 | 500 | 400 |
| 10 | $f_{(DEVCLK)}$ / 10 | $f_{(DEVCLK)}$ / 10 | 0.8 × $f_{(DEVCLK)}$ / 10 | 400 | 400 | 320 |
| 16 | $f_{(DEVCLK)}$ / 16 | $f_{(DEVCLK)}$ / 16 | 0.8 × $f_{(DEVCLK)}$ / 16 | 250 | 250 | 200 |
| 20 | $f_{(DEVCLK)}$ / 20 | $f_{(DEVCLK)}$ / 20 | 0.8 × $f_{(DEVCLK)}$ / 20 | 200 | 200 | 160 |
| 32 | $f_{(DEVCLK)}$ / 32 | $f_{(DEVCLK)}$ / 32 | 0.8 × $f_{(DEVCLK)}$ / 32 | 125 | 125 | 100 |

For maximum efficiency a group of high speed filter blocks are implemented with specific blocks used for each decimation setting. The first table below describes the combination of filter blocks used for each decimation setting. The next table lists the coefficient details and decimation factor of each filter block.

**Table 8. Decimation Mode Filter Usage**

| Decimation Setting | Filter Blocks Used |
|---|---|
| 4 | CS19, CS55 |
| 8 | CS11, CS15, CS55 |
| 10 | CS11, CS139 |
| 16 | CS7, CS11, CS15, CS55 |
| 20 | CS7, CS11, CS139 |
| 32 | CS7, CS7, CS11, CS15, CS55 |

Copyright © 2014–2017, Texas Instruments Incorporated

## Table 9. Filter Coefficient Details

| Filter Coefficient Set (Decimation Factor of Filter) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CS7 (2) | | CS11 (2) | | CS15 (2) | | CS19 (2) | | CS55 (2) | | CS139 (5) | |
| –65 | –65 | 109 | 109 | –327 | –327 | 22 | 22 | –37 | –37 | –5 | –5 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | –9 | –9 |
| 577 | 577 | –837 | –837 | 2231 | 2231 | –174 | –174 | 118 | 118 | –9 | –9 |
| **1024** | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | –5 | –5 |
| | | 4824 | 4824 | –8881 | –8881 | 744 | 744 | –291 | –291 | 0 | 0 |
| | | **8192** | | 0 | 0 | 0 | 0 | 0 | 0 | 20 | 20 |
| | | | | 39742 | 39742 | –2429 | –2429 | 612 | 612 | 33 | 33 |
| | | | | **65536** | | 0 | 0 | 0 | 0 | 33 | 33 |
| | | | | | | 10029 | 10029 | –1159 | –1159 | 21 | 21 |
| | | | | | | **16384** | | 0 | 0 | 0 | 0 |
| | | | | | | | | 2031 | 2031 | –54 | –54 |
| | | | | | | | | 0 | 0 | –88 | –88 |
| | | | | | | | | –3356 | –3356 | –89 | –89 |
| | | | | | | | | 0 | 0 | –56 | –56 |
| | | | | | | | | 5308 | 5308 | 0 | 0 |
| | | | | | | | | 0 | 0 | 119 | 119 |
| | | | | | | | | –8140 | –8140 | 196 | 196 |
| | | | | | | | | 0 | 0 | 199 | 199 |
| | | | | | | | | 12284 | 12284 | 125 | 125 |
| | | | | | | | | 0 | 0 | 0 | 0 |
| | | | | | | | | –18628 | –18628 | –234 | –234 |
| | | | | | | | | 0 | 0 | –385 | –385 |
| | | | | | | | | 29455 | 29455 | –393 | –393 |
| | | | | | | | | 0 | 0 | –248 | –248 |
| | | | | | | | | –53191 | –53191 | 0 | 0 |
| | | | | | | | | 0 | 0 | 422 | 422 |
| | | | | | | | | 166059 | 166059 | 696 | 696 |
| | | | | | | | | **262144** | | 711 | 711 |
| | | | | | | | | | | 450 | 450 |
| | | | | | | | | | | 0 | 0 |
| | | | | | | | | | | –711 | –711 |
| | | | | | | | | | | –1176 | –1176 |
| | | | | | | | | | | –1206 | –1206 |
| | | | | | | | | | | –766 | –766 |
| | | | | | | | | | | 0 | 0 |
| | | | | | | | | | | 1139 | 1139 |
| | | | | | | | | | | 1893 | 1893 |
| | | | | | | | | | | 1949 | 1949 |
| | | | | | | | | | | 1244 | 1244 |
| | | | | | | | | | | 0 | 0 |
| | | | | | | | | | | –1760 | –1760 |
| | | | | | | | | | | –2940 | –2940 |
| | | | | | | | | | | –3044 | –3044 |
| | | | | | | | | | | –1955 | –1955 |
| | | | | | | | | | | 0 | 0 |
| | | | | | | | | | | 2656 | 2656 |
| | | | | | | | | | | 4472 | 4472 |
| | | | | | | | | | | 4671 | 4671 |
| | | | | | | | | | | 3026 | 3026 |
| | | | | | | | | | | 0 | 0 |
| | | | | | | | | | | –3993 | –3993 |
| | | | | | | | | | | –6802 | –6802 |
| | | | | | | | | | | –7196 | –7196 |
| | | | | | | | | | | –4730 | –4730 |
| | | | | | | | | | | 0 | 0 |


Copyright © 2014–2017, Texas Instruments Incorporated

**Table 9. Filter Coefficient Details (continued)**

| Filter Coefficient Set (Decimation Factor of Filter) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CS7 (2) | | CS11 (2) | | CS15 (2) | | CS19 (2) | | CS55 (2) | | CS139 (5) | |
| | | | | | | | | | | 6159 | 6159 |
| | | | | | | | | | | 10707 | 10707 |
| | | | | | | | | | | 11593 | 11593 |
| | | | | | | | | | | 7825 | 7825 |
| | | | | | | | | | | 0 | 0 |
| | | | | | | | | | | –10423 | –10423 |
| | | | | | | | | | | –18932 | –18932 |
| | | | | | | | | | | –21629 | –21629 |
| | | | | | | | | | | –15618 | –15618 |
| | | | | | | | | | | 0 | 0 |
| | | | | | | | | | | 24448 | 24448 |
| | | | | | | | | | | 52645 | 52645 |
| | | | | | | | | | | 78958 | 78958 |
| | | | | | | | | | | 97758 | 97758 |
| | | | | | | | | | | **104858** | |

### *7.3.6.4 DDC Output Data*

The DDC output data consist of 15-bit complex data plus the two over-range threshold-detection control bits. The following table lists the data format:

| | 16-BIT OUTPUT WORD | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CHANNEL** | **15** | **14** | **13** | **12** | **11** | **10** | **9** | **8** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| I | DDC Output In-Phase (I) 15 bit | | | | | | | | | | | | | | | OR_T0 |
| Q | DDC Output Quadrature (Q) 15 bit | | | | | | | | | | | | | | | OR_T1 |

### *7.3.6.5 Decimation Settings*

#### 7.3.6.5.1 Decimation Factor

The decimation setting is adjustable over the following settings:

- Decimate-by-4
- Decimate-by-8
- Decimate-by-10
- Decimate-by-16
- Decimate-by-20
- Decimate-by-32

**NOTE**

Because the output format is complex I+Q, the effective output bandwidth is approximately two-times the value for a *real* output with the same decimation factor.

#### 7.3.6.5.2 DDC Gain Boost

The DDC gain boost (register 0x200, bit 4) provides additional gain through the DDC block. With a setting of 1 the final filter has 6.02-dB gain. With a setting of 0, the final filter has a 0-dB gain. This setting is recommended when the NCO is set near DC.

### 7.3.7 Data Outputs

The data outputs (DSx±) are very high-speed differential outputs and conform to the JESD204B JEDEC standard. A CML (current-mode logic)-type output driver is used for each output pair. Output pre-emphasis is adjustable to compensate for longer PCB-trace lengths.

Copyright © 2014–2017, Texas Instruments Incorporated

#### 7.3.7.1 The Digital Outputs

The LM15851 output data is transmitted on up to five high-speed serial-data lanes. The output data from the DDC is formatted to the five lanes, 8b10b encoded, and serialized. Up to four different serial output rates are possible depending on the decimation mode setting: 1x, 1.25x, 2x, and 2.5x. In 1x mode, the output serializers run at the same bit rate as the frequency of the applied DEVCLK. In 1.25x mode, the output serializers run at a bit rate that is 1.25-times that of the applied DEVCLK, and so on. For example, for a 1.6-GHz input DEVCLK, the output rates are 1.6 Gbps in 1x mode, 2 Gbps in 1.25x mode, 3.2 Gbps in 2x mode and 4 Gbps in 2.5x mode.

#### 7.3.7.2 JESD204B Interface Features and Settings

##### 7.3.7.2.1 Scrambler Enable

Scrambling randomizes the 8b10b encoded data, spreading the frequency content of the data interface. This reduces the peak EMI energy at any given frequency reducing the possibility of feedback to the device inputs impacting performance. The scrambler is disabled by default and is enabled via SCR (register 0x201, bit 7).

##### 7.3.7.2.2 Frames Per Multi-Frame (K-1)

The frames per multi-frame (K) setting can be adjusted within constraints that are dependant on the selected decimation (D) and serial rate (DDR) settings. The K-minus-1 (KM1) register setting (register 0x201, bits 6:2) must be one less than the desired K setting.

##### 7.3.7.2.3 DDR

The serial rate can be either $1f_{(CLK)}$ (DDR = 0) or $2f_{(CLK)}$ (DDR = 1).

##### 7.3.7.2.4 JESD Enable

The JESD interface must be disabled (JESD_EN is set to 0) while any of the other JESD parameters are changed. While JESD_EN is set 0 the block is held in reset and the serializers are powered down. The clocks for this section are also gated off to further save power. When the parameters have been set as desired the JESD block can be enabled (JESD_EN is set to 1).

##### 7.3.7.2.5 JESD Test Modes

Several different JESD204B test modes are available to assist in link verification and debugging. The list of modes follows.

**NOTE**

PRBS test signals are output directly, without 8b10b encoding.

- Normal operation
- PRBS7 test mode
- PRBS15 test mode
- PRBS23 test mode
- Ramp test mode
- Short or long transport-layer test mode
- D21.5 test mode
- K28.5 test mode
- Repeated ILA test mode
- Modified RPAT test mode
- Serial-outputs differential 0 test mode
- Serial-outputs differential 1 test mode


Copyright © 2014–2017, Texas Instruments Incorporated

#### 7.3.7.2.6 Configurable Pre-Emphasis

The high-speed serial-output drivers incorporate a configurable pre-emphasis feature. This feature allows the output drive waveform to be optimized for different PCB materials and signal transmission distances. The pre-emphasis setting is adjusted through the serializer pre-emphasis setting in register 0x040, bits 3 to 0. The default setting is 4d. Higher values will increase the pre-emphasis to compensate for more lossy PCB materials. This adjustment is best used in conjunction with an eye-diagram analysis capability in the receiver. The pre-emphasis setting should be adjusted to optimize the eye-opening for the hardware configuration and line rates needed.

#### 7.3.7.2.7 Serial Output-Data Formatting

Output data is generated by the DDC then formatted according to the selected decimation and output rate settings. When less than the maximum of five lanes are active, lanes are disabled beginning with the highest numerical lanes. For example when only two lanes are active, lanes 0 and 1 are active, while all higher lanes are inactive.

**Table 10. Parameter Definitions**

| PARAMETER | DESCRIPTION | USER CONFIGURED OR DERIVED | STANDARD JESD204B LINK PARAMETER |
|---|---|---|---|
| D | Decimation factor, determined by DMODE register | User | No |
| DDR | Serial line rate: 1 = DDR rate (2x), 0 = SDR rate (1x) | User | No |
| P54 | Enable 5/4 PLL to increase line rate by 1.25x. | User | No |
| | 0 = no PLL (1x), 1 = enable PLL (1.25x) | | |
| K | Number of frames per multiframe | User | Yes |
| N | Bits per sample (before adding control bits and tails bits) | Derived | Yes |
| CS | Control bits per sample | Derived | Yes |
| N’ | Bits per sample (after adding control bits and tail bits). Must be a multiple of 4. | Derived | Yes |
| L | Number of serial lanes | Derived | Yes |
| F | Number of octets (bytes) per frame (per lane) | Derived | Yes |
| M | Number of (logical) converters | Derived | Yes |
| S | Number of samples per converter per frame | Derived | Yes |
| CF | Number of control words per frame | Derived | Yes |
| HD | 1=High density mode (samples may be broken across lanes), 0 = normal mode (samples may not be broken across lanes) | Derived | Yes |
| KS | Legal adjustment step for K, to ensure that the multi-frame clock is a sub-harmonic of other internal clocks | Derived | No |

**Table 11. Serial Link Parameters (1)**

| USER SPECIFIED PARAMETERS | | | DERIVED PARAMETERS | | | | | | | | OTHER INFORMATION | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DECIMATION FACTOR (D) | DDR | P54 | N | CS | N’ | L | F | M | S | KS | LEGAL K RANGE | BIT RATE / ADC CLOCK (2) |
| 4 | 1 | 0 | 15 | 1 | 16 | 5 | 4 | 2 | 5 | 4 | 8-32 | 2x |
| 4 | 1 | 1 | 15 | 1 | 16 | 4 | 2 | 2 | 2 | 2 | 10-32 | 2.5x |
| 8 | 0 | 0 | 15 | 1 | 16 | 5 | 4 | 2 | 5 | 2 | 6-32 | 1x |
| 8 | 0 | 1 | 15 | 1 | 16 | 4 | 2 | 2 | 2 | 1 | 9-32 | 1.25x |
| 8 | 1 | 0 | 15 | 1 | 16 | 3 | 8 | 2 | 5 | 2 | 4-32 | 2x |
| 8 | 1 | 1 | 15 | 1 | 16 | 2 | 2 | 2 | 1 | 2 | 10-32 | 2.5x |
| 10 | 0 | 0 | 15 | 1 | 16 | 4 | 2 | 2 | 2 | 4 | 12-32 | 1x |
| 10 | 1 | 0 | 15 | 1 | 16 | 2 | 2 | 2 | 1 | 8 | 16-32 | 2x |
| 16 | 0 | 0 | 15 | 1 | 16 | 3 | 8 | 2 | 5 | 1 | 3-32 | 1x |
| 16 | 0 | 1 | 15 | 1 | 16 | 2 | 2 | 2 | 1 | 1 | 9-32 | 1.25x |
| 16 | 1 | 0 | 15 | 1 | 16 | 2 | 16 | 2 | 5 | 1 | 2-32 | 2x |

(1) In all modes: HD = 0 and CF = 0
(2) x = times (for example, 2x = 2-times)

Copyright © 2014–2017, Texas Instruments Incorporated

### Table 11. Serial Link Parameters(1) (continued)

| USER SPECIFIED PARAMETERS | | | DERIVED PARAMETERS | | | | | | | | OTHER INFORMATION | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DECIMATION FACTOR (D) | DDR | P54 | N | CS | N' | L | F | M | S | KS | LEGAL K RANGE | BIT RATE / ADC CLOCK(2) |
| 16 | 1 | 1 | 15 | 1 | 16 | 1 | 4 | 2 | 1 | 1 | 5-32 | 2.5x |
| 20 | 0 | 0 | 15 | 1 | 16 | 2 | 2 | 2 | 1 | 4 | 12-32 | 1x |
| 20 | 1 | 0 | 15 | 1 | 16 | 1 | 4 | 2 | 1 | 4 | 8-32 | 2x |
| 32 | 0 | 0 | 15 | 1 | 16 | 2 | 16 | 2 | 5 | 1 | 2-32 | 1x |
| 32 | 0 | 1 | 15 | 1 | 16 | 1 | 4 | 2 | 1 | 1 | 5-32 | 1.25x |
| 32 | 1 | 0 | 15 | 1 | 16 | 1 | 32 | 2 | 5 | 1 | 1-32 | 2x |

Output data is formatted in a specific optimized fashion for each decimation and DDR setting combination. The following tables list the specific mapping formats. In all mappings the T or tail bits are 0 (zero).

### Table 12. Decimate-by-4, DDR = 1, P54 = 0, LMF = 5,2,4

| TIME → | | | | |
|---|---|---|---|---|
| CHAR NUMBER | 0 | 1 | 2 | 3 |
| Lane 0 | $I_0$ | | $I_1$ | |
| Lane 1 | $I_2$ | | $I_3$ | |
| Lane 2 | $I_4$ | | $Q_0$ | |
| Lane 3 | $Q_1$ | | $Q_2$ | |
| Lane 4 | $Q_3$ | | $Q_4$ | |
| | Frame n | | | |

### Table 13. Decimate-by-4, DDR = 1, P54 = 1, LMF = 4,2,2

| TIME → | | | | | | |
|---|---|---|---|---|---|---|
| CHAR NUMBER | 0 | 1 | 2 | 3 | 4 | 5 |
| Lane 0 | $I_0$ | | $I_2$ | | $I_4$ | |
| Lane 1 | $I_1$ | | $I_3$ | | $I_5$ | |
| Lane 2 | $Q_0$ | | $Q_2$ | | $Q_4$ | |
| Lane 3 | $Q_1$ | | $Q_3$ | | $Q_5$ | |
| | Frame n | | Frame n + 1 | | Frame n + 2 | |

### Table 14. Decimate-by-8, DDR = 0, P54 = 0, LMF = 5,2,4

| TIME → | | | | |
|---|---|---|---|---|
| CHAR NUMBER | 0 | 1 | 2 | 3 |
| Lane 0 | $I_0$ | | $I_1$ | |
| Lane 1 | $I_2$ | | $I_3$ | |
| Lane 2 | $I_4$ | | $Q_0$ | |
| Lane 3 | $Q_1$ | | $Q_2$ | |
| Lane 4 | $Q_3$ | | $Q_4$ | |
| | Frame n | | | |


Copyright © 2014–2017, Texas Instruments Incorporated

### Table 15. Decimate-by-8, DDR = 0, P54 = 1, LMF = 4,2,2

| TIME → | | | | | | |
|---|---|---|---|---|---|---|
| **CHAR NUMBER** | **0** | **1** | **2** | **3** | **4** | **5** |
| Lane 0 | $I_0$ | | $I_2$ | | $I_4$ | |
| Lane 1 | $I_1$ | | $I_3$ | | $I_5$ | |
| Lane 2 | $Q_0$ | | $Q_2$ | | $Q_4$ | |
| Lane 3 | $Q_1$ | | $Q_3$ | | $Q_5$ | |
| | Frame n | | Frame n + 1 | | Frame n + 2 | |

### Table 16. Decimate-by-8, DDR = 1, P54 = 0, LMF = 3,2,8

| TIME → | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **CHAR NUMBER** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
| Lane 0 | $I_0$ | | $I_1$ | | $I_2$ | | $I_3$ | |
| Lane 1 | $I_4$ | | $Q_0$ | | $Q_1$ | | $Q_2$ | |
| Lane 2 | $Q_3$ | | $Q_4$ | | T | | T | |
| | Frame n | | | | | | | |

### Table 17. Decimate-by-8, DDR = 1, P54=1, LMF = 2,2,2

| TIME → | | | | | | |
|---|---|---|---|---|---|---|
| **CHAR NUMBER** | **0** | **1** | **2** | **3** | **4** | **5** |
| Lane 0 | $I_0$ | | $I_1$ | | $I_2$ | |
| Lane 1 | $Q_0$ | | $Q_1$ | | $Q_2$ | |
| | Frame n | | Frame n + 1 | | Frame n + 2 | |

### Table 18. Decimate-by-10, DDR = 0, P54 = 0, LMF = 4,2,2

| TIME → | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **CHAR NUMBER** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
| Lane 0 | $I_0$ | | $I_2$ | | $I_4$ | | $I_6$ | |
| Lane 1 | $I_1$ | | $I_3$ | | $I_5$ | | $I_7$ | |
| Lane 2 | $Q_0$ | | $Q_2$ | | $Q_4$ | | $Q_6$ | |
| Lane 3 | $Q_1$ | | $Q_3$ | | $Q_5$ | | $Q_7$ | |
| | Frame n | | Frame n + 1 | | Frame n + 2 | | Frame n + 3 | |

### Table 19. Decimate-by-10, DDR = 1, P54 = 0, LMF = 2,2,2

| TIME → | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **CHAR NUMBER** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
| Lane 0 | $I_0$ | | $I_1$ | | $I_2$ | | $I_3$ | |
| Lane 1 | $Q_0$ | | $Q_1$ | | $Q_2$ | | $Q_3$ | |
| | Frame n | | Frame n + 1 | | Frame n + 2 | | Frame n+3 | |

Copyright © 2014–2017, Texas Instruments Incorporated

### Table 20. Decimate-by-16, DDR = 0, P54 = 0, LMF = 3,2,8

| TIME → | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **CHAR NUMBER** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
| Lane 0 | $I_0$ | | $I_1$ | | $I_2$ | | $I_3$ | |
| Lane 1 | $I_4$ | | $Q_0$ | | $Q_1$ | | $Q_2$ | |
| Lane 2 | $Q_3$ | | $Q_4$ | | T | | T | |
| | Frame n | | | | | | | |

### Table 21. Decimate-by-16, DDR = 0, P54 = 1, LMF = 2,2,2

| TIME → | | | | | | |
|---|---|---|---|---|---|---|
| **CHAR NUMBER** | **0** | **1** | **2** | **3** | **4** | **5** |
| Lane 0 | $I_0$ | | $I_1$ | | $I_2$ | |
| Lane 1 | $Q_0$ | | $Q_1$ | | $Q_2$ | |
| | Frame n | | Frame n + 1 | | Frame n + 2 | |

### Table 22. Decimate-by-16, DDR = 1, P54 = 0, LMF = 2,2,16

| TIME → | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CHAR NUMBER** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** | **11** | **12** | **13** | **14** | **15** |
| Lane 0 | $I_0$ | | $I_1$ | | $I_2$ | | $I_3$ | | $I_4$ | | $Q_0$ | | $Q_1$ | | $Q_2$ | |
| Lane 1 | $Q_3$ | | $Q_4$ | | T | | T | | T | | T | | T | | T | |
| | Frame n | | | | | | | | | | | | | | | |

### Table 23. Decimate-by-16, DDR = 1, P54 = 1, LMF = 1,2,4

| TIME → | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CHAR NUMBER** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** | **11** |
| Lane 0 | $I_0$ | | $Q_0$ | | $I_1$ | | $Q_1$ | | $I_2$ | | $Q_2$ | |
| | Frame n | | | | Frame n + 1 | | | | Frame n + 2 | | | |

### Table 24. Decimate-by-20, DDR = 0, P54 = 0, LMF = 2,2,2

| TIME → | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **CHAR NUMBER** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
| Lane 0 | $I_0$ | | $I_1$ | | $I_2$ | | $I_3$ | |
| Lane 1 | $Q_0$ | | $Q_1$ | | $Q_2$ | | $Q_3$ | |
| | Frame n | | Frame n + 1 | | Frame n + 2 | | Frame n + 3 | |

### Table 25. Decimate-by-20, DDR = 1, P54 = 0, LMF = 1,2,2

| TIME → | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **CHAR NUMBER** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
| Lane 0 | $I_0$ | | $Q_0$ | | $I_1$ | | $Q_1$ | |
| | Frame n | | | | Frame n + 1 | | | |


Copyright © 2014–2017, Texas Instruments Incorporated

**Table 26. Decimate-by-32, DDR = 0, P54 = 0, LMF = 2,2,16**

| TIME → | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CHAR NUMBER** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** | **11** | **12** | **13** | **14** | **15** |
| Lane 0 | $I_0$ | | $I_1$ | | $I_2$ | | $I_3$ | | $I_4$ | | $Q_0$ | | $Q_1$ | | $Q_2$ | |
| Lane 1 | $Q_3$ | | $Q_4$ | | T | | T | | T | | T | | T | | T | |
| | Frame n | | | | | | | | | | | | | | | |

**Table 27. Decimate-by-32, DDR = 0, P54 = 1, LMF = 1,2,4**

| TIME → | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CHAR NUMBER** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** | **11** |
| Lane 0 | $I_0$ | | $Q_0$ | | $I_1$ | | $Q_1$ | | $I_2$ | | $Q_2$ | |
| | Frame n | | | | Frame n + 1 | | | | Frame n + 2 | | | |

**Table 28. Decimate-by-32, DDR = 1, P54 = 0, LMF = 1,2,32**

| TIME → | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **CHAR NUMBER** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** | **11** | **12** | **13** | **14** | **15** | **16** | **17** | **18** | **19** | **20** | **21** | **22** | **23** | **24** | **25** | **26** | **27** | **28** | **29** | **30** | **31** |
| Lane 0 | $I_0$ | | $I_1$ | | $I_2$ | | $I_3$ | | $I_4$ | | $Q_0$ | | $Q_1$ | | $Q_2$ | | $Q_3$ | | $Q_4$ | | T | | T | | T | | T | | T | | T | |
| | Frame n | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

The formatted data is 8b10b encoded and output on the serial lanes. The 8b10b encoding provides a number of specific benefits, including:

- Standard encoding format. Therefore the IP is readily available in off-the-shelf FPGAs and ASIC building blocks.
- Inherent DC balance allows AC coupling of lanes with small on-chip capacitors
- Inherent error checking

#### 7.3.7.2.8 JESD204B Synchronization Features

The JESD204B standard defines methods for synchronization and deterministic latency in a multi-converter system. This device is a JESD204B Subclass 1 device and conforms to the various aspects of link operation as described in section 5.3.3 of the JESD204B standard. The specific signals used to achieve link operation are described briefly in the following sections.

#### 7.3.7.2.9 SYSREF

The SYSREF is a periodic signal which is sampled by the device clock, and is used to align the boundary of the local multi-frame clock inside the data converter. SYSREF

is required to be a sub-harmonic of the LMFC internal timing. To meet this requirement, the timing of SYSREF is dependent on the device clock frequency and the LMFC frequency as determined by the selected DDC decimation and frames per multi-frame settings. This clock is typically in the range of 10 MHz to 300 MHz. See the *Multiple ADC Synchronization* section for more details on SYSREF timing requirements.

#### 7.3.7.2.10 SYNC~

SYNC~ is asserted by the receiver to initiate a synchronization event.

Single ended and differential SYNC~ inputs are provided. The SYNC_DIFFSEL bit (register 0x202, bit 6) is used to select which input is used. . To assert SYNC~, a logic low is applied. To deassert SYNC~ a logic high is applied.

#### 7.3.7.2.11 Code-Group Synchronization

Code-group synchronization is achieved using the following process:

- The receiver issues a synchronization request through the SYNC~ input
- The transmitter issues a stream of K28.5 symbols

- The receiver synchronizes and waits for correct reception of at least 4 consecutive K symbols
- The receiver deactivates the synchronization request
- Upon detecting that the receiver has deactivated the SYNC~ pin, the transmitter continues emitting K symbols until the next LMFC boundary (or optionally a later LMFC boundary)
- On the first frame following the selected LMFC boundary the transmitters emit an initial lane-alignment sequence

The initial-lane alignment sequence transmitted by the ADC device is defined in additional detail in JESD204B section 5.3.3.5.

#### 7.3.7.2.12 Multiple ADC Synchronization

The second function for the SYSREF input is to facilitate the precise synchronization of multiple ADCs in a system.

One key challenge is to ensure that this synchronization works is to ensure that the SYSREF inputs are repeatedly captured by the input CLK. Two key elements must occur for the SYSREF inputs to be captured. First, the SYSREF input must be created so that it is synchronous to the input DEVCLK, be an integer sub-harmonic of the multi-frame ($K \times t_{(FRAME)}$) and a repeatable and fixed-phase offset. When this constraint is achieved, repeatedly capturing SYSREF is easier. To further ease this task, the SYSREF signal is routed through a user-adjustable delay which eases the timing requirements with respect to the input DEVCLK signal. The SYSREF delay RDEL is adjusted through bits 3 through 0 in register 0x032.

As long as the SYSREF signal has a fixed timing relationship to DEVCLK, the internal delay can be used to maximize the setup and hold times between the internally delayed SYSREF and the internal DEVCLK signal. These timing relationships are listed in the *Timing Requirements* table. To find the proper delay setting, the RDEL value is adjusted from minimum to maximum while applying SYSREF and monitoring the SysRefDet and Dirty Capture detect bits. The SysRefDet bit is set whenever a rising edge of SYSREF is detected. The Dirty Capture bit is set whenever the setup or hold time between DEVCLK and the delayed SYSREF is insufficient. The SysRefDetClr bit is used to clear the SysRefDet bit. The Clear Dirty Capture bit is used to clear that bit.

This procedure should be followed to determine the range of delay settings where a clean SYSREF capture is achieved. The delay value at the center of the clean capture range must be loaded as the final RDEL setting. Table 29 lists a summary of the control bits that are used and the monitor bits that are read.

**Table 29. SYSREF Capture Control and Status**

| BIT NAME | REGISTER ADDRESS | REGISTER BIT | FUNCTION |
|---|---|---|---|
| RDEL | 0x032 | 3:0 | Adjust relative delay between DEVCLK and SYSREF |
| SysRefDet | 0x031 | 7 | Detect if a SYSREF rising edge has been captured (not self clearing) |
| Dirty Capture | 0x031 | 6 | Detect if SYSREF rising edge capture failed setup/hold (not self clearing) |
| SysRefDetClr | 0x030 | 5 | Clear SYSREF detection bit |
| Clear Dirty Capture | 0x030 | 4 | Clear Dirty Capture detection bit |
| SysRef_Rcvr_En | 0x030 | 7 | Enable SYSREF receiver. See the CLKGEN_0 descriptions in the *Clock Generator Control 0 Register* section for more information. |
| SysRef_Pr_En | 0x030 | 6 | Enable SYSREF processing. See the CLKGEN_0 descriptions in the *Clock Generator Control 0 Register* section for more information. |

One final aspect of multi-device synchronization relates to phase alignment of the NCO phase accumulators when DDC modes are enabled. The NCO phase accumulators are reset during the ILA phase of link startup which means that for multiple ADCs to have NCO phase alignment, all links must be enabled in the same LMFC period. Enabling all links in the same LMFC period requires synchronizing the SYNC~ de-assertion across all data receivers in the system, so that all of the SYNC~ signals are released during the same LMFC period. Using large K values and resulting longer LMFC periods will ease this task, at the expense of potentially higher latency in the receiving device.


Copyright © 2014–2017, Texas Instruments Incorporated

## 7.4 Device Functional Modes

### 7.4.1 DDC Modes

In the DDC modes (decimation > 1) complex (I,Q) data is output at a lower sample rate as determined by the decimation factor (4, 8, 10, 16, 20, and 32).

### 7.4.2 Calibration

Calibration adjusts the ADC core to optimize the following device parameters:

- ADC core linearity
- ADC core-to-core offset matching
- ADC core-to-core full-scale range matching
- ADC core 4-way interleave timing

All calibration processes occur internally. Calibration does not require any external signals to be present and works properly as long as the device is maintained within the values listed in the *Recommended Operating Conditions* table.

#### *7.4.2.1 Foreground Calibration Mode*

In foreground mode the calibration process interrupts normal ADC operation and no output data is available during this time (the output code is forced to a static value). The calibration process should be repeated if the device temperature changes by more than 20ºC to ensure rated performance is maintained. Foreground calibration is initiated by setting the CAL_SFT bit (register 0x050, bit 3) which is self clearing. The foreground calibration process finishes within $t_{(CAL)}$ number of DEVCLK cycles. The process occurs somewhat longer when the timing calibration mode is enabled.

**NOTE**

Initiating a foreground calibration asynchronously resets the calibration control logic and may glitch internal device clocks. Therefore after setting the CAL_SFT bit clearing and then setting JESD_EN is necessary. If resetting the JESD204B link is undesirable for system reasons, background calibration mode may be preferred.

#### *7.4.2.2 Background Calibration Mode*

In background mode an additional ADC core is powered-up for a total of 5 ADC cores. At any given time, one core is off-line and not used for data conversion. This core is calibrated in the background and then placed on-line simultaneous with another core going off-line for calibration. This process operates continuously without interrupting data flow in the application and ensures that all cores are optimized in performance regardless of any changes of temperature. The background calibration cycle rate is fixed and is not adjustable by the user.

Because of the additional circuitry active in background calibration mode, a slight degradation in performance occurs in comparison to foreground calibration mode at a fixed temperature. As a result of this degradation, using foreground calibration mode is recommended if the expected change in operating temperature is <30°C. Using background calibration mode is recommended if the expected change in operating temperature is >30°C. The exact difference in performance is dependent on the DEVCLK (sampling clock) frequency, and the analog input signal frequency and amplitude. For this reason, device and system performance should be evaluated using both calibration modes before finalizing the choice of calibration mode.

To enable the background calibration feature, set the CAL_BCK bit (register 0x057, bit 0) and the CAL_CONT bit (register 0x057, bit 1). The value written to the register 0x057 to enable background calibration is therefore 0x013h. After writing this value to register 0x057, set the CAL_SFT bit in register 0x050 to perform the one-time foreground calibration to begin the process.

**NOTE**

The ADC offset-adjust feature has no effect when background calibration mode is enabled.

Copyright © 2014–2017, Texas Instruments Incorporated

## Device Functional Modes (continued)

### 7.4.3 Timing Calibration Mode

The timing calibration process optimizes the matching of sample timing for the 4 internally interleaved converters. This process minimize the presence of any timing related interleaving spurs in the captured spectrum. The timing calibration feature is disabled by default, but using this feature is highly recommended. To enable timing calibration, set the T_AUTO bit (register 0x066, bit 0). When this bit is set, the timing calibration performs each time the CAL_SFT bit is set.

**Table 30. Calibration Cycle Timing for Different Calibration Modes and Options**

| CAL_CONT, CAL_BCK | T_AUTO | LOW_SIG_EN | INITIAL ONE-TIME CALIBRATION CAL_SFT 0 → 1 ($t_{DEVCLK}$) | BACKGROUND CALIBRATION CYCLE[(1)] (ALL CORES) ($t_{DEVCLK}$) |
|---|---|---|---|---|
| 0 | 0 | 0 | 102 E+6 | N/A |
| 0 | 0 | 1 | 64 E+6 | N/A |
| 0 | 1 | 0 | 227 E+6 | N/A |
| 0 | 1 | 1 | 189 E+6 | N/A |
| 1 | 0 | 0 | 127.5 E+6 | 816 E+6 |
| 1 | 0 | 1 | 80 E+6 | 512 E+6 |
| 1 | 1 | 0 | 283.75 E+6 | 816 E+6 |
| 1 | 1 | 1 | 236.25 E+6 | 512 E+6 |

(1) N/A = not applicable

### 7.4.4 Test-Pattern Modes

A number of device test modes are available. These modes insert known patterns of information into the device data path for assistance with system debug, development, or characterization.

#### *7.4.4.1 Serializer Test-Mode Details*

Test modes are enabled by setting the appropriate configuration of the JESD204B_TEST setting (Register 0x202, Bits 3:0). Each test mode is described in detail in the following sections. Regardless of the test mode, the serializer outputs are powered up based on the configuration decimation and DDR settings. The test modes should only be enabled while the JESD204B link is disabled.

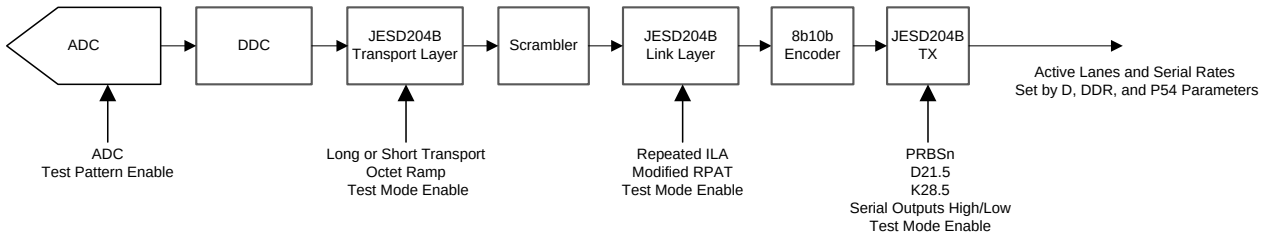



**Figure 34. Test-Mode Insertion Points**

#### *7.4.4.2 PRBS Test Modes*

The PRBS test modes bypass the 8B10B encoder. These test modes produce pseudo-random bit streams that comply with the ITU-T O.150 specification. These bit streams are used with lab test equipment that can self-synchronize to the bit pattern and therefore the initial phase of the pattern is not defined.

The sequences are defined by a recursive equation. For example, the PRBS7 sequence is defined as shown in Equation 9.

$$y[n] = y[n-6]^{y[n-7]} \tag{9}$$

where

- Bit n is the XOR of bit [n – 6] and bit [n – 7] which are previously transmitted bits


Copyright © 2014–2017, Texas Instruments Incorporated

**Table 31. PBRS Mode Equations**

| PRBS TEST MODE | SEQUENCE | SEQUENCE LENGTH (bits) |
|---|---|---|
| PRBS7 | $y[n] = y[n-6]^{y[n-7]}$ | 127 |
| PRBS15 | $y[n] = y[n-14]^{y[n-15]}$ | 32767 |
| PRBS23 | $y[n] = y[n-18]^{y[n-23]}$ | 8388607 |

The initial phase of the pattern is unique for each lane.

#### *7.4.4.3 Ramp Test Mode*

In the ramp test mode, the JESD204B link layer operates normally, but the transport layer is disabled and the input from the formatter is ignored. After the ILA sequence, each lane transmits an identical octet stream that increments from 0x00 to 0xFF and repeats.

#### *7.4.4.4 Short and Long-Transport Test Mode*

The long-transport test mode is available in all DDC modes (decimation > 1). Patterns are generated in accordance with the JESD204B standard and are different for each output format.

Table 32 lists one example of the long transport test pattern:

**Table 32. Long Transport Test Pattern - Decimate-by-4, DDR = 1, P54 = 1, K=10**

| TIME → | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CHAR NO. | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 |
| Lane 0 | 0x0003 | | 0x0002 | | 0x8000 | | 0x8000 | | 0x8000 | | 0x8000 | | 0x8000 | | 0x8000 | | 0x8000 | | 0x8000 | | 0x0003 | |
| Lane 1 | 0x0002 | | 0x0005 | | 0x8000 | | 0x8000 | | 0x8000 | | 0x8000 | | 0x8000 | | 0x8000 | | 0x8000 | | 0x8000 | | 0x0002 | |
| Lane 2 | 0x0004 | | 0x0002 | | 0x8001 | | 0x8000 | | 0x8000 | | 0x8000 | | 0x8000 | | 0x8000 | | 0x8000 | | 0x8000 | | 0x0004 | |
| Lane 3 | 0x0004 | | 0x0004 | | 0x8000 | | 0x8001 | | 0x8000 | | 0x8000 | | 0x8000 | | 0x8000 | | 0x8000 | | 0x8000 | | 0x0004 | |
| | Frame n | | Frame n + 1 | | Frame n + 2 | | Frame n + 3 | | Frame n + 4 | | Frame n + 5 | | Frame n + 6 | | Frame n + 7 | | Frame n + 8 | | Frame n + 9 | | Frame n + 10 | |

If multiple devices are all programmed to the transport layer test mode (while JESD_EN = 0), then JESD_EN is set to 1, and then SYSREF is used to align the LMFC of the devices, the patterns will be aligned to the SYSREF event (within the skew budget of JESD204B). For more details see JESD204B, section 5.1.6.3.

#### *7.4.4.5 D21.5 Test Mode*

In this test mode, the controller transmits a continuous stream of D21.5 characters (alternating 0s and 1s).

#### *7.4.4.6 K28.5 Test Mode*

In this test mode, the controller transmits a continuous stream of K28.5 characters.

#### *7.4.4.7 Repeated ILA Test Mode*

In this test mode, the JESD204B link layer operates normally with one exception: when the ILA sequence completes, the sequence repeats indefinitely. Whenever the receiver issues a synchronization request, the transmitter will initiate code group synchronization. Upon completion of code group synchronization, the transmitter will repeatedly transmit the ILA sequence. If there is no active code group synchronization request at the moment the transmitter enters the test mode, the transmitter will behave as if it received one.

#### *7.4.4.8 Modified RPAT Test Mode*

A 12-octet repeating pattern is defined in INCITS TR-35-2004. The purpose of this pattern is to generate white spectral content for JESD204B compliance and jitter testing. Table 33 lists the pattern before and after 8b10b encoding.

Copyright © 2014–2017, Texas Instruments Incorporated

**Table 33. Modified RPAT Pattern Values**

| OCTET NUMBER | Dx.y NOTATION | 8-BIT INPUT TO 8b10b ENCODER | 20b OUTPUT OF 8b10b ENCODER (2 CHARACTERS) |
|---|---|---|---|
| 0 | D30.5 | 0xBE | 0x86BA6 |
| 1 | D23.6 | 0xD7 | |
| 2 | D3.1 | 0x23 | 0xC6475 |
| 3 | D7.2 | 0x47 | |
| 4 | D11.3 | 0x6B | 0xD0E8D |
| 5 | D15.4 | 0x8F | |
| 6 | D19.5 | 0xB3 | 0xCA8B4 |
| 7 | D20.0 | 0x14 | |
| 8 | D30.2 | 0x5E | 0x7949E |
| 9 | D27.7 | 0xFB | |
| 10 | D21.1 | 0x35 | 0xAA665 |
| 11 | D25.2 | 0x59 | |

## 7.5 Programming

### 7.5.1 Using the Serial Interface

The serial interface is accessed using the following four pins: serial clock (SCLK), serial-data in (SDI), serial-data out (SDO), and serial-interface chip-select ($\overline{SCS}$). Registers access is enabled through the $\overline{SCS}$ pin.

**$\overline{SCS}$** This signal must be asserted low to access a register through the serial interface. Setup and hold times with respect to the SCLK must be observed.

**SCLK** Serial data input is accepted at the rising edge of this signal. SCLK has no minimum frequency requirement.

**SDI** Each register access requires a specific 24-bit pattern at this input. This pattern consists of a read-and-write (R/W) bit, register address, and register value. The data is shifted in MSB first. Setup and hold times with respect to the SCLK must be observed (see Figure 2).

**SDO** The SDO signal provides the output data requested by a read command. This output is high impedance during write bus cycles and during the read bit and register address portion of read bus cycles.

Each register access consists of 24 bits, as shown in Figure 2. The first bit is high for a read and low for a write.

The next 15 bits are the address of the register that is to be written to. During write operations, the last 8 bits are the data written to the addressed register. During read operations, the last 8 bits on SDI are ignored, and, during this time, the SDO outputs the data from the addressed register. The serial protocol details are illustrated in Figure 35.

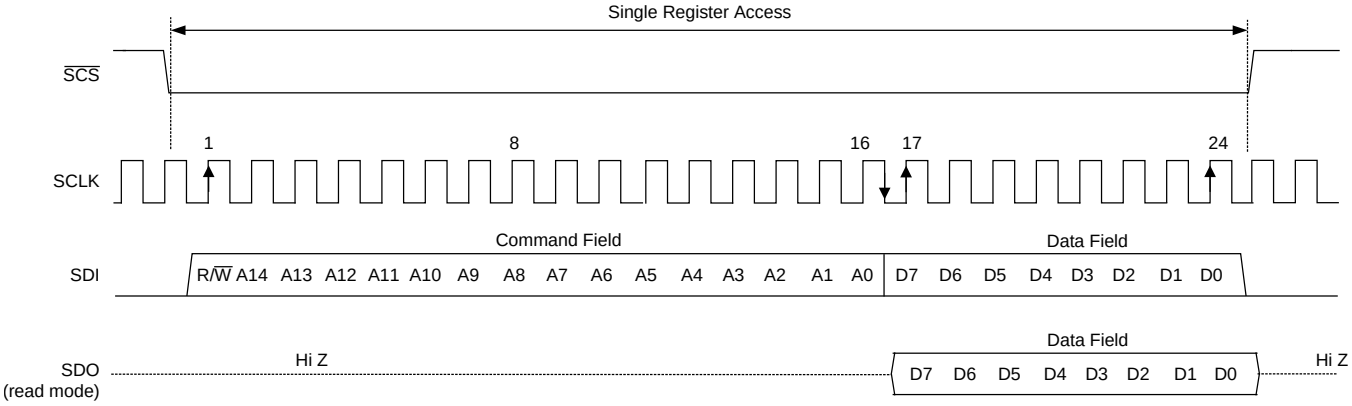



**Figure 35. Serial Interface Protocol - Single Read / Write**


Copyright © 2014–2017, Texas Instruments Incorporated

## Programming (continued)

### *7.5.1.1 Streaming Mode*

The serial interface supports streaming reads and writes. In this mode, the initial 24 bits of the transaction specifics the access type, register address, and data value as normal. Additional clock cycles of write or read data are immediately transferred, as long as the $\overline{SCS}$ input is maintained in the asserted (logic low) state. The register address auto increments (default) or decrements for each subsequent 8 bit transfer of the streaming transaction. The ADDR_ASC bit (register 000h, bits 5 and 2) controls whether the address value ascends (increments) or descends (decrements). Streaming mode can be disabled by setting the ADDR_STATIC bit (register 010h, bit 0). The streaming mode transaction details are shown in Figure 36.

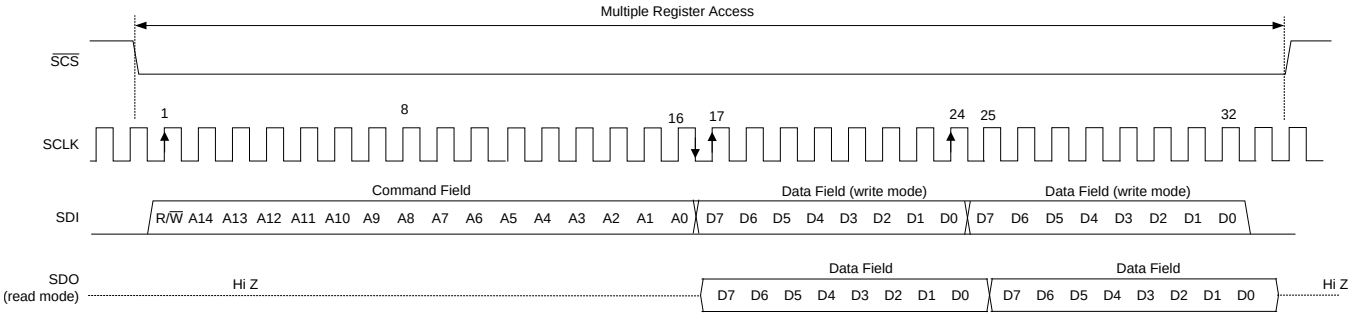



**Figure 36. Serial Interface Protocol - Streaming Read / Write**

See the *Register Map* section for detailed information regarding the registers.

**NOTE**

The serial interface must not be accessed during calibration of the ADC. Accessing the serial interface during this time impairs the performance of the device until the device is calibrated correctly. Writing or reading the serial registers also reduces dynamic performance of the ADC for the duration of the register access time.

## 7.6 Register Map

Several groups of registers provide control and configuration options for this device. Each following register description also shows the power-on reset (POR) state of each control bit.

**NOTE**

All multi-byte registers are arranged in little-endian format (the least-significant byte is stored at the lowest address) unless explicitly stated otherwise.

**Memory Map**

| Address | Reset | Type | Register |
|---|---|---|---|
| **Standard SPI-3.0 (0x000 to 0x00F)** | | | |
| 0x000 | 0x3C | R/W | Configuration A Register |
| 0x001 | 0x00 | R | Configuration B Register |
| 0x002 | 0x00 | R/W | Device Configuration Register |
| 0x003 | 0x03 | R | Chip Type Register |
| 0x004-0x005 | Undefined | R | RESERVED |
| 0x006 | 0x13 | R | Chip Version Register |
| 0x007-0x00B | Undefined | R | RESERVED |
| 0x00C-0x00D | 0x0451 | R | Vendor Identification Register |
| 0x00E-0x00F | Undefined | R | RESERVED |
| **User SPI Configuration (0x010 to 0x01F)** | | | |
| 0x010 | 0x00 | R/W | User SPI Configuration Register |
| 0x011-0x01F | Undefined | R | RESERVED |
| **General Analog, Bias, Band Gap, and Track and Hold (0x020 to 0x02F)** | | | |
| 0x020 | 0x9D | R/W | RESERVED |
| 0x021 | 0x00 | R/W | Power-On Reset Register |
| 0x022 | 0x40 | R/W | I/O Gain 0 Register |
| 0x023 | 0x00 | R/W | I/O Gain 1 Register |
| 0x024 | 0x00 | R/W | RESERVED |
| 0x025 | 0x40 | R/W | I/O Offset 0 Register |
| 0x026 | 0x00 | R/W | I/O Offset 1 Register |
| 0x027 | 0x06 | R/W | RESERVED |
| 0x028 | 0xBA | R/W | RESERVED |
| 0x029 | 0xD4 | R/W | RESERVED |
| 0x02A | 0xEA | R/W | RESERVED |
| 0x02B-0x02F | Undefined | R | RESERVED |
| **Clock (0x030 to 0x03F)** | | | |
| 0x030 | 0xC0 | R/W | Clock Generator Control 0 Register |
| 0x031 | 0x07 | R | Clock Generator Status Register |
| 0x032 | 0x80 | R/W | Clock Generator Control 2 Register |
| 0x033 | 0xC3 | R/W | Analog Miscellaneous Register |
| 0x034 | 0x2F | R/W | Input Clamp Enable Register |
| 0x035 | 0xDF | R/W | RESERVED |
| 0x036 | 0x00 | R/W | RESERVED |
| 0x037 | 0x45 | R/W | RESERVED |
| 0x038-0x03F | Undefined | R/W | RESERVED |
| **Serializer (0x040 to 0x04F)** | | | |
| 0x040 | 0x04 | R/W | Serializer Configuration Register |
| 0x041-0x04F | Undefined | R | RESERVED |


Copyright © 2014–2017, Texas Instruments Incorporated

## Register Map (continued)

### Memory Map (continued)

| Address | Reset | Type | Register |
|---|---|---|---|
| **ADC Calibration (0x050 to 0x1FF)** | | | |
| 0x050 | 0x06 | R/W | Calibration Configuration 0 Register |
| 0x051 | 0xF4 | R/W | Calibration Configuration 1 Register |
| 0x052 | 0x00 | R/W | RESERVED |
| 0x053 | 0x5C | R/W | RESERVED |
| 0x054 | 0x1C | R/W | RESERVED |
| 0x055 | 0x92 | R/W | RESERVED |
| 0x056 | 0x20 | R/W | RESERVED |
| 0x057 | 0x10 | R/W | Calibration Background Control Register |
| 0x058 | 0x00 | R/W | ADC Pattern and Over-Range Enable Register |
| 0x059 | 0x00 | R/W | RESERVED |
| 0x05A | 0x00 | R/W | Calibration Vectors Register |
| 0x05B | Undefined | R | Calibration Status Register |
| 0x05C | 0x00 | R/W | RESERVED |
| 0x05D-0x05E | Undefined | R/W | RESERVED |
| 0x05F | 0x00 | R/W | RESERVED |
| 0x060 | Undefined | R | RESERVED |
| 0x061 | Undefined | R | RESERVED |
| 0x062 | Undefined | R | RESERVED |
| 0x063 | Undefined | R | RESERVED |
| 0x064 | Undefined | R | RESERVED |
| 0x065 | Undefined | R | RESERVED |
| 0x066 | 0x02 | R/W | Timing Calibration Register |
| 0x067 | 0x01 | R/W | RESERVED |
| 0x068 | Undefined | R | RESERVED |
| 0x069 | Undefined | R | RESERVED |
| 0x06A | 0x00 | R/W | RESERVED |
| 0x06B | 0x20 | R/W | RESERVED |
| 0x06C-0x1FF | Undefined | R | RESERVED |
| **Digital Down Converter and JESD204B (0x200-0x27F)** | | | |
| 0x200 | 0x10 | R/W | Digital Down-Converter (DDC) Control |
| 0x201 | 0x0F | R/W | JESD204B Control 1 |
| 0x202 | 0x00 | R/W | JESD204B Control 2 |
| 0x203 | 0x00 | R/W | JESD204B Device ID (DID) |
| 0x204 | 0x00 | R/W | JESD204B Control 3 |
| 0x205 | Undefined | R/W | JESD204B and System Status Register |
| 0x206 | 0xF2 | R/W | Overrange Threshold 0 |
| 0x207 | 0xAB | R/W | Overrange Threshold 1 |
| 0x208 | 0x00 | R/W | Overrange Period |
| 0x209-0x20B | 0x00 | R/W | RESERVED |
| 0x20C | 0x00 | R/W | DDC Configuration Preset Mode |
| 0x20D | 0x00 | R/W | DDC Configuration Preset Select |
| 0x20E-0x20F | 0x0000 | R/W | Rational NCO Reference Divisor |
| **PRESET 0** | | | |
| 0x210-0x213 | 0xC0000000 | R/W | NCO Frequency (Preset 0) |
| 0x214-0x215 | 0x0000 | R/W | NCO Phase (Preset 0) |

Copyright © 2014–2017, Texas Instruments Incorporated

## Register Map (continued)

### Memory Map (continued)

| Address | Reset | Type | Register |
|---|---|---|---|
| 0x216 | 0xFF | R/W | DDC Delay (Preset 0) |
| 0x217 | 0x00 | R/W | RESERVED |
| **PRESET 1** | | | |
| 0x218-0x21B | 0xC0000000 | R/W | NCO Frequency (Preset 1) |
| 0x21C-0x21D | 0x0000 | R/W | NCO Phase (Preset 1) |
| 0x21E | 0xFF | R/W | DDC Delay (Preset 1) |
| 0x21F | 0x00 | R/W | RESERVED |
| **PRESET 2** | | | |
| 0x220-0x223 | 0xC0000000 | R/W | NCO Frequency (Preset 2) |
| 0x224-0x225 | 0x0000 | R/W | NCO Phase (Preset 2) |
| 0x226 | 0xFF | R/W | DDC Delay (Preset 2) |
| 0x227 | 0x00 | R/W | RESERVED |
| **PRESET 3** | | | |
| 0x228-0x22B | 0xC0000000 | R/W | NCO Frequency (Preset 3) |
| 0x22C-0x22D | 0x0000 | R/W | NCO Phase (Preset 3) |
| 0x22E | 0xFF | R/W | DDC Delay (Preset 3) |
| 0x22F | 0x00 | R/W | RESERVED |
| **PRESET 4** | | | |
| 0x230-0x233 | 0xC0000000 | R/W | NCO Frequency (Preset 4) |
| 0x234-0x235 | 0x0000 | R/W | NCO Phase (Preset 4) |
| 0x236 | 0xFF | R/W | DDC Delay (Preset 4) |
| 0x237 | 0x00 | R/W | RESERVED |
| **PRESET 5** | | | |
| 0x238-0x23B | 0xC0000000 | R/W | NCO Frequency (Preset 5) |
| 0x23C-0x23D | 0x0000 | R/W | NCO Phase (Preset 5) |
| 0x23E | 0xFF | R/W | DDC Delay (Preset 5) |
| 0x23F | 0x00 | R/W | RESERVED |
| **PRESET 6** | | | |
| 0x240-0x243 | 0xC0000000 | R/W | NCO Frequency (Preset 6) |
| 0x244-0x245 | 0x0000 | R/W | NCO Phase (Preset 6) |
| 0x246 | 0xFF | R/W | DDC Delay (Preset 6) |
| 0x247 | 0x00 | R/W | RESERVED |
| **PRESET 7** | | | |
| 0x248-0x24B | 0xC0000000 | R/W | NCO Frequency (Preset 7) |
| 0x24C-0x24D | 0x0000 | R/W | NCO Phase (Preset 7) |
| 0x24E | 0xFF | R/W | DDC Delay (Preset 7) |
| 0x24F-0x251 | 0x00 | R/W | RESERVED |
| 0x252-0x27F | Undefined | R | RESERVED |
| **Reserved** | | | |
| 0x0280-0x7FFF | Undefined | R | RESERVED |


Copyright © 2014–2017, Texas Instruments Incorporated

### 7.6.1 Register Descriptions

#### *7.6.1.1 Standard SPI-3.0 (0x000 to 0x00F)*

**Table 34. Standard SPI-3.0 Registers**

| Address | Reset | Acronym | Register Name | Section |
|---|---|---|---|---|
| 0x000 | 0x3C | CFGA | Configuration A Register | Go |
| 0x001 | 0x00 | CFGB | Configuration B Register | Go |
| 0x002 | 0x00 | DEVCFG | Device Configuration Register | Go |
| 0x003 | 0x03 | CHIP_TYPE | Chip Type Register | Go |
| 0x004-0x005 | 0x0000 | RESERVED | RESERVED | Go |
| 0x006 | 0x13 | CHIP_VERSION | Chip Version Register | Go |
| 0x007-0x00B | Undefined | RESERVED | RESERVED | |
| 0x00C-0x00D | 0x0451 | VENDOR_ID | Vendor Identification Register | Go |
| 0x00E-0x00F | Undefined | RESERVED | RESERVED | |

##### 7.6.1.1.1 Configuration A Register (address = 0x000) [reset = 0x3C]

All writes to this register must be a palindrome (for example: bits [3:0] are a mirror image of bits [7:4]). If the data is not a palindrome, the entire write is ignored.

**Figure 37. Configuration A Register (CFGA)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SWRST | RESERVED | ADDR_ASC | RESERVED | RESERVED | ADDR_ASC | RESERVED | SWRST |
| R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-0 |

**Table 35. CFGA Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | SWRST | R/W | 0 | Setting this bit causes all registers to be reset to their default state. This bit is self-clearing. |
| 6 | RESERVED | R/W | 0 | |
| 5 | ADDR_ASC | R/W | 1 | This bit is NOT reset by a soft reset (SWRST)<br>0 : descend – decrement address while streaming (address wraps from 0x0000 to 0x7FFF)<br>1 : ascend – increment address while streaming (address wraps from 0x7FFF to 0x0000) (default) |
| 4 | RESERVED | R/W | 1 | Always returns 1 |
| 3 | RESERVED | R/W | 1100 | Palindrome bits<br>bit 3 = bit 4, bit 2 = bit 5, bit 1 = bit 6, bit 0 = bit 7 |
| 2 | ADDR_ASC | R/W | | |
| 1 | RESERVED | R/W | | |
| 0 | SWRST | R/W | | |

##### 7.6.1.1.2 Configuration B Register (address = 0x001) [reset = 0x00]

**Figure 38. Configuration B Register (CFGB)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | |
| R - 0x00h | | | | | | | |

**Table 36. CFGB Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | RESERVED | R | 0000 0000 | |

#### 7.6.1.1.3 Device Configuration Register (address = 0x002) [reset = 0x00]

**Figure 39. Device Configuration Register (DEVCFG)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | MODE | |
| R/W-000000 | | | | | | R/W-00 | |

**Table 37. DEVCFG Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | RESERVED | R/W | 0000 00 | |
| 1-0 | MODE | R/W | 00 | SPI 3.0 specification has 1 as low power functional mode and 2 as low power fast resume. This chip does not support these modes.<br>0: Normal Operation – full power and full performance (default)<br>1: Normal Operation – full power and full performance (default)<br>2: Power Down – Everything powered down<br>3: Power Down – Everything powered down |

#### 7.6.1.1.4 Chip Type Register (address = 0x003) [reset = 0x03]

**Figure 40. Chip Type Register (CHIP_TYPE)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | CHIP_TYPE | | | |
| R-0000 | | | | R-0011 | | | |

**Table 38. CHIP_TYPE Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | RESERVED | R | 0000 | |
| 3-0 | CHIP_TYPE | R | 0011 | Always returns 0x3, indicating that the part is a high speed ADC. |

#### 7.6.1.1.5 Chip Version Register (address = 0x006) [reset = 0x13]

**Figure 41. Chip Version Register (CHIP_VERSION)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CHIP_VERSION | | | | | | | |
| R-0001 0011 | | | | | | | |

**Table 39. CHIP_VERSION Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | CHIP_VERSION | R | 0001 0011 | Chip version, returns 0x13 |


Copyright © 2014–2017, Texas Instruments Incorporated

#### 7.6.1.1.6 Vendor Identification Register (address = 0x00C to 0x00D) [reset = 0x0451]

**Figure 42. Vendor Identification Register (VENDOR_ID)**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| VENDOR_ID | | | | | | | |
| R-0x04h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VENDOR_ID | | | | | | | |
| R-0x51h | | | | | | | |

**Table 40. VENDOR_ID Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-0 | VENDOR_ID | R | 0x0451h | Always returns 0x0451 (TI Vendor ID) |

### *7.6.1.2 User SPI Configuration (0x010 to 0x01F)*

**Table 41. User SPI Configuration Registers**

| Address | Reset | Acronym | Register Name | Section |
|---|---|---|---|---|
| 0x010 | 0x00 | USR0 | User SPI Configuration Register | Go |
| 0x011-0x01F | Undefined | RESERVED | RESERVED | |

#### 7.6.1.2.1 User SPI Configuration Register (address = 0x010) [reset = 0x00]

**Figure 43. User SPI Configuration Register (USR0)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | ADDR_STATIC |
| R/W-0000 000 | | | | | | | R/W-0 |

**Table 42. USR0 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | RESERVED | R/W | 0000 000 | |
| 0 | ADDR_STATIC | R/W | 0 | 0 : Use ADDR_ASC bit to define what happens to address during streaming (default).<br>1 : Address stays static throughout streaming operation. Useful for reading/writing calibration vector information at CAL_VECTOR register. |

Copyright © 2014–2017, Texas Instruments Incorporated

### 7.6.1.3 General Analog, Bias, Band Gap, and Track and Hold (0x020 to 0x02F)

**Table 43. General Analog, Bias, Band Gap, and Track and Hold Registers**

| Address | Reset | Acronym | Register Name | Section |
|---|---|---|---|---|
| 0x020 | 0x9D | RESERVED | RESERVED | |
| 0x021 | 0x00 | POR | Power-On Reset Register | Go |
| 0x022 | 0x40 | IO_GAIN_0 | I/O Gain 0 Register | Go |
| 0x023 | 0x00 | IO_GAIN_1 | I/O Gain 1 Register | Go |
| 0x024 | 0x00 | RESERVED | RESERVED | |
| 0x025 | 0x40 | IO_OFFSET_0 | I/O Offset 0 Register | Go |
| 0x026 | 0x00 | IO_OFFSET_1 | I/O Offset 1 Register | Go |
| 0x027 | 0x06 | RESERVED | RESERVED | |
| 0x028 | 0xBA | RESERVED | RESERVED | |
| 0x029 | 0xD4 | RESERVED | RESERVED | |
| 0x02A | 0xAA | RESERVED | RESERVED | |
| 0x02B-0x02F | Undefined | RESERVED | RESERVED | |

#### 7.6.1.3.1 Power-On Reset Register (address = 0x021) [reset = 0x00]

**Figure 44. Power-On Reset Register (POR)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | SPI_RES |
| R/W-0000 000 | | | | | | | R/W-0 |

**Table 44. POR Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | RESERVED | R/W | 0000 000 | |
| 0 | SPI_RES | R/W | 0 | Reset all digital. Emulates a power on reset (not self-clearing). Write a *0* and then write a *1* to emulate a reset. Transition from 0—>1 initiates reset.<br>Default: 0 |

#### 7.6.1.3.2 I/O Gain 0 Register (address = 0x022) [reset = 0x40]

**Figure 45. I/O Gain 0 Register (IO_GAIN_0)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | GAIN_FS[14] | GAIN_FS[13] | GAIN_FS[12] | GAIN_FS[11] | GAIN_FS[10] | GAIN_FS[9] | GAIN_FS[8] |
| R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 45. IO_GAIN_0 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R/W | 0 | |
| 6-0 | GAIN_FS[14:8] | R/W | 100 0000 | MSB Bits for GAIN_FS[14:0]. (See the IO_GAIN_1 description in *General Analog, Bias, Band Gap, and Track and Hold (0x020 to 0x02F)*) |


Copyright © 2014–2017, Texas Instruments Incorporated

#### 7.6.1.3.3 IO_GAIN_1 Register (address = 0x023) [reset = 0x00]

**Figure 46. IO_GAIN_1 Register (IO_GAIN_1)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| GAIN_FS[7] | GAIN_FS[6] | GAIN_FS[5] | GAIN_FS[4] | GAIN_FS[3] | GAIN_FS[2] | GAIN_FS[1] | GAIN_FS[0] |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 46. IO_GAIN_1 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | GAIN_FS[7:0] | R/W | 0000 0000 | LSB bits for GAIN_FS[14:0]<br>GAIN_FS[14:0] Value<br>0x0000 500 mVp-p<br>0x4000 725 mVp-p (default)<br>0x7FFF 950 mVp-p |

#### 7.6.1.3.4 I/O Offset 0 Register (address = 0x025) [reset = 0x40]

**Figure 47. I/O Offset 0 Register (IO_OFFSET_0)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | OFFSET_FS[14] | OFFSET_FS[13] | OFFSET_FS[12] | OFFSET_FS[11] | OFFSET_FS[10] | OFFSET_FS[9] | OFFSET_FS[8] |
| R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 47. IO_OFFSET_0 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R/W | 0 | |
| 6-0 | OFFSET_FS[14:8] | R/W | 100 0000 | MSB Bits for OFFSET_FS[14:0].<br>The ADC offset adjust feature has no effect when Background Calibration Mode is enabled. (See IO_OFFSET_1 description in the *General Analog, Bias, Band Gap, and Track and Hold (0x020 to 0x02F) section*). |

#### 7.6.1.3.5 I/O Offset 1 Register (address = 0x026) [reset = 0x00]

**Figure 48. I/O Offset 1 Register (IO_OFFSET_1)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OFFSET_FS[7] | OFFSET_FS[6] | OFFSET_FS[5] | OFFSET_FS[4] | OFFSET_FS[3] | OFFSET_FS[2] | OFFSET_FS[1] | OFFSET_FS[0] |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 48. IO_OFFSET_1 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | OFFSET_FS[7:0] | R/W | 0000 0000 | LSB bits for OFFSET_FS[14:0]. OFFSET_FS[14:0] adjusts the offset of the entire ADC (all banks are impacted).<br>OFFSET_FS[14:0] Value<br>0x0000 –28-mV offset<br>0x4000 no offset (default)<br>0x7FFF 28-mV offset<br>The ADC offset adjust feature has no effect when Background Calibration Mode is enabled. |

### 7.6.1.4 Clock (0x030 to 0x03F)

**Table 49. Clock Registers**

| Address | Reset | Acronym | Register Name | Section |
|---|---|---|---|---|
| 0x030 | 0xC0 | CLKGEN_0 | Clock Generator Control 0 Register | Go |
| 0x031 | 0x07 | CLKGEN_1 | Clock Generator Status Register | Go |
| 0x032 | 0x80 | CLKGEN_2 | Clock Generator Control 2 Register | Go |
| 0x033 | 0xC3 | ANA_MISC | Analog Miscellaneous Register | Go |
| 0x034 | 0x2F | IN_CL_EN | Clamp Enable Register | Go |
| 0x035 | 0xDF | RESERVED | RESERVED | |
| 0x036 | 0x00 | RESERVED | RESERVED | |
| 0x037 | 0x45 | RESERVED | RESERVED | |
| 0x038-0x03F | Undefined | RESERVED | RESERVED | |

#### 7.6.1.4.1 Clock Generator Control 0 Register (address = 0x030) [reset = 0xC0]

**Figure 49. Clock Generator Control 0 Register (CLKGEN_0)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SysRef_Rcvr_En | SysRef_Pr_En | SysRefDetClr | Clear Dirty Capture | RESERVED | DC_LVPECL_CLK_en | DC_LVPECL_SYSREF_en | DC_LVPECL_SYNC_en |
| R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 50. CLKGEN_0 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | SysRef_Rcvr_En | R/W | 1 | Default: 1<br>0 : SYSREF receiver is disabled.<br>1 : SYSREF receiver is enabled (default) |
| 6 | SysRef_Pr_En | R/W | 1 | To power down the SYSREF receiver, clear this bit first, then clear SysRef_Rcvr_En. To power up the SYSREF receiver, set SysRef_Rcvr_En first, then set this bit.<br>Default: 1<br>0 : SYSREF Processor is disabled.<br>1 : SYSREF Processor is enabled (default) |
| 5 | SysRefDetClr | R/W | 0 | Default: 0<br>Write a *1* and then a *0* to clear the SysRefDet status bit. |
| 4 | Clear Dirty Capture | R/W | 0 | Default: 0<br>Write a *1* and then a *0* to clear the DC status bit. |
| 3 | RESERVED | R/W | 0 | Default: 0 |
| 2 | DC_LVPECL_CLK_en | R/W | 0 | Default: 0<br>Set this bit if DEVCLK is a DC-coupled LVPECL signal through a 50-Ω resistor. |
| 1 | DC_LVPECL_SYSREF_en | R/W | 0 | Default: 0<br>Set this bit if SYSREF is a DC-coupled LVPECL signal through a 50-Ω resistor. |
| 0 | DC_LVPECL_SYNC_en | R/W | 0 | Default: 0<br>Set this bit if SYNC~ is a DC-coupled LVPECL signal through a 50-Ω resistor. |


Copyright © 2014–2017, Texas Instruments Incorporated

#### 7.6.1.4.2 Clock Generator Status Register (address = 0x031) [reset = 0x07]

**Figure 50. Clock Generator Status Register (CLKGEN_1)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SysRefDet | Dirty Capture | RESERVED | | | | | |
| R-0 | R-0 | R-00 0111 | | | | | |

**Table 51. CLKGEN_1 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | SysRefDet | R | 0 | When high, indicates that a SYSREF rising edge was detected. To clear this bit, write SysRefDetClr to *1* and then back to *0*. |
| 6 | Dirty Capture | R | 0 | When high, indicates that a SYSREF rising edge occurred very close to the device clock edge, and setup or hold is not ensured (dirty capture). To clear this bit, write CDC to*1* and then back to *0*.<br>**NOTE**: When sweeping the timing on SYSREF, it may jump across the clock edge without triggering this bit. The REALIGNED status bit must be used to detect this (see the JESD_STATUS register description in Digital Down Converter and JESD204B (0x200-0x27F)) |
| 5-0 | RESERVED | R | 00 0111 | Reserved register. Always returns 000111b |

#### 7.6.1.4.3 Clock Generator Control 2 Register (address = 0x032) [reset = 0x80]

**Figure 51. Clock Generator Control 2 Register (CLKGEN_2)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | RDEL | | | |
| R/W-1000 | | | | R/W-0000 | | | |

**Table 52. CLKGEN_2 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | RESERVED | R/W | 1000 | Default: 1000b |
| 3-0 | RDEL | R/W | 0000 | Adjusts the delay of the SYSREF input signal with respect to DEVCLK.<br>Each step delays SYSREF by 20 ps (nominal)<br>Default: 0<br>Range: 0 to 15 decimal |

Copyright © 2014–2017, Texas Instruments Incorporated

#### 7.6.1.4.4 Analog Miscellaneous Register (address = 0x033) [reset = 0xC3]

**Figure 52. Analog Miscellaneous Register (ANA_MISC)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | SYNC_DIFF_PD | RESERVED | |
| R/W-1100 0 | | | | | R/W-0 | R/W-11 | |

**Table 53. ANA_MISC Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-3 | RESERVED | R/W | 1100 0 | |
| 2 | SYNC_DIFF_PD | R/W | 0 | Set this bit to power down the differential SYNC~± inputs for the JESD204B interface.<br>The receiver must be powered up to support the differential SYNC~.<br>Default: 0b |
| 1-0 | RESERVED | R/W | 11 | Default: 11b |

#### 7.6.1.4.5 Input Clamp Enable Register (address = 0x034) [reset = 0x2F]

**Figure 53. Input Clamp Enable Register (IN_CL_EN)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | INPUT_CLAMP_EN | RESERVED | | | | |
| R/W-00 | | R/W-1 | R/W-0 1111 | | | | |

**Table 54. IN_CL_EN Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | RESERVED | R/W | 00 | Default: 00b |
| 5 | INPUT_CLAMP_EN | R/W | 1 | Set this bit to enable the analog input active clamping circuit.<br>Enabled by default.<br>Default: 1b |
| 4-0 | RESERVED | R/W | 0 1111 | Default: 01111b |


Copyright © 2014–2017, Texas Instruments Incorporated

### *7.6.1.5 Serializer (0x040 to 0x04F)*

**Table 55. Serializer Registers**

| Address | Reset | Acronym | Register Name | Section |
|---|---|---|---|---|
| 0x040 | 0x04 | SER_CFG | Serializer Configuration Register | Go |
| 0x041-0x04F | Undefined | RESERVED | RESERVED | |

#### 7.6.1.5.1 Serializer Configuration Register (address = 0x040) [reset = 0x04]

**Figure 54. Serializer configuration Register (SER_CFG)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | SERIALIZER PRE-EMPHASIS | | | |
| R/W-0000 | | | | R/W-0100 | | | |

**Table 56. SER_CFG Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | RESERVED | R/W | 0000 | |
| 3-0 | SERIALIZER PRE-EMPHASIS | R/W | 0100 | Control bits for the pre-emphasis strength of the serializer output driver. Pre-emphasis is required to compensate the low pass behavior of the PCB trace.<br>Default: 4d |

Copyright © 2014–2017, Texas Instruments Incorporated

### 7.6.1.6 ADC Calibration (0x050 to 0x1FF)

**Table 57. ADC Calibration Registers**

| Address | Reset | Acronym | Register Name | Section |
|---|---|---|---|---|
| 0x050 | 0x06 | CAL_CFG0 | Calibration Configuration 0 Register | Go |
| 0x051 | 0xF4 | CAL_CFG1 | Calibration Configuration 1 Register | Go |
| 0x052 | 0x00 | RESERVED | RESERVED | |
| 0x053 | 0x5C | RESERVED | RESERVED | |
| 0x054 | 0x1C | RESERVED | RESERVED | |
| 0x055 | 0x92 | RESERVED | RESERVED | |
| 0x056 | 0x20 | RESERVED | RESERVED | |
| 0x057 | 0x10 | CAL_BACK | Calibration Background Control Register | Go |
| 0x058 | 0x00 | ADC_PAT_OVR_EN | ADC Pattern and Over-Range Enable Register | Go |
| 0x059 | 0x00 | RESERVED | RESERVED | |
| 0x05A | 0x00 | CAL_VECTOR | Calibration Vectors Register | Go |
| 0x05B | Undefined | CAL_STAT | Calibration Status Register | Go |
| 0x05C | 0x00 | RESERVED | RESERVED | |
| 0x05D-0x05E | Undefined | RESERVED | RESERVED | |
| 0x05F | 0x00 | RESERVED | RESERVED | |
| 0x060 | Undefined | RESERVED | RESERVED | |
| 0x061 | Undefined | RESERVED | RESERVED | |
| 0x062 | Undefined | RESERVED | RESERVED | |
| 0x063 | Undefined | RESERVED | RESERVED | |
| 0x064 | Undefined | RESERVED | RESERVED | |
| 0x065 | Undefined | RESERVED | RESERVED | |
| 0x066 | 0x02 | T_CAL | Timing Calibration Register | Go |
| 0x067 | 0x01 | RESERVED | RESERVED | |
| 0x068 | Undefined | RESERVED | RESERVED | |
| 0x069 | Undefined | RESERVED | RESERVED | |
| 0x06A | 0x00 | RESERVED | RESERVED | |
| 0x06B | 0x20 | RESERVED | RESERVED | |
| 0x06C-0x1FF | Undefined | RESERVED | RESERVED | |


Copyright © 2014–2017, Texas Instruments Incorporated

#### 7.6.1.6.1 Calibration Configuration 0 Register (address = 0x050) [reset = 0x06]

**Figure 55. Calibration Configuration 0 Register (CAL_CFG0)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | CALIBRATION_READ_WRITE_EN | CAL_SFT | RESERVED | | |
| R/W-00 | | R/W-0 | R/W-0 | R/W-0 | R/W-110 | | |

**Table 58. CAL_CFG0 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-5 | RESERVED | R/W | 000 | |
| 4 | CALIBRATION_READ_WRITE_EN | R/W | 0 | Enables the scan register to read or write calibration vectors at register 0x05A.<br>Default: 0 |
| 3 | CAL_SFT(1) | R/W | 0 | Software calibration bit. Set bit to initiate foreground calibration. This bit is self-clearing.<br>This bit resets the calibration state machine. Most calibration SPI registers are not synchronized to the calibration clock. Changing them may corrupt the calibration state machine. Always set CAL_SFT AFTER making any changes to the calibration registers. |
| 2-0 | RESERVED | R/W | 110 | Default: 110 |

(1) IMPORTANT NOTE: Setting CAL_SFT can glitch internal state machines. The JESD_EN bit must be cleared and then set after setting CAL_SFT.

#### 7.6.1.6.2 Calibration Configuration 1 Register (address = 0x051) [reset = 0xF4]

**Figure 56. Calibration Configuration 1 Register (CAL_CFG1)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | LOW_SIG_EN | | | RESERVED | | | |
| R/W-1 | R/W-111 | | | R/W-0100 | | | |

**Table 59. CAL_CFG1 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R/W | 1 | |
| 6-4 | LOW_SIG_EN | R/W | 111 | Controls signal range optimization for calibration processes.<br>111: Calibration is optimized for lower amplitude input signals (< –10dBFS).<br>**000: Calibration is optimized for large (-1dBFS) input signals.**<br>Default: 111 but recommend 000 for large input signals. |
| 3-0 | RESERVED | R/W | 0100 | |

#### 7.6.1.6.3 Calibration Background Control Register (address = 0x057) [reset = 0x10]

**Figure 57. Calibration Background Control Register (CAL_BACK)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | CAL_CONT | CAL_BCK |
| R/W-0001 00 | | | | | | R/W-0 | R/W-0 |

**Table 60. CAL_BACK Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | RESERVED | R/W | 0001 00 | Set to 0001 00b |
| 1 | CAL_CONT | R/W | 0 | CAL_CONT is the only calibration register bit that can be modified while background calibration is ongoing. This bit must be set to 0 before modifying any of the other bits.<br>0 : Pause or stop background calibration sequence.<br>1 : Start background calibration sequence. |
| 0 | CAL_BCK | R/W | 0 | Background calibration mode enabled. When pausing background calibration leave this bit set, only change CAL_CONT to 0.<br>If CAL_BCK is set to 0 after background calibration has been operation the calibration processes may stop in an incomplete condition. Set CAL_SFT to perform a foreground calibration |

#### 7.6.1.6.4 ADC Pattern and Over-Range Enable Register (address = 0x058) [reset = 0x00]

**Figure 58. ADC Pattern and Over-Range Enable Register (ADC_PAT_OVR_EN)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | ADC_PAT_EN | OR_EN | RESERVED |
| R/W-0000 0 | | | | | R/W-0 | R/W-0 | R/W-0 |

**Table 61. ADC_PAT_OVR_EN Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-3 | RESERVED | R/W | 0000 0 | Set to 00000b |
| 2 | ADC_PAT_EN | R/W | 0 | Enable ADC test pattern |
| 1 | OR_EN | R/W | 0 | Enable over-range output |
| 0 | RESERVED | R/W | 0 | Set to 0 |

#### 7.6.1.6.5 Calibration Vectors Register (address = 0x05A) [reset = 0x00]

**Figure 59. Calibration Vectors Register (CAL_VECTOR)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CAL_DATA | | | | | | | |
| R/W-0000 0000 | | | | | | | |

**Table 62. CAL_VECTOR Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | CAL_DATA | R/W | 0000 0000 | Repeated reads of this register outputs all the calibration register values for analysis if the CALIBRATION_READ_WRITE_EN bit is set.<br>Repeated writes of this register inputs all the calibration register values for configuration if the CAL_RD_EN bit is set. |


Copyright © 2014–2017, Texas Instruments Incorporated

#### 7.6.1.6.6 Calibration Status Register (address = 0x05B) [reset = undefined]

**Figure 60. Calibration Status Register (CAL_STAT)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | CAL_CONT_OFF | FIRST_CAL_DONE |
| R-0000 10 | | | | | | R-X | R-X |

**Table 63. CAL_STAT Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | RESERVED | R | 0000 10XX | |
| 1 | CAL_CONT_OFF | R | X | After clearing CAL_CONT, calibration does not stop immediately. Use this register to confirm it has stopped before changing calibration settings.<br>0: Indicates calibration is running (foreground or background)<br>1: Indicates that calibration is finished or stopped because CAL_CONT = 0 |
| 0 | FIRST_CAL_DONE | R | X | Indicates first calibration sequence has been done and ADC is operational. |

#### 7.6.1.6.7 Timing Calibration Register (address = 0x066) [reset = 0x02]

**Figure 61. Timing Calibration Register (T_CAL)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | T_AUTO |
| R/W-0000 001 | | | | | | | R/W-0 |

**Table 64. CAL_STAT Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | RESERVED | R/W | 0000 001 | Set to 0000001b |
| 0 | T_AUTO | R/W | 0 | Set to enable automatic timing optimization. Timing calibration will occur once CAL_SFT is set. |

Copyright © 2014–2017, Texas Instruments Incorporated

### 7.6.1.7 Digital Down Converter and JESD204B (0x200-0x27F)

**Table 65. Digital Down Converter and JESD204B Registers**

| Address | Reset | Acronym | Register Name | Section |
|---|---|---|---|---|
| 0x200 | 0x10 | DDC_CTRL1 | Digital Down-Converter (DDC) Control | Go |
| 0x201 | 0x0F | JESD_CTRL1 | JESD204B Control 1 | Go |
| 0x202 | 0x00 | JESD_CTRL2 | JESD204B Control 2 | Go |
| 0x203 | 0x00 | JESD_DID | JESD204B Device ID (DID) | Go |
| 0x204 | 0x00 | JESD_CTRL3 | JESD204B Control 3 | Go |
| 0x205 | Undefined | JESD_STATUS | JESD204B and System Status Register | Go |
| 0x206 | 0xF2 | OVR_T0 | Overrange Threshold 0 | Go |
| 0x207 | 0xAB | OVR_T1 | Overrange Threshold 1 | Go |
| 0x208 | 0x00 | OVR_N | Overrange Period | Go |
| 0x209-0x20B | 0x00 | RESERVED | RESERVED | |
| 0x20C | 0x00 | NCO_MODE | DDC Configuration Preset Mode | Go |
| 0x20D | 0x00 | NCO_SEL | DDC Configuration Preset Select | Go |
| 0x20E-0x20F | 0x0000 | NCO_RDIV | Rational NCO Reference Divisor | Go |
| 0x210-0x213 | 0xC0000000 | NCO_FREQ0 | NCO Frequency (Preset 0) | Go |
| 0x214-0x215 | 0x0000 | NCO_PHASE0 | NCO Phase (Preset 0) | Go |
| 0x216 | 0xFF | DDC_DLY0 | DDC Delay (Preset 0) | Go |
| 0x217 | 0x00 | RESERVED | RESERVED | |
| 0x218-0x21B | 0xC0000000 | NCO_FREQ1 | NCO Frequency (Preset 1) | Go |
| 0x21C-0x21D | 0x0000 | NCO_PHASE1 | NCO Phase (Preset 1) | Go |
| 0x21E | 0xFF | DDC_DLY1 | DDC Delay (Preset 1) | Go |
| 0x21F | 0x00 | RESERVED | RESERVED | |
| 0x220-0x223 | 0xC0000000 | NCO_FREQ2 | NCO Frequency (Preset 2) | Go |
| 0x224-0x225 | 0x0000 | NCO_PHASE2 | NCO Phase (Preset 2) | Go |
| 0x226 | 0xFF | DDC_DLY2 | DDC Delay (Preset 2) | Go |
| 0x227 | 0x00 | RESERVED | RESERVED | |
| 0x228-0x22B | 0xC0000000 | NCO_FREQ3 | NCO Frequency (Preset 3) | Go |
| 0x22C-0x22D | 0x0000 | NCO_PHASE3 | NCO Phase (Preset 3) | Go |
| 0x22E | 0xFF | DDC_DLY3 | DDC Delay (Preset 3) | Go |
| 0x22F | 0x00 | RESERVED | RESERVED | |
| 0x230-0x233 | 0xC0000000 | NCO_FREQ4 | NCO Frequency (Preset 4) | Go |
| 0x234-0x235 | 0x0000 | NCO_PHASE4 | NCO Phase (Preset 4) | Go |
| 0x236 | 0xFF | DDC_DLY4 | DDC Delay (Preset 4) | Go |
| 0x237 | 0x00 | RESERVED | RESERVED | |
| 0x238-0x23B | 0xC0000000 | NCO_FREQ5 | NCO Frequency (Preset 5) | Go |
| 0x23C-0x23D | 0x0000 | NCO_PHASE5 | NCO Phase (Preset 5) | Go |
| 0x23E | 0xFF | DDC_DLY5 | DDC Delay (Preset 5) | Go |
| 0x23F | 0x00 | RESERVED | RESERVED | |
| 0x240-0x243 | 0xC0000000 | NCO_FREQ6 | NCO Frequency (Preset 6) | Go |
| 0x244-0x245 | 0x0000 | NCO_PHASE6 | NCO Phase (Preset 6) | Go |
| 0x246 | 0xFF | DDC_DLY6 | DDC Delay (Preset 6) | Go |
| 0x247 | 0x00 | RESERVED | RESERVED | |
| 0x248-0x24B | 0xC0000000 | NCO_FREQ7 | NCO Frequency (Preset 7) | Go |
| 0x24C-0x24D | 0x0000 | NCO_PHASE7 | NCO Phase (Preset 7) | Go |
| 0x24E | 0xFF | DDC_DLY7 | DDC Delay (Preset 7) | Go |
| 0x24F-0x251 | 0x00 | RESERVED | RESERVED | |
| 0x252-0x27F | Undefined | RESERVED | RESERVED | |


Copyright © 2014–2017, Texas Instruments Incorporated

#### 7.6.1.7.1 Digital Down-Converter (DDC) Control Register (address = 0x200) [reset = 0x10]

**Figure 62. Digital Down-Converter (DDC) Control Register (DDC_CTRL1)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | DDC GAIN BOOST | DMODE | | | |
| R/W-000 | | | R/W-1 | R/W-0000 | | | |

**Table 66. DDC_CTRL1 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-5 | RESERVED | R/W | 000 | |
| 4 | DDC GAIN BOOST | R/W | 1 | 0 : Final filter has 0-dB gain (recommended when NCO is set near DC).<br>1 : Final filter has 6.02-dB gain (default) |
| 3-0 | DMODE (1) | R/W | 0000 | 0 : decimate-by-4 (default)<br>1 : Reserved<br>2 : decimate-by-4<br>3 : decimate-by-8<br>4 : decimate-by-10<br>5 : decimate-by-16<br>6 : decimate-by-20<br>7 : decimate-by-32<br>8..15 : RESERVED |

(1) The DMODE setting must only be changed when JESD_EN is 0.

#### 7.6.1.7.2 JESD204B Control 1 Register (address = 0x201) [reset = 0x0F]

**Figure 63. JESD204B Control 1 Register (JESD_CTRL1)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SCR | K_Minus_1 | | | | | DDR | JESD_EN |
| R/W-0 | R/W-000 11 | | | | | R/W-1 | R/W-1 |

**Table 67. JESD_CTRL1 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | SCR | R/W | 0 | 0 : Scrambler disabled (default)<br>1 : Scrambler enabled |
| 6-2 | K_Minus_1 | R/W | 000 11 | K is the number of frames per multiframe, and K – 1 is programmed here.<br>Default: K = 4, K_Minus_1 = 3.<br>Depending on the decimation (D) and serial rate (DDR), there are constraints on the legal values of K. |
| 1 | DDR | R/W | 1 | 0 : SDR serial rate ($f_{(BIT)} = f_S$)<br>1 : DDR serial rate ($f_{(BIT)} = 2f_S$) (default) |
| 0 | JESD_EN (1) | R/W | 1 | 0 : Block disabled<br>1 : Normal operation (default) |

(1) Before altering any parameters in the JESD_CTRL1 register, you must set JESD_EN to 0. When JESD_EN is 0, the block is held in reset and the serializers are powered down. The clocks are gated off to save power.

Copyright © 2014–2017, Texas Instruments Incorporated

#### 7.6.1.7.3 JESD204B Control 2 Register (address = 0x202) [reset = 0x00]

**Figure 64. JESD204B Control 2 Register (JESD_CTRL2)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| P54 | SYNC_DIFFSEL | RESERVED | | JESD204B_TEST | | | |
| R/W-0 | R/W-0 | R/W-00 | | R/W-0000 | | | |

**Table 68. JESD_CTRL2 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | P54 | R/W | 0 | 0 : Disable 5/4 PLL. Serial bit rate is 1x or 2x based on DDR parameter.<br>1 : Enable 5/4 PLL. Serial bit rate is 1.25x or 2.5x based on DDR parameter. |
| 6 | SYNC_DIFFSEL | R/W | 0 | 0 : Use SYNC_SE_N input for SYNC_N function<br>1 : Use SYNC_DIFF_N input for SYNC_N function |
| 5-4 | RESERVED | R/W | 00 | Set to 00b |
| 3-0 | JESD204B_TEST(1) | R/W | 0000 | See<br>0 : Test mode disabled. Normal operation (default)<br>1 : PRBS7 test mode<br>2 : PRBS15 test mode<br>3 : PRBS23 test mode<br>4 : Ramp test mode<br>5 : Short and long transport layer test mode<br>6 : D21.5 test mode<br>7 : K28.5 test mode<br>8 : Repeated ILA test mode<br>9 : Modified RPAT test mode<br>10: Serial outputs held low<br>11: Serial outputs held high<br>12 through 15 : RESERVED |

(1) The JESD_CTRL2 register must only be changed when JESD_EN is 0.

#### 7.6.1.7.4 JESD204B Device ID (DID) Register (address = 0x203) [reset = 0x00]

**Figure 65. JESD204B Device ID (DID) Register (JESD_DID)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| JESD_DID | | | | | | | |
| R/W-0000 0000 | | | | | | | |

**Table 69. JESD_DID Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | JESD_DID(1) | R/W | 0000 0000 | Specifies the DID value that is transmitted during the second multiframe of the JESD204B ILA. |

(1) The DID setting must only be changed when JESD_EN is 0.


Copyright © 2014–2017, Texas Instruments Incorporated

#### 7.6.1.7.5 JESD204B Control 3 Register (address = 0x204) [reset = 0x00]

**Figure 66. JESD204B Control 3 Register (JESD_CTRL3)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | FCHAR | |
| R/W-0000 00 | | | | | | R/W-00 | |

**Table 70. JESD_CTRL3 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | RESERVED | R/W | 0000 00 | |
| 1-0 | FCHAR (1) | R/W | 00 | Specify which comma character is used to denote end-of-frame. This character is transmitted opportunistically according to JESD204B Section 5.3.3.4.<br>When using a JESD204B receiver, always use FCHAR=0.<br>When using a general purpose 8-b or 10-b receiver, the K28.7 character can cause issues. When K28.7 is combined with certain data characters, a false, misaligned comma character can result, and some receivers realign to the false comma. To avoid this, program FCHAR to 1 or 2.<br>0 : Use K28.7 (default) (JESD204B compliant)<br>1 : Use K28.1 (not JESD204B compliant)<br>2 : Use K28.5 (not JESD204B compliant)<br>3 : Reserved |

(1) The JESD_CTRL3 register must only be changed when JESD_EN is 0.

#### 7.6.1.7.6 JESD204B and System Status Register (address = 0x205) [reset = Undefined]

See the *JESD204B Synchronization Features* section for more details.

**Figure 67. JESD204B and System Status Register (JESD_STATUS)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | LINK_UP | SYNC_STATUS | REALIGNED | ALIGNED | PLL_LOCKED | RESERVED | |
| R/W-0 | R/W-0 | R/W-X | R/W-X | R/W-0 | R/W-0 | R/W-00 | |

**Table 71. JESD_STATUS Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R/W | 0 | Always returns 0 |
| 6 | LINK_UP | R/W | 0 | When set, indicates that the JESD204B link is in the DATA_ENC state. |
| 5 | SYNC_STATUS | R/W | X | Returns the state of the JESD204B SYNC~ signal (SYNC_SE_N or SYNC_DIFF_N).<br>0 : SYNC~ asserted<br>1 : SYNC~ deasserted |
| 4 | REALIGNED | R/W | X | When high, indicates that the div8 clock, frame clock, or multiframe clock phase was realigned by SYSREF.<br>Writing a *1* to this bit clears it. |
| 3 | ALIGNED | R/W | 0 | When high, indicates that the multiframe clock phase has been established by SYSREF. The first SYSREF event after enabling the JESD204B encoder will set this bit.<br>Writing a *1* to this bit clears it. |
| 2 | PLL_LOCKED | R/W | 0 | When high, indicates that the PLL is locked. |
| 1-0 | RESERVED | R/W | 0 | Always returns 0 |

Copyright © 2014–2017, Texas Instruments Incorporated

#### 7.6.1.7.7 Overrange Threshold 0 Register (address = 0x206) [reset = 0xF2]

**Figure 68. Overrange Threshold 0 Register (OVR_T0)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OVR_T0 | | | | | | | |
| R/W-1111 0010 | | | | | | | |

**Table 72. OVR_T0 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | OVR_T0 | R/W | 1111 0010 | Over-range threshold 0. This parameter defines the absolute sample level that causes control bit 0 to be set. Control bit 0 is attached to the DDC I output samples. The detection level in dBFS (peak) is<br>$20_{log10}$(OVR_T0 / 256)<br>Default: 0xF2 = 242 → –0.5 dBFS |

#### 7.6.1.7.8 Overrange Threshold 1 Register (address = 0x207) [reset = 0xAB]

**Figure 69. Overrange Threshold 1 Register (OVR_T1)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OVR_T1 | | | | | | | |
| R/W-1010 1011 | | | | | | | |

**Table 73. OVR_T1 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | OVR_T1 | R/W | 1010 1011 | Overrange threshold 1. This parameter defines the absolute sample level that causes control bit 1 to be set. Control bit 1 is attached to the DDC Q output samples. The detection level in dBFS (peak) is<br>$20_{log10}$(OVR_T1 / 256)<br>Default: 0xAB = 171 → –3.5 dBFS |

#### 7.6.1.7.9 Overrange Period Register (address = 0x208) [reset = 0x00]

**Figure 70. Overrange Period Register (OVR_N)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | OVR_N | | |
| R/W-0000 0 | | | | | R/W-000 | | |

**Table 74. OVR_N Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-3 | RESERVED | R/W | 0000 0 | |
| 2-0 | OVR_N (1) | R/W | 000 | This bit adjusts the monitoring period for the OVR[1:0] output bits. The period is scaled by $2^{OVR_N}$. Incrementing this field doubles the monitoring period. |

(1) Changing the OVR_N setting while JESD_EN=1 may cause the phase of the monitoring period to change.


Copyright © 2014–2017, Texas Instruments Incorporated

#### 7.6.1.7.10 DDC Configuration Preset Mode Register (address = 0x20C) [reset = 0x00]

**Figure 71. DDC Configuration Preset Mode Register (NCO_MODE)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | CFG_MODE |
| R/W-0000 000 | | | | | | | R/W-0 |

**Table 75. NCO_MODE Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | RESERVED | R/W | 0000 000 | |
| 0 | CFG_MODE | R/W | 0 | The NCO frequency and phase are set by the NCO_FREQx and NCO_PHASEx registers, where *x* is the configuration preset (0 through 7). The DDC delay setting is defined by the DDC_DLYx register.<br>0 : Use NCO_[2:0] input pins to select the active DDC and NCO configuration preset.<br>1 : Use the NCO_SEL register to select the active DDC and NCO configuration preset. |

#### 7.6.1.7.11 DDC Configuration Preset Select Register (address = 0x20D) [reset = 0x00]

**Figure 72. DDC Configuration Preset Select Register (NCO_SEL)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | NCO_SEL | | |
| R/W-0000 0 | | | | | R/W-000 | | |

**Table 76. NCO_SEL Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-3 | RESERVED | R/W | 0000 0 | |
| 2-0 | NCO_SEL | R/W | 000 | When NCO_MODE = 1, this register is used to select the active configuration preset. |

Copyright © 2014–2017, Texas Instruments Incorporated

#### 7.6.1.7.12 Rational NCO Reference Divisor Register (address = 0x20E to 0x20F) [reset = 0x0000]

**Figure 73. Rational NCO Reference Divisor Register (NCO_RDIV)**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| NCO_RDIV | | | | | | | |
| R/W-0x00h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NCO_RDIV | | | | | | | |
| R/W-0x00h | | | | | | | |

**Table 77. NCO_RDIV Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-0 | NCO_RDIV | R/W | 0x0000h | Sometimes the 32-bit NCO frequency word does not provide the desired frequency step size and can only approximate the desired frequency. This results in a frequency error. Use this register to eliminate the frequency error. Use this equation to compute the proper value to program:<br>NCO_RDIV = $f_S$ / $f_{(STEP)}$ / 128<br>where<br>• $f_S$ is the ADC sample rate<br>• $f_{(STEP)}$ is the desired NCO frequency step size (10)<br>For example, if $f_S$= 3072 MHz, and $f_{(STEP)}$ = 10 KHz then:<br>NCO_RDIV = 3072 MHz / 10 KHz / 128 = 2400 (11)<br>Any combination of $f_S$ and $f_{(STEP)}$ that results in a fractional value for NCO_RDIV is not supported. Values of NCO_RDIV larger than 8192 can degrade the NCO's SFDR performance and are not recommended. This register is used for all configuration presets. |


Copyright © 2014–2017, Texas Instruments Incorporated

#### 7.6.1.7.13 NCO Frequency (Preset x) Register (address = see Table 65) [reset = see Table 65]

**Figure 74. NCO Frequency (Preset x) Register (NCO_FREQ_x)**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| NCO_FREQ_x | | | | | | | |
| R/W-0xC0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| NCO_FREQ_x | | | | | | | |
| R/W-0x00h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| NCO_FREQ_x | | | | | | | |
| R/W-0x00h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NCO_FREQ_x | | | | | | | |
| R/W-0x00h | | | | | | | |

**Table 78. NCO_FREQ_x Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 31-0 | NCO_FREQ_x | R/W | 0xC0000000h | Changing this register after the JESD204B interface is running results in non-deterministic NCO phase. If deterministic phase is required, the JESD204B interface must be re-initialized after changing this register.<br>The NCO frequency ($f_{(NCO)}$) is:<br>$f_{(NCO)} = NCO_FREQ_x \times 2^{-32} \times f_S$<br>where<br>• $f_S$ is the sampling frequency of the ADC<br>• NCO_FREQ_x is the integer value of this register (12)<br>This register can be interpreted as signed or unsigned.<br>Use this equation to determine the value to program:<br>$NCO_FREQ_x = 2^{32} \times f_{(NCO)} / f_S$ (13)<br>If the equation does not result in an integer value, you must choose an alternate frequency step ($f_{(STEP)}$) and program the NCO_RDIV register. Then use one of the following equations to compute NCO_FREQ_x:<br>$NCO_FREQ_x = round(2^{32} \times f_{(NCO)} / f_S)$ (14)<br>$NCO_FREQ_x = round(2^{25} \times f_{(NCO)} / f_{(STEP)} / NCO_RDIV)$ (15) |

#### 7.6.1.7.14 NCO Phase (Preset x) Register (address = see Table 65) [reset = see Table 65]

**Figure 75. NCO Phase (Preset) Register (NCO_PHASE_x)**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| NCO_PHASE_x | | | | | | | |
| R/W-0x00h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NCO_PHASE_x | | | | | | | |
| R/W-0x00h | | | | | | | |

**Table 79. NCO_PHASE_x Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-0 | NCO_PHASE_x | R/W | 0x0000h | This value is MSB-justified into a 32−bit field and then added to the phase accumulator. The phase (in radians) is<br>$NCO_PHASE_x \times 2^{-16} \times 2\pi$ (16)<br>This register can be interpreted as signed or unsigned. |

#### 7.6.1.7.15 DDC Delay (Preset x) Register (address = see Table 65) [reset = see Table 65]

**Figure 76. DDC Delay (Preset) Register (DDC_DLY_x)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DDC_DLY_x | | | | | | | |
| R/W-0xFFh | | | | | | | |

**Table 80. DDC_DLY_x Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | DDC_DLY_x | R/W | 0xFFh | DDC delay for configuration preset 0<br>This register provides fine adjustments to the DDC group delay. The step size is one half of an ADC sample period ($t_{(DEVCLK)}$ / 2). This is equivalent to Equation 17.<br>$t_O / (2 \times D)$<br>where<br>• $t_O$ is the DDC output sample period<br>• D is the decimation factor (17)<br>The legal range for this register is 0 to 2D-1. Illegal values result in undefined behavior.<br>Example: When D = 8, the legal register range is 0 to 15. The step size is $t_O$ / 16 and the maximum delay is 15 × $t_O$ / 16. Programming this register to 0xFF (the default value) powers down and bypasses the fractional delay filter which reduces the DDC latency by 34 ADC sample periods (as compared to the 0 setting). |


版权 © 2014–2017, Texas Instruments Incorporated

# 8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The LM15851 device is a wideband sampling and digital tuning device. The ADC input captures input signals from DC to greater than 3 GHz. The DDC performs digital-down conversion and programmable decimation filtering, and outputs complex (15 bit I and 15 bit Q) data. The resulting output data is output on the JESD204B data interface for capture by the downstream capture or processing device. Most frequency-domain applications benefit from DDC capability to select the desired frequency band and provide only the necessary bandwidth of output data, minimizing the required number of data signals.

## 8.2 Typical Application

### 8.2.1 RF Sampling Receiver

An RF Sampling Receiver is used to directly sample a signal in the RF frequency range and provide the data for the captured signal to downstream processing. The wide input bandwidth, high sampling rate, and DDC features of the LM15851 make it ideally suited for this application.

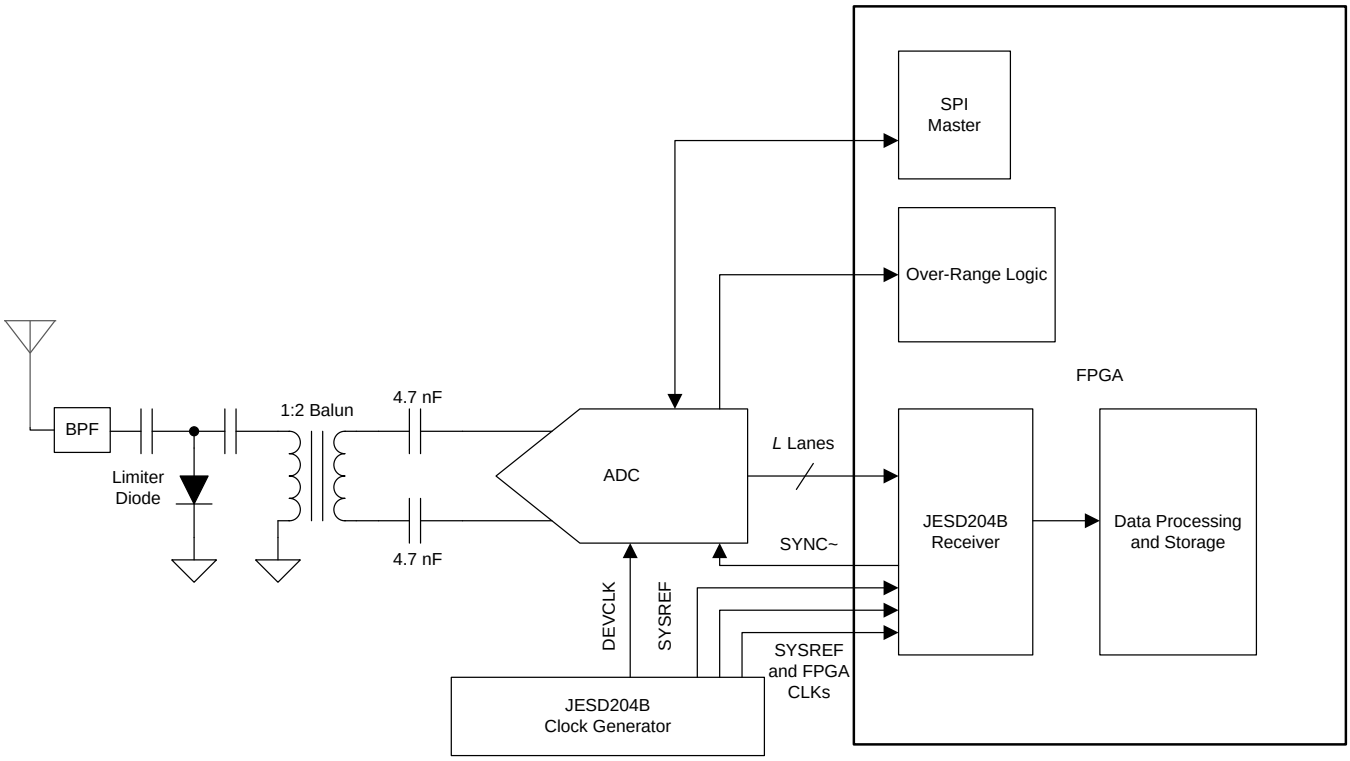



图 77. Simplified Schematic

## Typical Application (接下页)

### 8.2.1.1 Design Requirements

For this design example, use the parameters listed in 表 81.

**表 81. Design Parameters**

| DESIGN PARAMETERS | EXAMPLE VALUES |
|---|---|
| Signal center frequency | 2500 MHz |
| Signal bandwidth | 100 MHz |
| Signal nominal amplitude | –7 dBm |
| Signal maximum amplitude | 6 dBm |
| Minimum SINAD (in bandwidth of interest) | 48 dBc |
| Minimum SFDR (in bandwidth of interest) | 60 dBc |

### 8.2.1.2 Detailed Design Procedure

Use the following steps to design the RF receiver:

- Use the signal-center frequency and signal bandwidth to select an appropriate sampling rate (DEVCLK frequency) and decimate factor (x / 4 to x / 32).
- Select the sampling rate so that the band of interest is completely within a Nyquist zone.
- Select the sampling rate so that the band of interest is away from any harmonics or interleaving tones.
- Use a frequency planning tool, such as the ADC harmonic calculator (see the *开发支持* section).
- Select the decimation factor that provides the highest factor possible with an adequate alias-protected output bandwidth to capture the frequency bandwidth of interest.
- Select other system components to provide the needed signal frequency range and DEVCLK rate.
- See Table 1 for recommended balun components.
- Select bandpass filters and limiter components based on the requirement to attenuate unwanted signals outside the band of interest (blockers) and to prevent large signals from damaging the ADC inputs. See the *Absolute Maximum Ratings* table.

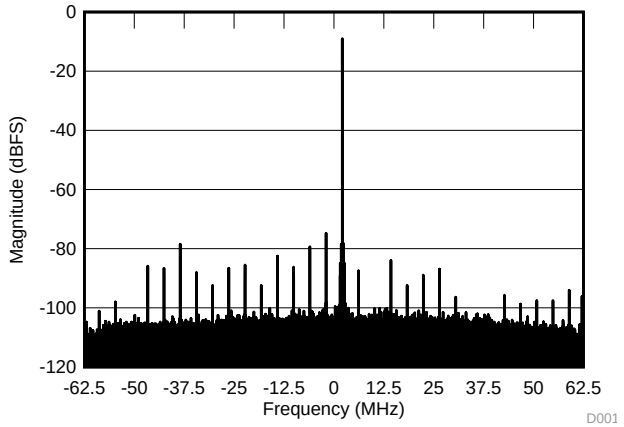
The LMK048xx JESD204B clocking devices can provide the DEVCLK clock and other system clocks for $f_{(DEVCLK)}$ < 3101 MHz.

For DEVCLK frequencies up to 4 GHz the consider using the LMX2581 and TRF3765 devices as the DEVCLK source. Use the LMK048xx device to provide the JESD204B clocks. For additional device information, see the *相关文档* section.

### 8.2.1.3 Application Curves

The following curve shows an RF signal at 2497.97 MHz captured at a sample rate of 4000 MSPS. 图 78 shows the spectrum for the output data in decimate-by-32 mode with $f_{(NCO)}$ equal to 2500 MHz. 图 78 shows the ability to provide only the spectrum of interest in the decimated output data.


版权 © 2014–2017, Texas Instruments Incorporated




$f_S$ = 4000 MSPS $F_{IN}$ = 2497.97 MHz at –7 dBFS $f_{(NCO)}$ = 2500 MHz

**图 78. Spectrum — Decimate-by-32**

## 8.3 Initialization Set-Up

### 8.3.1 JESD204B Startup Sequence

The JESD204B interface requires a specific startup and alignment sequence. The general order of that sequence is listed in the following steps.

1. Power up or reset the LM15851 device.
2. Program JESD_EN = 0 to shut down the link and enable configuration changes.
3. Program DECIMATE, SCRAM_EN, KM1 and DDR to the desired settings.
4. Configure the device calibration settings as desired, and initiate a calibration (set CAL_SFT = 1).
5. Program JESD_EN = 1 to enable the link.
6. Apply at least one SYSREF rising edge to establish the LMFC phase.
7. Assert SYNC~ from the data receiver to initiate link communications.
8. After the JESD204B receiver has established code group synchronization, SYNC~ is de-asserted and the ILA process begins.
9. Immediately following the end of the ILA sequence normal data output begins.

**注**

If deterministic latency is not required this step can be omitted.

## 8.4 Dos and Don'ts

### 8.4.1 Common Application Pitfalls

**Driving the inputs (analog or digital) beyond the power supply rails.** For device reliability, an input must not go more than 150 mV below the ground pins or 150 mV above the supply pins. Exceeding these limits even on a transient basis can cause faulty, or erratic, operation and can impair device reliability. High-speed digital circuits exhibiting undershoot that goes more than a volt below ground is common. To control overshoot, the impedance of high-speed lines must be controlled and these lines must be terminated in the characteristic impedance.

Care must be taken not to overdrive the inputs of the LM15851 device. Such practice can lead to conversion inaccuracies and even to device damage.

**Incorrect analog input common-mode voltage in the DC-coupled mode.** As described in the *The Analog Inputs* and *DC Coupled Input Usage* sections, the input common-mode voltage ($V_{CMI}$) must remain the specified range as referenced to the VCMO pin, which has a variability with temperature that must also be tracked. Distortion performance is degraded if the input common mode voltage is outside the specified $V_{CMI}$ range.

### Dos and Don'ts (接下页)

**Using an inadequate amplifier to drive the analog input.** Use care when choosing a high frequency amplifier to drive the LM15851 device because many high-speed amplifiers have higher distortion than the LM15851 device which results in overall system performance degradation.

**Driving the clock input with an excessively high level signal.** The ADC input clock level must not exceed the level described in the *Recommended Operating Conditions* table because the input offset can change if these levels are exceeded.

**Inadequate input clock levels.** As described in the *Using the Serial Interface* section, insufficient input clock levels can result in poor performance. Excessive input-clock levels can result in the introduction of an input offset.

**Using a clock source with excessive jitter, using an excessively long input clock signal trace, or having other signals coupled to the input clock signal trace.** These pitfalls cause the sampling interval to vary which causes excessive output noise and a reduction in SNR performance.

**Failure to provide adequate heat removal.** As described in the *Thermal Management* section, providing adequate heat removal is important to ensure device reliability. Adequate heat removal is primarily provided by properly connecting the thermal pad to the circuit board ground planes. Multiple vias should be arranged in a grid pattern in the area of the thermal pad. These vias will connect the topside pad to the internal ground planes and to a copper pour area on the opposite side of the printed circuit board.

## 9 Power Supply Recommendations

Data-converter-based systems draw sufficient transient current to corrupt their own power supplies if not adequately bypassed. A 10-µF capacitor must be placed within one inch (2.5 cm) of the device power pins for each supply voltage. A 0.1-µF capacitor must be placed as close as possible to each supply pin, preferably within 0.5 cm. Leadless chip capacitors are preferred due to their low-lead inductance.

As is the case with all high-speed converters, the LM15851 device must be assumed to have little power-supply noise-rejection. Any power supply used for digital circuitry in a system where a large amount of digital power is consumed must not be used to supply power to the LM15851 device. If not a dedicated supply, the ADC supplies must be the same supply used for other analog circuitry.

### 9.1 Supply Voltage

The LM15851 device is specified to operate with nominal supply voltages of 1.9 V (VA19) and 1.2 V (VA12, VD12). For detailed information regarding the operating voltage minimums and maximums see the *Recommended Operating Conditions* table.

During power-up the voltage on all 1.9-V supplies must always be equal to or greater than the voltage on the 1.2-V supplies. Similarly, during power-down, the voltage on the 1.2-V supplies must always be lower than or equal to that of the 1.9-V supplies. In general, supplying all 1.9-V buses from a single regulator, and all 1.2-V buses from a single regulator is the easiest method to ensure that the 1.9-V supplies are greater than the 1.2-V supplies. If the 1.2-V buses are generated from separate regulators, they must rise and fall together (within 200 mV).

The voltage on a pin, including a transient basis, must not have a voltage that is in excess of the supply voltage or below ground by more than 150 mV. A pin voltage that is higher than the supply or that is below ground can be a problem during startup and shutdown of power. Ensure that the supplies to circuits driving any of the input pins, analog or digital, do not rise faster than the voltage at the LM15851 power pins.

The values in the *Absolute Maximum Ratings* table must be strictly observed including during power up and power down. A power supply that produces a voltage spike at power turnon, turnoff, or both can destroy the LM15851 device. Many linear regulators produce output spiking at power on unless there is a minimum load provided. Active devices draw very little current until the supply voltages reach a few hundred millivolts. The result can be a turn-on spike that destroys the LM15851 device, unless a minimum load is provided for the supply. A 100-Ω resistor at the regulator output provides a minimum output current during power up to ensure that no turn-on spiking occurs. Whether a linear or switching regulator is used, TI recommends using a soft-start circuit to prevent overshoot of the supply.


版权 © 2014–2017, Texas Instruments Incorporated

# 10 Layout

## 10.1 Layout Guidelines

Proper grounding and proper routing of all signals is essential to ensure accurate conversion. Each ground layer should be a single unified ground plane, rather than splitting the ground planes into analog and digital areas.

Because digital switching transients are composed largely of high frequency components, the skin effect dictates that the total ground-plane copper weight has little effect upon the logic-generated noise. Total surface area is more important than the total ground-plane volume. Coupling between the typically-noisy digital circuitry and the sensitive analog circuitry can lead to poor performance that can be impossible to isolate and remedy. The solution is to keep the analog circuitry well separated from the digital circuitry.

High-power digital components must not be located on or near any linear component or power-supply trace or plane that services analog or mixed-signal components because the resulting common return current path could cause fluctuation in the analog input *ground* return of the ADC which causes excessive noise in the conversion result.

In general, assume that analog and digital lines must cross each other at 90° to avoid digital noise into the analog path. In high frequency systems, however, avoid crossing analog and digital lines altogether. The input clock lines must be isolated from **all** other lines, both analog and digital. The generally-accepted 90° crossing must be avoided because even a same amount of coupling causes problems at high frequencies. Best performance at high frequencies is obtained with a straight signal path.

Coupling onto or between the clock and input signal paths must be avoided using any isolation techniques available including distance isolation, orientation planning to prevent field coupling of components like inductors and transformers, and providing well coupled reference planes. Via stitching around the clock signal path and the input analog signal path provides a quiet ground reference for the critical signal paths and reduces noise coupling onto these paths. Sensitive signal traces must not cross other signal traces or power routing on adjacent PCB layers, rather a ground plane must separate the traces. If necessary, the traces should cross at 90° angles to minimize crosstalk.

Isolation of the analog input is important because of the low-level drive required of the LM15851 device. Quality analog input signal and clock signal path layout is required for full dynamic performance. Symmetry of the differential signal paths and discrete components in the path is mandatory and symmetrical shunt-oriented components should have a common grounding via. The high frequency requirements of the input and clock signal paths necessitate using differential routing with controlled impedances and minimizing signal path stubs (including vias) when possible.

Layout of the high-speed serial-data lines is of particular importance. These traces must be routed as tightly coupled 100-Ω differential pairs, with minimal vias. When vias must be used, care must be taken to implement control-impedance vias (that is, 50-Ω) with adjacent ground vias for image current control.

## 10.2 Layout Example

The following examples show layout-example plots (top and bottom layers only). 图 81 shows a typical stackup for a 10 layer board.

## Layout Example (接下页)

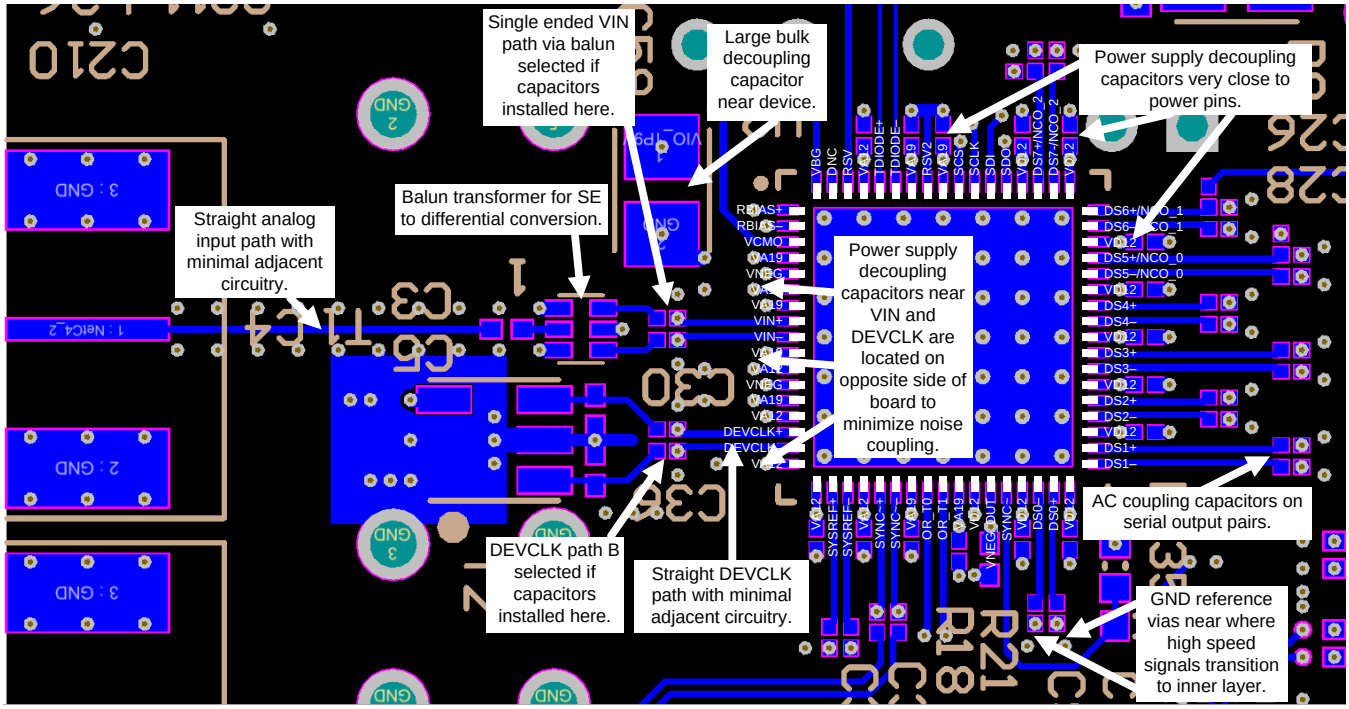



图 79. LM15851 Layout Example 1 — Top Side

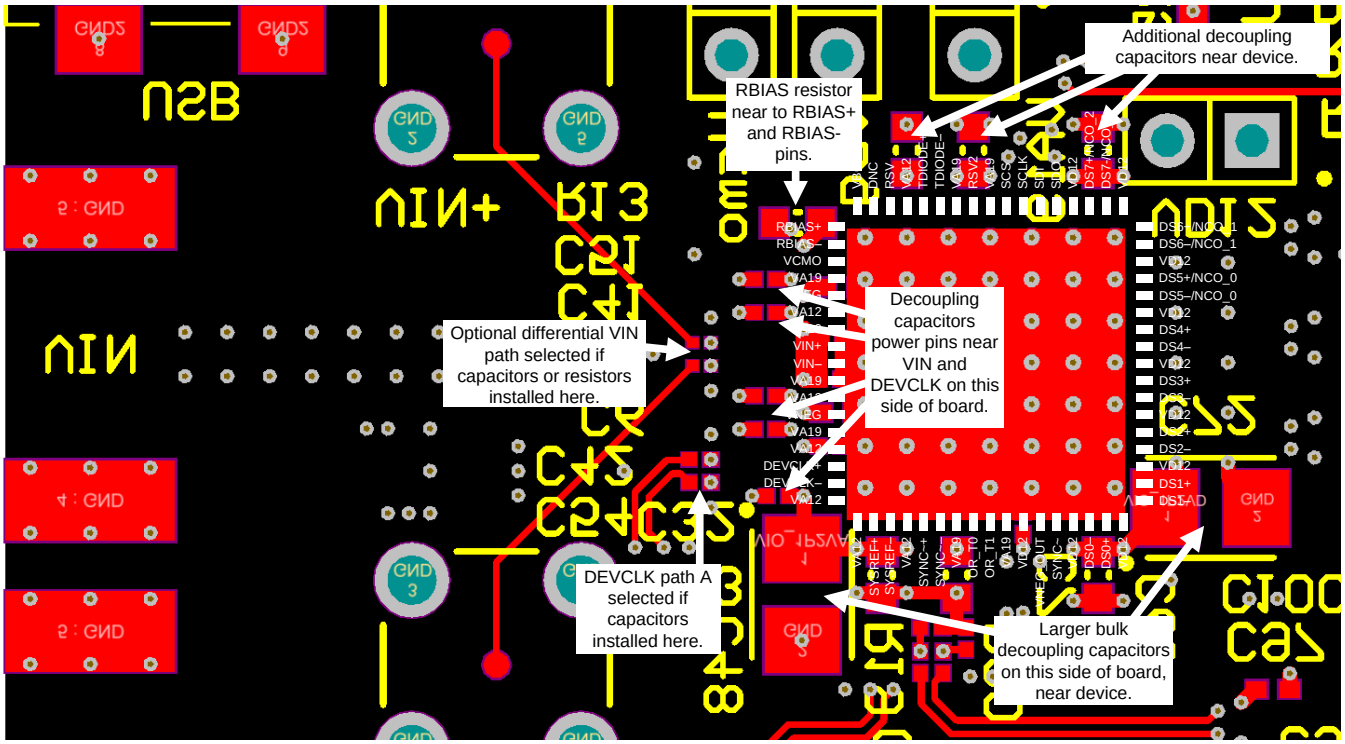
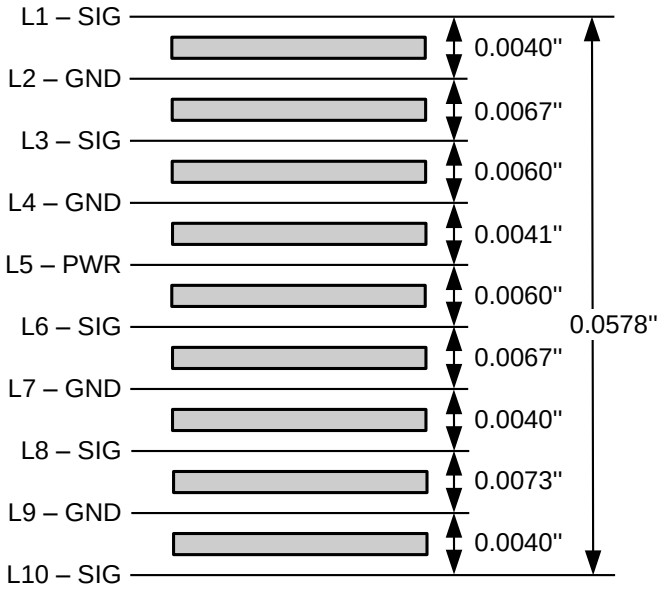



图 80. LM15851 Layout Example 2 — Bottom Side


版权 © 2014–2017, Texas Instruments Incorporated

## Layout Example (接下页)




1/2 oz. Copper on L1, L3, L6, L8, L10
1 oz. Copper on L2, L4, L5, L7, L9
100 Differential Signaling on SIG Layers
Low loss dielectric adjacent very high speed trace layers
Finished thickness 0.0620" including plating and solder mask

**图 81. LM15851 Typical Stackup — 10 Layer Board**

## 10.3 Thermal Management

The LM15851 device is capable of impressive speeds and performance at low power levels for speed. However, the power consumption is still high enough to require attention to thermal management. The VQFN package has a primary-heat transfer path through the center pad on the bottom of the package. The thermal resistance of this path is provided as $R_{\theta JCbot}$.

For reliability reasons, the die temperature must be kept to a maximum of 135°C which is the ambient temperature ($T_A$) plus the ADC power consumption multiplied by the net junction-to-ambient thermal resistance ($R_{\theta JA}$). Maintaining this temperature is not a problem if the ambient temperature is kept to a maximum of 85°C as specified in the *Recommended Operating Conditions* table and the center ground pad on the bottom of the package is thermally connected to a large-enough copper area of the PC board.

The package of the LM15851 device has a center pad that provides the primary heat-removal path as well as excellent electrical grounding to the PCB. Recommended land pattern and solder paste examples are provided in the *机械、封装和可订购信息* section. The center-pad vias shown must be connected to internal ground planes to remove the maximum amount of heat from the package, as well as to ensure best product parametric performance.

If needed to further reduce junction temperature, TI recommends to build a simple heat sink into the PCB which occurs by including a copper area of about 1 to 2 $cm^2$ on the opposite side of the PCB. This copper area can be plated or solder-coated to prevent corrosion, but should not have a conformal coating which would provide thermal insulation. Thermal vias will be used to connect these top and bottom copper areas and internal ground planes. These thermal vias act as *heat pipes* to carry the thermal energy from the device side of the board to the opposite side of the board where the heat can be more effectively dissipated.

# 11 器件和文档支持

## 11.1 器件支持

### 11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

### 11.1.2 开发支持

如需 ADC 谐波计算器，请访问 http://www.ti.com/tool/adc-harmonic-calc。

### 11.1.3 器件命名规则

孔径（采样）延迟 是在时钟输入的采样边沿测得的延迟量，经过此段延迟后将在器件内部对输入引脚的信号进行采样。

孔径抖动 **($t_{(AJ)}$)** 是采样与采样之间的孔径延迟变化。孔径抖动以输入噪声的形式出现。

时钟占空比 是时钟波形为逻辑高电平的时间与一个时钟周期总时长的比率。

全功率带宽 **(FPBW)** 是一个频率测量值，在此频率下，重构的输出基频会降至满量程输入的低频值以下 3dB。

交错毛刺 是 ADC 多组交叉架构中的非理想条件产生的频域 (FFT) 效应。
各组间的偏移误差在 $f_S/4$ 和 $f_S/2$ 时会产生固定毛刺。增益和时序误差在 $f_S / 4 \pm F_{IN}$ 以及 $f_S / 2 \pm F_{IN}$ 时会产生输入信号相关毛刺。

互调失真 **(IMD)** 是由于两个正弦频率同时被施加到 ADC 输入上所产生的额外频谱分量。IMD 定义为二阶和三阶互调产品功率与某原始频率下的功率之比。IMD 通常以 dBFS 为单位。

最低有效位 **(LSB)** 是所有位中具有最小值或最低权重的位。此值根据公式 18 进行计算。

$V_{FS(dif)} / 2^n$

其中

- $V_{FS(dif)}$ 为 $V_I$ 的差分满量程幅值，如 FSR 输入所设（引脚 14）


版权 © 2014–2017, Texas Instruments Incorporated

器件支持 (接下页)

- *n* 为 ADC 分辨率（以位为单位），LM15851 器件对应的 n = 12 (18)

**电流模式逻辑 (CML) 差分输出电压 ($V_{OD}$)** 是正负输出电压间差值的绝对值。所有输出均相对于接地端测量。

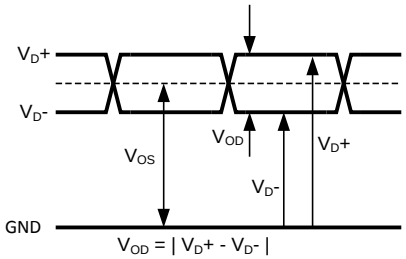



图 **82. CML** 输出信号电平

**CML 输出偏移电压 ($V_{O(ofs)}$)** 是 D+ 和 D– 引脚间输出电压的平均值。公式 19 为 $V_{OS}$ 示例。

$$[(V_D+) + (V_D–)] / 2 \quad (19)$$

**最高有效位 (MSB)** 是具有最大值或最高权重的位。MSB 的值为满量程的一半。

**超量程恢复时间** 是转换器差分输入电压从 ±1.2V 变为 0V 后恢复并以额定精度进行转换所需的时间。

**其它毛刺** 是所有高次谐波（四次及以上）、交错毛刺和所有其它固定毛刺或输入相关毛刺的总和。

**数据延迟（延迟）** 是开始转换到串行器输出相关数据期间的输入时钟周期数。

**无杂散动态范围 (SFDR)** 是输出端输入信号与杂散信号峰值的均方根 (RMS) 值间的差值（以 dB 为单位），其中杂散信号是出现在输出频谱但未出现在输入频谱的所有信号，直流信号除外。

**总谐波失真 (THD)** 是输出端前九个谐波总值与输出端基频值之比的 RMS 值（以 dB 为单位）。总谐波失真 (THD) 根据公式 20 计算。

$$THD = 20 \times \log \sqrt{\frac{A_{f2}^2 + \ldots + A_{f10}^2}{A_{f1}^2}}$$

其中

- $A_{(f1)}$ 是基频（输出）的 RMS 功率
- $A_{(f2)}$ 到 $A_{(f10)}$ 是输出频谱中前九个谐波频率的 RMS 功率 (20)

**二次谐波失真 (2nd Harm)** 是输出端检测到的输入频率 RMS 功率与输出端二次谐波功率之间的差值（以 dB 为单位）。

**三次谐波失真 (3rd Harm)** 是输出端检测到的输入频率 RMS 功率与输出端三次谐波功率之间的差值（以 dB 为单位）。

**误字率** 是出错率，定义为单位时间内可能出错的字数除以该时间内检查的字数。误字率 $10^{-18}$ 指大约每四年会有一个转换出现统计误差。

## 11.2 文档支持

### 11.2.1 相关文档

请参阅如下相关文档：

- *LMH3401 7GHz 超宽带固定增益全差分放大器*，SBOS695
- *LMK0482x 具有双环 PLL 的超低噪声 JESD204B 兼容时钟抖动消除器*，SNAS605
- *LMX2581 具有集成压控振荡器 (VCO) 的宽带频率合成器*，SNAS601
- *TRF3765 具有集成 VCO 的整数 N/分数 N 锁相环 (PLL)*，SLWS230

## 11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

社区资源 (接下页)

**TI E2E™ 在线社区** ***TI 的工程师对工程师 (E2E) 社区。***此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

**设计支持** ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

### 11.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

### 11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。


版权 © 2014–2017, Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LM15851NKE | ACTIVE | VQFN | NKE | 68 | 168 | RoHS & Green | SN | Level-3-260C-168 HR | -40 to 85 | LM15851 | Samples |
| LM15851NKER | ACTIVE | VQFN | NKE | 68 | 2000 | RoHS & Green | SN | Level-3-260C-168 HR | -40 to 85 | LM15851 | Samples |
| LM15851NKET | ACTIVE | VQFN | NKE | 68 | 250 | RoHS & Green | SN | Level-3-260C-168 HR | -40 to 85 | LM15851 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

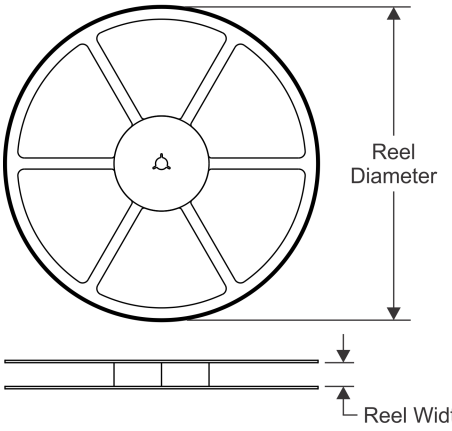
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

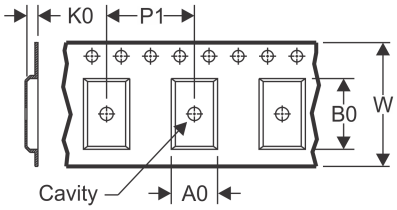
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

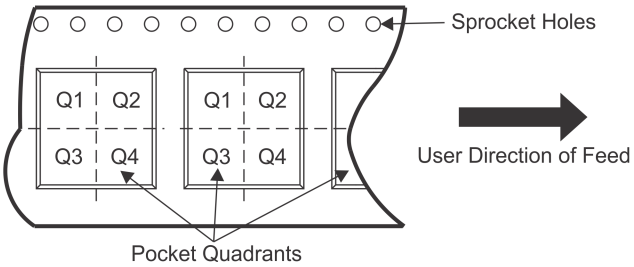



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

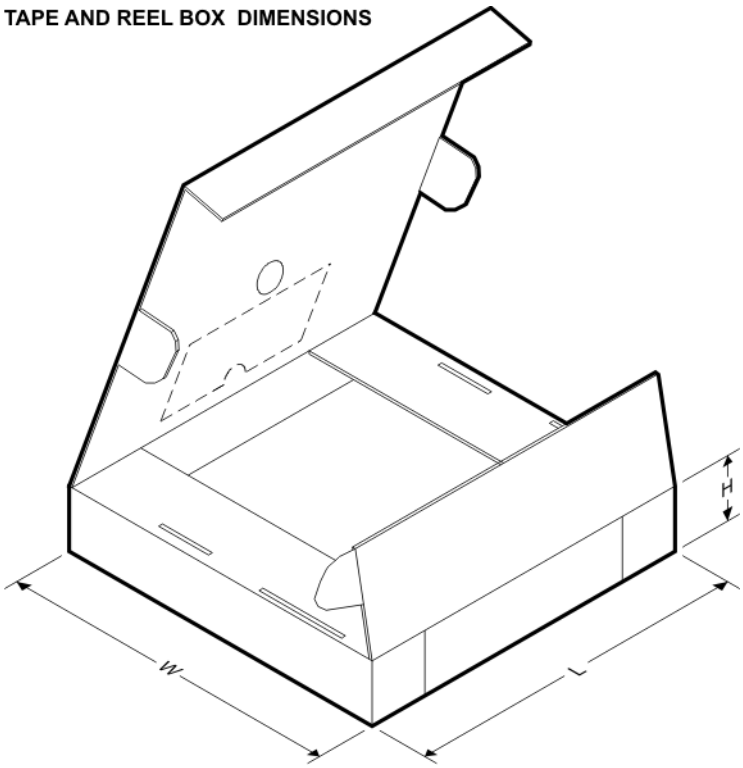
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM15851NKER | VQFN | NKE | 68 | 2000 | 330.0 | 24.4 | 10.3 | 10.3 | 1.1 | 16.0 | 24.0 | Q1 |
| LM15851NKET | VQFN | NKE | 68 | 250 | 178.0 | 24.4 | 10.3 | 10.3 | 1.1 | 16.0 | 24.0 | Q1 |

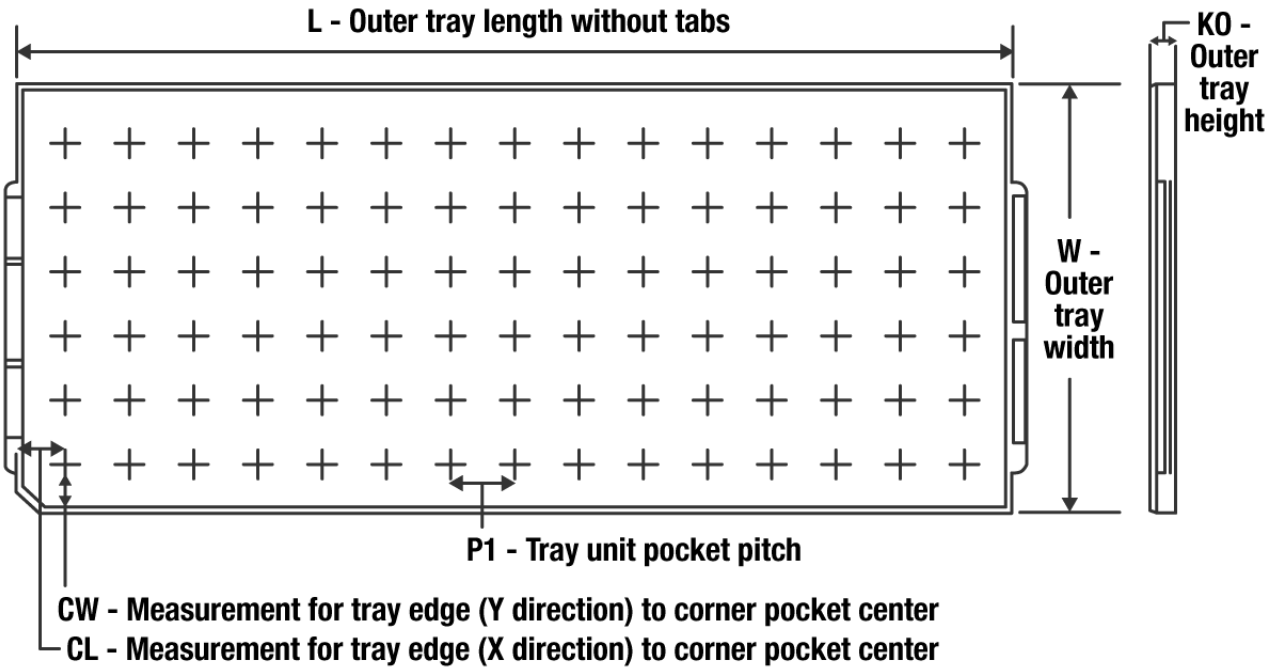
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM15851NKER | VQFN | NKE | 68 | 2000 | 367.0 | 367.0 | 45.0 |
| LM15851NKET | VQFN | NKE | 68 | 250 | 213.0 | 191.0 | 55.0 |

## TRAY




Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

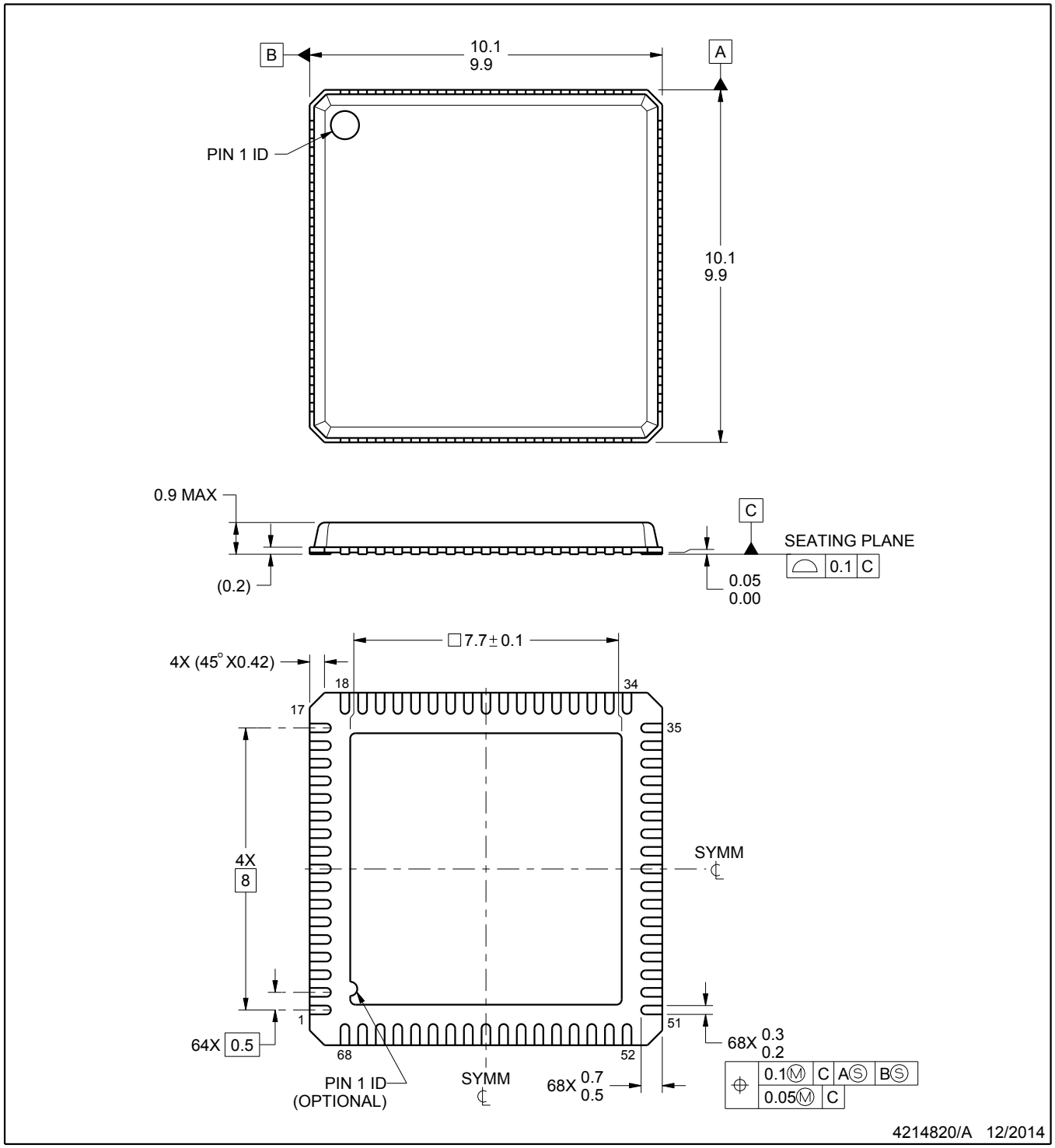
| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM15851NKE | NKE | VQFNP | 68 | 168 | 8 X 21 | 150 | 322.6 | 135.9 | 7620 | 14.65 | 11 | 11.95 |

# PACKAGE OUTLINE

## NKE0068A

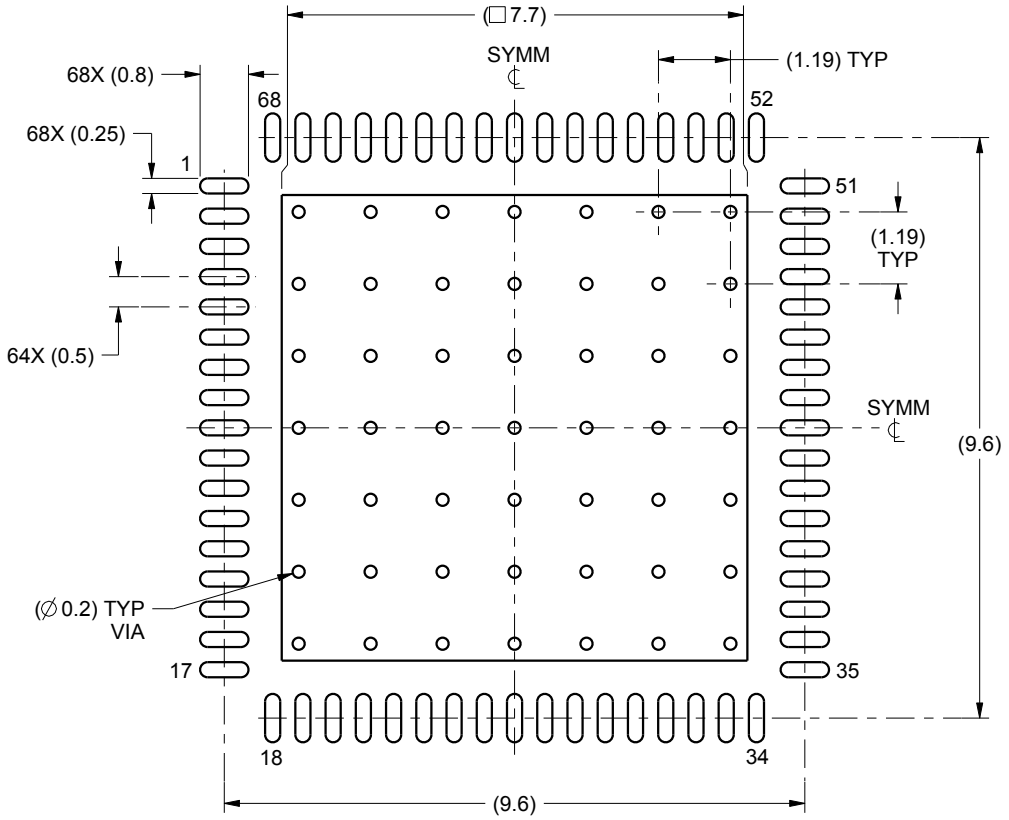
## VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

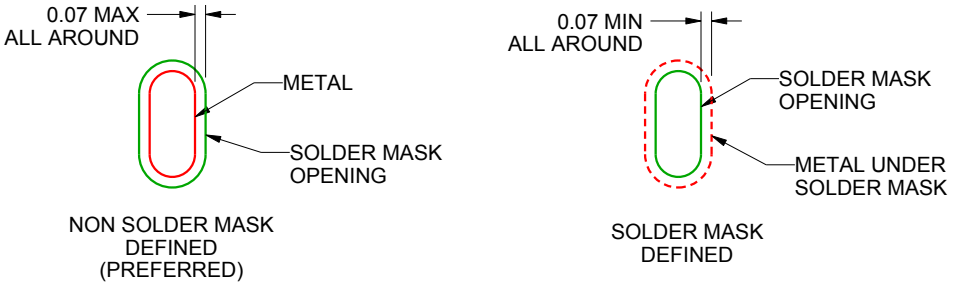



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:8X

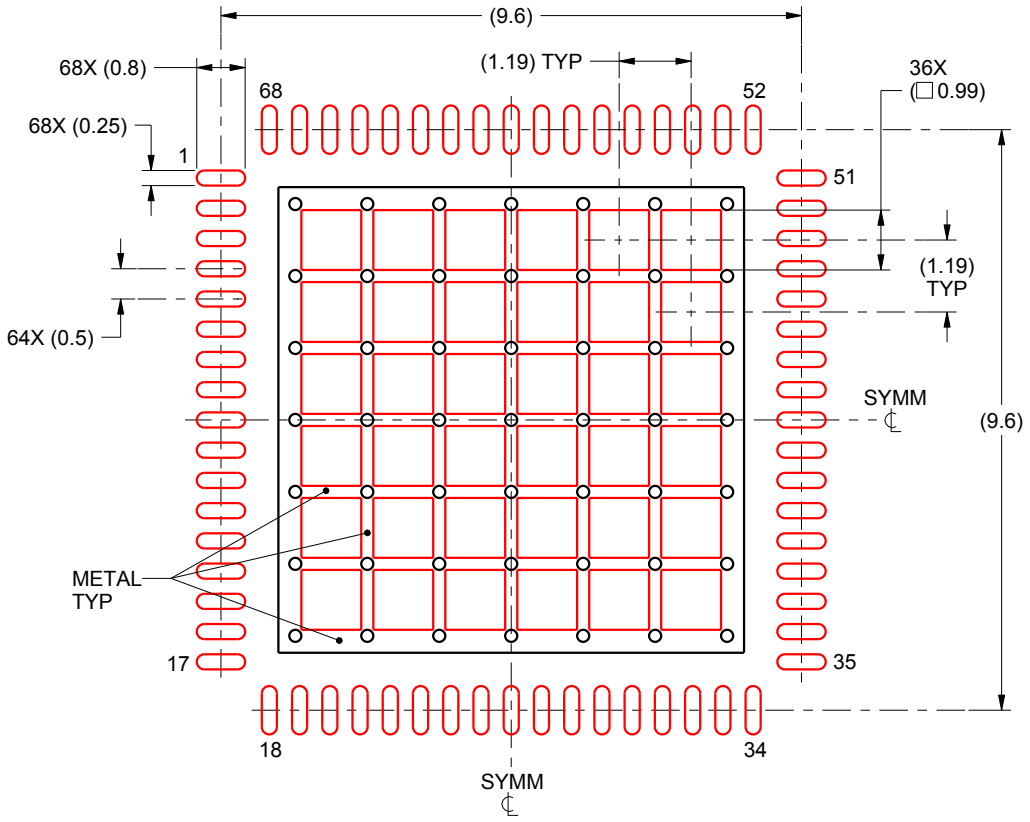



SOLDER MASK DETAILS

4214820/A 12/2014

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
60% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

4214820/A 12/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# 重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022，德州仪器 (TI) 公司