

LM339、LM239、LM139、LM2901 四路差分比较器

1 特性

- 宽电源范围
 - 单电源：2V 至 36V
(对于非 V 后缀器件进行了 30V 测试，对于 V 后缀器件进行了 32V 测试)
 - 双电源：±1V 至 ±18V
(对于非 V 后缀器件进行了 ±15V 测试，对于 V 后缀器件进行了 ±16V 测试)
- 独立于电源电压的低电源电流
消耗：0.8mA (典型值)
- 低输入偏置电流：25nA (典型值)
- 低输入失调电流：3nA (典型值) (LM139)
- 低输入失调电压：2mV (典型值)
- 共模输入电压范围
包括接地
- 差分输入电压范围等于最大额定电源电压：±36V
- 低输出饱和电压
- 输出与 TTL、MOS 和 CMOS 兼容
- 对于符合 MIL-PRF-38535 标准的产品，所有参数均经过测试，除非另外注明。对于所有其他产品，生产流程不一定包含对所有参数的测试。

2 应用

- 工业
- 汽车应用
 - 信息娱乐系统和仪表组
 - 车身控制模块
- 电源监控
- 振荡器
- 峰值检测器
- 逻辑电压转换

3 说明

LMx39x 和 LM2901x 器件包含四个独立的电压比较器，这些比较器可在宽电压范围内由单电源供电。这些器件也可以由双电源供电，只要两个电源之间的电压差处于 2V 至 36V 的范围之内且 V_{CC} 比输入共模电压至少高 +1.5V 以上即可。漏极电流不受电源电压的影响。可将输出连接到其它集电极开路输出，以实现有线 AND 关联。

LM139 和 LM139A 器件在 -55°C 至 +125°C 的完整军用温度范围内运行。LM239 和 LM239A 器件的额定工作温度范围是 -25°C 至 +85°C。LM339 和 LM339A 器件的额定工作温度范围是 -0°C 至 70°C。LM2901、LM2901AV 和 LM2901V 器件的额定工作温度范围是 -40°C 至 125°C。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
LM139x	CDIP (14)	21.30mm × 7.60mm
	LCCC (20)	8.90mm × 8.90mm
	CFP (14)	9.20mm × 6.29mm
LM139x、LM239x、LM339x、LM2901x	SOIC (14)	8.70mm × 3.90mm
LM239、LM339x、LM2901	PDIP (14)	19.30mm × 6.40mm
LM239、LM2901	TSSOP (14)	5.00mm × 4.40mm
LM339x、LM2901	SO (14)	10.20mm × 5.30mm
LM339x	SSOP (14)	6.50mm × 5.30mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision T (June 2015) to Revision U	Page
• 已更改 在说明 部分中将 LM239x 温度范围从 125°C 更改成了 85°C	1
• 已更改 更改了数据表标题	1
• Changed LM293AD to LM239AD in <i>Device Comparison Table</i>	3
• Changed 'I' to dash in GND and VCC in I/O column of the <i>Pin Functions</i> table	4
• Added Input Current and related footnote in <i>Absolute Maximum Ratings</i>	5
• Changed layout of <i>Recommended Operating Conditions</i> temperatures to separate rows	5
• Changed values in the Thermal Information table to align with JEDEC standards	6
• Added LM2901V and LMV2901AV to LM2901 Elect Char Table title to make more clear which devices are covered.	8
• Changed "Dual" to "Quad" and removed "Absolute Maximum" wording and mention of Q100 in <i>Overview</i> section text. ...	11
• Changed and corrected text in <i>Feature Description</i> section	11
• Changed Example Values in <i>Typical Application Design Parameters</i> table	12
• 已添加 添加了接收文档更新通知 部分	15

Changes from Revision S (August 2012) to Revision T	Page
• 删除了订购信息 表。	1
• 在特性 列表中添加了“军用免责声明”。	1
• 添加了 应用、器件信息 表、引脚配置和功能 部分、ESD 额定值 表、热性能信息 表、特性 说明 部分、器件功能模式、应用和实施 部分、电源建议 部分、布局 部分、器件和文档支持 部分以及机械、封装和可订购信息 部分。无规格变化。	1

5 Device Comparison Table

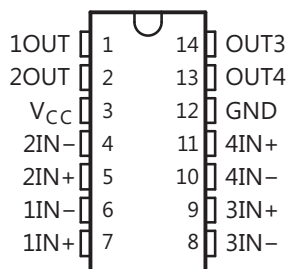
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM139J, LM139AJ	CDIP (14)	21.30 mm × 7.60 mm
LM139FK, LM139AFK	LCCC (20)	8.90 mm × 8.90 mm
LM139W, LM139AW	CFP (14)	9.20 mm × 6.29 mm
LM139D, LM139AD, LM239D, LM239AD, LM339D, LM339AD, LM2901D	SOIC (14)	8.70 mm × 3.90 mm
LM239N, LM339N, LM339AN, LM2901N	PDIP (14)	19.30 mm × 6.40 mm
LM239PW, LM2901PW	TSSOP (14)	5.00 mm × 4.40 mm
LM339NS, LM339ANS, LM2901NS	SOP (14)	10.20 mm × 5.30 mm
LM339DB, LM339ADB	SSOP (14)	6.50 mm × 5.30 mm

OTHER QUALIFIED VERSIONS OF LM139-SP, LM239A, LM2901, LM2901AV, LM2901V:

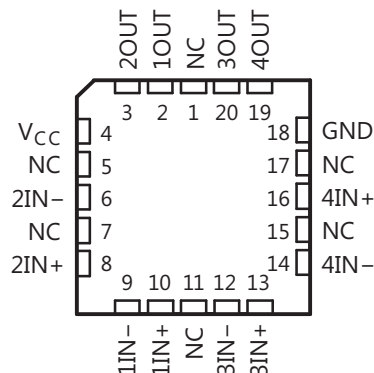
- Automotive Q100: [LM239A-Q1](#), [LM2901-Q1](#), [LM2901AV-Q1](#), [LM2901V-Q1](#)
- Enhanced Product: [LM239A-EP](#)
- Space: [LM139-SP](#)

6 Pin Configuration and Functions

D, DB, N, NS, PW, J, or W Package
SOIC, SSOP, PDIP, SO, TSSOP, CDIP, or CFP
Top View



FK Package
20-Pin LCCC⁽¹⁾
Top View



(1) NC = no internal connection.

Pin Functions

PIN			I/O ⁽¹⁾	DESCRIPTION
NAME	D, J, W, B, PW, DB, N, NS	FK		
1IN+	7	10	I	Positive input pin of the comparator 1
1IN-	6	9	I	Negative input pin of the comparator 1
1OUT	1	2	O	Output pin of the comparator 1
2IN+	5	8	I	Positive input pin of the comparator 2
2IN-	4	6	I	Negative input pin of the comparator 2
2OUT	2	3	O	Output pin of the comparator 2
3IN+	9	13	I	Positive input pin of the comparator 3
3IN-	8	12	I	Negative input pin of the comparator 3
3OUT	14	20	O	Output pin of the comparator 3
4IN+	11	16	I	Positive input pin of the comparator 4
4IN-	10	14	I	Negative input pin of the comparator 4
4OUT	13	19	O	Output pin of the comparator 4
GND	12	18	—	Ground
V _{CC}	3	4	—	Supply pin
NC	—	1	—	No connect (no internal connection)
		5		
		7		
		11		
		15		
		17		

(1) I = Input, O = Output

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽²⁾		36	V
V _{ID}	Differential input voltage ⁽³⁾		±36	V
V _I	Input voltage range (either input)	–0.3	36	V
I _K	Input current ⁽⁴⁾		–50	mA
V _O	Output voltage		36	V
I _O	Output current		20	mA
	Duration of output short circuit to ground ⁽⁵⁾	Unlimited		
T _J	Operating virtual-junction temperature		150	°C
	Case temperature for 60 s	FK package	260	°C
	Lead temperature 1.6 mm (1/16 in) from case for 60 s	J package	300	°C
T _{stg}	Storage temperature	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to network ground.
- (3) Differential voltages are at xIN+ with respect to xIN–.
- (4) Input current flows through parasitic diode to ground and will turn on parasitic transistors that will increase I_{CC} and may cause output to be incorrect. Normal operation resumes when input is removed.
- (5) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±500
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±750

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage	Non-V devices	2	30	V
		V devices	2	32	V
T _J	Junction temperature	LM139x	–55	125	°C
		LM239x	–25	85	
		LM339x	–0	70	
		LM2901x	–40	125	

7.4 Thermal Information (14-Pin Packages)

THERMAL METRIC ⁽¹⁾	LMx39, LM2901x							UNIT
	D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	J (CDIP)	W (CFP)	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	98.8	111.8	79	96.2	120	89.5	156.2	°C/W
$R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance	64.3	63.6	73.4	56.1	59	46.1	86.7	°C/W
$R_{\theta JB}$ Junction-to-board thermal resistance	59.7	60.5	58.7	56.9	68.8	78.7	154.6	°C/W
Ψ_{JT} Junction-to-top characterization parameter	25.7	26.2	48.3	24.8	9.9	3	56.5	°C/W
Ψ_{JB} Junction-to-board characterization parameter	59.3	59.8	58.5	56.4	68.2	71.8	133.5	°C/W
$R_{\theta JC(bot)}$ Junction-to-case (bottom) thermal resistance	—	—	—	—	—	24.2	14.3	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Thermal Information (20-Pin Packages)

THERMAL METRIC ⁽¹⁾	LM139x	UNIT
	FK (LCCC)	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	82.5	°C/W
$R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance	60.7	°C/W
$R_{\theta JB}$ Junction-to-board thermal resistance	59.4	°C/W
Ψ_{JT} Junction-to-top characterization parameter	53	°C/W
Ψ_{JB} Junction-to-board characterization parameter	58.4	°C/W
$R_{\theta JC(bot)}$ Junction-to-case (bottom) thermal resistance	9.7	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.6 Electrical Characteristics for LM139 and LM139A

at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS ⁽¹⁾	T_A ⁽²⁾	LM139			LM139A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{CC} = 5\text{ V to } 30\text{ V}$, $V_{IC} = V_{ICR\text{ min}}$, $V_O = 1.4\text{ V}$	25°C		2	5		1	2	mV
		Full range			9			4	
I_{IO} Input offset current	$V_O = 1.4\text{ V}$	25°C		3	25		3	25	nA
		Full range			100			100	
I_{IB} Input bias current	$V_O = 1.4\text{ V}$	25°C		–25	–100		–25	–100	nA
		Full range			–300			–300	
V_{ICR} Common-mode input-voltage range ⁽³⁾		25°C		0 to $V_{CC} - 1.5$			0 to $V_{CC} - 1.5$		V
		Full range		0 to $V_{CC} - 2$			0 to $V_{CC} - 2$		
A_{VD} Large-signal differential-voltage amplification	$V_{CC+} = \pm 7.5\text{ V}$, $V_O = -5\text{ V to } 5\text{ V}$	25°C		200			50	200	V/mV
I_{OH} High-level output current	$V_{ID} = 1\text{ V}$ $V_{OH} = 5\text{ V}$ $V_{OH} = 30\text{ V}$	25°C		0.1			0.1		nA
		Full range			1			1	μA
V_{OL} Low-level output voltage	$V_{ID} = -1\text{ V}$, $I_{OL} = 4\text{ mA}$	25°C		150	400		150	400	mV
		Full range			700			700	
I_{OL} Low-level output current	$V_{ID} = -1\text{ V}$, $V_{OL} = 1.5\text{ V}$	25°C		6	16		6	16	mA
I_{CC} Supply current (four comparators)	$V_O = 2.5\text{ V}$, No load	25°C		0.8	2		0.8	2	mA

- (1) All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
- (2) Full range (MIN to MAX) for LM139 and LM139A is –55°C to +125°C. All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
- (3) The voltage at either input or common-mode must not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is $V_{CC+} - 1.5\text{ V}$; however, one input can exceed V_{CC} , and the comparator will provide a proper output state as long as the other input remains in the common-mode range. Either or both inputs can go to 30 V without damage.

7.7 Electrical Characteristics for LMx39 and LMx39A

at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS ⁽¹⁾	T_A ⁽²⁾	LM239 LM339			LM239A LM339A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{CC} = 5\text{ V to } 30\text{ V}$, $V_{IC} = V_{ICR\text{ min}}$, $V_O = 1.4\text{ V}$	25°C		2	5		1	3	mV
		Full range			9			4	
I_{IO} Input offset current	$V_O = 1.4\text{ V}$	25°C		5	50		5	50	nA
		Full range			150			150	
I_{IB} Input bias current	$V_O = 1.4\text{ V}$	25°C		–25	–250		–25	–250	nA
		Full range			–400			–400	
V_{ICR} Common-mode input-voltage range ⁽³⁾		25°C		0 to $V_{CC} - 1.5$			0 to $V_{CC} - 1.5$		V
		Full range		0 to $V_{CC} - 2$			0 to $V_{CC} - 2$		
A_{VD} Large-signal differential-voltage amplification	$V_{CC} = 15\text{ V}$, $V_O = 1.4\text{ V to } 11.4\text{ V}$, $R_L \geq 15\text{ k}\Omega\text{ to } V_{CC}$	25°C		50	200		50	200	V/mV

- (1) All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
- (2) Full range (MIN to MAX) for LM239/LM239A is –25°C to +85°C, and for LM339/LM339A is 0°C to 70°C. All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
- (3) The voltage at either input or common-mode must not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is $V_{CC+} - 1.5\text{ V}$; however, one input can exceed V_{CC} , and the comparator will provide a proper output state as long as the other input remains in the common-mode range. Either or both inputs can go to 30 V without damage.

Electrical Characteristics for LMx39 and LMx39A (continued)

at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS ⁽¹⁾		T_A ⁽²⁾	LM239 LM339			LM239A LM339A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{OH} High-level output current	$V_{ID} = 1\text{ V}$	$V_{OH} = 5\text{ V}$	25°C		0.1	50		0.1	50	nA
		$V_{OH} = 30\text{ V}$	Full range			1			1	μA
V_{OL} Low-level output voltage	$V_{ID} = -1\text{ V}$, $I_{OL} = 4\text{ mA}$		25°C		150	400		150	400	mV
			Full range			700			700	
I_{OL} Low-level output current	$V_{ID} = -1\text{ V}$, $V_{OL} = 1.5\text{ V}$		25°C	6	16		6	16		mA
I_{CC} Supply current (four comparators)	$V_O = 2.5\text{ V}$, No load		25°C		0.8	2		0.8	2	mA

7.8 Electrical Characteristics for LM2901, LM2901V and LM2901AV

at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS ⁽¹⁾		T_A ⁽²⁾	LM2901			UNIT
				MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = V_{ICR}\text{ min}$, $V_O = 1.4\text{ V}$, $V_{CC} = 5\text{ V to MAX}^{(3)}$	Non-A devices	25°C		2	7	mV
			Full range			15	
		A-suffix devices	25°C		1	2	
			Full range			4	
I_{IO} Input offset current	$V_O = 1.4\text{ V}$		25°C		5	50	nA
			Full range			200	
I_{IB} Input bias current	$V_O = 1.4\text{ V}$		25°C		-25	-250	nA
			Full range			-500	
V_{ICR} Common-mode input-voltage range ⁽⁴⁾			25°C		0 to $V_{CC} - 1.5$		V
			Full range		0 to $V_{CC} - 2$		
A_{VD} Large-signal differential-voltage amplification	$V_{CC} = 15\text{ V}$, $V_O = 1.4\text{ V to } 11.4\text{ V}$, $R_L \geq 15\text{ k}\Omega\text{ to } V_{CC}$		25°C		25	100	V/mV
I_{OH} High-level output current	$V_{ID} = 1\text{ V}$	$V_{OH} = 5\text{ V}$	25°C		0.1	50	nA
		$V_{OH} = V_{CC}\text{ MAX}^{(3)}$	Full range			1	μA
V_{OL} Low-level output voltage	$V_{ID} = -1\text{ V}$, $I_{OL} = 4\text{ mA}$	Non-V devices	25°C		150	500	mV
		V-suffix devices			150	400	
		All devices	Full range			700	
I_{OL} Low-level output current	$V_{ID} = -1\text{ V}$, $V_{OL} = 1.5\text{ V}$		25°C	6	16		mA
I_{CC} Supply current (four comparators)	$V_O = 2.5\text{ V}$, No load	$V_{CC} = 5\text{ V}$	25°C		0.8	2	mA
		$V_{CC} = \text{MAX}^{(3)}$			1	2.5	

- (1) All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
- (2) Full range (MIN to MAX) for LM2901 is -40°C to +125°C. All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
- (3) $V_{CC}\text{ MAX} = 30\text{ V}$ for non-V devices, and 32 V for V-suffix devices
- (4) The voltage at either input or common-mode must not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is $V_{CC} + 1.5\text{ V}$; however, one input can exceed V_{CC} , and the comparator will provide a proper output state as long as the other input remains in the common-mode range. Either or both inputs can go to $V_{CC}\text{ MAX}$ without damage.

7.9 Switching Characteristics for LM2901

 $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS		LM2901	UNIT
			TYP	
Response time	R_L connected to 5 V through 5.1 k Ω , $C_L = 15\text{ pF}^{(1)(2)}$	100-mV input step with 5-mV overdrive	1.3	μs
		TTL-level input step	0.3	

(1) C_L includes probe and jig capacitance.

(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

7.10 Switching Characteristics for LM139 and LM139A

 $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS		LM139 LM139A	UNIT
			TYP	
Response time	R_L connected to 5 V through 5.1 k Ω , $C_L = 15\text{ pF}^{(1)(2)}$	100-mV input step with 5-mV overdrive	1.3	μs
		TTL-level input step	0.3	

(1) C_L includes probe and jig capacitance.

(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

7.11 Switching Characteristics for LMx39 and LMx39A

 $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS		LM239 LM239A LM339 LM339A	UNIT
			TYP	
Response time	R_L connected to 5 V through 5.1 k Ω , $C_L = 15\text{ pF}^{(1)(2)}$	100-mV input step with 5-mV overdrive	1.3	μs
		TTL-level input step	0.3	

(1) C_L includes probe and jig capacitance.

(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

7.12 Typical Characteristics

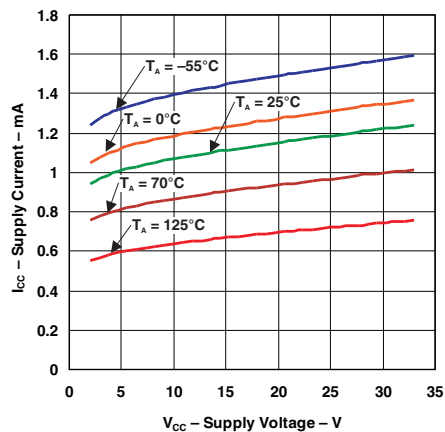


Figure 1. Supply Current vs Supply Voltage

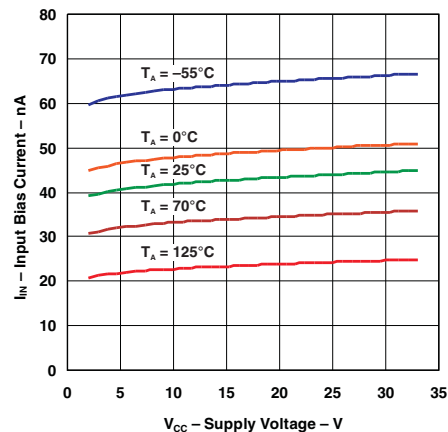


Figure 2. Input Bias Current vs Supply Voltage

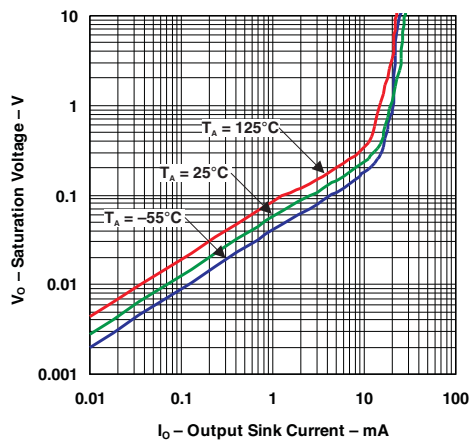


Figure 3. Output Saturation Voltage

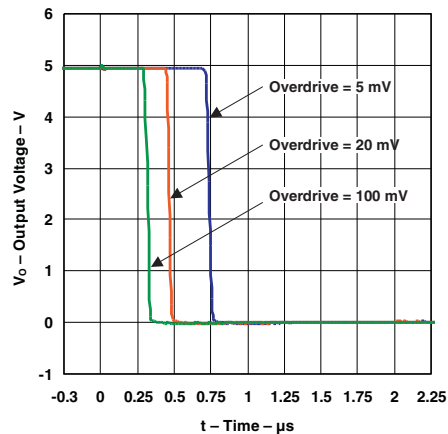


Figure 4. Response Time for Various Overdrives
Negative Transition

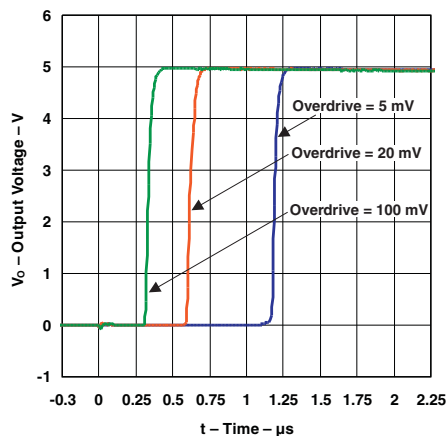


Figure 5. Response Time for Various Overdrives
Positive Transition

8 Detailed Description

8.1 Overview

The LMx39 and LM2901x are quad comparators with the ability to operate up to an absolute maximum of 36 V on the supply pin. This standard device has proven ubiquity and versatility across a wide range of applications. This is due to very wide supply voltages range (2 V up to 32 V), low I_q , and fast response of the device.

The open-drain output allows the user to configure the output logic low voltage (V_{OL}) and allows the comparator to be used in AND functionality.

8.2 Functional Block Diagram

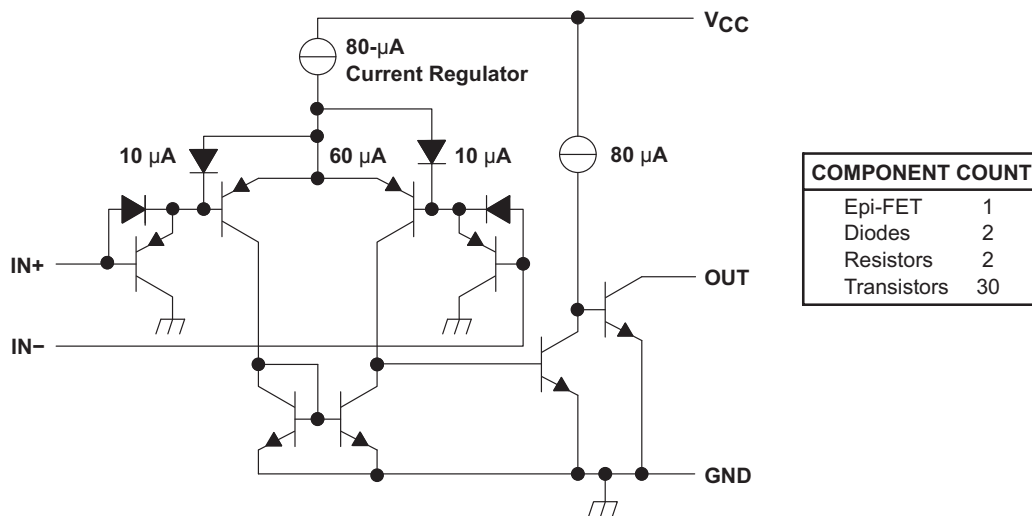


Figure 6. Schematic (Each Comparator)

8.3 Feature Description

The comparator consists of a PNP Darlington pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The input Darlington pair creates a limit on the input common-mode voltage capability, allowing the comparator to accurately function from ground to ($V_{CC} - 1.5$ V) differential input. Allow for ($V_{CC} - 2$ V) at cold temperature.

The output consists of an open-collector NPN (pulldown or low-side) transistor. The output NPN sinks current when the negative input voltage is higher than the positive input voltage and the offset voltage. The V_{OL} is resistive and scales with the output current. See the [Specifications](#) section for V_{OL} values with respect to the output current.

8.4 Device Functional Modes

8.4.1 Voltage Comparison

The comparator operates solely as a voltage comparator, comparing the differential voltage between the positive and negative pins and outputting a logic low or high impedance (logic high with pullup) based on the input differential polarity.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Validate and test the design implementation to confirm system functionality.

9.1 Application Information

Typically, a comparator compares either a single signal to a reference, or to two different signals. Many users take advantage of the open-drain output to drive the comparison logic output to a logic voltage level to an MCU or logic device. The wide supply range and high voltage capability makes LMx39 or LM2901x optimal for level shifting to a higher or lower voltage.

9.2 Typical Application

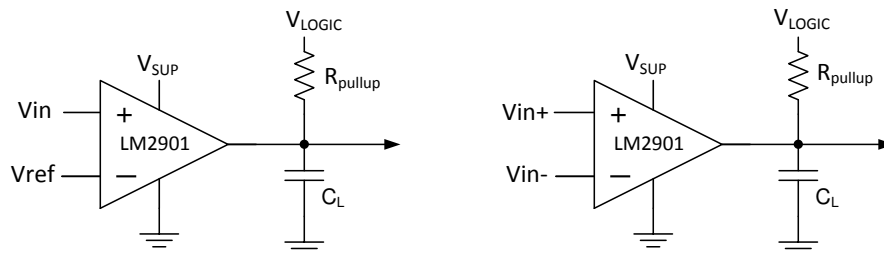


Figure 7. Single-ended and Differential Comparator Configurations

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0 V to $V_{sup}-1.5$ V
Supply Voltage	4.5 V to V_{CC} maximum
Logic Supply Voltage	0 V to V_{CC} maximum
Output Current (R_{PULLUP})	1 μ A to 4 mA
Input Overdrive Voltage	100 mV
Reference Voltage	2.5 V
Load Capacitance (C_L)	15 pF

9.2.2 Detailed Design Procedure

When using the LMx39 in a general comparator application, determine the following:

- Input voltage range
- Minimum overdrive voltage
- Output and drive current
- Response time

9.2.2.1 Input Voltage Range

When choosing the input voltage range, the input common-mode voltage range (V_{ICR}) must be taken in to account. If temperature operation is above or below 25°C the V_{ICR} can range from 0 V to $V_{CC}-2$ V. This limits the input voltage range to as high as $V_{CC}-2$ V and as low as 0 V. Operation outside of this range can yield incorrect comparisons.

The following list describes the outcomes of some input voltage situations.

- When both IN– and IN+ are both within the common-mode range:
 - If IN– is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
 - If IN– is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting
- When IN– is higher than common mode and IN+ is within common mode, the output is low and the output transistor is sinking current
- When IN+ is higher than common mode and IN– is within common mode, the output is high impedance and the output transistor is not conducting
- When IN– and IN+ are both higher than common mode, the output is low and the output transistor is sinking current

9.2.2.2 Minimum Overdrive Voltage

Overdrive voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage (V_{IO}). To make an accurate comparison, the overdrive voltage (V_{OD}) must be higher than the input offset voltage (V_{IO}). Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive. [Figure 8](#) and [Figure 9](#) show positive and negative response times with respect to overdrive voltage.

9.2.2.3 Output and Drive Current

Output current is determined by the load and pullup resistance and logic and pullup voltage. The output current produces a low-level output voltage (V_{OL}) from the comparator, where V_{OL} is proportional to the output current.

The output current can also effect the transient response.

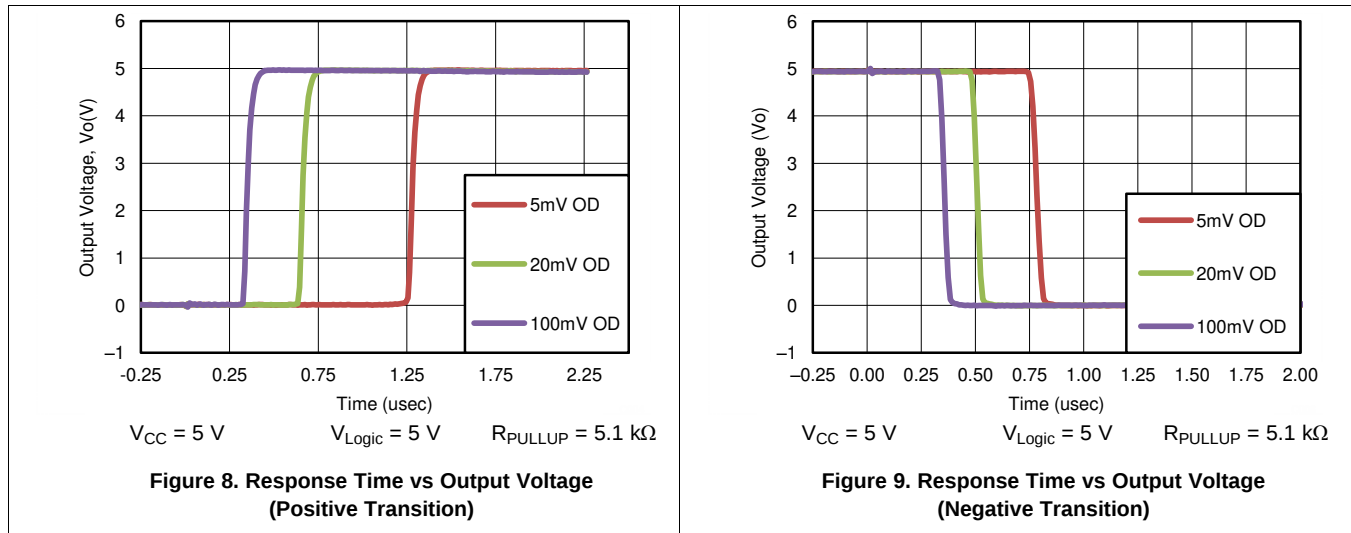
9.2.2.4 Response Time

Response time is a function of input over-drive. See the [Typical Characteristics](#) graphs for typical response times. The rise and fall times can be determined by the load capacitance (C_L), load/pull-up resistance (R_{PULLUP}) and equivalent collector-emitter resistance (R_{CE}).

- The rise time (τ_R) is approximately $\tau_R \sim R_{PULLUP} \times C_L$
- The fall time (τ_F) is approximately $\tau_F \sim R_{CE} \times C_L$
 - R_{CE} can be determined by taking the slope of [Figure 3](#) in its linear region at the desired temperature, or by dividing the V_{OL} by I_{OUT}

9.2.3 Application Curves

Figure 8 and Figure 9 were generated with scope probe parasitic capacitance of 50 pF.



10 Power Supply Recommendations

For fast response and comparison applications with noisy or AC inputs, use a bypass capacitor on the supply pin to reject any variation on the supply voltage. This variation can affect the common-mode range of the comparator input and create an inaccurate comparison.

11 Layout

11.1 Layout Guidelines

To create an accurate comparator application without hysteresis, maintain a stable power supply with minimized noise and glitches, which can affect the high level input common-mode voltage range. To achieve this accuracy, add a bypass capacitor between the supply voltage and ground. Place a bypass capacitor on the positive power supply and negative supply (if available).

NOTE

If a negative supply is not being used, do not place a capacitor between the GND pin of the device and system ground.

11.2 Layout Example

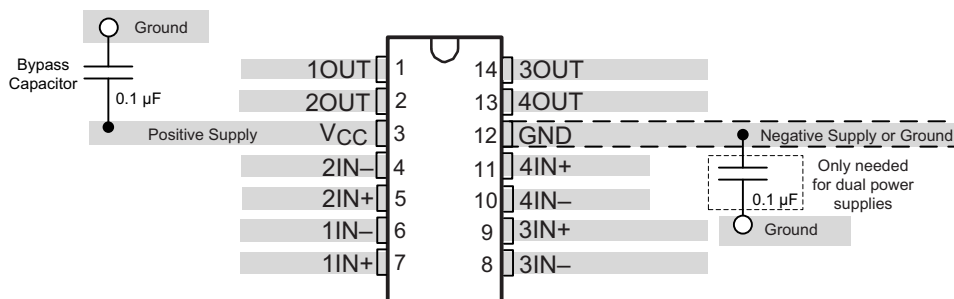


Figure 10. LMx39 Layout Example

12 器件和文档支持

12.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 2. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持和社区
LM139	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
LM239	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
LM339	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
LM139A	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
LM239A	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
LM339A	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
LM2901	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
LM2901AV	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
LM2901V	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.2 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](#) 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

TI E2E™ 在线社区 **TI 的工程师对工程师 (E2E) 社区。**此社区的创建目的在于促进工程师之间的协作。在 [e2e.ti.com](#) 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 **TI 参考设计支持** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 术语表

SLYZ022 — TI 术语表。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM139AD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM139A	Samples
LM139ADG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM139A	Samples
LM139ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM139A	Samples
LM139ADRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM139A	Samples
LM139D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM139	Samples
LM139DG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM139	Samples
LM139DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM139	Samples
LM139DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM139	Samples
LM239AD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM239A	Samples
LM239ADE4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM239A	Samples
LM239ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-25 to 85	LM239A	Samples
LM239ADRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM239A	Samples
LM239ADRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM239A	Samples
LM239D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM239	Samples
LM239DE4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM239	Samples
LM239DG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM239	Samples
LM239DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-25 to 85	LM239	Samples
LM239DRG3	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-25 to 85	LM239	Samples
LM239DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM239	Samples
LM239N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU SN	N / A for Pkg Type	-25 to 85	LM239N	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM239NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	LM239N	Samples
LM239PW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	L239	Samples
LM239PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-25 to 85	L239	Samples
LM239PWRE4	ACTIVE	TSSOP	PW	14	2000	TBD	Call TI	Call TI	-25 to 85		Samples
LM239PWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	L239	Samples
LM2901AVQDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2901AV	Samples
LM2901AVQDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2901AV	Samples
LM2901AVQPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2901AV	Samples
LM2901AVQPWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2901AV	Samples
LM2901D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2901	Samples
LM2901DE4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2901	Samples
LM2901DG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2901	Samples
LM2901DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LM2901	Samples
LM2901DRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2901	Samples
LM2901DRG3	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM2901	Samples
LM2901DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2901	Samples
LM2901N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	LM2901N	Samples
LM2901NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	LM2901N	Samples
LM2901NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2901	Samples
LM2901PW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2901	Samples
LM2901PWG4	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2901	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2901PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	L2901	Samples
LM2901PWRG3	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L2901	Samples
LM2901PWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2901	Samples
LM2901VQDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2901V	Samples
LM2901VQPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2901V	Samples
LM2901VQPWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2901V	Samples
LM339AD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339A	Samples
LM339ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L339A	Samples
LM339ADE4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339A	Samples
LM339ADG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339A	Samples
LM339ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	LM339A	Samples
LM339ADRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339A	Samples
LM339ADRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339A	Samples
LM339AN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU SN	N / A for Pkg Type	0 to 70	LM339AN	Samples
LM339ANE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM339AN	Samples
LM339ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339A	Samples
LM339ANSRG4	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339A	Samples
LM339APW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L339A	Samples
LM339APWG4	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L339A	Samples
LM339APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	L339A	Samples
LM339APWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L339A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM339D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339	Samples
LM339DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339	Samples
LM339DBRE4	ACTIVE	SSOP	DB	14	2000	TBD	Call TI	Call TI	0 to 70		Samples
LM339DE4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339	Samples
LM339DG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339	Samples
LM339DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	LM339	Samples
LM339DRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339	Samples
LM339DRG3	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	LM339	Samples
LM339DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339	Samples
LM339N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU SN	N / A for Pkg Type	0 to 70	LM339N	Samples
LM339NE3	ACTIVE	PDIP	N	14	25	RoHS & Non-Green	SN	N / A for Pkg Type	0 to 70	LM339N	Samples
LM339NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM339N	Samples
LM339NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339	Samples
LM339NSRG4	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM339	Samples
LM339PW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L339	Samples
LM339PWG4	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L339	Samples
LM339PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	L339	Samples
LM339PWRE4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L339	Samples
LM339PWRG3	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	L339	Samples
LM339PWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L339	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM139, LM239A, LM2901, LM2901AV, LM2901V :

- Automotive : [LM239A-Q1](#), [LM2901-Q1](#), [LM2901AV-Q1](#), [LM2901V-Q1](#)
- Enhanced Product : [LM239A-EP](#)
- Space : [LM139-SP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM139ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM139ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM139DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM139DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM239ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM239ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM239DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM239DR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
LM239DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM239DRG3	SOIC	D	14	2500	330.0	17.5	6.4	9.05	2.1	8.0	16.0	Q1
LM239DRG3	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
LM239DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM239DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM239PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM239PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM239PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2901AVQPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901AVQPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901DR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
LM2901DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2901DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2901DRG3	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
LM2901DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2901DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2901NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
LM2901PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901PWRG3	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901VQPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2901VQPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM339ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
LM339ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM339ADR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
LM339ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM339ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM339ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM339ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
LM339APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM339APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM339APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM339DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
LM339DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM339DR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
LM339DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM339DRG3	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
LM339DRG3	SOIC	D	14	2500	330.0	17.5	6.4	9.05	2.1	8.0	16.0	Q1
LM339DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM339DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM339NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
LM339PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM339PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM339PWRG3	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM339PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

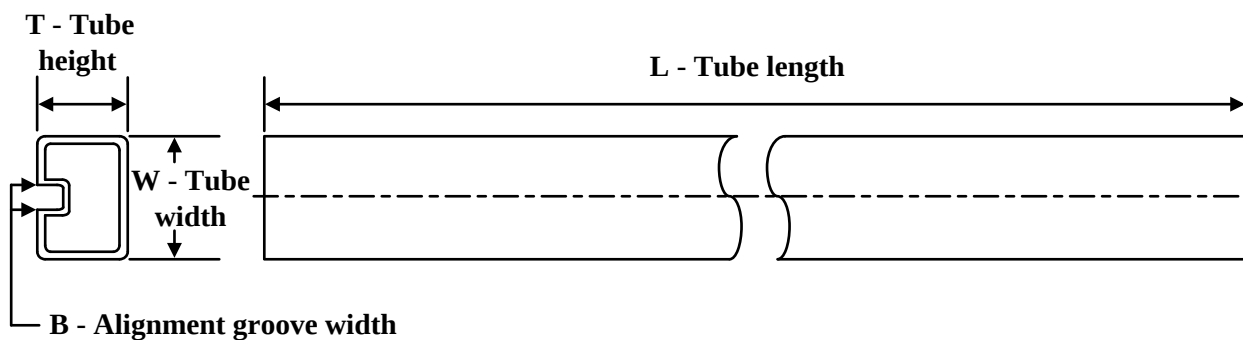
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM139ADR	SOIC	D	14	2500	350.0	350.0	43.0
LM139ADRG4	SOIC	D	14	2500	350.0	350.0	43.0
LM139DR	SOIC	D	14	2500	350.0	350.0	43.0
LM139DRG4	SOIC	D	14	2500	350.0	350.0	43.0
LM239ADR	SOIC	D	14	2500	356.0	356.0	35.0
LM239ADR	SOIC	D	14	2500	340.5	336.1	32.0
LM239DR	SOIC	D	14	2500	356.0	356.0	35.0
LM239DR	SOIC	D	14	2500	364.0	364.0	27.0
LM239DR	SOIC	D	14	2500	340.5	336.1	32.0
LM239DRG3	SOIC	D	14	2500	333.2	345.9	28.6
LM239DRG3	SOIC	D	14	2500	364.0	364.0	27.0
LM239DRG4	SOIC	D	14	2500	340.5	336.1	32.0
LM239DRG4	SOIC	D	14	2500	356.0	356.0	35.0
LM239PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM239PWR	TSSOP	PW	14	2000	364.0	364.0	27.0
LM239PWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
LM2901AVQPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM2901AVQPWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2901DR	SOIC	D	14	2500	364.0	364.0	27.0
LM2901DR	SOIC	D	14	2500	356.0	356.0	35.0
LM2901DR	SOIC	D	14	2500	340.5	336.1	32.0
LM2901DRG3	SOIC	D	14	2500	364.0	364.0	27.0
LM2901DRG4	SOIC	D	14	2500	340.5	336.1	32.0
LM2901DRG4	SOIC	D	14	2500	356.0	356.0	35.0
LM2901NSR	SO	NS	14	2000	356.0	356.0	35.0
LM2901PWR	TSSOP	PW	14	2000	364.0	364.0	27.0
LM2901PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM2901PWRG3	TSSOP	PW	14	2000	364.0	364.0	27.0
LM2901PWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
LM2901VQPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM2901VQPWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
LM339ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
LM339ADR	SOIC	D	14	2500	340.5	336.1	32.0
LM339ADR	SOIC	D	14	2500	364.0	364.0	27.0
LM339ADR	SOIC	D	14	2500	356.0	356.0	35.0
LM339ADRG4	SOIC	D	14	2500	340.5	336.1	32.0
LM339ADRG4	SOIC	D	14	2500	356.0	356.0	35.0
LM339ANSR	SO	NS	14	2000	356.0	356.0	35.0
LM339APWR	TSSOP	PW	14	2000	364.0	364.0	27.0
LM339APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM339APWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
LM339DBR	SSOP	DB	14	2000	356.0	356.0	35.0
LM339DR	SOIC	D	14	2500	340.5	336.1	32.0
LM339DR	SOIC	D	14	2500	364.0	364.0	27.0
LM339DR	SOIC	D	14	2500	356.0	356.0	35.0
LM339DRG3	SOIC	D	14	2500	364.0	364.0	27.0
LM339DRG3	SOIC	D	14	2500	333.2	345.9	28.6
LM339DRG4	SOIC	D	14	2500	356.0	356.0	35.0
LM339DRG4	SOIC	D	14	2500	340.5	336.1	32.0
LM339NSR	SO	NS	14	2000	356.0	356.0	35.0
LM339PWR	TSSOP	PW	14	2000	364.0	364.0	27.0
LM339PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM339PWRG3	TSSOP	PW	14	2000	364.0	364.0	27.0
LM339PWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LM139AD	D	SOIC	14	50	505.46	6.76	3810	4
LM139ADG4	D	SOIC	14	50	505.46	6.76	3810	4
LM139D	D	SOIC	14	50	505.46	6.76	3810	4
LM139DG4	D	SOIC	14	50	505.46	6.76	3810	4
LM239AD	D	SOIC	14	50	507	8	3940	4.32
LM239AD	D	SOIC	14	50	506.6	8	3940	4.32
LM239ADE4	D	SOIC	14	50	507	8	3940	4.32
LM239ADE4	D	SOIC	14	50	506.6	8	3940	4.32
LM239D	D	SOIC	14	50	506.6	8	3940	4.32
LM239D	D	SOIC	14	50	507	8	3940	4.32
LM239DE4	D	SOIC	14	50	507	8	3940	4.32
LM239DE4	D	SOIC	14	50	506.6	8	3940	4.32
LM239DG4	D	SOIC	14	50	506.6	8	3940	4.32
LM239DG4	D	SOIC	14	50	507	8	3940	4.32
LM239N	N	PDIP	14	25	506	13.97	11230	4.32
LM239N	N	PDIP	14	25	506.1	9	600	5.4
LM239NE4	N	PDIP	14	25	506.1	9	600	5.4
LM239NE4	N	PDIP	14	25	506	13.97	11230	4.32
LM239PW	PW	TSSOP	14	90	530	10.2	3600	3.5
LM2901D	D	SOIC	14	50	506.6	8	3940	4.32
LM2901DE4	D	SOIC	14	50	506.6	8	3940	4.32
LM2901DG4	D	SOIC	14	50	506.6	8	3940	4.32
LM2901N	N	PDIP	14	25	506	13.97	11230	4.32
LM2901NE4	N	PDIP	14	25	506	13.97	11230	4.32
LM2901PW	PW	TSSOP	14	90	530	10.2	3600	3.5
LM2901PWG4	PW	TSSOP	14	90	530	10.2	3600	3.5
LM339AD	D	SOIC	14	50	507	8	3940	4.32
LM339AD	D	SOIC	14	50	506.6	8	3940	4.32
LM339ADE4	D	SOIC	14	50	507	8	3940	4.32

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LM339ADE4	D	SOIC	14	50	506.6	8	3940	4.32
LM339ADG4	D	SOIC	14	50	507	8	3940	4.32
LM339ADG4	D	SOIC	14	50	506.6	8	3940	4.32
LM339AN	N	PDIP	14	25	506	13.97	11230	4.32
LM339AN	N	PDIP	14	25	506.1	9	600	5.4
LM339AN	N	PDIP	14	25	506	13.97	11230	4.32
LM339ANE4	N	PDIP	14	25	506	13.97	11230	4.32
LM339ANE4	N	PDIP	14	25	506	13.97	11230	4.32
LM339ANE4	N	PDIP	14	25	506.1	9	600	5.4
LM339APW	PW	TSSOP	14	90	530	10.2	3600	3.5
LM339APWG4	PW	TSSOP	14	90	530	10.2	3600	3.5
LM339D	D	SOIC	14	50	506.6	8	3940	4.32
LM339D	D	SOIC	14	50	507	8	3940	4.32
LM339DE4	D	SOIC	14	50	507	8	3940	4.32
LM339DE4	D	SOIC	14	50	506.6	8	3940	4.32
LM339DG4	D	SOIC	14	50	507	8	3940	4.32
LM339DG4	D	SOIC	14	50	506.6	8	3940	4.32
LM339N	N	PDIP	14	25	506	13.97	11230	4.32
LM339N	N	PDIP	14	25	506	13.97	11230	4.32
LM339N	N	PDIP	14	25	506.1	9	600	5.4
LM339NE3	N	PDIP	14	25	506.1	9	600	5.4
LM339NE4	N	PDIP	14	25	506	13.97	11230	4.32
LM339NE4	N	PDIP	14	25	506	13.97	11230	4.32
LM339PW	PW	TSSOP	14	90	530	10.2	3600	3.5
LM339PWG4	PW	TSSOP	14	90	530	10.2	3600	3.5

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

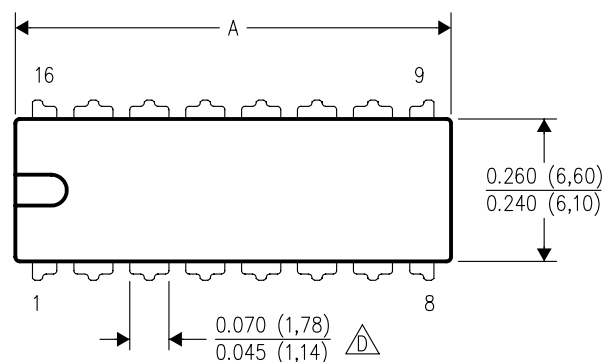


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

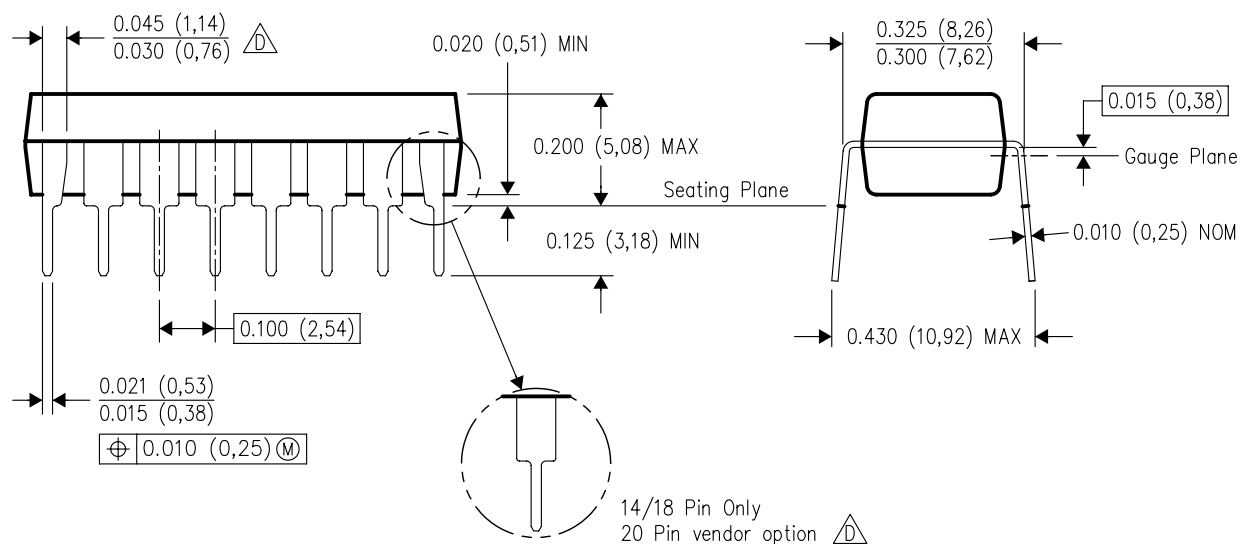
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



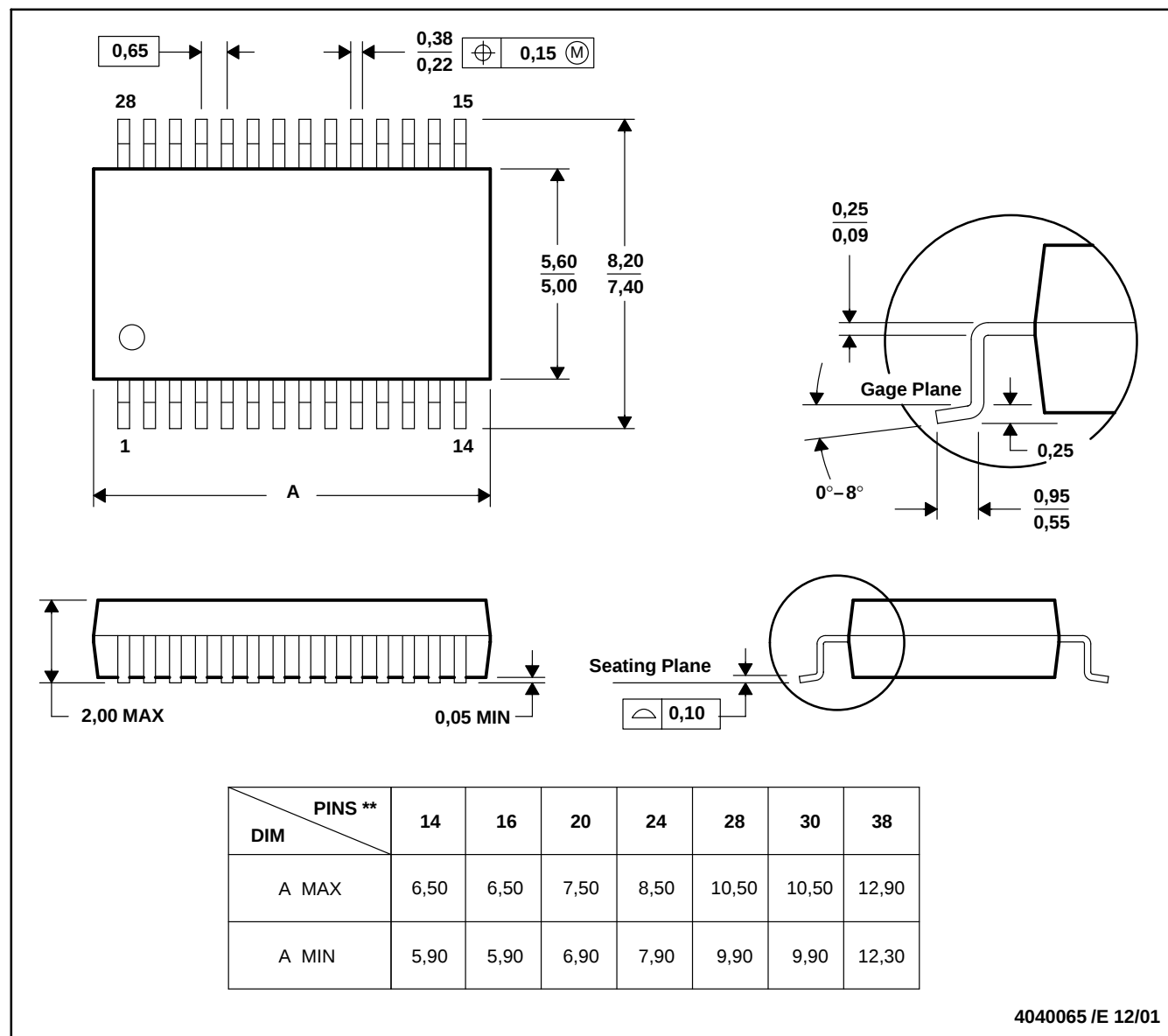
4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

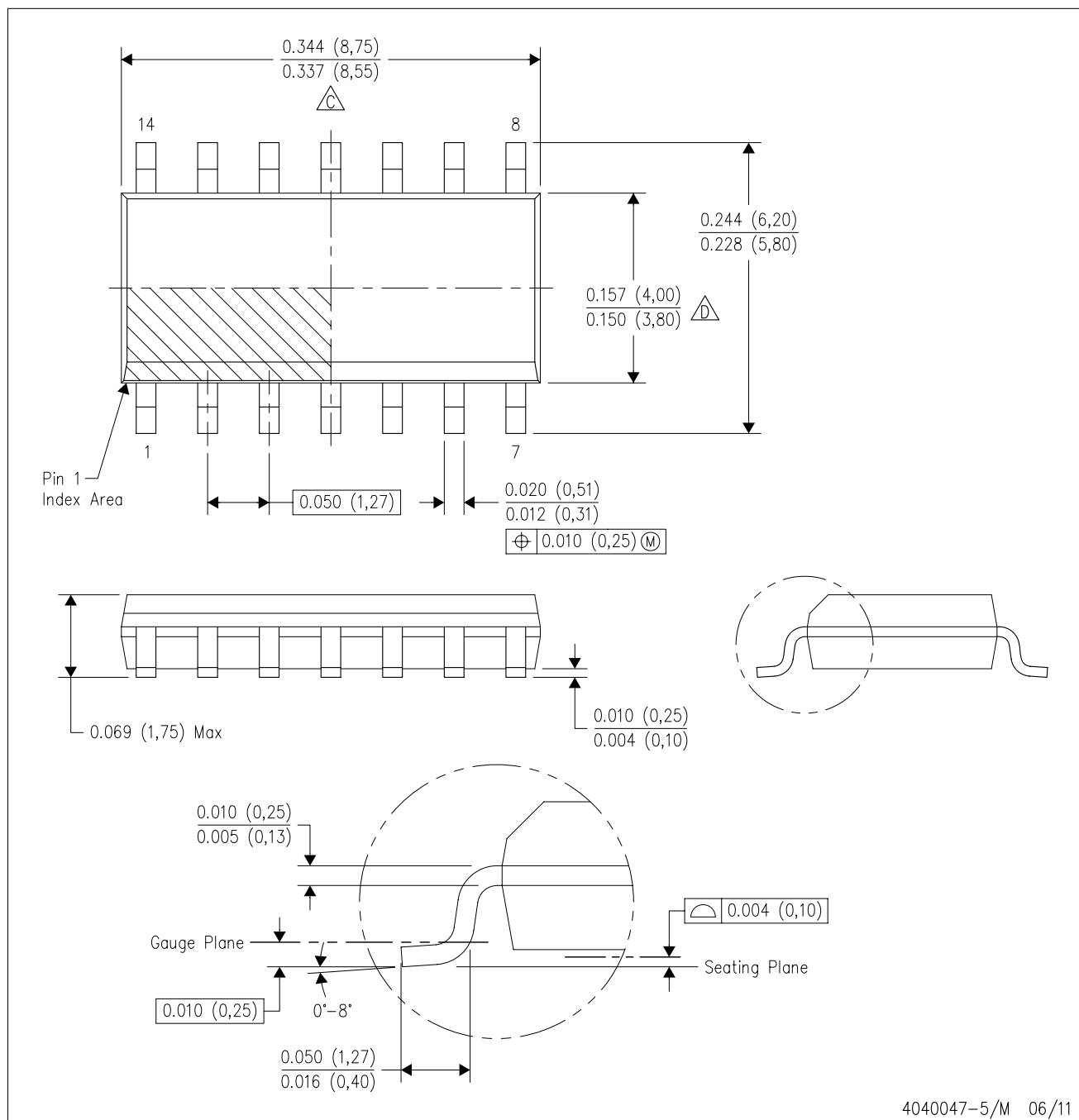
28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

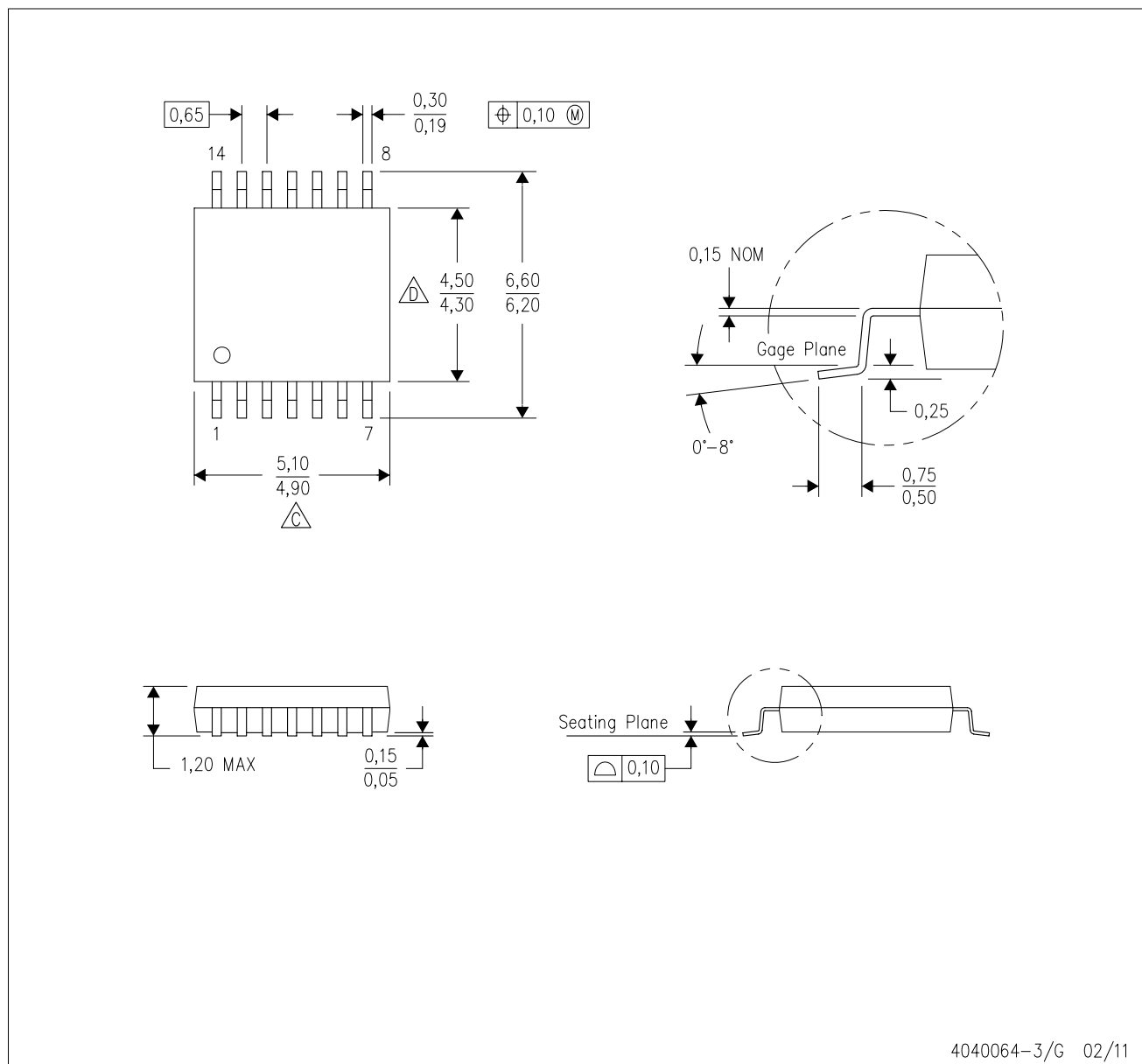
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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