

LM2904-Q1、LM2904B-Q1 和 LM2904BA-Q1 适用于汽车应用的行业标准双路运算放大器

1 特性

- 符合面向汽车应用的 AEC Q-100 标准
 - 温度等级 1：-40°C 至 +125°C
 - 器件 HBM ESD 分类等级 2
 - 器件 CDM ESD 分类等级 C5
- 3V 至 36V 的宽电源电压范围 (LM2904B-Q1 和 LM2904BA-Q1)
- 每通道电源电流为 300 μA (LM2904B-Q1 和 LM2904BA-Q1, 典型值)
- 单位增益带宽为 1.2 MHz (LM2904B-Q1 和 LM2904BA-Q1)
- 共模输入电压范围包括接地, 支持近地直接感测
- 低输入失调电压在 25°C 时为 2mV (LM2904BA-Q1, 最大值)
- 低输入失调电压在 25°C 时为 3mV (LM2904B-Q1, 最大值)
- 内部射频和 EMI 滤波器 (LM2904B-Q1 和 LM2904BA-Q1)
- 提供功能安全
 - 有助于进行功能安全系统设计的文档

2 应用

- 汽车照明
- 车身电子装置
- 汽车音响主机
- 远程信息处理控制单元
- 紧急呼叫 (eCall)
- 被动安全：制动系统
- 电动汽车/混合动力电动汽车：
 - 逆变器和电机控制
 - 车载充电器 (OBC) 和无线充电器
 - 电池管理系统 (BMS)

3 说明

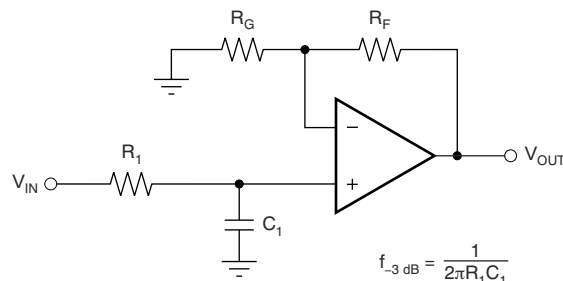
LM2904-Q1、LM2904B-Q1 和 LM2904BA-Q1 是符合 AEC-Q100 规范的业界通用运算放大器, 适合汽车应用。LM2904B-Q1 和 LM2904BA-Q1 是 LM2904-Q1 的下一代版本, 包含两个高电压 (36V) 运算放大器。LM2904B-Q1 和 LM2904BA-Q1 为成本敏感型应用提供了卓越的价值, 其特性包括低失调电压 (最大值分别为 3mV 和 2mV)、对地共模输入范围和高差分输入电压能力。

LM2904B-Q1 和 LM2904BA-Q1 利用单位增益稳定性、更低的失调电压 (0.3mV, 典型值) 和更低的静态电流 (300μA, 典型值) 等增强型特性简化了电路设计。得益于高 ESD (2kV, HBM) 及集成 EMI 和射频滤波器, LM2904B-Q1 和 LM2904BA-Q1 器件可用于汽车市场中要求最为严苛、极具环境挑战性的应用。

器件信息

器件型号 ⁽¹⁾	封装	封装尺寸 (标称值)
LM2904B-Q1	SOIC (8)	4.90mm × 3.90mm
	TSSOP (8)	3.00mm × 4.40mm
	VSSOP (8)	3.00mm × 3.00mm
LM2904BA-Q1	SOIC (8)	4.90mm × 3.90mm
	TSSOP (8)	3.00mm × 4.40mm
	VSSOP (8)	3.00mm × 3.00mm
LM2904-Q1	SOIC (8)	4.90mm × 3.90mm
	TSSOP (8)	3.00mm × 4.40mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。



$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \left(1 + \frac{R_F}{R_G}\right) \left(\frac{1}{1 + sR_1 C_1}\right)$$

单极低通滤波器



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision J (February 2021) to Revision K (April 2022)	Page
• 向数据表中添加了 LM2904BA-Q1.....	1
• Increased ESD (CDM) rating for LM2904B-Q1 and LM2904BA-Q1 from ± 750 V to ± 1500 V.....	6

Changes from Revision I (June 2020) to Revision J (February 2021)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• 向 <i>特性</i> 部分添加了“提供功能安全”特性和指向支持文档的链接.....	1
• 删除了整个数据表中 VSSOP (8) 封装的预发布标签.....	1
• 删除了整个数据表中的 SOT-23 (8) 封装信息.....	1
• Deleted preview tag from VSSOP package in <i>Pin Configuration and Functions</i> section.....	5
• Deleted DDF (SOT23-8) package in <i>Pin Configuration and Functions</i> section.....	5
• Updated VSSOP package thermal information in <i>Thermal Information</i> section.....	7

Changes from Revision H (December 2019) to Revision I (June 2020)	Page
• 在 <i>应用</i> 部分中添加了应用链接.....	1
• 删除了 <i>器件信息</i> 表中 TSSOP (8) 封装的预发布标签.....	1
• 向 <i>器件信息</i> 表添加了 VSSOP-8 封装信息.....	1
• Added information on VSSOP-8 package to the <i>Device Comparison Table</i> section.....	4
• Deleted preview tag on TSSOP-8 package in the <i>Device Comparison Table</i> section.....	4
• Deleted preview tag from TSSOP package in <i>Pin Configuration and Functions</i> section.....	5
• Added VSSOP package information in <i>Pin Configuration and Functions</i> section.....	5
• Added VSSOP package to <i>Thermal Information</i> table	7
• Changed section title from <i>Community Resources</i> to <i>Support Resources</i> in the <i>Device and Documentation Support</i> section.....	25

Changes from Revision G (February 2019) to Revision H (December 2019)

Page

• 向器件信息表添加了 SOT23-8 封装信息.....	1
• Added information on SOT23-8 package to the <i>Device Comparison Table</i>	4
• Added the <i>Typical Characteristics</i> section for the LM2904B-Q1 device.....	11
• Added test circuit for THD+N and small-signal step response, $G = -1$ in the <i>Parameter Measurement Information</i> section.....	18
• Changed specific voltages to a <i>Recommended Operating Conditions</i> reference.....	19
• Changed the functional block diagram for LM2904B-Q1 in the <i>Detailed Description</i> section.....	19

Changes from Revision F (April 2008) to Revision G (February 2019)

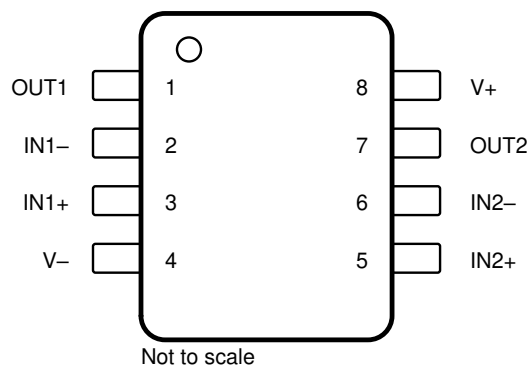
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• 添加了应用部分、ESD 等级表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分.....	1
• 向数据表添加了新器件.....	1
• 添加了语句“通过 AEC-Q100 认证”	1

5 Device Comparison Table

PART NUMBER	SUPPLY VOLTAGE	AMBIENT TEMPERATURE RANGE	V_{OS} (MAXIMUM AT 25°C)	I_Q / CH (TYPICAL AT 25°C)	INTEGRATED EMI FILTER	PACKAGE
LM2904B-Q1	3 V to 36 V	– 40°C to 125°C	3 mV	300 μ A	Yes	D, DGK, PW
LM2904BA-Q1	3 V to 36 V	– 40°C to 125°C	2 mV	300 μ A	Yes	D, DGK, PW
LM2904-Q1	3 V to 26 V	– 40°C to 125°C	7 mV	350 μ A	No	D, PW
LM2904V-Q1	3 V to 32 V	– 40°C to 125°C	7 mV	350 μ A	No	D, PW
LM2904AV-Q1	3 V to 32 V	– 40°C to 125°C	2 mV	350 μ A	No	D, PW

6 Pin Configuration and Functions



**图 6-1. D, DGK, and PW Package
8-Pin SOIC, VSSOP, and TSSOP
Top View**

表 6-1. Pin Functions

PIN ⁽¹⁾		I/O	DESCRIPTION
NAME	NO.		
IN1 -	2	I	Negative input
IN1+	3	I	Positive input
IN2 -	6	I	Negative input
IN2+	5	I	Positive input
OUT1	1	O	Output
OUT2	7	O	Output
V -	4	—	Negative (lowest) supply or ground (for single-supply operation)
V+	8	—	Positive (highest) supply

(1) For a listing of which devices are available in what packages, see [节 5](#).

7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
Supply voltage, V _S = ([V+] - [V-])		LM2904B-Q1, LM2904BA-Q1	40		V
		LM2904V-Q1, LM2904AV-Q1	32		
		LM2904-Q1	26		
Differential input voltage, V _{ID} ⁽²⁾		LM2904B-Q1, LM290BA-Q1, LM2904V-Q1, LM2904AV-Q1	- 32	32	V
		LM2904-Q1	- 26	26	
Input voltage, V _I	Either input	LM2904B-Q1, LM2904BA-Q1	- 0.3	40	V
		LM2904V-Q1, LM2904AV-Q1	- 0.3	32	
		LM2904-Q1	- 0.3	26	
Duration of output short circuit (one amplifier) to V ₋ at (or below) T _A = 25°C, V _S ≤ 15 V ⁽³⁾			Unlimited		s
Operating ambient temperature, T _A			- 40	125	°C
Operating virtual-junction temperature, T _J				150	°C
Storage temperature, T _{stg}			- 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Differential voltages are at $IN+$, with respect to $IN-$.

(3) Short circuits from outputs to the supply pins can cause excessive heating and eventual destruction.

7.2 ESD Ratings

		VALUE	UNIT	
LM2904B-Q1 and LM2904BA-Q1				
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	
LM2904-Q1, LM2904AV-Q1, AND LM2904V-Q1				
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±1000	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V _S	Supply voltage, V _S = ([V+] - [V-])	LM2904B-Q1, LM2904BA-Q1	3	36	V
		LM2904AV-Q1, LM2904V-Q1	3	30	
		LM2904-Q1	3	26	
V _{CM}	Common-mode voltage	V -	(V+) - 2	V	
T _A	Operating ambient temperature	- 40	125	°C	

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LM2904-Q1, LM2904AV-Q1, LM2904B-Q1, LM2904BA-Q1, LM2904V-Q1 ⁽²⁾			UNIT
		D (SOIC)	DGK (VSSOP)	PW (TSSOP)	
		8 PINS	8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	124.7	186.1	171.7	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	66.9	77.1	68.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	67.9	107.7	99.2	°C/W
ψ _{JT}	Junction-to-top characterization parameter	19.2	17.2	11.5	°C/W
ψ _{JB}	Junction-to-board characterization parameter	67.2	106.1	97.9	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

(2) For a listing of which devices are available in what packages, see [节 5](#).

7.5 Electrical Characteristics: LM2904B-Q1 and LM2904BA-Q1

$V_S = (V+) - (V-) = 5\text{ V} - 36\text{ V} (\pm 2.5\text{ V} - \pm 18\text{ V})$, $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S / 2$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V _{OS}	Input offset voltage	LM2904B-Q1			±0.3	±3.0	mV
				T _A = - 40°C to +125°C		±4	
		LM2904BA-Q1				±2.0	mV
				T _A = - 40°C to +125°C		±3.0	mV
dV _{OS} /dT	Input offset voltage drift			T _A = - 40°C to +125°C ⁽¹⁾	±3.5	12	µV/°C
PSRR	Power supply rejection ratio				±2	15	µV/V
	Channel separation, dc	f = 1 kHz to 20 kHz			±1		µV/V
INPUT VOLTAGE RANGE							
V _{CM}	Common-mode voltage range	V _S = 3 V to 36 V			(V -)	(V+) - 1.5	V
		V _S = 5 V to 36 V		T _A = - 40°C to +125°C	(V -)	(V+) - 2	
CMRR	Common-mode rejection ratio	(V -) ≤ V _{CM} ≤ (V+) - 1.5 V	V _S = 3 V to 36 V		20	100	µV/V
		(V -) ≤ V _{CM} ≤ (V+) - 2.0 V	V _S = 5 V to 36 V	T _A = - 40°C to +125°C	25	316	
INPUT BIAS CURRENT							
I _B	Input bias current				±10	±35	nA
				T _A = - 40°C to +125°C ⁽¹⁾		±50	
I _{OS}	Input offset current				0.5	4	nA
				T _A = - 40°C to +125°C ⁽¹⁾		5	
dI _{OS} /dT	Input offset current drift			T _A = - 40°C to +125°C	10		pA/°C
NOISE							
E _n	Input voltage noise	f = 0.1 to 10 Hz			3		µV _{PP}
e _n	Input voltage noise density	f = 1 kHz			40		nV/√/Hz
INPUT IMPEDANCE							
Z _{ID}	Differential				10 0.1		M Ω pF
Z _{IC}	Common-mode				4 1.5		G Ω pF
OPEN-LOOP GAIN							
A _{OL}	Open-loop voltage gain	V _S = 15 V; V _O = 1 V to 11 V; R _L ≥ 10 kΩ, connected to (V-)			70	140	V/mV
				T _A = - 40°C to +125°C	35		
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				1.2		MHz
SR	Slew rate	G = + 1			0.5		V/µs
ϕ _m	Phase margin	G = + 1, R _L = 10 k Ω , C _L = 20 pF			56		°
t _{OR}	Overload recovery time	V _{IN} × gain > V _S			10		µs
t _s	Settling time	To 0.1%, V _S = 5 V, 2-V Step , G = +1, C _L = 100 pF			4		µs
THD+N	Total harmonic distortion + noise	G = + 1, f = 1 kHz, V _O = 3.53 V _{RMS} , V _S = 36 V, R _L = 100k, I _{OUT} ≤ ±50 µA, BW = 80 kHz			0.001%		
OUTPUT							
V _O	Voltage output swing from rail	Positive rail (V+)		I _{OUT} = 50 µA	1.35	1.42	V
				I _{OUT} = 1 mA	1.4	1.48	
				I _{OUT} = 5 mA ⁽¹⁾	1.5	1.61	
		Negative rail (V-)		I _{OUT} = 50 µA	100	150	mV
				I _{OUT} = 1 mA	0.75	1	V
				V _S = 5 V, R _L ≤ 10 kΩ connected to (V -)	T _A = - 40°C to +125°C	5	20
I _O	Output current	V _S = 15 V; V _O = V-; V _{ID} = 1 V	Source ⁽¹⁾		-20	-30	mA
			T _A = - 40°C to +125°C	-10			
		V _S = 15 V; V _O = V+; V _{ID} = -1 V	Sink ⁽¹⁾		10	20	
			T _A = - 40°C to +125°C	5			
		V _{ID} = -1 V; V _O = (V-) + 200 mV			60	100	µ A
I _{SC}	Short-circuit current	V _S = 20 V, (V+) = 10 V, (V-) = -10 V, V _O = 0 V			±40	±60	mA
C _{LOAD}	Capacitive load drive				100		pF

7.5 Electrical Characteristics: LM2904B-Q1 and LM2904BA-Q1 (continued)

$V_S = (V_+) - (V_-) = 5\text{ V} - 36\text{ V} (\pm 2.5\text{ V} - \pm 18\text{ V})$, $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S / 2$, $R_L = 10\text{k}$ connected to $V_S / 2$
(unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
R _O	Open-loop output resistance	f = 1 MHz, I _O = 0 A			300		Ω
POWER SUPPLY							
I _Q	Quiescent current per amplifier	V _S = 5 V; I _O = 0 A	T _A = - 40°C to +125°C		300	460	μA
		V _S = 36 V; I _O = 0 A			800		

(1) Specified by characterization only.

7.6 Electrical Characteristics: LM2904-Q1, LM2904AV-Q1, LM2904V-Q1

For $V_S = (V_+) - (V_-) = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to V_- (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V _{OS}	Input offset voltage	V _S = 5 V to maximum; V _{C M} = 0 V; V _O = 1.4 V	LM2904-Q1, LM2904V-A1		±3	±7	mV
				T _A = - 40°C to 125°C		±10	
			LM2904AV-Q1		±1	±2	
				T _A = - 40°C to 125°C		±4	
dV _{OS} /dT	Input offset voltage drift		T _A = - 40°C to 125°C		±7		µV/°C
PSRR	Input offset voltage vs power supply (Δ V _{IO} / Δ V _S)	V _S = 5 V to 30 V		65	100		dB
V _{O1} / V _{O2}	Channel separation	f = 1 kHz to 20 kHz			120		dB
INPUT VOLTAGE RANGE							
V _{CM}	Common-mode voltage range	V _S = 5 V to maximum		(V -)	(V+) - 1.5		V
			T _A = - 40°C to 125°C	(V -)	(V+) - 2		
CMRR	Common-mode rejection ratio	V _S = 5 V to maximum; V _{CM} = 0 V		65	80		dB
INPUT BIAS CURRENT							
I _B	Input bias current	V _O = (V -) + 1.4 V			- 20	- 250	nA
				T _A = - 40°C to 125°C		- 500	
I _{OS}	Input offset current	V _O = (V -) + 1.4 V	LM2904-Q1		2	50	nA
				T _A = - 40°C to 125°C		300	
			LM2904AV-Q1, LM2904V-Q1		2	50	
				T _A = - 40°C to 125°C		150	
dI _{OS} /dT	Input offset current drift		T _A = - 40°C to 125°C		10		pA/°C
NOISE							
e _n	Input voltage noise density	f = 1 kHz			40		nV/ √ Hz
OPEN-LOOP GAIN							
A _{OL}	Open-loop voltage gain	V _S = 15 V; V _O = (V -) + 1 V to (V -) + 11 V; R _L ≥ 2 k Ω , connected to (V -)		25	100		V/mV
			T _A = - 40°C to 125°C	15			
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				0.7		MHz
SR	Slew rate	G = +1			0.3		V/µs
OUTPUT							
V _O	Voltage output swing from rail	Positive rail	R _L ≥ 10 k Ω		V _S - 1.5		V
			LM2904-Q1	V _S = maximum; R _L = 2 k Ω		4	
				V _S = maximum; R _L ≥ 10 k Ω	T _A = - 40°C to 125°C	3	
			LM2904AV-Q1, LM2904V-Q1	V _S = maximum; R _L = 2 k Ω		6	
				V _S = maximum; R _L ≥ 10 k Ω		5	
		Negative rail	V _S = 5 V; R _L ≤ 10 k Ω	T _A = - 40°C to 125°C	5	20	mV
		I _O	Output current	V _S = 15 V; V _O = V - ; V _{ID} = 1 V	Source		- 20
	T _A = - 40°C to 125°C				- 10		
V _S = 15 V; V _O = V+; V _{ID} = - 1 V	Sink				10	20	
				T _A = - 40°C to 125°C	5		
V _{ID} = - 1 V; V _O = (V -) + 200 mV	LM2904-Q1				30		µA
	LM2904AV-Q1, LM2904V-Q1		12	40			
I _{SC}	Short-circuit current	V _S = 10 V; V _O = V _S / 2			±40	±60	mA
POWER SUPPLY							
I _Q	Quiescent current per amplifier	V _O = V _S / 2; I _O = 0 A	T _A = - 40°C to 125°C		350	600	µA
		V _S = maximum; V _O = maximum / 2; I _O = 0 A			500	1000	

- (1) All characteristics are measured with zero common-mode input voltage, unless otherwise specified. Maximum V_S for testing purposes is 26 V for LM2904-Q1 and 32 V for LM2904AV-Q1/LM2904V-Q1.

7.7 Typical Characteristics

Typical characteristics section is applicable for LM2904B-Q1 and LM2904BA-Q1. The typical characteristics data section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V}$ ($\pm 18\text{ V}$), $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).

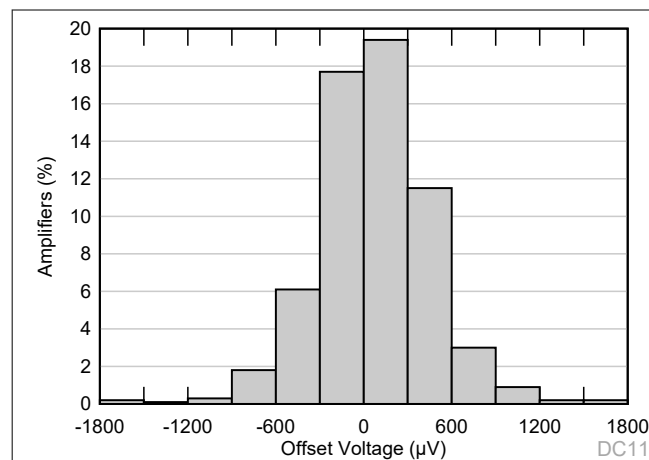


图 7-1. Offset Voltage Production Distribution

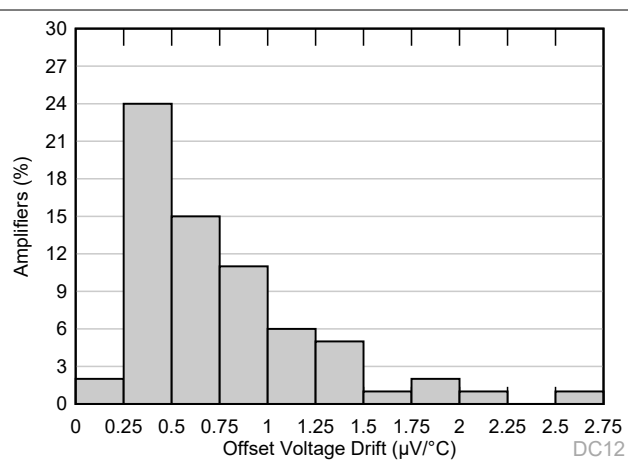


图 7-2. Offset Voltage Drift Distribution

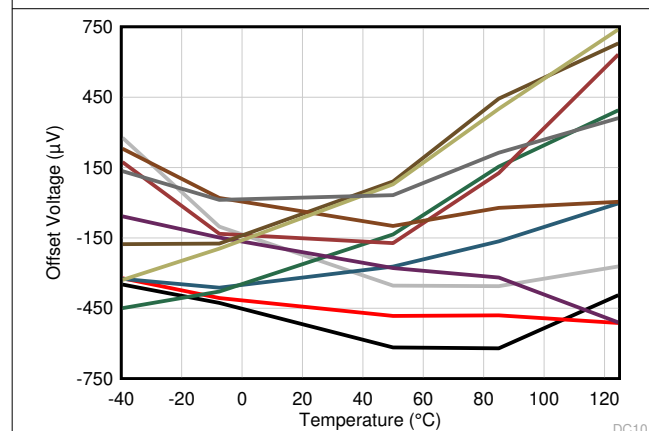


图 7-3. Offset Voltage vs Temperature

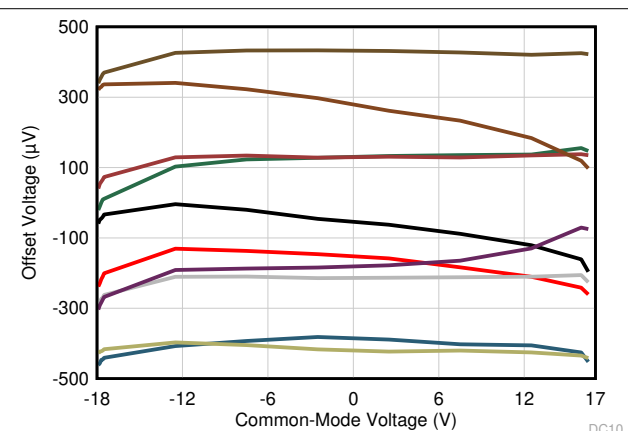


图 7-4. Offset Voltage vs Common-Mode Voltage

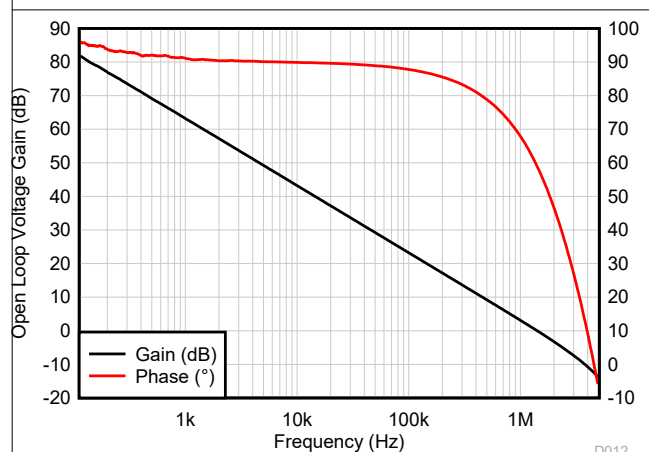


图 7-5. Open-Loop Gain and Phase vs Frequency

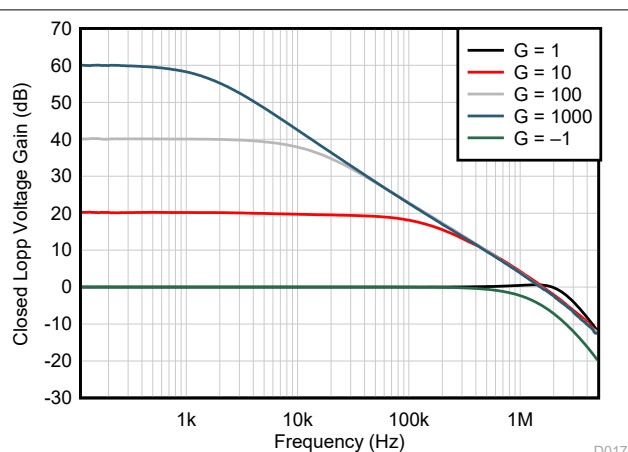


图 7-6. Closed-Loop Gain vs Frequency

7.7 Typical Characteristics (continued)

Typical characteristics section is applicable for LM2904B-Q1 and LM2904BA-Q1. The typical characteristics data section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V}$ ($\pm 18\text{ V}$), $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).

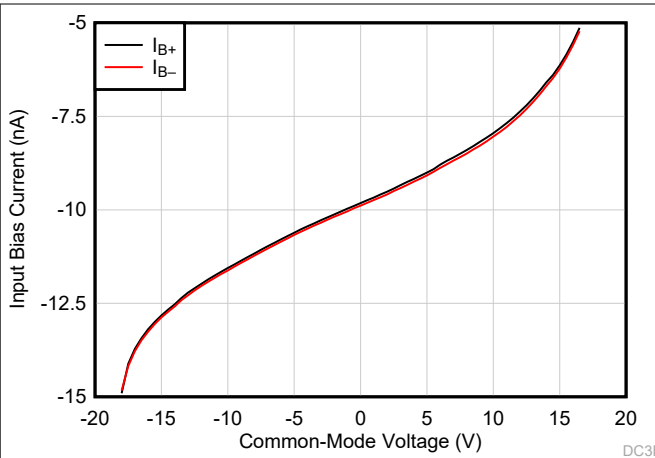


图 7-7. Input Bias Current vs Common-Mode Voltage

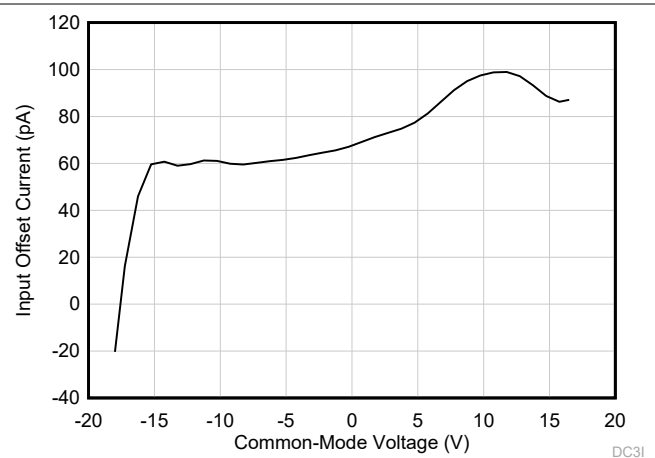


图 7-8. Input Offset Current vs Common-Mode Voltage

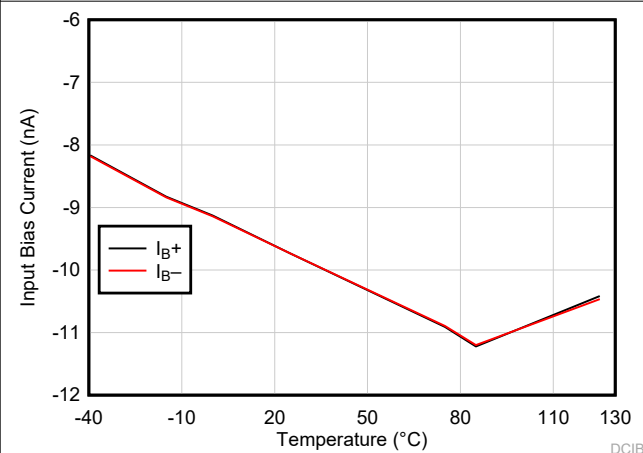


图 7-9. Input Bias Current vs Temperature

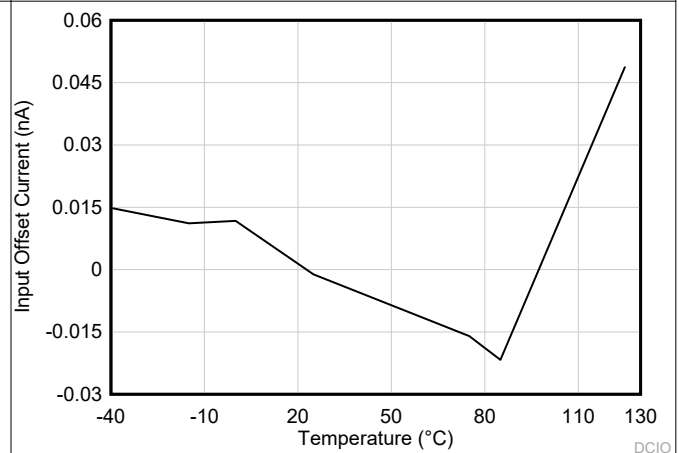


图 7-10. Input Offset Current vs Temperature

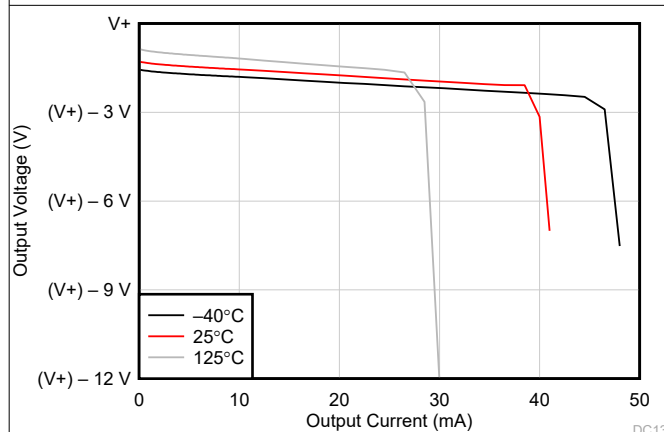


图 7-11. Output Voltage Swing vs Output Current (Sourcing)

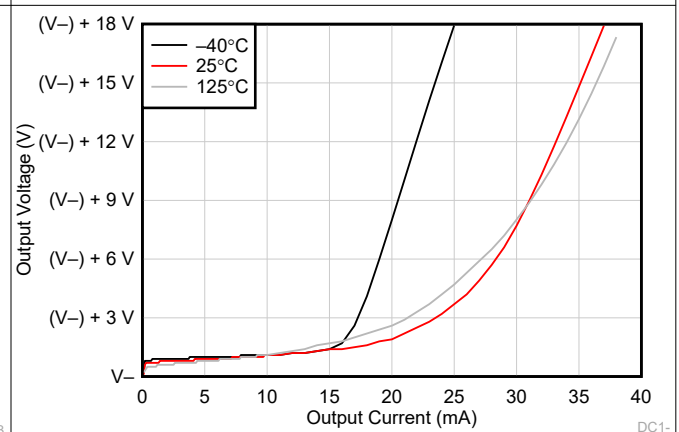


图 7-12. Output Voltage Swing vs Output Current (Sinking)

7.7 Typical Characteristics (continued)

Typical characteristics section is applicable for LM2904B-Q1 and LM2904BA-Q1. The typical characteristics data section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V}$ ($\pm 18\text{ V}$), $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).

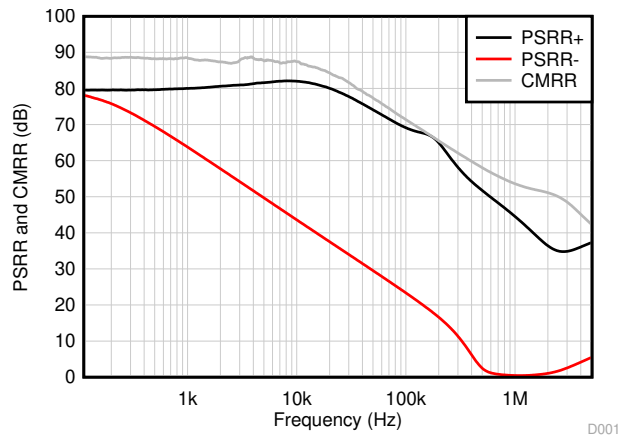


图 7-13. CMRR and PSRR vs Frequency

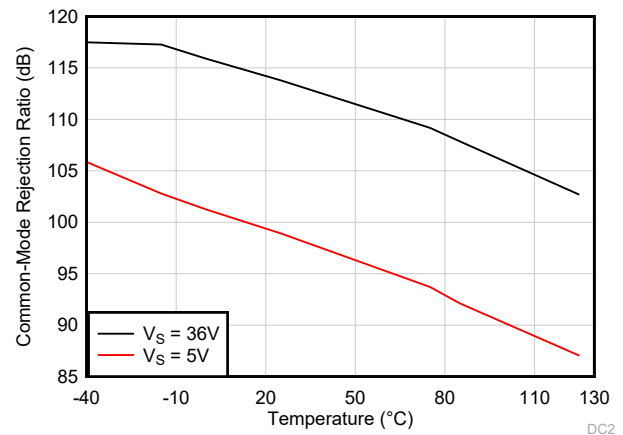


图 7-14. Common-Mode Rejection Ratio vs Temperature (dB)

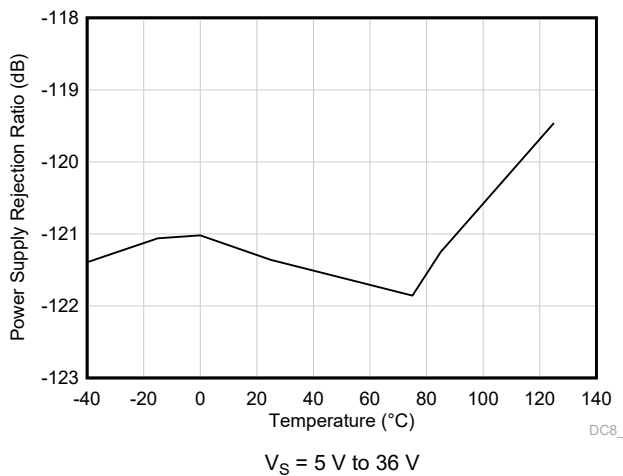


图 7-15. Power Supply Rejection Ratio vs Temperature (dB)

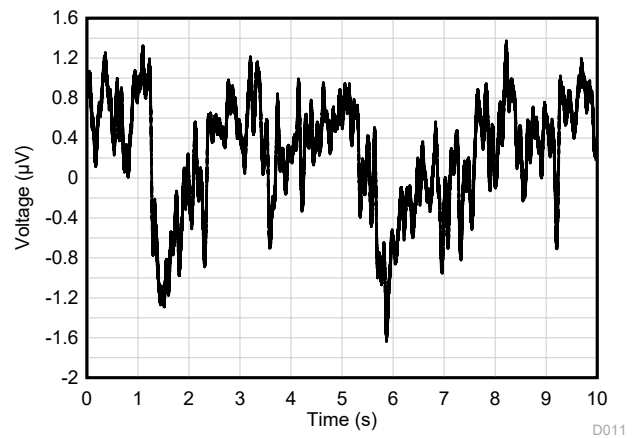


图 7-16. 0.1-Hz to 10-Hz Noise

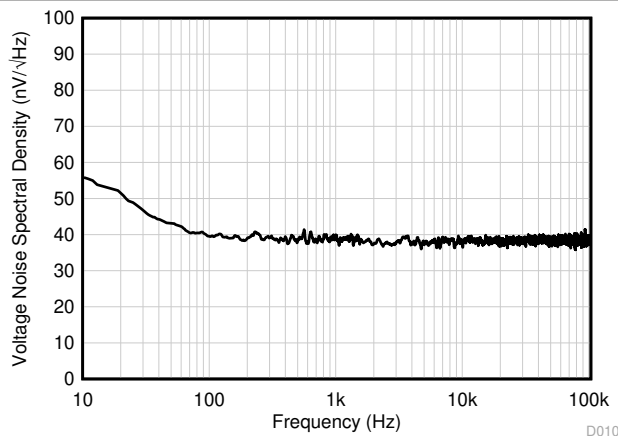
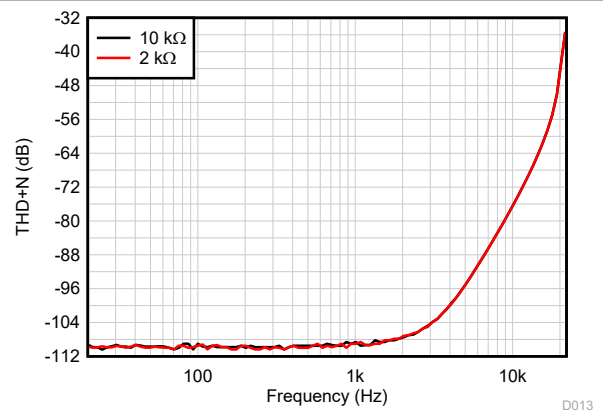


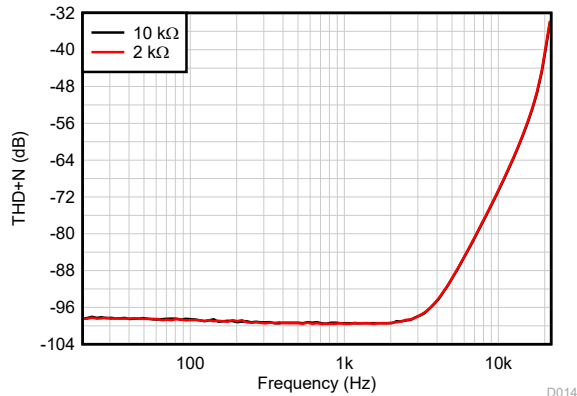
图 7-17. Input Voltage Noise Spectral Density vs Frequency



$G = 1$, $f = 1\text{ kHz}$, $BW = 80\text{ kHz}$,
 $V_{OUT} = 10\text{ V}_{PP}$, R_L connected to V_-
图 7-18. THD+N Ratio vs Frequency, $G = 1$

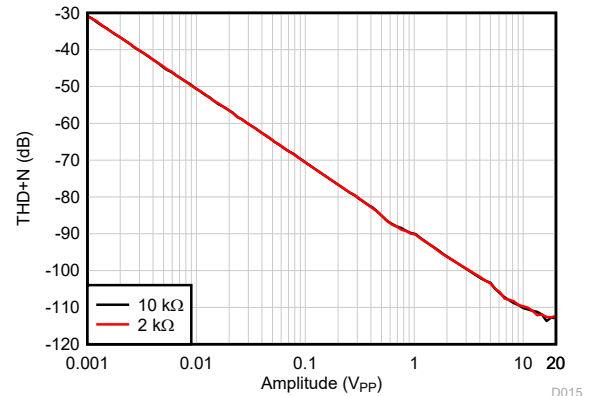
7.7 Typical Characteristics (continued)

Typical characteristics section is applicable for LM2904B-Q1 and LM2904BA-Q1. The typical characteristics data section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V}$ ($\pm 18\text{ V}$), $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).



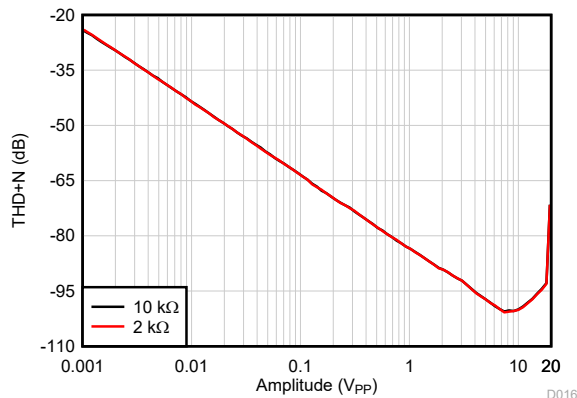
$G = -1$, $f = 1\text{ kHz}$, $BW = 80\text{ kHz}$,
 $V_{OUT} = 10\text{ V}_{PP}$, R_L connected to V_-
See 图 8-3

图 7-19. THD+N Ratio vs Frequency, $G = -1$



$G = 1$, $f = 1\text{ kHz}$, $BW = 80\text{ kHz}$,
 R_L connected to V_-

图 7-20. THD+N vs Output Amplitude, $G = 1$



$G = -1$, $f = 1\text{ kHz}$, $BW = 80\text{ kHz}$,
 R_L connected to V_-
See 图 8-3

图 7-21. THD+N vs Output Amplitude, $G = -1$

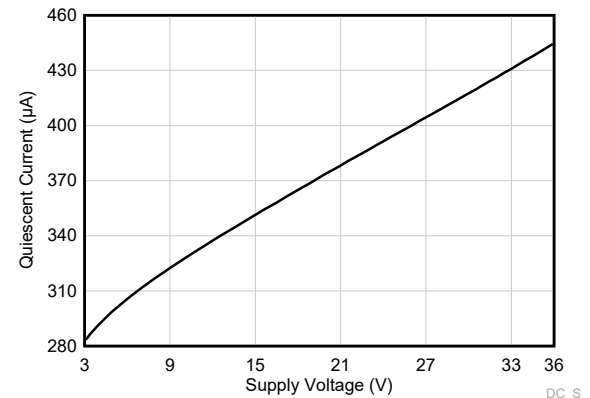


图 7-22. Quiescent Current vs Supply Voltage

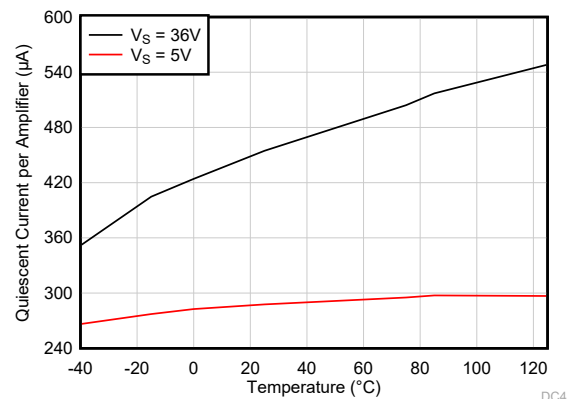


图 7-23. Quiescent Current vs Temperature

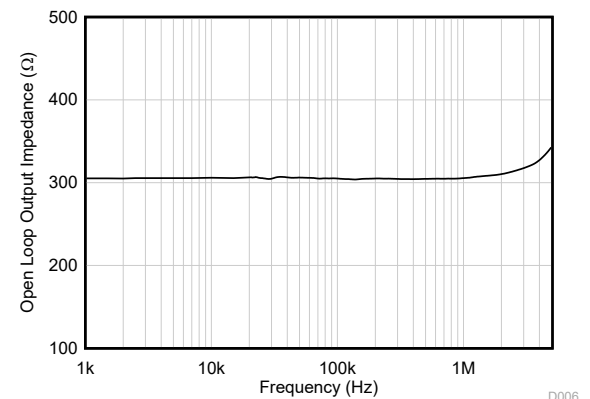


图 7-24. Open-Loop Output Impedance vs Frequency

7.7 Typical Characteristics (continued)

Typical characteristics section is applicable for LM2904B-Q1 and LM2904BA-Q1. The typical characteristics data section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V}$ ($\pm 18\text{ V}$), $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).

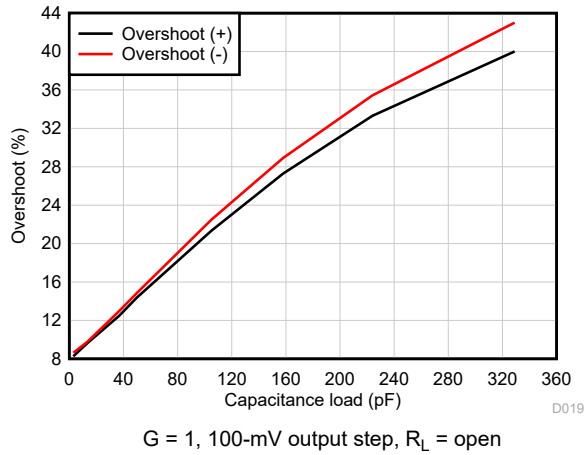


图 7-25. Small-Signal Overshoot vs Capacitive Load

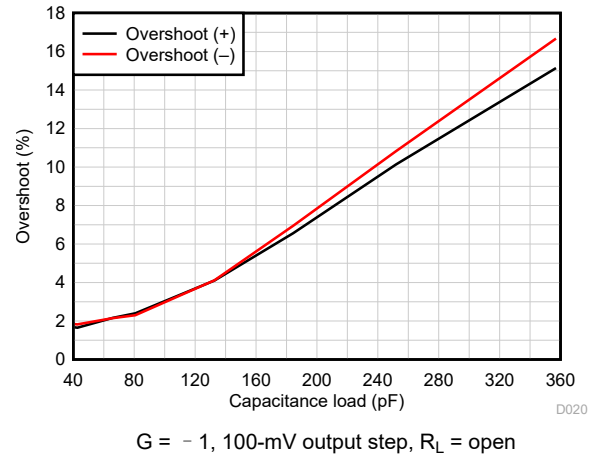


图 7-26. Small-Signal Overshoot vs Capacitive Load

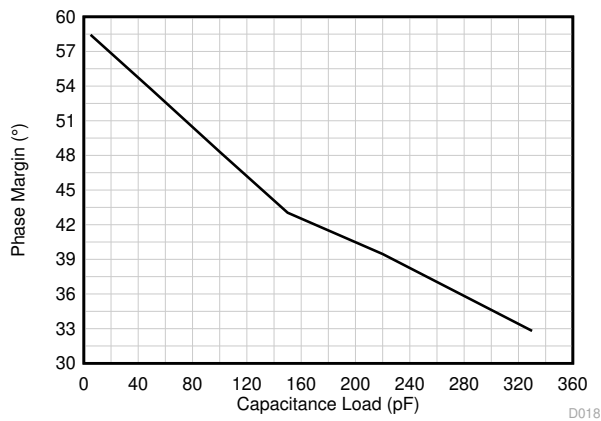


图 7-27. Phase Margin vs Capacitive Load

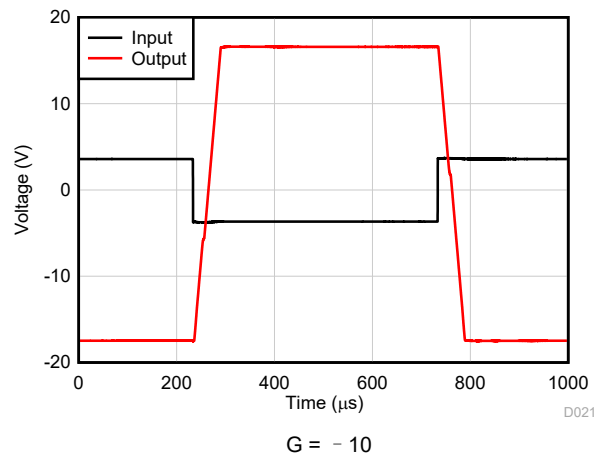


图 7-28. Overload Recovery

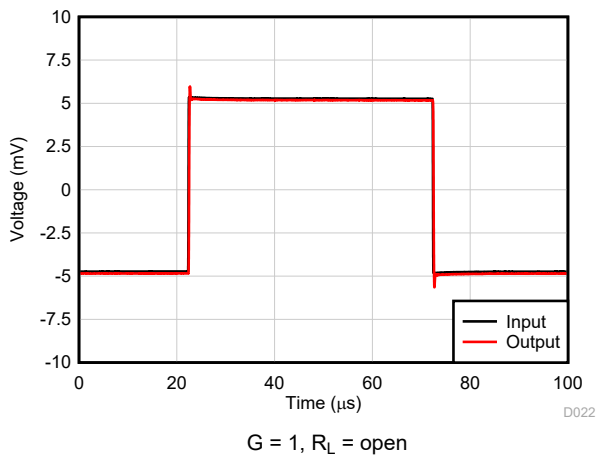


图 7-29. Small-Signal Step Response, $G = 1$

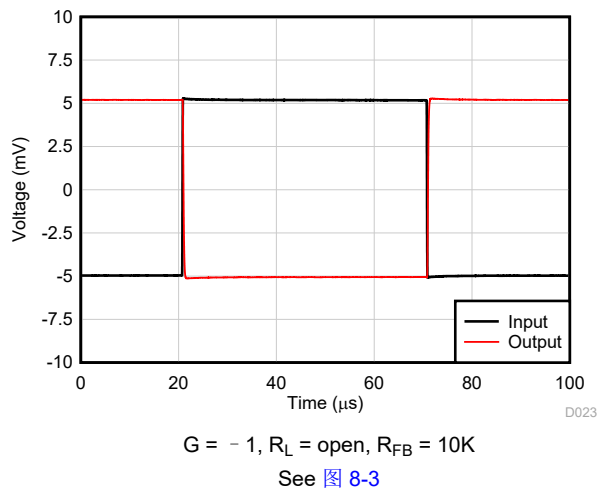
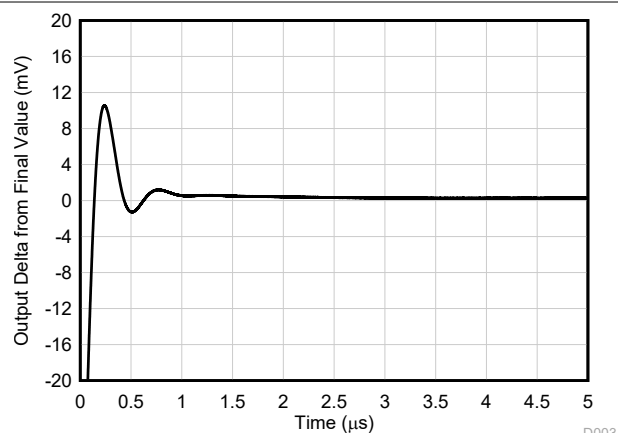


图 7-30. Small-Signal Step Response, $G = -1$

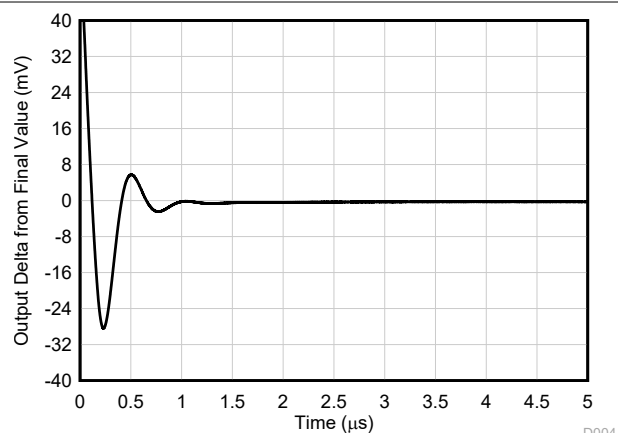
7.7 Typical Characteristics (continued)

Typical characteristics section is applicable for LM2904B-Q1 and LM2904BA-Q1. The typical characteristics data section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V}$ ($\pm 18\text{ V}$), $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).



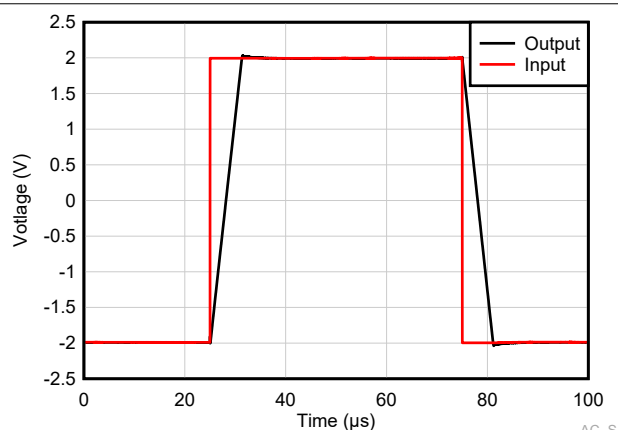
$G = 1$, $R_L = \text{open}$

图 7-31. Large-Signal Step Response (Rising)



$G = 1$, $R_L = \text{open}$

图 7-32. Large-Signal Step Response (Falling)



$G = 1$, $R_L = \text{open}$

图 7-33. Large-Signal Step Response

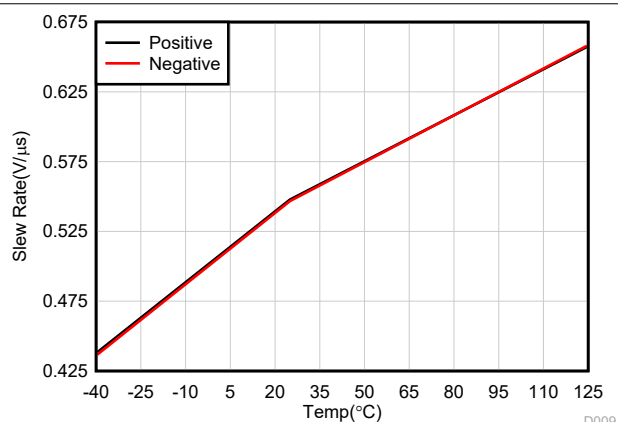


图 7-34. Slew Rate vs Temperature

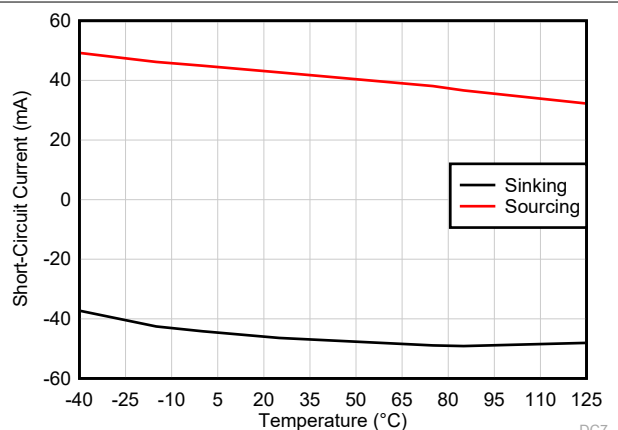
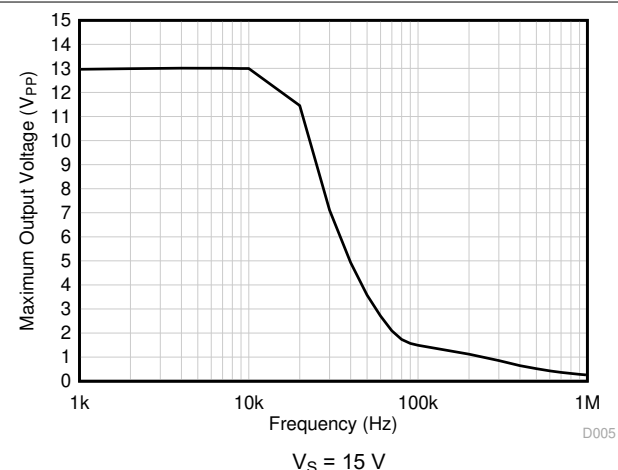


图 7-35. Short-Circuit Current vs Temperature



$V_S = 15\text{ V}$

图 7-36. Maximum Output Voltage vs Frequency

7.7 Typical Characteristics (continued)

Typical characteristics section is applicable for LM2904B-Q1 and LM2904BA-Q1. The typical characteristics data section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V}$ ($\pm 18\text{ V}$), $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).

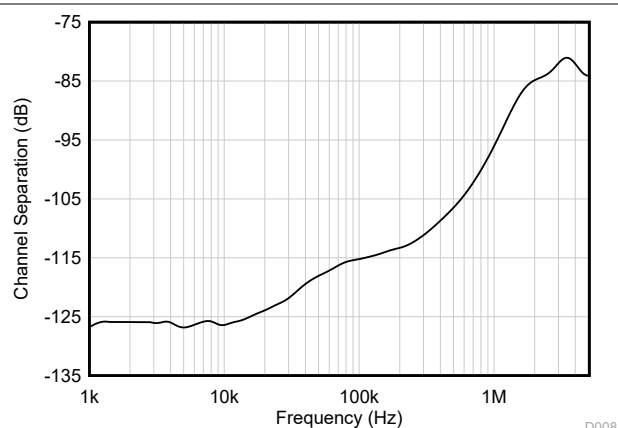


图 7-37. Channel Separation vs Frequency

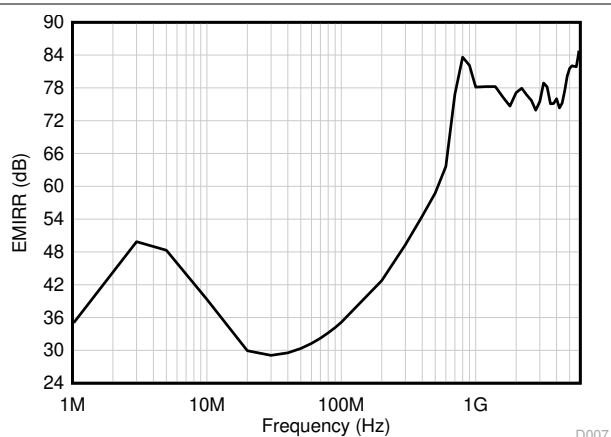


图 7-38. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

8 Parameter Measurement Information

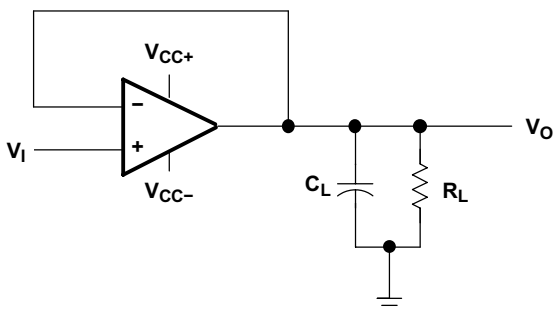


图 8-1. Unity-Gain Amplifier

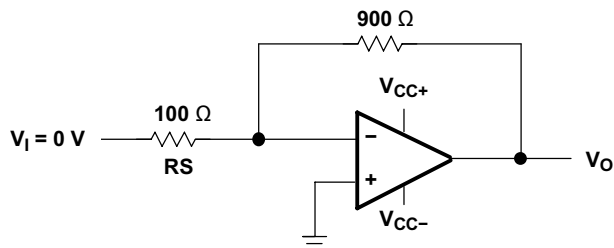
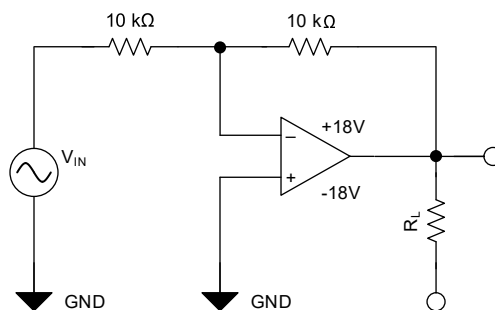


图 8-2. Noise-Test Circuit

图 8-3. Test Circuit, $G = -1$, for THD+N and Small-Signal Step Response

9.3 Feature Description

9.3.1 Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal. These devices have a 1.2-MHz unity-gain bandwidth (LM2904B-Q1 and LM2904BA-Q1).

9.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. These devices have a 0.5-V/ μ s slew rate (LM2904B-Q1 and LM2904BA-Q1).

9.3.3 Input Common Mode Range

The valid common mode range is from device ground to $V_S - 1.5\text{ V}$ ($V_S - 2\text{ V}$ across temperature). Inputs may exceed V_S up to the maximum V_S without device damage. At least one input must be in the valid input common-mode range for the output to be the correct phase. If both inputs exceed the valid range, then the output phase is undefined. If either input more than 0.3 V below V_- then input current should be limited to 1 mA and the output phase is undefined.

9.4 Device Functional Modes

The LM2904-Q1, LM2904B-Q1, and LM2904BA-Q1 devices are powered on when the supply is connected. This device can be operated as a single-supply operational amplifier or dual-supply amplifier, depending on the application.

10 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The LM2904-Q1, LM2904B-Q1, LM2904BA-Q1 operational amplifiers are useful in a wide range of signal conditioning applications. Inputs can be powered before V_S for flexibility in multiple supply circuits. For full application design guidelines related to this family of devices, please refer to the application report [Application design guidelines for LM324/LM358 devices](#).

10.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

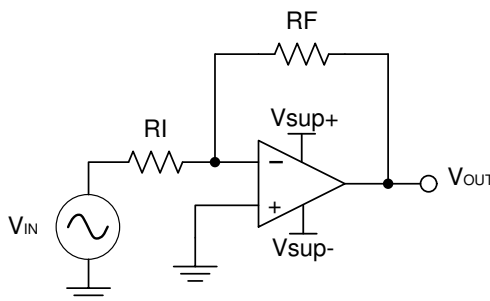


图 10-1. Application Schematic

10.2.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application scales a signal of ± 0.5 V to ± 1.8 V. Setting the supply at ± 12 V is sufficient to accommodate this application.

10.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using [方程式 1](#) and [方程式 2](#):

$$A_V = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

Once the desired gain is determined, choose a value for R_I or R_F . Choosing a value in the kilohm range is desirable because the amplifier circuit uses currents in the milliamperage range. This ensures the part does not draw too much current. This example uses $10 \text{ k}\Omega$ for R_I which means $36 \text{ k}\Omega$ is used for R_F . This was determined by [方程式 3](#).

$$A_V = -\frac{R_F}{R_I} \quad (3)$$

10.2.3 Application Curve

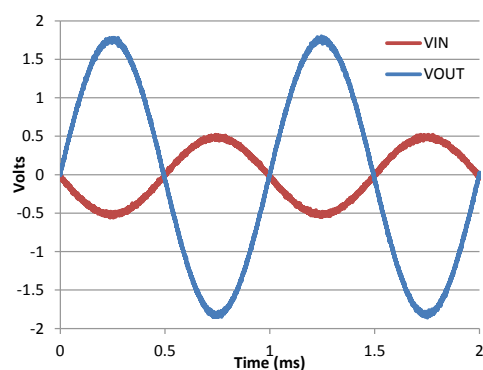


图 10-2. Input and Output Voltages of the Inverting Amplifier

11 Power Supply Recommendations

CAUTION

Supply voltages larger than specified in the recommended operating region can permanently damage the device (see [节 7.1](#)).

Place 0.1- μ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see [节 12](#).

12 Layout

12.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V_+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping R_F and R_G close to the inverting input minimizes parasitic capacitance, as shown in 节 12.2.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

12.2 Layout Examples

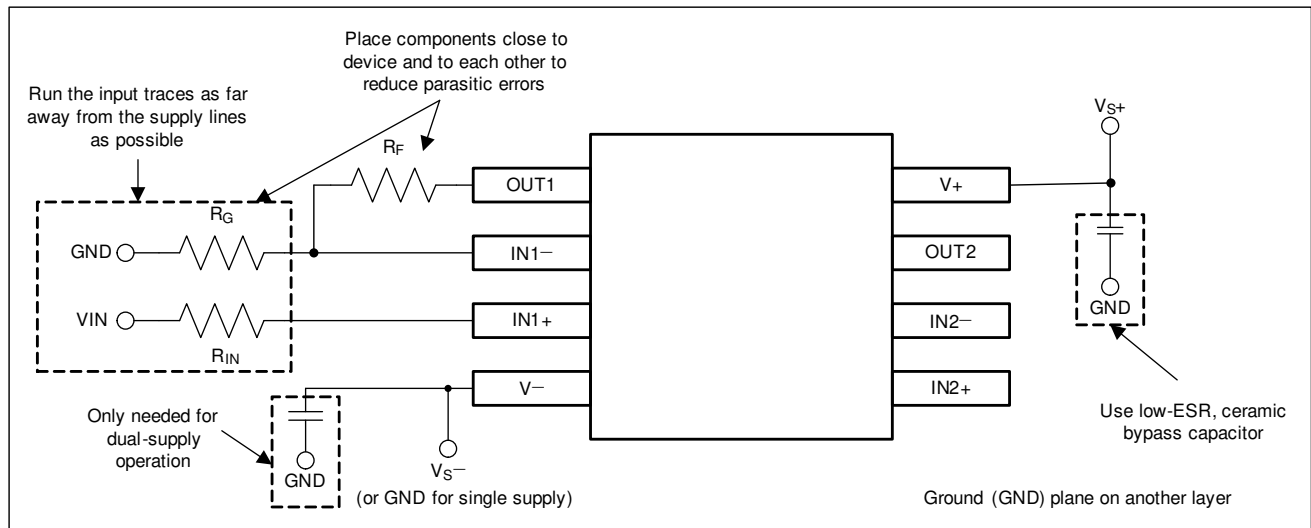


图 12-1. Operational Amplifier Board Layout for Noninverting Configuration

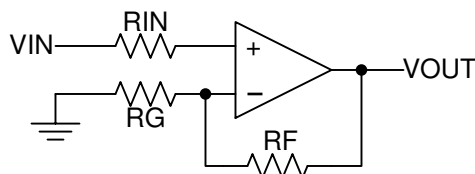


图 12-2. Operational Amplifier Schematic for Noninverting Configuration

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

Texas Instruments, [Application Design Guidelines for LM324/LM358 Devices application report](#)

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

表 13-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM2904-Q1	Click here	Click here	Click here	Click here	Click here
LM2904B-Q1	Click here	Click here	Click here	Click here	Click here
LM2904BA-Q1	Click here	Click here	Click here	Click here	Click here

13.3 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](#) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

13.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

13.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 术语表

TI 术语表

本术语表列出并解释了术语、首字母缩略词和定义。

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2904AVQDRG4Q1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904AVQ	Samples
LM2904AVQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904AVQ	Samples
LM2904AVQPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904AVQ	Samples
LM2904AVQPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904AVQ	Samples
LM2904BAQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2EMB	Samples
LM2904BAQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904BA	Samples
LM2904BAQPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	294BAQ	Samples
LM2904BQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27ZB	Samples
LM2904BQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904BQ	Samples
LM2904BQPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904BQ	Samples
LM2904BTQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4BTQ	Samples
LM2904BTQDRQ1	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904TQ	Samples
LM2904BTQPWRQ1	ACTIVE	TSSOP	PW	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904BT	Samples
LM2904QDRG4Q1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904Q1	Samples
LM2904QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904Q1	Samples
LM2904QPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904Q1	Samples
LM2904QPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904Q1	Samples
LM2904VQDRG4Q1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904VQ	Samples
LM2904VQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904VQ1	Samples
LM2904VQPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904VQ	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2904VQPWRQ1	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904VQ	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LM2904-Q1, LM2904B-Q1, LM2904BA-Q1 :

• Catalog : [LM2904](#), [LM2904B](#), [LM2904BA](#)

- Enhanced Product : [LM2904-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2904AVQDRG4Q1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2904AVQDRG4Q1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904AVQDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2904AVQPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904AVQPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904AVQPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904BAQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2904BAQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904BAQPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904BQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2904BQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904BQPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904BTQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2904BTQDRQ1	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904BTQPWRQ1	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904QDRG4Q1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2904QDRG4Q1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904QDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2904QPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904QPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904QPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904VQDRG4Q1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2904VQDRG4Q1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904VQDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2904VQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904VQPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904VQPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904VQPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904VQPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2904AVQDRG4Q1	SOIC	D	8	2500	340.5	336.1	25.0
LM2904AVQDRG4Q1	SOIC	D	8	2500	340.5	336.1	25.0
LM2904AVQDRQ1	SOIC	D	8	2500	340.5	336.1	25.0
LM2904AVQPWRG4Q1	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2904AVQPWRG4Q1	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904AVQPWRQ1	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904BAQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM2904BAQDRQ1	SOIC	D	8	2500	340.5	336.1	25.0
LM2904BAQPWRQ1	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904BQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM2904BQDRQ1	SOIC	D	8	2500	340.5	336.1	25.0
LM2904BQPWRQ1	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904BTQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM2904BTQDRQ1	SOIC	D	8	3000	340.5	338.1	20.6
LM2904BTQPWRQ1	TSSOP	PW	8	3000	356.0	356.0	35.0
LM2904QDRG4Q1	SOIC	D	8	2500	340.5	336.1	25.0
LM2904QDRG4Q1	SOIC	D	8	2500	340.5	336.1	25.0
LM2904QDRQ1	SOIC	D	8	2500	340.5	336.1	25.0

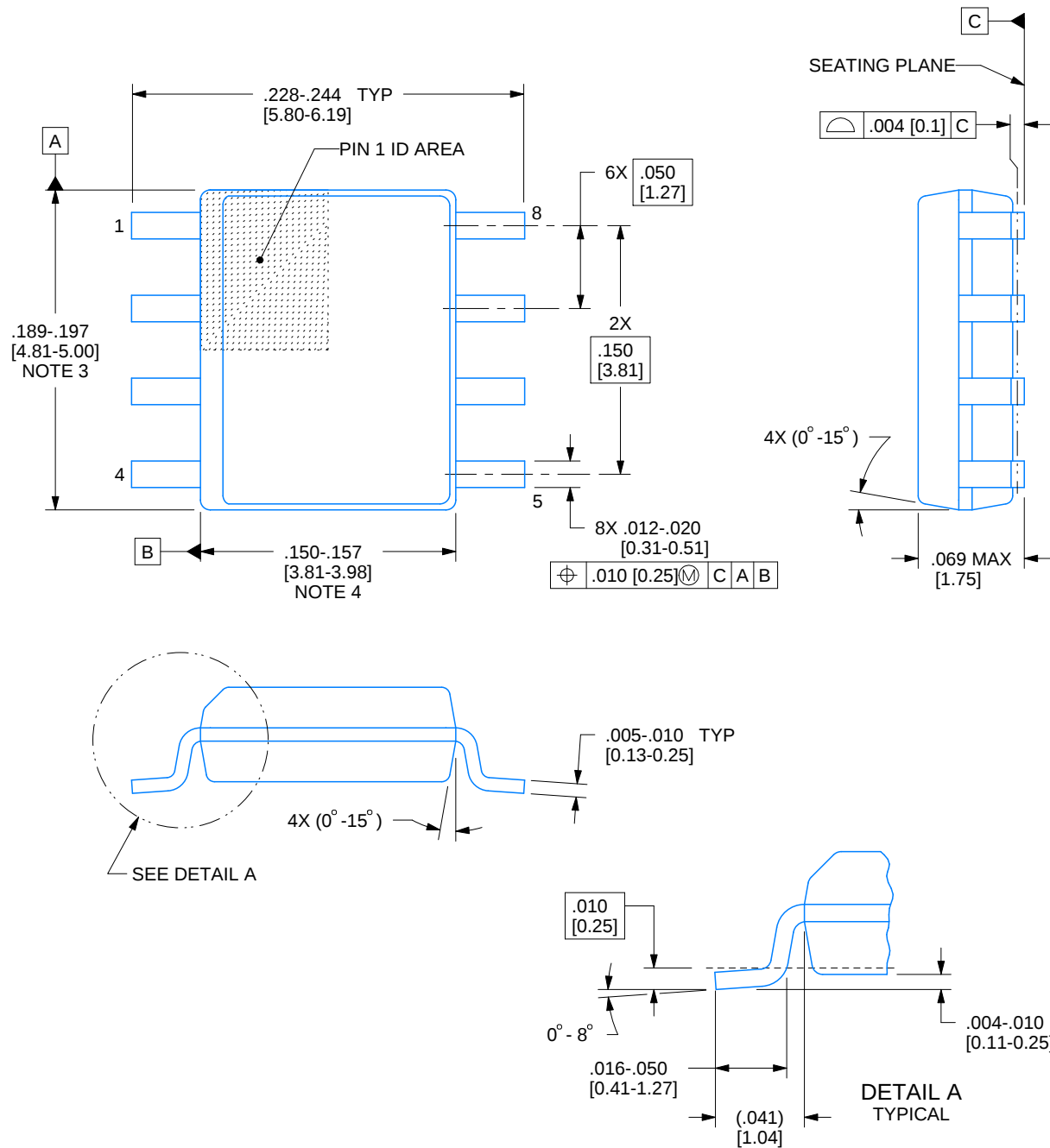
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2904QPWRG4Q1	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904QPWRG4Q1	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904QPWRQ1	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904VQDRG4Q1	SOIC	D	8	2500	340.5	336.1	25.0
LM2904VQDRG4Q1	SOIC	D	8	2500	340.5	336.1	25.0
LM2904VQDRQ1	SOIC	D	8	2500	340.5	336.1	25.0
LM2904VQDRQ1	SOIC	D	8	2500	340.5	336.1	25.0
LM2904VQPWRG4Q1	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904VQPWRG4Q1	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2904VQPWRQ1	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904VQPWRQ1	TSSOP	PW	8	2000	356.0	356.0	35.0

D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

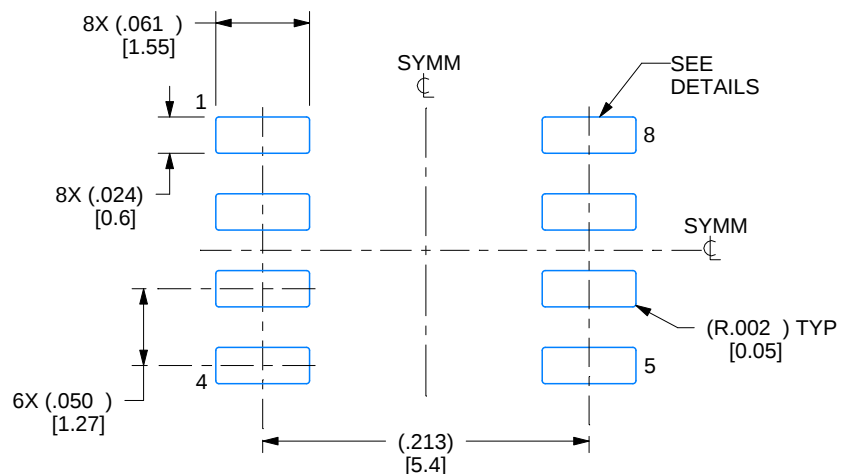
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

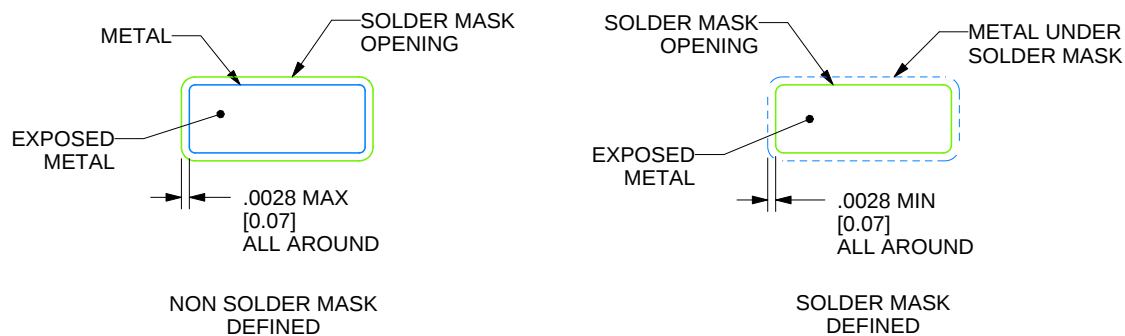
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE



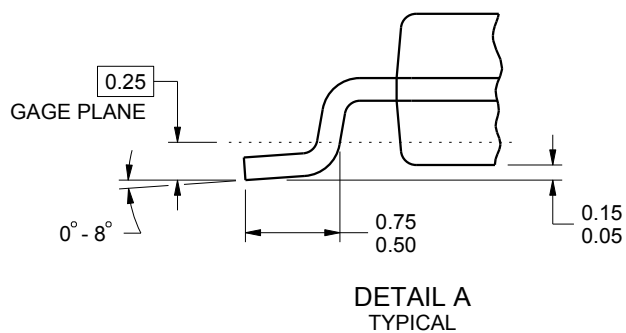
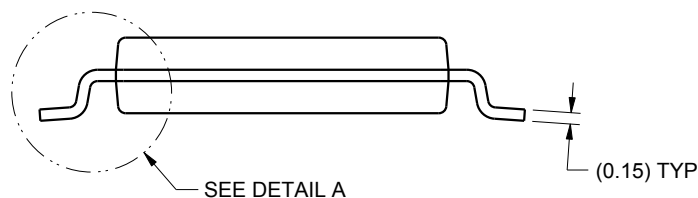
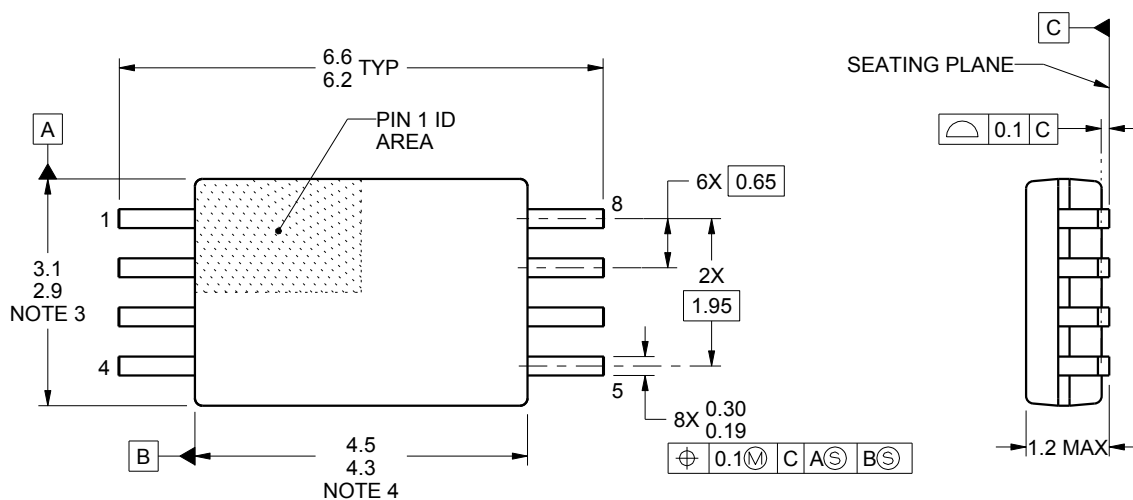
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

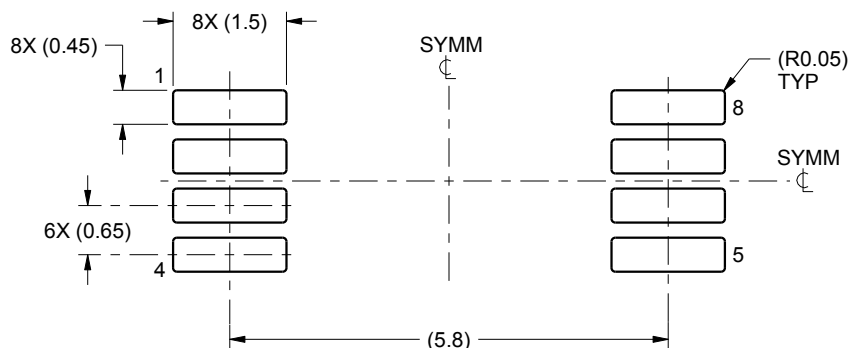
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

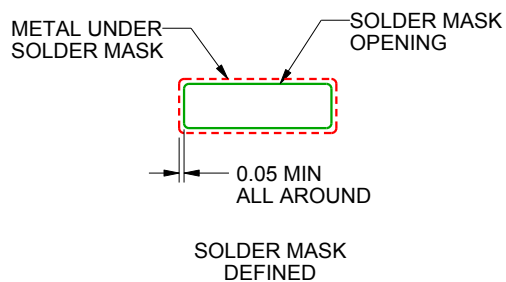
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

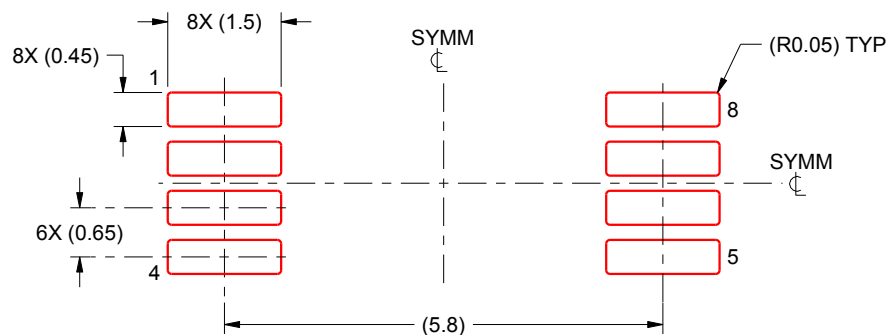
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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