LM3881 Simple Power Sequencer With Adjustable Timing

1 Features

- Easiest Method to Sequence Rails
- Power-Up and Power-Down Control
- Tiny Footprint
- Low Quiescent Current of 80 µA
- Input Voltage Range of 2.7 V to 5.5 V
- Output Invert Feature
- Timing Controlled by Small Value External Capacitor

2 Applications

- Security Cameras
- Servers
- Networking Elements
- FPGA Sequencing
- Microprocessor and Microcontroller Sequencing
- Multiple Supply Sequencing

3 Description

The LM3881 Simple Power Sequencer offers the easiest method to control power up and power down of multiple power supplies (switching or linear regulators). By staggering the start-up sequence, it is possible to avoid latch conditions or large inrush currents that can affect the reliability of the system.

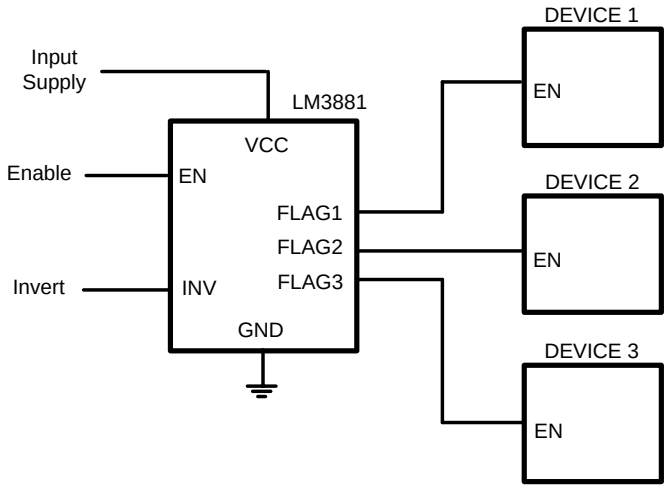
Available in VSSOP-8 package, the Simple Sequencer contains a precision enable pin and three open-drain output flags. When the LM3881 is enabled, the three output flags will sequentially release, after individual time delays, thus permitting the connected power supplies to start up. The output flags will follow a reverse sequence during power down to avoid latch conditions. Time delays are defined using an external capacitor and the output flag states can be inverted by the user.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM3881	VSSOP (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical System Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (April 2013) to Revision D	Page
• Added *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	4

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	13

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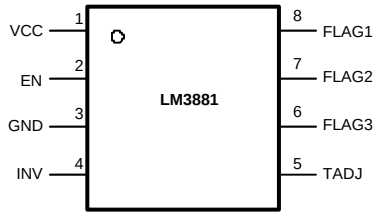
5 Pin Configuration and Functions

VSSOP Package
8-Pin DGK
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VCC	1	I	Input Supply
EN	2	I	Precision Enable
GND	3	–	Ground
INV	4	I	Output Logic Invert
TADJ	5	O	Timer Adjust
FLAG3	6	O	Open-Drain Output 3
FLAG2	7	O	Open-Drain Output 2
FLAG1	8	O	Open-Drain Output 1

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (1)(2)

	MIN	MAX	UNIT
VCC, EN, INV, TADJ, FLAG1, FLAG2, FLAG3 to GND	–0.3	6.0	V
Junction Temperature		150	°C
Lead Temperature (Soldering, 5 s)		260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)		2	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
VCC to GND	2.7	5.5	V
EN, INV, TADJ, FLAG1, FLAG2, FLAG3 to GND	–0.3	VCC + 0.3	V
Junction Temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM3881 DGK 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	224.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	107.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	145.3	
ψ_{JT}	Junction-to-top characterization parameter	31.8	
ψ_{JB}	Junction-to-board characterization parameter	143.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). Minimum and Maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C and are provided for reference purposes only. T_J = –40°C to +125°C, V_{CC} = 3.3 V, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
I_Q	Operating Quiescent Current			80	110	µA
OPEN-DRAIN FLAGS						
I_{FLAG}	FLAGx Leakage Current	V_{FLAGx} = 3.3 V		0.001	1	µA
V_{OL}	FLAGx Output Voltage Low	I_{FLAGx} = 1.2 mA			0.4	V
TIME DELAYS						
I_{TADJ_SRC}	TADJ Source Current		4	12	20	µA
I_{TADJ_SNK}	TADJ Sink Current		4	12	20	µA
V_{HTH}	High Threshold Level		1.0	1.22	1.4	V
V_{LTH}	Low Threshold Level		0.3	0.5	0.7	V
T_{CLK}	Clock Cycle	C_{ADJ} = 10 nF		1.2		ms
T_{D1}, T_{D4}	Flag Time Delay		9		10	Clock cycles
T_{D2}, T_{D3}, T_{D5}, T_{D6}	Flag Time Delay			8		Clock cycles
ENABLE PIN						
V_{EN}	EN Pin Threshold		1.0	1.22	1.5	V
I_{EN}	EN Pin Pullup Current	V_{EN} = 0 V		7		µA
INV PIN						
V_{IH_INV}	Invert Pin V_{IH}		90% VCC			V
V_{IL_INV}	Invert Pin V_{IL}				10% VCC	V

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate TI's Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely parametric norm.

6.6 Typical Characteristics

V_{CC} = 3.3 V unless otherwise specified.

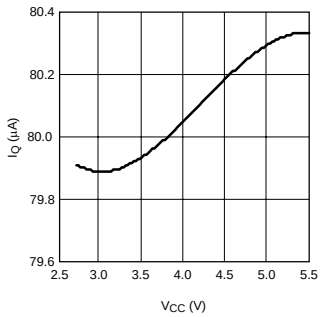

Figure 1. Quiescent Current vs V_{CC}

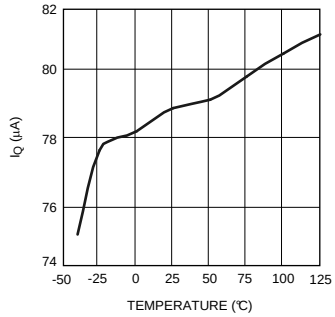

Figure 2. Quiescent Current vs Temperature

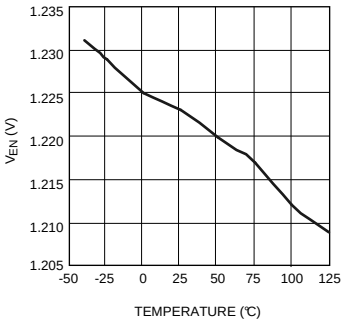

Figure 3. Enable Threshold vs Temperature

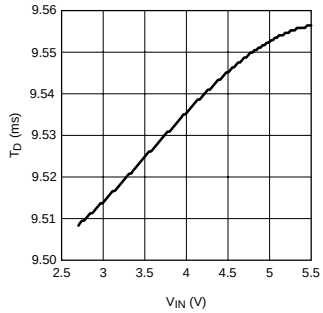

Figure 4. Time Delay vs V_{IN} (C_{ADJ} = 10 nF Nominal)

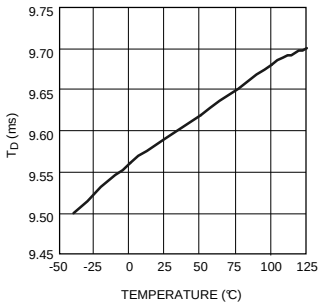

Figure 5. Time Delay vs Temperature (C_{ADJ} = 10 nF Nominal)

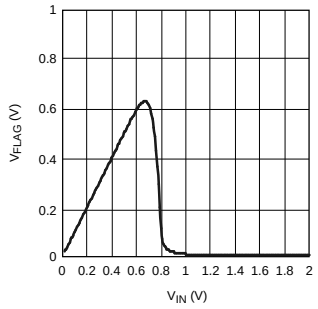

Figure 6. V_{FLAG} vs V_{IN} (INV Low, R_{FLAG} = 100 kΩ)

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Typical Characteristics (continued)

V_{CC} = 3.3 V unless otherwise specified.

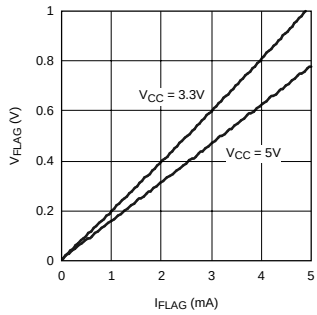


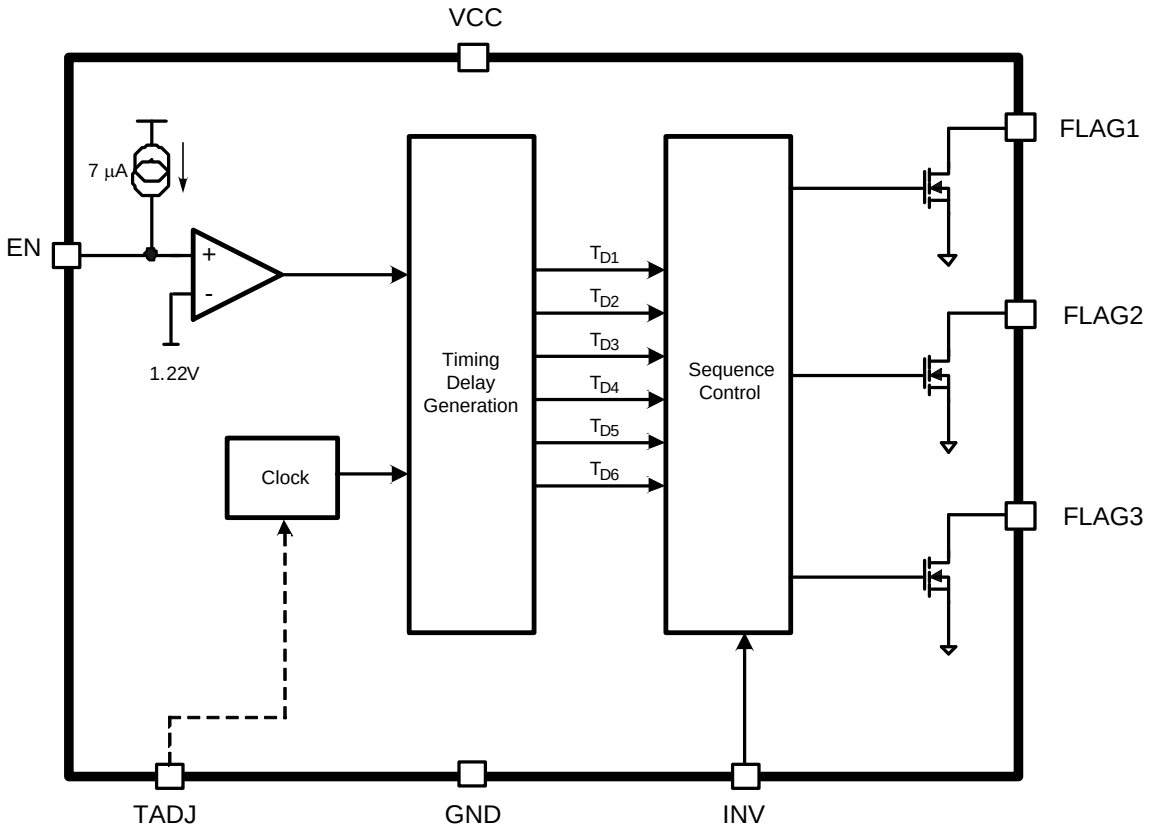
Figure 7. FLAG Voltage vs Current

7 Detailed Description

7.1 Overview

The LM3881 Simple Power Sequencer provides a simple solution for sequencing multiple rails in a controlled manner. An established clock signal facilitates control of the power up and power down of three open-drain FET output flags. These flags permit connection to shutdown or enable pins of linear regulators and/or switching regulators to control the operation of the power supplies. This allows design of a complete power system without the concern of large inrush currents or latch-up conditions that can occur during an uncontrolled startup. An invert (INV) pin reverses the logic of the output flags. This pin should be tied to a logic output high or low and not allowed to remain open circuit. The following discussion assumes the INV pin is held low such that the flag output is active high.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Adjustable Timing

A small external timing capacitor is connected to the TADJ pin that establishes the clock waveform. This capacitor is linearly charged/discharged by a fixed current source/sink, denoted I_{TADJ_SRC} / I_{TADJ_SNK}, of magnitude 12 µA between predefined voltage threshold levels, denoted V_{LTH} and V_{HTH}, to generate the timing waveform as shown in Figure 8.

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Feature Description (continued)

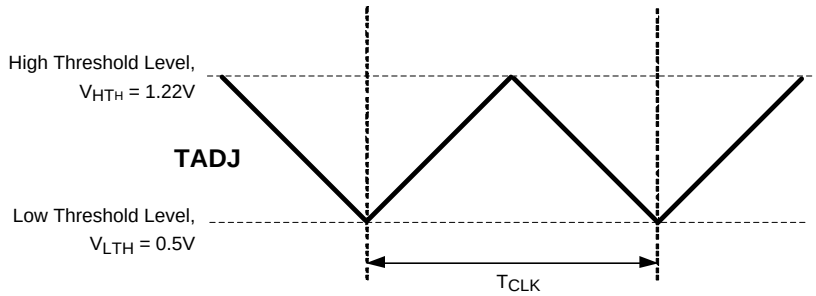

Figure 8. TADJ Pin Timing Waveform

Thus, the clock cycle duration is directly proportional to the timing capacitor value. Considering the TADJ voltage threshold levels and the charge/discharge current magnitude, it can be shown that the timing capacitor-clock period relationship is typically 120 µs/nF. For example, a 10-nF capacitor sets up a clock period of 1.2 ms.

The timing sequence of the LM3881 is controlled by the enable (EN) pin. Upon power up, all the flags are held low until the precision enable pin exceeds its threshold. After the EN pin is asserted, the power-up sequence will commence and the open-drain flags will be sequentially released.

An internal counter will delay the first flag (FLAG1) from rising until a fixed time period, denoted by T_{D1} in Figure 9, elapses. This corresponds to at least nine, maximum 10, clock cycles depending on where EN is asserted relative to the clock signal. Upon release of the first flag, another timer will begin to delay the release of the second flag (FLAG2). This time delay, denoted T_{D2}, corresponds to exactly eight clock periods. Similarly, FLAG3 is released after time delay T_{D3}, again eight clock cycles, has expired. Accordingly, a TADJ capacitor of 10 nF generates typical time delays T_{D2} and T_{D3} of 9.6 ms and T_{D1} of from 10.8 ms to 12.0 ms.

The power-down sequence is the same as power up, but in reverse order. When the EN pin is deasserted, a timer will begin that delays the third flag (FLAG3) from pulling low. The second and first flag will then follow in a sequential manner after their appropriate time delays. These time delays, denoted T_{D4}, T_{D5}, T_{D6}, are equal to T_{D1}, T_{D2}, T_{D3}, respectively.

For robustness, the pulldown FET associated with each flag is designed such that it can sustain a short circuit to VCC.

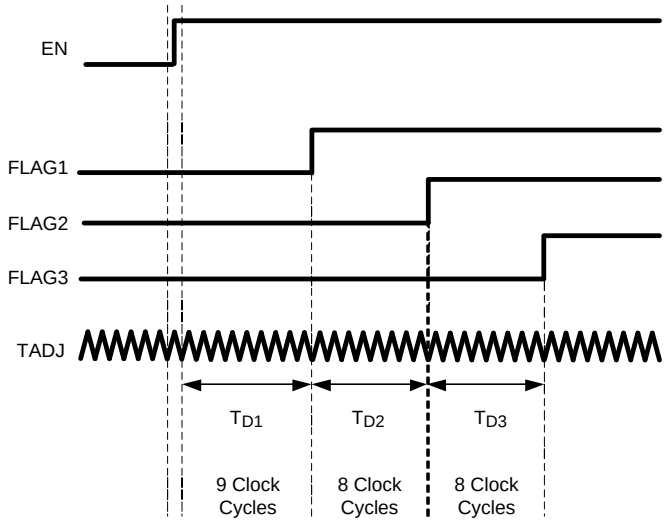

Figure 9. Power-Up Sequence, INV Low

Feature Description (continued)

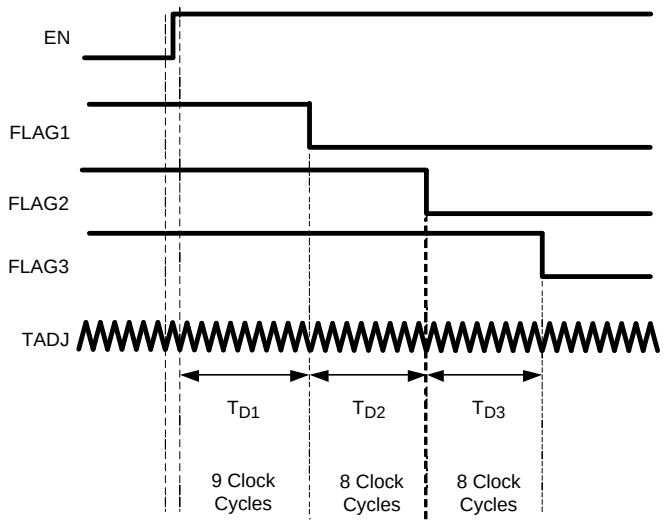

Figure 10. Power-Up Sequence, INV High

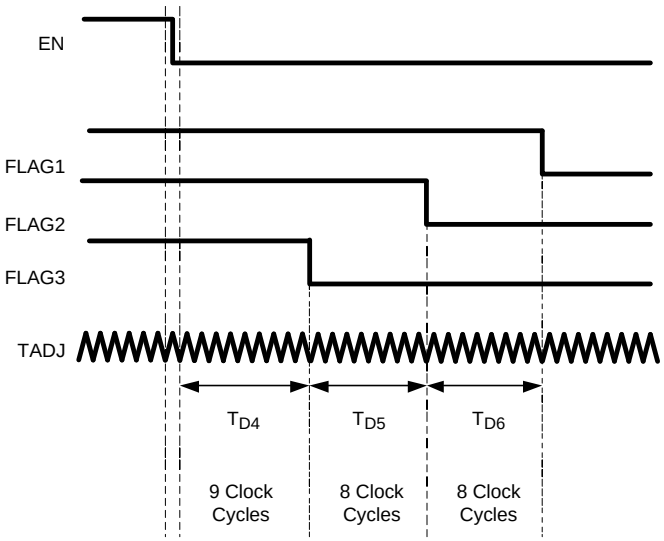

Figure 11. Power-Down Sequence, INV Low

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Feature Description (continued)

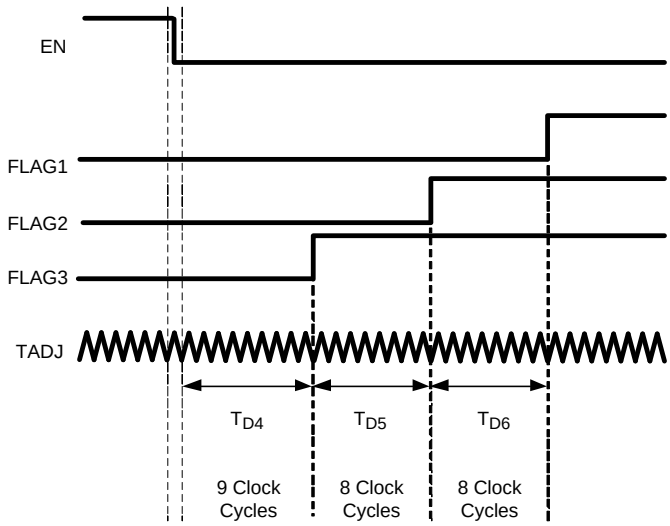

Figure 12. Power-Down Sequence, INV High

7.3.2 Enable Circuit

The enable circuit is designed with an internal comparator, referenced to a bandgap voltage (1.22 V), to provide a precision threshold. This allows the timing to be set externally using a capacitor as shown in Figure 13. Alternatively, sequencing can be based on a certain event such as a line voltage reaching 90% of its nominal value by employing a resistor divider from VCC to Enable.

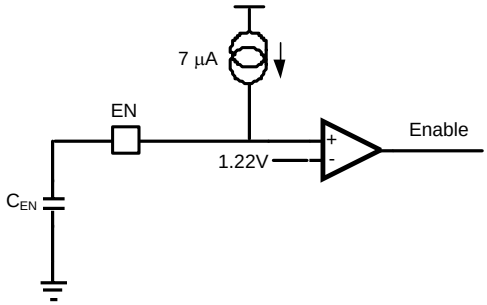

Figure 13. Precision Enable Circuit

Using the internal pullup current source to charge the external capacitor C_{EN}, the time delay while the enable voltage reaches the required threshold, assuming EN is charging from 0V, can be calculated by the equation as follows.

$$T_{enable_delay} = \frac{1.22V \times C_{EN}}{7\ \mu A} \tag{1}$$

Feature Description (continued)

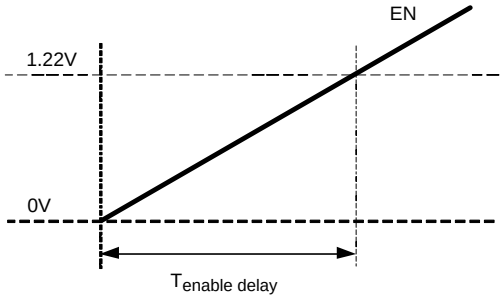

Figure 14. Enable Delay Timing

A resistor divider can also be used to enable the LM3881 based on exceeding a certain VCC supply voltage threshold. Take care when sizing the resistor divider to include the effects of the internal EN pullup current source. The supply voltage for which EN is asserted is given by

$$VCC_{ENABLE} = 1.22V\left(1 + \frac{R_{EN1}}{R_{EN2}}\right) - 7\ \mu A\ (R_{EN1} \| R_{EN2}) \tag{2}$$

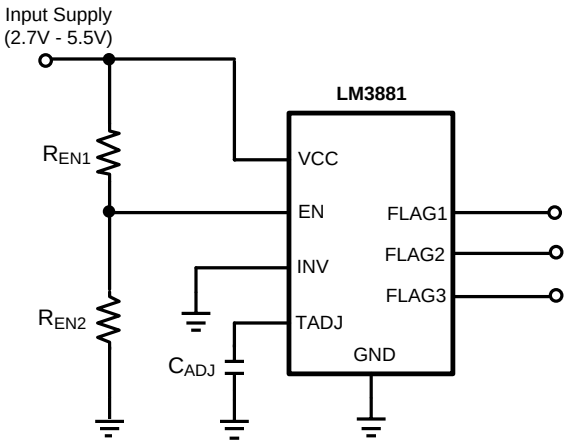

Figure 15. Enable Based On Input Supply Level

One of the features of the EN pin is that it provides glitch free operation. The timer will start counting at a rising threshold, but will always reset if the EN pin is deasserted before the first output flag is released. This is illustrated in Figure 16, assuming INV is low.

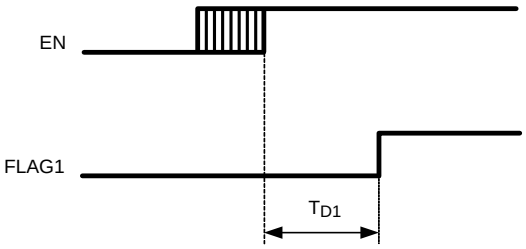

Figure 16. Enable Glitch Timing, INV Low

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Feature Description (continued)

If the EN pin remains high for the entire power up sequence, then the part will operate as shown in the standard timing diagrams. However, if the EN signal is deasserted before the power-up sequence completes, the part will enter a controlled shutdown. This allows the system to initiate a controlled power sequence, preventing any latch conditions to occur. Figure 17 describes the flag sequence if the EN pin is deasserted after FLAG1 releases, but before the entire power-up sequence is completed. INV is assumed low.

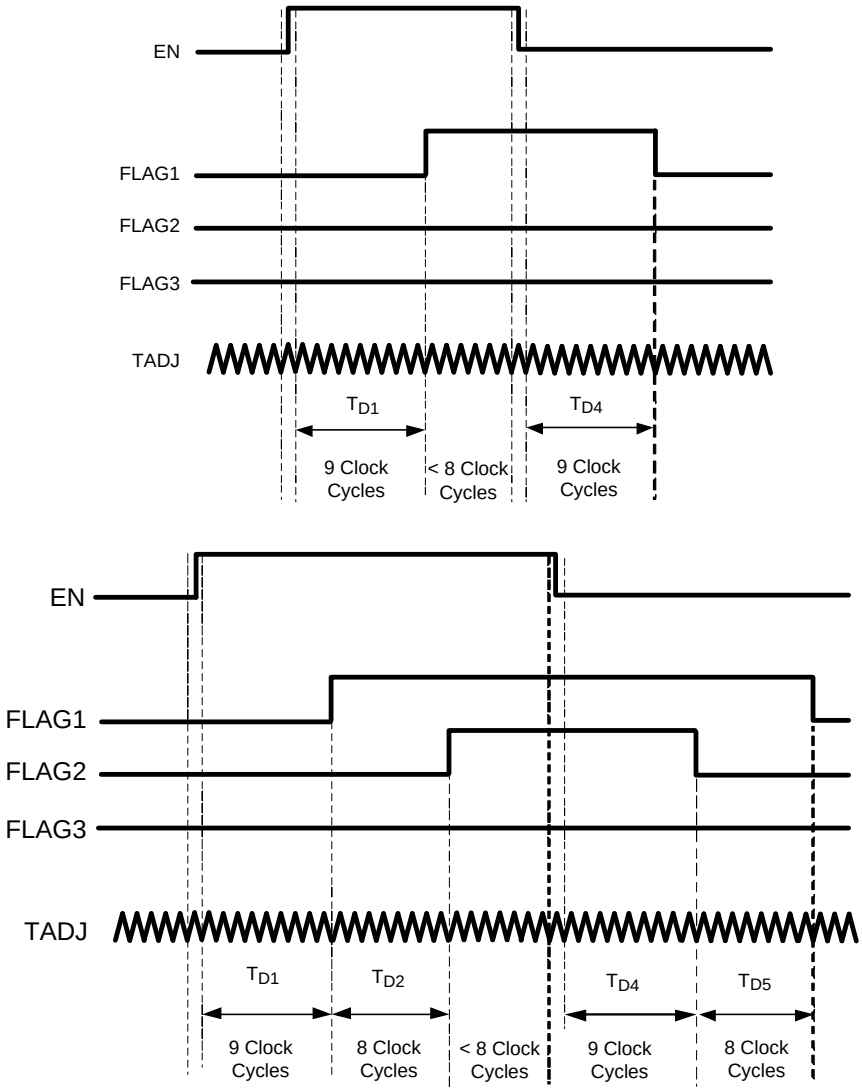

Figure 17. Incomplete Sequence Timing, INV Low

7.4 Device Functional Modes

7.4.1 Power Up with EN Pin

The timing sequence of the Simple Power Sequencer is controlled entirely by the enable (EN) pin. Upon power up, all the flags are held low until this precision enable is pulled high. After the EN pin is asserted, the power-up sequence will commence.

Device Functional Modes (continued)

7.4.2 Power Down with EN Pin

When EN pin is deasserted, the power down sequence will commence. A timer will begin that delays the third flag (FLAG3) from pulling low. The second and first flag will then follow in a sequential manner after their appropriate delays.

7.4.3 Noninverted Output Mode

When the INV pin is tied to a logic output low, the logic mode of the output flags is active high. This mode is useful to sequence power supplies which have an active high enable input.

7.4.4 Inverted Output Mode

When the INV pin is tied to a logic output high, the logic mode of the output flags is active low. This mode is useful to sequence power supplies which have an active low enable input.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Open-Drain Flags Pullup

The Simple Power Sequencer contains three open-drain output flags which need to be pulled up for proper operation. 100-kΩ resistors can be used as pullup resistors.

8.1.2 Enable the Device

See *Enable Circuit*.

8.1.3 Timing Adjust

See *Adjustable Timing*.

8.2 Typical Application

8.2.1 Simple Sequencing of Three Power Supplies

The Simple Power Sequencer is used to implement a power-up (1 - 2 - 3) and power-down (3 - 2 - 1) sequence of three power supplies.

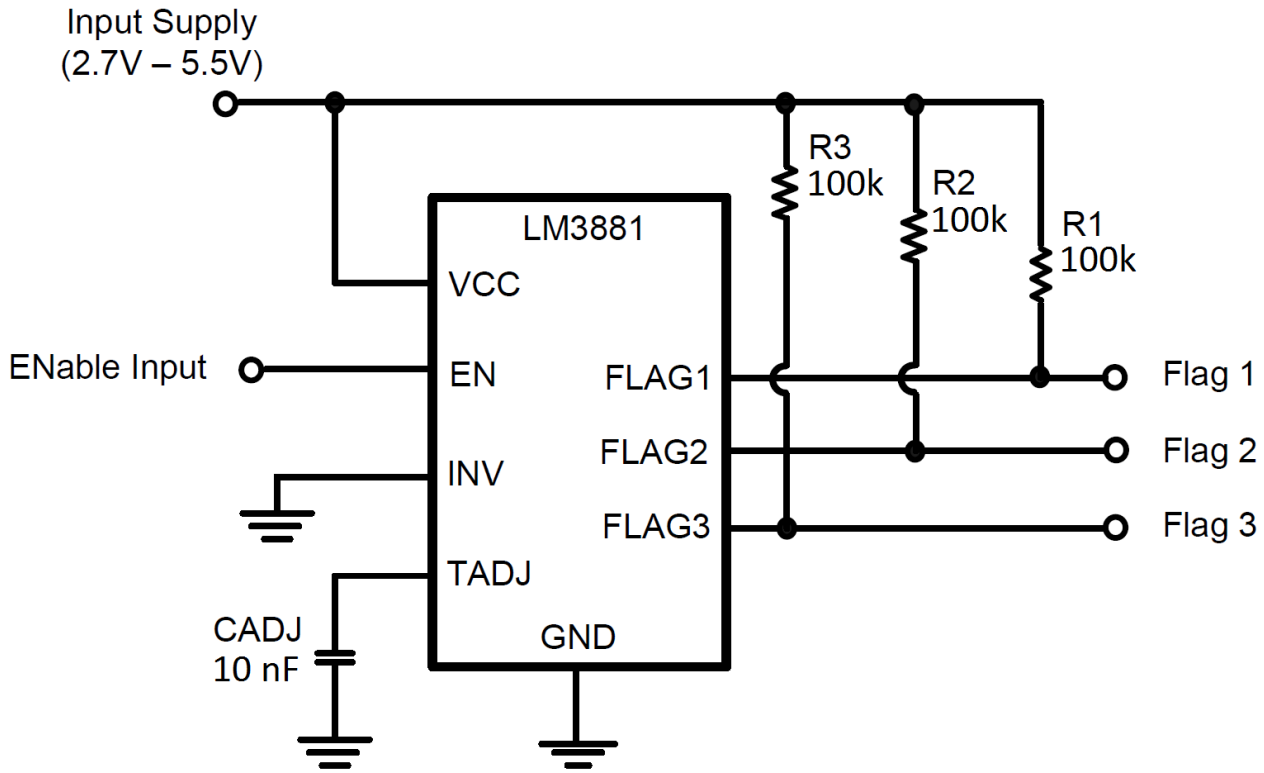

Figure 18. Typical Application Circuit

Typical Application (continued)

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

Design Parameter	Example Value
Input Supply voltage range	2.7 V to 5.5 V
Flag Output voltage, EN high	Input Supply
Flag Output voltage, EN low	0 V
Flag Timing Delay, T_{D1}	10.8 ms - 12.0 ms
Flag Timing Delay, T_{D2} and T_{D3}	9.6 ms
Power-Up Sequence	1 - 2 - 3
Power-Down Sequence	3 - 2 - 1

8.2.1.2 Detailed Design Procedure

Table 2. Evaluation Board Bill of Materials

Ref Des	Description	Case Size	Manufacturer	Manufacturer P/N
U1	LM3881 Sequencer	MSOP-8	Texas Instruments	LM388
R1	100 kΩ	0603	Vishay Dale	CRCW06031003F-e3
R2	100 kΩ	0603	Vishay Dale	CRCW06031003F-e3
R3	100 kΩ	0603	Vishay Dale	CRCW06031003F-e3
CADJ	10 nF ±10% X7R 16 V	0603	Murata	GRM188R71C103KA01

A timing capacitor of C_{ADJ} = 10 nF generates typical time delays T_{D2} and T_{D3} of 9.6 ms and T_{D1} of between 10.8 ms and 12.0 ms. The INV pin is tied to GND so that the output flags are active high. See *Adjustable Timing* for calculating the value for C_{ADJ}.

8.2.1.3 Application Curves

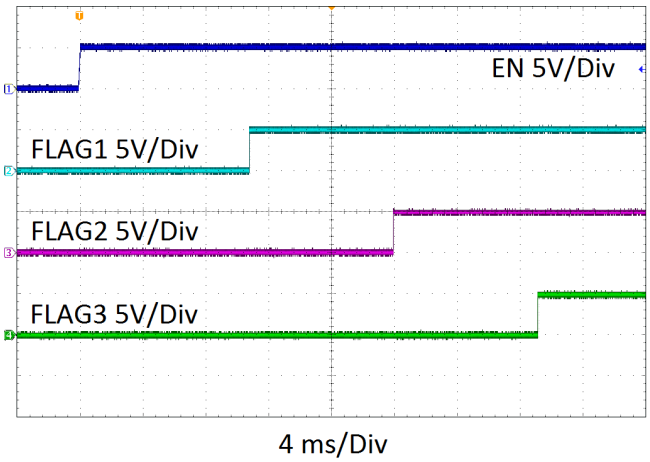

Figure 19. Power-Up Sequence, C_{ADJ} = 10 nF

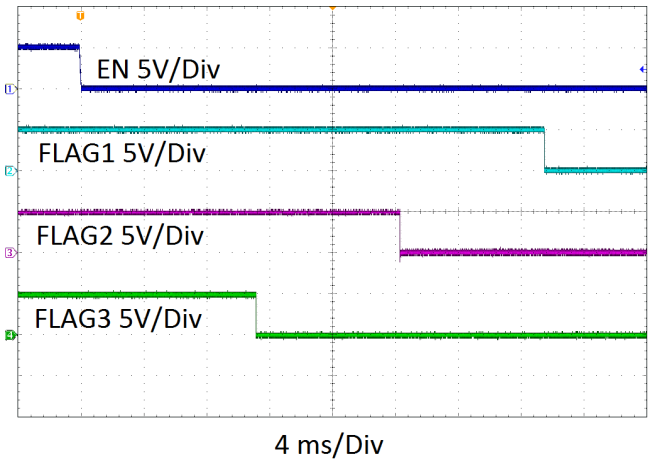

Figure 20. Power-Down Sequence, C_{ADJ} = 10 nF

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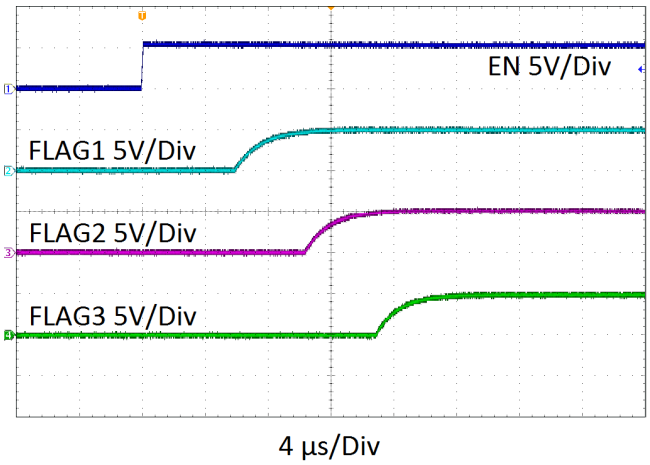

Figure 21. Power-Up Sequence, TADJ Open

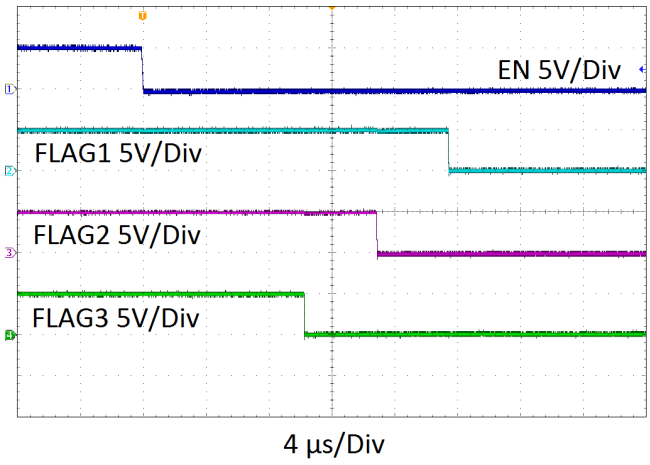

Figure 22. Power-Down Sequence, TADJ Open

8.2.2 Sequencing Using Independent Flag Supply

For applications requiring a flag output voltage that is different from the VCC, a separate Flag Supply may be used to pullup the open-drain outputs of the Simple Power Sequencer. This is useful when interfacing the flag outputs with inputs that require a different voltage than VCC. The designer must ensure the Flag Supply voltage is within the range specified in the *Recommended Operating Conditions*.

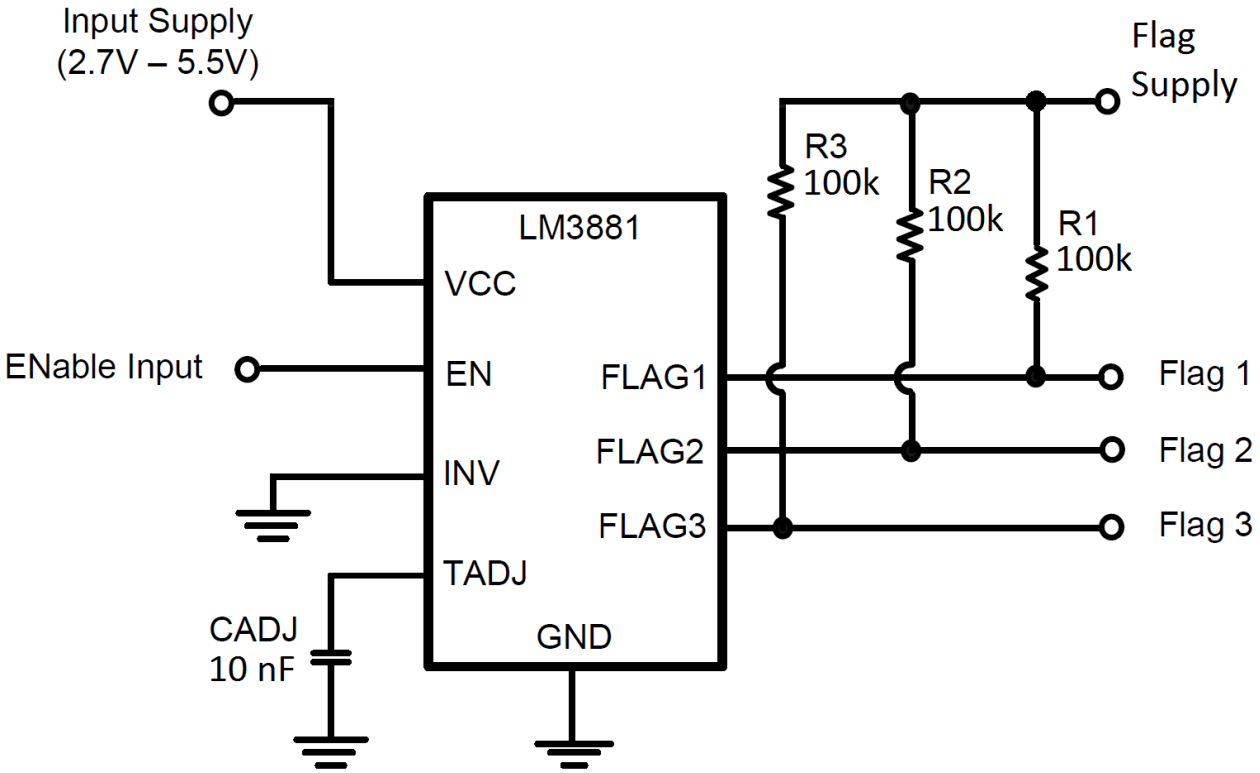

Figure 23. Sequencing Using Independent Flag Supply

9 Power Supply Recommendations

The VCC pin should be located as close as possible to the input supply (2.7V - 5.5V). An input capacitor is not required but is recommended when noise might be present on the VCC pin. A 0.1 µF ceramic capacitor may be used to bypass this noise.

10 Layout

10.1 Layout Guidelines

- Pullup resistors should be connected between the flag output pins and a positive input supply, usually VCC. An independent flag supply may also be used. These resistors should be placed as close as possible to the Simple Power Sequencer and the flag supply. Minimal trace length is recommended to make the connections. A typical value for the pullup resistors is 100kΩ.
- For very tight sequencing requirements, minimal and equal trace lengths should be used to connect the flag outputs to the desired inputs. This will reduce any propagation delay and timing errors between the flag outputs along the line.

10.2 Layout Example

Figure 24 and Figure 25 are layout examples for the LM3881. These examples are taken from the LM3881EVAL. An optional component, assigned reference designator R4, is placed on the bottom side of the PCB to facilitate connection of INV to GND.

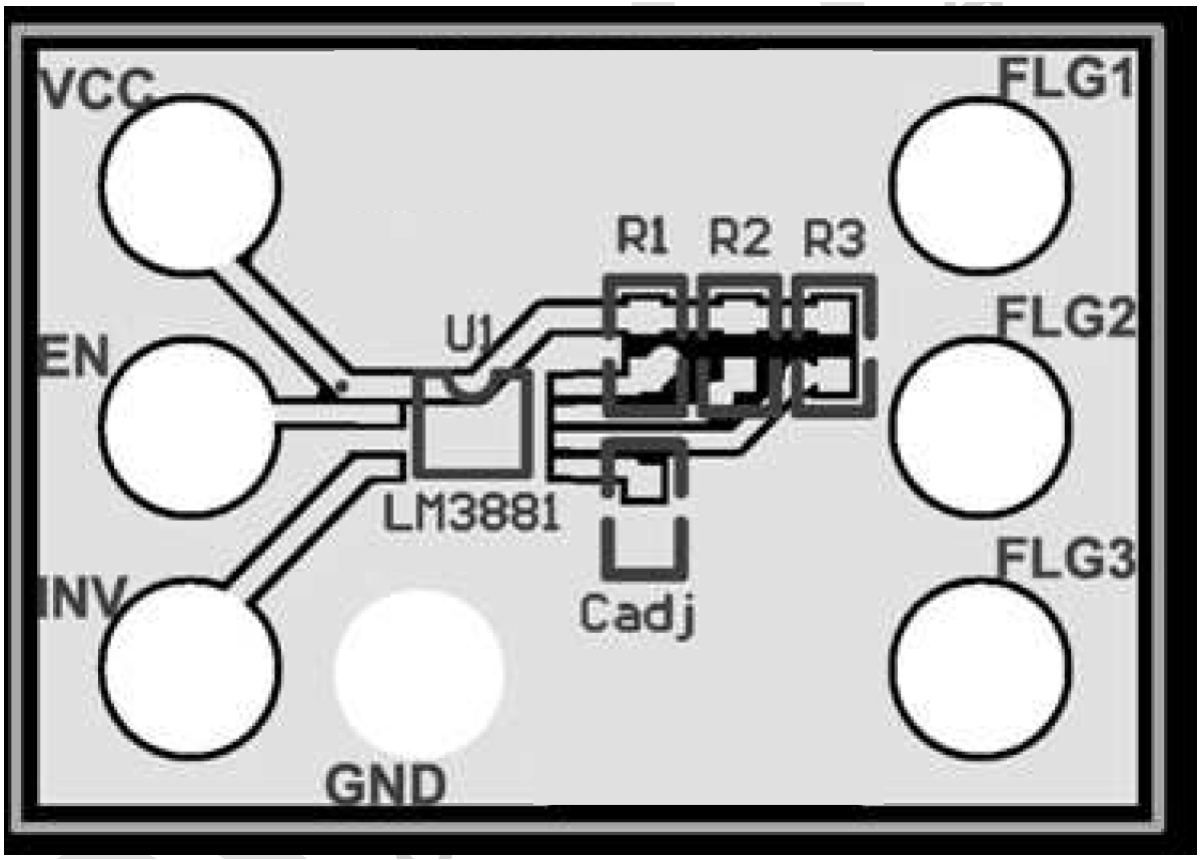

Figure 24. LM3881 Top

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Layout Example (continued)

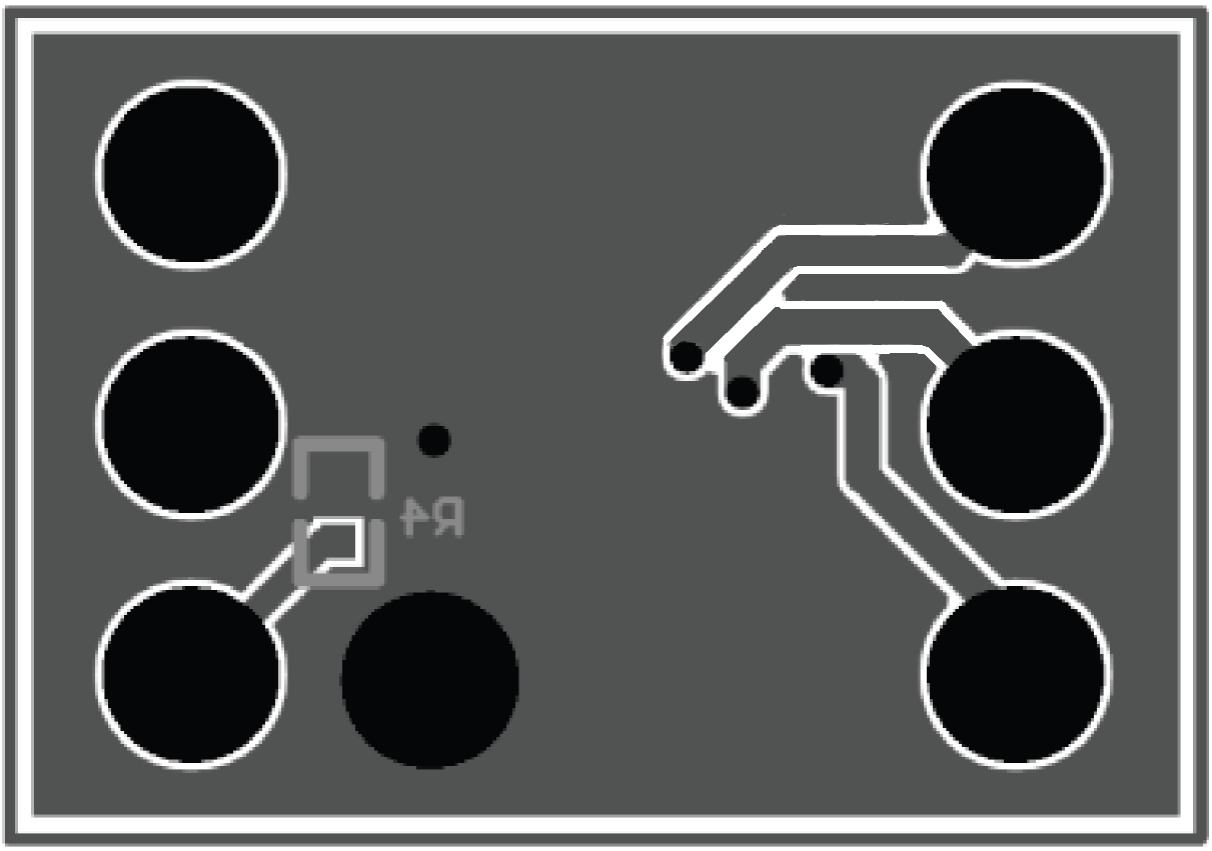

Figure 25. LM3881 Bottom

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3881MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	STBB	Samples
LM3881MME/NOPB	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	STBB	Samples
LM3881MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	STBB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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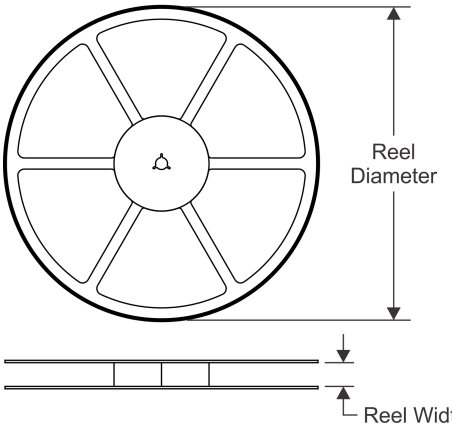
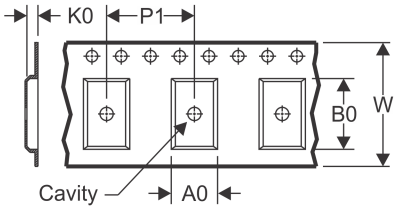
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

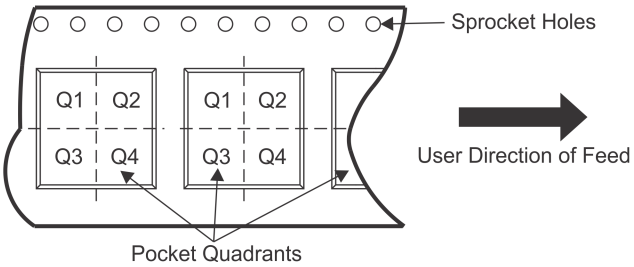


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

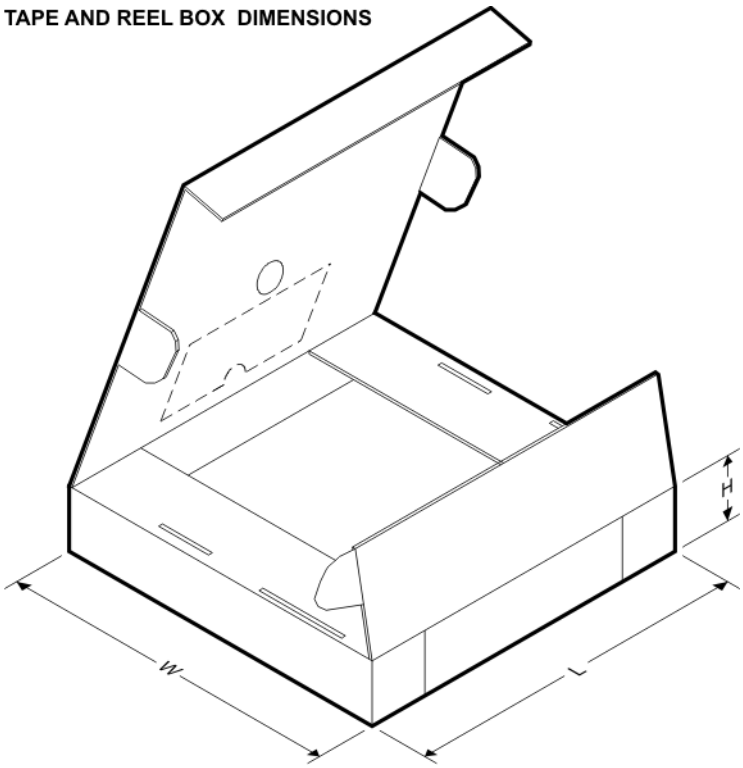
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3881MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3881MME/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3881MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

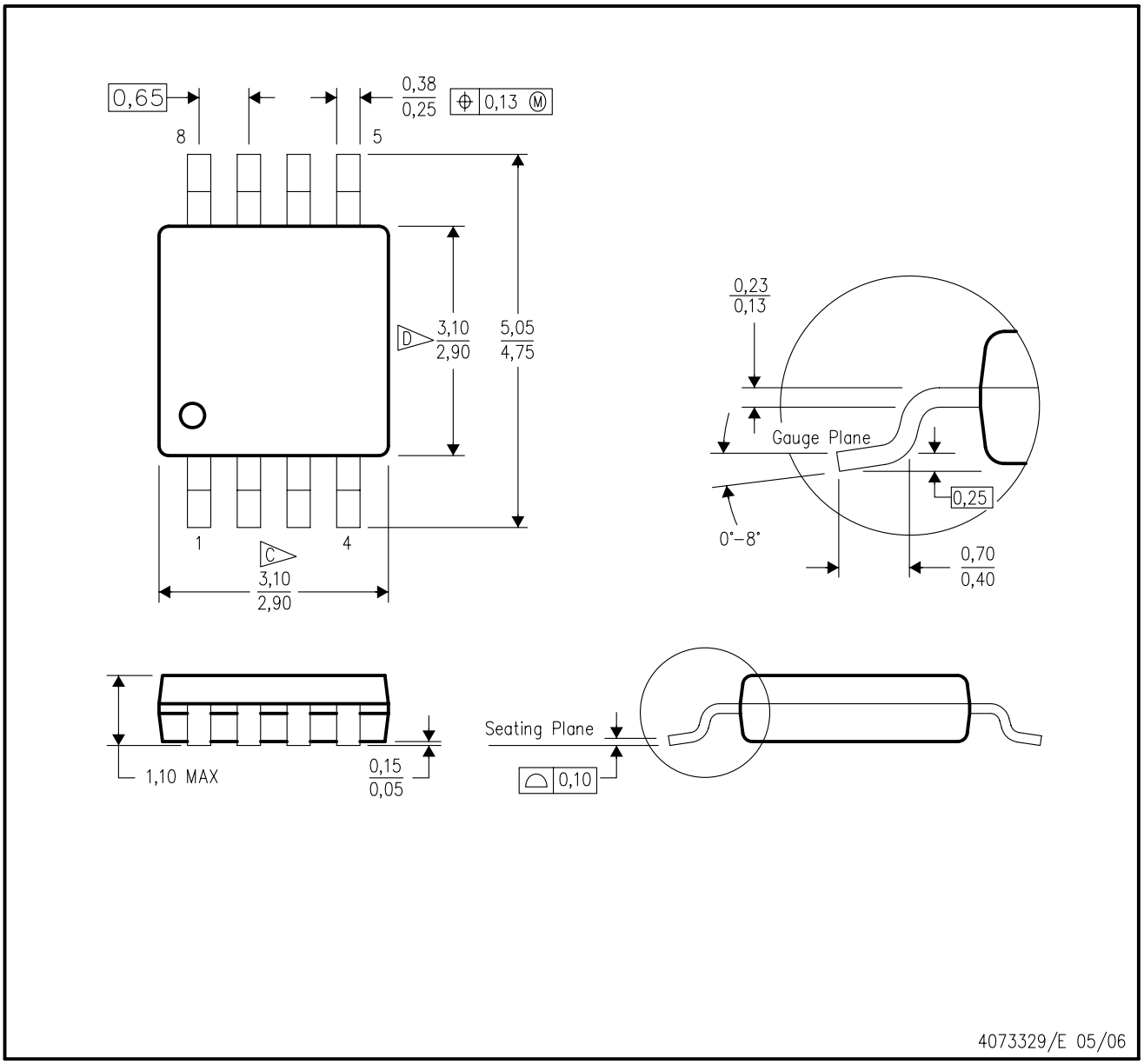
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

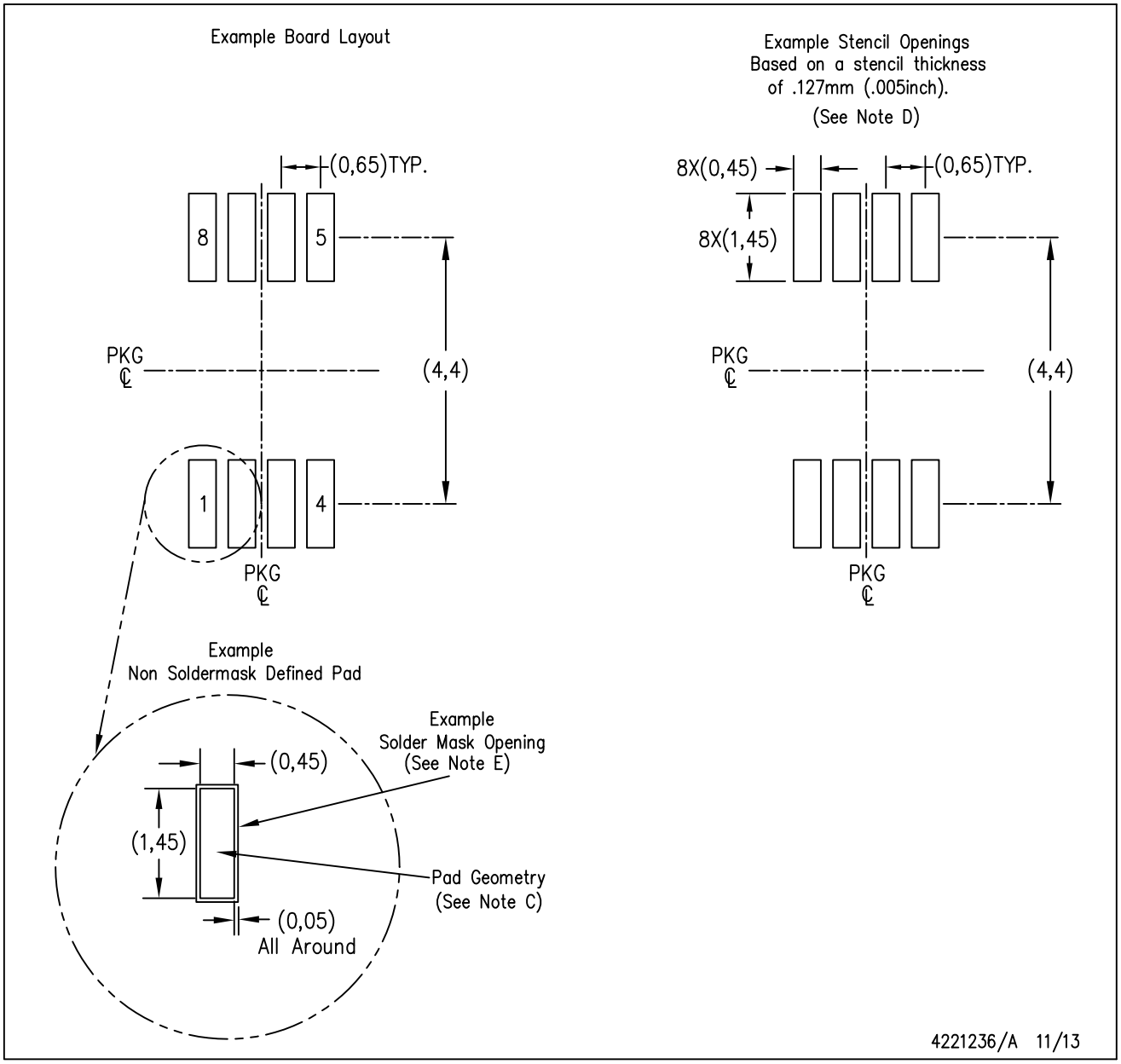
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3881MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM3881MME/NOPB	VSSOP	DGK	8	250	208.0	191.0	35.0
LM3881MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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