LM5050-2 High Side OR-ing FET Controller

Check for Samples: LM5050-2

FEATURES

- **Wide Operating Input Voltage Range: +6V to +75V**
- **+100 Volt Transient Capability**
- **Charge Pump Gate Driver for External N-Channel MOSFET**
- **MOSFET Diagnostic Test Mode**
- **Fast 50ns Response to Current Reversal**
- **2A Peak Gate Turn-off Current**
- **Minimum V_{DS} Clamp for Faster Turn-off**
- **Package: SOT-6 (Thin SOT23-6)**

APPLICATIONS

- **Active OR-ing of Redundant (N+1) Power Supplies**

DESCRIPTION

The LM5050-2 High Side OR-ing FET Controller operates in conjunction with an external MOSFET as an ideal diode rectifier when connected in series with a power source. This OR-ing controller allows MOSFETs to replace diode rectifiers in power distribution networks thus reducing both power loss and voltage drops.

The LM5050-2 controller provides charge pump gate drive for an external N-Channel MOSFET and a fast response comparator to turn off the FET when current flows in the reverse direction. The LM5050-2 can connect power supplies ranging from +6V to +75V and can withstand transients up to +100V.

The LM5050-2 also provides a FET test diagnostic mode which allows the system controller to test for shorted MOSFETs.

Typical Application Circuits

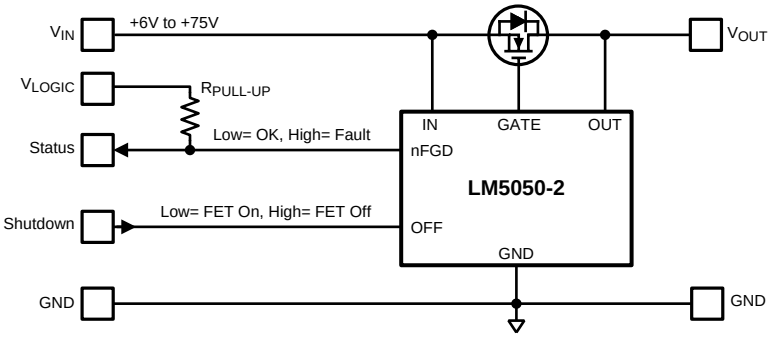


Figure 1. Full Application with MOSFET Diagnostic

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2010–2013, Texas Instruments Incorporated

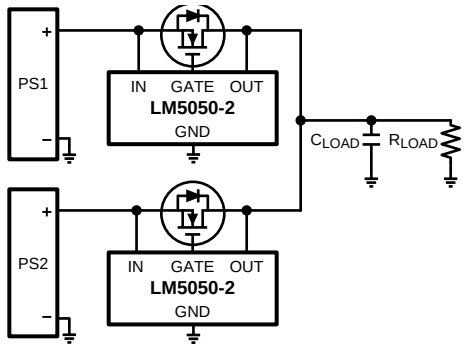


Figure 2. Typical Redundant Supply Configuration

Connection Diagram

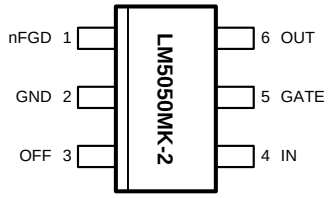


Figure 3. LM5050MK-2
SOT-6 Package (Top View)

PIN DESCRIPTIONS

Pin #	Name	Function
1	nFGD	Open drain output for the FET Test circuit. Status pin used in conjunction with the OFF test mode pin. When the OFF pin is in the logic high state, an active low state on nFGD indicates that the forward voltage (from source to drain) of the external MOSFET is greater than 350 mV. The nFGD pin requires an external pull-up resistor to a voltage not higher than 5.5V.
2	GND	Ground return for the controller
3	OFF	FET Test Mode control input. Logic low or open state at the OFF pin will deactivate the FET Test Mode. A logic high state at the OFF pin will pull the GATE pin low and turn off the external MOSFET. If the body diode forward voltage of the MOSFET (from source to drain) is greater than 350mV when the OFF pin is in the high state, the nFGD pin will indicate that the MOSFET is not shorted by pulling to the active low state.
4	IN	Voltage sense connection to the external MOSFET Source pin and supply input to the internal charge pump.
5	GATE	Connection to the external MOSFET Gate.
6	OUT	Voltage sense connection to the external MOSFET Drain pin and supply pin for biasing the internal control circuitry.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Copyright © 2010–2013, Texas Instruments Incorporated

Absolute Maximum Ratings (1)(2)

IN, OUT Pins to Ground (3)	-0.3V to 100V
GATE Pin to Ground (3)	-0.3V to 100V
OFF Pin to Ground	-0.3V to 7V
nFGD Pin to Ground (Off)	-0.3V to 7V
Storage Temperature Range	−65°C to 150°C
ESD HBM (4) MM (5)	 2 kV 150V
Peak Reflow Temperature (6)	260°C, 30sec

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including in-operability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. Operating Range conditions indicate the conditions at which the device is functional and the device should not be operated beyond such conditions. For specifications and conditions, see Electrical Characteristics.
(3) The GATE pin voltage is typically 12V above the IN pin voltage when the LM5050-2 is enabled (i.e. OFF Pin is Open or Low, and $V_{IN} > V_{OUT}$). Therefore, the Absolute Maximum Rating for the IN pin voltage applies only when the LM5050-2 is disabled (i.e. OFF Pin is logic high), or for a momentary surge to that voltage since the Absolute Maximum Rating for the GATE pin is also 100V
(4) The Human Body Model (HBM) is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. Applicable test standard is JESD-22-A114-C.
(5) The Machine Model (MM) is a 200 pF capacitor discharged through a 0Ω resistor (i.e. directly) into each pin. Applicable test standard is JESD-A115-A.
(6) For soldering specifications visit www.ti.com.

Operating Ratings (1)

IN, OUT Pins	+6.0V to +75V
OFF Pin Voltage	0.0V to 5.5V
nFGD Voltage (Off)	0.0V to 5.5V
nFGD Sink Current (On)	0 mA to 1 mA
Junction Temperature Range (T_J)	−40°C to +125°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including in-operability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. Operating Range conditions indicate the conditions at which the device is functional and the device should not be operated beyond such conditions. For specifications and conditions, see Electrical Characteristics.

Copyright © 2010–2013, Texas Instruments Incorporated

Electrical Characteristics

Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the operating junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12.0V, V_{OUT} = 12.0V, V_{OFF}= 0.0V, C_{GATE}= 47 nF, and T_J = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IN Pin						
V_{IN}	Operating Supply Range		**6.0**	-	**75.0**	V
I_{IN}	IN Pin current	V_{IN} = 6.0V GATE = Open V_{OUT} = V_{IN} - 100 mV	**180**	240	**300**	µA
		V_{IN} = 12.0V GATE = Open V_{OUT} = V_{IN} - 100 mV	**262**	350	**440**	
		V_{IN} = 75.0V GATE = Open V_{OUT} = V_{IN} - 100 mV	**275**	355	**460**	
OUT Pin						
I_{OUT}	OUT Pin Current	V_{IN} = 6.0V V_{OUT} = V_{IN} - 100 mV	**74**	95	**115**	uA
		V_{IN} = 12.0V V_{OUT} = V_{IN} - 100 mV	**70**	110	**160**	
		V_{IN} = 75.0V V_{OUT} = V_{IN} - 100 mV	**35**	125	**265**	
GATE Pin						
$I_{GATE(ON)}$	GATE Pin Source Current	V_{IN} = 6.0V to 75V V_{GATE} = V_{IN} V_{OUT} = V_{IN} - 175 mV	**18.0**	32.	**45.0**	uA
V_{GS}	V_{GATE} - V_{IN} in Forward Operation (1)	V_{IN} = 6.0V V_{OUT} = V_{IN} - 175 mV	**6.0**	6.8	**7.4**	V
		V_{IN} = 12.0V V_{OUT} = V_{IN} - 175 mV	**8.0**	11.5	**14.7**	
		V_{IN} = 75.0V V_{OUT} = V_{IN} - 175 mV	**8.0**	11	**14.5**	
$t_{GATE(REV)}$	Gate Capacitance Discharge Time at Forward to Reverse Transition See Figure 4	C_{GATE} = 0 (2)	-	27	**100**	ns
		C_{GATE} = 10 nF (2)	-	61	-	
		C_{GATE} = 47 nF (2)	-	205	**425**	
$t_{GATE(OFF)}$	Gate Capacitance DischargeTime at OFF pin Low to High Transition See Figure 5	C_{GATE} = 47 nF (3)	-	450	-	ns
$I_{GATE(OFF)}$	GATE Pin Sink Current	V_{GATE} = V_{IN} + 3V V_{OUT} > V_{IN} + 100 mV t ≤ 10ms	**1.9**	2.8	-	A
$V_{SD(REV)}$	Reverse V_{SD} Threshold V_{IN} < V_{OUT}	V_{IN} - V_{OUT}	**-37**	-27	**-17**	mV
$\Delta V_{SD(REV)}$	Reverse V_{SD} Hysteresis		-	10	-	mV
$V_{SD(REG)}$	Regulated Forward V_{SD} Threshold V_{IN} > V_{OUT}	V_{IN} = 6.0V V_{IN} - V_{OUT}	**6**	20	**33**	mV
		V_{IN} = 12.0V V_{IN} - V_{OUT}	**2**	16	**31**	

(1) Measurement of V_{GS} voltage (i.e. V_{GATE} - V_{IN}) includes 1 MΩ in parallel with C_{GATE}
(2) Time from V_{IN}-V_{OUT} voltage transition from 200mV to -500mV until GATE pin voltage falls to V_{IN} + 1V. See Figure 4
(3) Time from V_{OFF} voltage transition from 0.0V to 5.0V until GATE pin voltage falls to V_{IN} + 1V. See Figure 5

Copyright © 2010–2013, Texas Instruments Incorporated

Electrical Characteristics (continued)

Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the operating junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12.0V, V_{OUT} = 12.0V, V_{OFF}= 0.0V, C_{GATE}= 47 nF, and T_J = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
OFF Pin						
$V_{OFF(IH)}$	OFF Input High Threshold Voltage	V_{OUT} = V_{IN}-500 mV V_{OFF} Rising	-	1.55	**1.73**	V
$V_{OFF(IL)}$	OFF Input Low Threshold Voltage	V_{OUT} = V_{IN} - 500 mV V_{OFF} Falling	**1.09**	1.41	-	
ΔV_{OFF}	OFF Threshold Voltage Hysteresis	$V_{OFF(IH)}$ - $V_{OFF(IL)}$	-	160	-	mV
I_{OFF}	OFF Pin Internal Pull-down	V_{OFF} = 5.0V	**2.0**	5	**8.0**	µA
nFGD Pin						
$V_{SD(TST)}$	FET Test Threshold Voltage V_{IN} < V_{OUT}	V_{OFF} = 5V V_{OUT} = 12V V_{IN} falling from 12V	**250**	350	**450**	mV
$\Delta V_{SD(TST)}$	FET Test Threshold Voltage Hysteresis		-	95	-	mV
$nFGD_{VOL}$	nFGD Output Low Voltage nFGD Output = On	V_{OFF} = 5V I_{nFGD} = 1 mA Sinking	-	630	**850**	mV
$nFGD_{IOL}$	nFGD Output Leakage Current nFGD Output = Off	V_{OFF} = 0V V_{nFGD} = 5.5V	-	0.001	**0.7**	µA

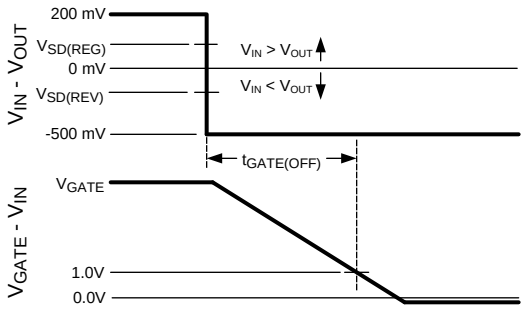


Figure 4. Gate Off Timing for Forward to Reverse Transition

Copyright © 2010–2013, Texas Instruments Incorporated

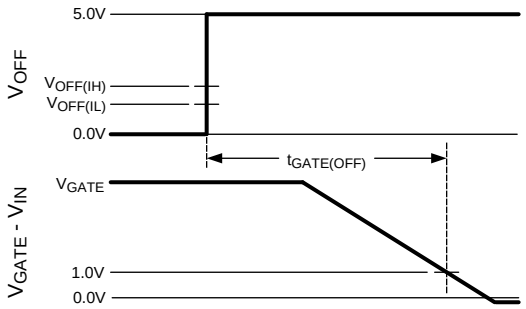


Figure 5. Gate Off Timing for OFF pin Low to High Transition

Copyright © 2010–2013, Texas Instruments Incorporated

Typical Performance Characteristics

Unless otherwise stated V_{IN} = 12V, V_{OFF} = 0.0V, and T_J = 25°C

I_{IN} vs V_{IN}

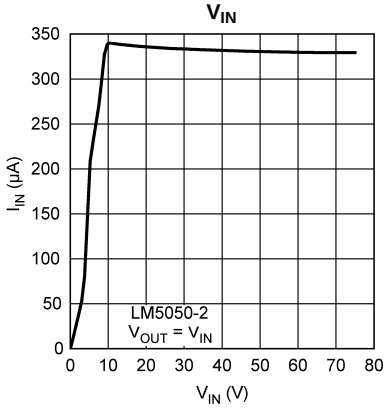


Figure 6.

I_{OUT} vs V_{OUT}

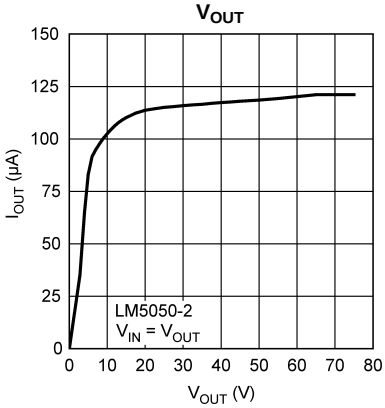


Figure 7.

V_{GATE} vs V_{IN}

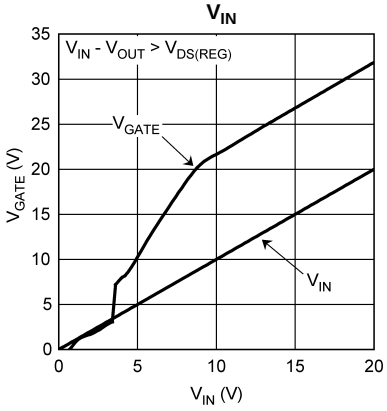


Figure 8.

V_{GS} vs V_{IN}

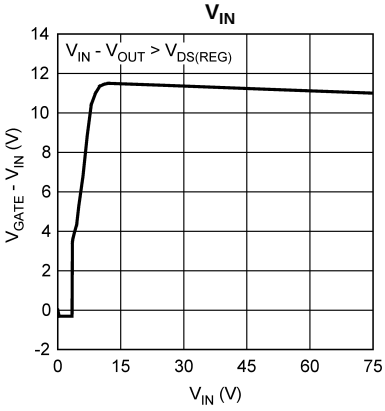


Figure 9.

V_{GS} vs Temperature

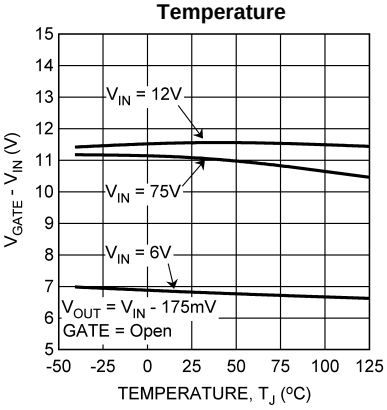


Figure 10.

Forward Gate Charge Time, C_{GATE} = 10 nF

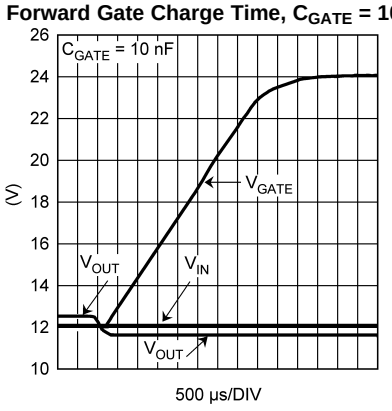


Figure 11.

Typical Performance Characteristics (continued)

Unless otherwise stated V_{IN} = 12V, V_{OFF} = 0.0V, and T_J = 25°C

Forward Gate Charge Time, C_{GATE} = 47 nF

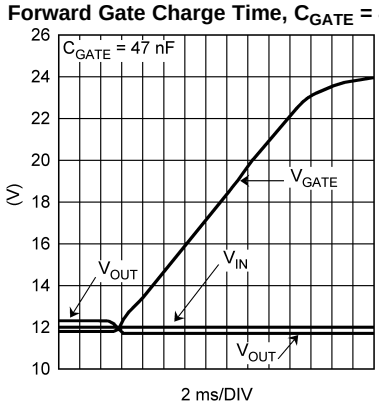


Figure 12.

Reverse C_{GATE} Discharge

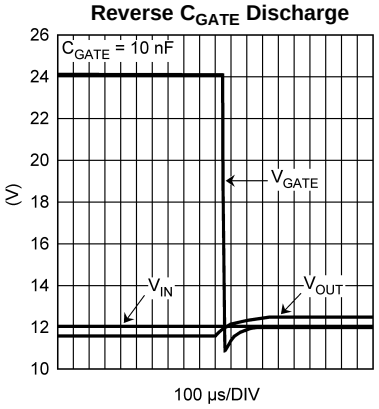


Figure .

$t_{GATE(REV)}$ vs Temperature

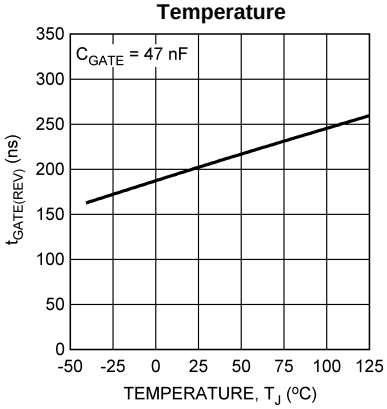


Figure 13.

OFF Pin Thresholds vs Temperature

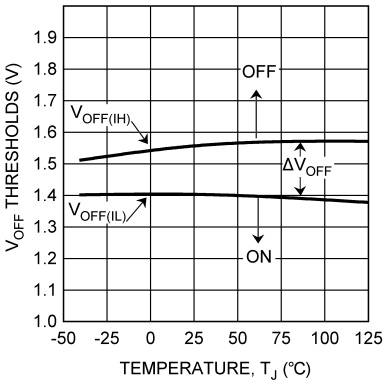


Figure 14.

OFF Pin Pull-Down vs V_{OUT}

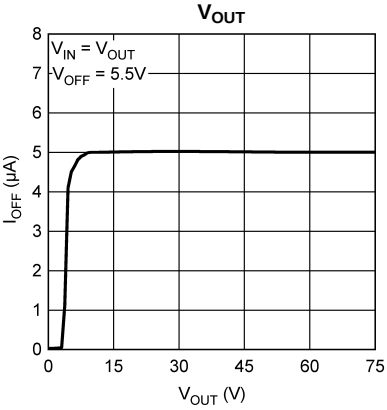


Figure 15.

C_{GATE} Charge and Discharge vs OFF Pin

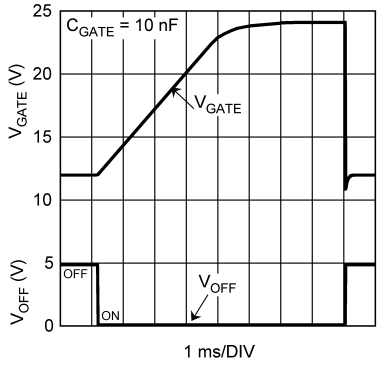


Figure 16.

Copyright © 2010–2013, Texas Instruments Incorporated

Typical Performance Characteristics (continued)

Unless otherwise stated V_{IN} = 12V, V_{OFF} = 0.0V, and T_J = 25°C

OFF Pin, On to Off Transition

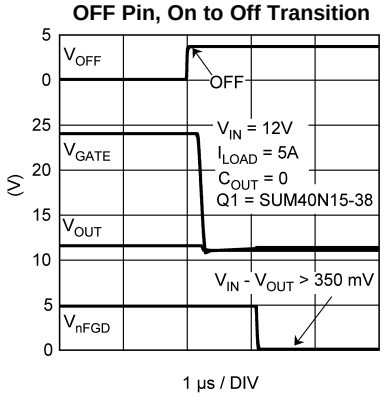


Figure 17.

OFF Pin, Off to On Transition

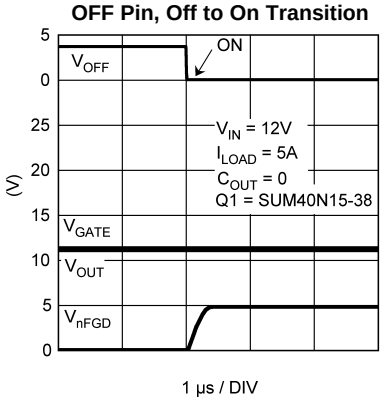


Figure .

GATE Pin vs ($R_{DS(ON)}$ x I_{DS})

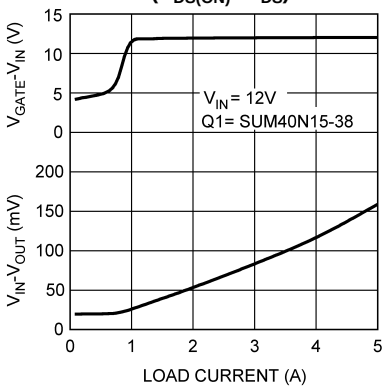
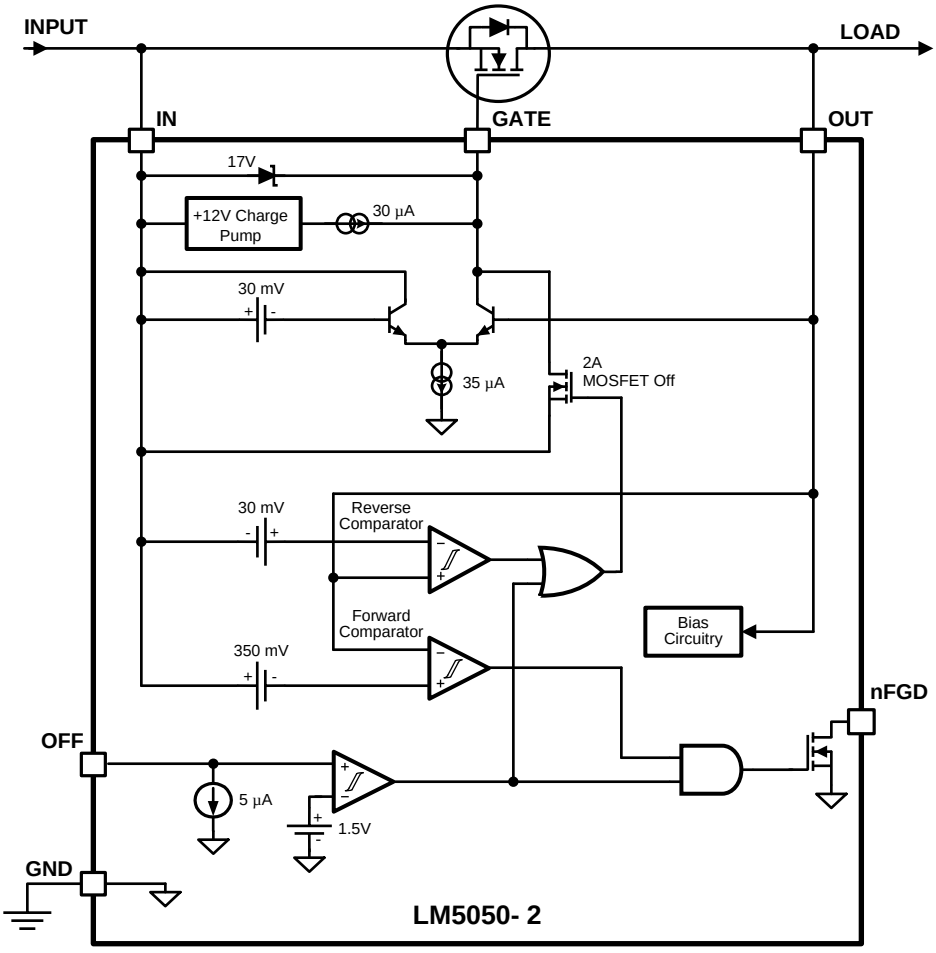


Figure 18.

BLOCK DIAGRAM



Copyright © 2010–2013, Texas Instruments Incorporated

APPLICATIONS INFORMATION

FUNCTIONAL DESCRIPTION

Systems that require high availability often use multiple, parallel-connected redundant power supplies to improve reliability. Schottky OR-ing diodes are typically used to connect these redundant power supplies to a common point at the load. The disadvantage of using OR-ing diodes is the forward voltage drop, which reduces the available voltage, and the associated power losses as load currents increase. Using an N-channel MOSFET to replace the OR-ing diode requires a small increase in the level of complexity, but reduces, or eliminates, the need for diode heat sinks or large thermal copper area in circuit board layouts for high power applications.

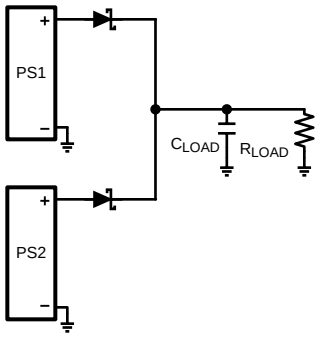


Figure 19. Traditional OR-ing with Diodes

The LM5050-2 is a positive voltage (i.e. high-side) OR-ing controller that will drive an external N-channel MOSFET to replace an OR-ing diode. The voltage across the MOSFET source and drain pins is monitored by the LM5050-2 at the IN and OUT pins, while the GATE pin drives the MOSFET to control its operation based on the monitored source-drain voltage. The resulting behavior is that of an ideal rectifier with source and drain pins of the MOSFET acting as the anode and cathode pins of a diode respectively.

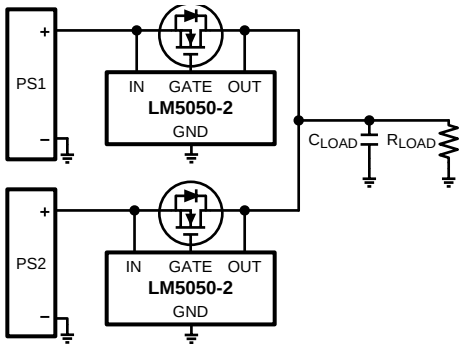


Figure 20. OR-ing with MOSFETs

IN, GATE AND OUT PINS

When power is initially applied, the load current will flow from source to drain through the body diode of the MOSFET. The resulting voltage across the body diode will be detected at the LM5050-2 IN and OUT pins which then begins charging the MOSFET gate through a 30 µA (typical) charge pump current source . In normal operation, the gate of the MOSFET is charged until it reaches typically 12V above the IN pin. With an IN pin voltage that is less than approximately 10V, the gate of the MOSFET is charged to typically twice the voltage on the IN pin.

The LM5050-2 is designed to regulate the MOSFET gate-to-source voltage if the voltage across the MOSFET source and drain pins falls below the $V_{SD(REG)}$ voltage of 27 mV (typical).

Copyright © 2010–2013, Texas Instruments Incorporated

If the MOSFET current decreases to the point that the voltage across the MOSFET falls below the $V_{SD(REG)}$ voltage regulation point of 27 mV (typical), the GATE pin voltage will be decreased until the voltage across the MOSFET is regulated at 27 mV. If the drain-to-source voltage is greater than $V_{SD(REG)}$ voltage the gate-to-source will increase, eventually reaching the 12V GATE to IN zener clamp level.

If the MOSFET current reverses, possibly due to failure of the input supply, such that the voltage across the LM5050-2 IN and OUT pins is more negative than the $V_{SD(REV)}$ voltage of -27 mV (typical), the LM5050-2 will quickly discharge the MOSFET gate through a strong GATE to IN pin discharge transistor.

If the input supply fails abruptly, as would occur if the supply was shorted directly to ground, a reverse current will temporarily flow through the MOSFET until the gate can be fully discharged. This reverse current is sourced from the output load capacitance and from the parallel connected supplies. The LM5050-2 responds to a voltage reversal condition typically within 27 ns. The actual time required to turn off the MOSFET will depend on the charge held by gate capacitance of the MOSFET being used. A MOSFET with 47 nF of effective gate capacitance can be turned off in typically 205 ns. This fast turn off time minimizes voltage disturbances at the output, as well as the current transients from the redundant supplies.

OFF PIN and nFGD PIN

The OFF pin is a logic level input pin that is used to control the gate drive to the external MOSFET in the FET Test Mode. The maximum operating voltage on this pin is 5.5V. The nFGD pin is an open drain output pin that supports a logic level voltage. The maximum operating voltage on this pin is 5.5V.

When the OFF pin is high, the MOSFET is turned off (independent of the sensed IN and OUT voltages) and the FET Test Mode is activated. In this mode, load current will flow through the body diode of the MOSFET. The voltage difference between the IN pin and OUT pins will be approximately 700 mV if the MOSFET is operating normally through the body diode. The FET test comparator of the LM5050-2 monitors the IN to OUT pin voltage difference with a $V_{SD(TST)}$ threshold of 350 mV (typical). If the IN pin to OUT pin voltage difference is greater than this threshold, the nFGD pin will switch to a low impedance state and the nFGD pin voltage will be at a logic low. If the MOSFET is shorted, the voltage difference between the IN pin and the OUT pin will be less than the $V_{SD(TST)}$ threshold. In this case, the nFGD pin will remain in a high impedance state and the pin voltage can be pulled high by an external pull-up resistor.

In normal operation the OFF pin must be pulled low (or left open). In this mode, the GATE pin voltage will depend upon the forward or reverse voltage across the MOSFET source to drain as previously described.

The OFF pin has an internal pull-down of 5 µA (typical). If the OFF function is not required, the pin may be left open or connected to ground.

While the OFF pin is low the nFGD pin will always be in a high impedance open state.

Several factors can prevent the nFGD pin from indicating that the external MOSFET is operating normally. If the LM5050-2 is used to connect parallel, redundant power supplies, one of the connected supplies may hold the OUT pin voltage close enough to the LM5050-2 IN pin voltage that the $V_{SD(TST)}$ threshold is not exceeded. Additionally, operating with a high output capacitance value and low load current may require a significant amount of time before the output capacitance is discharged to the point where the $V_{SD(TST)}$ threshold is exceeded and the nFGD pin switches low.

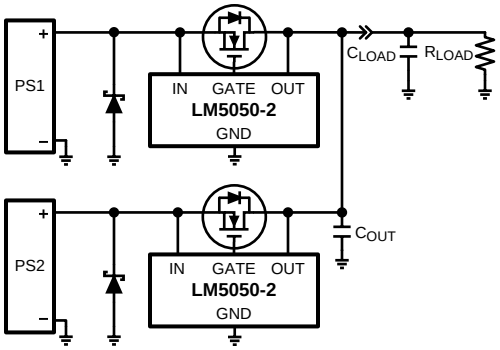


Figure 21. Typical Connection

Copyright © 2010–2013, Texas Instruments Incorporated

SHORT CIRCUIT FAILURE OF AN INPUT SUPPLY

An abrupt zero ohm short circuit across the input supply will cause the highest possible reverse current to flow while the internal LM5050-2 control circuitry discharges the gate of the MOSFET. During this time, the reverse current is limited only by the $R_{DS(ON)}$ of the MOSFET, along with parasitic wiring resistances and inductances. Worst case instantaneous reverse current would be limited to:

$$I_{D(REV)} = (V_{OUT} - V_{IN}) / R_{DS(ON)} \quad (1)$$

The internal Reverse Comparator will react, and will start the process of discharging the Gate, when the reverse current reaches:

$$I_{D(REV)} = V_{SD(REV)} / R_{DS(ON)} \quad (2)$$

When the MOSFET is finally switched off, the energy stored in the parasitic wiring inductances will be transferred to the rest of the circuit. As a result, the LM5050-2 IN pin will see a negative voltage spike while the OUT pin will see a positive voltage spike. The IN pin can be protected by diode clamping the pin to GND in the negative direction. The OUT pin can be protected with a TVS protection diode, a local bypass capacitor, or both. In low voltage applications, the MOSFET drain-to-source breakdown voltage rating may be adequate to protect the OUT pin (i.e. $V_{IN} + V_{(BR)DSS(MAX)} < 75V$), but most MOSFET datasheets do not specifiy the maximum breakdown rating, so this method should be used with caution.

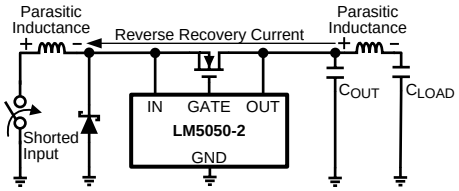


Figure 22. Input Supply Fault Transients

Table 1. FET Test Status Table

OFF Pin	Mode	FET Gate Drive	$V_{IN} - V_{OUT}$	FET Status	nFGD Pin Status	nFGD Pin Voltage
Low or Open	Normal Operation	Active	-	-	High Z	High
High	FET Test	Off	> $V_{SD(TST)}$	OK	Low Z	Low
			< $V_{SD(TST)}$	Not OK	High Z	High

MOSFET SELECTION

The important MOSFET electrical parameters are the maximum continuous Drain current I_D, the maximum Source current (i.e. body diode), the maximum drain-to-source voltage $V_{DS(MAX)}$, the gate-to-source threshold voltage $V_{GS(TH)}$, the drain-to-source reverse breakdown voltage $V_{(BR)DSS}$, and the drain-to-source On resistance $R_{DS(ON)}$.

The maximum continuous drain current, I_D, rating must be exceed the maximum continuous load current. The rating for the maximum current through the body diode, I_S, is typically rated the same as, or slightly higher than the drain current, but body diode current only flows while the MOSFET gate is being charged to $V_{GS(TH)}$:

$$\text{Gate Charge Time} = Q_g / I_{GATE(ON)} \quad (3)$$

The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. This would include any anticipated fault conditions.

The drain-to-source reverse breakdown voltage, $V_{(BR)DSS}$, may provide some transient protection to the OUT pin in low voltage applications by allowing conduction back to the IN pin during positive transients at the OUT pin.

The gate-to-source threshold voltage, $V_{GS(TH)}$, should be compatible with the LM5050 gate drive capabilities. Logic level MOSFETs are recommended, but sub-Logic level MOSFETs can also be used.

Copyright © 2010–2013, Texas Instruments Incorporated

The dominate MOSFET loss for the LM5050 active OR-ing controller is conduction loss due to source-to-drain current to the output load, and the $R_{DS(ON)}$ of the MOSFET. This conduction loss could be reduced by using a MOSFET with the lowest possible $R_{DS(ON)}$. However, contrary to popular belief, arbitrarily selecting a MOSFET based solely on having low $R_{DS(ON)}$ may not always give desirable results for several reasons:

1) Reverse transition detection. Higher $R_{DS(ON)}$ will provide increased voltage information to the LM5050 Reverse Comparator at a lower reverse current level. This will give an earlier MOSFET turn-off condition should the input voltage become shorted to ground. This will minimize any disturbance of the redundant bus.

2) Reverse current leakage. In cases where multiple input supplies are closely matched it may be possible for some small current to flow continuously through the MOSFET drain to source (i.e. reverse) without activating the LM5050 Reverse Comparator. Higher $R_{DS(ON)}$ will reduce this reverse current level.

3) Cost. Generally, as the $R_{DS(ON)}$ rating goes lower, the cost of the MOSFET goes higher.

Selecting a MOSFET with an $R_{DS(ON)}$ that is too large will result in excessive power dissipation. Additionally, the MOSFET gate will be charged to the full value that the LM5050 can provide as it attempts to drive the Drain to Source voltage down to the $V_{SD(REG)}$ of 20 mV typical. This increased Gate charge will require some finite amount of additional discharge time when the MOSFET needs to be turned off.

As a guideline, it is suggest that $R_{DS(ON)}$ be selected to provide at least 20 mV, and no more than 100 mV, at the nominal load current.

$$(20\ mV / I_D) \le R_{DS(ON)} \le (100mV / I_D) \quad (4)$$

The thermal resistance of the MOSFET package should also be considered against the anticipated dissipation in the MOSFET in order to ensure that the junction temperature (T_J) is reasonably well controlled, since the $R_{DS(ON)}$ of the MOSFET increases as the junction temperature increases.

$$P_{DISS} = I_D^2 \times (R_{DS(ON)}) \quad (5)$$

Operating with a maximum ambient temperature ($T_{A(MAX)}$) of 35°C, a load current of 10A, and an $R_{DS(ON)}$ of 10 mΩ, and desiring to keep the junction temperature under 100°C, the maximum junction-to-ambient thermal resistance rating (θ_{JA}) would need to be:

$$\theta_{JA} \le (T_{J(MAX)} - T_{A(MAX)})/(I_D^2 \times R_{DS(ON)}) \quad (6)$$

$$\theta_{JA} \le (100°C - 35°C)/(10A \times 10A \times 0.01\Omega) \quad (7)$$

$$\theta_{JA} \le 65°C/W \quad (8)$$

Copyright © 2010–2013, Texas Instruments Incorporated

TYPICAL APPLICATIONS

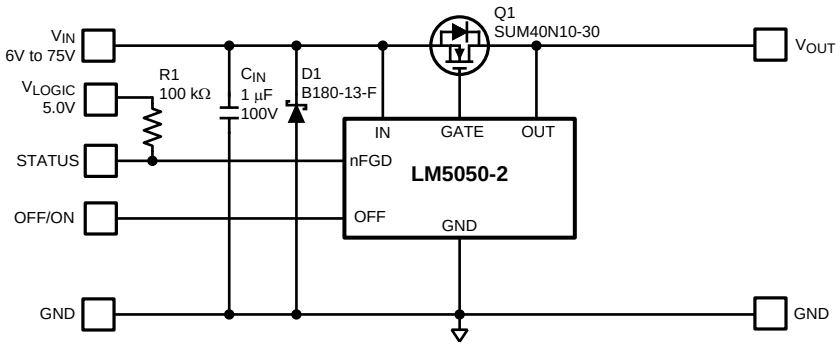


Figure 23. Basic Application with Input Transient Protection

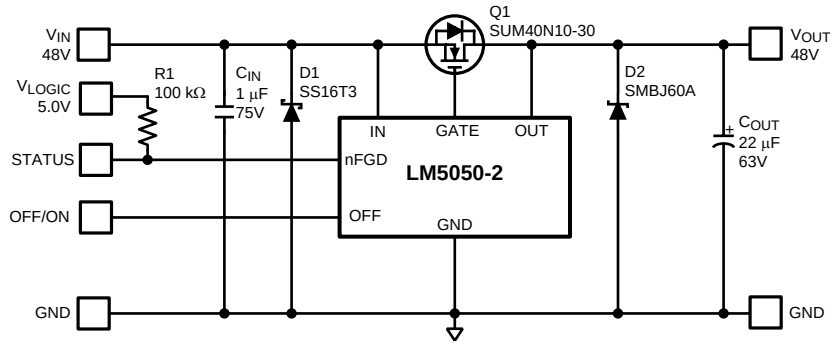


Figure 24. Typical +48V Application with Transient Protection

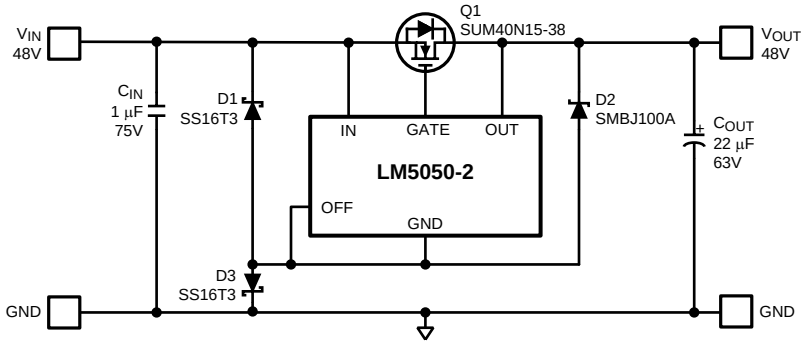


Figure 25. +48V Application with Reversed Input Voltage (V_{IN} = -48V) Protection

REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	15

Copyright © 2010–2013, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5050MK-2/NOPB	ACTIVE	SOT-23-THIN	DDC	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SZJB	Samples
LM5050MKX-2/NOPB	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SZJB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

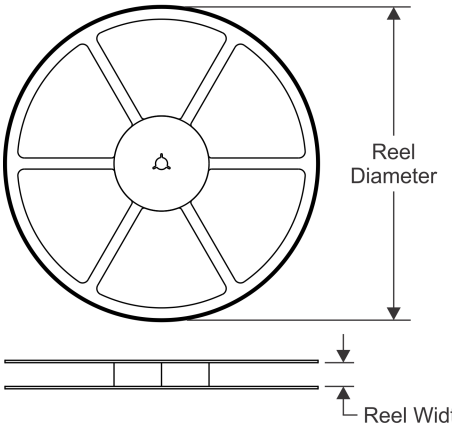
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

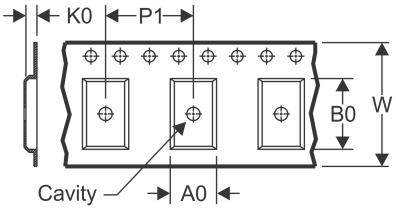
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

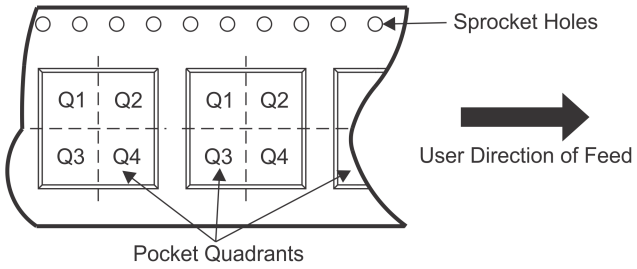


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

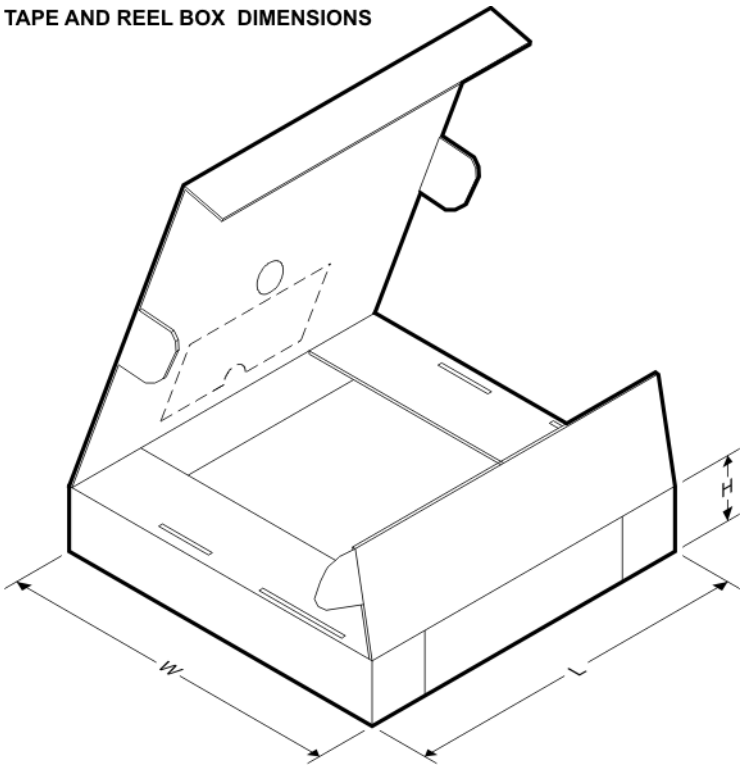
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5050MK-2/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM5050MKX-2/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

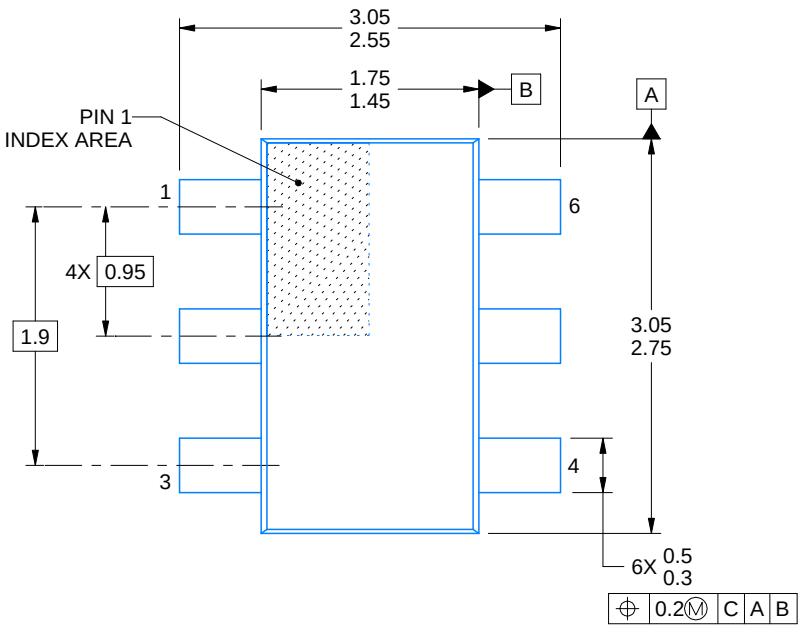
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5050MK-2/NOPB	SOT-23-THIN	DDC	6	1000	208.0	191.0	35.0
LM5050MKX-2/NOPB	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0

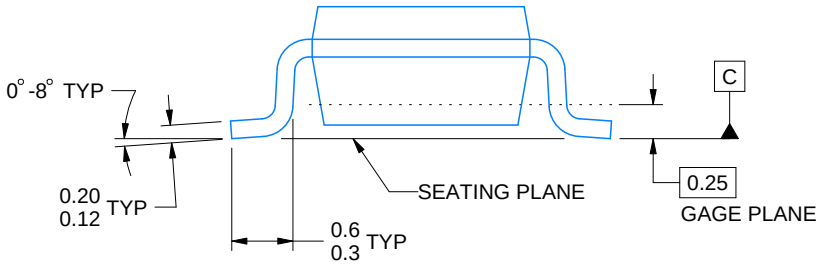
PACKAGE OUTLINE

DDC0006A

SOT - 1.1 max height

SOT

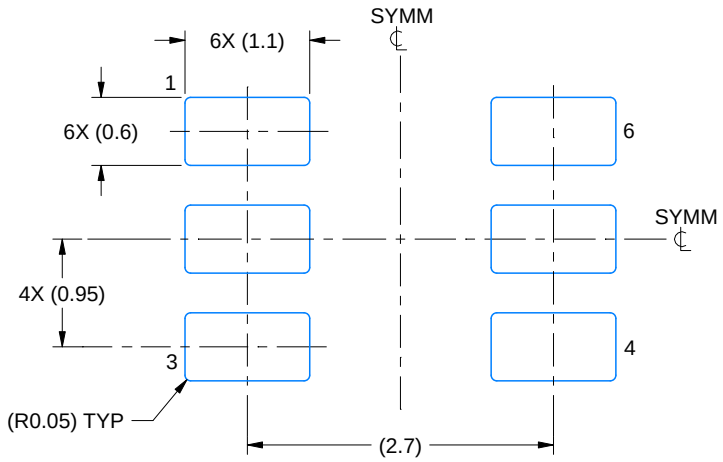




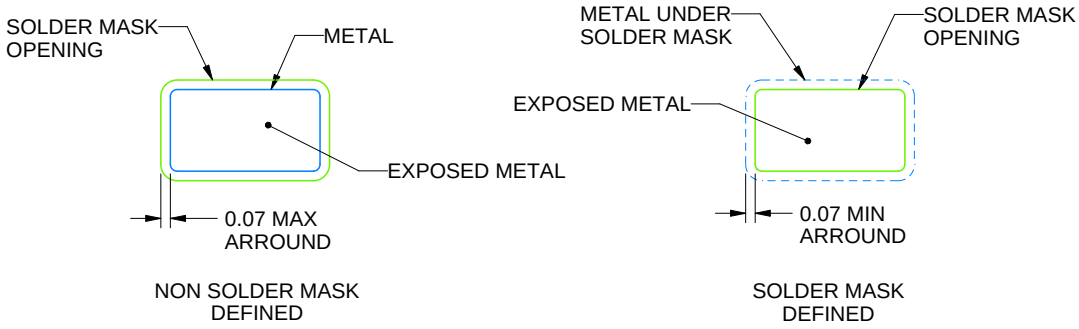
4214841/B 11/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

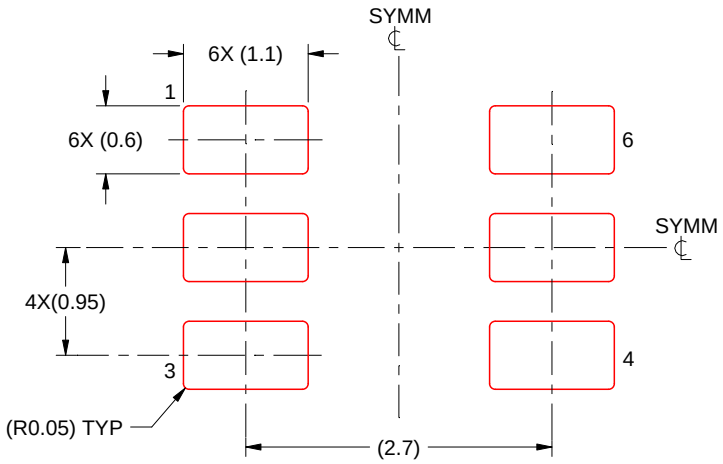


SOLDERMASK DETAILS

4214841/B 11/2020

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/B 11/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021, Texas Instruments Incorporated