LM5642/LM5642X High Voltage, Dual Synchronous Buck Converter with Oscillator Synchronization

Check for Samples: LM5642, LM5642X

FEATURES

- **Two Synchronous Buck Regulators**
- **180° Out of Phase Operation**
- **200 kHz Fixed Nominal Frequency: LM5642**
- **375 kHz Fixed Nominal Frequency: LM5642X**
- **Synchronizable Switching Frequency from 150 kHz to 250 kHz for the LM5642 and 200 kHz to 500 kHz for the LM5642X**
- **4.5V to 36V Input Range**
- **50 µA Shutdown Current**
- **Adjustable Output from 1.3V to 90% of Vin**
- **0.04% (Typical) Line and Load Regulation Accuracy**
- **Current Mode Control with or without a Sense Resistor**
- **Independent Enable/Soft-start Pins Allow Simple Sequential Startup Configuration.**
- **Configurable for Single Output Parallel Operation. (See Figure 4)**
- **Adjustable Cycle-by-cycle Current Limit**
- **Input Under-voltage Lockout**
- **Output Over-voltage Latch Protection**
- **Output Under-voltage Protection with Delay**
- **Thermal Shutdown**
- **Self Discharge of Output Capacitors when the Regulator is OFF**
- **TSSOP and HTSSOP (Exposed PAD) Packages**

APPLICATIONS

- **Embedded Computer Systems**
- **Navigation Systems**
- **Telecom Systems**
- **Set-Top Boxes**
- **WebPAD**
- **Point Of Load Power Architectures**

DESCRIPTION

The LM5642 series consists of two current mode synchronous buck regulator controllers operating 180° out of phase with each other at a normal switching frequency of 200kHz for the LM5642 and at 375kHz for the LM5642X.

Out of phase operation reduces the input RMS ripple current, thereby significantly reducing the required input capacitance. The switching frequency can be synchronized to an external clock between 150 kHz and 250 kHz for the LM5642 and between 200 kHz and 500 kHz for the LM5642X. The two switching regulator outputs can also be paralleled to operate as a dual-phase, single output regulator.

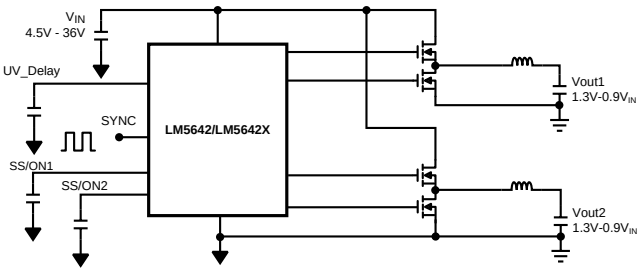
The output of each channel can be independently adjusted from 1.3V to 90% of Vin. An internal 5V rail is also available externally for driving bootstrap circuitry.

Current-mode feedback control assures excellent line and load regulation and wide loop bandwidth for excellent response to fast load transients. Current is sensed across either the Vds of the top FET or across an external current-sense resistor connected in series with the drain of the top FET.

The LM5642 features analog soft-start circuitry that is independent of the output load and output capacitance making the soft-start behavior more predictable and controllable than traditional soft-start circuits.

Over-voltage protection is available for both outputs. A UV-Delay pin is also available to allow delayed shut off time for the IC during an output under-voltage event.

Typical Application Circuit



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Connection Diagram

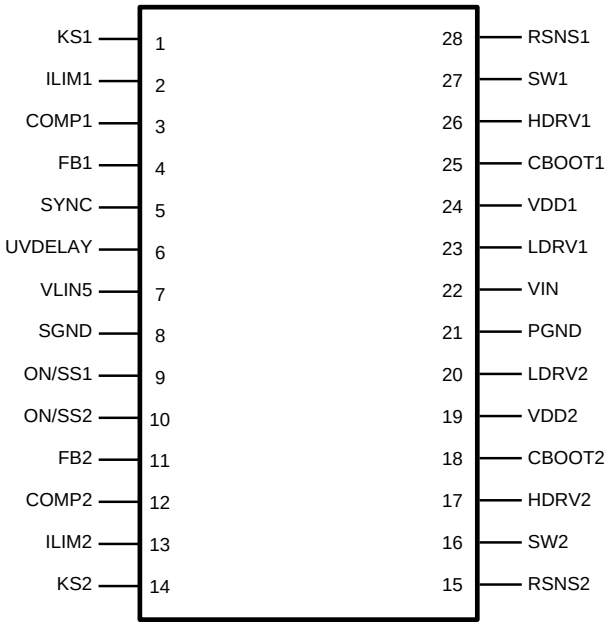

Figure 1. Top View

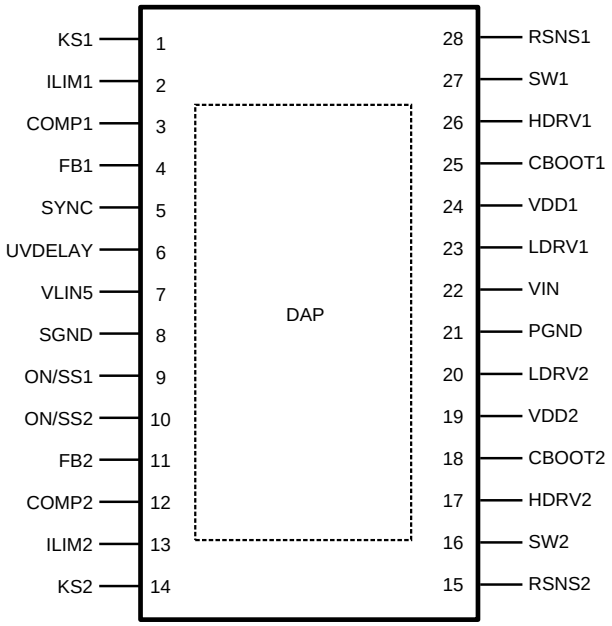

Figure 2. Top View

PIN DESCRIPTIONS

KS1 (Pin 1)	The positive (+) Kelvin sense for the internal current sense amplifier of Channel 1. Use a separate trace to connect this pin to the current-sense point. It should be connected to VIN as close as possible to the current-sense resistor. When no current-sense resistor is used, connect as close as possible to the drain node of the upper MOSFET.
ILIM1 (Pin 2)	Current limit threshold setting for Channel 1. It sinks a constant current of 9.9 µA, which is converted to a voltage across a resistor connected from this pin to VIN. The voltage across the resistor is compared with either the V_{DS} of the top MOSFET or the voltage across the external current sense resistor to determine if an over-current condition has occurred in Channel 1.
COMP1 (Pin 3)	Compensation pin for Channel 1. This is the output of the internal transconductance error amplifier. The loop compensation network should be connected between this pin and the signal ground, SGND (Pin 8).
FB1 (Pin 4)	Feedback input for channel 1. Connect to VOUT through a voltage divider to set the Channel 1 output voltage.
SYNC (Pin 5)	The switching frequency of the LM5642 can be synchronized to an external clock. **SYNC = LOW:** Free running at 200 kHz for LM5642, and at 375kHz for LM5642X. Channels are 180° out of phase. **SYNC = HIGH:** Waiting for external clock **SYNC = Falling Edge:** Channel 1 HDRV pin goes high. Channel 2 HDRV pin goes high after 2.5 µs delay. The maximum SYNC pulse width must be greater than 100 ns. For SYNC = Low operation, connect this pin to signal ground through a 220 kΩ resistor.
UV_DELAY (Pin 6)	A capacitor from this pin to ground sets the delay time for UVP. The capacitor is charged from a 5 µA current source. When UV_DELAY charges to 2.3V (typical), the system immediately latches off. Connecting this pin to ground will disable the output under-voltage protection.
VLIN5 (Pin 7)	The output of an internal 5V LDO regulator derived from VIN. It supplies the internal bias for the chip and powers the bootstrap circuitry for gate drive. Bypass this pin to signal ground with a minimum of 4.7 µF ceramic capacitor.
SGND (Pin 8)	The ground connection for the signal-level circuitry. It should be connected to the ground rail of the system.
ON/SS1 (Pin 9)	Channel 1 enable pin. This pin is internally pulled up to one diode drop above VLIN5. Pulling this pin below 1.2V (open-collector type) turns off Channel 1. If both ON/SS1 and ON/SS2 pins are pulled below 1.2V, the whole chip goes into *shut down mode*. Adding a capacitor to this pin provides a soft-start feature that minimizes inrush current and output voltage overshoot.
ON/SS2 (Pin 10)	Channel 2 enable pin. See the description for Pin 9, ON/SS1. May be connected to ON/SS1 for simultaneous startup or for parallel operation.
FB2 (Pin 11)	Feedback input for channel 2. Connect to VOUT through a voltage divider to set the Channel 2 output voltage.

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PIN DESCRIPTIONS (continued)

COMP2 (Pin 12)	Compensation pin for Channel 2. This is the output of the internal transconductance error amplifier. The loop compensation network should be connected between this pin and the signal ground SGND (Pin 8).
ILIM2 (Pin 13)	Current limit threshold setting for Channel 2. See ILIM1 (Pin 2).
KS2 (Pin 14)	The positive (+) Kelvin sense for the internal current sense amplifier of Channel 2. See KS1 (Pin 1).
RSNS2 (Pin 15)	The negative (-) Kelvin sense for the internal current sense amplifier of Channel 2. Connect this pin to the low side of the current sense resistor that is placed between VIN and the drain of the top MOSFET. When the Rds of the top MOSFET is used for current sensing, connect this pin to the source of the top MOSFET. Always use a separate trace to form a Kelvin connection to this pin.
SW2 (Pin 16)	Switch-node connection for Channel 2, which is connected to the source of the top MOSFET of Channel 2. It serves as the negative supply rail for the top-side gate driver, HDRV2.
HDRV2 (Pin 17)	Top-side gate-drive output for Channel 2. HDRV is a floating drive output that rides on the corresponding switching-node voltage.
CBOOT2 (Pin 18)	Bootstrap capacitor connection. It serves as the positive supply rail for the Channel 2 top-side gate drive. Connect this pin to VDD2 (Pin 19) through a diode, and connect the low side of the bootstrap capacitor to SW2 (Pin16).
VDD2 (Pin 19)	The supply rail for the Channel 2 low-side gate drive. Connected to VLIN5 (Pin 7) through a 4.7Ω resistor and bypassed to power ground with a ceramic capacitor of at least 1μF. Tie this pin to VDD1 (Pin 24).
LDRV2 (Pin 20)	Low-side gate-drive output for Channel 2.
PGND (Pin 21)	The power ground connection for both channels. Connect to the ground rail of the system.
VIN (Pin 22)	The power input pin for the chip. Connect to the positive (+) input rail of the system. This pin must be connected to the same voltage rail as the top FET drain (or the current sense resistor when used).
LDRV1 (Pin 23)	Low-side gate-drive output for Channel 1.
VDD1 (Pin 24)	The supply rail for Channel 1 low-side gate drive. Tie this pin to VDD2 (Pin 19).
CBOOT1 (Pin 25)	Bootstrap capacitor connection. This pin serves as the positive supply rail for the Channel 1 top-side gate drive. See CBOOT2 (Pin 18).
HDRV1 (Pin 26)	Top-side gate-drive output for Channel 1. See HDRV2 (Pin 17).
SW1 (Pin 27)	Switch-node connection for Channel 1. See SW2 (Pin16).
RSNS1 (Pin 28)	The negative (-) Kelvin sense for the internal current sense amplifier of Channel 1. See RSNS2 (Pin 15).
PGND (DAP)	The power ground connection for both channels. Connect to the ground rail of the system. Use of multiple vias to internal ground plane or GND layer helps to dissipate heat generated by output power.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS[1][2]

Voltages from the indicated pins to SGND/PGND:		
VIN, ILIM1, ILIM2, KS1, KS2		−0.3V to 38V
SW1, SW2, RSNS1, RSNS2		−0.3 to (V_{IN} + 0.3)V
FB1, FB2, VDD1, VDD2		−0.3V to 6V
SYNC, COMP1, COMP2, UV Delay		−0.3V to (VLIN5 +0.3)V
ON/SS1, ON/SS2 [3]		−0.3V to (VLIN5 +0.6)V
CBOOT1, CBOOT2		43V
CBOOT1 to SW1, CBOOT2 to SW2		−0.3V to 7V
LDRV1, LDRV2		−0.3V to (VDD+0.3)V
HDRV1 to SW1, HDRV2 to SW2		−0.3V
HDRV1 to CBOOT1, HDRV2 to CBOOT2		+0.3V
Power Dissipation (T_A = 25°C)[4]		
TSSOP		1.1W
HTSSOP		3.4W
Ambient Storage Temp. Range		−65°C to +150°C
Soldering Dwell Time, Temp.[5]	Wave	4 sec, 260°C
	Infrared	10sec, 240°C
	Vapor Phase	75sec, 219°C
ESD Rating [6]		2kV

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Range indicates conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) ON/SS1 and ON/SS2 are internally pulled up to one diode drop above VLIN5. Do not apply an external pull-up voltage to these pins. It may cause damage to the IC.
(4) The maximum allowable power dissipation is calculated by using $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$, where T_{JMAX} is the maximum junction temperature, T_A is the ambient temperature and θ_{JA} is the junction-to-ambient thermal resistance of the specified package. The power dissipation ratings results from using 125°C, 25°C, and 90.6°C/W for T_{JMAX}, T_A, and θ_{JA} respectively. A θ_{JA} of 90.6°C/W represents the worst-case condition of no heat sinking of the 28-pin TSSOP. The HTSSOP package has a θ_{JA} of 29°C/W. The HTSSOP package thermal ratings results from the IC being mounted on a 4 layer JEDEC standard board using the same temperature conditions as the TSSOP package above. A thermal shutdown will occur if the temperature exceeds the maximum junction temperature of the device.
(5) See http://www.ti.com for other methods of soldering plastic small-outline packages.
(6) For testing purposes, ESD was applied using the human-body model, a 100pF capacitor discharged through a 1.5 kΩ resistor.

OPERATING RATINGS [1]

VIN (VLIN5 tied to VIN)	4.5V to 5.5V
VIN (VIN and VLIN5 separate)	5.5V to 36V
Junction Temperature	−40°C to +125°C

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Range indicates conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

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ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = 28V, GND = PGND = 0V, VLIN5 = VDD1 = VDD2. Limits appearing in **boldface** type apply over the specified operating junction temperature range, (-40°C to +125°C, if not otherwise specified). Specifications appearing in plain type are measured using low duty cycle pulse testing with T_A = 25°C (1), (2). Min/Max limits are specified by design, test, or statistical analysis.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
System						
$\Delta V_{OUT}/V_{OUT}$	Load Regulation	VIN = 28V, V_{compx} = 0.5V to 1.5V		0.04		%
	Line Regulation	5.5V ≤ VIN ≤ 36V, V_{compx} =1.25V		0.04		%
V_{FB1_FB2}	Feedback Voltage	5.5V ≤ VIN ≤ 36V	**1.2154**	1.2364	**1.2574**	V
		-20°C to 85°C	**1.2179**	1.2364	**1.2549**	
I_{VIN}	Input Supply Current	V_{ON_SSx} > 2V 5.5V ≤ VIN ≤ 36V		1.1	**2.0**	mA
		Shutdown (3) V_{ON_SS1} = V_{ON_SS2}= 0V		50	**110**	µA
VLIN5	VLIN5 Output Voltage	IVLIN5 = 0 to 25mA, 5.5V ≤ VIN ≤ 36V	**4.70**	5	**5.30**	V
V_{CLos}	Current Limit Comparator Offset (VILIMX −VRSNSX)	V_{IN} = 6V		±2	±7.0	mV
I_{CL}	Current Limit Sink Current		**8.4**	9.9	**11.4**	µA
I_{ss_SC1}, I_{ss_SC2}	Soft-Start Source Current	V_{ON_ss1} = V_{ON_ss2} = 1.5V (on)	**0.5**	2.4	**5.0**	µA
I_{ss_SK1}, I_{ss_SK2}	Soft-Start Sink Current	V_{ON_ss1} = V_{ON_ss2} = 1.5V	**2**	5.5	**10**	µA
V_{ON_SS1}, V_{ON_SS2}	Soft-Start On Threshold		**0.7**	1.12	**1.4**	V
V_{SSTO}	Soft-Start Timeout Threshold	(4)		3.4		V
$I_{sc_uvdelay}$	UV_DELAY Source Current	UV-DELAY = 2V	**2**	5	**9**	µA
$I_{sk_uvdelay}$	UV_DELAY Sink Current	UV-DELAY = 0.4V	**0.2**	0.48	**1.2**	mA
$V_{UVDelay}$	UV_DELAY Threshold Voltage			2.3		V
V_{UVP}	FB1, FB2, Under Voltage Protection Latch Threshold	As a percentage of nominal output voltage (falling edge)	**75**	80.7	**86**	%
	Hysteresis			3.7		%
V_{OVP}	V_{OUT} Overvoltage Shutdown Latch Threshold	As a percentage measured at V_{FB1}, V_{FB2}	**107**	114	**122**	%
S_{wx_R}	SW1, SW2 ON-Resistance	V_{SW1} = V_{SW2} = 0.4V	420	487	560	Ω

(1) A typical is the center of characterization data measured with low duty cycle pulse tsting at T_A = 25°C. Typicals are not ensured.
(2) All limits are specified. All electrical characteristics having room-temperature limits are tested during production with T_A = T_J = 25°C. All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) Both switching controllers are off. The linear regulator VLIN5 remains on.
(4) When SS1 and SS2 pins are charged above this voltage and either of the output voltages at Vout1 or Vout2 is still below the regulation limit, the under voltage protection feature is initialized.

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ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified, V_{IN} = 28V, GND = PGND = 0V, VLIN5 = VDD1 = VDD2. Limits appearing in **boldface** type apply over the specified operating junction temperature range, (-40°C to +125°C, if not otherwise specified). Specifications appearing in plain type are measured using low duty cycle pulse testing with T_A = 25°C (1), (2). Min/Max limits are specified by design, test, or statistical analysis.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Gate Drive						
I_{CBOOT}	CBOOTx Leakage Current	V_{CBOOT1} = V_{CBOOT2} = 7V		10		nA
I_{SC_DRV}	HDRVx and LDRVx Source Current	V_{CBOOT1} = V_{CBOOT2} = 5V, VSWx=0V, HDRVx=LDRVx=2.5V		0.5		A
I_{sk_HDRV}	HDRVx Sink Current	V_{CBOOTx} = VDDx = 5V, V_{SWx} = 0V, HDRVX = 2.5V		0.8		A
I_{sk_LDRV}	LDRVx Sink Current	V_{CBOOTx} = VDDx = 5V, V_{SWx} = 0V, LDRVX = 2.5V		1.1		A
R_{HDRV}	HDRV1 & 2 Source On-Resistance	V_{CBOOT1} = V_{CBOOT2} = 5V, V_{SW1} = V_{SW2} = 0V		3.1		Ω
	HDRV1 & 2 Sink On-Resistance			1.5		Ω
R_{LDRV}	LDRV1 & 2 Source On-Resistance	V_{CBOOT1} = V_{CBOOT2} = 5V, V_{SW1} = V_{SW2} = 0V V_{DD1} = V_{DD1} = 5V		3.1		Ω
	LDRV1 & 2 Sink On-Resistance			1.1		Ω
Oscillator and Sync Controls						
F_{osc}	Oscillator Frequency	5.5 ≤ V_{IN} ≤ 36V, LM5642	**166**	200	**226**	kHz
		5.5 ≤ V_{IN} ≤ 36V, LM5642X	**311**	375	**424**	
Don_max	Maximum On-Duty Cycle	V_{FB1} = V_{FB2} = 1V, Measured at pins HDRV1 and HDRV2	**96**	98.9		%
T_{on_min}	Minimum On-Time			166		ns
SS_{OT_delta}	HDRV1 and HDRV2 Delta On Time	ON/SS1 = ON/SS2 = 2V		20	250	ns
V_{HS}	SYNC Pin Min High Input		**2**	1.52		V
V_{LS}	SYNC Pin Max Low Input			1.44	**0.8**	V
Error Amplifier						
I_{FB1}, I_{FB2}	Feedback Input Bias Current	V_{FB1_FIX} = 1.5V, V_{FB2_FIX} = 1.5V		80	**±200**	nA
I_{comp1_SC}, I_{comp2_SC}	COMP Output Source Current	V_{FB1_FIX} = V_{FB2_FIX} = 1V, V_{COMP1} = V_{COMP2} = 1V	**6**	127		µA
		-20°C to 85°C	**18**			
I_{comp1_SK}, I_{comp2_SK}	COMP Output Sink Current	V_{FB1_FIX} = V_{FB2_FIX} = 1.5V and V_{COMP1} = V_{COMP2} = 0.5V	**6**	118		µA
		-20°C to 85°C	**18**			
gm1, gm2	Transconductance			720		µmho
GI_{SNS1}, GI_{SNS2}	Current Sense Amplifier (1&2) Gain	V_{COMPx} = 1.25V	4.2	5.2	7.5	
Voltage References and Linear Voltage Regulators						
UVLO	VLIN5 Under-voltage Lockout Threshold Rising	ON/SS1, ON/SS2 transition from low to high	**3.6**	4.0	**4.4**	V

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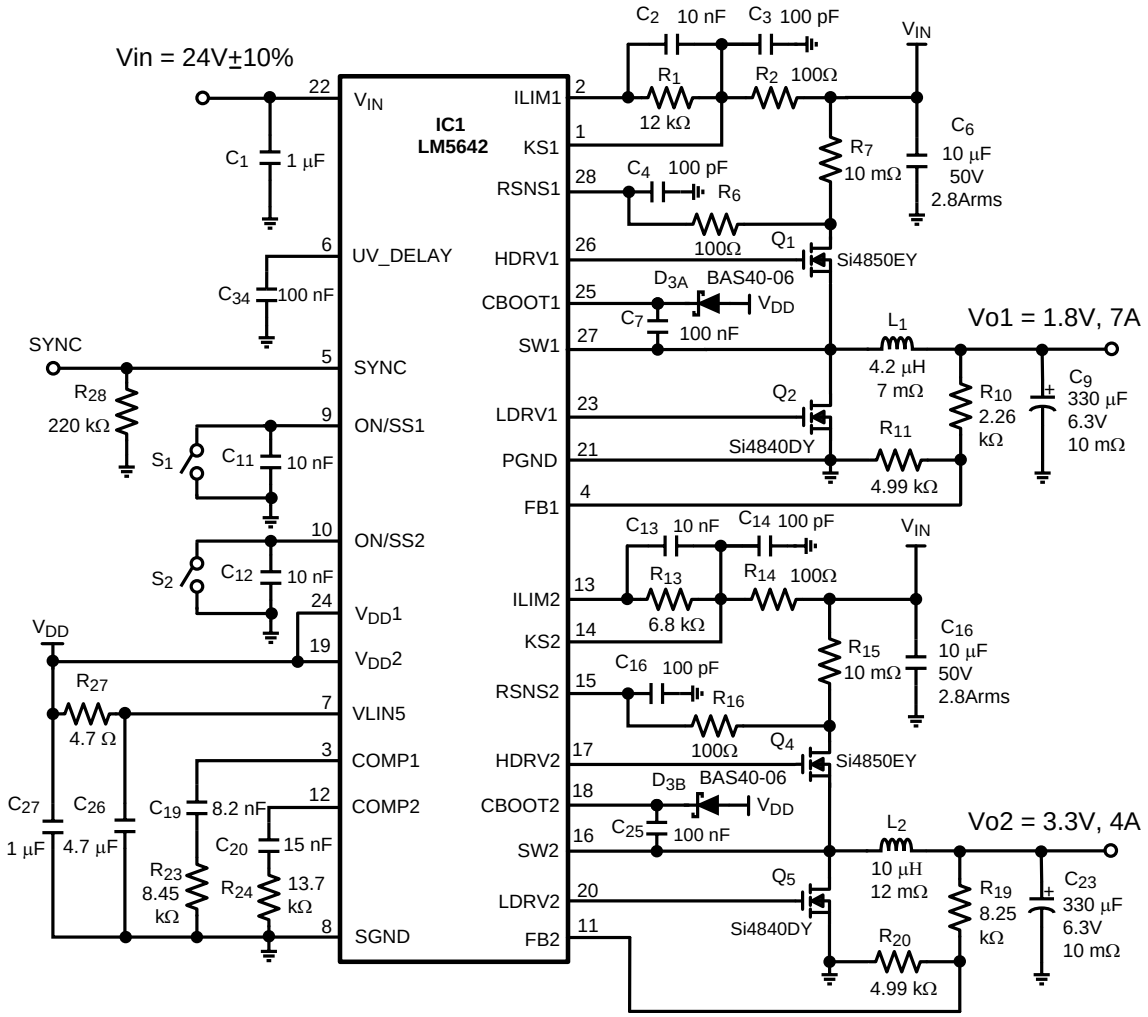

Figure 3. Typical 2 Channel Application Circuit

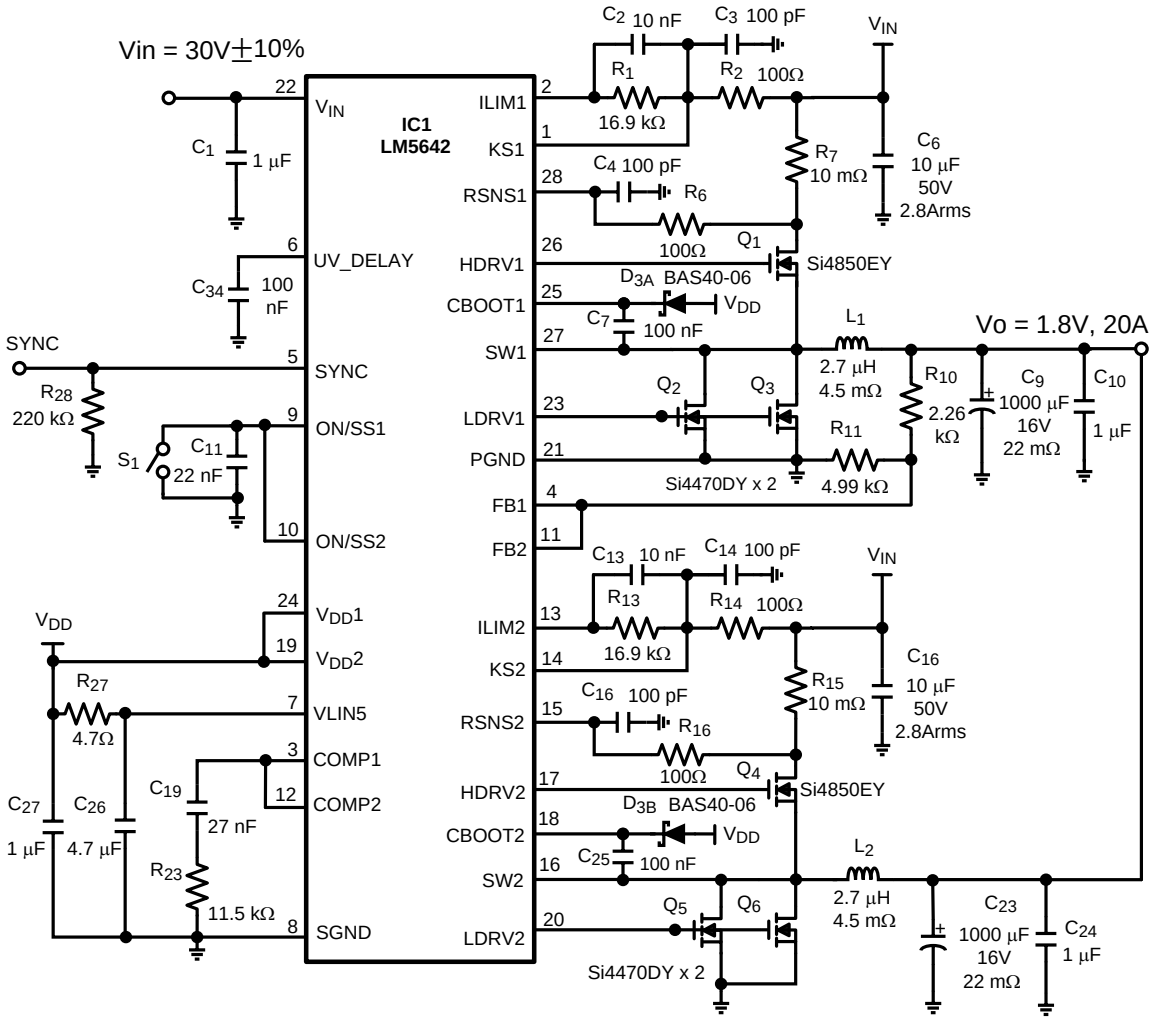

Figure 4. Typical Single Channel Application Circuit

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BLOCK DIAGRAM

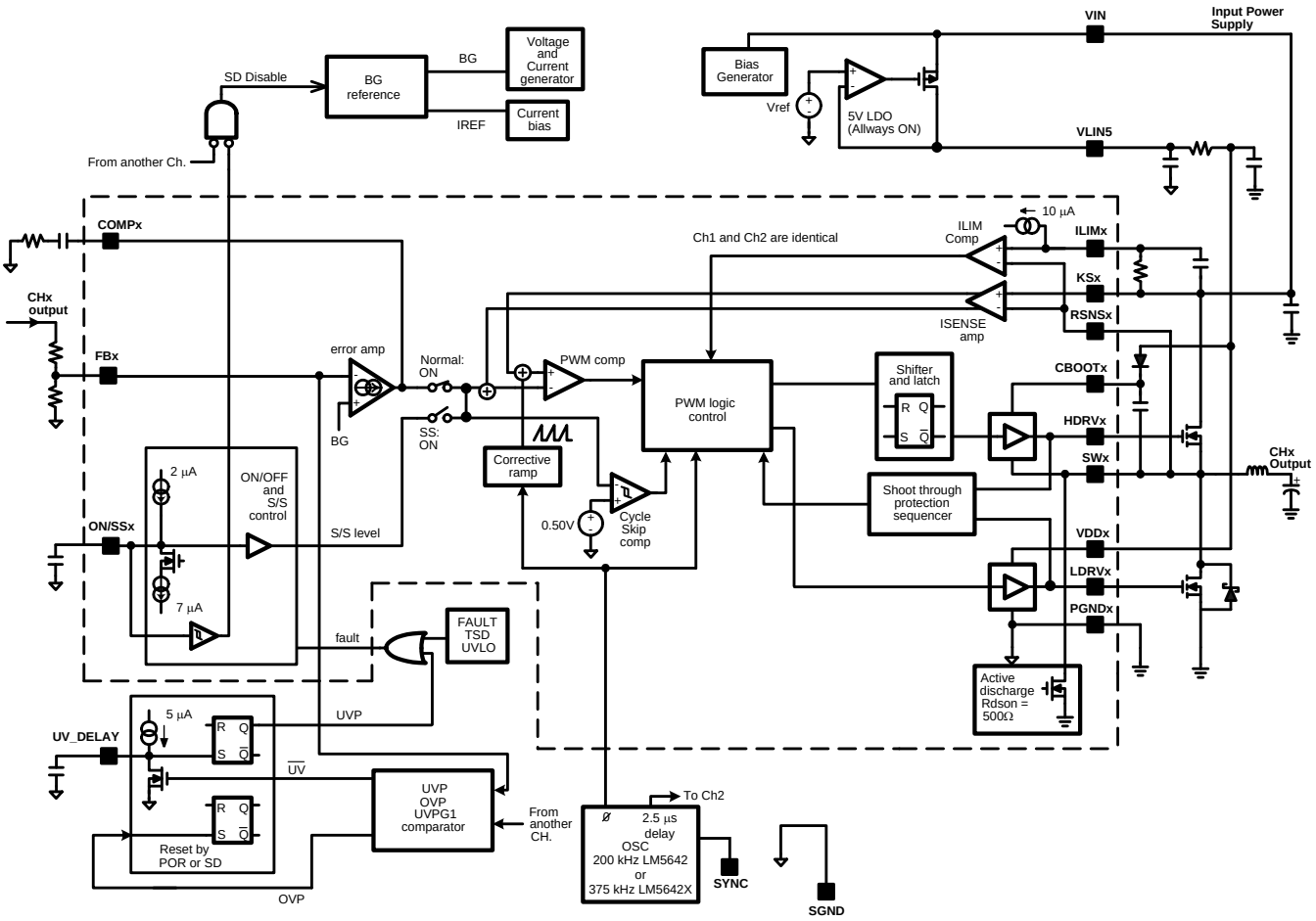
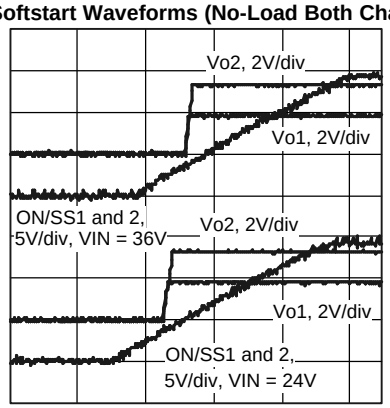


Figure 5. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

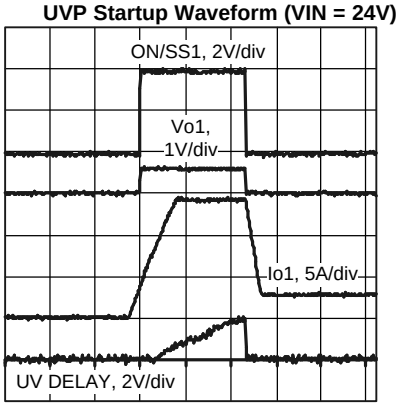
Softstart Waveforms (No-Load Both Channels)



4 ms/DIV

Figure 6.

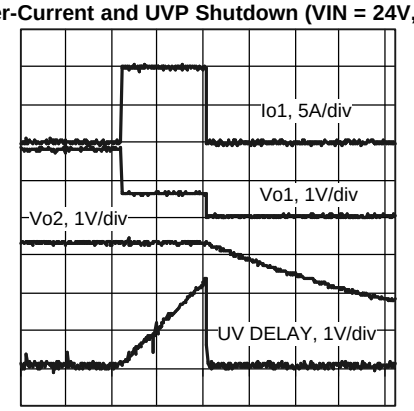
UVP Startup Waveform (VIN = 24V)



20ms/DIV

Figure 7.

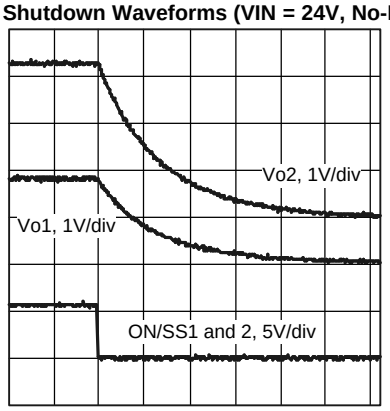
Over-Current and UVP Shutdown (VIN = 24V, Io2 = 0A)



20ms/DIV

Figure 8.

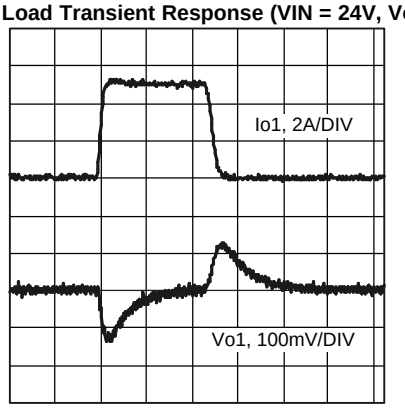
Shutdown Waveforms (VIN = 24V, No-Load)



100ms/DIV

Figure 9.

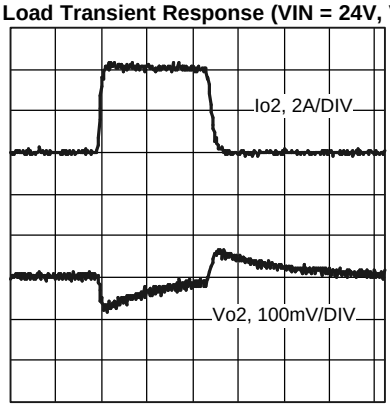
Ch.1 Load Transient Response (VIN = 24V, Vo1 = 1.8V)



100µs/DIV

Figure 10.

Ch.2 Load Transient Response (VIN = 24V, Vo2 = 3.3V)



100µs/DIV

Figure 11.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Ch. 2 Load Transient Response (VIN = 36V, Vo2 = 3.3V)

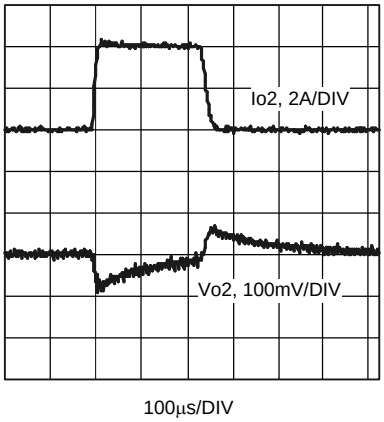

Figure 12.

Ch.1 Load Transient Response (VIN = 36V, Vo1 = 1.8V)

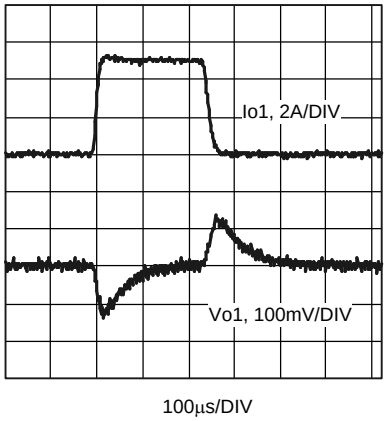

Figure 13.

Input Supply Current vs Temperature (Shutdown Mode V_{IN} = 28V)

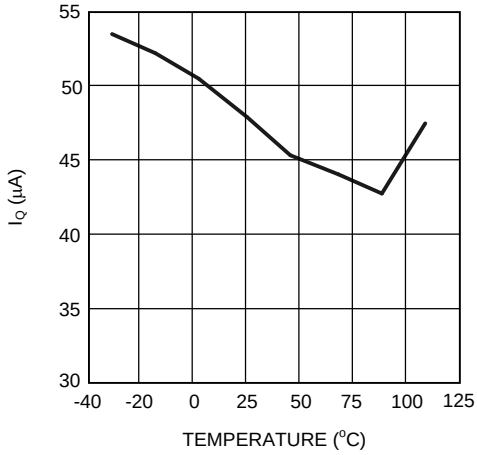

Figure 14.

Input Supply Current vs V_{IN} Shutdown Mode (25°C)

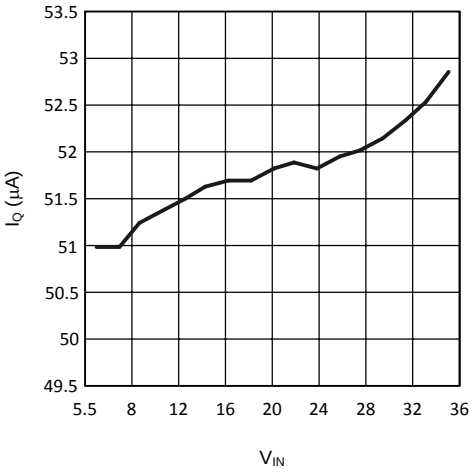

Figure 15.

VLIN5 vs Temperature

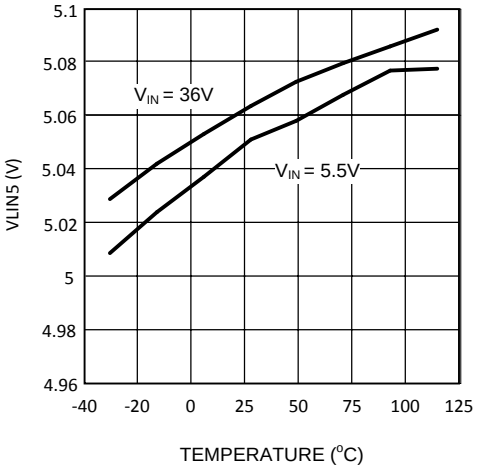

Figure 16.

VLIN5 vs V_{IN} (25°C)

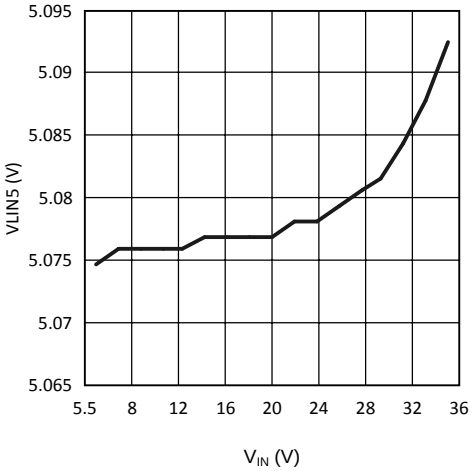

Figure 17.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

FB Reference Voltage vs Temperature

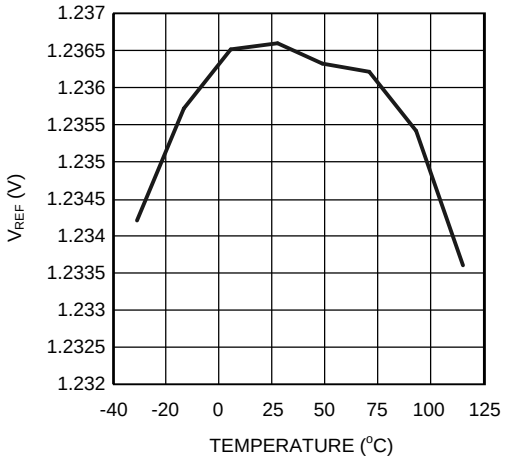

Figure 18.

Operating Frequency vs Temperature (VIN = 28V)

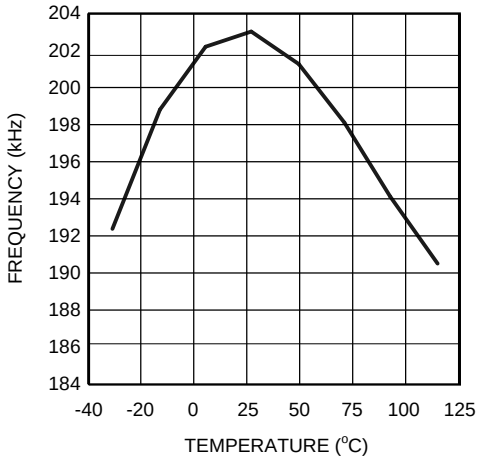

Figure 19.

Error Amplifier Tranconductance Gain vs Temperature

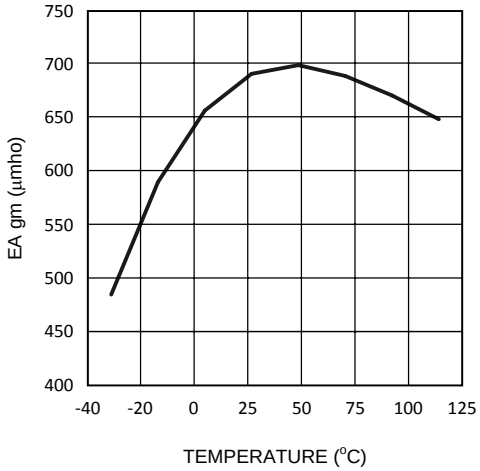

Figure 20.

Efficiency vs Load Current Using Resistor Sense Ch.1 = 1.8V, Ch.2 = Off

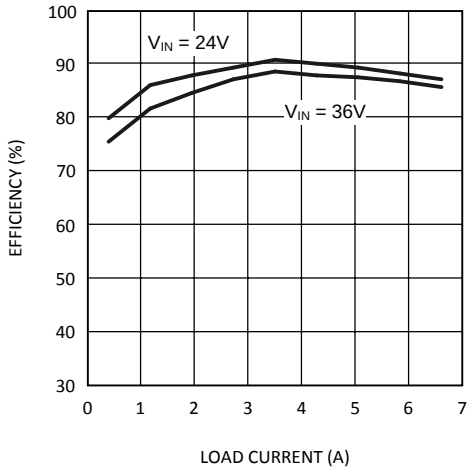

Figure 21.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Efficiency vs Load Current
Ch.2 = 3.3V, Ch.1 = Off

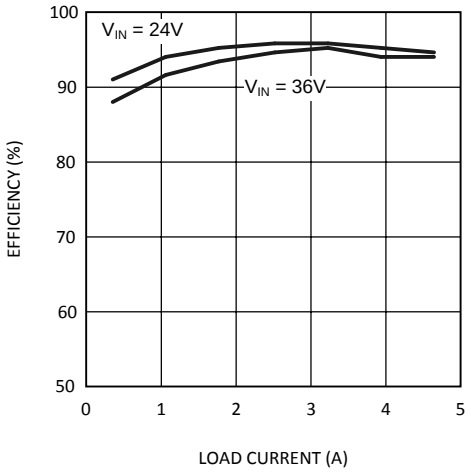

Figure 22.

Efficiency vs Load Current Using Vds Sense
Ch.2 = 1.8V, Ch.2 = Off

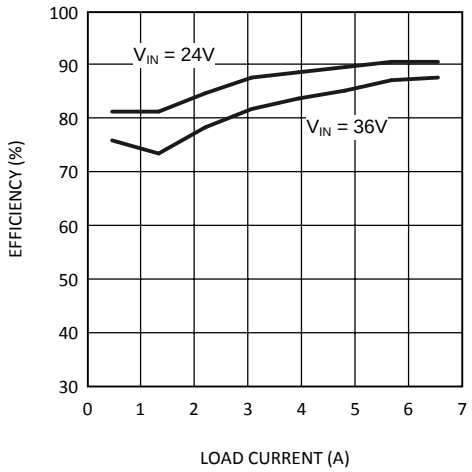

Figure 23.

Efficiency vs Load Current Using Vds Sense
Ch.2 = 3.3V, Ch.1 = Off

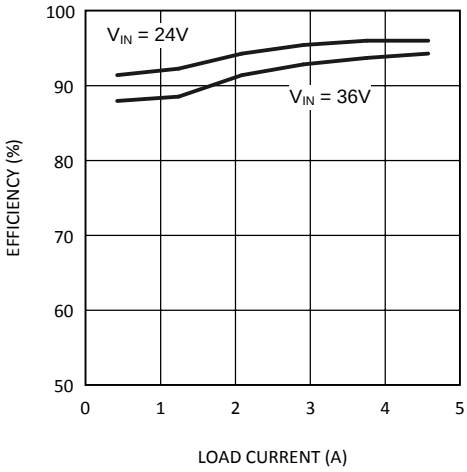

Figure 24.

OPERATING DESCRIPTIONS

SOFT START

The ON/SS1 pin has dual functionality as both channel enable and soft start control. Referring to the soft start block diagram is shown in Figure 25, the LM5642 will remain in shutdown mode while both soft start pins are grounded.

In a normal application (with a soft start capacitor connected between the ON/SS1 pin and SGND) soft start functions as follows: As the input voltage rises (note, Iss starts to flow when VIN ≥ 2.2V), the internal 5V LDO starts up, and an internal 2.4 µA current charges the soft start capacitor. During soft start, the error amplifier output voltage at the COMPx pin is clamped at 0.55V and the duty cycle is controlled only by the soft start voltage. As the SSx pin voltage ramps up, the duty cycle increases proportional to the soft start ramp, causing the output voltage to ramp up. The rate at which the duty cycle increases depends on the capacitance of the soft start capacitor. The higher the capacitance, the slower the output voltage ramps up. When the corresponding output voltage exceeds 98% (typical) of the set target voltage, the regulator switches from soft start to normal operating mode. At this time, the 0.55V clamp at the output of the error amplifier releases and peak current feedback control takes over. Once in peak current feedback control mode, the output voltage of the error amplifier will travel within a 0.5V and 2V window to achieve PWM control. See Figure 26.

The amount of capacitance needed for a desired soft-start time can be approximated in the following equation:

$$C_{ss} = \frac{I_{ss} \times t_{ss}}{V_{ss}}$$

where

- I_{ss} = 2.4 µA for one channel and 4.8µA if the channels are paralleled
- t_{ss} is the desired soft-start time (1)

Finally,

$$V_{ss} = 1.5\left(\frac{V_o}{V_{in}} + 1\right) \quad (2)$$

During soft start, over-voltage protection and current limit remain in effect. The under voltage protection feature is activated when the ON/SS pin exceeds the timeout threshold (3.4V typical). If the ON/SSx capacitor is too small, the duty cycle may increase too rapidly, causing the device to latch off due to output voltage overshoot above the OVP threshold. This becomes more likely in applications with low output voltage, high input voltage and light load. A capacitance of 10 nF is recommended at each soft start pin to provide a smooth monotonic output ramp.

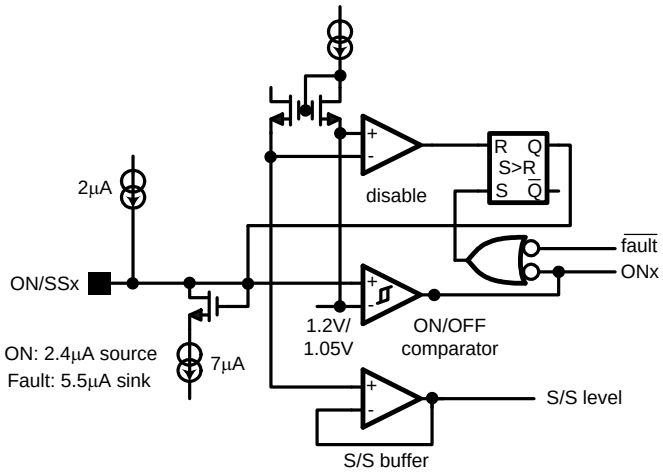

Figure 25. Soft-Start and ON/OFF

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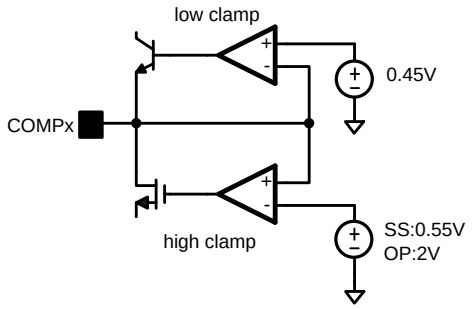

Figure 26. Voltage Clamp at COMPx Pin

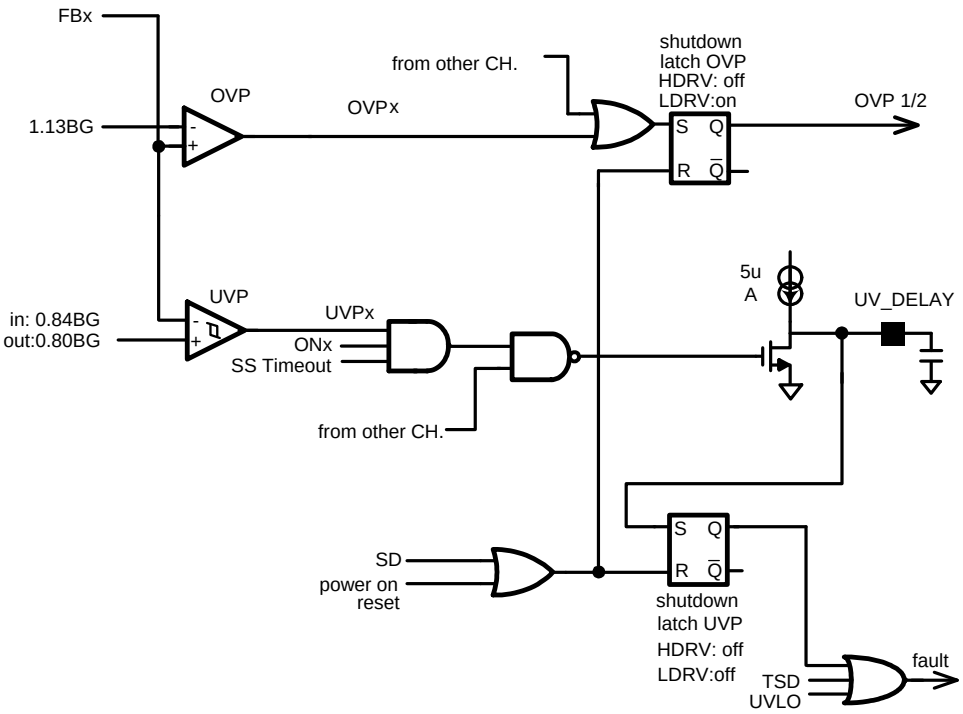

Figure 27. OVP and UVP

OVER VOLTAGE PROTECTION (OVP)

If the output voltage on either channel rises above 113% of nominal, over voltage protection activates. Both channels will latch off. When the OVP latch is set, the high side FET driver, HDRVx, is immediately turned off and the low side FET driver, LDRVx, is turned on to discharge the output capacitor through the inductor. To reset the OVP latch, either the input voltage must be cycled, or both channels must be switched off (both ON/SS pins pulled low).

UNDER VOLTAGE PROTECTION (UVP) AND UV DELAY

If the output voltage on either channel falls below 80% of nominal, under voltage protection activates. As shown in Figure 27, an under-voltage event will shut off the UV_DELAY MOSFET, which will allow the UV_DELAY capacitor to charge with 5µA (typical). If the UV_DELAY pin voltage reaches the 2.3V threshold both channels will latch off. UV_DELAY will then be disabled and the UV_DELAY pin will return to 0V. During UVP, both the high side and low side FET drivers will be turned off. If no capacitor is connected to the UV_DELAY pin, the UVP latch will be activated immediately. To reset the UVP latch, either the input voltage must be cycled, or both ON/SS pins must be pulled low. The UVP function can be disabled by connecting the UV_DELAY pin to ground.

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THERMAL SHUTDOWN

The LM5642 IC will enter thermal shutdown if the die temperature exceeds 160°C. The top and bottom FETs of both channels will be turned off immediately. In addition, both soft start capacitors will begin to discharge through separate 5.5 µA current sinks. The voltage on both capacitors will settle to approximately 1.1V, where it will remain until the thermal shutdown condition has cleared. The IC will return to normal operating mode when the die temperature has fallen to below 146°C. At this point the two soft start capacitors will begin to charge with their normal 2.4 µA current sources. This allows a controlled return to normal operation, similar to the soft start during turn-on. If the thermal shutdown condition clears before the voltage on the soft start capacitors has fallen to 1.1V, the capacitors will first be discharged to 1.1V, and then immediately begin charging back up.

OUTPUT CAPACITOR DISCHARGE

Each channel has an embedded 480Ω MOSFET with the drain connected to the SWx pin. This MOSFET will discharge the output capacitor of its channel if its channel is off, or the IC enters a fault state caused by one of the following conditions:

1. UVP
2. UVLO

If an output over voltage event occurs, the HDRVx will be turned off and LDRVx will be turned on immediately to discharge the output capacitors of both channels through the inductors.

BOOTSTRAP DIODE SELECTION

The bootstrap diode and capacitor form a supply that floats above the switch node voltage. VLIN5 powers this supply, creating approximately 5V (minus the diode drop) which is used to power the high side FET drivers and driver logic. When selecting a bootstrap diode, Schottky diodes are preferred due to their low forward voltage drop, but care must be taken for circuits that operate at high ambient temperature. The reverse leakage of some Schottky diodes can increase by more than 1000x at high temperature, and this leakage path can deplete the charge on the bootstrap capacitor, starving the driver and logic. Standard PN junction diodes and fast rectifier diodes can also be used, and these types maintain tighter control over reverse leakage current across temperature.

SWITCHING NOISE REDUCTION

Power MOSFETs are very fast switching devices. In synchronous rectifier converters, the rapid increase of drain current in the top FET coupled with parasitic inductance will generate unwanted Ldi/dt noise spikes at the source node of the FET (SWx node) and also at the VIN node. The magnitude of this noise will increase as the output current increases. This parasitic spike noise may produce excessive electromagnetic interference (EMI), and can also cause problems in device performance. Therefore, it must be suppressed using one of the following methods.

When using resistor based current sensing, it is strongly recommended to add R-C filters to the current sense amplifier inputs as shown in Figure 29. This will reduce the susceptibility to switching noise, especially during heavy load transients and short on time conditions. The filter components should be connected as close as possible to the IC.

As shown in Figure 28, adding a resistor in series with the HDRVx pin will slow down the gate drive, thus slowing the rise and fall time of the top FET, yielding a longer drain current transition time.

Usually a 3.3Ω to 4.7Ω resistor is sufficient to suppress the noise. Top FET switching losses will increase with higher resistance values.

Small resistors (1-5 ohms) can also be placed in series with the CBOOTx pin to effectively reduce switch node ringing. A CBOOT resistor will slow the rise time of the FET, whereas a resistor at HDRV will increase both rise and fall times.

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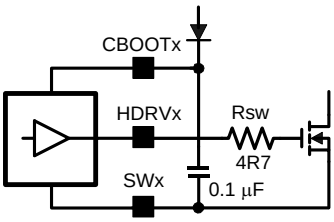

Figure 28. HDRV Series Resistor

CURRENT SENSING AND LIMITING

As shown in Figure 29, the KSx and RSNSx pins are the inputs of the current sense amplifier. Current sensing is accomplished either by sensing the Vds of the top FET or by sensing the voltage across a current sense resistor connected from VIN to the drain of the top FET. The advantages of sensing current across the top FET are reduced parts count, cost and power loss.

The $R_{DS\text{-}ON}$ of the top FET is not as stable over temperature and voltage as a sense resistor, hence great care must be used in layout for V_{DS} sensing circuits. At input voltages above 30V, the maximum recommended output current is 5A per channel.

Keeping the differential current-sense voltage below 200mV ensures linear operation of the current sense amplifier. Therefore, the $R_{DS\text{-}ON}$ of the top FET or the current sense resistor must be small enough so that the current sense voltage does not exceed 200 mV when the top FET is on. There is a leading edge blanking circuit that forces the top FET on for at least 166ns. Beyond this minimum on time, the output of the PWM comparator is used to turn off the top FET. Additionally, a minimum voltage of at least 50 mV across Rsns is recommended to ensure a high SNR at the current sense amplifier.

Assuming a maximum of 200 mV across Rsns, the current sense resistor can be calculated as follows:

$$R_{sns\ max} = \frac{200\ mV}{I_{max} + \frac{1}{2} I_{rip}}$$

where

- Imax is the maximum expected load current, including overload multiplier (ie: 120%)
- Irip is the inductor ripple current (see Equation 17) (3)

The above equation gives the maximum allowable value for Rsns. Conduction losses will increase with larger Rsns, thus lowering efficiency.

The peak current limit is set by an external resistor connected between the ILIMx pin and the KSx pin. An internal 10 µA current sink on the ILIMx pin produces a voltage across the resistor to set the current limit threshold which is then compared to the current sense voltage. A 10 nF capacitor across this resistor is required to filter unwanted noise that could improperly trip the current limit comparator.

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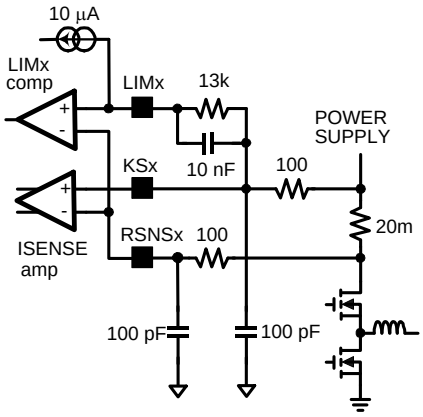

Figure 29. Current Sense and Current Limit

Current limit is activated when the inductor current is high enough to cause the voltage at the RSNSx pin to be lower than that of the ILIMx pin. This toggles the Ilim comparator, thus turning off the top FET immediately. The comparator is disabled when the top FET is turned off and during the leading edge blanking time. The equation for current limit resistor, R_{lim}, is as follows:

$$R_{lim} = \frac{\left(I_{lim} + \frac{1}{2} I_{rip}\right) R_{sns}}{10\ \mu A}$$

where

- Ilim is the load current at which the current limit comparator will be tripped (4)

When sensing current across the top FET, replace Rsns with the $R_{DS\text{-}ON}$ of the FET. This calculated Rlim value specifies that the minimum current limit will not be less than Imax. It is recommended that a 1% tolerance resistor be used.

When sensing across the top FET (V_{DS} sensing), $R_{DS\text{-}ON}$ will show more variation than a current-sense resistor, largely due to temperature variation. $R_{DS\text{-}ON}$ will increase proportional to temperature according to a specific temperature coefficient. Refer to the FET manufacturer's datasheet to determine the range of $R_{DS\text{-}ON}$ values over operating temperature or see the Component Selection section (Equation 27) for a calculation of maximum $R_{DS\text{-}ON}$. This will prevent $R_{DS\text{-}ON}$ variations from prematurely tripping the current limit comparator as the operating temperature increases.

To ensure accurate current sensing using V_{DS} sensing, special attention in board layout is required. The KSx and RSNSx pins require separate traces to form a Kelvin connection at the corresponding current sense nodes. In addition, the filter components R14, R16, C14, C15 should be removed.

INPUT UNDER VOLTAGE LOCKOUT (UVLO)

The input under-voltage lock out threshold, which is sensed via the VLIN5 internal LDO output, is 4.0V (typical). Below this threshold, both HDRVx and LDRVx will be turned off and the internal 480Ω MOSFETs will be turned on to discharge the output capacitors through the SWx pins. When the input voltage is below the UVLO threshold, the ON/SS pins will sink 5mA to discharge the soft start capacitors and turn off both channels. As the input voltage increases again above 4.0V, UVLO will be de-activated, and the device will restart through a normal soft start phase. If the voltage at VLIN5 remains below 4.5V, but above the 4.0V UVLO threshold, the device cannot be ensured to operate within specification.

If the input voltage is between 4.0V and 5.2V, the VLIN5 pin will not regulate, but will follow approximately 200 mV below the input voltage.

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DUAL-PHASE PARALLEL OPERATION

In applications with high output current demand, the two switching channels can be configured to operate as a two phase converter to provide a single output voltage with current sharing between the two switching channels. This approach greatly reduces the stress and heat on the output stage components while lowering input ripple current. The inductor ripple currents also cancel to a varying degree which results in lowered output ripple voltage. Figure 4 shows an example of a typical two-phase circuit. Because precision current sense is the primary design criteria to ensure accurate current sharing between the two channels, both channels must use external sense resistors for current sensing. To minimize the error between the error amplifiers of the two channels, tie the feedback pins FB1 and FB2 together and connect to a single voltage divider for output voltage sensing. Also, tie the COMP1 and COMP2 together and connect to the compensation network. ON/SS1 and ON/SS2 must be tied together to enable and disable both channels simultaneously.

EXTERNAL FREQUENCY SYNC

The LM5642 series has the ability to synchronize to external sources in order to set the switching frequency. This allows the LM5642 to use frequencies from 150 kHz to 250 kHz and the LM5642X to use frequencies from 200 kHz to 500 kHz. Lowering the switching frequency allows a smaller minimum duty cycle, DMIN, and hence a greater range between input and output voltage. Increasing switching frequency allows the use of smaller output inductors and output capacitors (see Component Selection). In general, synchronizing all the switching frequencies in multi-converter systems makes filtering of the switching noise easier.

The sync input can be from a system clock, from another switching converter in the system, or from any other periodic signal with a logic low-level less than 1.4V and a logic high level greater than 2V. Both CMOS and TTL level inputs are acceptable.

The LM5642 series uses a fixed delay between Channel 1 and Channel 2. The nominal switching frequency of 200kHz for the LM5642 corresponds to a switching period of 5µs. Channel 2 always turns its high-side switch on 2.5µs after Channel 1 Figure 30 (a). When the converter is synchronized to a frequency other than 200kHz, the switching period is reduced or increased, while the fixed delay between Channel 1 and Channel 2 remains constant. The phase difference between channels is therefore no longer 180°. At the extremes of the sync range, the phase difference drops to 135° Figure 30 (b) and Figure 30 (c). The result of this lower phase difference is a reduction in the maximum duty cycle of one channel that will not overlap the duty cycle of the other. As shown in Input Capacitor Selection section, when the duty cycle D1 for Channel 1 overlaps the duty cycle D2 for Channel 2, the input rms current increases, requiring more input capacitors or input capacitors with higher ripple current ratings. The new, reduced maximum duty cycle can be calculated by multiplying the sync frequency (in Hz) by 2.5×10^{-6} (the fixed delay in seconds). The same logic applies to the LM5642X. However the LM5642X has a nominal switching frequency of 375kHz which corresponds to a period of 2.67µs. Therefore channel 2 of the LM5642X always begins it's period after 1.33µs.

$$D_{MAX} = FSYNC^{*}2.5 \times 10^{-6} \quad (5)$$

At a sync frequency of 150 kHz, for example, the maximum duty cycle for Channel 1 that will not overlap Channel 2 would be 37.5%. At 250 kHz, it is the duty cycle for Channel 2 that is reduced to a D_{MAX} of 37.5%.

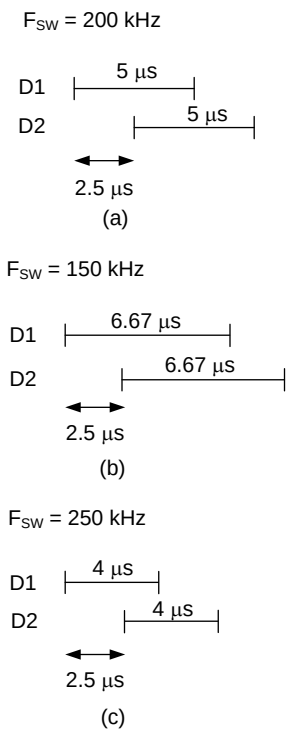

Figure 30. Period Fixed Delay Example

Component Selection

OUTPUT VOLTAGE SETTING

The output voltage for each channel is set by the ratio of a voltage divider as shown in Figure 31. The resistor values can be determined by the following equation:

$$R_1 = \frac{R_2}{\left(\frac{V_{nom}}{V_{fb}} - 1\right)}$$

where

- Vfb = 1.238V (6)

Although increasing the value of R1 and R2 will increase efficiency, this will also decrease accuracy. Therefore, a maximum value is recommended for R2 in order to keep the output within .3% of Vnom. This maximum R2 value should be calculated first with the following equation:

$$R_{2\ max} = \frac{.3\% \cdot V_{nom}}{200\ nA}$$

where

- 200nA is the maximum current drawn by FBx pin (7)

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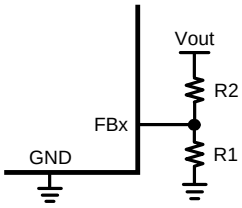

Figure 31. Output Voltage Setting

Example: Vnom = 5V, Vfb = 1.2364V, Ifbmax = 200nA.

$$R_{2\ max} = \frac{.003 \cdot 5V}{200\ nA} = 75\ k\Omega \tag{8}$$

Choose 60K

$$R_1 = \frac{60k}{\left(\frac{5V}{1.2364} - 1\right)} = 19.71\ k\Omega \cong 20\ k\Omega \tag{9}$$

The Cycle Skip and Dropout modes of the LM5642 series regulate the minimum and maximum output voltage/duty cycle that the converter can deliver. Both modes check the voltage at the COMP pin. Minimum output voltage is determined by the Cycle Skip Comparator. This circuitry skips the high side FET ON pulse when the COMP pin voltage is below 0.5V at the beginning of a cycle. The converter will continue to skip every other pulse until the duty cycle (and COMP pin voltage) rise above 0.5V, effectively halving the switching frequency.

Maximum output voltage is determined by the Dropout circuitry, which skips the low side FET ON pulse whenever the COMP pin voltage exceeds the ramp voltage derived from the current sense. Up to three low side pulses may be skipped in a row before a minimum on-time pulse must be applied to the low side FET.

Figure 32 shows the range of ouput voltage (for Io = 3A) with respect to input voltage that will keep the converter from entering either Skip Cycle or Dropout mode.

For input voltages below 5.5V, VLIN5 must be connected to Vin through a small resistor (approximately 4.7 ohm). This will ensure that VLIN5 does not fall below the UVLO threshold.

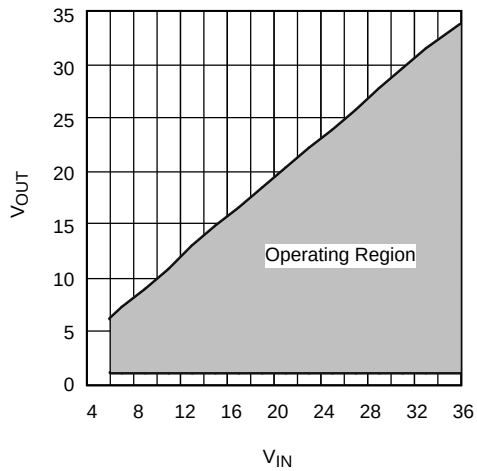

Figure 32. Output Voltage Range

Output Capacitor Selection

In applications that exhibit large, fast load current swings, the slew rate of such a load current transient will likely be beyond the response speed of the regulator. Therefore, to meet voltage transient requirements during worst-case load transients, special consideration should be given to output capacitor selection. The total combined ESR of the output capacitors must be lower than a certain value, while the total capacitance must be greater than a certain value. Also, in applications where the specification of output voltage regulation is tight and ripple voltage must be low, starting from the required output voltage ripple will often result in fewer design iterations.

ALLOWED TRANSIENT VOLTAGE EXCURSION

The allowed output voltage excursion during a load transient (ΔVc_s) is:

$$\Delta V_{c_s} = (\delta\% - \varepsilon\%) \cdot V_{nom} - \frac{1}{2} V_{rip}.$$

where

- ±δ% is the output voltage regulation window
- ±ε% is the output voltage initial accuracy (10)

Example: Vnom = 5V, δ% = 7%, ε% = 3.4%, Vrip = 40mV peak to peak.

$$\Delta V_{c_s} = (7\% - 3.4\%) \times 5V - \frac{40\ mV}{2}$$

$$= 160\ mV. \quad (11)$$

MAXIMUM ESR CALCULATION

Unless the rise and fall times of a load transient are slower than the response speed of the control loop, if the total combined ESR (Re) is too high, the load transient requirement will not be met, no matter how large the capacitance.

The maximum allowed total combined ESR is:

$$R_{e_max} = \frac{\Delta V_{c_s}}{\Delta I_{c_s}} \quad (12)$$

Since the ripple voltage is included in the calculation of ΔVc_s, the inductor ripple current should not be included in the worst-case load current excursion. Simply use the worst-case load current excursion for ΔIc_s.

Example: ΔVc_s = 160 mV, ΔIc_s = 3A. Then Re_max = 53.3 mΩ.

Maximum ESR criterion can be used when the associated capacitance is high enough, otherwise more capacitors than the number determined by this criterion should be used in parallel.

MINIMUM CAPACITANCE CALCULATION

In a switch mode power supply, the minimum output capacitance is typically dictated by the load transient requirement. If there is not enough capacitance, the output voltage excursion will exceed the maximum allowed value even if the maximum ESR requirement is met. The worst-case load transient is an unloading transient that happens when the input voltage is the highest and when the current switching cycle has just finished. The corresponding minimum capacitance is calculated as follows:

$$C_{min} = \frac{L \cdot \left[\Delta V_{c_s} - \sqrt{(\Delta V_{c_s})^2 - (\Delta I_{c_s} \cdot R_e)^2}\right]}{V_{nom} \cdot R_e^2} \quad (13)$$

Notice it is already assumed the total ESR, Re, is no greater than Re_max, otherwise the term under the square root will be a negative value. Also, it is assumed that L has already been selected, therefore the minimum L value should be calculated before C_{min} and after Re (see Inductor Selection below). Example: Re = 20 mΩ, Vnom = 5V, ΔVc_s = 160 mV, ΔIc_s = 3A, L = 8 µH

$$C_{min} = \frac{8\ \mu H \cdot \left[160\ mV - \sqrt{(160\ mV)^2 - (3A \times 20\ m\Omega)^2}\right]}{5 \times (20\ m\Omega)^2}$$

$$= 47\ \mu F. \quad (14)$$

Generally speaking, C_{min} decreases with decreasing Re, ΔIc_s, and L, but with increasing Vnom and ΔVc_s.

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Inductor Selection

The size of the output inductor can be determined from the desired output ripple voltage, Vrip, and the impedance of the output capacitors at the switching frequency. The equation to determine the minimum inductance value is as follows:

$$L_{min} = \frac{V_{in} - V_{nom}}{f \cdot V_{in}} \cdot \frac{V_{nom} \cdot R_e}{V_{rip}} \tag{15}$$

In the above equation, Re is used in place of the impedance of the output capacitors. This is because in most cases, the impedance of the output capacitors at the switching frequency is very close to Re. In the case of ceramic capacitors, replace Re with the true impedance at the switching frequency.

Example: Vin = 36V, Vo = 3.3V, V_{RIP} = 60 mV, Re = 20 mΩ, F = 200 kHz.

$$L_{min} = \frac{36 - 3.3}{200kHz \times 36} \times \frac{3.3 \times 0.02}{.060} = 5\mu H \tag{16}$$

The actual selection process usually involves several iterations of all of the above steps, from ripple voltage selection, to capacitor selection, to inductance calculations. Both the highest and the lowest input and output voltages and load transient requirements should be considered. If an inductance value larger than Lmin is selected, make sure that the Cmin requirement is not violated.

Priority should be given to parameters that are not flexible or more costly. For example, if there are very few types of capacitors to choose from, it may be a good idea to adjust the inductance value so that a requirement of 3.2 capacitors can be reduced to 3 capacitors.

Since inductor ripple current is often the criterion for selecting an output inductor, it is a good idea to double-check this value. The equation is:

$$I_{rip} = \frac{(V_{in} - V_{nom})}{f \cdot L} \cdot D \tag{17}$$

Also important is the ripple content, which is defined by Irip /Inom. Generally speaking, a ripple content of less than 50% is ok. Larger ripple content will cause too much power loss in the inductor.

Example: Vin = 36V, Vo = 3.3V, F = 200 kHz, L = 5 µH, 3A max I_{OUT}

$$I_{rip} = \frac{36 - 3.3}{200kHz \times 5x10^{-6}} \times \frac{3.3}{36} = 3A \tag{18}$$

3A is 100% ripple which is too high.

In this case, the inductor should be reselected on the basis of ripple current.

Example: 40% ripple, 40% • 3A = 1.2A

$$1.2A = \frac{36 - 3.3}{L \times 200kHz} \times \frac{3.3}{36} \tag{19}$$

$$L = \frac{36 - 3.3}{200kHz \times 1.2A} \times \frac{3.3}{36} = 12.5\mu H \tag{20}$$

When choosing the inductor, the saturation current should be higher than the maximum peak inductor current and the RMS current rating should be higher than the maximum load current.

Input Capacitor Selection

The fact that the two switching channels of the LM5642 are 180° out of phase will reduce the RMS value of the ripple current seen by the input capacitors. This will help extend input capacitor life span and result in a more efficient system. Input capacitors must be selected that can handle both the maximum ripple RMS current at highest ambient temperature as well as the maximum input voltage. In applications in which output voltages are less than half of the input voltage, the corresponding duty cycles will be less than 50%. This means there will be no overlap between the two channels' input current pulses.

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The equation for calculating the maximum total input ripple RMS current for duty cycles under 50% is:

$$I_{irrm} = \sqrt{I_1^2 D_1 (1 - D_1) + I_2^2 D_2 (1 - D_2) - 2 I_1 I_2 D_1 D_2}$$

where

- I1 is maximum load current of Channel 1
- I2 is the maximum load current of Channel 2
- D1 is the duty cycle of Channel 1
- D2 is the duty cycle of Channel 2 (21)

Example: Imax_1 = 3.6A, Imax_2 = 3.6A, D1 = 0.42, and D2 = 0.275

$$I_{irrm} = \left[(3.6A)^2 \cdot 0.42 \cdot (1 - 0.42) + (3.6A)^2 \cdot 0.275 \cdot (1 - 0.275) - 2 \cdot 3.6A \cdot 3.6A \cdot 0.42 \cdot 0.275 \right]^{.5} = 1.66A. \quad (22)$$

Choose input capacitors that can handle 1.66A ripple RMS current at highest ambient temperature. In applications where output voltages are greater than half the input voltage, the corresponding duty cycles will be greater than 50%, and there will be overlapping input current pulses. Input ripple current will be highest under these circumstances. The input RMS current in this case is given by:

$$I_{irrm} = \left[\begin{array}{l} \left[I_1 (1 - D_1) + I_2 (1 - D_2) \right]^2 (D_1 + D_2 - 1) \\ + \left[I_1 (1 - D_1) - I_2 (D_2) \right]^2 (1 - D_2) + \\ \left[I_2 (1 - D_2) - I_1 (D_1) \right]^2 (1 - D_1) \end{array} \right]^{.5} \quad (23)$$

Where, again, I1 and I2 are the maximum load currents of channel 1 and 2, and D1 and D2 are the duty cycles. This equation should be used when both duty cycles are expected to be higher than 50%.

If the LM5642 is being used with an external clock frequency other than 200kHz, or 375 kHz for the LM5642X, the preceding equations for input rms current can still be used. The selection of the first equation or the second changes because overlap can now occur at duty cycles that are less than 50%. From the EXTERNAL FREQUENCY SYNC section, the maximum duty cycle that ensures no overlap between duty cycles (and hence input current pulses) is:

$$D_{MAX} = F_{SYNC}^{*} 2.5 \times 10^{-6} \quad (24)$$

There are now three distinct possibilities which must be considered when selecting the equation for input rms current. The following applies for the LM5642, and also the LM5642X by replacing 200 kHz with 375 kHz:

1. Both duty cycles D_1 and D_2 are less than D_{MAX}. In this case, the first, simple equation can always be used.
2. One duty cycle is greater than D_{MAX} and the other duty cycle is less than D_{MAX}. In this case, the system designer can take advantage of the fact that the sync feature reduces D_{MAX} for one channel, but lengthens it for the other channel. For F_{SYNC} < 200kHz, D_1 is reduced to D_{MAX} while D_2 actually increases to (1-D_{MAX}). For F_{SYNC} > 200kHz, D_2 is reduced to D_{MAX} while D_1 increases to (1-D_{MAX}). By using the channel reduced to D_{MAX} for the lower duty cycle, and the channel that has been increased for the higher duty cycle, the first, simple rms input current equation can be used.
3. Both duty cycles are greater than D_{MAX}. This case is identical to a system at 200 kHz where either duty cycle is 50% or greater. Some overlap of duty cycles is specified, and hence the second, more complicated rms input current equation must be used.

Input capacitors must meet the minimum requirements of voltage and ripple current capacity. The size of the capacitor should then be selected based on hold up time requirements. Bench testing for individual applications is still the best way to determine a reliable input capacitor value. Input capacitors should always be placed as close as possible to the current sense resistor or the drain of the top FET. When high ESR capacitors such as tantalum are used, a 1µF ceramic capacitor should be added as closely as possible to the high-side FET drain and low-side FET source.

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MOSFET Selection

BOTTOM FET SELECTION

During normal operation, the bottom FET is switching on and off at almost zero voltage. Therefore, only conduction losses are present in the bottom FET. The most important parameter when selecting the bottom FET is the on-resistance ($R_{DS\text{-}ON}$). The lower the on-resistance, the lower the power loss. The bottom FET power loss peaks at maximum input voltage and load current. The equation for the maximum allowed on-resistance at room temperature for a given FET package, is:

$$R_{dson_max} = \frac{1}{I_{max}^2 \cdot \left(1 - \frac{V_{nom}}{V_{in_max}}\right)} \times \frac{T_{j_max} - T_{a_max}}{\left[1 + TC \cdot (T_{j_max} - 25°C/W)\right] \cdot R_{\theta ja}}$$

where

- Tj_max is the maximum allowed junction temperature in the FET
- Ta_max is the maximum ambient temperature
- $R_{\theta ja}$ is the junction-to-ambient thermal resistance of the FET
- TC is the temperature coefficient of the on-resistance which is typically in the range of 4000ppm/°C (25)

If the calculated $R_{DS\text{-}ON\ (MAX)}$ is smaller than the lowest value available, multiple FETs can be used in parallel. This effectively reduces the I_{max} term in the above equation, thus reducing $R_{DS\text{-}ON}$. When using two FETs in parallel, multiply the calculated $R_{DS\text{-}ON\ (MAX)}$ by 4 to obtain the $R_{DS\text{-}ON\ (MAX)}$ for each FET. In the case of three FETs, multiply by 9.

$$R_{ds_max} = \frac{1}{(3.6A)^2 \cdot \left(1 - \frac{5V}{30V}\right)} \times \frac{100°C - 60°C}{\left[1 + 0.01/°C \cdot (100°C - 25°C)\right] \cdot 60°C/W} = 35.3\ m\Omega \quad (26)$$

If the selected FET has an Rds value higher than 35.3Ω, then two FETs with an $R_{DS\text{-}ON}$ less than 141 mΩ (4 x 35.3 mΩ) can be used in parallel. In this case, the temperature rise on each FET will not go to Tj_max because each FET is now dissipating only half of the total power.

TOP FET SELECTION

The top FET has two types of losses: switching loss and conduction loss. The switching losses mainly consist of crossover loss and losses related to the low-side FET body diode reverse recovery. Since it is rather difficult to estimate the switching loss, a general starting point is to allot 60% of the top FET thermal capacity to switching losses. The best way to precisely determine switching losses is through bench testing. The equation for calculating the on resistance of the top FET is thus:

$$R_{ds_max} = \frac{V_{in_min} \cdot .4}{I_{max}^2 \cdot V_{nom}} \times \frac{T_{j_max} - T_{a_max}}{\left[1 + TC \cdot (T_{j_max} - 25°C/W)\right] \cdot R_{\theta ja}} \quad (27)$$

Example: Tj_max = 100°C, Ta_max = 60°C, Rqja = 60°C/W, Vin_min = 5.5V, Vnom = 5V, and Iload_max = 3.6A.

$$R_{ds_max} = \frac{5.5V \times .4}{(3.6A)^2 \times 5V} \times \frac{100°C - 60°C}{\left[1 + 0.01/°C \cdot (100°C - 25°C)\right] \cdot 60°C/W} = 13\,m\Omega \quad (28)$$

When using FETs in parallel, the same guidelines apply to the top FET as apply to the bottom FET.

Loop Compensation

The general purpose of loop compensation is to meet static and dynamic performance requirements while maintaining stability. Loop gain is what is usually checked to determine small-signal performance. Loop gain is equal to the product of control-output transfer function and the feedback transfer function (the compensation network transfer function). Generally speaking it is desirable to have a loop gain slope that is roughly -20dB /decade from a very low frequency to well beyond the crossover frequency. The crossover frequency should not exceed one-fifth of the switching frequency. The higher the bandwidth, the faster the load transient response speed will be. However, if the duty cycle saturates during a load transient, further increasing the small signal bandwidth will not help. Since the control-output transfer function usually has very limited low frequency gain, it is a good idea to place a pole in the compensation at zero frequency, so that the low frequency gain will be relatively large. A large DC gain means high DC regulation accuracy (i.e. DC voltage changes little with load or line variations). The rest of the compensation scheme depends highly on the shape of the control-output plot.

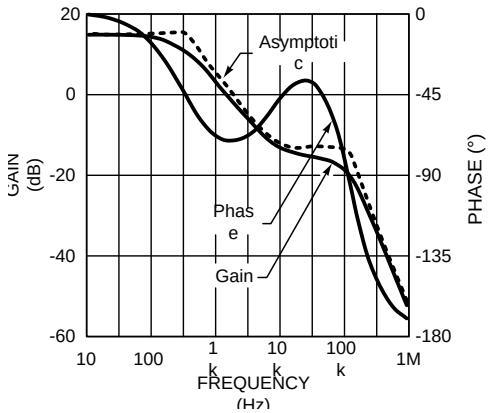

Figure 33. Control-Output Transfer Function

As shown in Figure 33, the control-output transfer function consists of one pole (fp), one zero (fz), and a double pole at fn (half the switching frequency). The following can be done to create a -20dB /decade roll-off of the loop gain: Place the first pole at 0Hz, the first zero at fp, the second pole at fz, and the second zero at fn. The resulting feedback transfer function is shown in Figure 34.

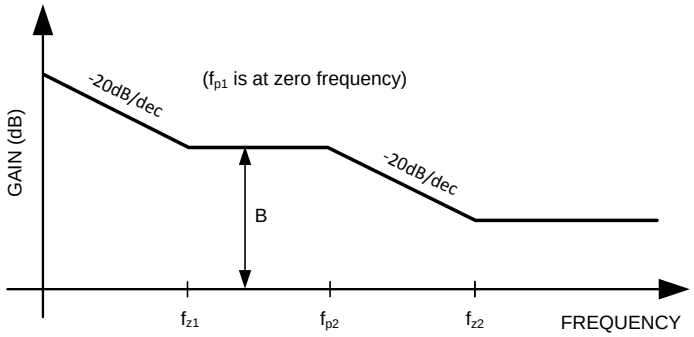

Figure 34. Feedback Transfer Function

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The control-output corner frequencies, and thus the desired compensation corner frequencies, can be determined approximately by the following equations:

$$f_Z = \frac{1}{2\pi R_e C_o} \tag{29}$$

$$f_P = \frac{1}{2\pi R_O C_O} + \frac{1 - D - .5}{2\pi f L C_O} \tag{30}$$

Since fp is determined by the output network, it will shift with loading (Ro). It is best to use a minimum Iout value of approximately 100mA when determining the maximum Ro value.

Example: Re = 20 mΩ, Co = 100 uF, Romax = 5V/100 mA = 50Ω:

$$f_z = \frac{1}{2\pi \cdot 20\,m\Omega \cdot 100\,\mu F} = 80\,kHz \tag{31}$$

$$f_{p\ min} = \frac{1}{2\pi \cdot 50\Omega \cdot 100\,\mu F} + \frac{1}{2\pi \cdot 200k \cdot 8\mu \cdot 100\,\mu F} = 995\,Hz \tag{32}$$

First determine the minimum frequency (fpmin) of the pole across the expected load range, then place the first compensation zero at or below that value. Once fpmin is determined, Rc1 should be calculated using:

$$R_{c1} = \frac{B}{gm}\left(\frac{R_1 + R_2}{R_1}\right)$$

where

- B is the desired gain in V/V at fp (fz1)
- gm is the transconductance of the error amplifier
- R1 and R2 are the feedback resistors (33)

A gain value around 10dB (3.3v/v) is generally a good starting point.

Example: B = 3.3v/v, gm = 650m, R1 = 20 kKΩ, R2 = 60.4 kΩ:

$$R_{c1} = \frac{3.3}{650\mu}\left(\frac{20k + 60.4k}{20k}\right) = 20.4\,k\Omega \cong 20\,k\Omega \tag{34}$$

Bandwidth will vary proportional to the value of Rc1. Next, Cc1 can be determined with the following equation:

$$C_{c1} = \frac{1}{2\pi \cdot f_{p\ min} \cdot R_{c1}} \tag{35}$$

Example: fpmin = 995 Hz, Rc1 = 20 kΩ:

$$C_{c1} = \frac{1}{2\pi \cdot 995\,Hz \cdot 20\,k\Omega} \cong 8\,nF \tag{36}$$

The compensation network (Figure 35) will also introduce a low frequency pole which will be close to 0 Hz.

A second pole should also be placed at fz. This pole can be created with a single capacitor Cc2 and a shorted Rc2 (see Figure 35). The minimum value for this capacitor can be calculated by:

$$C_{c2\ min} = \frac{1}{2\pi \cdot f_z \cdot R_{c1}} \tag{37}$$

Cc2 may not be necessary, however it does create a more stable control loop. This is especially important with high load currents and in current sharing mode.

Example: fz = 80 kHz, Rc1 = 20 kΩ:

$$C_{c2\ min} = \frac{1}{2\pi \cdot 80\,kHz \cdot 20\,k\Omega} \cong 100\,pF \tag{38}$$

A second zero can also be added with a resistor in series with Cc2. If used, this zero should be placed at fn, where the control to output gain rolls off at -40dB/dec. Generally, fn will be well below the 0dB level and thus will have little effect on stability. Rc2 can be calculated with the following equation:

$$R_{c2} = \frac{1}{2\pi \cdot f_n \cdot C_{c2}} \tag{39}$$

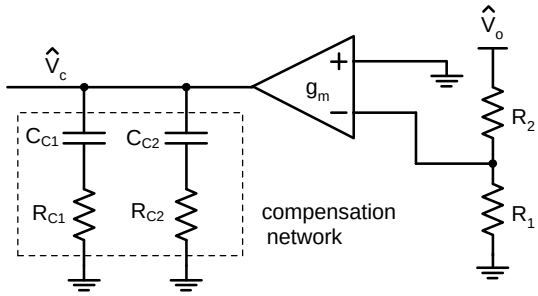

Figure 35. Compensation Network

PCB Layout Considerations

To produce an optimal power solution with the LM5642 series, good layout and design of the PCB are as important as the component selection. The following are several guidelines to aid in creating a good layout.

KELVIN TRACES FOR SENSE LINES

When using the current sense resistor to sense the load current connect the KS pin using a separate trace to VIN, as close as possible to the current-sense resistor. The RSNS pin should be connected using a separate trace to the low-side of the current sense resistor. The traces should be run parallel to each other to give common mode rejection. Although it can be difficult in a compact design, these traces should stay away from the output inductor and switch node if possible, to avoid coupling stray flux fields. When a current-sense resistor is not used the KS pin should be connected as close as possible to the drain node of the upper MOSFET and the RSNS pin should be connected as close as possible to the source of the upper MOSFET using Kelvin traces. To further help minimize noise pickup on the sense lines is to use RC filtering on the KS and RSNS pins.

SEPARATE PGND AND SGND

Good layout techniques include a dedicated ground plane, usually on an internal layer. Signal level components like the compensation and feedback resistors should be connected to a section of this internal SGND plane. The SGND section of the plane should be connected to the power ground at only one point. The best place to connect the SGND and PGND is right at the PGND pin..

MINIMIZE THE SWITCH NODE

The plane that connects the power FETs and output inductor together radiates more EMI as it gets larger. Use just enough copper to give low impedance to the switching currents, preferably in the form of a wide, but short, trace run.

LOW IMPEDANCE POWER PATH

The power path includes the input capacitors, power FETs, output inductor, and output capacitors. Keep these components on the same side of the PCB and connect them with thick traces or copper planes (shapes) on the same layer. Vias add resistance and inductance to the power path, and have relatively high impedance connections to the internal planes. If high switching currents must be routed through vias and/or internal planes, use multiple vias in parallel to reduce their resistance and inductance. The power components should be kept close together. The longer the paths that connect them, the more they act as antennas, radiating unwanted EMI.

Please see AN-1229 (literature number SNVA054) for further PCB layout considerations.

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Table 1. Bill Of Materials for Figure 3 24V to 1.8, 3.3V LM5642

ID	Part Number	Type	Size	Parameters	Qty	Vendor
U1	LM5642	Dual Synchronous Controller	TSSOP-28		1	TI
Q1, Q4	Si4850EY	N-MOSFET	SO-8	60V	2	Vishay
Q2, Q5	Si4840DY	N-MOSFET	SO-8	40V	2	Vishay
D3	BAS40-06	Schottky Diode	SOT-23	40V	1	Vishay
L1	RLF12560T-4R2N100	Inductor	12.5x12.5x 6mm	4.2µH, 7mΩ 10A	1	TDK
L2	RLF12545T-100M5R1	Inductor	12.5x12.5x 4.5mm	10µH, 12mΩ 5.1A	1	TDK
C1	C3216X7R1H105K	Capacitor	1206	1µF, 50V	1	TDK
C3, C4, C14, C15	VJ1206Y101KXXAT	Capacitor	1206	100pF, 25V	3	Vishay
C27	C2012X5R1C105K	Capacitor	0805	1µF, 16V	1	TDK
C6, C16	C5750X5R1H106M	Capacitor	2220	10µF 50V, 2.8A	2	TDK
C9, C23	6TPD330M	Capacitor	7.3x4.3x 3.8mm	330µF, 6.3V, 10mΩ	2	Sanyo
C2, C11, C12, C13	VJ1206Y103KXXAT	Capacitor	1206	10nF, 25V	4	Vishay
C7, C25, C34	VJ1206Y104KXXAT	Capacitor	1206	100nF, 25V	3	Vishay
C19	VJ1206Y822KXXAT	Capacitor	1206	8.2nF 10%	1	Vishay
C20	VJ1206Y153KXXAT	Capacitor	1206	15nF 10%	1	Vishay
C26	C3216X7R1C475K	Capacitor	1206	4.7µF 25V	1	TDK
R1	CRCW1206123J	Resistor	1206	12kΩ 5%	1	Vishay
R2, R6, R14, R16	CRCW1206100J	Resistor	1206	100Ω 5%	1	Vishay
R13	CRCW1206682J	Resistor	1206	6.8kΩ 12%	1	Vishay
R7, R15	WSL-2512 .010 1%	Resistor	2512	10mΩ 1W	2	Vishay
R8, R9, R12, R17, R18, R21, R31, R32	CRCW1206000Z	Resistor	1206	0Ω	8	Vishay
R10	CRCW12062261F	Resistor	1206	2.26kΩ 1%	1	Vishay
R23	CRCW12068451F	Resistor	1206	8.45kΩ 1%	1	Vishay
R24	CRCW12061372F	Resistor	1206	13.7kΩ 1%	1	Vishay
R11, R20	CRCW12064991F	Resistor	1206	4.99kΩ 1%	2	Vishay
R19	CRCW12068251F	Resistor	1206	8.25kΩ 1%	1	Vishay
R27	CRCW12064R7J	Resistor	1206	4.7Ω 5%	1	Vishay
R28	CRCW1206224J	Resistor	1206	220kΩ 5%	1	Vishay

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Table 2. Bill of Materials for Figure 4 30V to 1.8V, 20A LM5642

ID	Part Number	Type	Size	Parameters	Qty	Vendor
U1	LM5642	Dual Synchronous Controller	TSSOP-28		1	TI
Q1, Q4	Si4850EY	N-MOSFET	SO-8	60V	2	Vishay
Q2, Q3, Q5, Q6	Si4470DY	N-MOSFET	SO-8	60V	4	Vishay
D3	BAS40-06	Schottky Diode	SOT-23	40V	1	Vishay
L1,L2	RLF12560T-2R7N110	Inductor	12.5x12.5x 6mm	2.7µH,4.5mΩ 11.5A	2	TDK
C1	C3216X7R1H105K	Capacitor	1206	1µF, 50V	1	TDK
C10, C24, C27	C2012X5R1C105K	Capacitor	0805	1µF, 16V	3	TDK
C6, C16, C28, C30	C5750X5R1H106M	Capacitor	2220	10µF 50V, 2.8A	4	TDK
C9, C23	16MV1000WX	Capacitor	10mm D20mm H	1000µF, 16V, 22mΩ	2	Sanyo
C2, C13	VJ1206Y103KXXAT	Capacitor	1206	10nF, 25V	2	Vishay
C11	VJ1206Y223KXXAT	Capacitor	1206	22nF, 25V	1	Vishay
C7,C25, C34	VJ1206Y104KXXAT	Capacitor	1206	100nF, 25V	3	Vishay
C19	VJ1206Y273KXXAT	Capacitor	1206	27nF 10%	1	Vishay
C26	C3216X7R1C475K	Capacitor	1206	4.7µF 25V	1	TDK
R1, R13	CRCW1206123J	Resistor	1206	16.9kΩ 1%	1	Vishay
R2, R6, R14, R16	CRCW1206100J	Resistor	1206	100Ω 5%	1	Vishay
R7, R15	WSL-2512 .010 1%	Resistor	2512	10mΩ 1W	2	Vishay
R8, R9, R12, R17, R18, R21, R31, R32	CRCW1206000Z	Resistor	1206	0Ω	8	Vishay
R10	CRCW12062261F	Resistor	1206	2.26kΩ 1%	1	Vishay
R11	CRCW12064991F	Resistor	1206	4.99kΩ 1%	1	Vishay
R23	CRCW12061152F	Resistor	1206	11.5kΩ 1%	1	Vishay
R27	CRCW12064R7J	Resistor	1206	4.7Ω 5%	1	Vishay
R28	CRCW1206224J	Resistor	1206	220kΩ 5%	1	Vishay

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Table 3. Bill Of Materials Based on Figure 3 V_{in}= 9-16V, $V_{O1,2}$=1.5V,1.8V, 5A LM5642X

ID	Part Number	Type	Size	Parameters	Qty	Vendor
U1	LM5642X	Dual Synchronous Controller	TSSOP-28		1	TI
Q1, Q4	Si4850EY	N-MOSFET	SO-8	60V	2	Vishay
Q2, Q5	Si4840DY	N-MOSFET	SO-8	40V	2	Vishay
D3	BA54A	Schottky Diode	SOT-23	30V	1	Vishay
L1, L2	RLF12545T-4R2N100	Inductor	12.5x12.5x 4.5mm	4.2µH, 7mΩ 6.5A	2	TDK
C1	C3216X7R1H105K	Capacitor	1206	1µF, 50V	1	TDK
C3, C4, C14, C15	VJ1206Y101KXXAT	Capacitor	1206	100pF, 25V	4	Vishay
C27	C2012X5R1C105K	Capacitor	0805	1µF, 16V	1	TDK
C6, C28	C5750X7R1H106M	Capacitor	2220	10µF 50V, 2.8A	2	TDK
C9, C23	C4532X7R0J107M	Capacitor	1812	100µF, 6.3V, 1mΩ	2	TDK
C2, C11, C12, C13	VJ1206Y103KXXAT	Capacitor	1206	10nF, 25V	4	Vishay
C7, C25, C34	VJ1206Y104KXXAT	Capacitor	1206	100nF, 25V	3	Vishay
C18, C20	VJ1206Y473KXXAT	Capacitor	1206	47nF 10%	2	Vishay
C26	C3216X7R1C475K	Capacitor	1206	4.7µF 25V	1	TDK
R1, R13	CRCW12061912F	Resistor	1206	19.1kΩ 1%	2	Vishay
R2, R6, R14, R16	CRCW1206100J	Resistor	1206	100Ω 5%	1	Vishay
R7, R15	WSL-1206 .020 1%	Resistor	1206	20mΩ 1W	2	Vishay
R8, R9, R12, R17, R18, R21, R31, R32	CRCW1206000Z	Resistor	1206	0Ω	8	Vishay
R10, R19	CRCW12061001F	Resistor	1206	1kΩ 1%	2	Vishay
R11	CRCW12062611F	Resistor	1206	2.61kΩ 1%	1	Vishay
R20	CRCW12062321F	Resistor	1206	2.32kΩ 1%	1	Vishay
R22, R24	CRCW12063011F	Resistor	1206	3.01kΩ 1%	2	Vishay
R27	CRCW12064R7J	Resistor	1206	4.7Ω 5%	1	Vishay
R28	CRCW1206224J	Resistor	1206	220kΩ 5%	1	Vishay

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Table 4. Bill Of Materials Based on Figure 3 V_{in}= 9-16V, $V_{O1,2}$=3.3V,5V, 5A LM5642X

ID	Part Number	Type	Size	Parameters	Qty	Vendor
U1	LM5642X	Dual Synchronous Controller	TSSOP-28		1	TI
Q1, Q4	Si4850EY	N-MOSFET	SO-8	60V	2	Vishay
Q2, Q5	Si4840DY	N-MOSFET	SO-8	40V	2	Vishay
D3	BA54A	Schottky Diode	SOT-23	30V	1	Vishay
L1, L2	RLF12545T-5R6N6R1	Inductor	12.5x12.5x 4.5mm	5.6µH, 9mΩ 6.1A	2	TDK
C1	C3216X7R1H105K	Capacitor	1206	1µF, 50V	1	TDK
C3, C4, C14, C15	VJ1206Y101KXXAT	Capacitor	1206	100pF, 25V	4	Vishay
C27	C2012X5R1C105K	Capacitor	0805	1µF, 16V	1	TDK
C6, C28	C5750X7R1H106M	Capacitor	2220	10µF 50V, 2.8A	2	TDK
C9, C23	C4532X7R0J107M	Capacitor	1812	100µF, 6.3V, 1mΩ	2	TDK
C2, C11, C12, C13	VJ1206Y103KXXAT	Capacitor	1206	10nF, 25V	4	Vishay
C7, C25, C34	VJ1206Y104KXXAT	Capacitor	1206	100nF, 25V	3	Vishay
C18, C20	VJ1206Y393KXXAT	Capacitor	1206	39nF 10%	2	Vishay
C26	C3216X7R1C475K	Capacitor	1206	4.7µF 25V	1	TDK
R1, R13	CRCW12061912F	Resistor	1206	19.1kΩ 1%	2	Vishay
R2, R6, R14, R16	CRCW1206100J	Resistor	1206	100Ω 5%	1	Vishay
R7, R15	WSL-1206 .020 1%	Resistor	1206	20mΩ 1W	2	Vishay
R8, R9, R12, R17, R18, R21, R31, R32	CRCW1206000Z	Resistor	1206	0Ω	8	Vishay
R10, R19	CRCW12061002F	Resistor	1206	10kΩ 1%	2	Vishay
R11	CRCW12066191F	Resistor	1206	6.19kΩ 1%	1	Vishay
R20	CRCW12063321F	Resistor	1206	3.32kΩ 1%	1	Vishay
R22, R24	CRCW12063831F	Resistor	1206	3.83kΩ 1%	2	Vishay
R27	CRCW12064R7J	Resistor	1206	4.7Ω 5%	1	Vishay
R28	CRCW1206224J	Resistor	1206	220kΩ 5%	1	Vishay

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REVISION HISTORY

Changes from Revision J (April 2013) to Revision K	Page
• Changed layout of National Data Sheet to TI format	32

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5642MH/NOPB	ACTIVE	HTSSOP	PWP	28	48	RoHS & Green	SN	Level-1-260C-UNLIM		LM5642 MH	Samples
LM5642MHX/NOPB	ACTIVE	HTSSOP	PWP	28	2500	RoHS & Green	SN	Level-1-260C-UNLIM		LM5642 MH	Samples
LM5642MTC	NRND	TSSOP	PW	28	48	Non-RoHS & Green	Call TI	Level-3-235C-168 HR	-40 to 125	LM5642 MTC	
LM5642MTC/NOPB	ACTIVE	TSSOP	PW	28	48	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LM5642 MTC	Samples
LM5642MTCX	NRND	TSSOP	PW	28	2500	Non-RoHS & Green	Call TI	Level-3-235C-168 HR	-40 to 125	LM5642 MTC	
LM5642MTCX/NOPB	ACTIVE	TSSOP	PW	28	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LM5642 MTC	Samples
LM5642XMH/NOPB	ACTIVE	HTSSOP	PWP	28	48	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM5642 XMH	Samples
LM5642XMHX/NOPB	ACTIVE	HTSSOP	PWP	28	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM5642 XMH	Samples
LM5642XMT/NOPB	ACTIVE	TSSOP	PW	28	48	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LM5642 XMT	Samples
LM5642XMTX/NOPB	ACTIVE	TSSOP	PW	28	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LM5642 XMT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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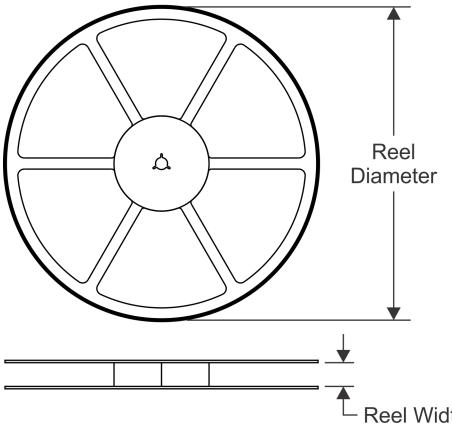
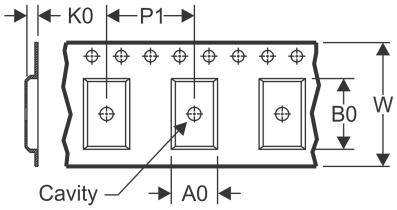
TAPE AND REEL INFORMATION

REEL DIMENSIONS

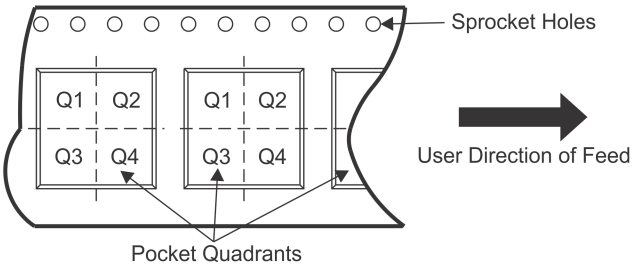


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

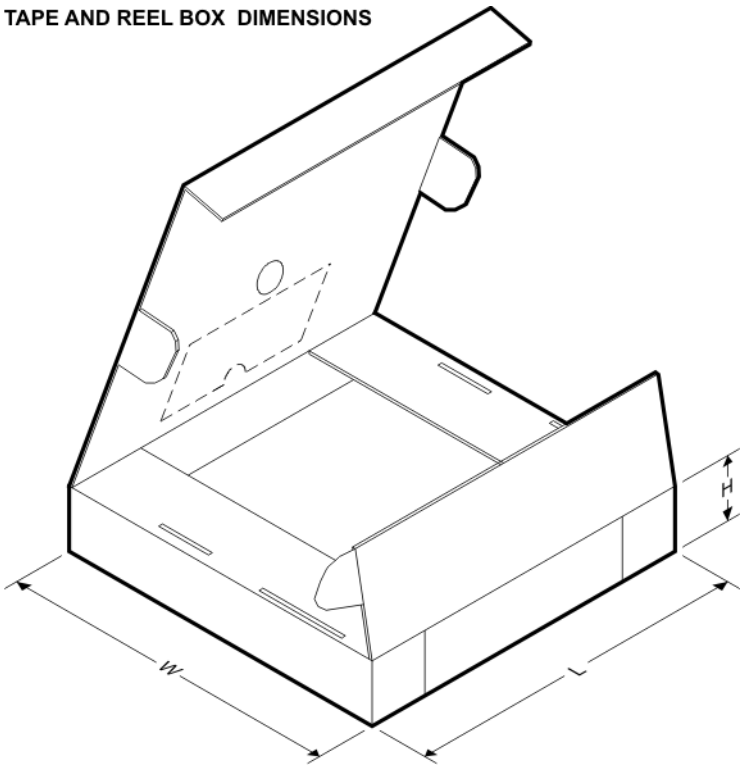
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5642MHX/NOPB	HTSSOP	PWP	28	2500	330.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1
LM5642MTCX	TSSOP	PW	28	2500	330.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1
LM5642MTCX/NOPB	TSSOP	PW	28	2500	330.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1
LM5642XMHX/NOPB	HTSSOP	PWP	28	2500	330.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1
LM5642XMTX/NOPB	TSSOP	PW	28	2500	330.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1

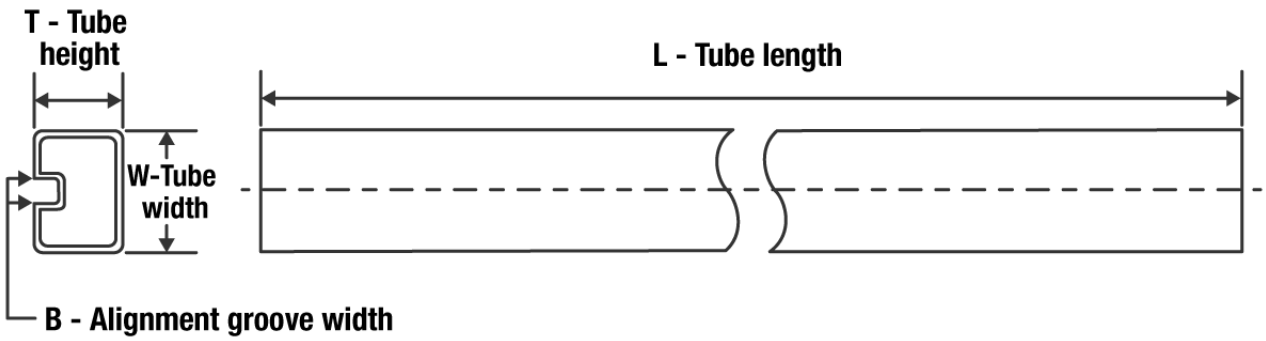
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5642MHX/NOPB	HTSSOP	PWP	28	2500	367.0	367.0	35.0
LM5642MTCX	TSSOP	PW	28	2500	853.0	449.0	35.0
LM5642MTCX/NOPB	TSSOP	PW	28	2500	853.0	449.0	35.0
LM5642XMHX/NOPB	HTSSOP	PWP	28	2500	367.0	367.0	35.0
LM5642XMTX/NOPB	TSSOP	PW	28	2500	853.0	449.0	35.0

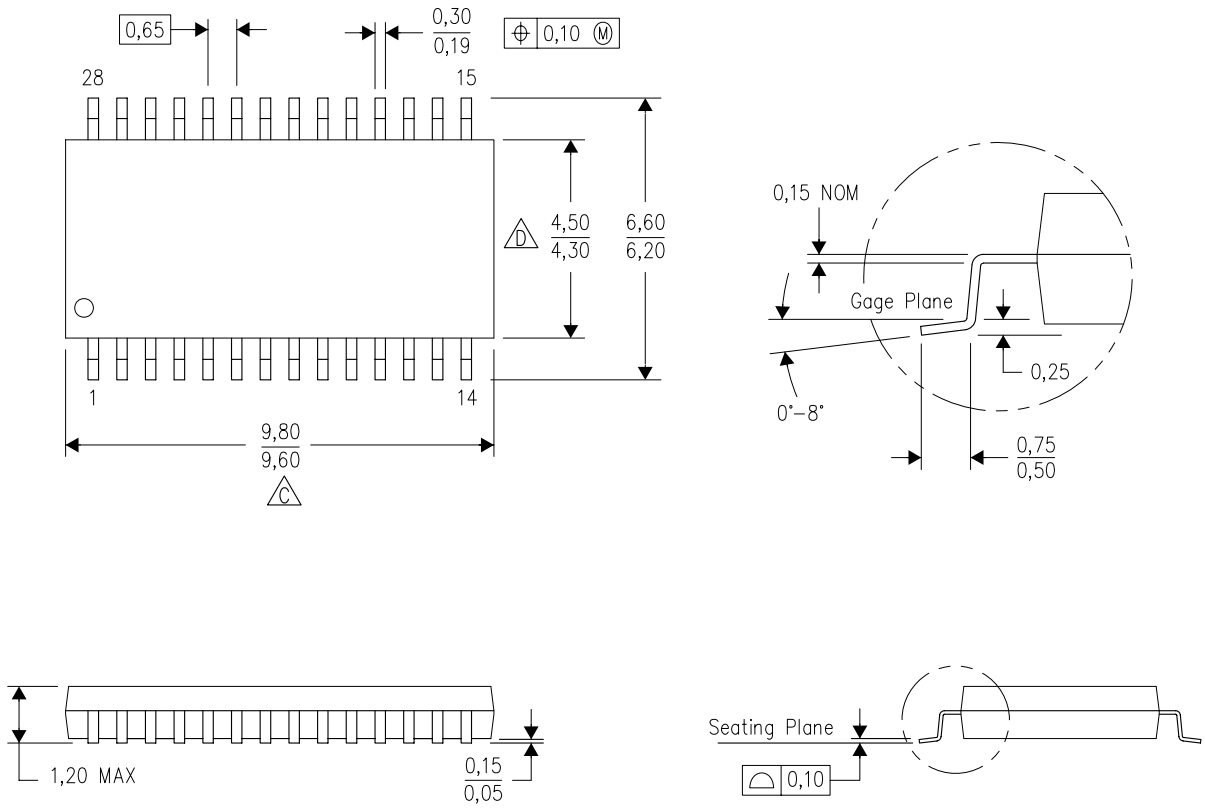
TUBE



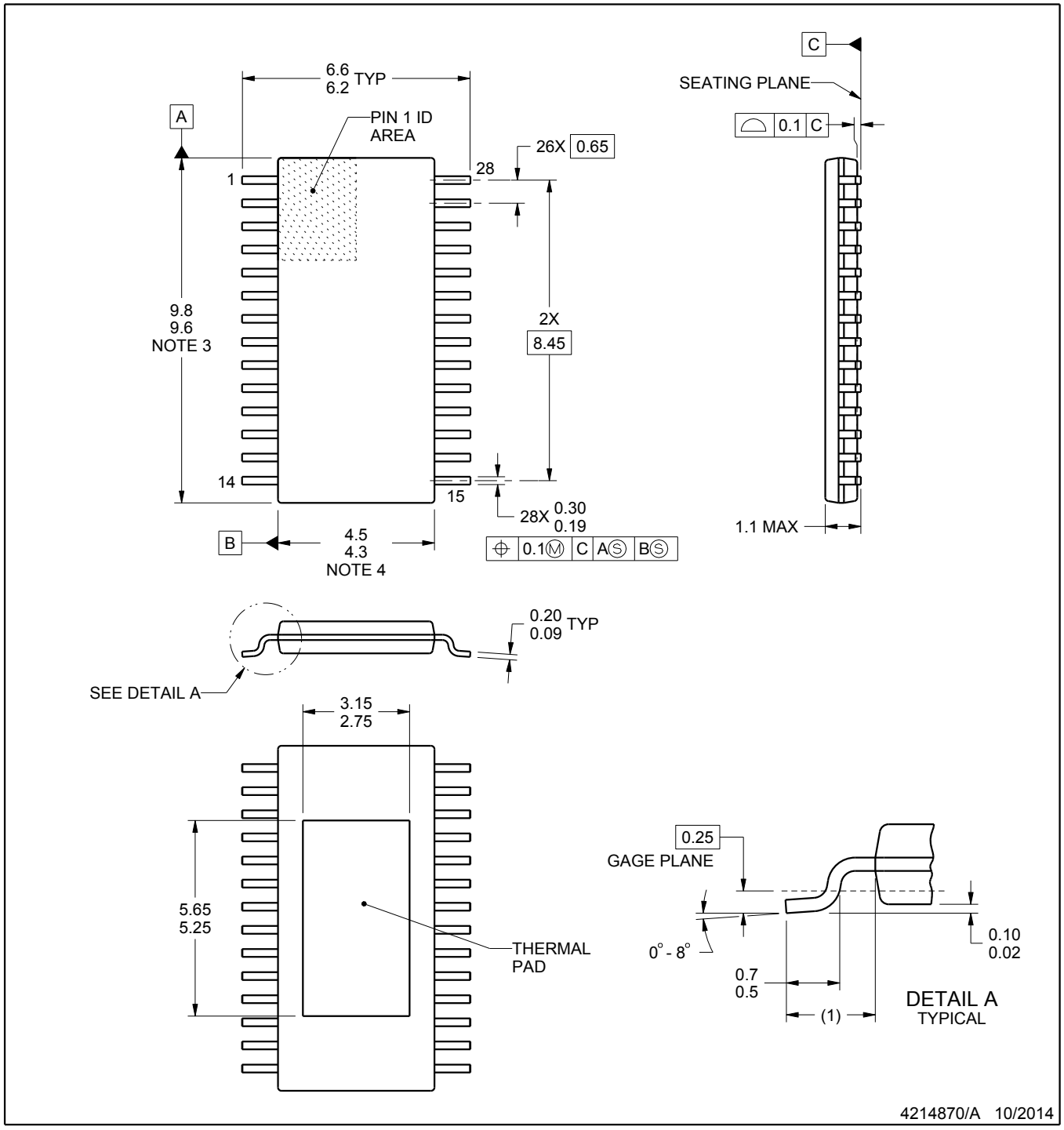
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM5642MH/NOPB	PWP	HTSSOP	28	48	495	8	2514.6	4.06
LM5642MTC	PW	TSSOP	28	48	495	8	2514.6	4.06
LM5642MTC	PW	TSSOP	28	48	495	8	2514.6	4.06
LM5642MTC/NOPB	PW	TSSOP	28	48	495	8	2514.6	4.06
LM5642XMH/NOPB	PWP	HTSSOP	28	48	495	8	2514.6	4.06
LM5642XMT/NOPB	PW	TSSOP	28	48	495	8	2514.6	4.06

PW (R-PDSO-G28) PLASTIC SMALL OUTLINE



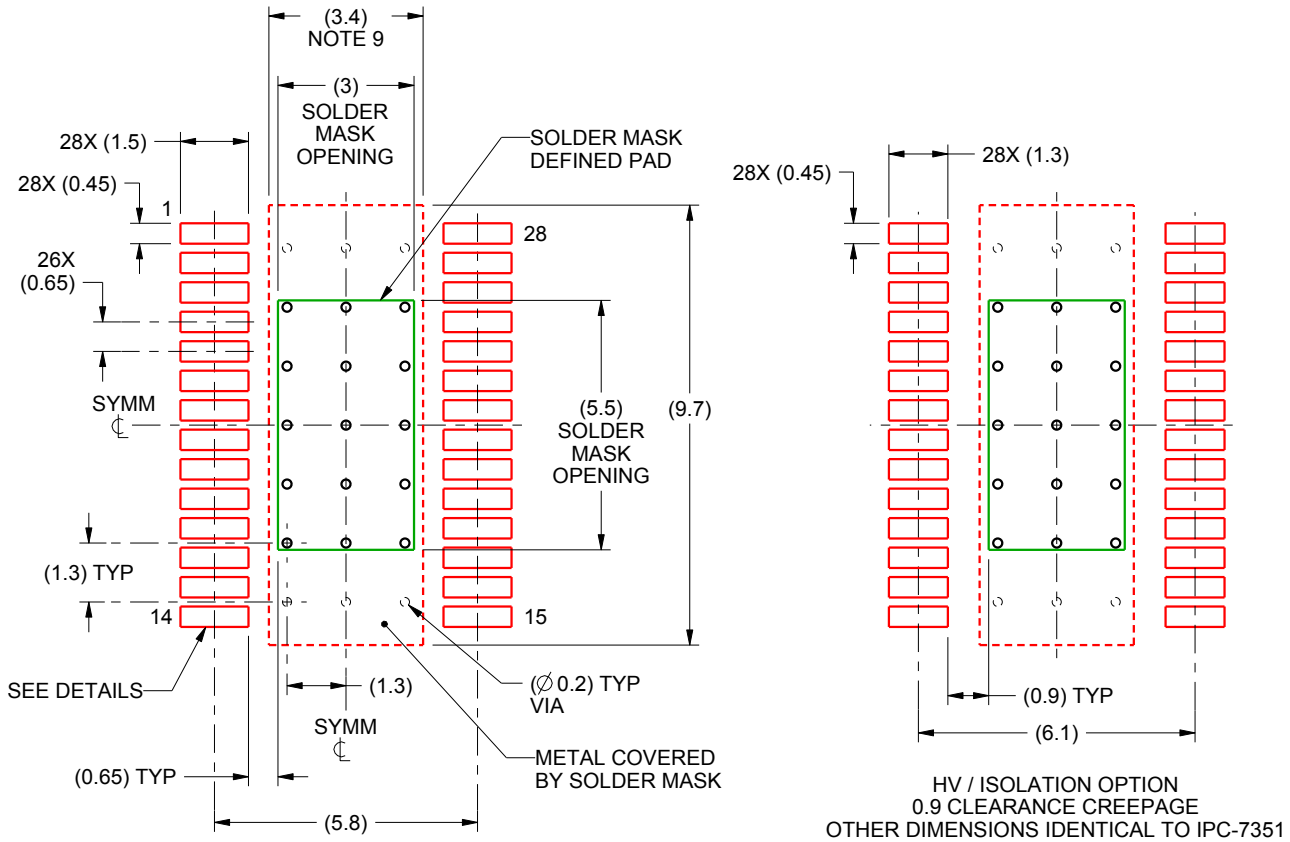
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153



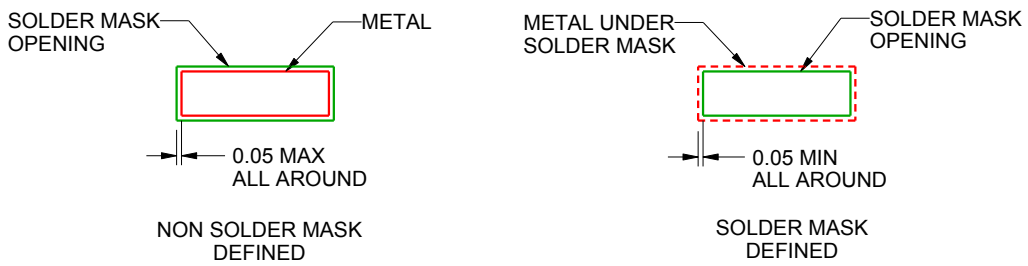
NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MO-153, variation AET.



LAND PATTERN EXAMPLE
SCALE:6X

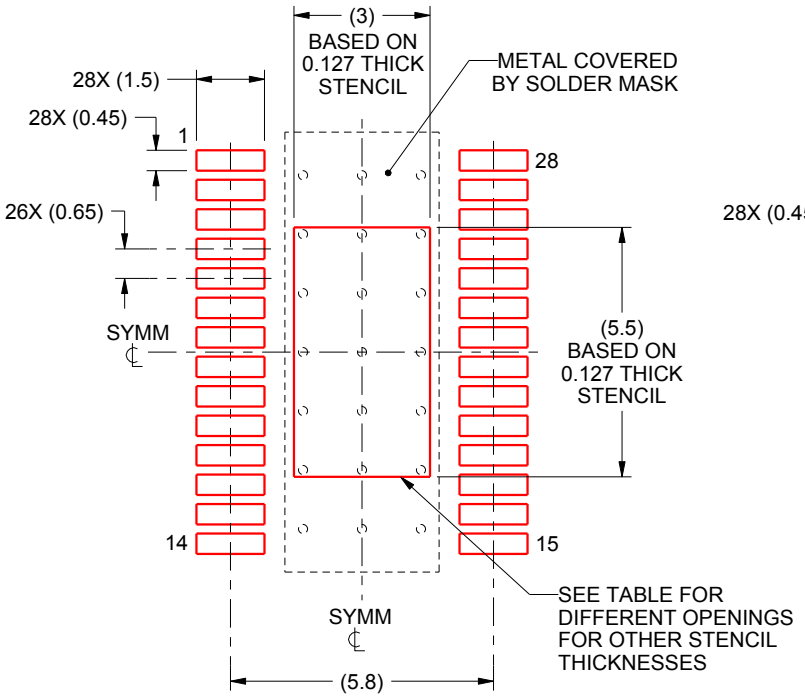


SOLDER MASK DETAILS

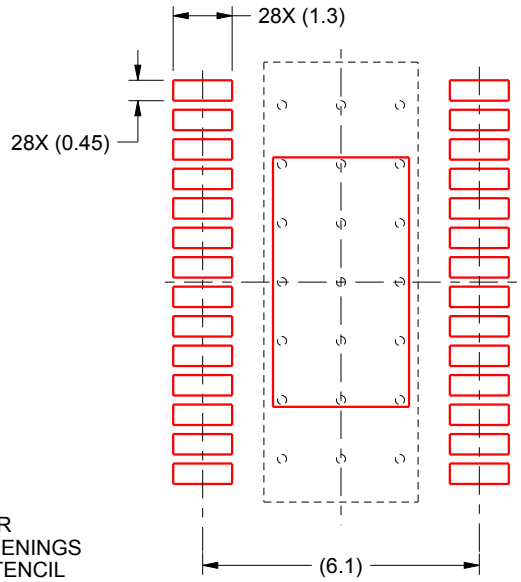
4214870/A 10/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



IPC-7351 NOMINAL
0.65 CLEARANCE CREEPAGE



HV / ISOLATION OPTION
0.9 CLEARANCE CREEPAGE
OTHER DIMENSIONS IDENTICAL TO IPC-7351

SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.55 X 6.37
0.127	3.0 X 5.5 (SHOWN)
0.152	2.88 X 5.16
0.178	2.66 X 4.77

4214870/A 10/2014

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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