

## LM833 Dual High-Speed Audio Operational Amplifier

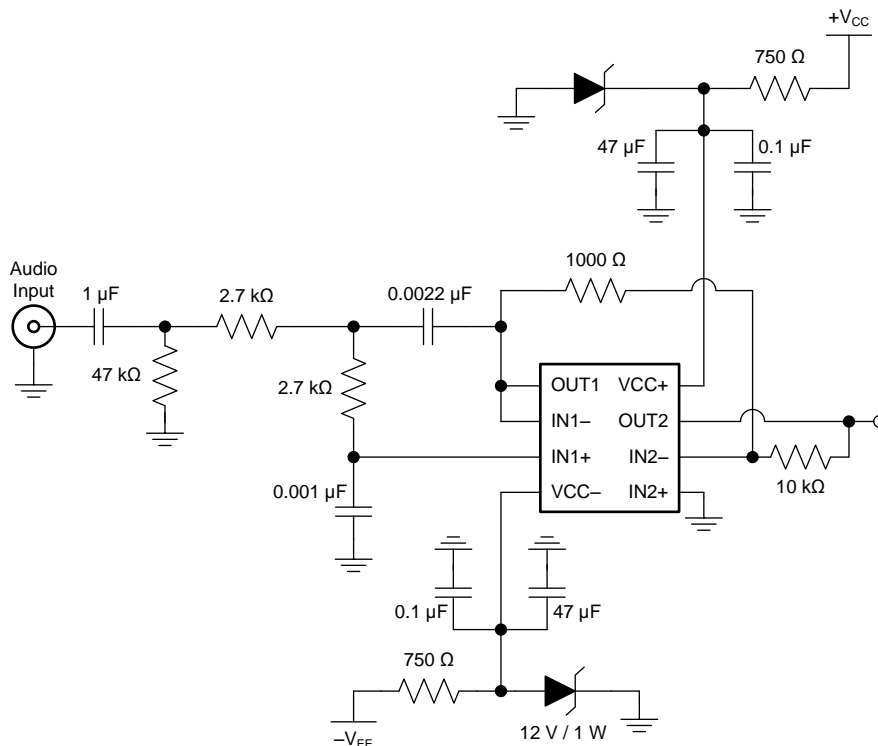
### 1 Features

- Dual-Supply Operation:  $\pm 5$  V to  $\pm 18$  V
- Low Noise Voltage:  $4.5 \text{ nV}/\sqrt{\text{Hz}}$
- Low Input Offset Voltage: 0.15 mV
- Low Total Harmonic Distortion: 0.002%
- High Slew Rate:  $7 \text{ V}/\mu\text{s}$
- High-Gain Bandwidth Product: 16 MHz
- High Open-Loop AC Gain: 800 at 20 kHz
- Large Output-Voltage Swing:  $-14.6 \text{ V}$  to  $14.1 \text{ V}$
- Excellent Gain and Phase Margins
- Available in 8-Terminal MSOP Package (3.0 mm x 4.9 mm x 0.65 mm)

### 2 Applications

- HiFi Audio System Equipment
- Pre amplification and Filtering
- Set-Top Box
- Microphone Pre amplifier Circuit
- General-Purpose Amplifier Applications

### 4 Typical Design Example Audio Pre-Amplifier



### 3 Description

The LM833 device is a dual operational amplifier with high-performance specifications for use in quality audio and data-signal applications. Dual amplifiers are utilized widely in audio circuits optimized for all preamp and high level stages in PCM and HiFi systems. The LM833 device is pin-for-pin compatible with industry-standard dual operation amplifiers. With addition of a preamplifier, the gain of the power stage can be greatly reduced to improve performance.

#### Device Information

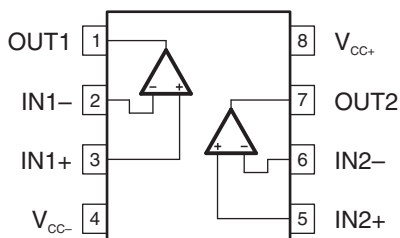
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM833	SOIC (8)	4.90 mm x 3.91 mm
	VSSOP (8)	3.00 mm x 3.00 mm
	PDIP (8)	9.81 mm x 6.35 mm





## 6 Pin Configuration and Functions

D (SOIC), DGK (MSOP), OR P (PDIP) PACKAGE  
(TOP VIEW)



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
IN1+	3	Input	Noninverting input
IN1-	2	Input	Inverting Input
IN2+	5	Input	Noninverting input
IN2-	6	Input	Inverting Input
OUT1	1	Output	Output 1
OUT2	7	Output	Output 2
V <sub>CC+</sub>	8	—	Positive Supply
V <sub>CC-</sub>	4	—	Negative Supply

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC+</sub>	Supply voltage <sup>(2)</sup>		18	V
V <sub>CC-</sub>	Supply voltage <sup>(2)</sup>		-18	V
V <sub>CC+</sub> – V <sub>CC-</sub>	Supply voltage		36	V
	Input voltage, either input <sup>(2)(3)</sup>	V <sub>CC-</sub>	V <sub>CC+</sub>	V
	Input current <sup>(4)</sup>		±10	mA
	Duration of output short circuit <sup>(5)</sup>	Unlimited		
T <sub>J</sub>	Operating virtual junction temperature		150	°C

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- All voltage values, except differential voltages, are with respect to the midpoint between V<sub>CC+</sub> and V<sub>CC-</sub>.
- The magnitude of the input voltage must never exceed the magnitude of the supply voltage.
- Excessive input current will flow if a differential input voltage in excess of approximately 0.6 V is applied between the inputs, unless some limiting resistance is used.
- The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

### 7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
T <sub>stg</sub>	Storage temperature range	-65	150	°C
V <sub>(ESD)</sub>	Human-Body Model (HBM) <sup>(1)</sup>	0	2.5	kV
	Charged-Device Model (CDM) <sup>(2)</sup>	0	1.5	

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V <sub>CC-</sub>	Supply voltage	-5	-18	V
V <sub>CC+</sub>		5	18	
T <sub>A</sub>	Operating free-air temperature range	-40	85	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LM833			UNIT
		D	DGK	P	
		8 PINS			
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(2)(3)</sup>	97	172	85	°C/W

- For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).
- Maximum power dissipation is a function of T<sub>J(max)</sub>, θ<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J(max)</sub> – T<sub>A</sub>) / θ<sub>JA</sub>. Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.
- The package thermal impedance is calculated in accordance with JESD 51-7.

## 7.5 Electrical Characteristics

 $V_{CC-} = -15\text{ V}$ ,  $V_{CC+} = 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
$V_{IO}$	Input offset voltage	$V_O = 0$ , $R_S = 10\ \Omega$ , $V_{CM} = 0$	$T_A = 25^\circ\text{C}$	0.15	2	3	mV	
			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$					
$\alpha V_{IO}$	Input offset voltage temperature coefficient	$V_O = 0$ , $R_S = 10\ \Omega$ , $V_{CM} = 0$	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		2		$\mu\text{V}/^\circ\text{C}$	
$I_{IB}$	Input bias current	$V_O = 0$ , $V_{CM} = 0$	$T_A = 25^\circ\text{C}$	300	750	800	nA	
			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$					
$I_{IO}$	Input offset current	$V_O = 0$ , $V_{CM} = 0$	$T_A = 25^\circ\text{C}$	25	150	175	nA	
			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$					
$V_{ICR}$	Common-mode input voltage range	$\Delta V_{IO} = 5\text{ mV}$ , $V_O = 0$		$\pm 13$	$\pm 14$		V	
$A_{VD}$	Large-signal differential voltage amplification	$R_L \geq 2\text{ k}\Omega$ , $V_O = \pm 10\text{ V}$	$T_A = 25^\circ\text{C}$	90	110	85	dB	
			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$					
$V_{OM}$	Maximum output voltage swing	$V_{ID} = \pm 1\text{ V}$	$R_L = 600\ \Omega$	$V_{OM+}$	10.7		V	
				$V_{OM-}$	-11.9			
			$R_L = 2000\ \Omega$	$V_{OM+}$	13.2	13.8		
				$V_{OM-}$	-13.2	-13.7		
			$R_L = 10,000\ \Omega$	$V_{OM+}$	13.5	14.1		
				$V_{OM-}$	-14	-14.6		
CMMR	Common-mode rejection ratio	$V_{IN} = \pm 13\text{ V}$		80	100		dB	
$k_{SVR}^{(1)}$	Supply-voltage rejection ratio	$V_{CC+} = 5\text{ V}$ to $15\text{ V}$ , $V_{CC-} = -5\text{ V}$ to $-15\text{ V}$		80	105		dB	
$I_{OS}$	Output short-circuit current	$ V_{ID}  = 1\text{ V}$ , Output to GND	Source current	15	29	-20	-37	mA
			Sink current					
$I_{CC}$	Supply current (per channel)	$V_O = 0$	$T_A = 25^\circ\text{C}$	2.05	2.5	2.75	mA	
			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$					

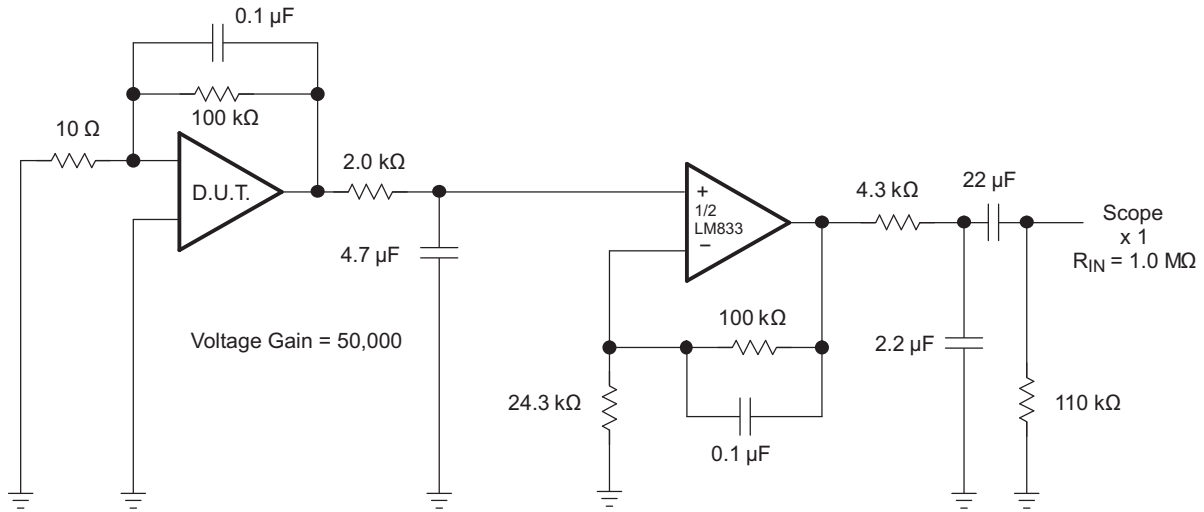
(1) Measured with  $V_{CC\pm}$  differentially varied at the same time

## 7.6 Operating Characteristics

 $V_{CC-} = -15\text{ V}$ ,  $V_{CC+} = 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

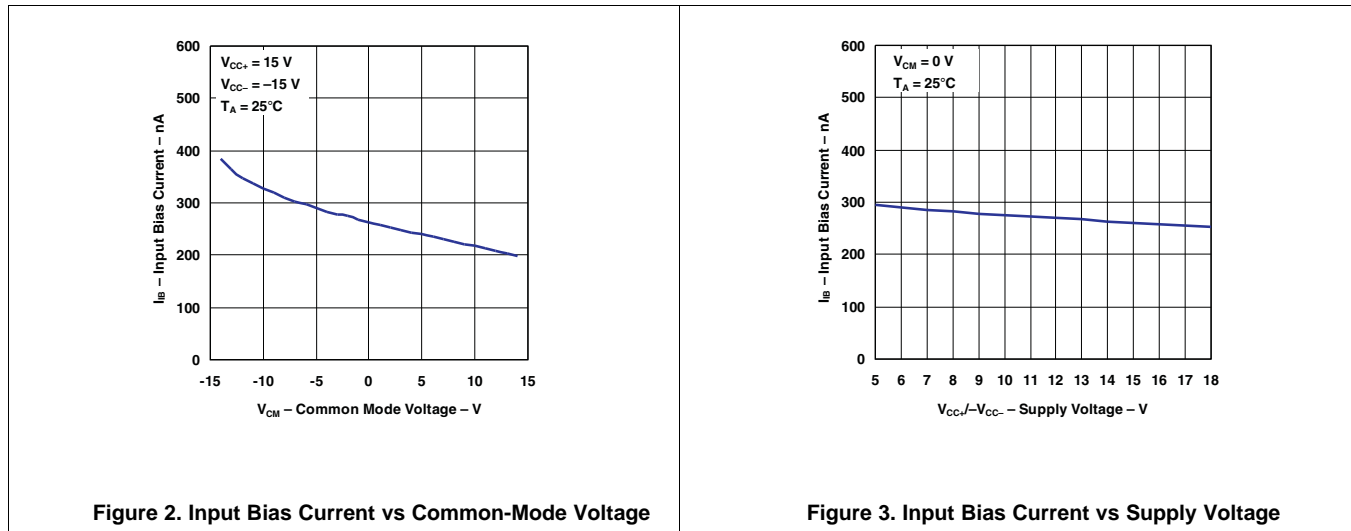
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$A_{VD} = 1$ , $V_{IN} = -10\text{ V}$ to $10\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$		5	7		V/ $\mu\text{s}$
GBW	Gain bandwidth product	$f = 100\text{ kHz}$		10	16		MHz
$B_1$	Unity gain frequency	Open loop			9		MHz
$G_m$	Gain margin	$R_L = 2\text{ k}\Omega$	$C_L = 0\text{ pF}$		-11		dB
			$C_L = 100\text{ pF}$		-6		
$\Phi_m$	Phase margin	$R_L = 2\text{ k}\Omega$	$C_L = 0\text{ pF}$		55		degrees
			$C_L = 100\text{ pF}$		40		
	Amp-to-amp isolation	$f = 20\text{ Hz}$ to $20\text{ kHz}$			-120		dB
	Power bandwidth	$V_O = 27\text{ V}_{PP}$ , $R_L = 2\text{ k}\Omega$ , $\text{THD} \leq 1\%$			120		kHz
THD	Total harmonic distortion	$V_O = 3\text{ V}_{rms}$ , $A_{VD} = 1$ , $R_L = 2\text{ k}\Omega$ , $f = 20\text{ Hz}$ to $20\text{ kHz}$			0.002%		
$z_o$	Open-loop output impedance	$V_O = 0$ , $f = 9\text{ MHz}$			37		$\Omega$
$r_{id}$	Differential input resistance	$V_{CM} = 0$			175		k $\Omega$
$C_{id}$	Differential input capacitance	$V_{CM} = 0$			12		pF
$V_n$	Equivalent input noise voltage	$f = 1\text{ kHz}$ , $R_S = 100\ \Omega$			4.5		nV/ $\sqrt{\text{Hz}}$
$I_n$	Equivalent input noise current	$f = 1\text{ kHz}$			0.5		pA/ $\sqrt{\text{Hz}}$

### 7.7 Typical Characteristics



NOTE: All capacitors are non-polarized.

Figure 1. Voltage Noise Test Circuit (0.1 Hz to 10 Hz)



Typical Characteristics (continued)

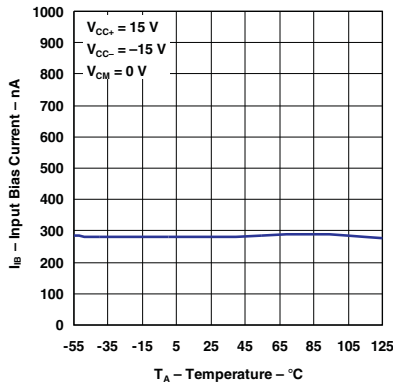


Figure 4. Input Bias Current vs Temperature

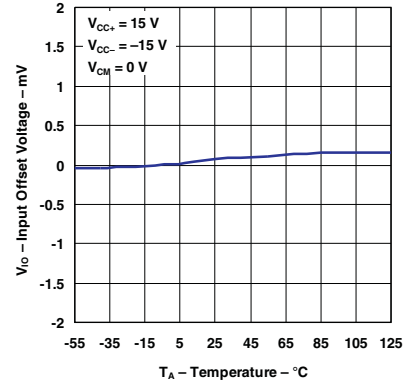


Figure 5. Input Offset Voltage vs Temperature

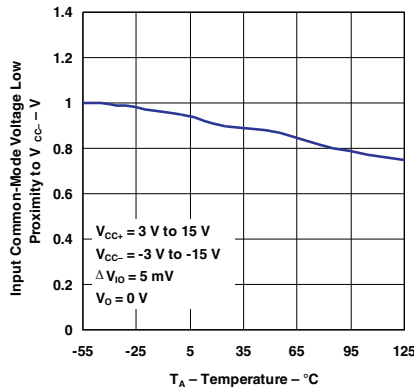


Figure 6. Input Common-Mode Voltage Low Proximity to  $V_{CC-}$  vs Temperature

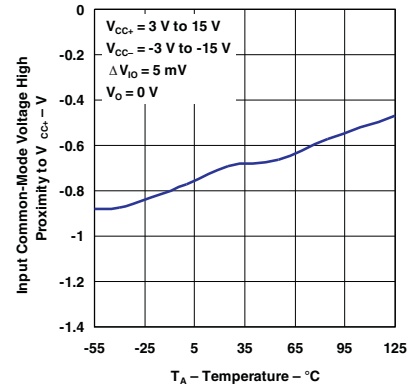


Figure 7. Input Common-Mode Voltage High Proximity to  $V_{CC+}$  vs Temperature

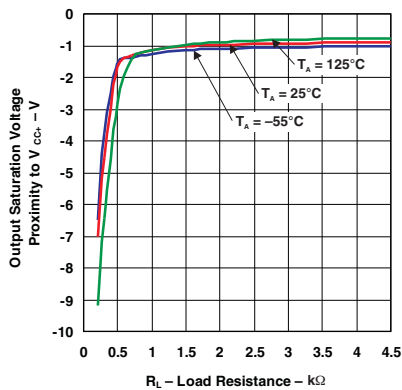


Figure 8. Output Saturation Voltage Proximity to  $V_{CC+}$  vs Load Resistance

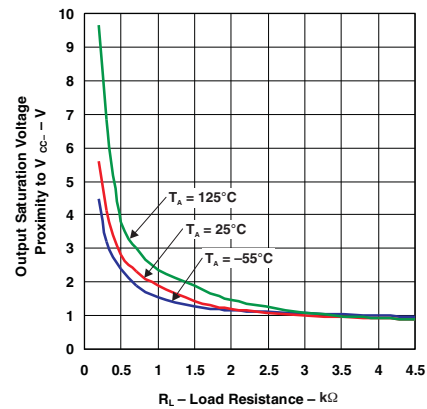


Figure 9. Output Saturation Voltage Proximity to  $V_{CC-}$  vs Load Resistance

Typical Characteristics (continued)

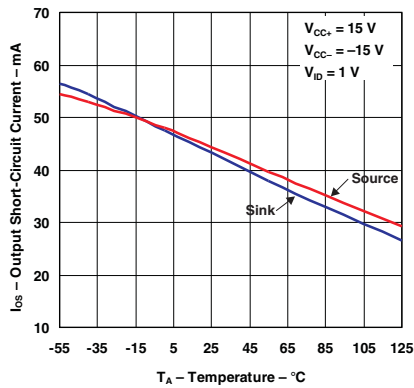


Figure 10. Output Short-Circuit Current vs Temperature

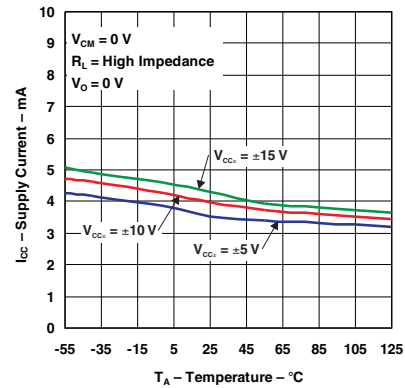


Figure 11. Supply Current vs Temperature

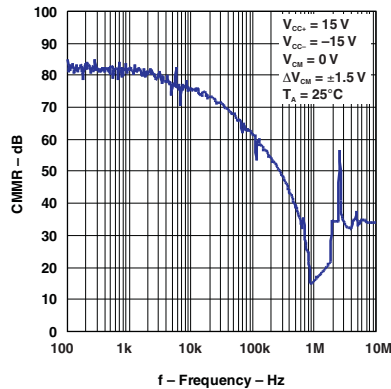


Figure 12. CMRR vs Frequency

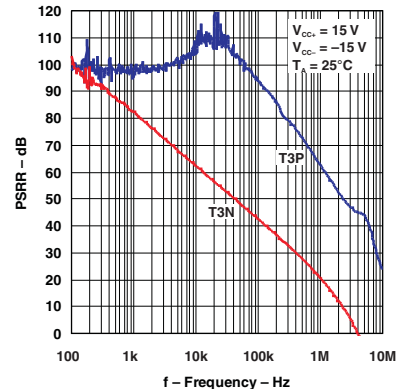


Figure 13. PSSR vs Frequency

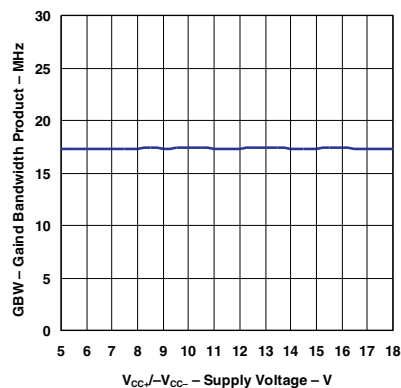


Figure 14. Gain Bandwidth Product vs Supply Voltage

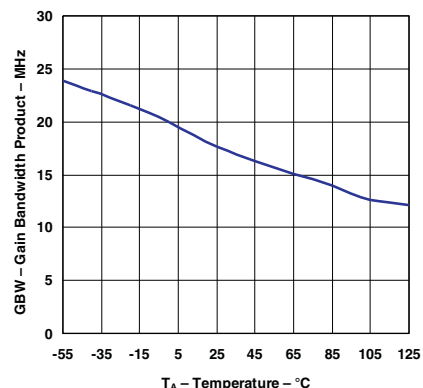


Figure 15. Gain Bandwidth Product vs Temperature

Typical Characteristics (continued)

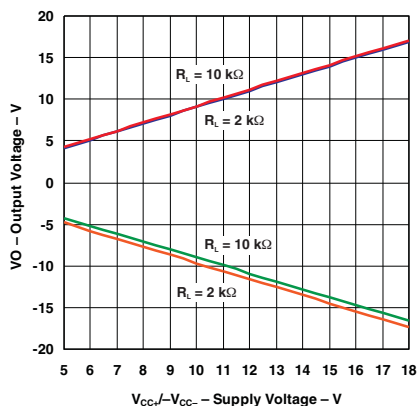


Figure 16. Output Voltage vs Supply Voltage

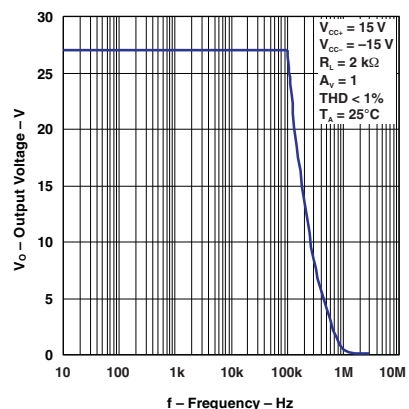


Figure 17. Output Voltage vs Frequency

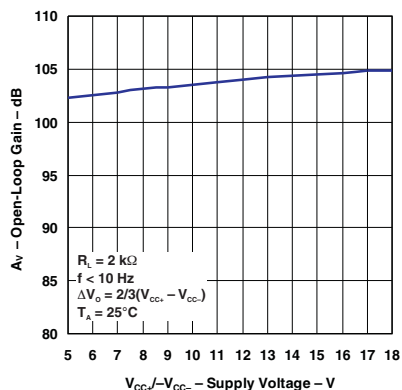


Figure 18. Open-Loop Gain vs Supply Voltage

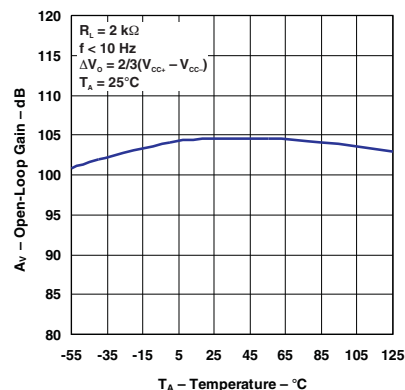


Figure 19. Open-Loop Gain vs Temperature

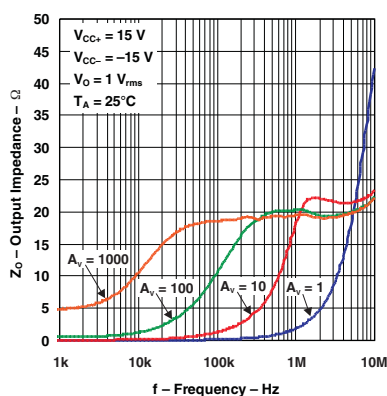


Figure 20. Output Impedance vs Frequency

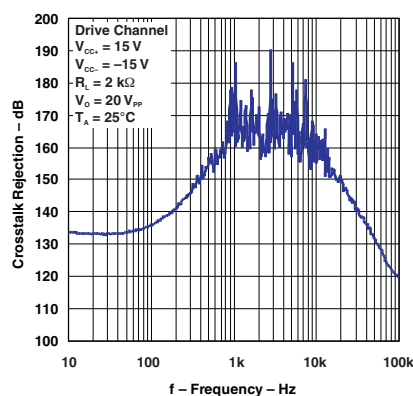


Figure 21. Crosstalk Rejection vs Frequency

Typical Characteristics (continued)

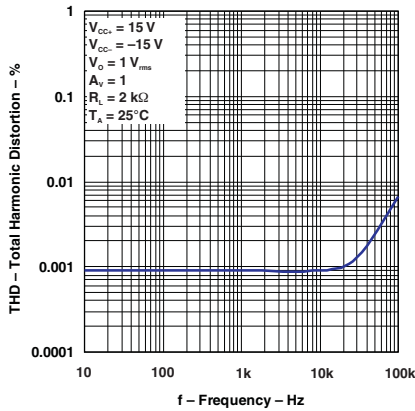


Figure 22. Total Harmonic Distortion vs Frequency

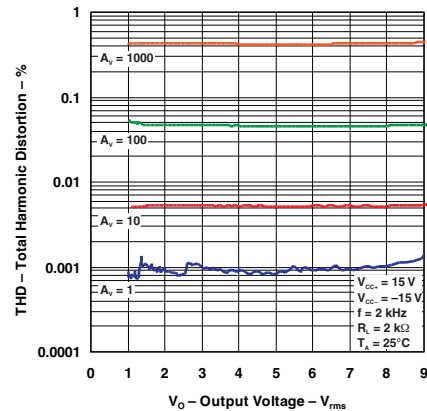


Figure 23. Total Harmonic Distortion vs Output Voltage

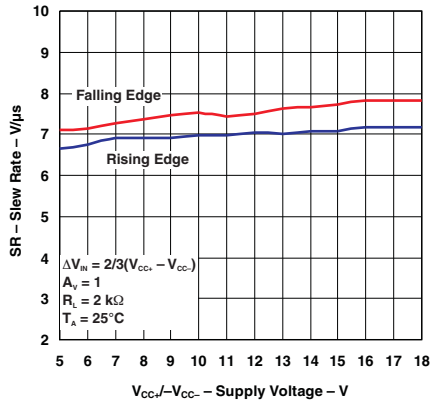


Figure 24. Slew Rate vs Supply Voltage

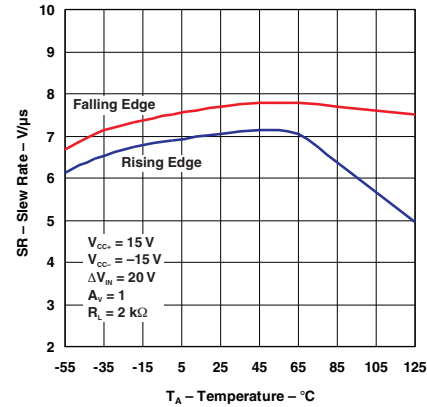


Figure 25. Slew Rate vs Temperature

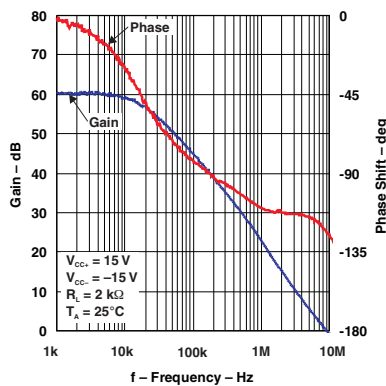


Figure 26. Gain and Phase vs Frequency

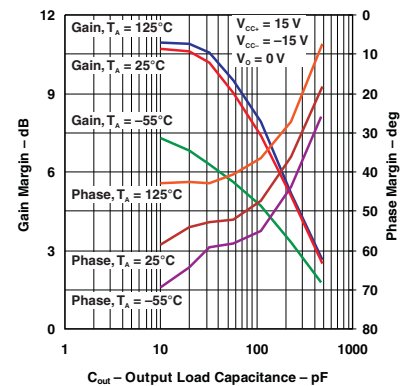


Figure 27. Gain and Phase Margin vs Output Load Capacitance

Typical Characteristics (continued)

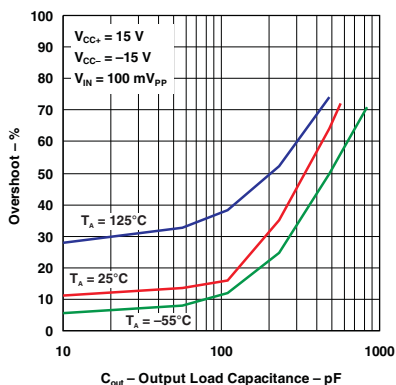


Figure 28. Overshoot vs Output Load Capacitance

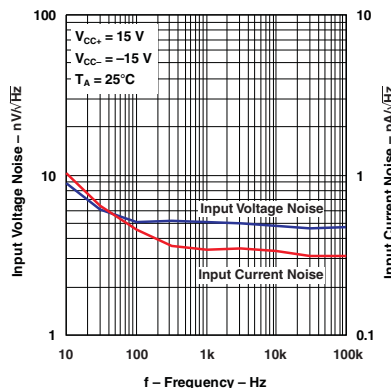


Figure 29. Input Voltage and Current Noise vs Frequency

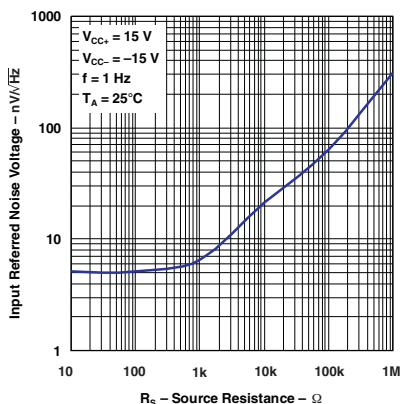


Figure 30. Input Referred Noise Voltage vs Source Resistance

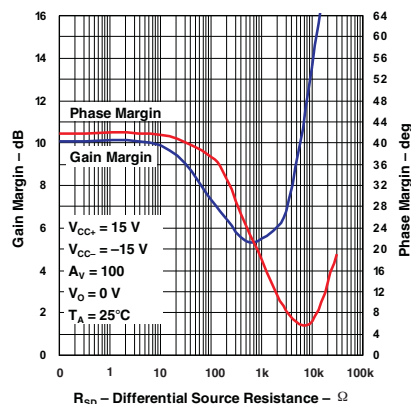


Figure 31. Gain and Phase Margin vs Differential Source Resistance

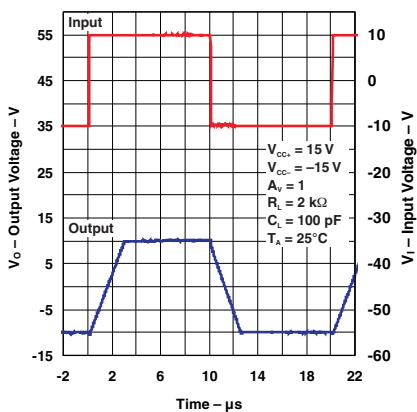


Figure 32. Large Signal Transient Response ( $A_V = 1$ )

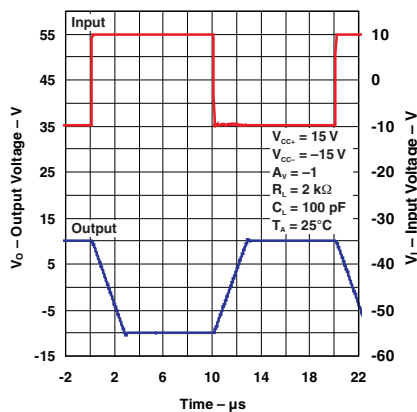
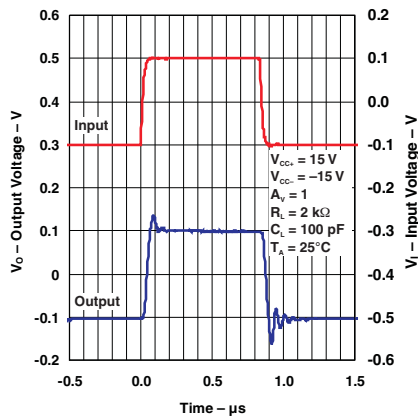
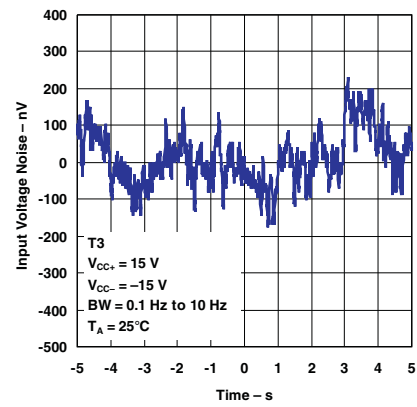


Figure 33. Large Signal Transient Response ( $A_V = -1$ )

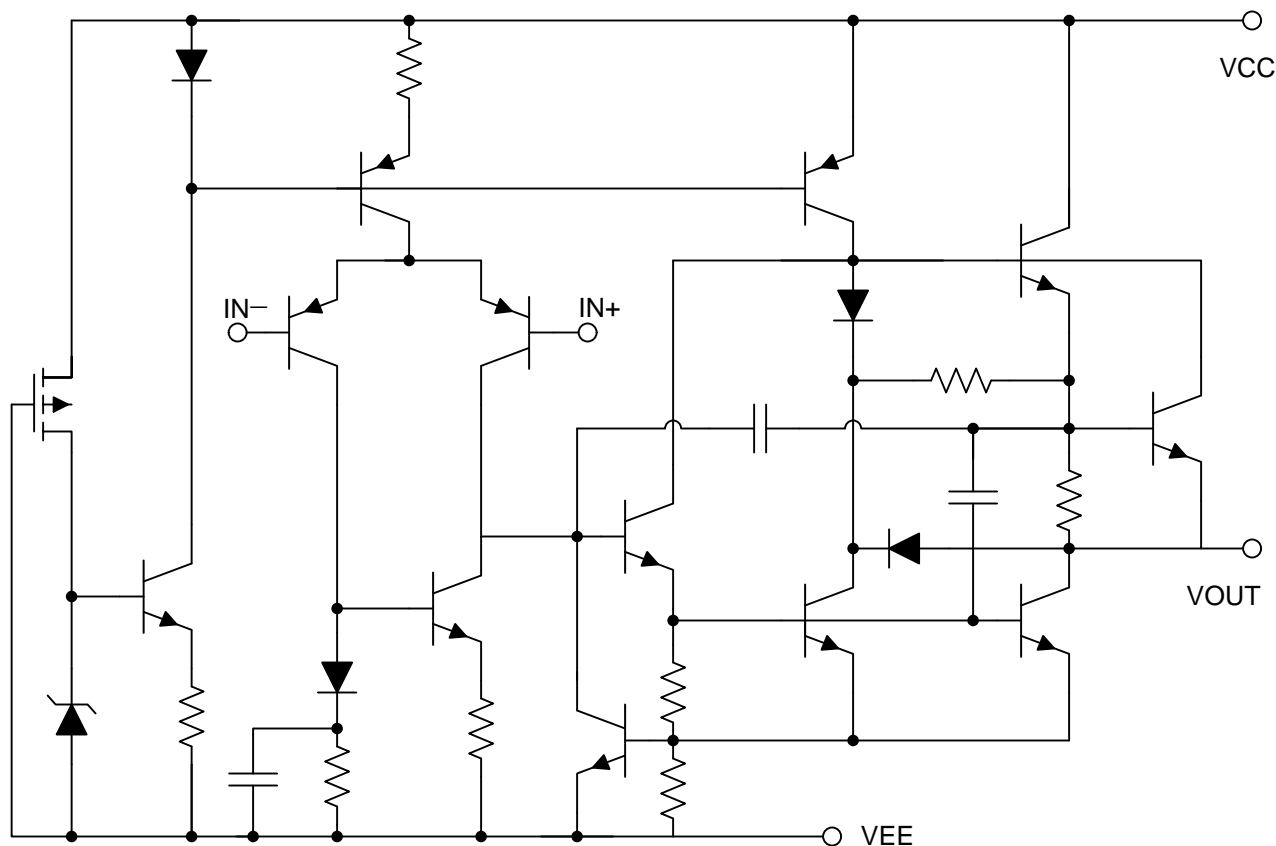
**Typical Characteristics (continued)**

**Figure 34. Small Signal Transient Response**

**Figure 35. Low-Frequency Noise**

## 8 Detailed Description

### 8.1 Overview

The LM833 device is a dual operational amplifier with high-performance specifications for use in quality audio and data-signal applications. This device operates over a wide range of single- and dual-supply voltage with low noise, high-gain bandwidth, and high slew rate. Additional features include low total harmonic distortion, excellent phase and gain margins, large output voltage swing with no deadband crossover distortions, and symmetrical sink/source performance. The dual amplifiers are utilized widely in circuit of audio optimized for all preamp and high-level stages in PCM and HiFi systems. The LM833 device is pin-for-pin compatible with industry-standard dual operation amplifiers' pin assignments. With addition of a preamplifier, the gain of the power stage can be greatly reduced to improve performance.

### 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Operating Voltage

The LM833 operational amplifier is fully specified and ensured for operation from  $\pm 5$  V to  $\pm 18$  V. In addition, many specifications apply from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . Parameters that vary significantly with operating voltages or temperature are shown in [Absolute Maximum Ratings](#).

### 8.3.2 High Gain Bandwidth Product

Gain bandwidth product is found by multiplying the measured bandwidth of an amplifier by the gain at which that bandwidth was measured. The LM833 has a high gain bandwidth of 16 MHz which stays relatively stable over a wide range of supply voltages. Parameters that vary significantly with temperature are shown in [Figure 14](#).

### 8.3.3 Low Total Harmonic Distortion

Harmonic distortions to an audio signal are created by electronic components in a circuit. Total harmonic distortion (THD) is a measure of harmonic distortions accumulated by a signal in an audio system. The LM833 has a very low THD of 0.002% meaning that the LM833 will add little harmonic distortion when used in audio signal applications. More specific characteristics are shown in [Figure 22](#).

## 8.4 Device Functional Modes

The LM833 is powered on when the supply is connected. It can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

An application of the LM833 is the two stage RIAA Phono Preamplifier. A primary task of the phono preamplifier is to provide gain (usually 30 to 40 dB at 1 kHz) and accurate amplitude and phase equalization to the signal from a moving magnet or a moving coil cartridge. In addition to the amplification and equalization functions, the phono preamp must not add significant noise or distortion to the signal from the cartridge. The circuit shown in Figure 36 uses two amplifiers, fulfills these qualifications, and has greatly improved performance over a single-amplifier design.

### 9.2 Typical Application

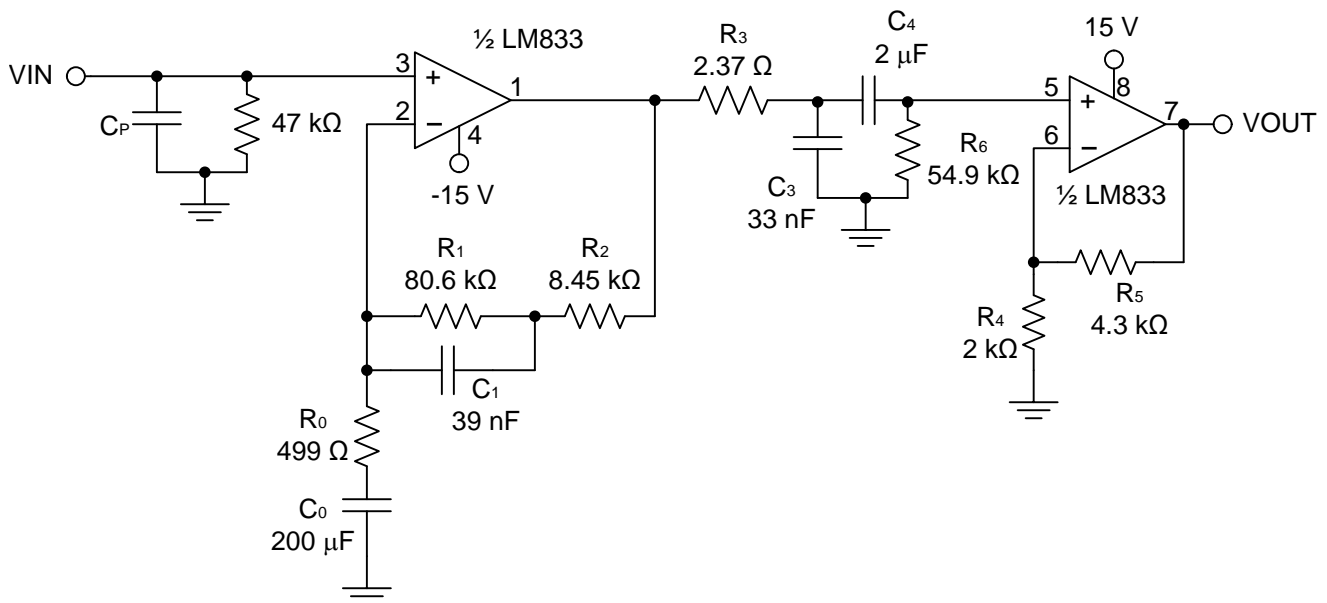


Figure 36. RIAA Phono Preamplifier

#### 9.2.1 Design Requirements

- Supply Voltage =  $\pm 15$  V
- Low-Frequency  $-3$  dB corner of the first amplifier ( $f_0$ ) > 20 Hz (below audible range)
- Low-Frequency  $-3$  dB corner of the second stage ( $f_L$ ) = 20.2 Hz

#### 9.2.2 Detailed Design Procedure

##### 9.2.2.1 Introduction to Design Method

Equation 1 through Equation 5 show the design equations for the preamplifier.

$$R_1 = 8.058 R_0 A_1$$

where

- $A_1$  is the 1 kHz voltage gain of the first amplifier

(1)

**Typical Application (continued)**

$$C_1 = \frac{3.18 \times 10^{-3}}{R_1} \quad (2)$$

$$R_2 = \frac{R_1}{9} - R_0 \quad (3)$$

$$C_3 = 7.5 \times 10^{-5} \frac{(R_3 + R_6)}{R_3 R_6} = \frac{7.5 \times 10^{-5}}{R_P} \quad (4)$$

$$C_4 = \frac{1}{2\pi f_L (R_3 + R_6)}$$

where

- $f_L$  is the low-frequency -3 dB corner of the second stage (5)

For standard RIAA preamplifiers,  $f_L$  should be kept well below the audible frequency range. If the preamplifier is to follow the IEC recommendation (IEC Publication 98, Amendment #4),  $f_L$  should equal 20.2 Hz.

$$A_{V2} = 1 + \frac{R_5}{R_4}$$

where

- $A_{V2}$  is the voltage gain of the second amplifier (6)

$$C_0 \approx \frac{1}{2\pi f_0 R_0}$$

where

- $f_0$  is the low-frequency -3 dB corner of the first amplifier (7)

This should be kept well below the audible frequency range.

A design procedure is shown below with an illustrative example using 1% tolerance E96 components for close conformance to the ideal RIAA curve. Because 1% tolerance capacitors are often difficult to find except in 5% or 10% standard values, the design procedure calls for re-calculation of a few component values so that standard capacitor values can be used.

**9.2.2.2 RIAA Phono Preamplifier Design Procedure**

A design procedure is shown below with an illustrative example using 1% tolerance E96 components for close conformance to the ideal RIAA curve. Since 1% tolerance capacitors are often difficult to find except in 5% or 10% standard values, the design procedure calls for re-calculation of a few component values so that standard capacitor values can be used.

Choose  $R_0$ .  $R_0$  should be small for minimum noise contribution, but not so small that the feedback network excessively loads the amplifier.

Example: Choose  $R_0 = 500$

Choose 1 kHz gain,  $A_{V1}$  of first amplifier. This will typically be around 20 dB to 30 dB.

Example: Choose  $A_{V1} = 26 \text{ dB} = 20$

Calculate  $R_1 = 8.058 R_0 A_{V1}$

Example:  $R_1 = 8.058 \times 500 \times 20 = 80.58 \text{ k}$

$$\text{Calculate } C_1 = \frac{3.18 \times 10^{-3}}{R_1} \quad (8)$$

$$\text{Example: } C_1 = \frac{3.18 \times 10^{-3}}{8.058 \times 10^4} = 0.03946 \mu\text{F} \quad (9)$$

If  $C_1$  is not a convenient value, choose the nearest convenient value and calculate a new  $R_1$  from [Equation 10](#).

**Typical Application (continued)**

$$R_1 = \frac{3.18 \times 10^{-3}}{C_1} \quad (10)$$

Example: New  $C_1 = 0.039 \mu\text{F}$ .

$$\text{New } R_1 = \frac{3.18 \times 10^{-3}}{3.9 \times 10^{-8}} = 81.54 \text{ k}$$

$$\text{Use } R_1 = 80.6 \text{ k} \quad (11)$$

Calculate a new value for  $R_0$  from [Equation 12](#).

$$R_0 = \frac{R_1}{8.058 A_{V1}} \quad (12)$$

$$\text{Example: New } R_0 = \frac{8.06 \times 10^4}{8.058 \times 20} = 498.8 \quad (13)$$

Use  $R_0 = 499$ .

$$\text{Calculate } R_2 = \frac{R_1}{9} - R_0$$

$$\text{Example: } R_2 = \frac{8.06 \times 10^4}{9} - 499 = 8456.56 \quad (14)$$

Use  $R_2 = 8.45 \text{ K}$ .

Choose a convenient value for  $C_3$  in the range from  $0.01 \mu\text{F}$  to  $0.05 \mu\text{F}$ .

Example:  $C_3 = 0.033 \mu\text{F}$

$$\text{Calculate } R_P = \frac{7.5 \times 10^{-5}}{C_3}$$

$$\text{Example: } R_P = \frac{7.5 \times 10^{-5}}{3.3 \times 10^{-8}} = 2.273 \text{ k} \quad (15)$$

Choose a standard value for  $R_3$  that is slightly larger than  $R_P$ .

Example:  $R_3 = 2.37 \text{ k}$

Calculate  $R_6$  from  $1 / R_6 = 1 / R_P - 1 / R_3$

Example:  $R_6 = 55.36 \text{ k}$

Use  $54.9 \text{ k}$

Calculate  $C_4$  for low-frequency rolloff below  $1 \text{ Hz}$  from design [Equation 5](#).

Example:  $C_4 = 2 \mu\text{F}$ . Use a good quality mylar, polystyrene, or polypropylene.

Choose gain of second amplifier.

Example: The  $1 \text{ kHz}$  gain up to the input of the second amplifier is about  $26 \text{ dB}$  for this example. For an overall  $1 \text{ kHz}$  gain equal to about  $36 \text{ dB}$  we choose:

$$A_{V2} = 10 \text{ dB} = 3.16$$

Choose value for  $R_4$ .

Example:  $R_4 = 2 \text{ k}$

Calculate  $R_5 = (A_{V2} - 1) R_4$

### Typical Application (continued)

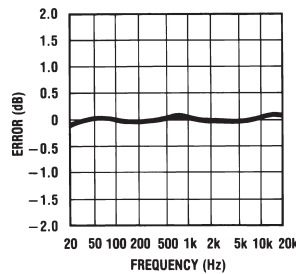
Example:  $R_5 = 4.32 \text{ k}$

Use  $R_5 = 4.3 \text{ k}$

Calculate  $C_0$  for low-frequency rolloff below 1 Hz from design Equation 7.

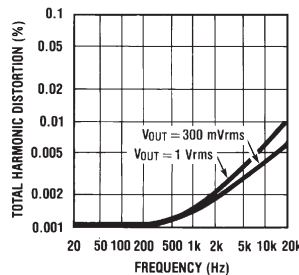
Example:  $C_0 = 200 \text{ }\mu\text{F}$

### 9.2.3 Application Curves for Output Characteristics



The maximum observed error for the prototype was 0.1 dB.

**Figure 37. Deviation from Ideal RIAA Response for Circuit of Figure 36 Using 1% Resistors**



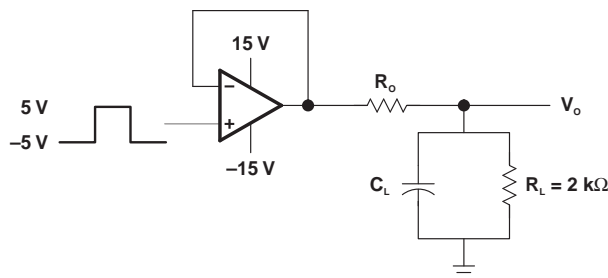
The lower curve is for an output level of 300 mV<sub>rms</sub> and the upper curve is for an output level of 1 V<sub>rms</sub>.

**Figure 38. THD of Circuit in Figure 36 as a Function of Frequency**

### 9.3 Typical Application — Reducing Oscillation from High-Capacitive Loads

While all the previously stated operating characteristics are specified with 100-pF load capacitance, the LM833 device can drive higher-capacitance loads. However, as the load capacitance increases, the resulting response pole occurs at lower frequencies, causing ringing, peaking, or oscillation. The value of the load capacitance at which oscillation occurs varies from lot-to-lot. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem (see Figure 39).

#### 9.3.1 Test Schematic

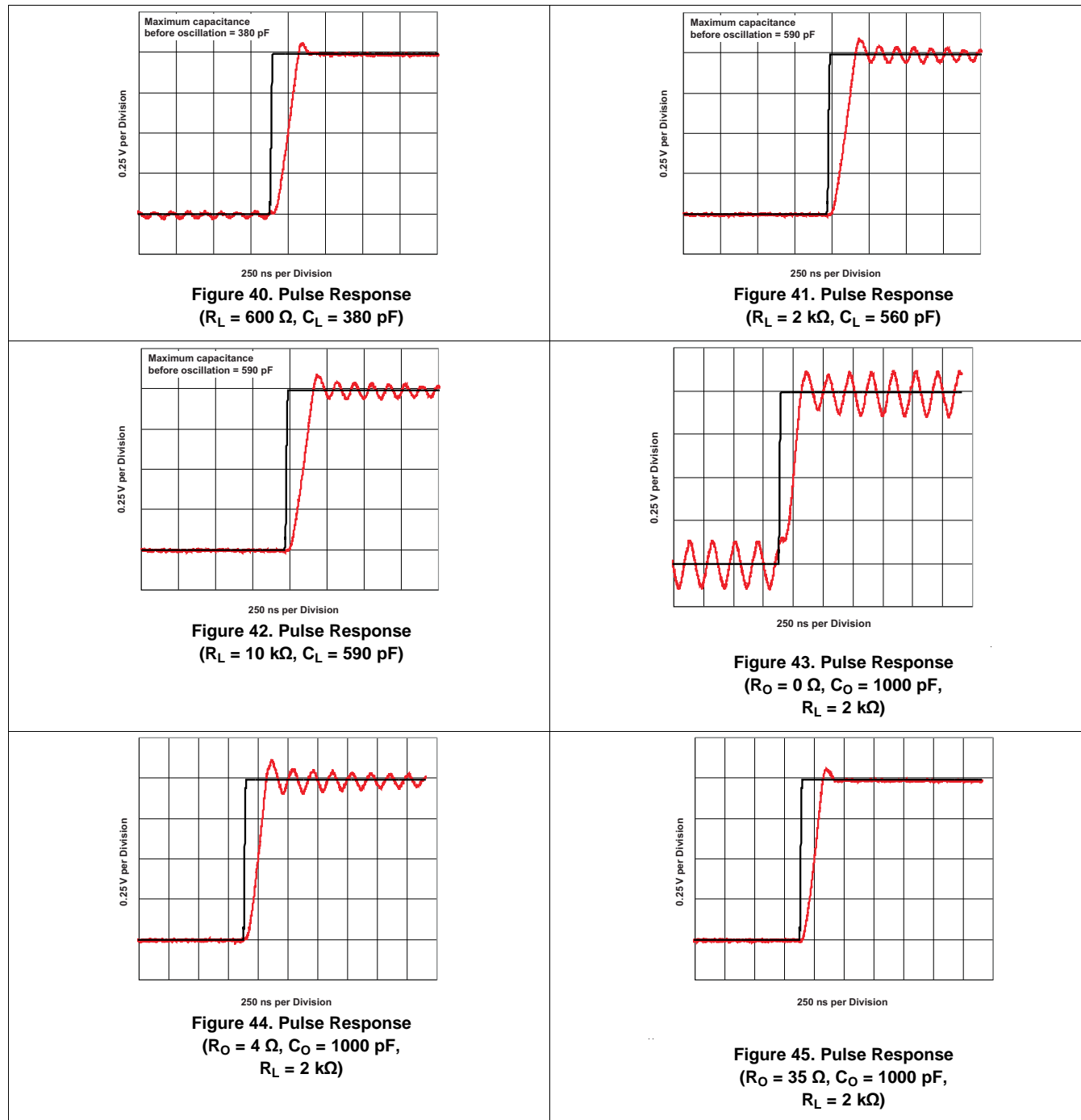


**Figure 39. Capacitive Load Testing Circuit**

Typical Application — Reducing Oscillation from High-Capacitive Loads (continued)

9.3.2 Output Characteristics

Figure 40 through Figure 45 demonstrate the effect adding this small resistance has on the ringing in the output signal.



## 10 Power Supply Recommendations

The LM833 is specified for operation from 10 to 36 V ( $\pm 5$  to  $\pm 18$  V); many specifications apply from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . The [Typical Characteristics](#) section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

### CAUTION

Supply voltages larger than 36 V can permanently damage the device (see [Absolute Maximum Ratings](#)).

Place 0.1- $\mu\text{F}$  bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the [Layout](#) section.

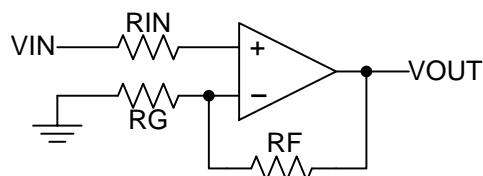
## 11 Layout

### 11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

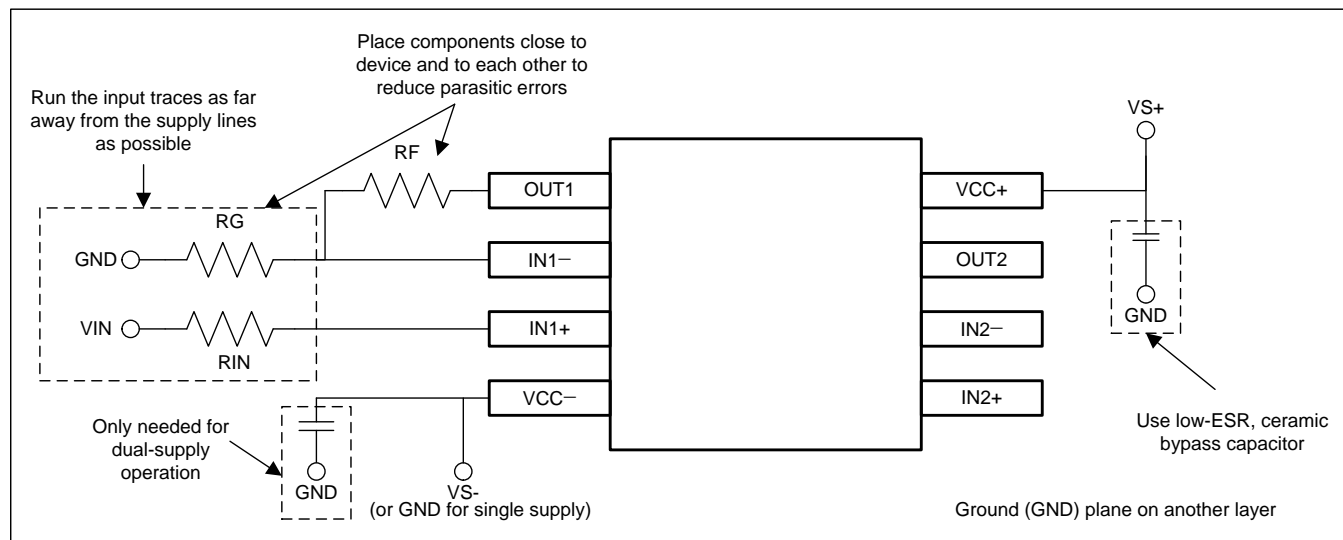
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu\text{F}$  ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from  $V+$  to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to [Circuit Board Layout Techniques](#), (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping  $R_F$  and  $R_G$  close to the inverting input minimizes parasitic capacitance, as shown in [Layout Example](#).
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

### 11.2 Layout Example



**Figure 46. Operational Amplifier Schematic for Noninverting Configuration**

**Layout Example (continued)**



**Figure 47. Operational Amplifier Board Layout for Noninverting Configuration**

## 12 Device and Documentation Support

### 12.1 Trademarks

All trademarks are the property of their respective owners.

### 12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## **13 Mechanical, Packaging, and Orderable Information**

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM833D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM833	<a href="#">Samples</a>
LM833DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RSU	<a href="#">Samples</a>
LM833DGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RSU	<a href="#">Samples</a>
LM833DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM833	<a href="#">Samples</a>
LM833P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	LM833P	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

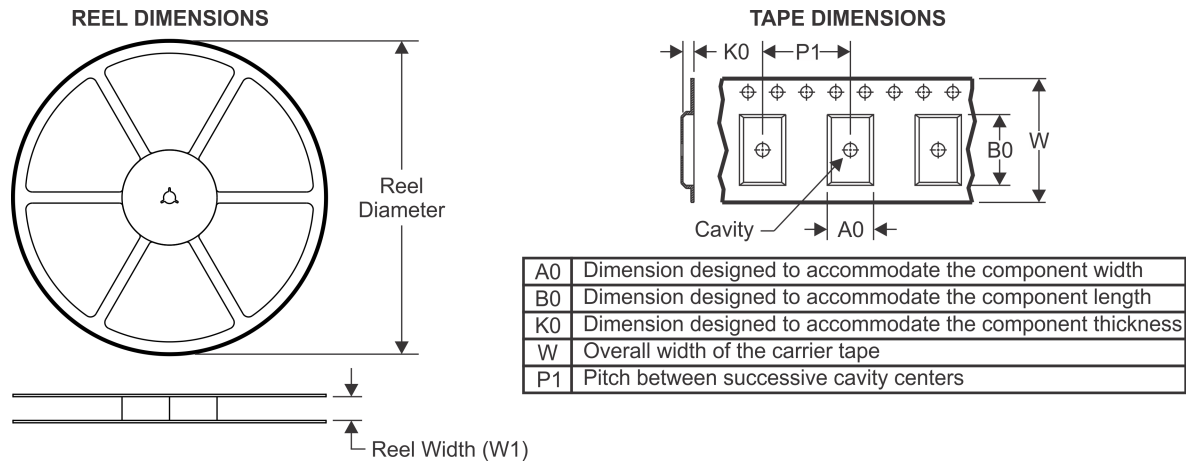
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

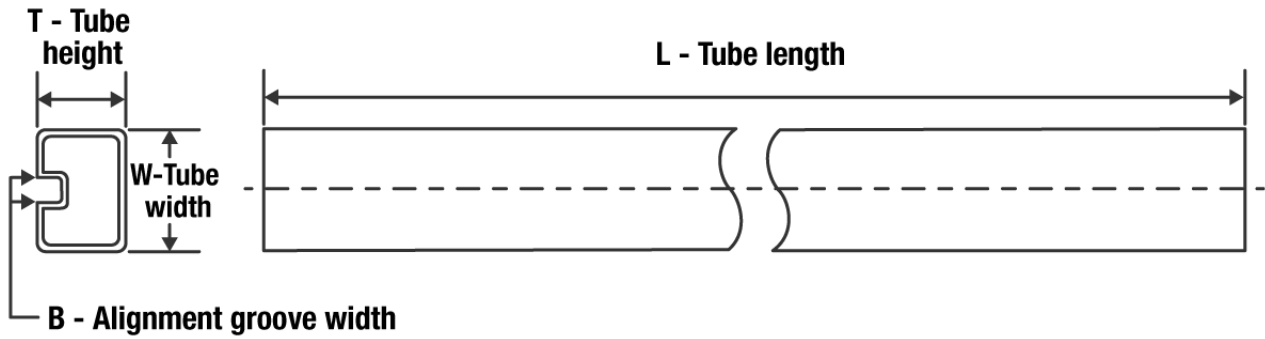

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM833DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
LM833DGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
LM833DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM833DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM833DGKR	VSSOP	DGK	8	2500	346.0	346.0	35.0
LM833DGKT	VSSOP	DGK	8	250	200.0	183.0	25.0
LM833DR	SOIC	D	8	2500	853.0	449.0	35.0
LM833DR	SOIC	D	8	2500	340.5	336.1	25.0

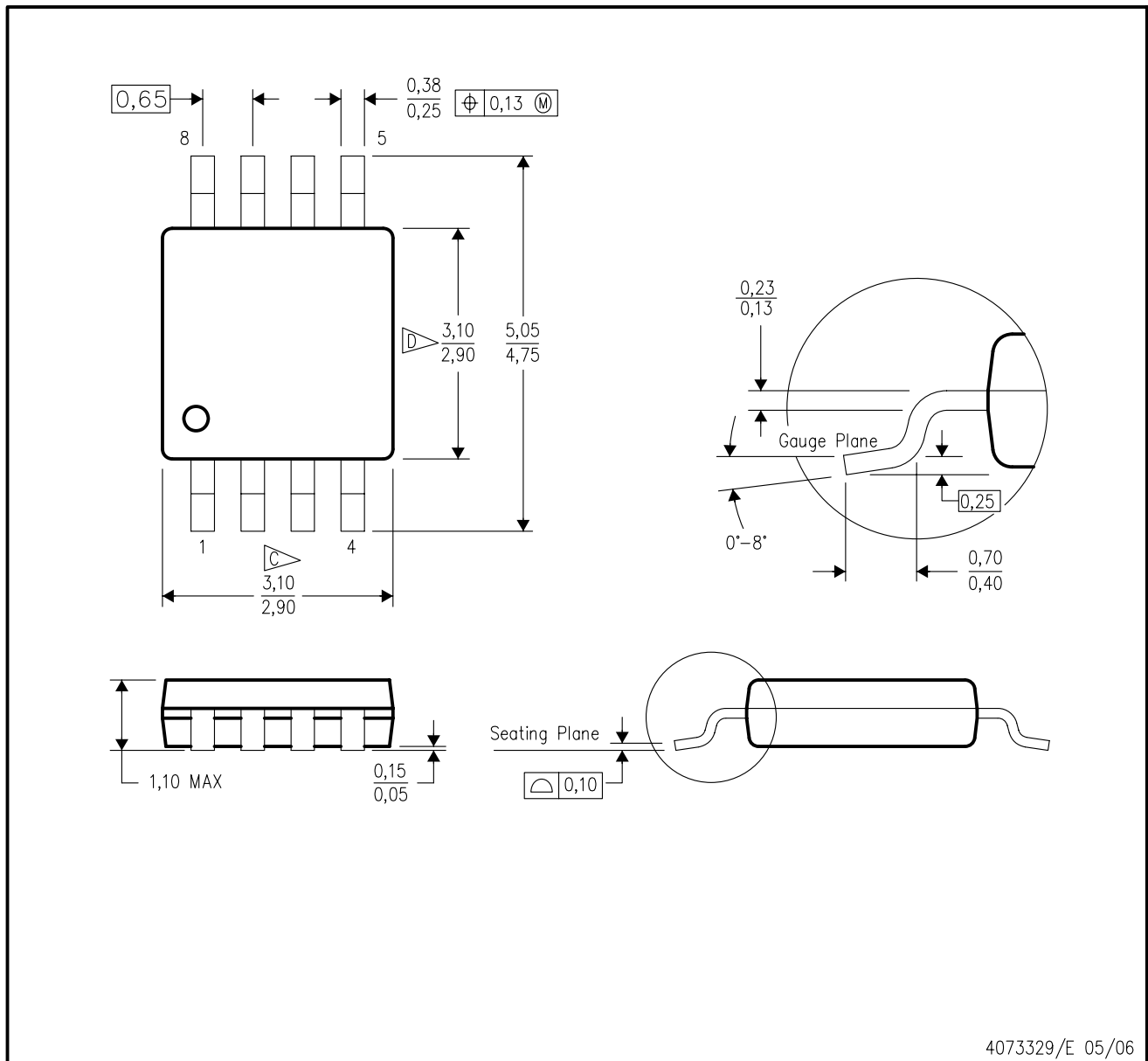
**TUBE**


\*All dimensions are nominal

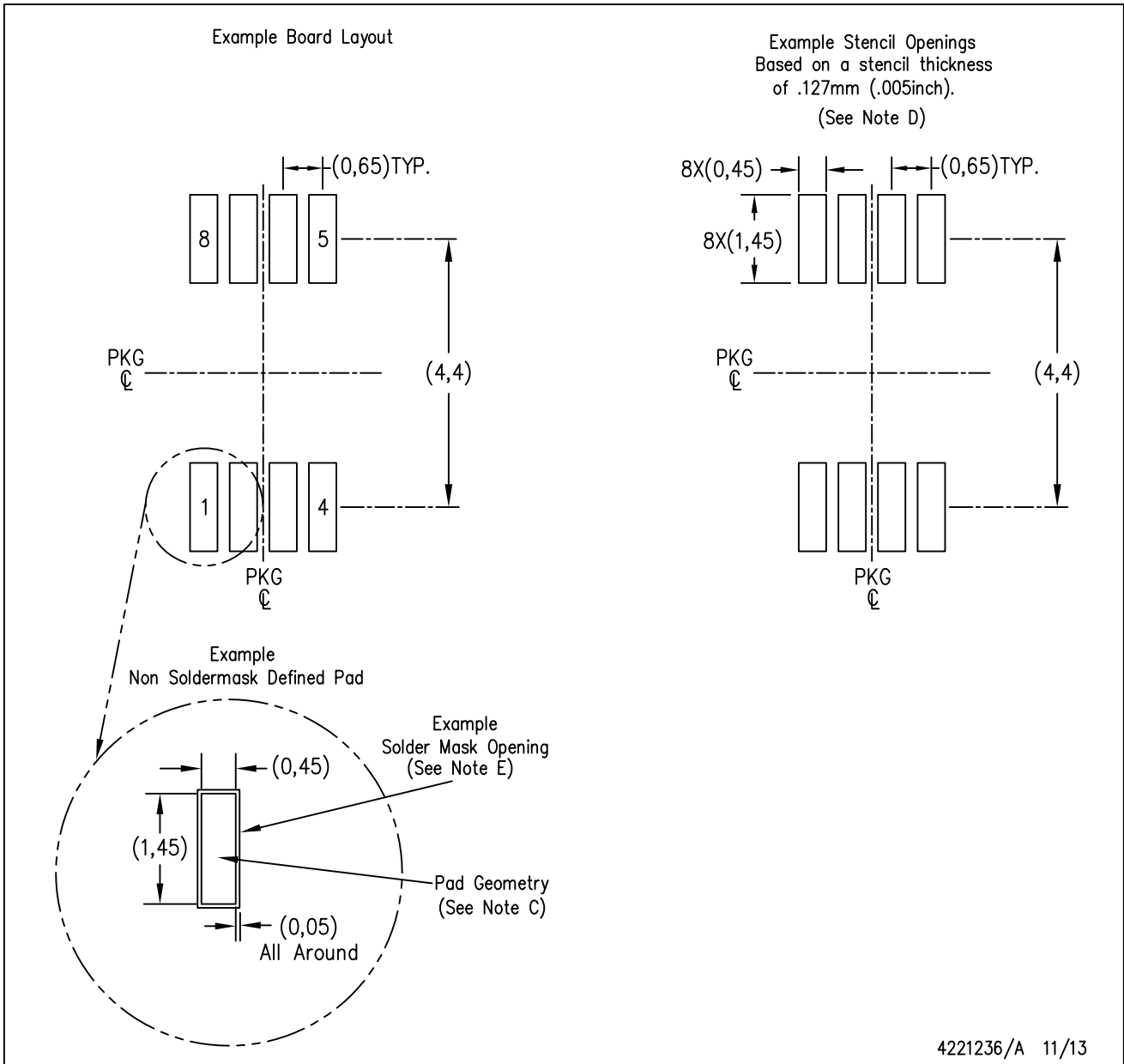
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LM833D	D	SOIC	8	75	506.6	8	3940	4.32
LM833D	D	SOIC	8	75	507	8	3940	4.32
LM833P	P	PDIP	8	50	506	13.97	11230	4.32

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



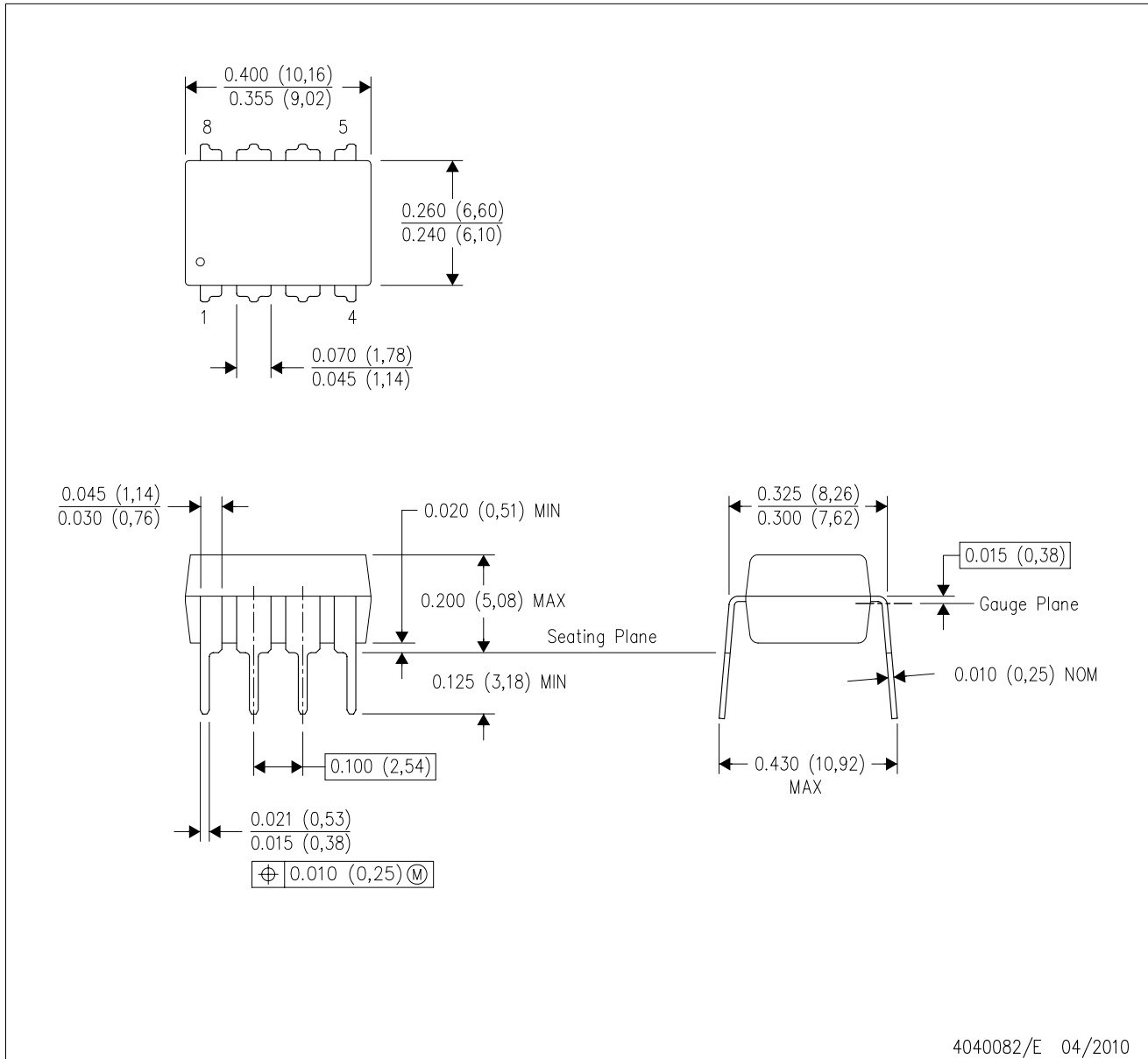
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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