LMC7660 Switched Capacitor Voltage Converter

Check for Samples: LMC7660

FEATURES

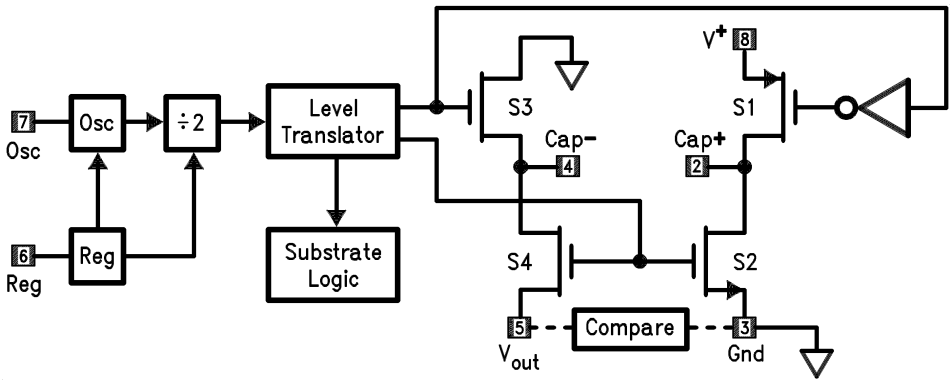
- **Operation Over Full Temperature and Voltage Range without an External Diode**
- **Low Supply Current, 200 µA Max**
- **Pin-for-pin Replacement for the 7660**
- **Wide Operating Range 1.5V to 10V**
- **97% Voltage Conversion Efficiency**
- **95% Power Conversion Efficiency**
- **Easy to Use, Only 2 External Components**
- **Extended Temperature Range**

DESCRIPTION

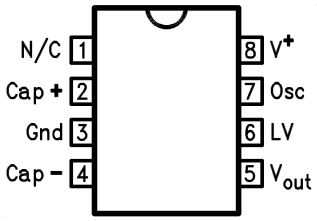
The LMC7660 is a CMOS voltage converter capable of converting a positive voltage in the range of +1.5V to +10V to the corresponding negative voltage of −1.5V to −10V. The LMC7660 is a pin-for-pin replacement for the industry-standard 7660. The converter features: operation over full temperature and voltage range without need for an external diode, low quiescent current, and high power efficiency.

The LMC7660 uses its built-in oscillator to switch 4 power MOS switches and charge two inexpensive electrolytic capacitors.

Block Diagram



Pin Configuration



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Supply Voltage	10.5V
Input Voltage on Pin 6, 7(3)	−0.3V to (V^+ + 0.3V)
	for V^+ < 5.5V
	(V^+ − 5.5V) to (V^+ + 0.3V)
	for V^+ > 5.5V
Current into Pin 6 (3)	20 µA
Output Short Circuit Duration (V^+ ≤ 5.5V)	Continuous
Power Dissipation (4)	
PDIP Package	1.4W
SOIC Package	0.6W
T_J Max (4)	150°C
θ_{JA}(4)	
PDIP Package	90°C/W
SOIC Package	160°C/W
Storage Temp. Range	−65°C ≤ T ≤ 150°C
Lead Temperature	
(Soldering, 5 sec.)	260°C
ESD Tolerance (5)	± 2000V

(1) Absolute Maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions. See Note (1) under Electrical Characteristics for conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Connecting any input terminal to voltages greater than V^+ or less than ground may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to “power-up” of the LMC7660.
(4) For operation at elevated temperature, these devices must be derated based on a thermal resistance of θ_{ja} and T_j max, $T_j = T_A + \theta_{ja} P_D$.
(5) The test circuit consists of the human body model of 100 pF in series with 1500Ω.

ELECTRICAL CHARACTERISTICS(1)

Symbol	Parameter	Conditions	Typ	LMC7660IN/ LMC7660IM Limit (2)	Units Limits
I_S	Supply Current	R_L = ∞	120	200 **400**	µA max
V^+H	Supply Voltage Range High (3)	R_L = 10 kΩ, Pin 6 Open Voltage Efficiency ≥ 90%	3 to 10	3 to 10 **3 to 10**	V
V^+L	Supply Voltage Range Low	R_L = 10 kΩ, Pin 6 to Gnd. Voltage Efficiency ≥ 90%	1.5 to 3.5	1.5 to 3.5 **1.5 to 3.5**	V

(1) Boldface numbers apply at temperature extremes. All other numbers apply at T_A = 25°C, V^+ = 5V, C_{osc} = 0, and apply for the LMC7660 unless otherwise specified. Test circuit is shown in Figure 1 .
(2) Limits at room temperature are specified and 100% production tested. Limits in **boldface** are specified over the operating temperature range (but not 100% tested), and are not used to calculate outgoing quality levels.
(3) The LMC7660 can operate without an external diode over the full temperature and voltage range. The LMC7660 can also be used with the external diode Dx, when replacing previous 7660 designs.

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ELECTRICAL CHARACTERISTICS[1] (continued)

Symbol	Parameter	Conditions	Typ	LMC7660IN/ LMC7660IM Limit [2]	Units Limits
R_{out}	Output Source Resistance	I_L = 20 mA	55	100 **120**	Ω max
		V = 2V, I_L = 3 mA Pin 6 Short to Gnd.	110	200 **300**	Ω max
F_{osc}	Oscillator Frequency		10		kHz
P_{eff}	Power Efficiency	R_L = 5 kΩ	97	95 **90**	% min
$V_{o\ eff}$	Voltage Conversion Efficiency	R_L = ∞	99.9	97 **95**	% min
I_{osc}	Oscillator Sink or Source Current	Pin 7 = Gnd. or V^+	3		µA

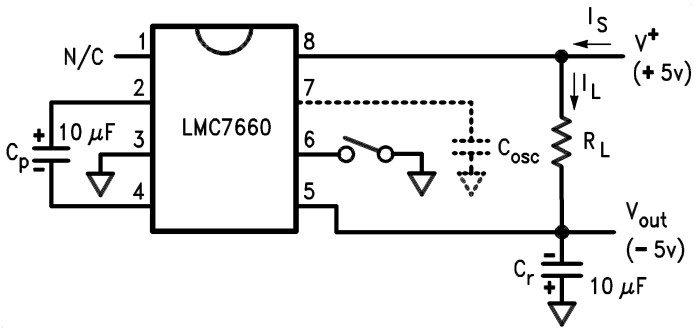


Figure 1. LMC7660 Test Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

OSC Freq. vs OSC Capacitance

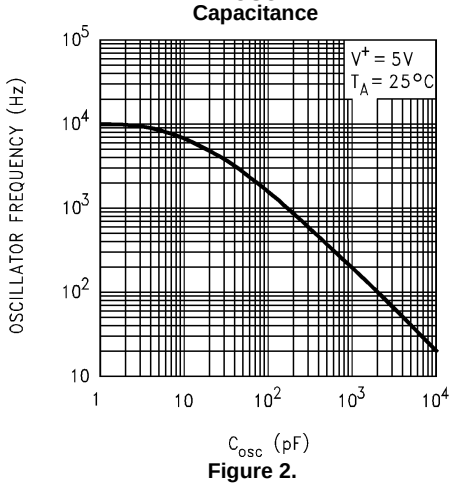


Figure 2.

V_{out} vs I_{out} @ $V^+ = 2V$

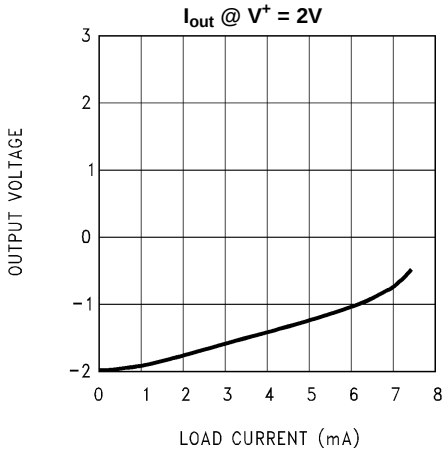


Figure 3.

V_{out} vs I_{out} @ $V^+ = 5V$

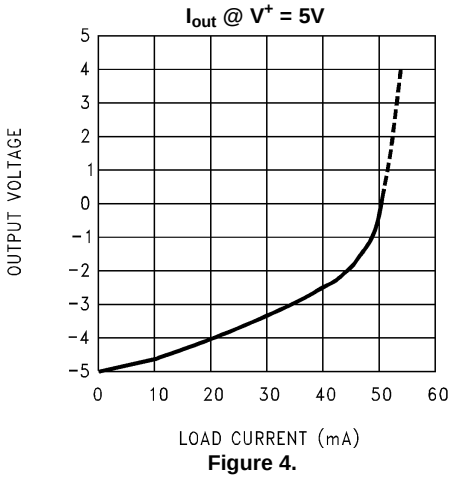


Figure 4.

Supply Current & Power Efficiency vs Load Current ($V^+ = 2V$)

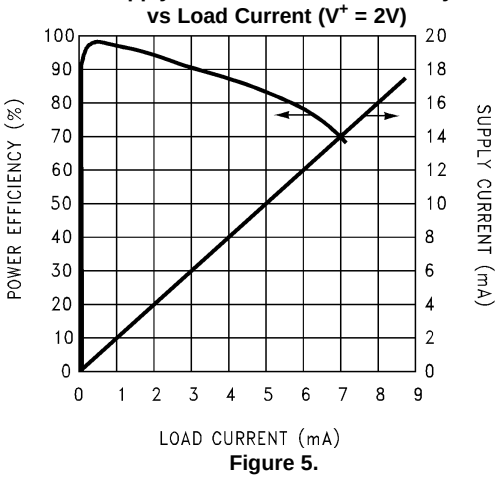


Figure 5.

Supply Current & Power Efficiency vs Load Current ($V^+ = 5V$)

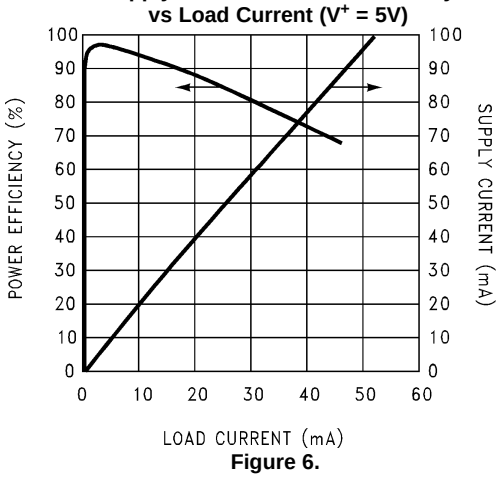


Figure 6.

Output Source Resistiance as a Function of Temperature

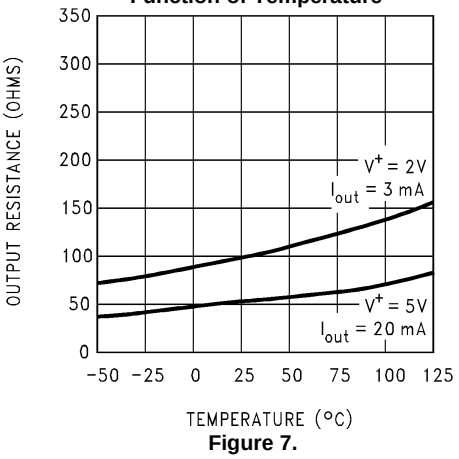


Figure 7.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unloaded Oscillator Frequency as a Function of Temperature

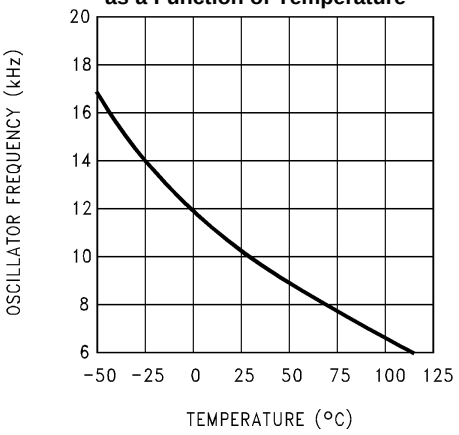


Figure 8.

Output R vs Supply Voltage

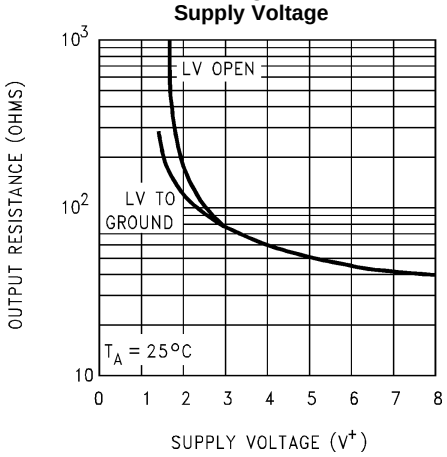


Figure 9.

P_{eff} vs OSC Freq. @ V^+ = 5V

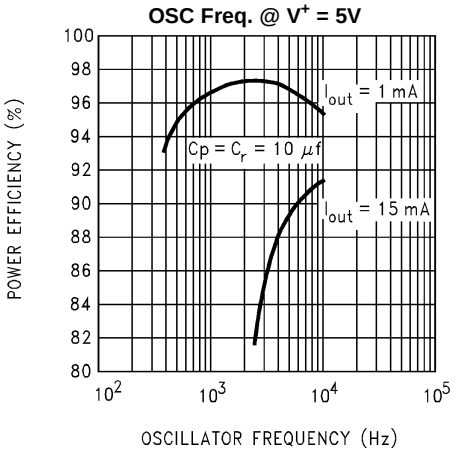


Figure 10.

APPLICATION INFORMATION

CIRCUIT DESCRIPTION

The LMC7660 contains four large CMOS switches which are switched in a sequence to provide supply inversion $V_{out} = -V_{in}$. Energy transfer and storage are provided by two inexpensive electrolytic capacitors. Figure 11 shows how the LMC7660 can be used to generate $-V^+$ from V^+. When switches S1 and S3 are closed, C_p charges to the supply voltage V^+. During this time interval, switches S2 and S4 are open. After C_p charges to V^+, S1 and S3 are opened, S2 and S4 are then closed. By connecting S2 to ground, C_p develops a voltage $-V^+/2$ on C_r. After a number of cycles C_r will be pumped to exactly $-V^+$. This transfer will be exact assuming no load on C_r, and no loss in the switches.

In the circuit of Figure 11, S1 is a P-channel device and S2, S3, and S4 are N-channel devices. Because the output is biased below ground, it is important that the p^- wells of S3 and S4 never become forward biased with respect to either their sources or drains. A substrate logic circuit specifies that these p^- wells are always held at the proper voltage. Under all conditions S4 p^- well must be at the lowest potential in the circuit. To switch off S4, a level translator generates $V_{GS4} = 0V$, and this is accomplished by biasing the level translator from the S4 p^- well.

An internal RC oscillator and ÷ 2 circuit provide timing signals to the level translator. The built-in regulator biases the oscillator and divider to reduce power dissipation on high supply voltage. The regulator becomes active at about $V^+ = 6.5V$. Low voltage operation can be improved if the LV pin is shorted to ground for $V^+ \leq 3.5V$. For $V^+ \geq 3.5V$, the LV pin must be left open to prevent damage to the part.

POWER EFFICIENCY AND RIPPLE

It is theoretically possible to approach 100% efficiency if the following conditions are met:

1. The drive circuitry consumes little power.
2. The power switches are matched and have low R_{on}.
3. The impedance of the reservoir and pump capacitors are negligibly small at the pumping frequency.

The LMC7660 closely approaches 1 and 2 above. By using a large pump capacitor C_p, the charge removed while supplying the reservoir capacitor is small compared to C_p's total charge. Small removed charge means small changes in the pump capacitor voltage, and thus small energy loss and high efficiency. The energy loss by C_p is:

$$E = \tfrac{1}{2} C_p (V1^2 - V2^2) \tag{1}$$

By using a large reservoir capacitor, the output ripple can be reduced to an acceptable level. For example, if the load current is 5 mA and the accepted ripple is 200 mV, then the reservoir capacitor can omit approximately be calculated from:

$$Is = C_r \frac{dv}{dt}$$

$$\sim C_r \times \frac{V_{ripple\ p\text{-}p}}{4/F_{osc}} \qquad C_r = \frac{0.5\ mA}{0.5V/ms} = 10\ \mu F \tag{2}$$

PRECAUTIONS

1. Do not exceed the maximum supply voltage or junction temperature.
2. Do not short pin 6 (LV terminal) to ground for supply voltages greater than 3.5V.
3. Do not short circuit the output to V^+.
4. External electrolytic capacitors C_r and C_p should have their polarities connected as shown in Figure 1.

REPLACING PREVIOUS 7660 DESIGNS

To prevent destructive latchup, previous 7660 designs require a diode in series with the output when operated at elevated temperature or supply voltage. Although this prevented the latchup problem of these designs, it lowered the available output voltage and increased the output series resistance.

The TI LMC7660 has been designed to solve the inherent latch problem. The LCM7660 can operate over the entire supply voltage and temperature range without the need for an output diode. When replacing existing designs, the LMC7660 can be operated with diode Dx.

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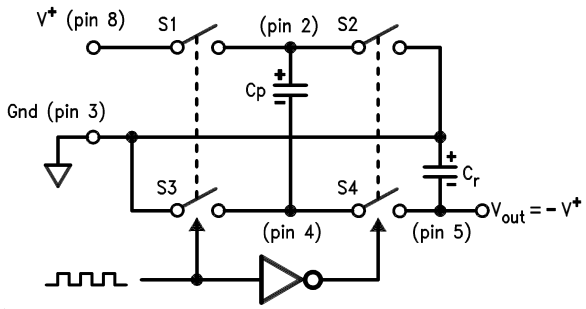


Figure 11. Idealized Voltage Converter

TYPICAL APPLICATIONS

CHANGING OSCILLATOR FREQUENCY

It is possible to dramatically reduce the quiescent operating current of the LMC7660 by lowering the oscillator frequency. The oscillator frequency can be lowered from a nominal 10 kHz to several hundred hertz, by adding a slow-down capacitor C_{osc} (Figure 12). As shown in the Typical Performance Curves the supply current can be lowered to the 10 µA range. This low current drain can be extremely useful when used in µPower and battery back-up equipment. It must be understood that the lower operating frequency and supply current cause an increased impedance of C_r and C_p. The increased impedance, due to a lower switching rate, can be offset by raising C_r and C_p until ripple and load current requirements are met.

SYNCHRONIZING TO AN EXTERNAL CLOCK

Figure 13 shows an LMC7660 synchronized to an external clock. The CMOS gate overrides the internal oscillator when it is necessary to switch faster or reduce power supply interference. The external clock still passes through the ÷2 circuit in the 7660, so the pumping frequency will be ½ the external clock frequency.

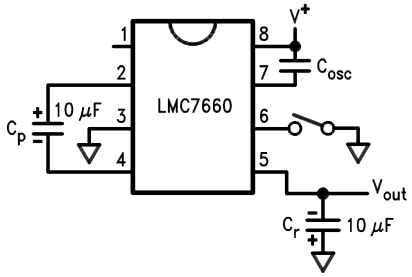


Figure 12. Reduce Supply Current by Lowering Oscillator Frequency

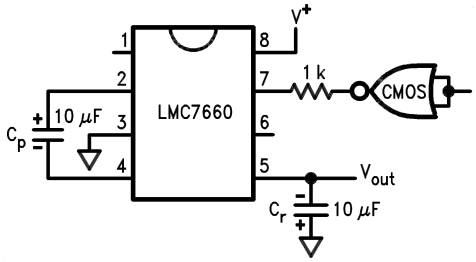


Figure 13. Synchronizing to an External Clock

LOWERING OUTPUT IMPEDANCE

Paralleling two or more LMC7660's lowers output impedance. Each device must have it's own pumping capacitor C_p, but the reservoir capacitor C_r is shared as depicted in Figure 14. The composite output resistance is:

$$R_{out} = \frac{R_{out} \text{ of one LMC7660}}{\text{Number of devices}} \quad (3)$$

INCREASING OUTPUT VOLTAGE

Stacking the LMC7660s is an easy way to produce a greater negative voltage. It should be noted that the input current required for each stage is twice the load current on that stage as shown in Figure 15. The effective output resistance is approximately the sum of the individual R_{out} values, and so only a few levels of multiplication can be used.

It is possible to generate −15V from +5V by connecting the second 7660's pin 8 to +5V instead of ground as shown in Figure 16. Note that the second 7660 sees a full 20V and the input supply should not be increased beyond +5V.

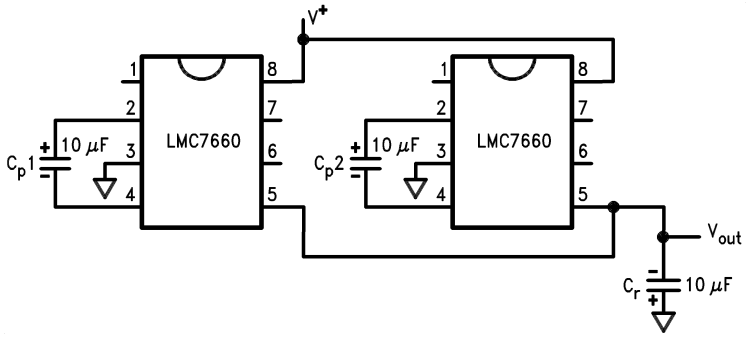


Figure 14. Lowering Output Resistance by Paralleling Devices

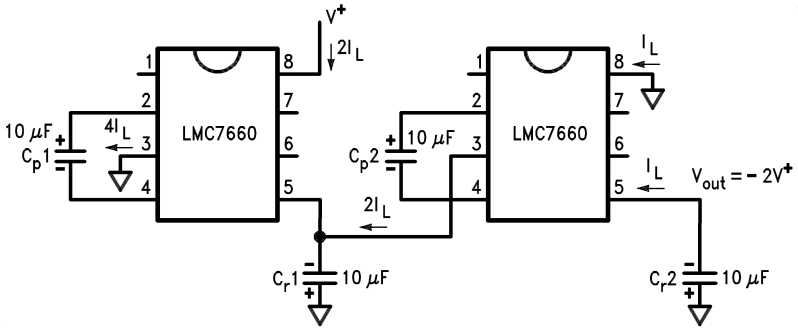


Figure 15. Higher Voltage by Cascade

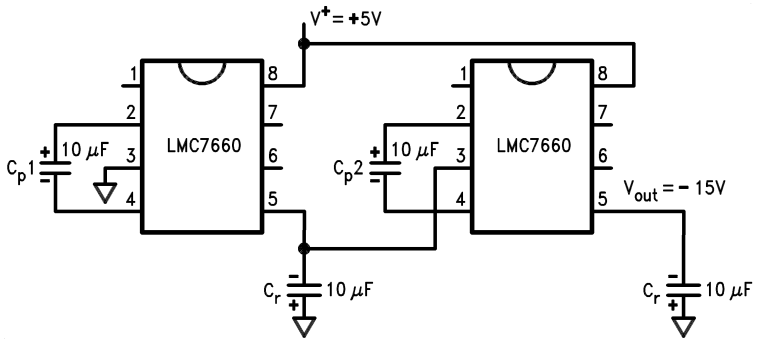


Figure 16. Getting −15V from +5V

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SPLIT V^+ IN HALF

Figure 17 is one of the more interesting applications for the LMC7660. The circuit can be used as a precision voltage divider (for very light loads), alternately it is used to generate a ½ supply point in battery applications. In the ½ cycle when S1 and S3 are closed, the supply voltage divides across the capacitors in a conventional way proportional to their value. In the ½ cycle when S2 and S4 are closed, the capacitors switch from a series connection to a parallel connection. This forces the capacitors to have the same voltage; the charge redistributes to maintain precisely $V^+/2$, across C_p and C_r. In this application all devices are only $V^+/2$, and the supply voltage can be raised to 20V giving exactly 10V at V_{out}.

GETTING UP … AND DOWN

The LMC7660 can also be used as a positive voltage multiplier. This application, shown in Figure 18, requires 2 additional diodes. During the first ½ cycle S2 charges C_p1 through D1; D2 is reverse biased. In the next ½ cycle S2 is open and S1 is closed. Since C_p1 is charged to $V^+ - V_{D1}$ and is referenced to V^+ through S1, the junction of D1 and D2 is at $V^+ + (V^+ - V_{D1})$. D1 is reverse biased in this interval. This application uses only two of the four switches in the 7660. The other two switches can be put to use in performing a negative conversion at the same time as shown in Figure 19. In the ½ cycle that D1 is charging C_p1, C_p2 is connected from ground to $-V_{out}$ via S2 and S4, and C_r2 is storing C_p2's charge. In the interval that S1 and S3 are closed, C_p1 pumps the junction of D1 and D2 above V^+, while C_p2 is refreshed from V^+.

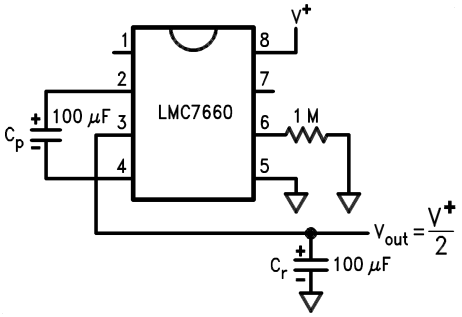


Figure 17. Split V^+ in Half

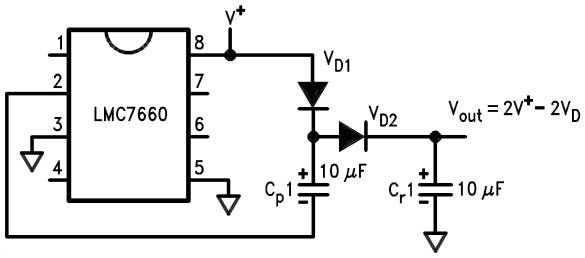


Figure 18. Positive Voltage Multiplier

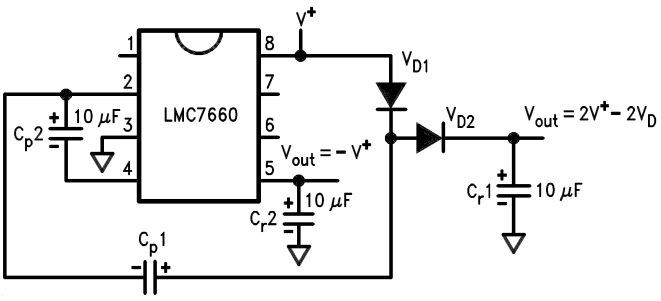


Figure 19. Combined Negative Converter and Positive Multiplier

THERMOMETER SPANS 180°C

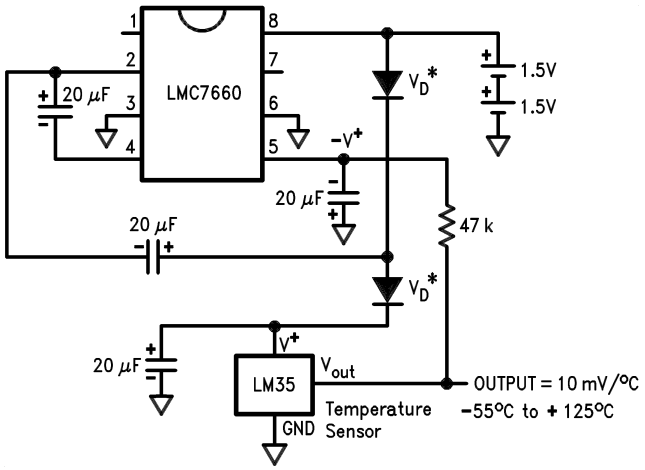
Using the combined negative and positive multiplier of Figure 20 with an LM35 it is possible to make a µPower thermometer that spans a 180°C temperature range. The LM35 temperature sensor has an output sensitivity of 10 mV/°C, while drawing only 50 µA of quiescent current. In order for the LM35 to measure negative temperatures, a pull down to a negative voltage is required. Figure 20 shows a thermometer circuit for measuring temperatures from −55°C to +125°C and requiring only two 1.5V cells. End of battery life can be extended by replacing the up converter diodes with Schottky's.

REGULATING $-V_{OUT}$

It is possible to regulate the output of the LMC7660 and still maintain µPower performance. This is done by enclosing the LMC7660 in a loop with a LP2951. The circuit of Figure 21 will regulate V_{out} to −5V for I_L = 10 mA, and V_{in} = 6V. For V_{in} > 7V, the output stays in regulation up to I_L = 25 mA. The error flag on pin 5 of the LP2951 sets low when the regulated output at pin 4 drops by about 5%. The LP2951 can be shutdown by taking pin 3 high; the LMC7660 can be shutdown by shorting pin 7 and pin 8.

The LP2951 can be reconfigured to an adjustable type regulator, which means the LMC7660 can give a regulated output from −2.0V to −10V dependent on the resistor ratios R1 and R2, as shown in Figure 22, V_{ref} = 1.235V:

$$V_{out} = V_{ref}\left(1 + \frac{R1}{R2}\right) \quad (4)$$



*For lower voltage operation, use Schottky rectifiers

Figure 20. µPower Thermometer Spans 180°C, and Pulls Only 150 µA

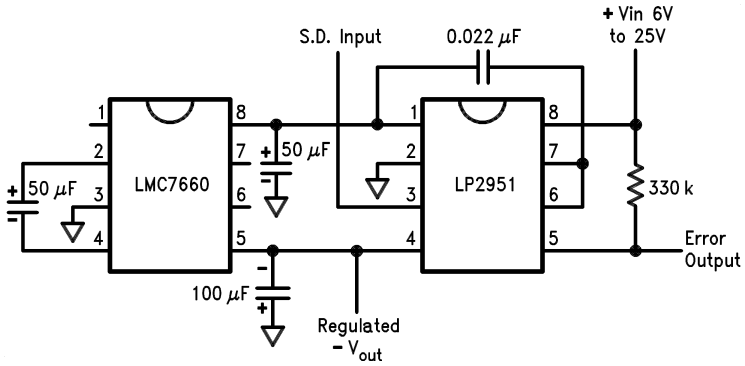
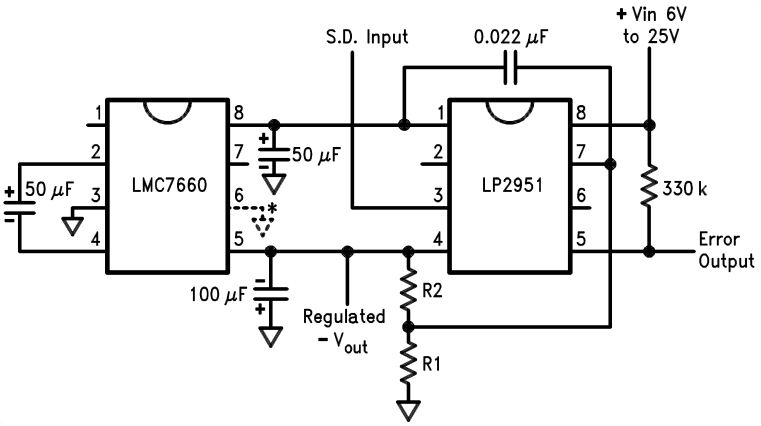


Figure 21. Regulated −5V with 200 µA Standby Current

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$$V_{out} = V_{ref}\left(1 + \frac{R1}{R2}\right)$$

V_{ref} = 1.235V
*Low voltage operation

Figure 22. LMC7660 and LP2951 Make a Negative Adjustable Regulator

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	11

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC7660IM	NRND	SOIC	D	8	95	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM		LMC76 60IM	
LMC7660IM/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC76 60IM	Samples
LMC7660IMX	NRND	SOIC	D	8	2500	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM		LMC76 60IM	
LMC7660IMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC76 60IM	Samples
LMC7660IN/NOPB	ACTIVE	PDIP	P	8	40	RoHS & Green	Call TI | SN	Level-1-NA-UNLIM	-40 to 85	LMC 7660IN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

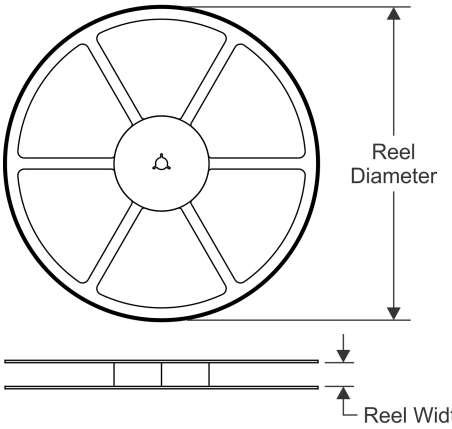
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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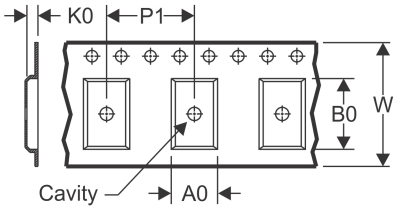
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

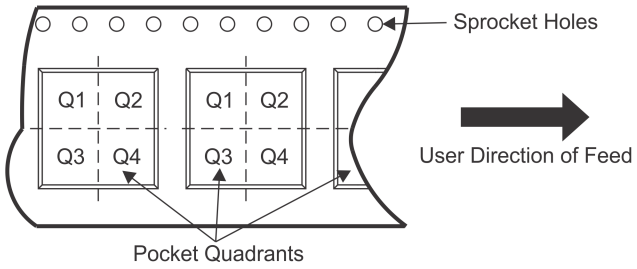


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

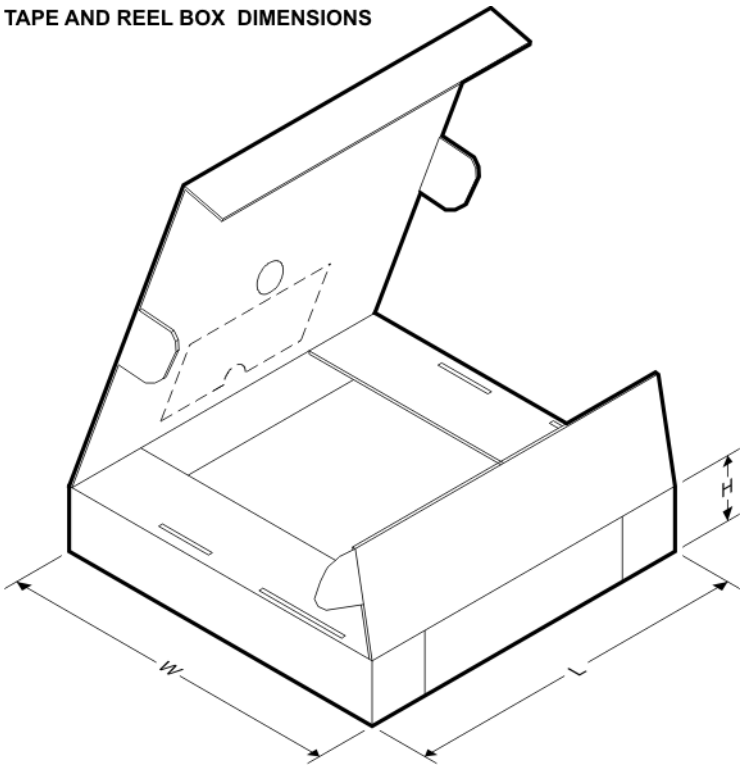
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC7660IMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC7660IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

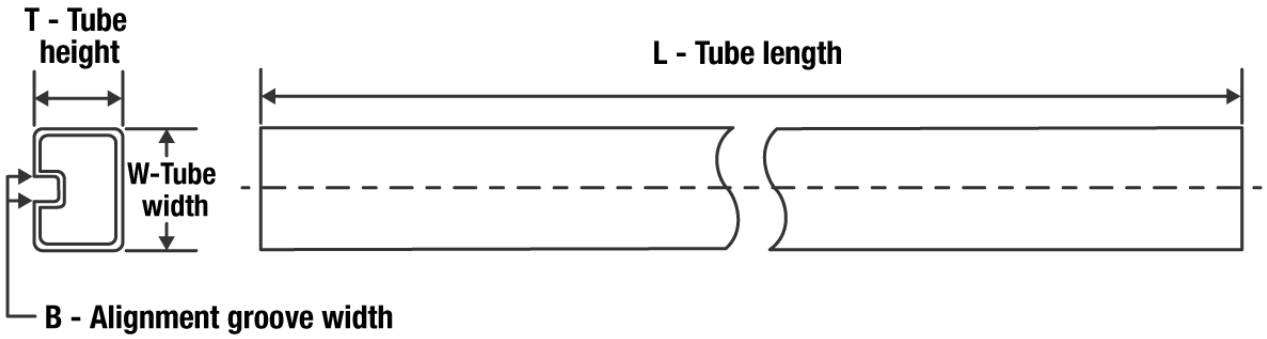
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

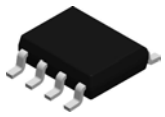
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC7660IMX	SOIC	D	8	2500	367.0	367.0	35.0
LMC7660IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMC7660IM	D	SOIC	8	95	495	8	4064	3.05
LMC7660IM	D	SOIC	8	95	495	8	4064	3.05
LMC7660IM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMC7660IN/NOPB	P	PDIP	8	40	502	14	11938	4.32

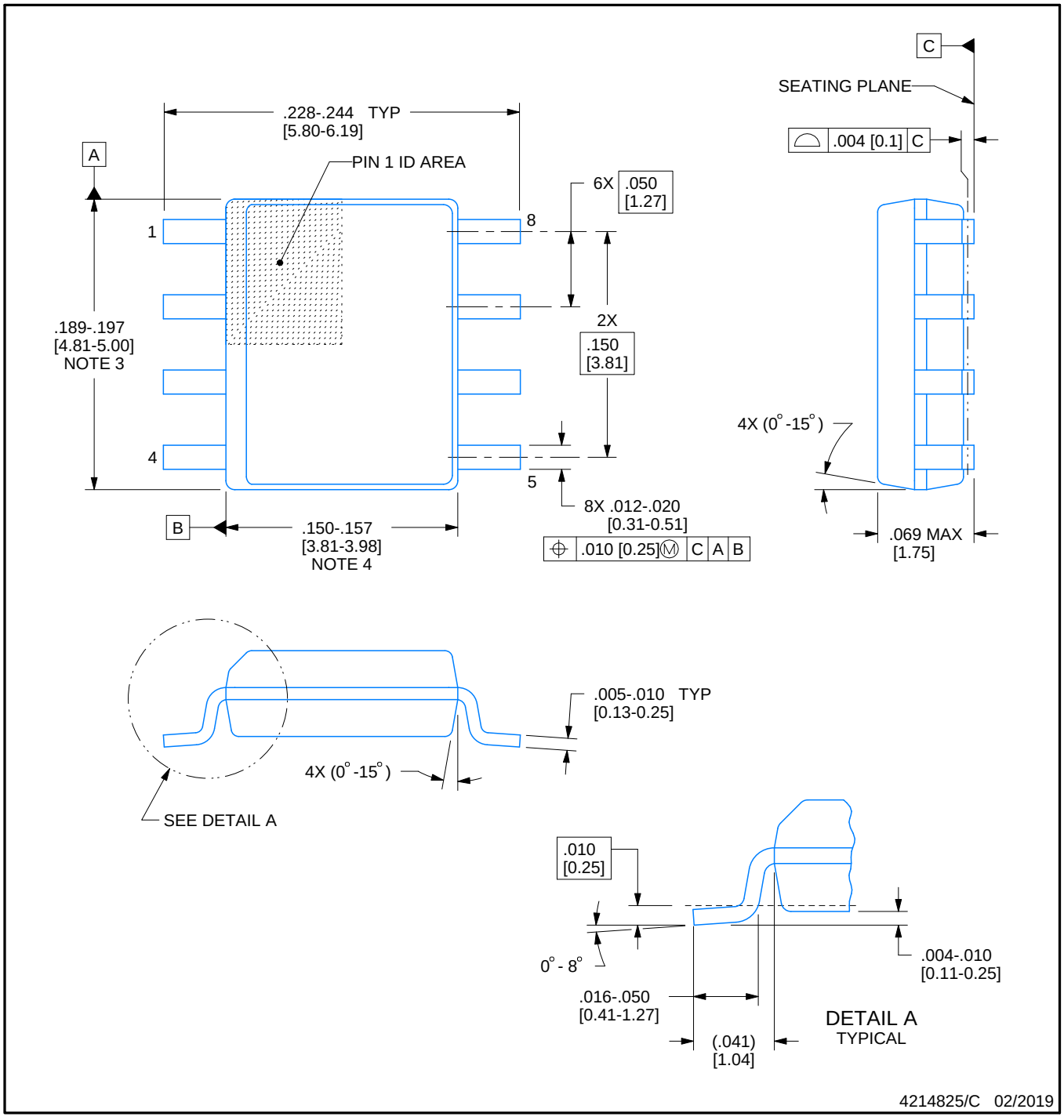


PACKAGE OUTLINE

D0008A

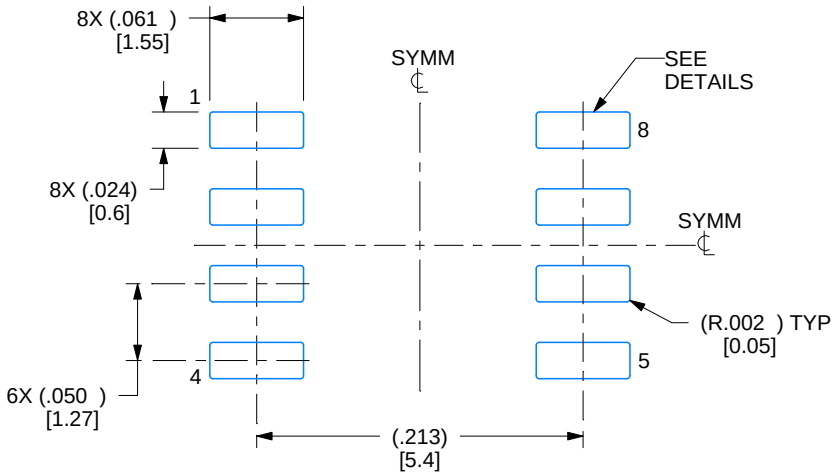
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

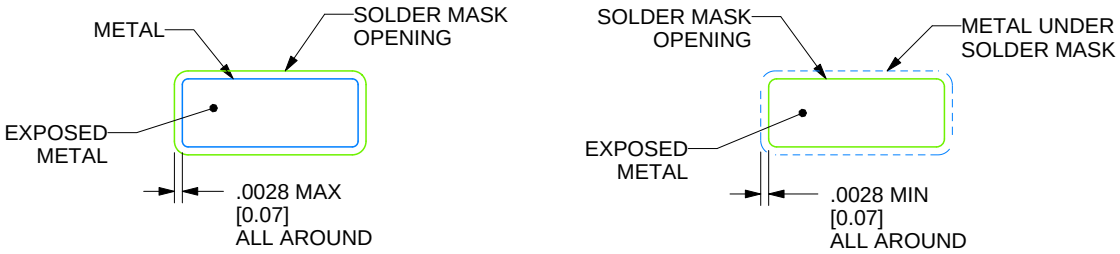


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

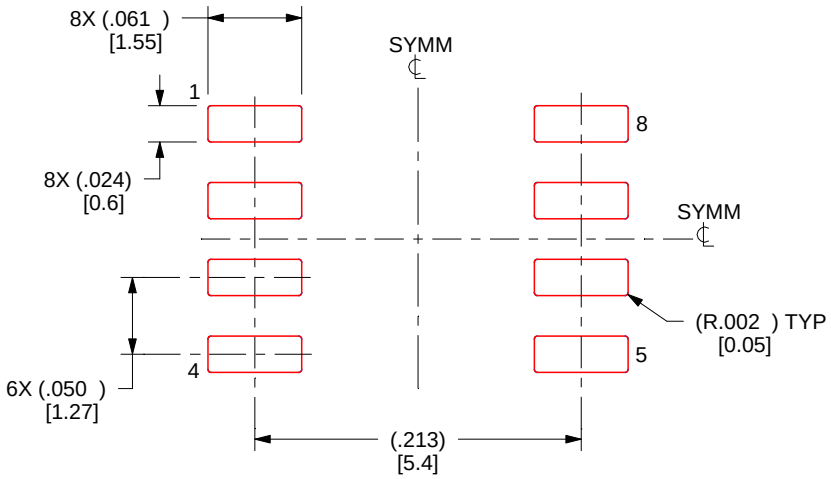
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



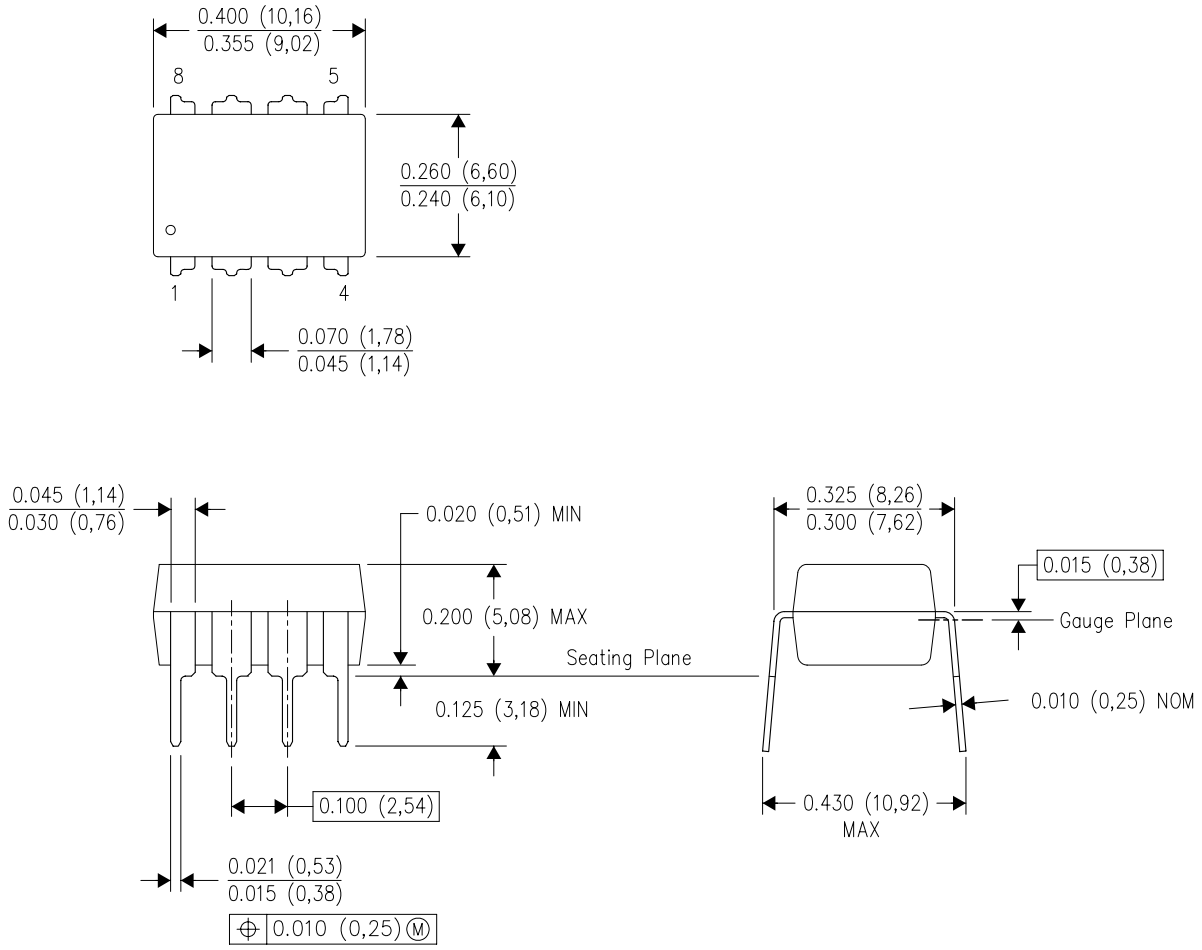
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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