

# LMR14006 SIMPLE SWITCHER<sup>®</sup> 40 V 600 mA Buck Regulator With High Efficiency Sleep Mode

## 1 Features

- Ultra Low 28  $\mu$ A Standby Current in Sleep Mode
- Input Voltage Range 4 V to 40 V
- 1  $\mu$ A Shutdown Current
- High Duty Cycle Operation Supported
- Output Current up to 600 mA
- 1.1 MHz and 2.1 MHz Switching Frequency
- Internal Compensation
- High Voltage Enable Input
- Internal Soft Start
- Over Current Protection
- Over Temperature Protection
- Small Overall Solution Size (TSOT-6L Package)

## 2 Applications

- Industrial Distributed Power Systems
- Automotive
- Battery Powered Equipment
- Portable Handheld Instruments
- Portable Media Players

## 3 Description

The LMR14006 is a PWM DC/DC buck (step-down) regulator. With a wide input range of 4 V-40 V, it is suitable for a wide range of application from industrial to automotive for power conditioning from an unregulated source. The regulator's standby current is 28  $\mu$ A in sleep mode, which is suitable for battery operating systems. An ultra low 1  $\mu$ A current can further prolong battery life in shutdown mode. Operating frequency is fixed at 1.1 MHz (X version) and 2.1 MHz (Y version) allowing the use of small external components while still being able to have low output ripple voltage. Soft-start and compensation circuits are implemented internally, and these allow the device to be used with minimized external components. The LMR14006 is optimized for up to 600 mA load current which has a 0.765 V typical feedback voltage. The device has built-in protection features such as pulse by pulse current limit, thermal sensing and shutdown due to excessive power dissipation. The LMR14006 is available in a low profile TSOT-6L package.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMR14006	TSOT-6L	2.9mm x 1.6 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

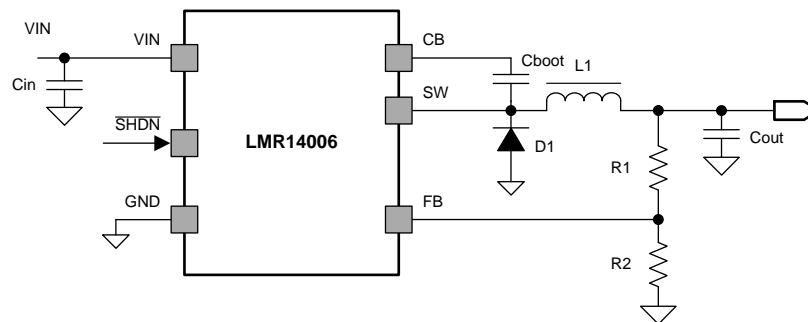


Figure 1. Typical Application Schematic



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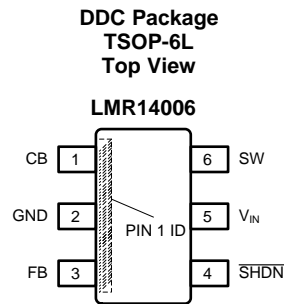
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Original (November 2013) to Revision A</b>	<b>Page</b>
• Deleted the other part number LMR14003 from the rest of the document .....	1
• Added <i>Device Information</i> and <i>Handling Rating</i> tables, <i>Feature Description</i> , <i>Application and Implementation</i> , , <i>Layout</i> , <i>Device and Documentation Support</i> , and <i>Mechanical, Packaging, and Orderable Information</i> sections; moved some curves to <i>Application Curves</i> section.....	1
• Changed from 2kV to 1kV .....	4

<b>Changes from Revision A (September 2014) to Revision B</b>	<b>Page</b>
• Changed from -0.3 to -1 .....	4
• Changed from -0.3 to -1 .....	4

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
CB	1	I	SW FET Gate Bias voltage. Connect $C_{boot}$ cap between CB and SW
GND	2	G	Ground Connection
FB	3	I	Feedback Pin. Set feedback voltage divider ratio with $V_{OUT} = V_{FB} (1+(R1/R2))$
/SHDN	4	I	Enable and disable input pin(high voltage tolerant). Internal pull-up current source. Pull below 1.2V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors.
VIN	5	I	Power input voltage pin. Input for internal supply and drain input for internal high-side MOSFET
SW	6	O	Switch node. Connect to inductor, diode, and $C_{boot}$ cap

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

	PARAMETER	MIN	MAX	UNIT
Input Voltages	V <sub>IN</sub> to GND	-0.3	45	V
	SHDN to GND	-0.3	45	
	FB to GND	-0.3	7	
	CB to SW	-0.3	7	
Output Voltages	SW to GND	-1	45	V
	SW to GND less than 30ns transients	-2	45	
T <sub>J</sub> Operation Junction Temperature		-40	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 Handling Ratings

		MIN	MAX	UNIT
T <sub>stg</sub>	Storage temperature range	-55	165	°C
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins except CB pin <sup>(1)</sup>	1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process, CB pin passes 500V test.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions <sup>(1)</sup>

Over operating free-air temperature range (unless otherwise noted)

	PARAMETER	MIN	MAX	UNIT
Buck Regulator	V <sub>IN</sub>	4	40	V
	CB	4	46	V
	CB to SW	-0.3	6	V
	SW	-1	40	
	FB	0	5.5	V
Control	SHDN	0	40	V
Temperature	Operating junction temperature range, T <sub>J</sub>	-40	125	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TSOT (6 PINS)	UNIT
Rθ <sub>JA</sub>	Junction-to-ambient thermal resistance	102	°C/W
Rθ <sub>JCtop</sub>	Junction-to-case (top) thermal resistance	36.9	
Rθ <sub>JB</sub>	Junction-to board characterization parameter	28.4	

- (1) All numbers apply for packages soldered directly onto a 3" x 3" PC board with 2 oz. copper on 4 layers in still air in accordance to JEDEC standards. Thermal resistance varies greatly with layout, copper thickness, number of layers in PCB, power distribution, number of thermal vias, board size, ambient temperature, and air flow.

## 6.5 Electrical Characteristics

 $V_{IN} = /SHDN = 12V$ ,  $T_A = 25^\circ C$ , unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
<b>VIN (Input Power Supply)</b>						
$V_{IN}$	Operating input voltage		4		40	V
$I_{SHDN}$	Shutdown supply current	$V_{EN} = 0V$		1	3	$\mu A$
$I_Q$	Operating quiescent current (non- switching)	no load, $V_{IN} = 12V$		28		$\mu A$
UVLO	Undervoltage lockout thresholds	Rising threshold			4	V
		Falling threshold	3			
<b>SHDN</b>						
$V_{SHDN\_Thre}$	Rising $\overline{SHDN}$ Threshold Voltage		1.05	1.25	1.38	V
$I_{SHDN\_PIN}$	Input current	$\overline{SHDN} = 2.3V$		-4.2		$\mu A$
		$\overline{SHDN} = 0.9V$		-1		
$I_{SHDN\_HYS}$	Hysteresis current			-3		$\mu A$
<b>HIGH-SIDE MOSFET</b>						
$R_{DS\_ON}$	On-resistance	$V_{IN} = 12V$ , CB to SW = 5.8V		600		m $\Omega$
<b>VOLTAGE REFERENCE (FB PIN)</b>						
$V_{FB}$	Feedback voltage		0.747	0.765	0.782	V
<b>CURRENT LIMIT</b>						
$I_{LIMIT}$	Current limit	$V_{IN} = 12V$ , $T_J = 25^\circ C$		1200		mA
<b>THERMAL PERFORMANCE</b>						
$T_{SHDN}$	Thermal shutdown threshold			170		$^\circ C$
$T_{HYS}$	Hysteresis			10		$^\circ C$

## 6.6 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SW (SW PIN)</b>						
$f_{SW}$	Switching frequency	LMR14006X	935	1100	1285	kHz
		LMR14006Y	1785	2100	2415	
$T_{ON\_MIN}$	Minimum turn-on time	$f_{SW} = 2.1$ MHz		95		ns
$D_{MAX}$	Maximum duty cycle	LMR14006X		96%		
		LMR14006Y		97%		

### 6.7 Typical Characteristics

$V_{IN} = 12V$ ,  $T_A = 25^\circ C$ , unless otherwise specified.

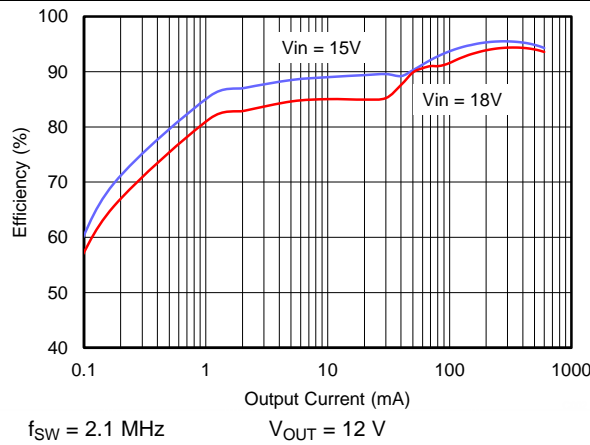


Figure 2. Efficiency vs. Load Current

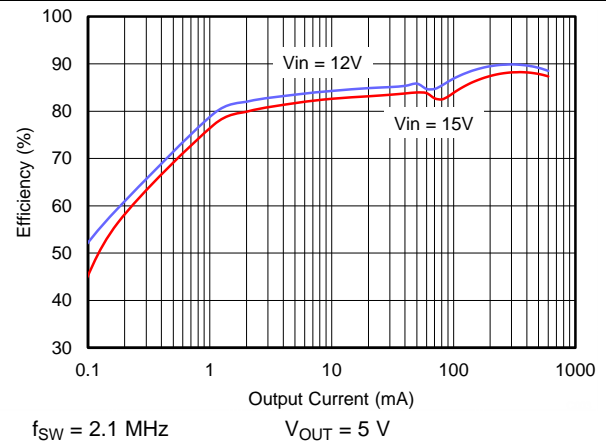


Figure 3. Efficiency vs. Load Current

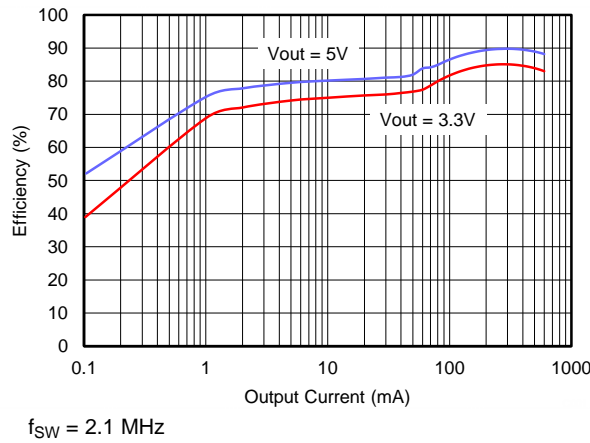


Figure 4. Efficiency vs. Load Current

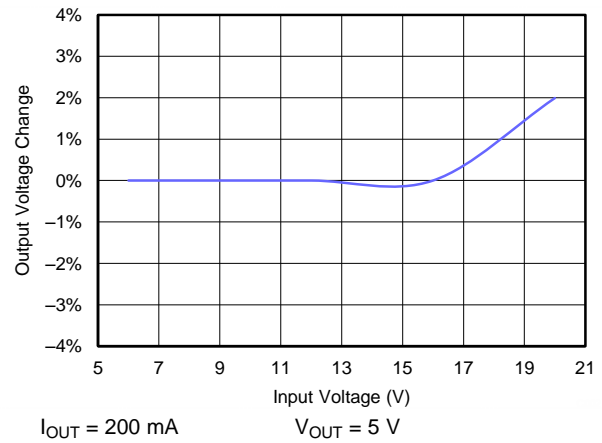


Figure 5. Line Regulation

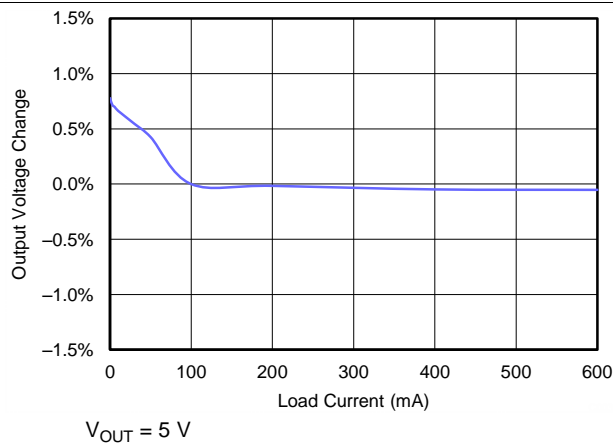


Figure 6. Load Regulation

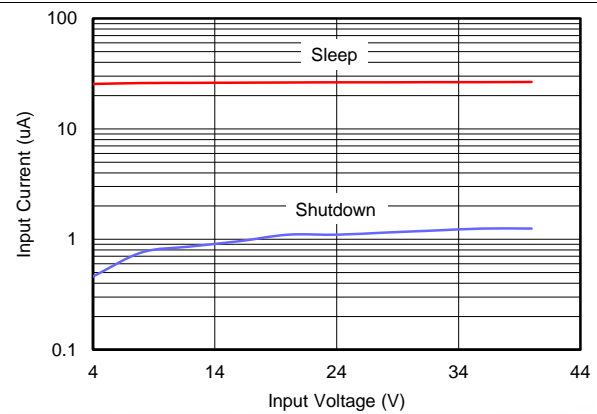
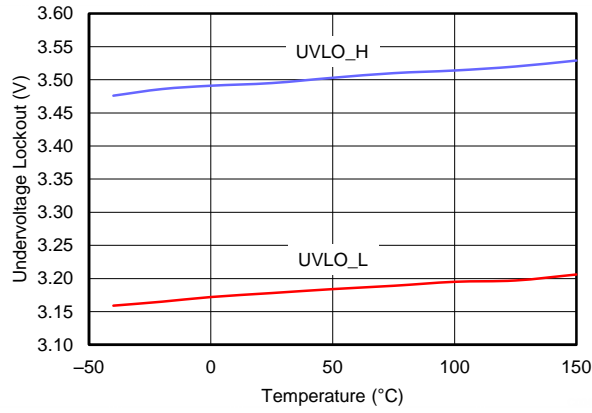


Figure 7. Supply Current vs Input Voltage (No Load)

**Typical Characteristics (continued)**

$V_{IN} = 12V$ ,  $T_A = 25^{\circ}C$ , unless otherwise specified.



**Figure 8. UVLO vs Temperature**

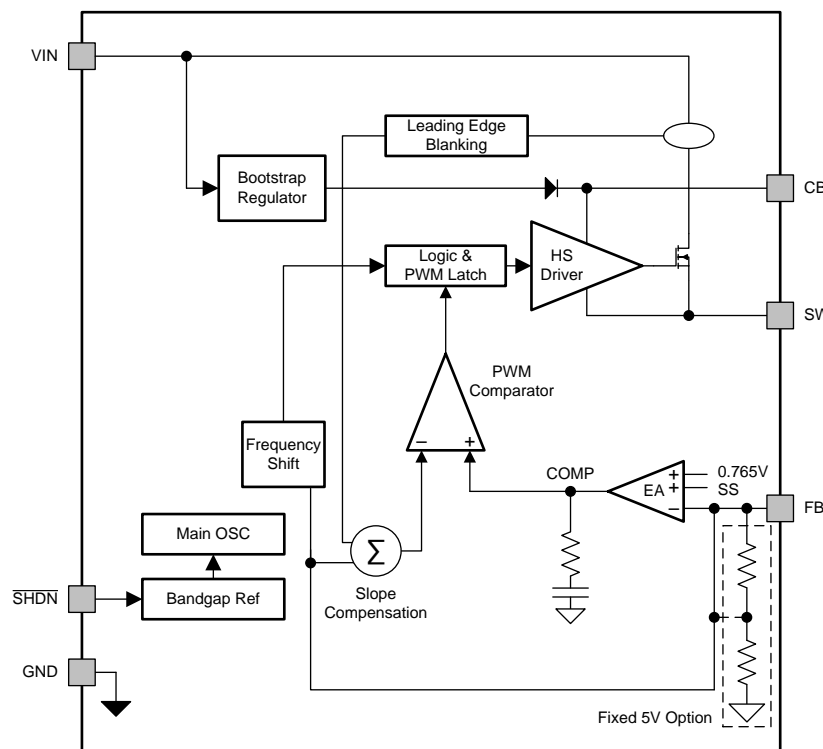
## 7 Detailed Description

### 7.1 Overview

The LMR14006 device is a 40 V, 600 mA, step-down (buck) regulator. The buck regulator has a very low quiescent current during light load to prolong the battery life.

For LMR14006, to improve performance during line and load transients it implements a constant frequency, current mode control which requires less output capacitance and simplifies frequency compensation design. Two switching frequency options, 1.1 MHz and 2.1 MHz, are available, thus smaller inductor and capacitor can be used. The LMR14006 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high side MOSFET is supplied by a capacitor on the CB to SW pin. The boot capacitor voltage is monitored by an UVLO circuit and will turn the high side MOSFET off when the boot voltage falls below a preset threshold. The LMR14006 can operate at high duty cycles because of the boot UVLO and refresh wimp FET. The output voltage can be stepped down to as low as the 0.8 V reference. Internal soft start is featured to minimize inrush currents.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Continuous Conduction Mode

The LMR14006 steps the input voltage down to a lower output voltage. In continuous conduction mode (when the inductor current never reaches zero at steady state), the buck regulator operates in two cycles. The power switch is connected between VIN and SW. In the first cycle of operation the transistor is closed and the diode is reverse biased. Energy is collected in the inductor and the load current is supplied by Cout and the rising current through the inductor. During the second cycle the transistor is open and the diode is forward biased due to the fact that the inductor current cannot instantaneously change direction. The energy stored in the inductor is transferred to the load and output capacitor. The ratio of these two cycles determines the output voltage. The output voltage is defined approximately as:  $D = V_{OUT}/V_{IN}$  and  $D' = (1-D)$  where D is the duty cycle of the switch, D and D' will be required for design calculations.



## Feature Description (continued)

### 7.3.2 Fixed Frequency Pwm Control

The LMR14006 has two fixed frequency options, and it implements peak current mode control. The output voltage is compared through external resistors on the VFB pin to an internal voltage reference by an error amplifier which drives the internal COMP node. An internal oscillator initiates the turn on of the high side power switch. The error amplifier output is compared to the high side power switch current. When the power switch current reaches the level set by the internal COMP voltage, the power switch is turned off. The internal COMP node voltage will increase and decrease as the output current increases and decreases. The device implements a current limit by clamping the COMP node voltage to a maximum level.

### 7.3.3 Sleep Mode

The LMR14006 operates in sleep mode at light load currents to improve efficiency by reducing switching and gate drive losses. The LMR14006 is designed so that if the output voltage is within regulation and the peak switch current at the end of any switching cycle is below the sleep current threshold,  $I_{INDUCTOR} \leq 80 \text{ mA}$ , the device enters sleep mode. For sleep mode operation, the LMR14006 senses peak current, not average or load current, so the load current where the device enters sleep mode is dependent on the output inductor value. When the load current is low and the output voltage is within regulation, the device enters a sleep mode and draws only 28  $\mu\text{A}$  input quiescent current.

### 7.3.4 Bootstrap Voltage (CB)

The LMR14006 has an integrated boot regulator, and requires a small ceramic capacitor between the CB and SW pins to provide the gate drive voltage for the high side MOSFET. The CB capacitor is refreshed when the high side MOSFET is off and the low side diode conducts. To improve drop out, the LMR14006 is designed to operate at 100% duty cycle as long as the CB to SW pin voltage is greater than 3 V. When the voltage from CB to SW drops below 3V, the high side MOSFET is turned off using an UVLO circuit which allows the low side diode to conduct and refresh the charge on the CB capacitor. Since the supply current sourced from the CB capacitor is low, the high side MOSFET can remain on for more switching cycles than are required to refresh the capacitor, thus the effective duty cycle of the switching regulator is high. Attention must be taken in maximum duty cycle applications with light load. To ensure SW can be pulled to ground to refresh the CB capacitor, an internal circuit will charge the CB capacitor when the load is light or the device is working in dropout condition.

### 7.3.5 Output Voltage Setting

The output voltage is set using the feedback pin and a resistor divider connected to the output as shown in [Functional Block Diagram](#). The feedback pin voltage 0.765V, so the ratio of the feedback resistors sets the output voltage according to the following equation:  $V_{OUT} = 0.765V (1+(R1/R2))$  Typically R2 will be given as 100  $\Omega$  - 10 k $\Omega$  for a starting value. To solve for R1 given R2 and Vout uses  $R1 = R2 ((V_{OUT}/0.765V)-1)$ .

### 7.3.6 Enable (/SHDN) and VIN Under Voltage Lockout

LMR14006 /SHDN pin is a high voltage tolerant input with an internal pull up circuit. The device can be enabled even if the /SHDN pin is floating. The regulator can also be turned on using 1.23V or higher logic signals. If the use of a higher voltage is desired due to system or other constraints, a 100 k $\Omega$  or larger resistor is recommended between the applied voltage and the /SHDN pin to protect the device. When /SHDN is pulled down to 0V, the chip is turned off and enters the lowest shutdown current mode. In shutdown mode the supply current will be decreased to approximately 1  $\mu\text{A}$ . If the shutdown function is not to be used the /SHDN pin may be tied to VIN. The maximum voltage to the SHDN pin should not exceed 40V. LMR14006 has an internal UVLO circuit to shutdown the output if the input voltage falls below an internally fixed UVLO threshold level. This ensures that the regulator is not latched into an unknown state during low input voltage conditions. The regulator will power up when the input voltage exceeds the voltage level. If there is a requirement for a higher UVLO voltage, the /SHDN can be used to adjust the input voltage UVLO by using external resistors.

## Feature Description (continued)

### 7.3.7 Current Limit

The LMR14006 implements current mode control which uses the internal COMP voltage to turn off the high side MOSFET on a cycle-by-cycle basis. Each cycle the switch current and internal COMP voltage are compared, when the peak switch current intersects the COMP voltage, the high side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier will respond by driving the COMP node high, increasing the switch current. The error amplifier output is clamped internally, which functions as a switch current limit.

### 7.3.8 Overvoltage Transient Protection

The LMR14006 incorporates an overvoltage transient protection (OVTP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients on power supply designs with low value output capacitance. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the FB pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier will respond by clamping the error amplifier output to a high voltage. Thus, requesting the maximum output current. Once the condition is removed, the regulator output rises and the error amplifier output transitions to the steady state duty cycle. In some applications, the power supply output voltage can respond faster than the error amplifier output can respond, this actuality leads to the possibility of an output overshoot. The OVTP feature minimizes the output overshoot, when using a low value output capacitor, by implementing a circuit to compare the FB pin voltage to OVTP threshold which is 108% of the internal voltage reference. If the FB pin voltage is greater than the OVTP threshold, the high side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVTP threshold, the high side MOSFET is allowed to turn on at the next clock cycle.

### 7.3.9 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 170°C(typ). The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the junction temperature decreases below 160°C(typ), the device reinitiates the power up sequence.

## 8 Applications and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Typical Applications

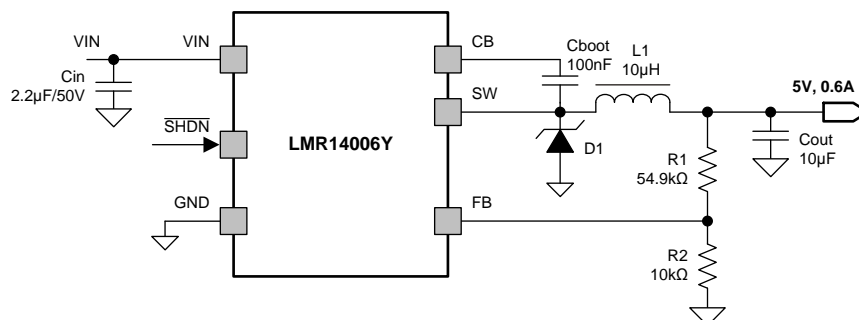


Figure 9. LMR14006 Design Example with 2.1 MHz Switching Frequency

Below are the recommended typical output voltage inductor/capacitor combinations for optimized total solution size.

P/N	Vout(V)	R1(kΩ)	R2(kΩ)	L(µH)	Cout(µF)
LMR14006 Y	5	54.9(1%)	10(1%)	3.3	22
LMR14006 Y	12	147(1%)	10(1%)	3.3	10

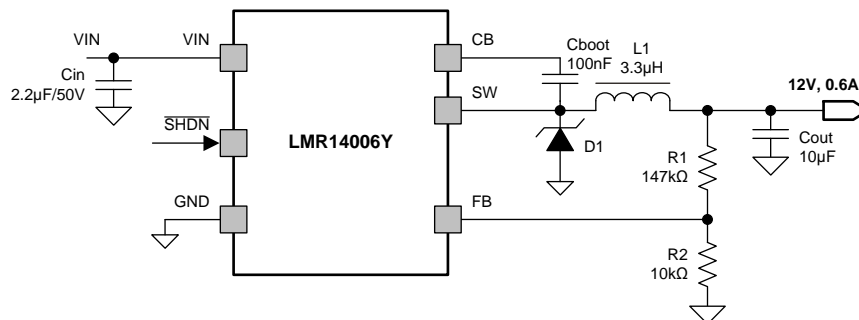


Figure 10. Application Circuit, 12 V Output

#### 8.1.1 Design Requirements

This example details the design of a high frequency switching regulator using ceramic output capacitors. A few parameters must be known in order to start the design process. These parameters are typically determined at the system level:

Table 1. Design Parameters

Input Voltage, $V_{IN}$	9V to 16V, Typical 12V
Output Voltage, $V_{OUT}$	5.0V $\pm$ 3%
Maximum Output Current $I_{O\_max}$	0.6A
Minimum Output Current $I_{O\_min}$	0.03A
Transient Response 0.03A to 0.6A	5%

**Table 1. Design Parameters (continued)**

Output Voltage Ripple		1%
Switching Frequency Fsw		2.1MHz
Target during Load Transient	Over Voltage Peak Value	106% of Output Voltage
	Under Voltage Value	91% of Output Voltage

## 8.1.2 Detailed Design Procedure

### 8.1.2.1 Selecting The Switching Frequency

The first step is to decide on a switching frequency for the regulator. Typically, the user will want to choose the highest switching frequency possible since this will produce the smallest solution size. The high switching frequency allows for lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. The switching frequency that can be selected is limited by the minimum on-time of the internal power switch, the input voltage and the output voltage and the frequency shift limitation. For this example, the output voltage is 5V and the maximum input voltage is 16 V, a switching frequency of 2100 kHz is used.

### 8.1.2.2 Output Inductor Selection

The most critical parameters for the inductor are the inductance, peak current and the DC resistance. The inductance is related to the peak-to-peak inductor ripple current, the input and the output voltages. Since the ripple current increases with the input voltage, the maximum input voltage is always used to determine the inductance. To calculate the minimum value of the output inductor, use [Equation 1](#).  $K_{IND}$  is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. A reasonable value is setting the ripple current to be 30% of the DC output current. For this design example, the minimum inductor value is calculated to be 9.1  $\mu$ H, and a nearest standard value was chosen: 10  $\mu$ H. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from [Equation 3](#) and [Equation 4](#). The inductor ripple current is 0.16 A, and the RMS current is 0.602 A. As the equation set demonstrates, lower ripple currents will reduce the output voltage ripple of the regulator but will require a larger value of inductance. A good starting point for most applications is a 10  $\mu$ H with 2 A current rating. Using a rating near 2 A will enable the LMR14006 to current limit without saturating the inductor. This is preferable to the LMR14006 going into thermal shutdown mode and the possibility of damaging the inductor if the output is shorted to ground or other long-term overload.

$$L_{o\ min} = \frac{V_{in\ max} - V_{out}}{I_o \times K_{IND}} \times \frac{V_{out}}{V_{in\ max} \times f_{sw}} \quad (1)$$

$$I_{ripple} = \frac{V_{out} \times (V_{in\ max} - V_{out})}{V_{in\ max} \times L_o \times f_{sw}} \quad (2)$$

$$I_{L-RMS} = \sqrt{I_o^2 + \frac{1}{12} I_{ripple}^2} \quad (3)$$

$$I_{L-peak} = I_o + \frac{I_{ripple}}{2} \quad (4)$$

### 8.1.2.3 Output Capacitor

The selection of  $C_{OUT}$  is mainly driven by three primary considerations. The output capacitor will determine the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 5 shows the minimum output capacitance necessary to accomplish this. For this example, the transient load response is specified as a 3% change in  $V_{OUT}$  for a load step from 0.03A to 0.6A (full load). For this example,  $\Delta I_{OUT} = 0.6 - 0.03 = 0.57$  A and  $\Delta V_{OUT} = 0.03 \times 5 = 0.15$  V. Using these numbers gives a minimum capacitance of 3.6 $\mu$ F. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation. Aluminum electrolytic and tantalum capacitors have higher ESR that should be taken into account.

The stored energy in the inductor will produce an output voltage overshoot when the load current rapidly decreases. The output capacitor must also be sized to absorb energy stored in the inductor when transitioning from a high load current to a lower load current. Equation 6 is used to calculate the minimum capacitance to keep the output voltage overshoot to a desired value. Where L is the value of the inductor,  $I_{OH}$  is the output current under heavy load,  $I_{OL}$  is the output under light load,  $V_f$  is the final peak output voltage, and  $V_i$  is the initial capacitor voltage. For this example, the worst case load step will be from 0.6 A to 0.03 A. The output voltage will increase during this load transition and the stated maximum in our specification is 3% of the output voltage. This will make  $V_o\_overshoot = 1.03 \times 5 = 5.15$  V.  $V_i$  is the initial capacitor voltage which is the nominal output voltage of 5V. Using these numbers in Equation 6 yields a minimum capacitance of 2.36  $\mu$ F.

Equation 7 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where  $f_{sw}$  is the switching frequency,  $V_o\_ripple$  is the maximum allowable output voltage ripple, and  $I_{L\_ripple}$  is the inductor ripple current. Equation 7 yields 0.21 $\mu$ F.

Equation 8 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 8 indicates the ESR should be less than 277m $\Omega$ .

Additional capacitance de-ratings for aging, temperature and dc bias should be factored in which will increase this minimum value. For this example, 10 $\mu$ F ceramic capacitors will be used. Capacitors in the range of 4.7 $\mu$ F-100 $\mu$ F are a good starting point with an ESR of 0.1 $\Omega$  or less.

$$C_{out} > \frac{2 \times \Delta I_{out}}{f_{sw} \times \Delta V_{out}} \quad (5)$$

$$C_{out} > L_o \times \frac{(I_{oh}^2 - I_{ol}^2)}{(V_f^2 - V_i^2)} \quad (6)$$

$$C_{out} > \frac{1}{8 \times f_{sw}} \times \frac{1}{\frac{V_o\_ripple}{I_{L\_ripple}}} \quad (7)$$

$$R_{ESR} < \frac{V_o\_ripple}{I_{L\_ripple}} \quad (8)$$

#### 8.1.2.4 Schottky Diode

The breakdown voltage rating of the diode is preferred to be 25% higher than the maximum input voltage. The current rating for the diode should be equal to the maximum output current for best reliability in most applications. In cases where the input voltage is much greater than the output voltage the average diode current is lower. In this case it is possible to use a diode with a lower average current rating, approximately  $(1-D) \times I_{OUT}$  however the peak current rating should be higher than the maximum load current. A 0.5A to 1A rated diode is a good starting point.

#### 8.1.2.5 Input Capacitor

A low ESR ceramic capacitor is needed between the  $V_{IN}$  pin and ground pin. This capacitor prevents large voltage transients from appearing at the input. Use a 1 $\mu$ F-10 $\mu$ F value with X5R or X7R dielectric. Depending on construction, a ceramic capacitor's value can decrease up to 50% of its nominal value when rated voltage is applied. Consult with the capacitor manufactures data sheet for information on capacitor derating over voltage and temperature. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the LMR14006. The input ripple current can be calculated using below Equation 9.

For this example design, one 2.2µF, 50V capacitor is selected. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 10. Using the design example values,  $I_{OUTmax} = 0.6A$ ,  $C_{IN} = 2.2\mu F$ ,  $f_{SW} = 2100kHz$ , yields an input voltage ripple of 32.5mV and a rms input ripple current of 0.3A.

$$I_{cirms} = I_{out} \times \sqrt{\frac{V_{out}}{V_{in\ min}} \times \frac{(V_{in\ min} - V_{out})}{V_{in\ min}}} \tag{9}$$

$$\Delta V_{in} = \frac{I_{out\ max} \times 0.25}{C_{in} \times f_{sw}} \tag{10}$$

### 8.1.2.6 Bootstrap Capacitor Selection

A 0.1µF ceramic capacitor or larger is recommended for the bootstrap capacitor ( $C_{BOOT}$ ). For applications where the input voltage is close to output voltage a larger capacitor is recommended, generally 0.1 µF to 1 µF to ensure plenty of gate drive for the internal switches and a consistently low  $R_{DS(ON)}$ . A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10V or higher is recommended because of the stable characteristics over temperature and voltage.

### 8.1.3 Application Performance Curves

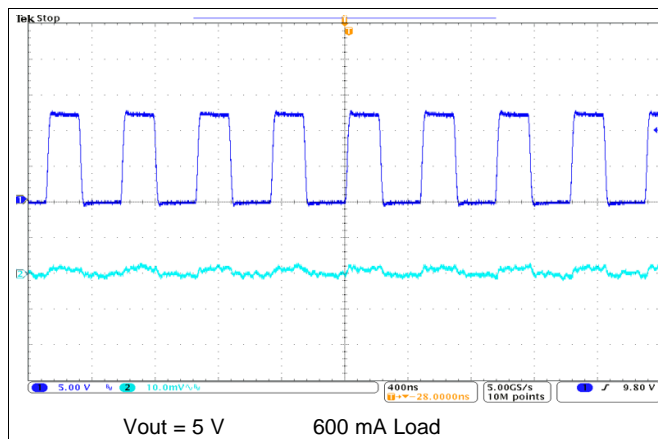


Figure 11. Switching Node And Output Voltage Waveform

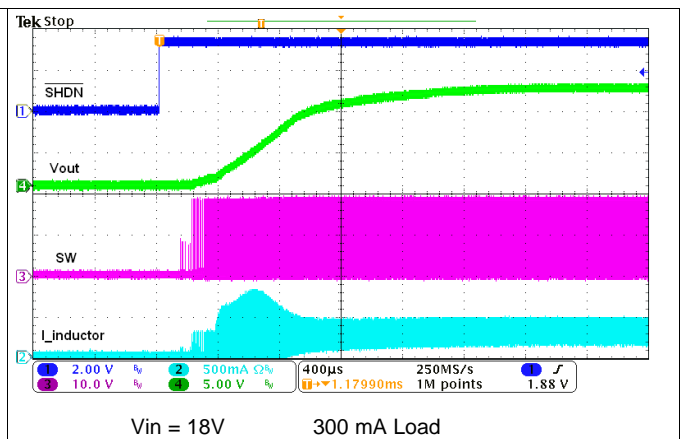


Figure 12. 12 V Output Start-Up Waveform

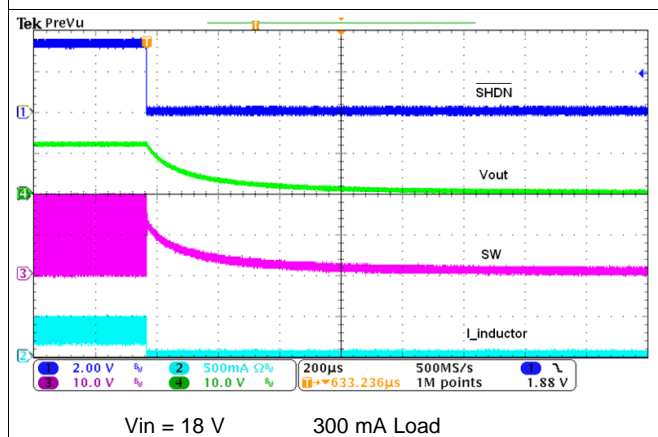


Figure 13. 12 V Output Shutdown Waveform

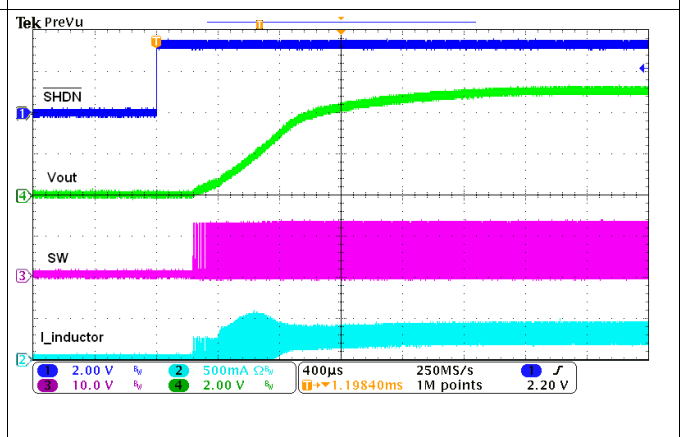


Figure 14. 5 V Output Start-Up Waveform (300 mA Load)

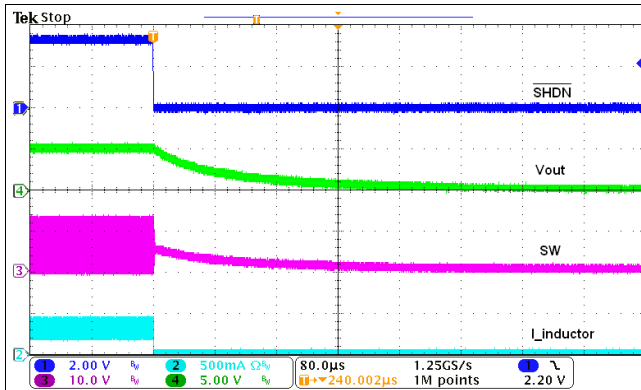


Figure 15. 5 V Output Shutdown Waveform (300 mA Load)

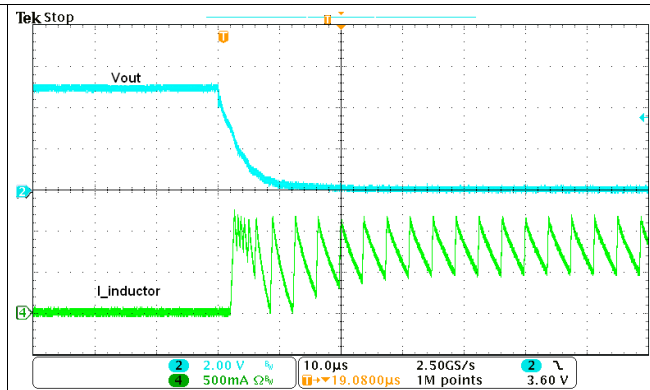


Figure 16. Short Circuit To Ground (5 V)

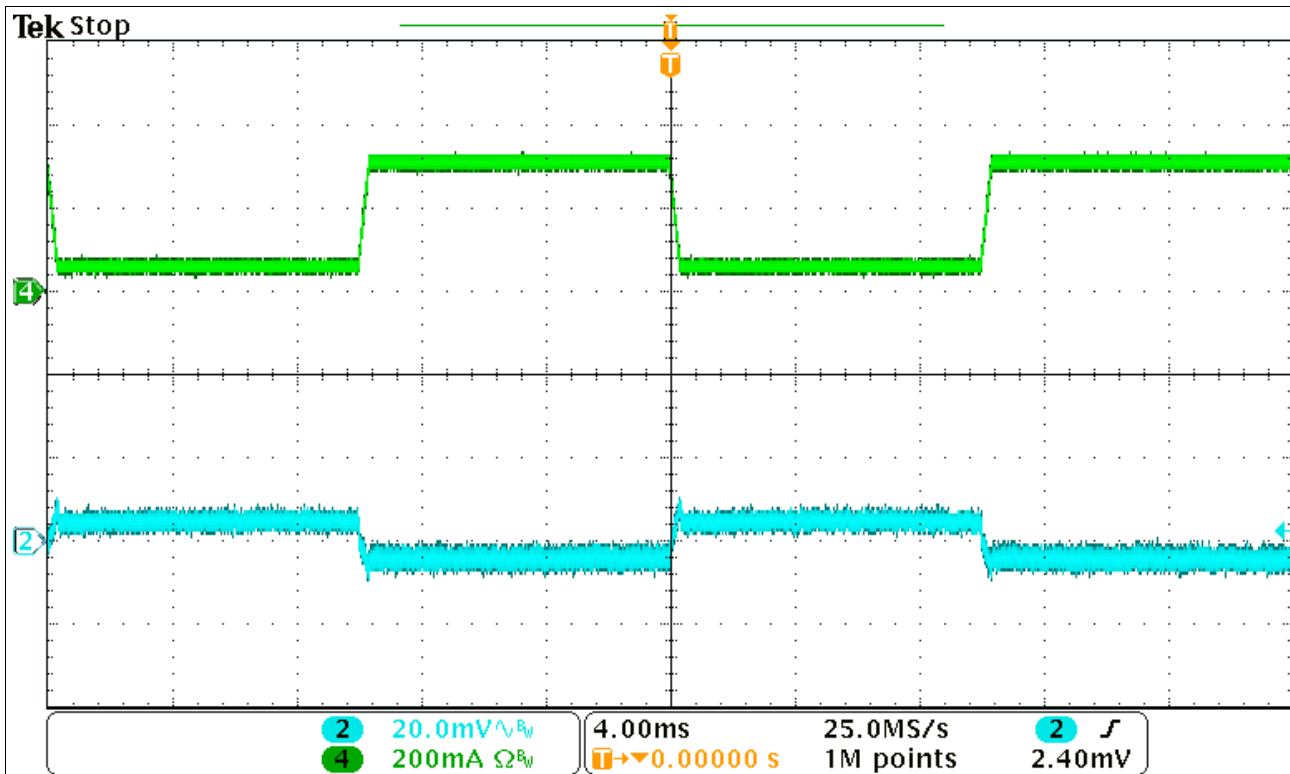


Figure 17. Load Transient Waveform (50 mA To 300 mA)

## 9 Layout

### 9.1 Layout Guidelines

To reduce problems with conducted noise pick up the ground side of feedback network should be connected directly to the GND pin with its own connection. The feedback network, resistors R1 and R2, should be kept close to the FB pin, and away from the inductor to minimize coupling noise into the feedback pin. The input bypass capacitor  $C_{IN}$  must be placed close to the VIN pin. This will reduce copper trace resistance which effects input voltage ripple of the IC. The inductor L1 should be placed close to the SW pin to reduce magnetic and electrostatic noise. The output capacitor,  $C_{OUT}$  should be placed close to the junction of L1 and the diode D1. The L1, D1, and  $C_{OUT}$  trace should be as short as possible to reduce conducted and radiated noise and increase overall efficiency. The ground connection for the diode,  $C_{IN}$ , and  $C_{OUT}$  should be as small as possible and tied to the system ground plane in only one spot (preferably at the  $C_{OUT}$  ground point) to minimize conducted noise in the system ground plane. For more detail on switching power supply layout considerations see Application Note AN-1149.



## 10 Device and Documentation Support

### 10.1 Trademarks

SIMPLE SWITCHER is a registered trademark of Texas Instruments. All other trademarks are the property of their respective owners.

### 10.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 10.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMR14006XDDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B02X	<a href="#">Samples</a>
LMR14006XDDCT	ACTIVE	SOT-23-THIN	DDC	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B02X	<a href="#">Samples</a>
LMR14006YDDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B02Y	<a href="#">Samples</a>
LMR14006YDDCT	ACTIVE	SOT-23-THIN	DDC	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B02Y	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

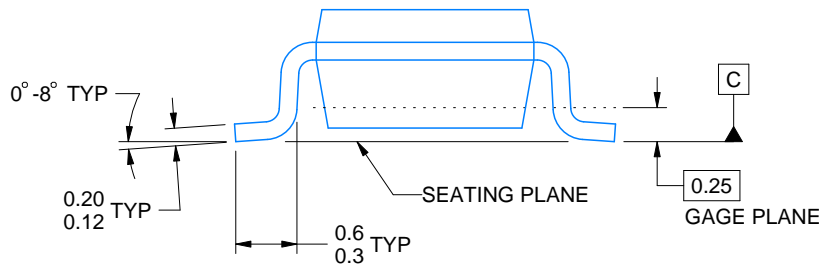
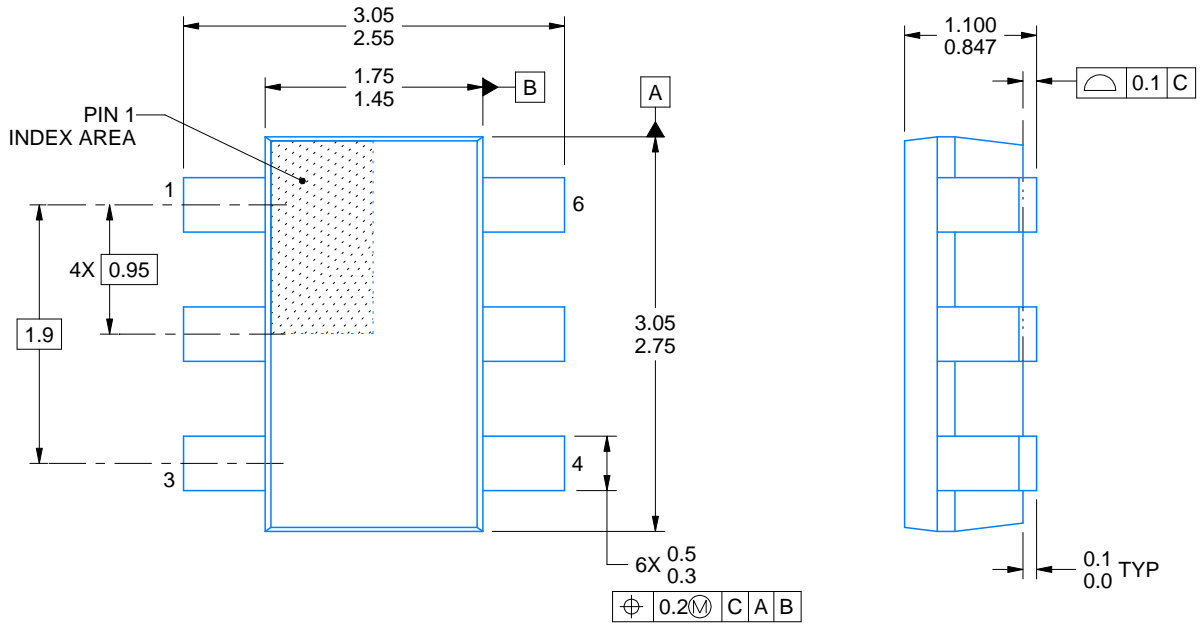

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR14006XDDCR	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR14006XDDCT	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR14006YDDCR	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR14006YDDCT	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

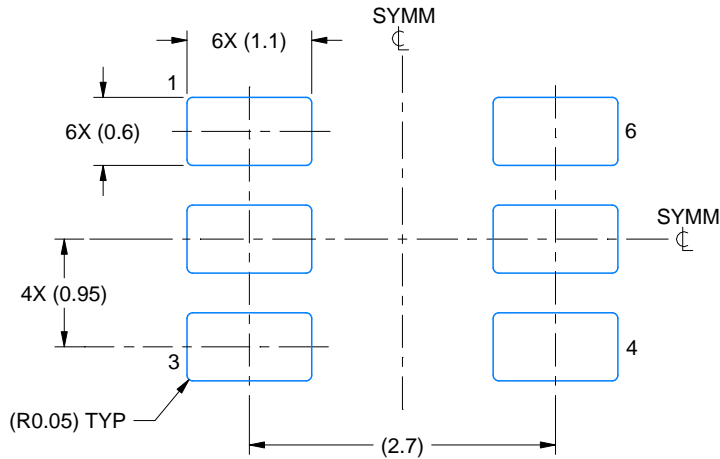
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR14006XDDCR	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0
LMR14006XDDCT	SOT-23-THIN	DDC	6	250	208.0	191.0	35.0
LMR14006YDDCR	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0
LMR14006YDDCT	SOT-23-THIN	DDC	6	250	208.0	191.0	35.0



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE  
EXPLODED METAL SHOWN  
SCALE:15X

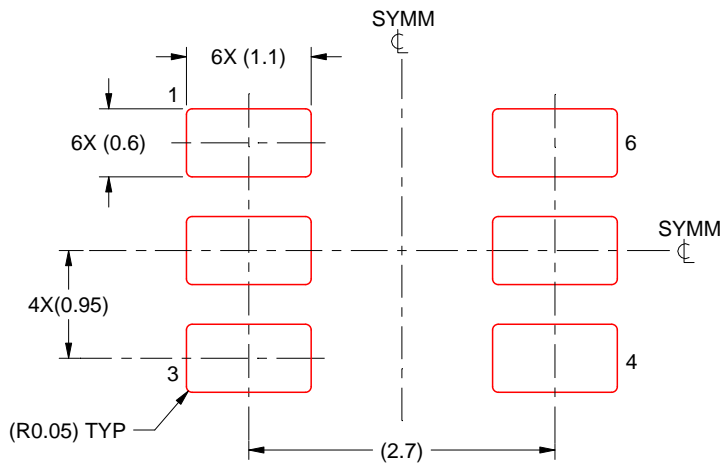


SOLDEMASK DETAILS

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NOTES: (continued)

- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 THICK STENCIL  
 SCALE:15X

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NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 7. Board assembly site may have different recommendations for stencil design.



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