

# LMV34x Rail-to-Rail Output CMOS Operational Amplifiers With Shutdown

## 1 Features

- 2.7-V and 5-V Performance
- Rail-to-Rail Output Swing
- Input Bias Current: 1 pA (Typical)
- Input Offset Voltage: 0.25 mV (Typical)
- Low Supply Current: 100  $\mu$ A (Typical)
- Low Shutdown Current: 45 pA (Typical)
- Gain Bandwidth of 1 MHz (Typical)
- Slew Rate: 1 V/ $\mu$ s (Typical)
- Turnon Time From Shutdown: 5  $\mu$ s (Typical)
- Input Referred Voltage Noise (at 10 kHz): 20 nV/ $\sqrt{\text{Hz}}$
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (HBM)
  - 750-V Charged-device model (CDM)

## 2 Applications

- Cordless and Cellular Phones
- Consumer Electronics (Laptops, PDAs)
- Audio Preamplifiers for Voice
- Portable, Battery-Powered Electronic Equipment
- Supply-Current Monitoring
- Battery Monitoring
- Buffers
- Filters
- Drivers

## 3 Description

The LMV34x devices are single, dual, and quad CMOS operational amplifiers, respectively, with low voltage, low power, and rail-to-rail output swing capabilities. The PMOS input stage offers an ultra-low input bias current of 1 pA (typical) and an offset voltage of 0.25 mV (typical). The single-supply amplifier is designed specifically for low-voltage (2.7 V to 5 V) operation, with a wide common-mode input voltage range that typically extends from -0.2 V to 0.8 V from the positive supply rail. The LMV341 (single) also offers a shutdown (SHDN) pin that can be used to disable the device. In shutdown mode, the supply current is reduced to 33 nA (typical). Additional features of the family are a 20-nV/ $\sqrt{\text{Hz}}$  voltage noise at 10 kHz, 1-MHz unity-gain bandwidth, 1-V/ $\mu$ s slew rate, and 100- $\mu$ A current consumption per channel.

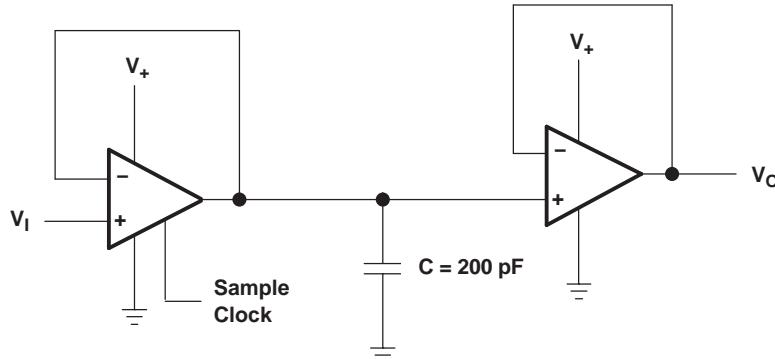
Offered in both the SOT-23 and smaller SC70 packages, the LMV341 is suitable for the most space-constraint applications. The LMV342 dual device is offered in the standard SOIC and VSSOP packages. An extended industrial temperature range from -40°C to 125°C makes these devices suitable in a wide variety of commercial and industrial environments.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMV341IDCK	SC70 (6)	2.00 mm x 1.25 mm
LMV341IDBV	SOT-23 (6)	2.90 mm x 1.60 mm
LMV342ID	SOIC (8)	4.90 mm x 3.91 mm
LMV342IDGK	VSSOP (8)	3.00 mm x 3.00 mm
LMV344ID	SOIC (14)	8.65 mm x 3.91 mm
LMV344IPW	TSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Sample-and-Hold Circuit



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

## Table of Contents

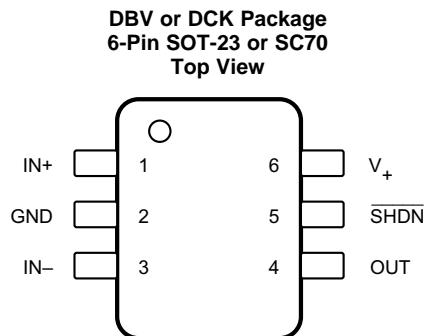
<b>1</b>	<b>Features</b> .....	<b>1</b>	7.2	Functional Block Diagram .....	<b>14</b>
<b>2</b>	<b>Applications</b> .....	<b>1</b>	7.3	Feature Description .....	<b>14</b>
<b>3</b>	<b>Description</b> .....	<b>1</b>	7.4	Device Functional Modes .....	<b>14</b>
<b>4</b>	<b>Revision History</b> .....	<b>2</b>	<b>8</b>	<b>Application and Implementation</b> .....	<b>15</b>
<b>5</b>	<b>Pin Configuration and Functions</b> .....	<b>3</b>	8.1	Application Information .....	<b>15</b>
<b>6</b>	<b>Specifications</b> .....	<b>4</b>	8.2	Typical Application .....	<b>15</b>
6.1	Absolute Maximum Ratings .....	4	<b>9</b>	<b>Power Supply Recommendations</b> .....	<b>16</b>
6.2	ESD Ratings .....	5	<b>10</b>	<b>Layout</b> .....	<b>17</b>
6.3	Recommended Operating Conditions .....	5	10.1	Layout Guidelines .....	<b>17</b>
6.4	Thermal Information .....	5	10.2	Layout Examples .....	<b>17</b>
6.5	Electrical Characteristics: $V_+ = 2.7$ V .....	5	<b>11</b>	<b>Device and Documentation Support</b> .....	<b>18</b>
6.6	Electrical Characteristics: $V_+ = 5$ V .....	6	11.1	Related Links .....	<b>18</b>
6.7	Shutdown Characteristics: $V_+ = 2.7$ V .....	7	11.2	Community Resources .....	<b>18</b>
6.8	Shutdown Characteristics: $V_+ = 5$ V .....	7	11.3	Trademarks .....	<b>18</b>
6.9	Typical Characteristics .....	8	11.4	Electrostatic Discharge Caution .....	<b>18</b>
<b>7</b>	<b>Detailed Description</b> .....	<b>14</b>	11.5	Glossary .....	<b>18</b>
7.1	Overview .....	14	<b>12</b>	<b>Mechanical, Packaging, and Orderable</b> <b>Information</b> .....	<b>18</b>

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

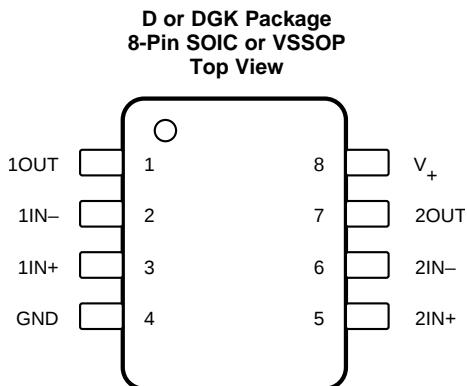
<b>Changes from Revision H (June 2012) to Revision I</b>	<b>Page</b>
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1
• Removed <i>Ordering Information</i> table .....	1

## 5 Pin Configuration and Functions



**Pin Functions: LMV341**

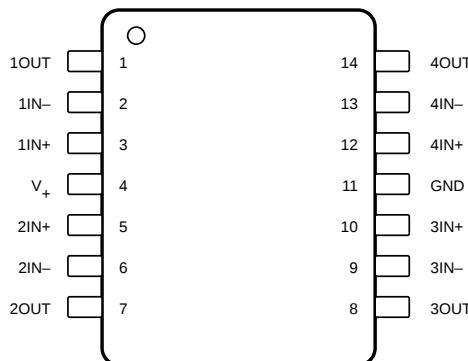
PIN		I/O	DESCRIPTION
NAME	SOT-23, SC70		
IN+	1	I	Noninverting input on channel 1
IN-	3	I	Inverting input on channel 1
OUT	4	O	Output on channel 1
GND	2	—	Ground
SHDN	5	I	Shutdown active low
V <sub>+</sub>	6	—	Positive power supply



**Pin Functions: LMV342**

PIN		I/O	DESCRIPTION
NAME	SOIC, VSSOP		
1IN+	3	I	Noninverting input on channel 1
1IN-	2	I	Inverting input on channel 1
1OUT	1	O	Output on channel 1
2IN+	5	I	Noninverting input on channel 2
2IN-	6	I	Inverting input on channel 2
2OUT	7	O	Output on channel 2
GND	4	—	Ground
V <sub>+</sub>	8	—	Positive power supply

**D or PW Package  
14-Pin SOIC or TSSOP  
Top View**



**Pin Functions: LMV344**

PIN		I/O	DESCRIPTION
NAME	SOIC, TSSOP		
1IN+	3	I	Noninverting input on channel 1
1IN-	2	I	Inverting input on channel 1
1OUT	1	O	Output on channel 1
2IN+	5	I	Noninverting input on channel 2
2IN-	6	I	Inverting input on channel 2
2OUT	7	O	Output on channel 2
3IN+	10	I	Noninverting input on channel 3
3IN-	9	I	Inverting input on channel 3
3OUT	8	O	Output on channel 3
4IN+	12	I	Noninverting input on channel 4
4IN-	13	I	Inverting input on channel 4
4OUT	14	O	Output on channel 4
GND	11	—	Ground
V <sub>+</sub>	4	—	Positive power supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>+</sub>	Supply voltage <sup>(2)</sup>	-0.3	5.5	V
V <sub>ID</sub>	Differential input voltage <sup>(3)</sup>		±5.5	V
V <sub>I</sub>	Input voltage (either input)	-0.3	5.5	V
V <sub>O</sub>	Output voltage	-0.3	V <sub>CC</sub> + 0.3	V
T <sub>J</sub>	Operating virtual junction temperature		150	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values (except differential voltages) are with respect to the network GND.

(3) Differential voltages are at IN+ with respect to IN-.

## 6.2 ESD Ratings

				VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>			±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>			±750

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

				MIN	MAX	UNIT
V <sub>+</sub>	Supply voltage (single-supply operation)			2.5	5.5	V
T <sub>A</sub>	Operating free-air temperature			-40	125	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	LMV342	LMV344	LMV341		LMV342	LMV344	UNIT
	D (SOIC)		DBV (SOT-23)	DCK (SC70)	DGK (VSSOP)	PW (TSSOP)	
	8 PINS	14 PINS	6 PINS	6 PINS	8 PINS	14 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(2) (3)</sup>	123.9	88.7	193.4	196.8	192.3	118 °C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	70.2	49	145.6	82.4	78.2	46.9 °C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	64.1	43	44.1	95.2	112.6	59.7 °C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	25	16.9	34.1	1.8	15.2	5.1 °C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	63.6	42.7	43.4	93.2	111.2	59.1 °C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

(2) Maximum power dissipation is a function of T<sub>J</sub>(max), R<sub>θJA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J</sub>(max) – T<sub>A</sub>)/R<sub>θJA</sub>. Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

## 6.5 Electrical Characteristics: V<sub>+</sub> = 2.7 V

V<sub>+</sub> = 2.7 V, GND = 0 V, V<sub>IC</sub> = V<sub>O</sub> = V<sub>+</sub>/2, R<sub>L</sub> > 1 MΩ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T <sub>A</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>IO</sub>	Input offset voltage	25°C		0.25	4	mV
		Full range			4.5	
α <sub>VIO</sub>	Average temperature coefficient of input offset voltage	Full range		1.7		µV/°C
I <sub>IB</sub>	Input bias current	25°C		1	120	pA
		–40°C to 85°C			250	
		–40°C to 125°C			3	
I <sub>IO</sub>	Input offset current	25°C		6.6		fA
CMRR	Common-mode rejection ratio	0 ≤ V <sub>ICR</sub> ≤ 1.7 V	25°C	56	80	dB
		0 ≤ V <sub>ICR</sub> ≤ 1.6 V	Full range	50		
k <sub>SVR</sub>	Supply-voltage rejection ratio	2.7 V ≤ V <sub>+</sub> ≤ 5 V	25°C	65	82	dB
			Full range	60		
V <sub>ICR</sub>	Common-mode input voltage range	Lower range, CMRR ≥ 50 dB	25°C	–0.2	0	V
		Upper range, CMRR ≥ 50 dB	25°C	1.7	1.9	
A <sub>V</sub>	Large-signal voltage gain <sup>(2)</sup>	R <sub>L</sub> = 10 kΩ to 1.35 V	25°C	78	113	dB
			Full range	70		
		R <sub>L</sub> = 2 kΩ to 1.35 V	25°C	72	103	
			Full range	64		

(1) Typical values represent the most likely parametric norm.

(2) GND + 0.2 V ≤ V<sub>O</sub> ≤ V<sub>+</sub> – 0.2 V

## Electrical Characteristics: $V_+ = 2.7$ V (continued)

$V_+ = 2.7$  V, GND = 0 V,  $V_{IC} = V_O = V_+/2$ ,  $R_L > 1$  MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A$	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_O$	Output swing (delta from supply rails)	$R_L = 2$ kΩ to 1.35 V	Low level	25°C	24	60		mV
				Full range		95		
			High level	25°C	26	60		
				Full range		95		
		$R_L = 10$ kΩ to 1.35 V	Low level	25°C	5	30		
				Full range		40		
			High level	25°C	5.3	30		
				Full range		40		
				25°C	100	170		
				Full range		230		
$I_{CC}$	Supply current (per channel)							μA
$I_{OS}$	Output short-circuit current	Sourcing	LMV341, LMV342	25°C	20	32		mA
			LMV344		18	24		
		Sinking			15	24		
SR	Slew rate	$R_L = 10$ kΩ <sup>(3)</sup>		25°C		1		V/μs
GBM	Unity-gain bandwidth	$R_L = 10$ kΩ, $C_L = 200$ pF		25°C		1		MHz
$\Phi_m$	Phase margin	$R_L = 100$ kΩ		25°C		72		°
$G_m$	Gain margin	$R_L = 100$ kΩ		25°C		20		dB
$V_n$	Equivalent input noise voltage	$f = 1$ kHz		25°C		40		nV/√Hz
$I_n$	Equivalent input noise current	$f = 1$ kHz		25°C		0.001		pA/√Hz
THD	Total harmonic distortion	$f = 1$ kHz, $A_V = 1$ , $R_L = 600$ Ω, $V_I = 1$ V <sub>PP</sub>		25°C		0.017%		

(3) Connected as voltage follower with 2-V<sub>PP</sub> step input. Number specified is the slower of the positive and negative slew rates.

## 6.6 Electrical Characteristics: $V_+ = 5$ V

$V_+ = 5$  V, GND = 0 V,  $V_{IC} = V_O = V_+/2$ ,  $R_L > 1$  MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A$	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{IO}$	Input offset voltage			25°C	0.25	4		mV
				Full range		4.5		
$\alpha_{VIO}$	Average temperature coefficient of input offset voltage			Full range		1.9		μV/°C
$I_{IB}$	Input bias current			25°C	1	200		pA
				–40°C to 85°C		375		
				–40°C to 125°C		5	nA	
$I_{IO}$	Input offset current			25°C		6.6		fA
CMRR	Common-mode rejection ratio	$0 \leq V_{ICR} \leq 4$ V		25°C	56	86		dB
				Full range	50			
$k_{SVR}$	Supply-voltage rejection ratio	$2.7 \text{ V} \leq V_+ \leq 5 \text{ V}$		25°C	65	82		dB
				Full range	60			
$V_{ICR}$	Common-mode input voltage range	Lower range, CMRR $\geq 50$ dB		25°C		–0.2	0	V
				25°C	4	4.2		
$A_V$	Large-signal voltage gain <sup>(2)</sup>	$R_L = 10$ kΩ to 2.5 V		25°C	78	116		dB
				Full range	70			
		$R_L = 2$ kΩ to 2.5 V		25°C	72	107		
				Full range	64			

(1) Typical values represent the most likely parametric norm.

(2)  $GND + 0.2$  V  $\leq V_O \leq V_+ - 0.2$  V

## Electrical Characteristics: $V_+ = 5$ V (continued)

$V_+ = 5$  V, GND = 0 V,  $V_{IC} = V_O = V_+/2$ ,  $R_L > 1$  MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A$	MIN	TYP <sup>(1)</sup>	MAX	UNIT	
$V_O$	Output swing (delta from supply rails)	$R_L = 2$ kΩ to 2.5 V	Low level	25°C		32	60	mV	
				Full range			95		
			High level	25°C		34	60		
				Full range			95		
		$R_L = 10$ kΩ to 2.5 V	Low level	25°C		7	30		
				Full range			40		
			High level	25°C		7	30		
				Full range			40		
				25°C		107	200	$\mu$ A	
				Full range			260		
$I_{CC}$	Supply current (per channel)		Sourcing	25°C	85	113		mA	
					85	113			
					50	75			
SR	Slew rate	$R_L = 10$ kΩ <sup>(3)</sup>		25°C		1		V/μs	
GBM	Unity-gain bandwidth	$R_L = 10$ kΩ, $C_L = 200$ pF		25°C		1		MHz	
$\Phi_m$	Phase margin	$R_L = 100$ kΩ		25°C		70		°	
$G_m$	Gain margin	$R_L = 100$ kΩ		25°C		20		dB	
$V_n$	Equivalent input noise voltage	$f = 1$ kHz		25°C		39		nV/√Hz	
$I_n$	Equivalent input noise current	$f = 1$ kHz		25°C		0.001		pA/√Hz	
THD	Total harmonic distortion	$f = 1$ kHz, $A_V = 1$ , $R_L = 600$ Ω, $V_I = 1$ V <sub>PP</sub>		25°C		0.012%			

(3) Connected as voltage follower with 2-V<sub>PP</sub> step input. Number specified is the slower of the positive and negative slew rates.

## 6.7 Shutdown Characteristics: $V_+ = 2.7$ V

$V_+ = 2.7$  V, GND = 0 V,  $V_{IC} = V_O = V_+/2$ ,  $R_L > 1$  MΩ (unless otherwise noted)

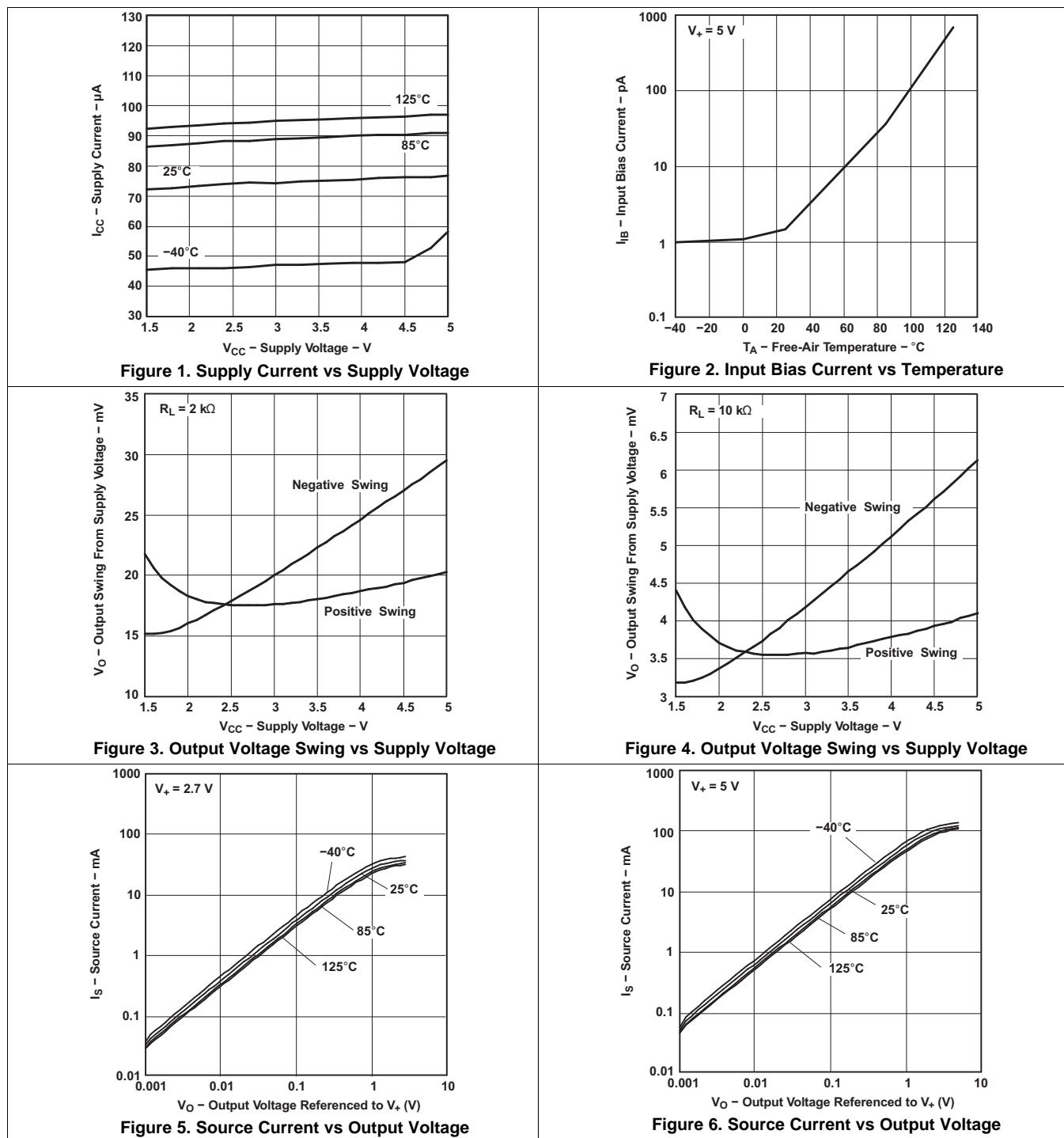
PARAMETER		TEST CONDITIONS		$T_A$	MIN	TYP	MAX	UNIT
$I_{CC(SHDN)}$	Supply current in shutdown mode	$V_{SD} = 0$ V		25°C		0.045	1000	nA
				Full range			1.5	$\mu$ A
$t_{(on)}$	Amplifier turnon time			25°C		5		μs
$V_{SD}$	Recommended shutdown pin voltage range	ON mode		25°C	2.4		2.7	V
		Shutdown mode			0		0.8	

## 6.8 Shutdown Characteristics: $V_+ = 5$ V

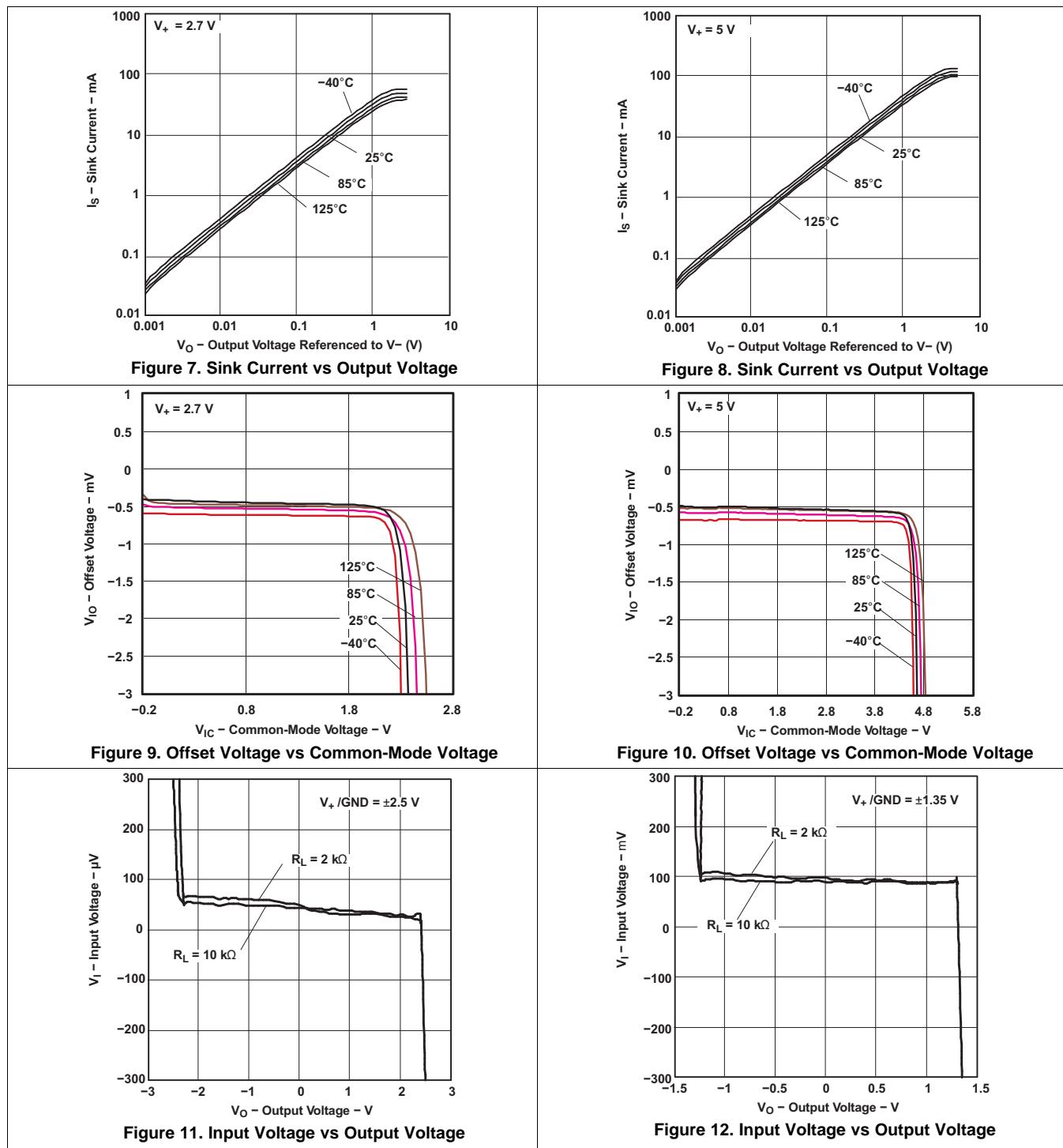
$V_+ = 5$  V, GND = 0 V,  $V_{IC} = V_O = V_+/2$ ,  $R_L > 1$  MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A$	MIN	TYP	MAX	UNIT
$I_{CC(SHDN)}$	Supply current in shutdown mode	$V_{SD} = 0$ V		25°C		0.033	1	$\mu$ A
				Full range			1.5	
$t_{(on)}$	Amplifier turnon time			25°C		5		μs
$V_{SD}$	Recommended shutdown pin voltage range	ON mode		25°C	4.5		5	V
		Shutdown mode			0		0.8	

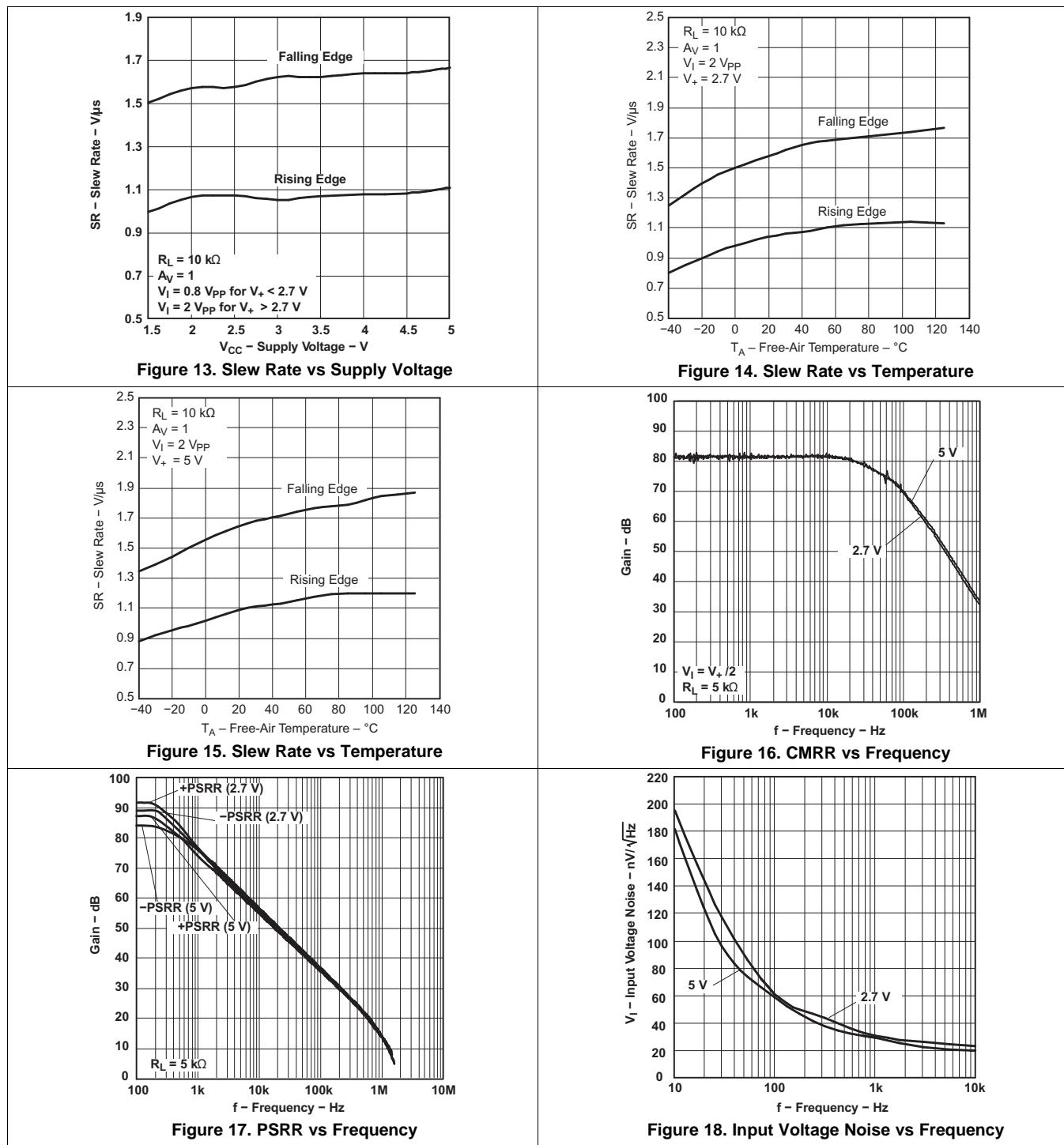
## 6.9 Typical Characteristics



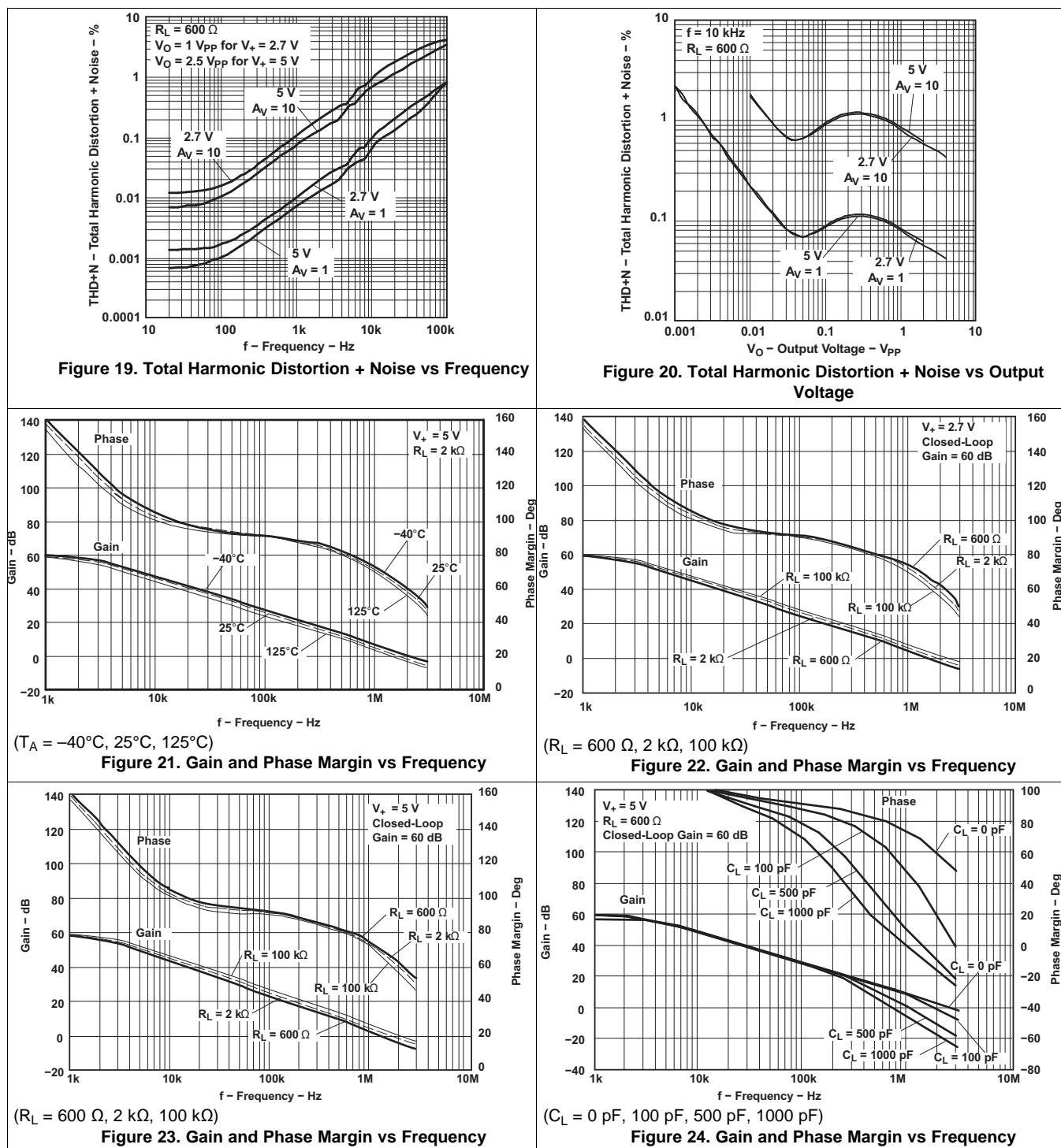
## Typical Characteristics (continued)

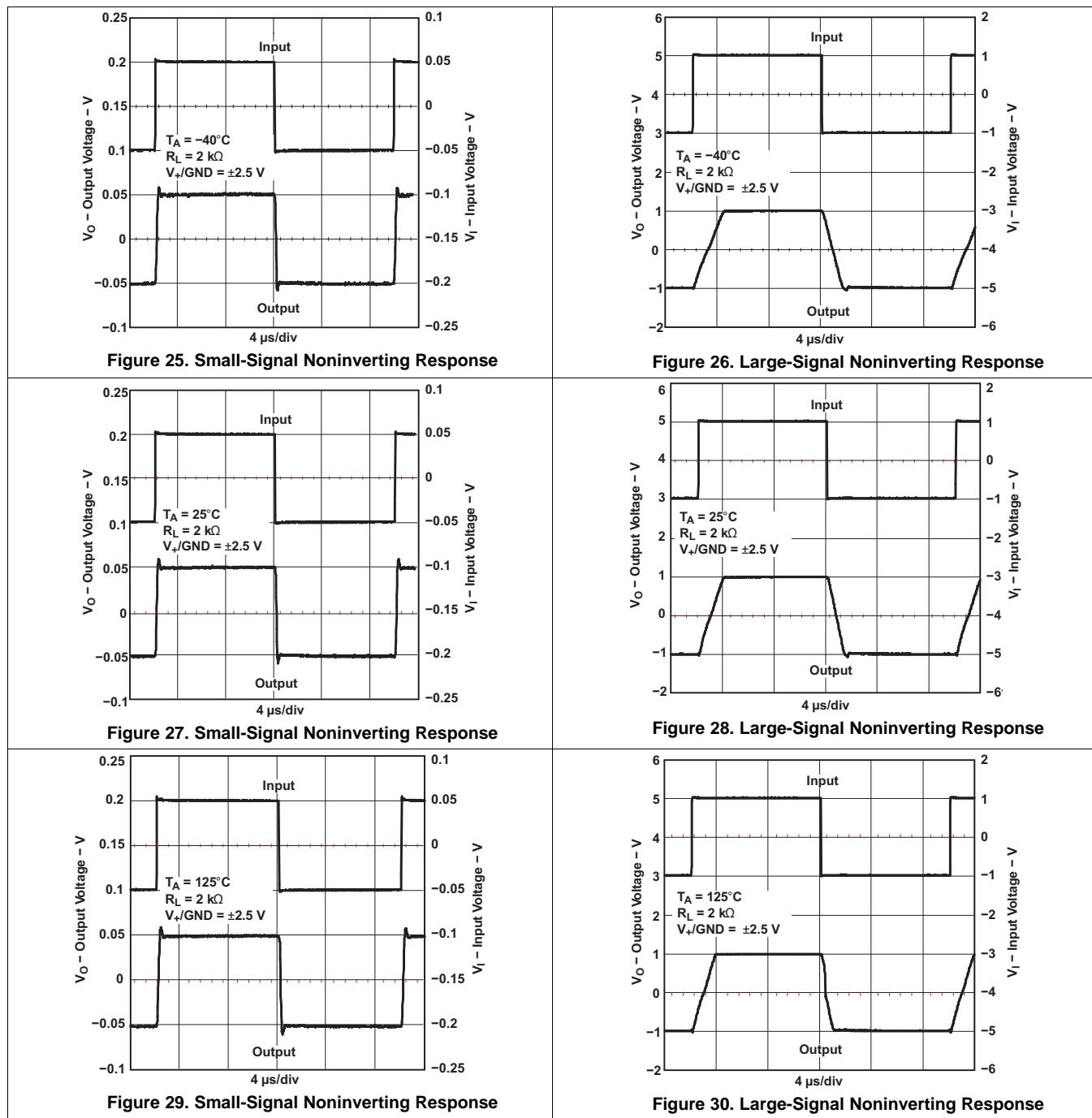


## Typical Characteristics (continued)



## Typical Characteristics (continued)



**Typical Characteristics (continued)**


## Typical Characteristics (continued)

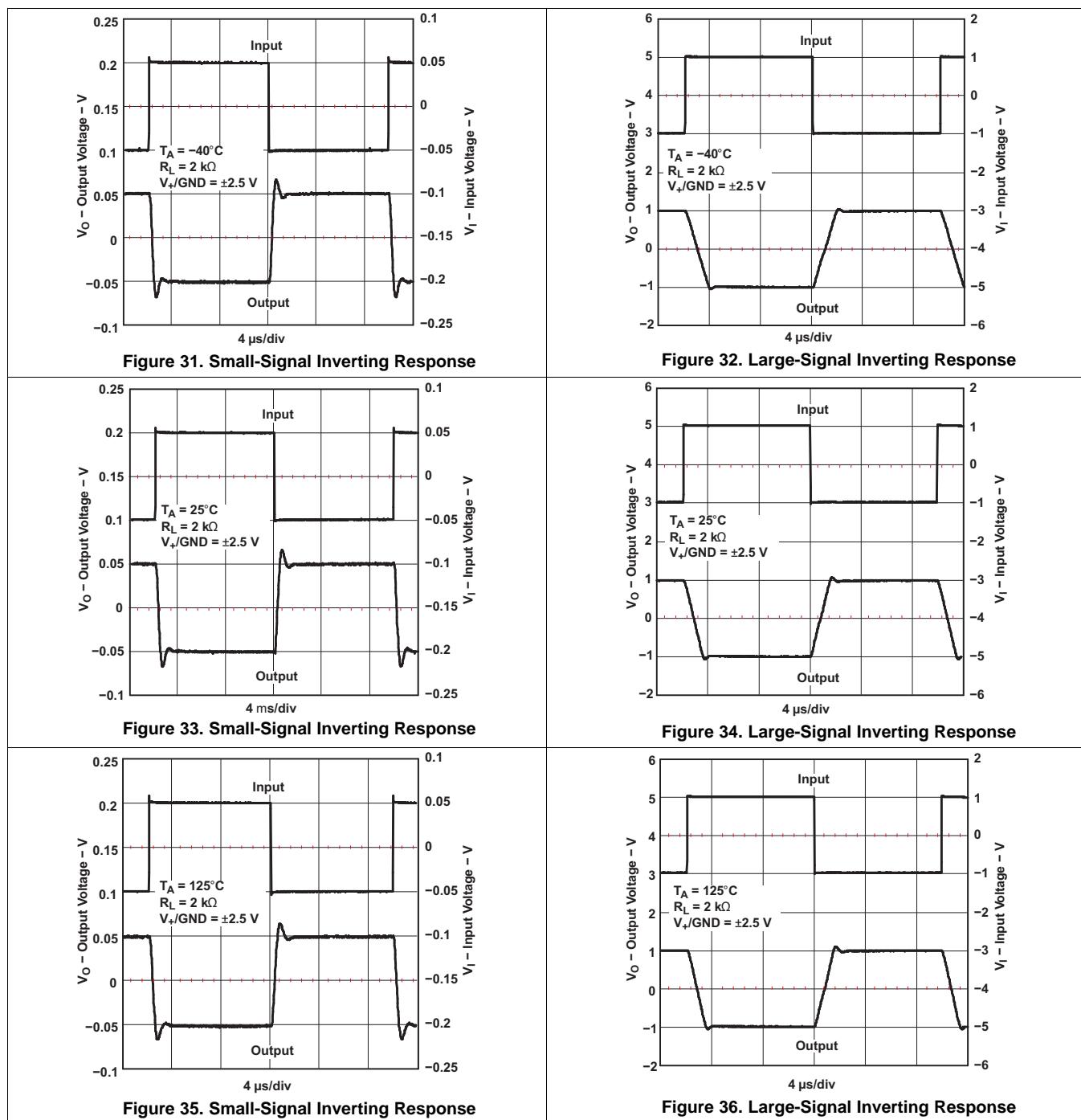


Figure 31. Small-Signal Inverting Response

Figure 32. Large-Signal Inverting Response

Figure 33. Small-Signal Inverting Response

Figure 34. Large-Signal Inverting Response

Figure 35. Small-Signal Inverting Response

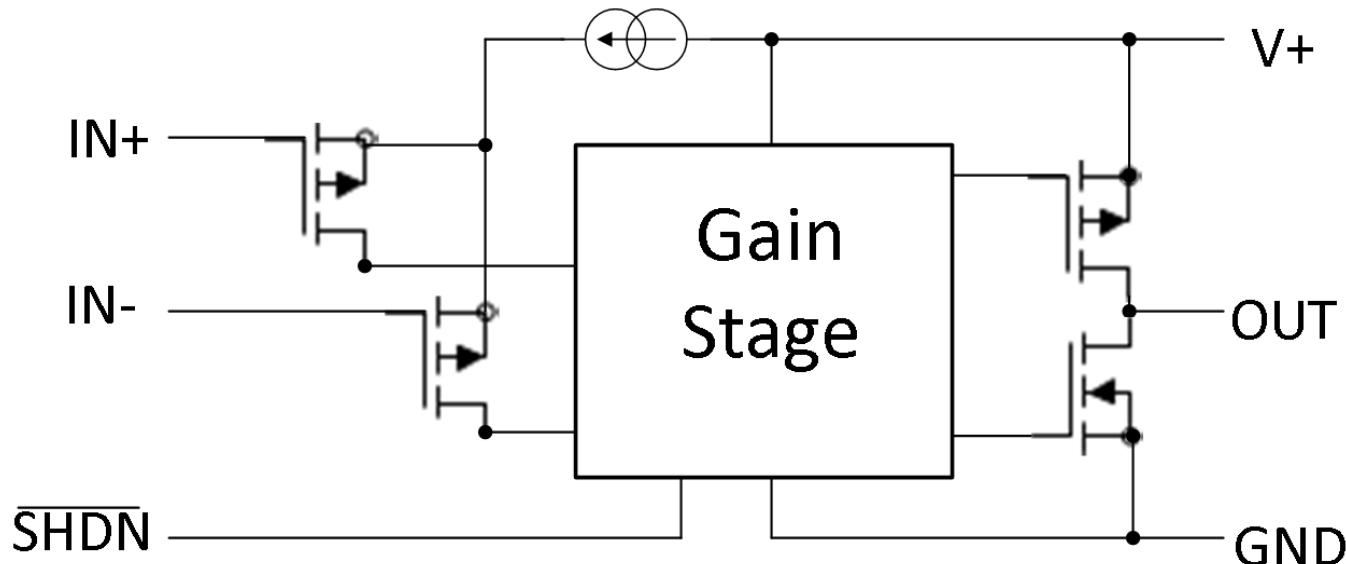
Figure 36. Large-Signal Inverting Response

## 7 Detailed Description

### 7.1 Overview

The LMV34x devices are precision operational amplifiers with CMOS inputs for very low input bias current. Output is rail-to-rail and input common-mode includes ground. LMV341 has a shutdown mode for very low supply current.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 PMOS Input Stage

PMOS Input Stage supports a lower input range that includes ground. Upper range limit is  $V_+ - 1\text{ V}$ .

#### 7.3.2 CMOS Output Stage

The CMOS drain output topology allows rail-to-rail output swing.

#### 7.3.3 Shutdown

LMV341 includes a shutdown pin. During shutdown,  $I_{CC}$  is nearly zero and the output becomes high impedance. The typical turnon time coming out of shutdown is 5  $\mu\text{s}$ .

## 7.4 Device Functional Modes

The LMV34x devices have two modes of operation:

- Normal operation when  $\overline{\text{SHDN}}$  pin is at  $V_+$  level or the  $\overline{\text{SHDN}}$  pin is not present
- Shutdown mode when  $\overline{\text{SHDN}}$  is at GND level;  $I_{CC}$  is very low and output is high impedance.

## 8 Application and Implementation

### NOTE

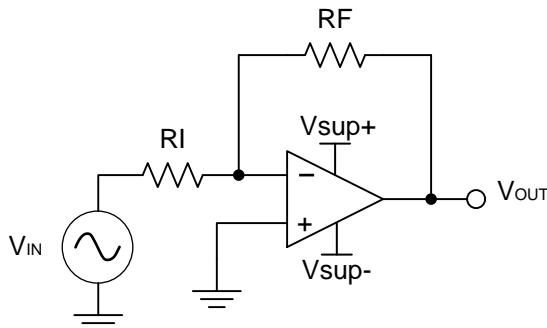
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

LMV34x devices have rail-to-rail output and input range from ground to VCC – 1 V. CMOS inputs provide very low input current. Shutdown capability is an option in dual amplifier version. Operation from 2.5-V to 5.5-V is possible.

### 8.2 Typical Application

A typical application for an operational amplifier in an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.



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**Figure 37. Application Schematic**

#### 8.2.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application scales a signal of  $\pm 0.5$  V to  $\pm 1.8$  V. Setting the supply at  $\pm 2$  V is sufficient to accommodate this application. The supplies can power up in any order; however, neither supply can be of opposite polarity relative to ground at any time; otherwise, a large current can flow through the input ESD diodes. To limit current in such an occurrence, TI highly recommends adding a series resistor to the grounded input.  $V_{sup+}$  must be more positive than  $V_{sup-}$  at all times; otherwise, a large reverse supply current may flow.

#### 8.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using [Equation 1](#) and [Equation 2](#).

$$A_v = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$A_v = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

Once the desired gain is determined, choose a value for  $R_I$  or  $R_F$ . Choosing a value in the  $k\Omega$  range is desirable because the amplifier circuit uses currents in the mA range. This ensures the part does not draw too much current. For this example, choose  $10\text{ k}\Omega$  for  $R_I$ , which means  $36\text{ k}\Omega$  is used for  $R_F$ . This was determined by [Equation 3](#).

$$A_v = -\frac{R_F}{R_I} \quad (3)$$

## Typical Application (continued)

### 8.2.3 Application Curve

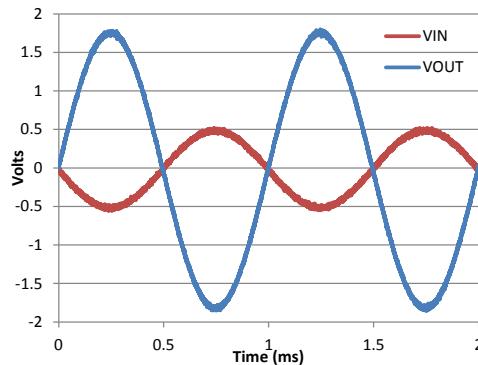


Figure 38. Input and Output Voltages of the Inverting Amplifier

## 9 Power Supply Recommendations

### CAUTION

Supply voltages larger than 5.5 V for a single supply can permanently damage the device (see the [Absolute Maximum Ratings](#)).

Place 0.1- $\mu$ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

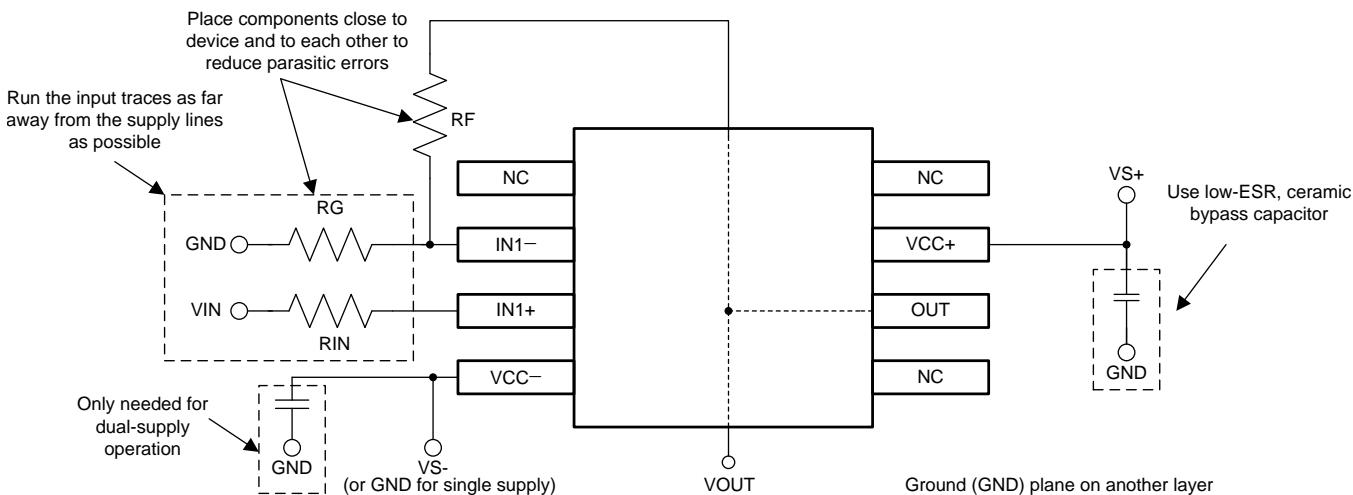
## 10 Layout

### 10.1 Layout Guidelines

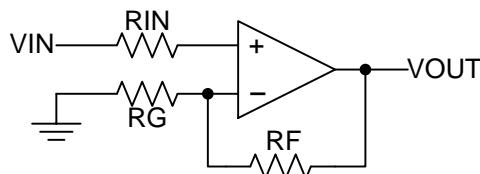
For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from  $V_+$  to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, and pay attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in [Layout Examples](#).
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

### 10.2 Layout Examples



**Figure 39. Operational Amplifier Layout for Noninverting Configuration**



**Figure 40. Operational Amplifier Schematic for Noninverting Configuration**

## 11 Device and Documentation Support

### 11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMV341	<a href="#">Click here</a>				
LMV342	<a href="#">Click here</a>				
LMV344	<a href="#">Click here</a>				

### 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.3 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 11.4 Electrostatic Discharge Caution

 This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

 ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.5 Glossary

**SLYZ022 — TI Glossary.**

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV341IDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(RC9A, RC9E, RC9S)	<a href="#">Samples</a>
LMV341IDBVRE4	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(RC9A, RC9E, RC9S)	<a href="#">Samples</a>
LMV341IDBVRG4	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(RC9A, RC9E, RC9S)	<a href="#">Samples</a>
LMV341IDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R4A, R4E)	<a href="#">Samples</a>
LMV341IDCKRG4	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R4A, R4E)	<a href="#">Samples</a>
LMV342ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV342I	<a href="#">Samples</a>
LMV342IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RPA	<a href="#">Samples</a>
LMV342IDGKRG4	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RPA	<a href="#">Samples</a>
LMV342IDGKT	PREVIEW	VSSOP	DGK	8	250	TBD	Call TI	Call TI	-40 to 125		
LMV342IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV342I	<a href="#">Samples</a>
LMV342IDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV342I	<a href="#">Samples</a>
LMV344ID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV344I	<a href="#">Samples</a>
LMV344IDG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV344I	<a href="#">Samples</a>
LMV344IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV344I	<a href="#">Samples</a>
LMV344IPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV344I	<a href="#">Samples</a>
LMV344IPWG4	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV344I	<a href="#">Samples</a>
LMV344IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV344I	<a href="#">Samples</a>
LMV344IPWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV344I	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

**(2) RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3) MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

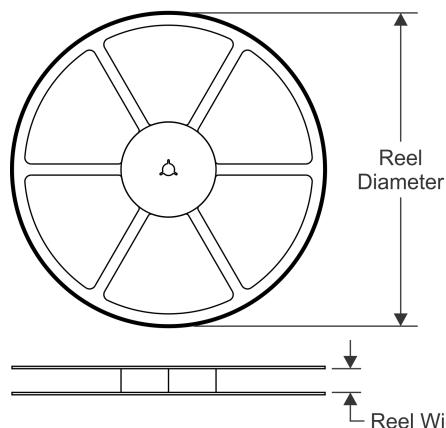
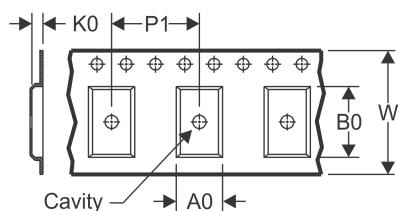
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF LMV341, LMV344 :**

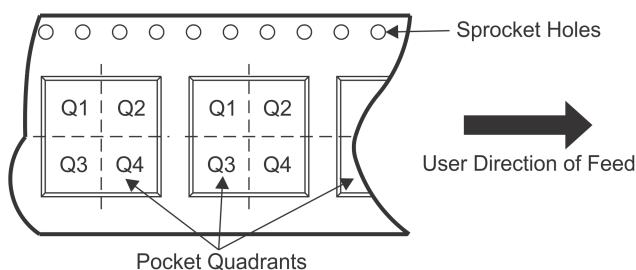
- Automotive : [LMV341-Q1](#), [LMV344-Q1](#)

**NOTE: Qualified Version Definitions:**

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

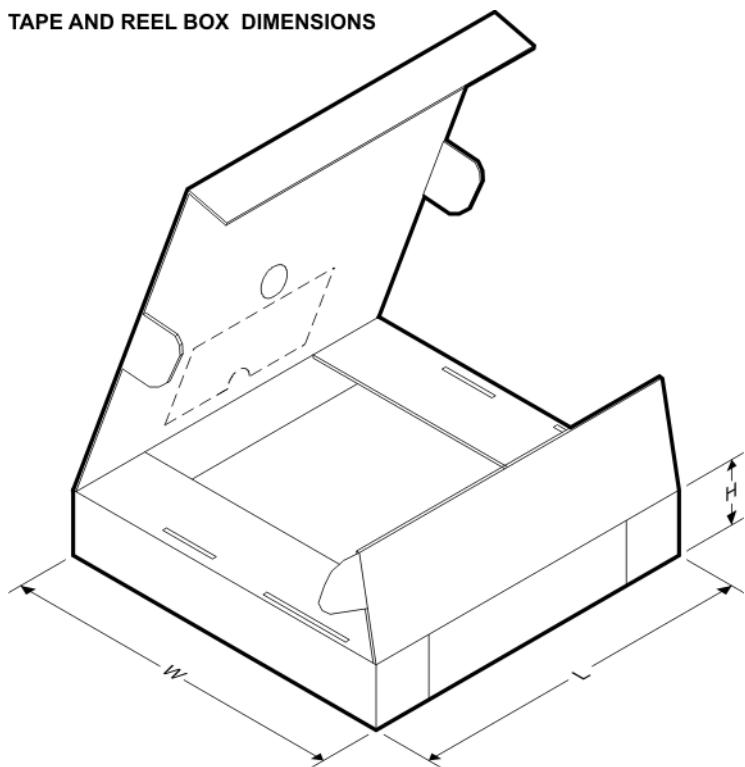
**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


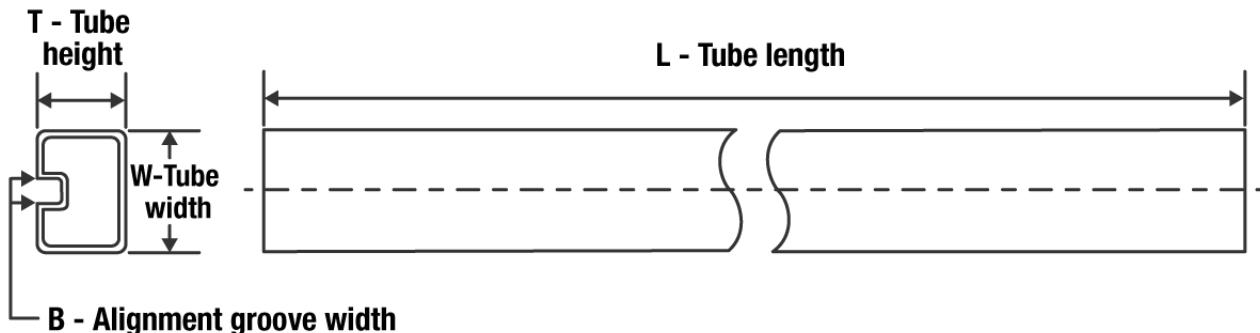
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV341IDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
LMV341IDCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
LMV342IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV342IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMV344IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMV344IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV341IDBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
LMV341IDCKR	SC70	DCK	6	3000	202.0	201.0	28.0
LMV342IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
LMV342IDR	SOIC	D	8	2500	340.5	336.1	25.0
LMV344IDR	SOIC	D	14	2500	853.0	449.0	35.0
LMV344IPWR	TSSOP	PW	14	2000	853.0	449.0	35.0

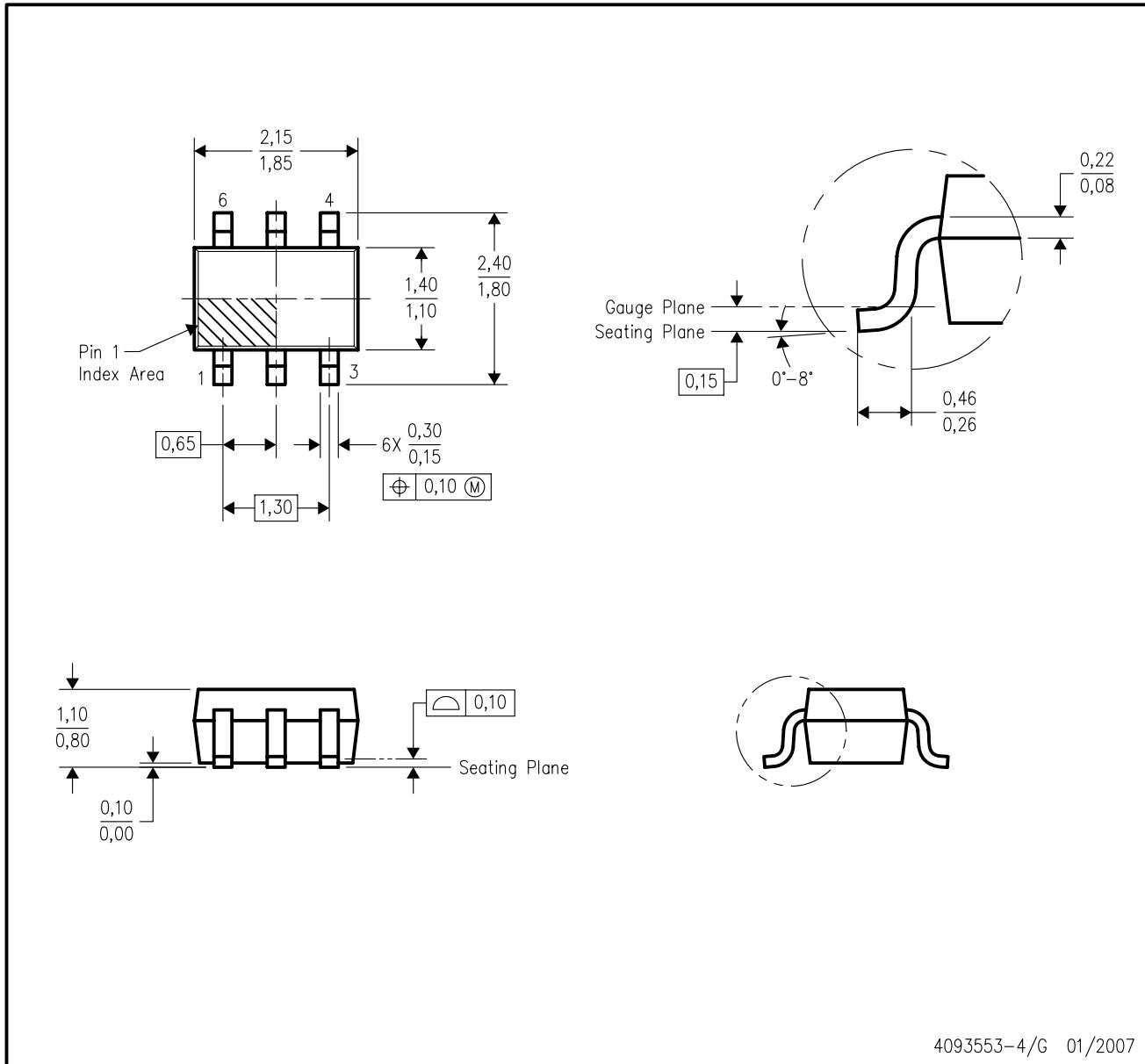
**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T ( $\mu$ m)	B (mm)
LMV342ID	D	SOIC	8	75	507	8	3940	4.32
LMV344ID	D	SOIC	14	50	506.6	8	3940	4.32
LMV344IDG4	D	SOIC	14	50	506.6	8	3940	4.32
LMV344IPW	PW	TSSOP	14	90	530	10.2	3600	3.5
LMV344IPWG4	PW	TSSOP	14	90	530	10.2	3600	3.5

## DCK (R-PDSO-G6)

## PLASTIC SMALL-OUTLINE PACKAGE



4093553-4/G 01/2007

NOTES:

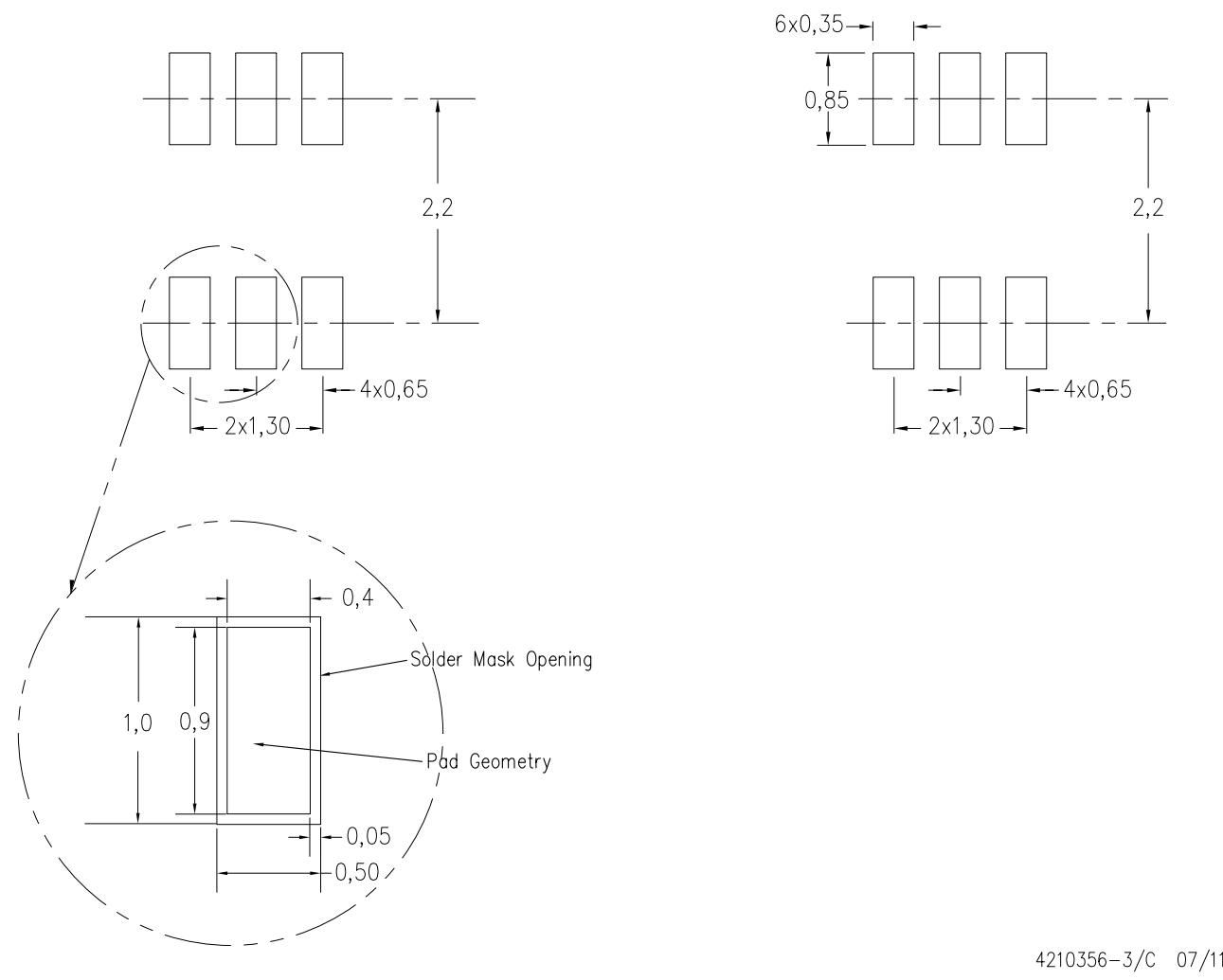
- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Falls within JEDEC MO-203 variation AB.

DCK (R-PDSO-G6)

PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings  
Based on a stencil thickness  
of .127mm (.005inch).

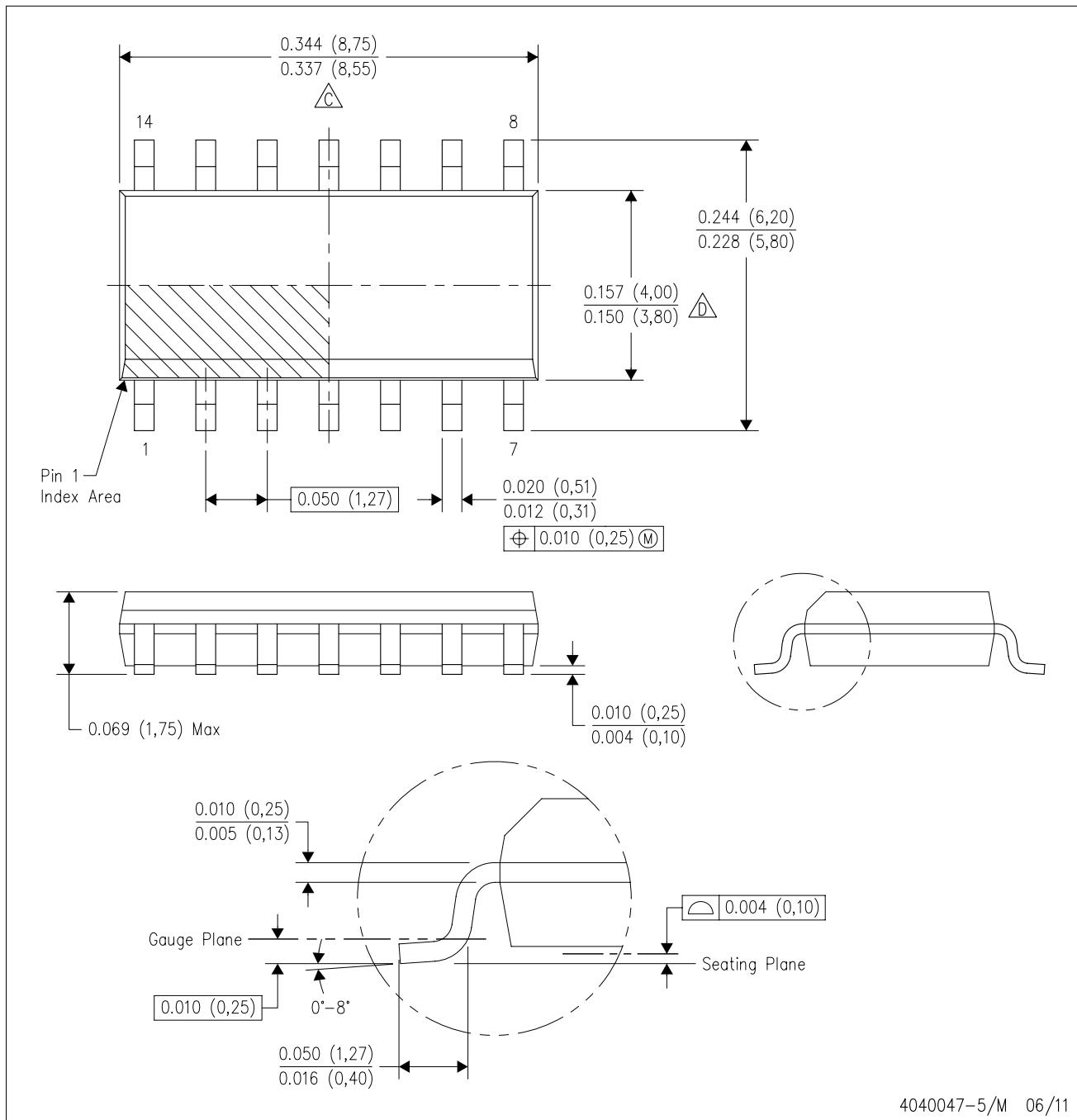


NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

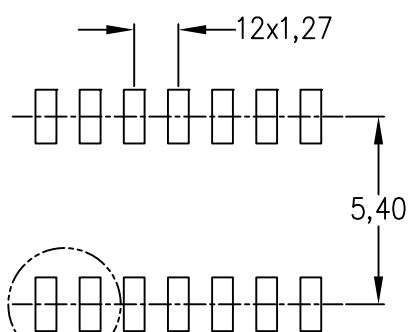
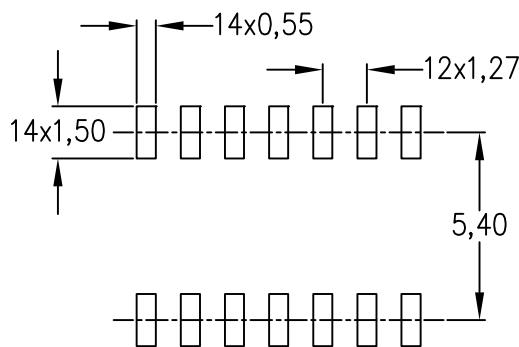
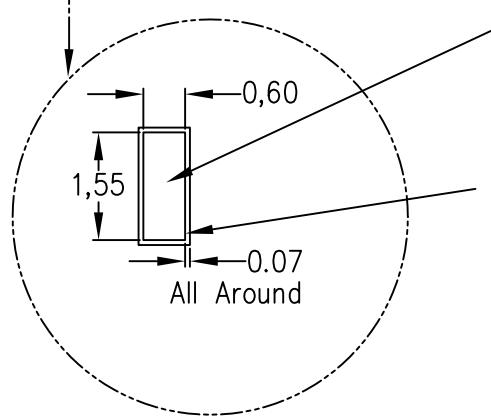
△C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

△D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)Example  
Non Soldermask Defined PadExample  
Pad Geometry  
(See Note C)Example  
Solder Mask Opening  
(See Note E)

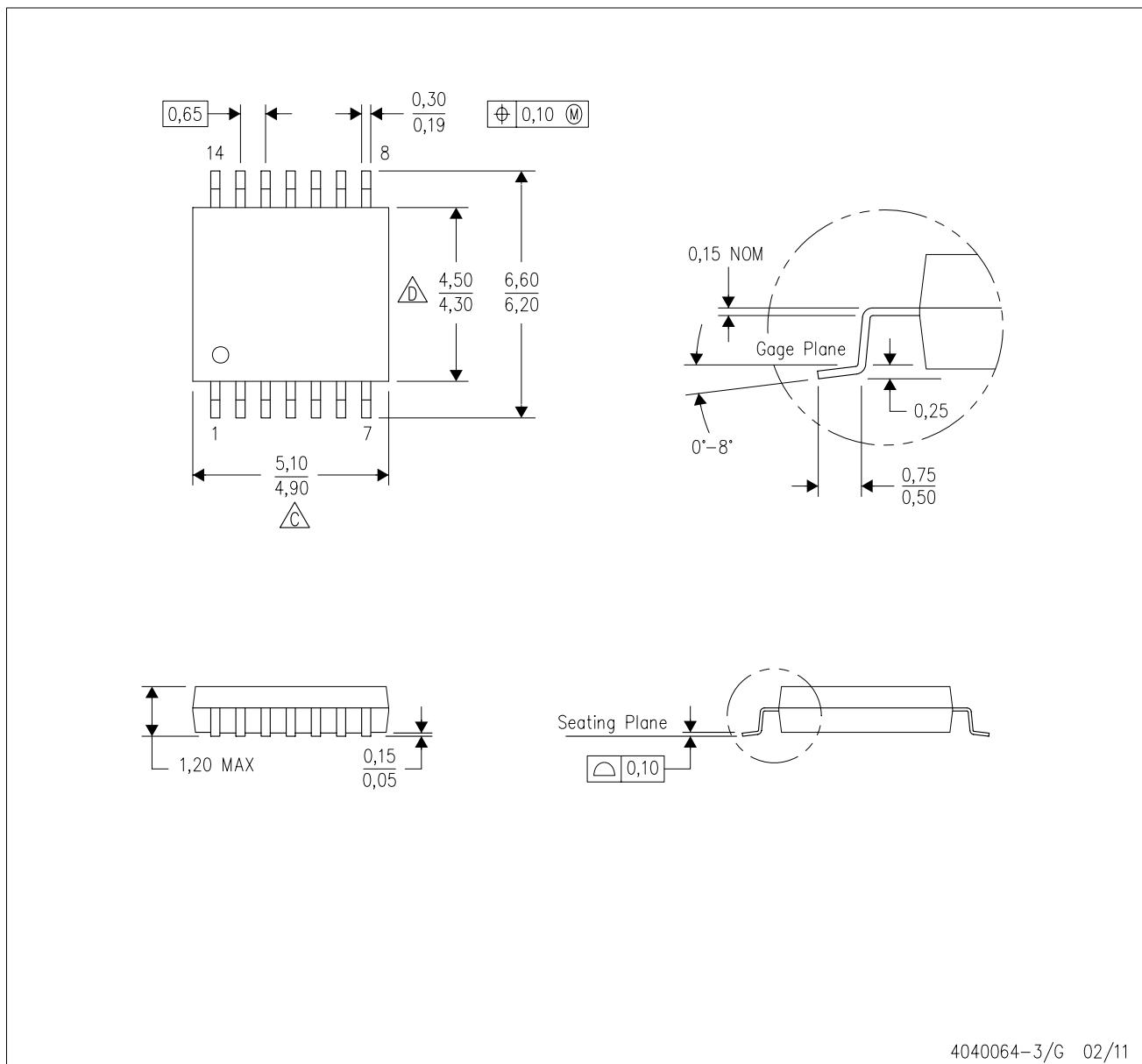
4211283-3/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

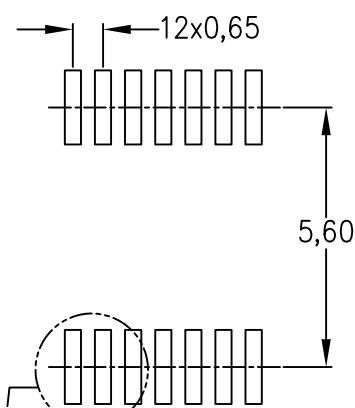
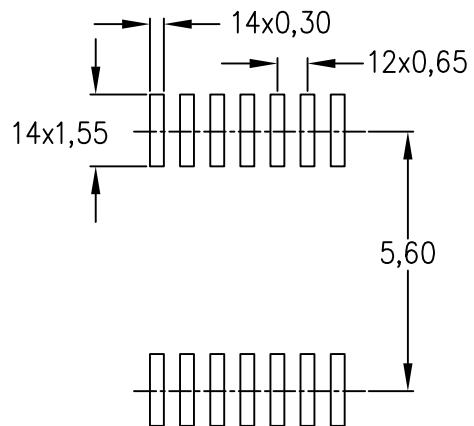
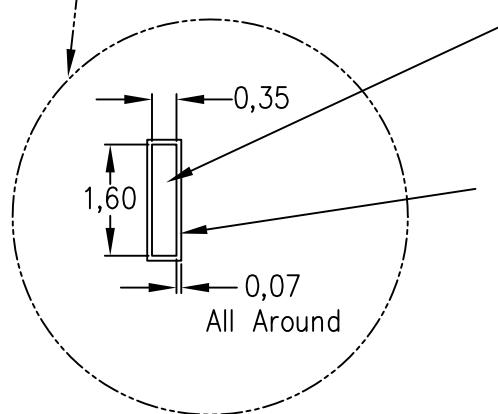
 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

 D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)Example  
Non Soldermask Defined PadExample  
Pad Geometry  
(See Note C)Example  
Solder Mask Opening  
(See Note E)

4211284-2/G 08/15

## NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

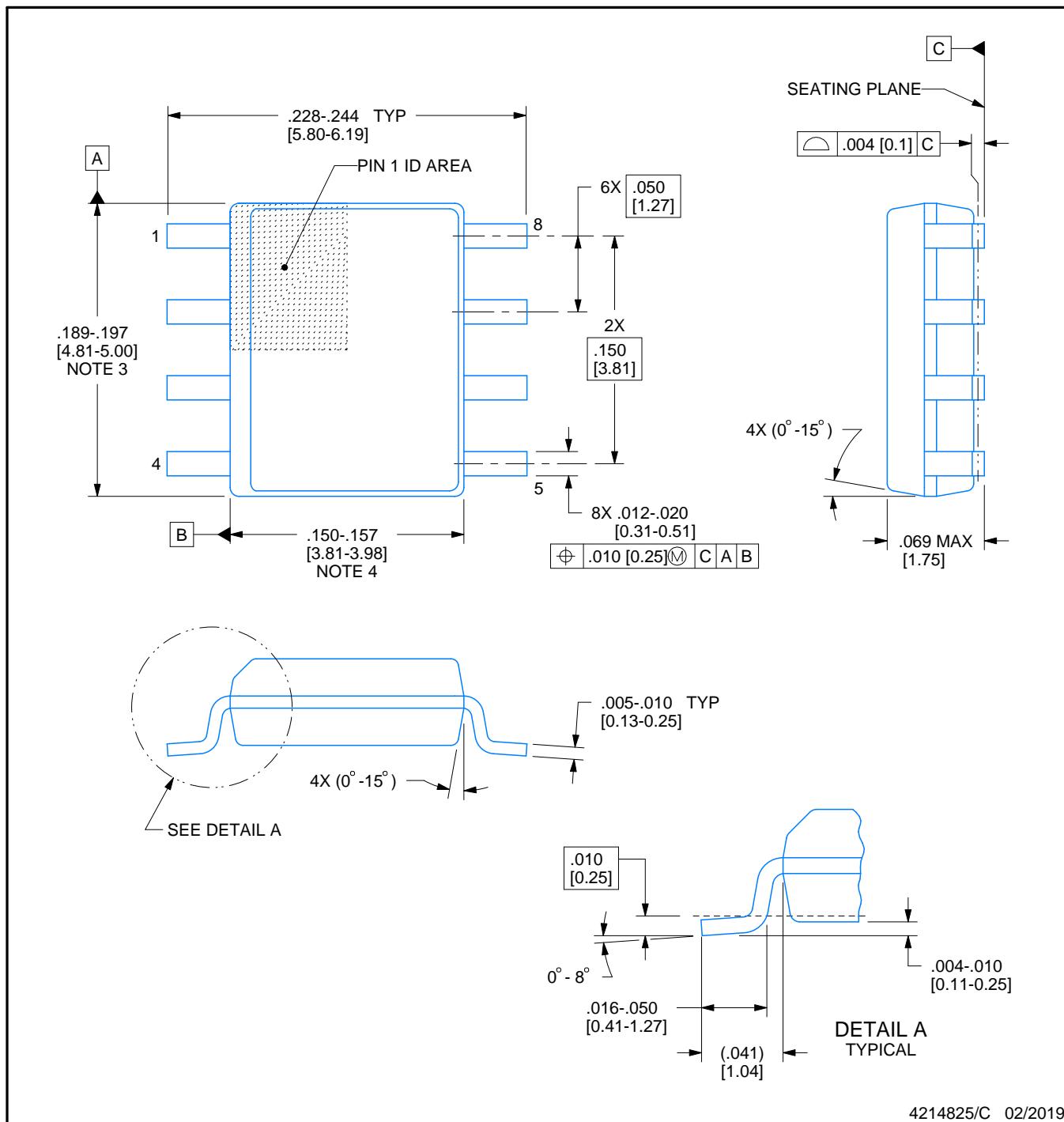


# PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



## NOTES:

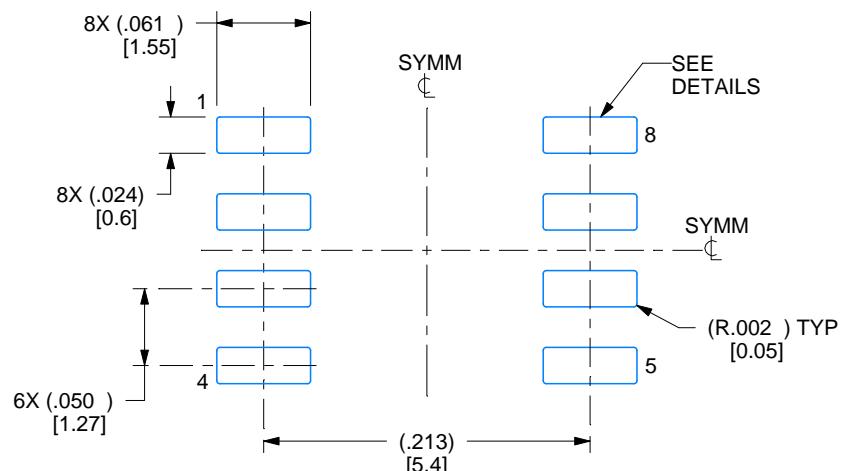
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

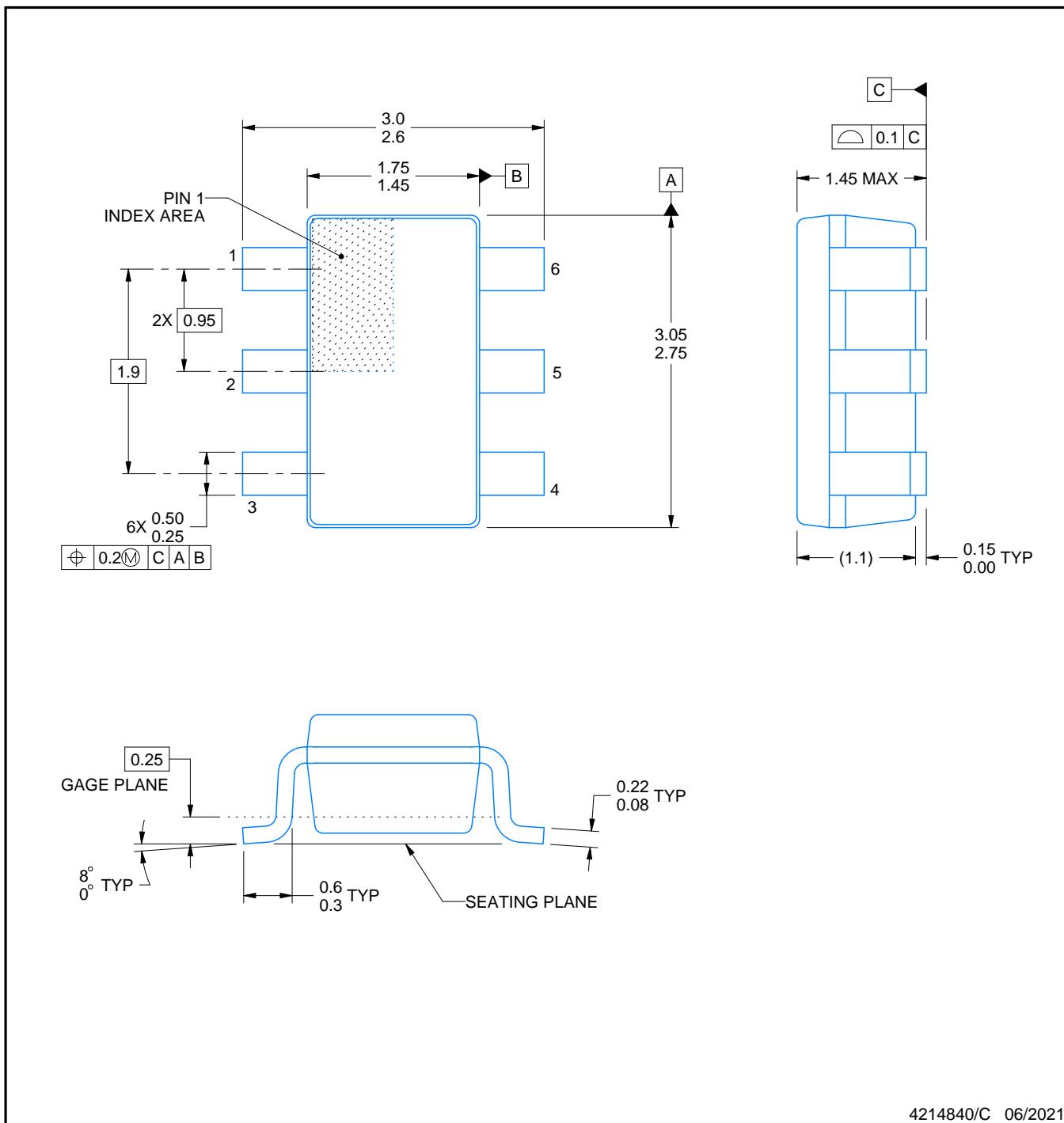
# PACKAGE OUTLINE

DBV0006A



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

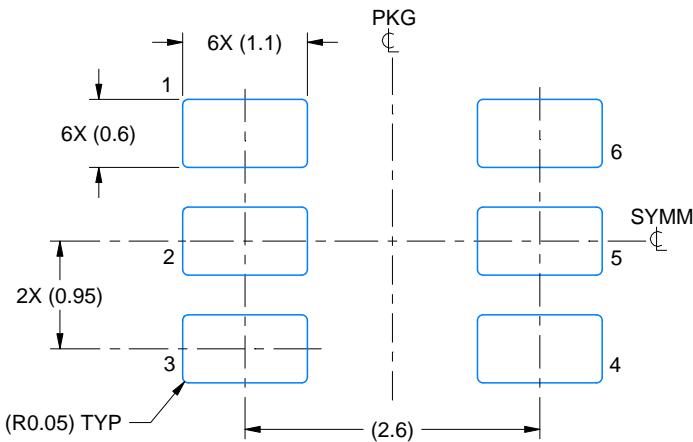
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

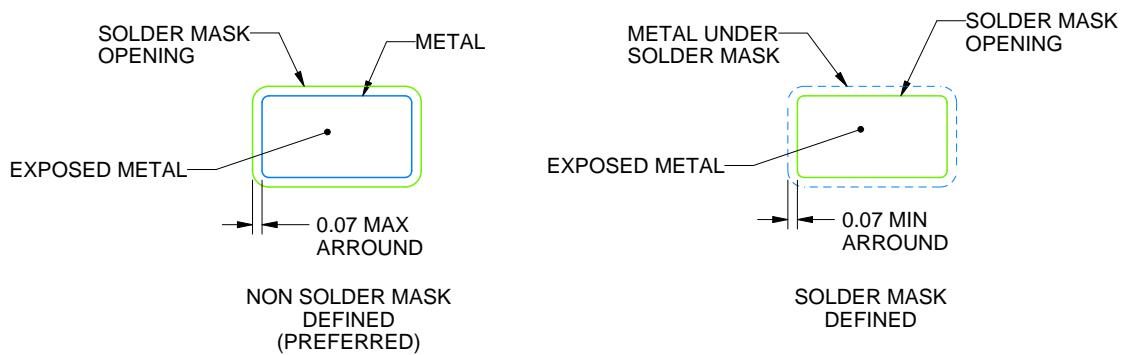
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214840/C 06/2021

NOTES: (continued)

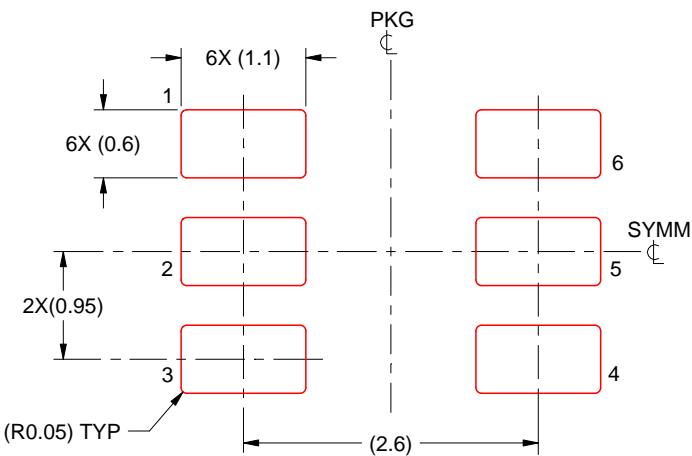
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

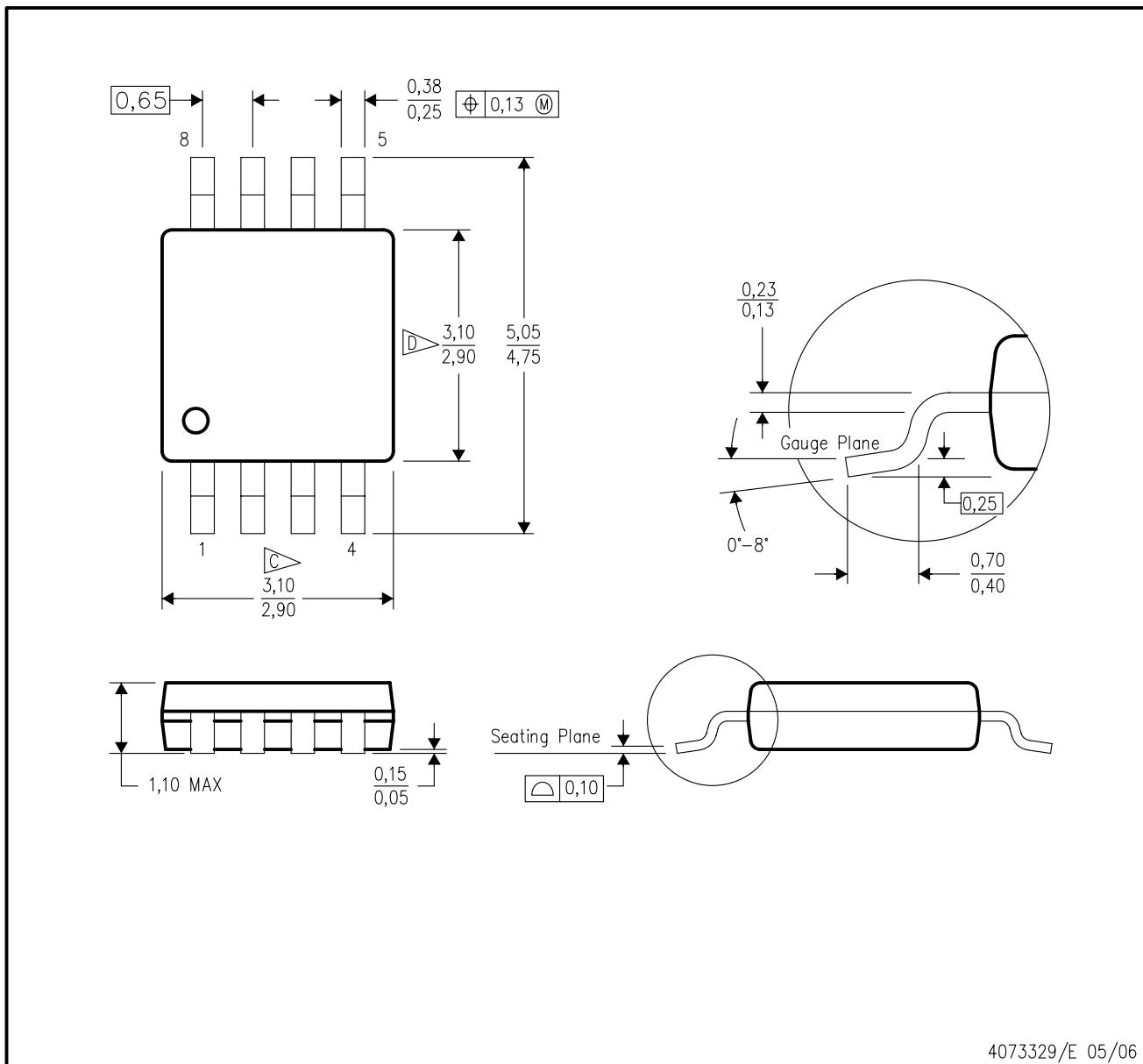
4214840/C 06/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## DGK (S-PDSO-G8)

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

 C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 per end.

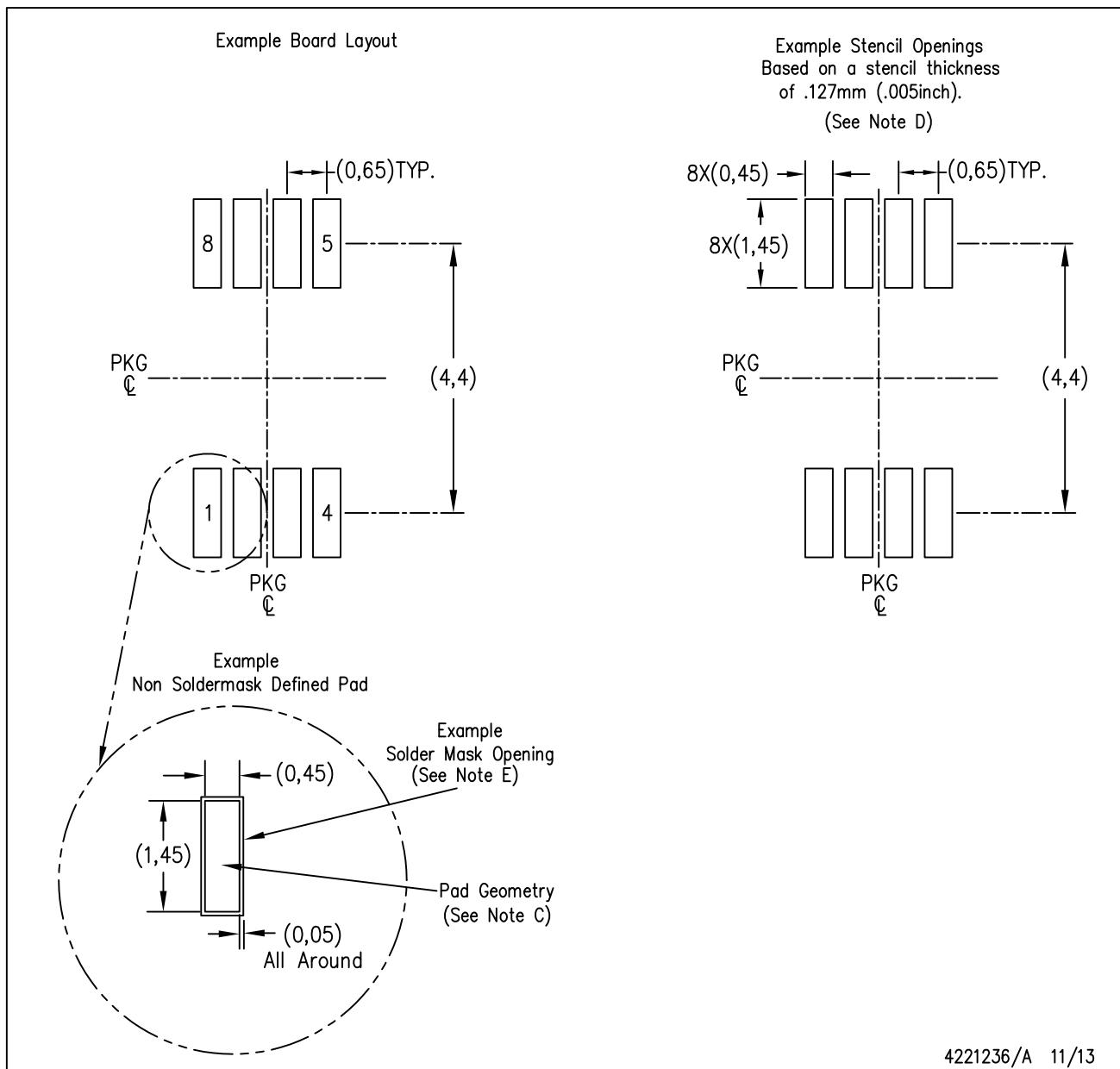
 D Body width does not include interlead flash. Interlead flash shall not exceed 0,50 per side.

E. Falls within JEDEC MO-187 variation AA, except interlead flash.

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DGK (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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