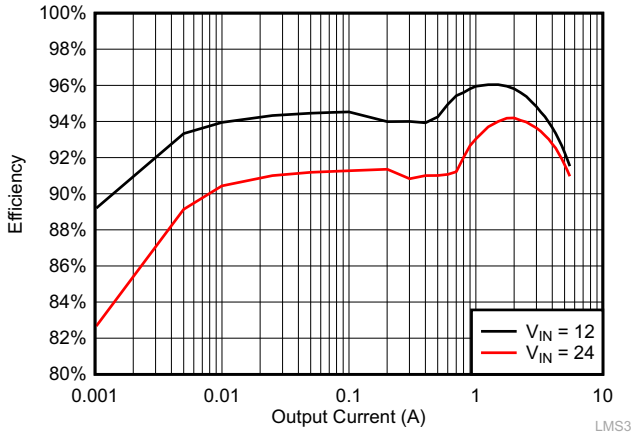
LMS3635-Q1 3.5A、LMS3655-Q1 5.5A、36V 同步、400kHz 降压转换器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 器件温度等级 1：–40°C 至 +125°C 的工作环境温度范围
  - 器件 HBM 分类等级 2
  - 器件 CDM 分类等级 C6
- 在将 12V 转换为 5V 时具有 96% 的峰值效率
- 低 EMI 和超低的开关节点振铃
- 400kHz (±10%) 固定开关频率
- 具有 –40°C 至 +150°C 的结温范围
- 外部频率同步
- 具有内部滤波器和 3ms 释放计时器的 $\overline{\text{RESET}}$ 输出
- 可提高效率的自动轻负载模式
- 引脚可选强制 PWM 模式
- 内置补偿、软启动、电流限制、热关断和 UVLO
- 25°C 时在 3.5A 负载下具有 0.35V 压降（典型值）
- 18μA I_{Q_VIN}：在 3.3 V_{OUT} 且无负载情况下的静态电流（典型值）
- 输出电压：5V、3.3V 和 ADJ（1V 至 20V）
- ±1.5% 基准电压容差
- 使用 LMS3655-Q1 并借助 WEBENCH® Power Designer 创建定制设计方案

2 应用

- 汽车 USB 充电
- 驾驶员监控
- 环视系统 ECU
- 机械扫描激光雷达
- 车辆对车辆



LMS3655-Q1 效率：V_{OUT} = 5V

3 说明

LMS3635-Q1 和 LMS3655-Q1 同步降压稳压器针对高性能应用进行了优化，可提供 3.3V 或 5V 的输出电压或 1V 至 20V 的可调节输出。PWM 和 PFM 模式之间的无缝转换以及低静态电流可确保在所有负载下实现高效率和出色的瞬态响应。

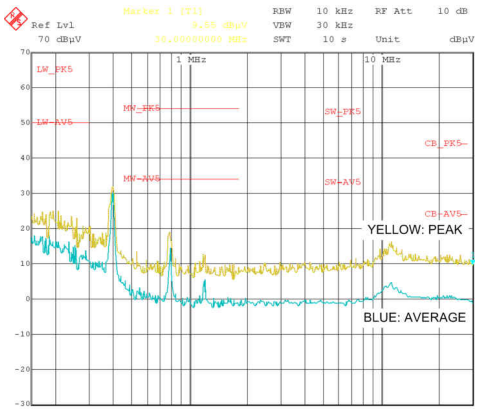
高级高速电路支持 LMS3655-Q1 将 24V 的输入调节至 3.3V 的输出（400kHz 固定频率），同时还支持 5.5A 的持续负载电流。创新的频率折返架构允许该器件通过仅 3.5V 的输入电压调节生成 3.3V 的输出。输入电压范围可高达 36V，瞬态容差高达 42V，有助于轻松实现输入浪涌保护设计。

开漏复位输出具有内置的滤波和延迟功能，可提供正确的系统状态指示。凭借这一特性，器件无需使用附加监控元件，这节省了成本和电路板空间。

器件信息

器件名称	封装(1)	封装尺寸
LMS3635-Q1	SON (22)	4.00mm × 5.00mm
LMS3655-Q1		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



LMS3655-Q1 传导 EMI：$V_{OUT\ =\ 5V}$，I_{OUT} = 5A

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (March 2018) to Revision C (August 2021) — **Page**

- 添加了 WEBENCH 链接和章节 1
- 更新了应用 1
- 更新了整个文档中的表格、图和交叉参考的编号格式 1
- 添加了非可湿性侧面选项 1

Changes from Revision A (September 2017) to Revision B (March 2018) — **Page**

- 已将最大可调节输出电压从：15V 更改为：20V 1
- Changed maximum extended output adjustment from: 15 V to: 20 V 5
- Added new extended output adjustment tablenote to the *Recommended Operating Conditions* 5

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5 Device Comparison Tables

表 5-1. LMS3635-Q1 Devices (3.5-A Output)

PART NUMBER	OUTPUT VOLTAGE	SPREAD SPECTRUM	PACKAGE QTY	WETTABLE FLANKS
LMS3635AQRNLRQ1	Adjustable	No	3000	Y
LMS3635AQRNLTQ1	Adjustable	No	250	Y
LMS36353QRNLRQ1	3.3 V	No	3000	Y
LMS36353QRNLTQ1	3.3 V	No	250	Y
LMS36355QRNLRQ1	5 V	No	3000	Y
LMS36355QRNLTQ1	5 V	No	250	Y
LMS3635MQRNLRQ1	Adjustable	Yes	3000	Y
LMS3635MQRNLTQ1	Adjustable	Yes	250	Y
LMS3635NQRNLRQ1	3.3 V	Yes	3000	Y
LMS3635NQRNLTQ1	3.3 V	Yes	250	Y
LMS3635LQRNLRQ1	5 V	Yes	3000	Y
LMS3635LQRNLTQ1	5 V	Yes	250	Y
LMS3635MQURNLRQ1	Adjustable	Yes	3000	N
LMS3635LQURNLRQ1	5V	Yes	3000	N

表 5-2. LMS3655-Q1 Devices (5.5-A Output)

PART NUMBER	OUTPUT VOLTAGE	SPREAD SPECTRUM	PACKAGE QTY	WETTABLE FLANK
LMS3655AQRNLRQ1	Adjustable	No	3000	Y
LMS3655AQRNLTQ1	Adjustable	No	250	Y
LMS36553QRNLRQ1	3.3 V	No	3000	Y
LMS36553QRNLTQ1	3.3 V	No	250	Y
LMS36555QRNLRQ1	5 V	No	3000	Y
LMS36555QRNLTQ1	5 V	No	250	Y
LMS3655MQRNLRQ1	Adjustable	Yes	3000	Y
LMS3655MQRNLTQ1	Adjustable	Yes	250	Y
LMS3655NQRNLRQ1	3.3 V	Yes	3000	Y
LMS3655NQRNLTQ1	3.3 V	Yes	250	Y
LMS3655LQRNLRQ1	5 V	Yes	3000	Y
LMS3655LQRNLTQ1	5 V	Yes	250	Y
LMS3655MQURNLRQ1	Adjustable	Yes	3000	N
LMS3655NQURNLRQ1	3.3	Yes	3000	N

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6 Pin Configuration and Functions

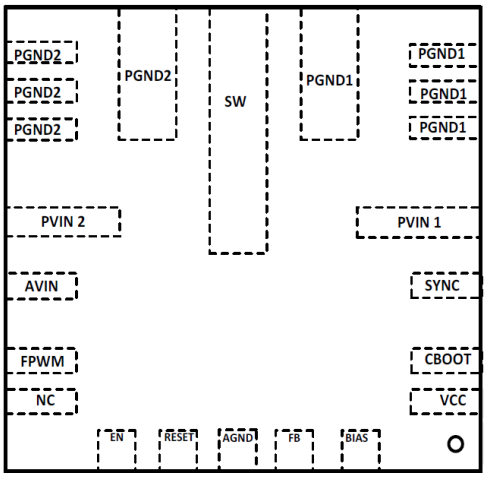

图 6-1. RNL Package 22-Pin VQFN Top View

表 6-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	VCC	A	Internal 3.1-V LDO output. Used as supply to internal control circuits. Connect a high-quality 4.7-µF capacitor from this pin to AGND.
2	CBOOT	P	Bootstrap capacitor connection for gate drivers. Connect a high quality 470-nF capacitor from this pin to the SW pin.
3	SYNC	I	Synchronization input to regulator. Used to synchronize the device switching frequency to a system clock. Triggers on rising edge of external clock; frequency must be in the range of 250 kHz and 500 kHz.
4	PVIN1	P	Input supply to regulator. Connect input bypass capacitors directly to this pin and PGND pins. Connect PVIN1 and PVIN2 pins directly together at PCB.
5	PGND1	G	Power ground to internal low-side MOSFET. These pins must be tied together on the PCB. Connect PGND1 and PGND2 directly together at PCB. Connect to AGND and system ground.
6			
7			
8			
9	SW	P	Regulator switch node. Connect to power inductor.
10	PGND2	G	Power ground to internal low-side MOSFET. These pins must be tied together. Connect PGND1 and PGND2 directly together at PCB. Connect to AGND and system ground.
11			
12			
13			
14	PVIN2	P	Input supply to regulator. Connect input bypass capacitors directly to this pin and PGND pins. Connect PVIN1 and PVIN2 pins directly together at PCB.
15	AVIN	A	Analog VIN. Connect to PVIN1 and PVIN2 on PCB.
16	FPWM	I	Mode control input of regulator. High = FPWM, low = Automatic light load mode. Do not float.
1 7	NC	—	No internal connection.
18	EN	I	Enable input to regulator. High = on, Low = off. Can be connected to VIN. Do not float.
19	$\overline{\text{RESET}}$	O	Open-drain reset output flag. Connect to suitable voltage supply through a current limiting resistor. High = regulator OK, Low = regulator fault. Goes low when EN = low.
20	AGND	G	Analog ground for regulator and system. All electrical parameters are measured with respect to this pin. Connect to PGND on PCB.
21	FB	A	Feedback input to regulator. Connect to output voltage node for fixed VOUT options. Connect to feedback voltage divider for adjustable option.
22	BIAS	P	Input to auxiliary bias regulator. Connect to output voltage node.

(1) A = Analog, O = Output, I = Input, G = Ground, P = Power

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7 Specifications

7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to +150°C (unless otherwise noted). (1)

PARAMETER	MIN	MAX	UNIT
VIN (AVIN, PVIN1, and PVIN2) to AGND, PGND(2)	–0.3	40	V
SW to AGND, PGND(3)	–0.3	V_{IN} + 0.3	V
CBOOT to SW	–0.3	3.6	V
EN to AGND, PGND(2)	–0.3	40	V
BIAS to AGND, PGND	–0.3	16	V
FB to AGND, PGND: Fixed 3.3-V Output, Fixed 5-V Output	–0.3	16	V
FB to AGND, PGND: Adjustable Output	–0.3	16	V
$\overline{\text{RESET}}$ to AGND, PGND	–0.3	8	V
$\overline{\text{RESET}}$ sink current(4)		10	mA
SYNC to AGND, PGND(2)	–0.3	40	V
FPWM to AGND, PGND(2)	–0.3	40	V
VCC to AGND, PGND	–0.3	3.6	V
Junction temperature	–40	150	°C
Storage temperature, T_{stg}	–40	150	°C

(1) Stresses beyond those listed under 节 7.1 may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under 节 7.3 are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) A maximum of 42 V can be sustained at this pin for a duration of ≤ 500 ms at a duty cycle of ≤ 0.01%.
(3) A voltage of 2 V below PGND and 2 V above VIN can appear on this pin for ≤ 200 ns with a duty cycle of ≤ 0.01%.
(4) Do not exceed the voltage rating on this pin.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2500	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to +150°C (unless otherwise noted).

	MIN	NOM	MAX	UNIT
Input voltage after start-up(1)	3.9		36	V
Output voltage for 3.3-V LMS36x5-Q1(2)			3.3	V
Output voltage for 5-V LMS36x5-Q1(2)			5	V
Output adjustment for adjustable version of LMS36x5-Q1 (2)	3.3		6	V
Extended output adjustment for adjustable version of LMS36x5-Q1 (3) (4)	1		20	V
Load current for LMS3635-Q1, fixed output option and adjustable			3.5	A
Load current for LMS3655-Q1 , fixed output option and adjustable			5.5	A
Operating ambient temperature(5)	–40		125	°C

(1) An extended input voltage range to 3.5 V is possible; see 节 7.7 table. See *Input UVLO* for start-up conditions.
(2) The output voltage must not be allowed to fall below zero volts during normal operation.
(3) Operation below 3.3 V and above 6 V may require changes to the typical application schematic, operation may not be possible over the full input voltage range, and some system specifications will not be achieved for this extended output voltage range. Consult the factory for further information.

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(4) Operation above 15 V requires the BIAS pin grounded or powered by an external source. A maximum of 16 V can be sustained on the BIAS pin.
(5) High junction temperatures degrade operating lifetime.

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7.4 Thermal Information

THERMAL METRIC[1]		LMS36x5-Q1 RNL (VQFN) 22 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.5	°C/W
$R_{\theta JC}$	Junction-to-case (top) thermal resistance	16.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Thermal Information (for Device Mounted on PCB)

THERMAL METRIC[1]		LMS36x5-Q1 RNL (VQFN) 22 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.4	°C/W
$R_{\theta JC}$	Junction-to-case (top) thermal resistance	14.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.4	°C/W

(1) Mounted on a thermally optimized FR4 four layer EVM with a size of 4000 mill × 3000 mill.

7.6 Electrical Characteristics

Limits apply over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise noted. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB}	Initial reference voltage for 5-V and 3.3-V options	V_{IN} = 3.8 V to 36 V, T_J = 25°C	–1%		1%	
		V_{IN} = 3.8 V to 36 V	–1.5%		1.5%	
I_Q	Operating quiescent current; measured at VIN pin when enabled and not switching[1]	V_{IN} = 13.5 V, V_{BIAS} = 5 V		7.5	16	µA
I_{B_NSW}	Bias current into BIAS pin, enabled, not switching	V_{IN} = 13.5 V, V_{BIAS} = 5 V, FPWM = 0 V		53	62	µA
		V_{IN} = 13.5 V, V_{BIAS} = 3.3 V, FPWM = 0 V		53	62	
I_{SD}	Shutdown quiescent current; measured at VIN pin	EN ⩽ 0.4 V		2	3	µA
$V_{IN-OPERATE}$	Minimum input voltage to operate	Rising	3.2	3.55	3.90	V
		Falling	2.95	3.25	3.55	
		Hysteresis	0.28	0.3	0.4	

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Limits apply over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise noted. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RESET}	$\overline{RESET}$ upper threshold voltage	Rising, % of V_{OUT}	105%	107%	110%	
	$\overline{RESET}$ lower threshold voltage	Falling, % V_{OUT}	92%	94%	96.5%	
	Magnitude of $\overline{RESET}$ lower threshold from steady state output voltage	Steady-state output voltage and $\overline{RESET}$ falling threshold read at the same T_J and V_{IN}			96%	
V_{RESET_HYST}	$\overline{RESET}$ hysteresis as a percent of output voltage setpoint			±1%		
V_{RESET_VALID}	Minimum input voltage for proper $\overline{RESET}$ function	50-µA pullup to $\overline{RESET}$ pin, EN = 0 V, T_J= 25°C			1.5	V
V_{OL}	Low level $\overline{RESET}$ function output voltage	50-µA pullup to $\overline{RESET}$ pin, V_{IN} = 1.5 V, EN = 0 V			0.4	V
		0.5-mA pullup to $\overline{RESET}$ pin, V_{IN} = 13.5 V, EN = 0 V			0.4	
		1-mA pullup to $\overline{RESET}$ pin, V_{IN} = 13.5 V, EN = 3.3 V			0.4	
F_{SW}	Switching frequency	V_{IN} = 13.5 V, center frequency with spread spectrum, PWM operation	360	400	440	kHz
		V_{IN} = 13.5 V, without spread spectrum, PWM operation	360	400	440	
F_{SYNC}	Sync frequency range		250	400	500	kHz
D_{SYNC}	Sync input duty cycle range	High state input < 5.5 V and > 2.3 V	25%		75%	
V_{FPWM}	FPWM input threshold voltage	FPWM input high (MODE = FPWM)	1.5			V
		FPWM input low (MODE = AUTO with diode emulation)			0.4	
		FPWM input hysteresis	0.15		1	
FS_{SS}	Frequency span of spread spectrum operation			±3%		
F_{PSS}	Spread-spectrum pattern frequency(2)				1.2	Hz
I_{FPWM}	FPWM leakage current	V_{IN} = 13.5 V, V_{FPWM} = 3.3 V		1		µA
		V_{IN} = V_{FPWM} = 13.5 V		1		
I_{SYNC}	SYNC leakage current	V_{IN} = 13.5 V, V_{SYNC} = 3.3 V		1		µA
		V_{IN} = V_{SYNC} = 13.5 V		1		
$I_{L\text{-}HS}$	High-side switch current limit	LMS3635-Q1	4.5	6	7.5	A
		LMS3655-Q1	6.7	8.5	9.5	
$I_{L\text{-}LS}$	Low-side switch current limit	LMS3635-Q1	4	4.5	6.5	A
		LMS3655-Q1	6	7	7.5	
$I_{L\text{-}ZC}$	Zero-cross current limit FPWM = low			–0.02		A
$I_{L\text{-}NEG}$	Negative current limit FPWM = high			–1.5		
R_{DSON}	Power switch on-resistance	High-side MOSFET R_{DSON}, V_{IN} = 13 V, IL = 1 A		60	130	mΩ
		Low-side MOSFET R_{DSON}, V_{IN} = 13 V, IL = 1 A		40	80	
V_{EN}	Enable input threshold voltage - rising	Enable rising	1.7		2	V
V_{EN_HYST}	Enable threshold hysteresis		0.45		0.55	V

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Limits apply over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise noted. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{EN_WAKE}	Enable wake-up threshold		0.4			V
I_{EN}	EN pin input current	V_{IN} = V_{EN} = 13.5 V		2	3	µA
V_{CC}	Internal V_{CC} voltage	V_{IN} = 13.5 V, V_{BIAS} = 0 V		3.05		V
		V_{IN} = 13.5 V, V_{BIAS} = 3.3 V		3.15		
V_{CC_UVLO}	Internal V_{CC} input undervoltage lockout	V_{IN} rising		2.7		V
		Hysteresis below $V_{CC-UVLO}$		185		mV
I_{FB}	Input current from FB to AGND	Adjustable LMS36x5-Q1, FB = 1 V		20		nA
V_{REF}	Reference voltage for adjustable option only	T_J = 25°C	0.993	1	1.007	V
		T_J = –40°C to 125°C	0.99	1	1.01	
R_{RESET}	R_{DSON} of $\overline{RESET}$output	Pull FB pin low. Sink 1-mA at RESET pin		50	120	Ω
V_{SYNC}	V_{IH}		1.5			V
	V_{IL}				0.4	
	V_{HYST}		0.15		1	
T_{SD}	Thermal shutdown thresholds(2)	Rising	160		185	°C
		Hysteresis		15		
D_{MAX}	Maximum switch duty cycle	F_{sw} = 400 kHz		96%		
		While in dropout(2)	98%			

(1) This is the current used by the device while not switching, open loop on the ATE. It does not represent the total input current from the regulator system.
(2) Ensured by Design, Not tested at production.

7.7 System Characteristics

The following specifications are ensured by design provided that the component values in the typical application circuit are used. These parameters are not ensured by production testing. Limits apply over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise noted. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN-MIN}	Minimum input voltage for full functionality at 3.5-A load, after start-up.	V_{OUT} = 3.3 V +2% or –3% regulation		3.5		V
	Minimum input voltage for full functionality at maximum rated load 5.5 A after start-up.	V_{OUT} = 3.3 V +2% or –3% regulation		3.8		
V_{OUT}	Output voltage for 5-V option	V_{IN} = 5.6 V to 36 V, I_{OUT} = 3.5 A	4.925	5	5.08	V
	Output voltage for 3.3-V option	V_{IN} = 3.9 V to 36 V, I_{OUT} = 3.5 A	3.24	3.3	3.35	
	Output voltage for 5-V option	V_{IN} = 5.5 V to 36 V, I_{OUT} = 100 µA to 100 mA	4.92	5.05	5.125	
	Output voltage for 3.3-V option	V_{IN} = 3.8 V to 36 V, I_{OUT} = 100 µA to 100 mA	3.24	3.33	3.38	
	Output voltage for adjustable option	V_{IN} = V_{OUT} + 1 V to 36 V, I_{OUT} = 3.5 A	–2.25		2.25	%
F_{SW}	Switching frequency	V_{IN} = 24 V, FPWM = 24V, V_{OUT} = 3.3 V, I_{OUT} = 200 mA		400		kHz
I_{Q_VIN}	Input current to VIN pin	V_{IN} = 13.5 V, V_{OUT} = 3.3 V, I_{OUT} = 0 A, FPWM = 0		18		µA
		V_{IN} = 13.5 V, V_{OUT} = 5 V, I_{OUT} = 0 A, FPWM = 0		24		
I_B	Bias current in AUTO mode at no load	V_{IN} = 13.5 V, I_{OUT} = 0 A, FPWM = 0		32	42	µA

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The following specifications are ensured by design provided that the component values in the typical application circuit are used. These parameters are not ensured by production testing. Limits apply over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise noted. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DROP1}	Minimum input to output voltage differential to maintain regulation accuracy without inductor DCR drop	V_{OUT} = 3.3 V or 5 V, I_{OUT}= 3.5 A, +2% or –3% output accuracy		0.35	0.6	V
		V_{OUT} = 3.3 V or 5 V, I_{OUT}= 5.5 A, +2% or –3% output accuracy		0.65	0.85	V
V_{DROP2}	Minimum input to output voltage differential to maintain F_{SW} ⩾ 330 kHz without inductor DCR drop	V_{OUT} = 3.3 V or 5 V, I_{OUT} = 3.5 A, F_{SW} = 330 kHz, 2% regulation accuracy		0.5	0.7	V
		V_{OUT} = 3.3 V or 5 V, I_{OUT} = 5.5 A, F_{SW} = 330 kHz, 2% regulation accuracy		0.7	1.2	V
Efficiency	Typical efficiency	V_{IN} = 13.5 V, V_{OUT} = 5 V, I_{OUT} = 3.5 A		94%		
		V_{IN} = 13.5 V, V_{OUT} = 3.3 V, I_{OUT} = 3.5 A		92%		
		V_{IN} = 13.5 V, V_{OUT} = 5 V, I_{OUT} = 100 mA		92%		

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7.8 Timing Requirements

Limits apply over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise noted. Minimum and maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5 V.

		MIN	NOM	MAX	UNIT
t_{ON}	Minimum switch on-time, V_{IN} = 18 V, I_L = 1 A		60	84	ns
t_{OFF}	Minimum switch off-time, V_{IN} = 3.8 V, I_L = 1 A		65	80	ns
$t_{RESET\text{-}act}$	Delay time to $\overline{RESET}$ high signal	2	3	4	ms
$t_{RESET\text{-}filter}$	Glitch filter time for $\overline{RESET}$ function(1)		24		µs
t_{SS}	Soft-start time from first switching pulse to V_{REF} at 90%	2.5	4	5	ms
t_{EN}	Turnon delay, C_{VCC} = 4.7 µF(2)		0.8		ms
t_W	Short-circuit wait time (*hiccup* time)(3)		6		ms
t_{FPWM}	Change transition time from AUTO to FPWM MODE, 10-mA load, V_{IN} = 13.5 V		250		µs
	Change transition time from FPWM to AUTO MODE, 10-mA load, V_{IN} = 13.5 V		450		

(1) See 节 8.
(2) This is the time from the rising edge of EN to the time that the soft-start ramp begins.
(3) T_w is the wait time between current limit trip and restart. T_w is proportional to the soft-start time. However, provision must be made to make T_w longer to ensure survivability during an output short circuit.

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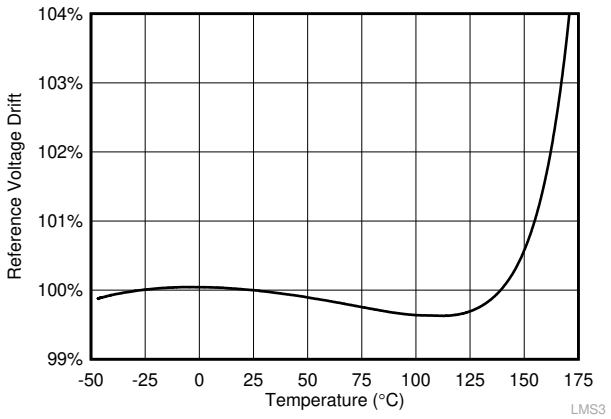
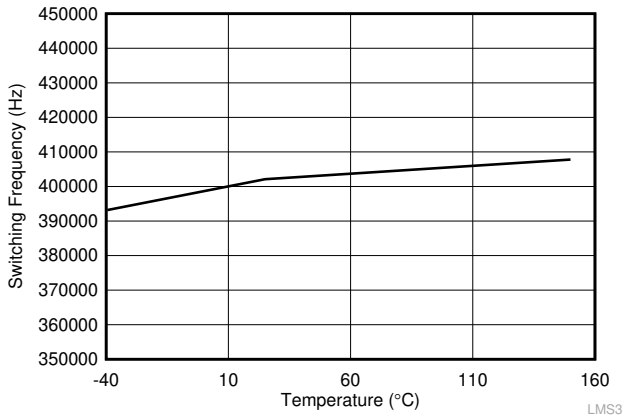
7.9 Typical Characteristics

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, T_A = 25°C. Specified temperatures are ambient.



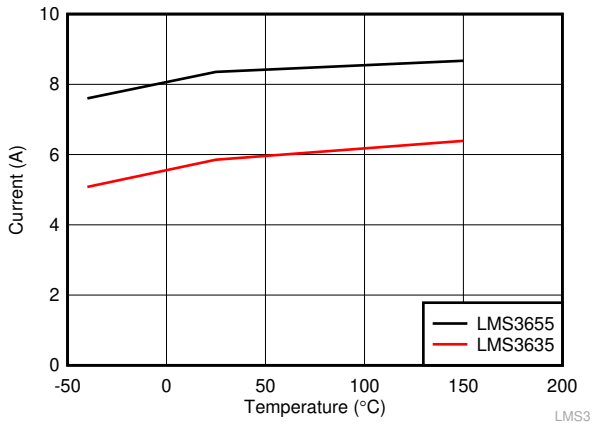
V_{IN} = 12 V

图 7-1. Reference Voltage Drift



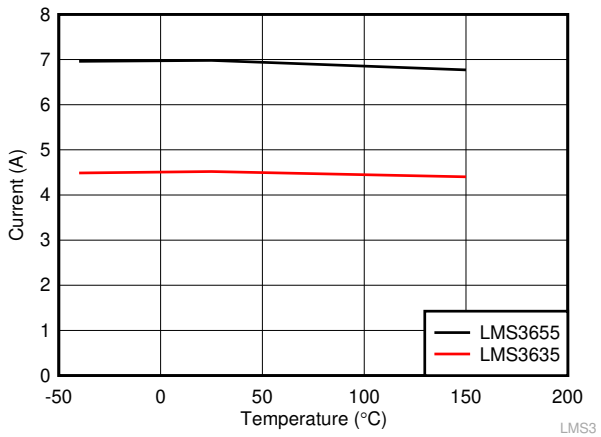
V_{IN} = 12 V

图 7-2. Switching Frequency vs Temperature



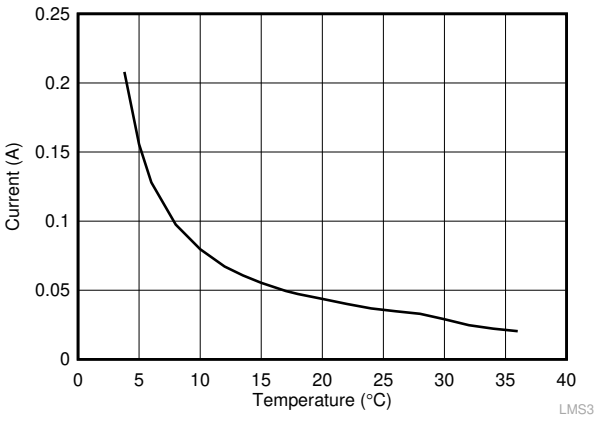
V_{IN} = 12 V

图 7-3. High-Side/Peak Current Limit for LMS36x5-Q1



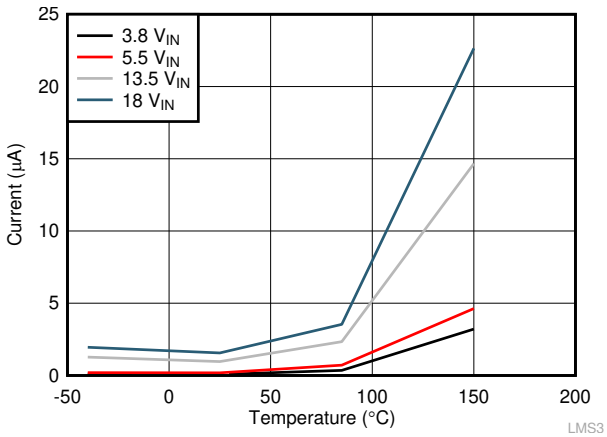
V_{IN} = 12V

图 7-4. Low-Side/Valley Current Limit for LMS36x5-Q1



V_{IN} = 12 V

图 7-5. Short Circuit Average Input Current for LMS3635-Q1



V_{IN} = 12 V

图 7-6. Shutdown Current

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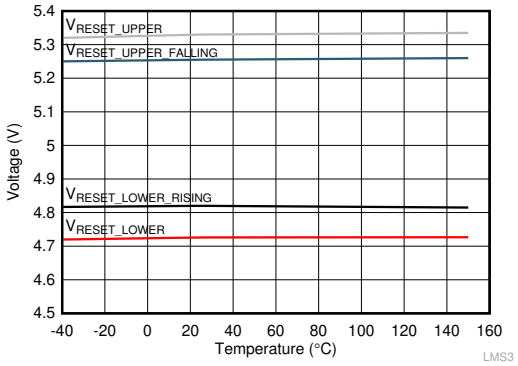

图 7-7. RESET Threshold Fixed 5-V Output

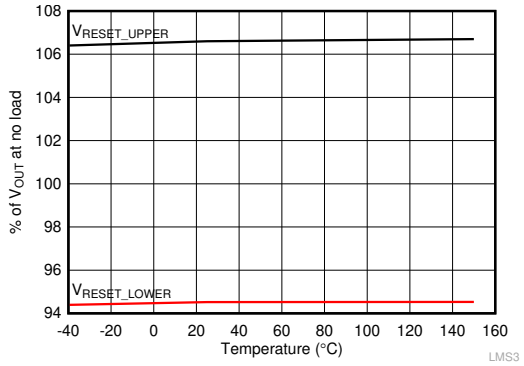

图 7-8. RESET Threshold as Percentage of Output Voltage

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8 Detailed Description

8.1 Overview

The LMS36x5-Q1 devices are wide-input voltage range, low quiescent current, high-performance regulators with internal compensation. This device is designed to minimize end-product cost and size while operating in demanding automotive and high-performance industrial environments. Normal operating frequency is 400 kHz, allowing the use of small passive components. This device has a low unloaded current consumption, eliminating the need for an external backup LDO. The LMS36x5-Q1 low shutdown current and high maximum operating voltage also allow for the elimination of an external load switch. To further reduce system cost, an advanced reset output is provided, which can often eliminate the use of an external reset or supervisor device.

The LMS36x5-Q1 is designed with a flip-chip or HotRod™ technology, greatly reducing the parasitic inductance of the pins. In addition, the layout of the device allows for partial cancellation of the current generated magnetic field which reduces the radiated noise generated by the switching action.

As a result the switch-node waveform exhibits less overshoot and ringing.

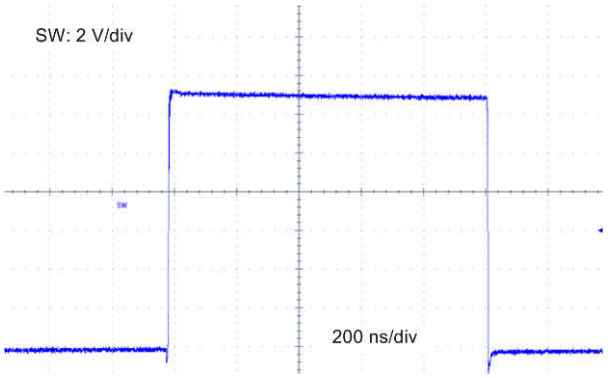

图 8-1. Switch Node Waveform (V_{IN} = 13.5 V, I_{OUT} = 5.5 A)

The LMS36x5-Q1 is AEC-Q1-qualified and has electrical characteristics ensured up to a maximum junction temperature of 150°C.

The LMS36x5-Q1 is available in a VQFN package with wettable flanks which allows easy inspection of the soldering without the requirement of x-ray checks.

Note

Throughout this data sheet, references to the LMS3635-Q1 apply equally to the LMS3655-Q1. The difference between the two devices is the maximum output current and specified MOSFET current limits.

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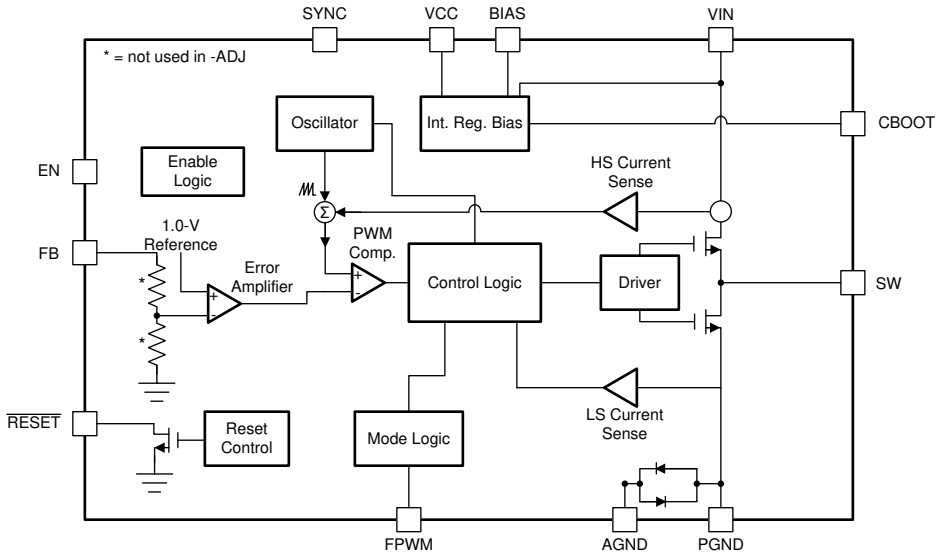
8.2 Functional Block Diagram



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8.2.1 Control Scheme

The LMS36x5-Q1 control scheme allows this device to operate under a wide range of conditions with a low number of external components. Peak current mode control allows a wide range of input voltages and output capacitance values while maintaining a constant switching frequency. Stable operation is maintained while output capacitance is changed during operation as well. This allows use in systems that require high performance during load transients and which have load switches that remove loads as the operating state changes. Short minimum on and off times ensure constant frequency regulation over a wide range of conversion ratios.

This architecture uses frequency spreading to achieve low dropout voltage maintaining output regulation as the input voltage falls close to output voltage. The frequency spreading is smooth and continuous, and activated as the off time approaches its minimum. Under these conditions, the LMS36x5-Q1 operates like a constant off-time converter, allowing the maximum duty cycle to reach 98% and output voltage regulation with 650-mV dropout. As load current is reduced, the LMS36x5-Q1 transitions to light load mode. In this mode, diode emulation is used to reduce RMS inductor current and switching frequency. Average output voltage increases slightly while lightly loaded as well.

Fixed voltage versions do not need a voltage divider connected to FB saving additional power. As a result, only 18 µA (typical, while converting 13.5 V to 3.3 V) is consumed to regulate output voltage if output is unloaded.

8.3 Feature Description

8.3.1 $\overline{\text{RESET}}$ Flag Output

While the LMS36x5-Q1 reset function resembles a standard Power-Good function, its functionality is designed to replace a discrete reset device, reducing additional component cost. There are three major differences between the reset function and the normal power good function seen in most regulators.

- A delay has been added between the point at which the output voltage is within specified limits and the flag asserts Power Good. A glitch filter prevents false flag operation for short excursions in the output voltage, such as during line and load transients. See 图 8-3 and 图 8-4 for more detail.
- $\overline{\text{RESET}}$ output signals a fault (pulls its output to ground) while the part is disabled.
- $\overline{\text{RESET}}$ continues to operate with input voltage as low as 1.5 V. Below this input voltage, $\overline{\text{RESET}}$ output may be high impedance.

Because the $\overline{\text{RESET}}$ comparator and the regulation loop share the same reference, the thresholds track with the output voltage. When EN is pulled low, the $\overline{\text{RESET}}$ flag output is forced low. When the device is disabled, $\overline{\text{RESET}}$ remains valid as long as the input voltage is ≥ 1.5 V. $\overline{\text{RESET}}$ operation can best be understood by reference to 图 8-2 and 图 8-3. Output voltage excursions lasting less than $T_{RESET\text{-}filter}$ do not trip $\overline{\text{RESET}}$. Once the output voltage is within the prescribed limits, a delay of $T_{RESET\text{-}act}$ is imposed before $\overline{\text{RESET}}$ goes high. This enables tighter tolerance than is possible with an external supervisor device while also expanding the system allowance for transient response without the need for extremely accurate internal circuitry.

This output consists of an open-drain NMOS; requiring an external pullup resistor to a suitable logic supply. It can also be pulled up to either V_{CC} or V_{OUT}, through an appropriate resistor, as desired. The pin can be left floating or grounded if the $\overline{\text{RESET}}$ function is not used in the application. The maximum current into this pin must be limited to 10 mA, and the maximum voltage must be less than 8 V.

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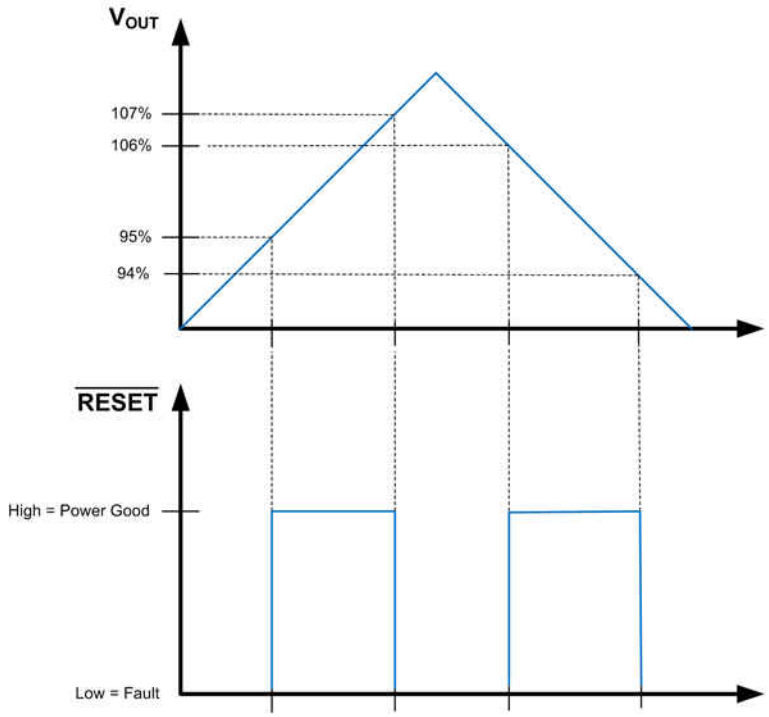

图 8-2. Static $\overline{\text{RESET}}$ Operation

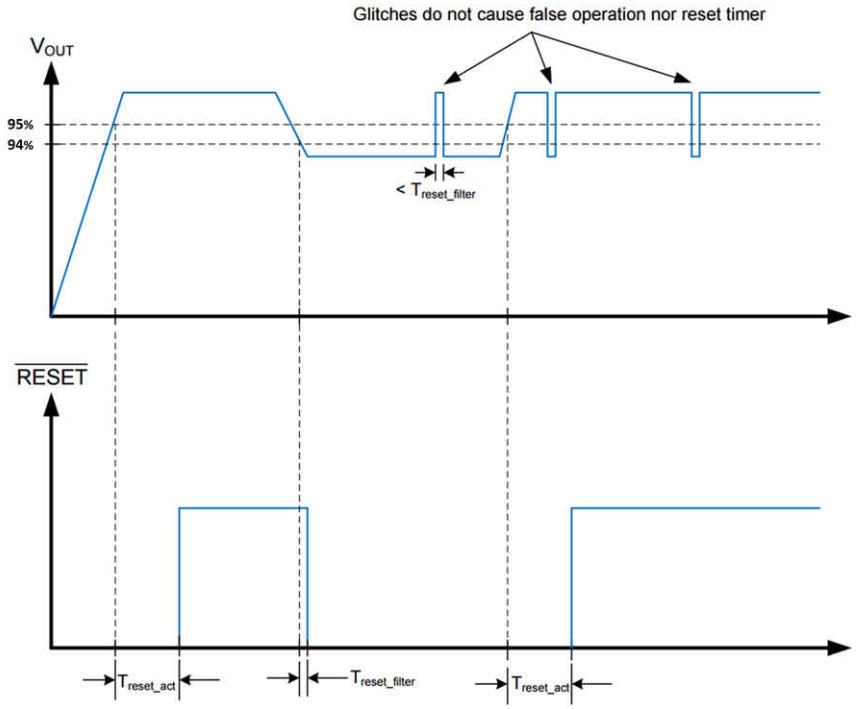

图 8-3. RESET Timing Behavior

The threshold voltage for the $\overline{\text{RESET}}$ function takes advantage of the availability of the LMS36x5-Q1 internal feedback threshold to the $\overline{\text{RESET}}$ circuit. This allows a maximum threshold of 96.5% of selected output voltage to be specified at the same time as 96% of actual set point.

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8.3.2 Enable and Start-Up

Start-up and shutdown of the LMS36x5-Q1 are controlled by the EN input. Applying a voltage of ≥ 2 V activates the device, while a voltage of ≤ 1.45 V is required for shutdown. The EN input may also be connected directly to the input voltage supply. This input must not be left floating. The LMS36x5-Q1 uses a reference-based soft start that prevents output voltage overshoots and large inrush currents as the regulator is starting up.

A typical start-up waveform is shown in 图 8-4 along with timing definitions. This waveform indicates the sequence and timing between the enable input, output voltage, and $\overline{\text{RESET}}$. From the figure, the user can define several different start-up times depending on what is relevant to the application. 表 8-1 lists the timing definitions and typical values.

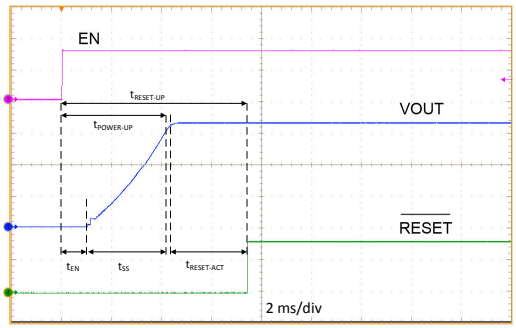

图 8-4. Typical Start-Up Waveform

表 8-1. Typical Start-Up Times

PARAMETER		DEFINITION	VALUE	UNIT
$t_{RESET-READY}$	Total start-up sequence time	Time from EN to $\overline{\text{RESET}}$ released	7.5	ms
$t_{POWER-UP}$	Start-up time	Time from EN to 90% of V_{OUT}	4	ms
t_{SS}	Soft-start time	Rise time of V_{OUT} from 10% to 90%	3.2	ms
t_{EN}	Delay time	Time from EN to start of V_{OUT} rising	1	ms
$t_{RESET-ACT}$	$\overline{\text{RESET}}$ time	Time from output voltage within 94% and $\overline{\text{RESET}}$ released	3	ms

8.3.3 Soft-Start Function

Soft-start time is fixed internally at about 4 ms. Soft start is achieved by ramping the internal reference. The LMS36x5-Q1 operates correctly even if there is a voltage present on the output before activation of the LMS36x5-Q1 (prebiased start-up). The device operates in AUTO mode during soft start, and the state of the FPWM pin is ignored during that period.

8.3.4 Current Limit

The LMS36x5-Q1 incorporates a valley current limit for normal overloads and for short-circuit protection. A precision low-side current limit prevents excessive average output current from the buck converter of the LMS36x5-Q1. A high-side peak-current limit is employed for protection of the top N MOSFET and inductors. The two current limits enable use of smaller inductors than a system with a single current limit. This scheme allows use of inductors with saturation current rated less than twice the operating current of the LMS36x5-Q1.

During overloads the low-side current limit, I_{L-LS} (see *节 7.6*), determines the maximum load current that the LMS36x5-Q1 can supply. When the low-side switch turns on, the inductor current begins to ramp down. If the current does not fall below I_{L-LS} before the next turnon cycle, then that cycle is skipped, and the low-side FET is left on until the current falls below I_{L-LS}. This is different than the more typical peak current limit, and results in 方程式 1 for the maximum load current.

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$$I_{OUT}|_{max} = I_{LS} + \frac{(V_{IN} - V_{OUT})}{2 \cdot F_S \cdot L} \cdot \frac{V_{OUT}}{V_{IN}} \quad (1)$$

If the converter continues triggering valley current limit for more than about 64 clock cycles, the device turns off both high and low side switches for approximately 6 ms (see T_W in 节 7.8). If the overload is still present after the hiccup time, another 64 cycles is counted, and the process is repeated. If the current limit is not tripped for two consecutive clock cycles, the counter is reset. The hiccup time allows the inductor current to fall to zero, resetting the inductor volt-second balance. Of course the output current is greatly reduced in this condition . A typical short-circuit transient and recovery is shown in 图 8-5.

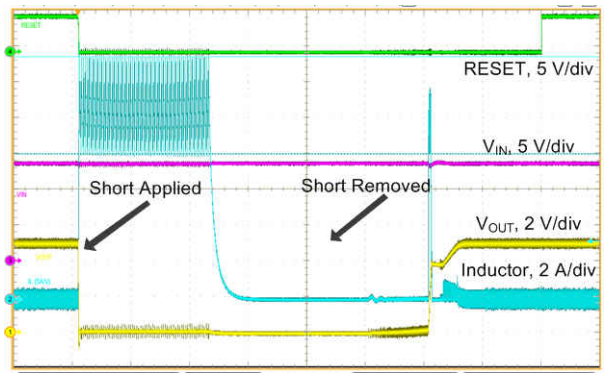

图 8-5. Short-Circuit Transient and Recovery

The high-side current limit trips when the peak inductor current reaches $I_{L\text{-}HS}$ (see 节 7.6). This is a cycle-by-cycle current limit and does not produce any frequency or current foldback. It is meant to protect the high-side MOSFET from excessive current. Under some conditions, such as high input voltage, this current limit may trip before the low-side protection. The peak value of this current limit varies with duty cycle.

In response to a short circuit, the peak current limit prevents excessive peak current while valley current limit prevents excessive average inductor current and keeps the power dissipation low during a fault. After a small number of cycles of valley current limit triggers, hiccup mode is activated.

In addition, the I_{NEG} current limit also protects the low-side switch from excessive negative current when the device is in FPWM mode. If this current exceeds I_{NEG}, the low-side switch is turned off until the next clock cycle. When the device is in AUTO mode, the negative current limit is increased to about I_{ZC} (about 0 A). This allows the device to operate in DCM.

8.3.5 Hiccup Mode

Hiccup mode prevents excessive heating and power consumption under sustained short-circuit conditions. If an overcurrent condition is maintained, the LMS36x5-Q1 shuts off its output and waits for T_W (approximately 6 ms), after which the LMS36x5-Q1 restarts operation by activating soft start.

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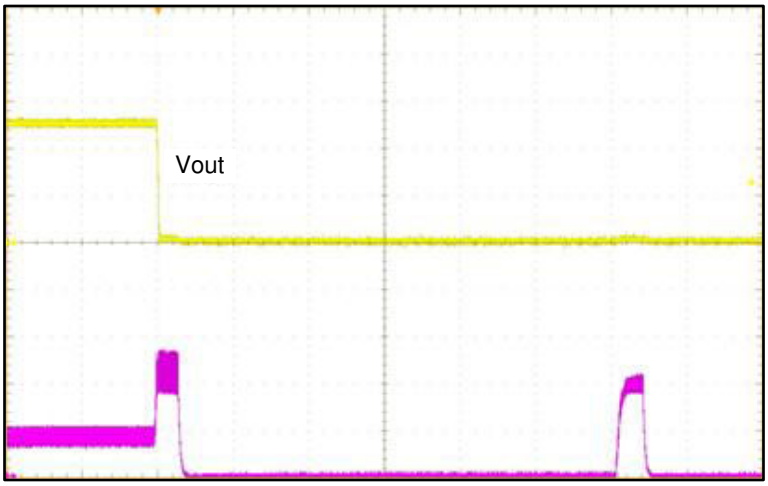

图 8-6. Hiccup Operation

During hiccup mode operation, the switch node of the LMS36x5-Q1 is high impedance after a short circuit or overcurrent persists for a short duration. Periodically, the LMS3655-Q1 attempts to restart. If the short has been removed before one of these restart attempts, the LMS36x5-Q1 operates normally.

8.3.6 Synchronizing Input

It is often desirable to synchronize the operation of multiple regulators in a single system. This technique results in better-defined EMI and can reduce the need for capacitance on some power rails. The LMS36x5-Q1 provides a SYNC input which allows synchronization with an external clock. The LMS36x5-Q1 implements an in-phase locking scheme—the rising edge of the clock signal provided to the SYNC input corresponds to turning on the high-side device within the LMS36x5-Q1. The SYNC mode operation is implemented using phase locking over a limited frequency range eliminating large glitches upon initial application of an external clock. The clock fed into the LMS36x5-Q1 replaces the internal free running clock but does not affect frequency foldback operation. Output voltage continues to be well regulated with duty factors outside of the normal 4% through 96% range though at reduced frequency.

The SYNC input recognizes a valid high level as that $\geqslant$ 1.5 V, and a valid low as that $\leqslant$ 0.4 V. The frequency synchronization signal must be in the range of 250 kHz to 500 kHz with a duty cycle of 10% to 90%. The internal clock is synced to the rising edge of the external clock. Ground this input if not used; this input must not be allowed to float. See 节 *8.4* to determine which modes are valid for synchronizing the clock.

The device remains in FPWM mode and operates in CCM for light loads when a synchronization input is provided. To prevent frequency foldback behavior at low duty cycles, provide a 200-mA load.

8.3.7 Undervoltage Lockout (UVLO) and Thermal Shutdown (TSD)

The LMS36x5-Q1 incorporates an input UVLO function. The device accepts an EN command when the input voltage rises above about 3.64 V and shuts down when the input falls below about 3.3 V. See 节 *7.6* under $V_{IN\text{-}OPERATE}$ for detailed specifications.

TSD is provided to protect the device from excessive temperature. When the junction temperature reaches about 165°C, the device shuts down; restart occurs at a temperature of about 150°C.

8.3.8 Input Supply Current

The LMS36x5-Q1 is designed to have very low input supply current when regulating light loads. This is achieved by powering much of the internal circuitry from the output. The BIAS pin is the input to the LDO that powers the majority of the control circuits. By connecting the BIAS input to the output of the regulator, this current acts as a small load on the output. This current is reduced by the ratio of V_{OUT} / V_{IN}, just like any other load. Another advantage of the LMS36x5-Q1 is that the feedback divider is integrated into the device. This allows the use of

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much larger resistors than can be used externally (>> 100 kΩ); this results in much lower divider current than is possible with external resistors.

I_{Q_VIN} is defined as the current consumed by a converter using a LMS3635-Q1 or LMS3655-Q1 device while regulating without a load. To calculate the theoretical total quiescent current, the below equation can be used with parameters from the *节 7.6* and *节 7.7* tables. While operating without a load, the LMS3635-Q1 or LMS3655-Q1 only powers itself. The device draws power from three sources: the V_{IN} pin (I_Q), the FB pin (I_{div}), and the BIAS pin (I_B). Because the BIAS and FB pins are connected to the output of the circuit, the power consumed is converted from input power with an effective efficiency, η eff, of approximately 80%. Here, effective efficiency is the added input power needed when lightly loading the converter of the LMS3635-Q1 and LMS3655-Q1 devices and is divided by the corresponding additional load. This allows unloaded current to be calculated in 方程式 2:

$$I_{Q_VIN} = I_Q + I_{EN} + (I_B + I_{div}) \frac{\text{Output Voltage}}{\eta_{eff} \times \text{Input Voltage}} \tag{2}$$

where

- I_{Q_VIN} is the current consumed by the operating (switching) buck converter while unloaded.
- I_Q is the current drawn by the LMS36x5-Q1 from its V_{IN} terminal. See I_Q in *节 7.6*.
- I_{EN} is current drawn by the LMS36x5-Q1 from its EN terminal. Include this current if EN is connected to VIN. See I_{EN} in *节 7.6*. Note that this current drops to a very low value if connected to a voltage less than 5 V.
- I_B is bias current drawn by the unloaded LMS36x5-Q1. See I_B in *节 7.7*.
- I_{div} is the current drawn by the feedback voltage divider used to set output voltage for adjustable devices. This current is zero for fixed output voltage devices.
- η_{eff} is the light load efficiency of the Buck converter with I_{Q_VIN} removed from the input current of the buck converter. 0.8 is a conservative value that can be used under normal operating conditions

Note

The EN pin consumes a few micro-amperes when tied to high; see I_{EN}. Add I_{EN} to I_Q as shown in 方程式 2 if EN is tied to V_{IN}. If EN is tied to a voltage less than 5 V, virtually no current is consumed allowing EN to be used as an UVLO pin once a voltage divider is added.

The *节 9.2.2.3* show measured values for the input supply current for both the 3.3-V and the 5-V output voltage versions.

8.4 Device Functional Modes

Refer to 表 8-2 and the following paragraphs for a detailed description of the functional modes for the LMS36x5-Q1.

These modes are controlled by the FPWM input as listed in 表 8-2. This input can be controlled by any compatible logic while the regulator is operating. If it is desired to fix the mode for a given application, the input can be either connected to ground, a logic supply, the VIN pin, or the VCC pin, as desired. The FPWM pin must not be allowed to float.

表 8-2. Mode Selection

FPWM INPUT VOLTAGE	OPERATING MODE
> 1.5 V	**Forced PWM**: The regulator operates as a constant frequency, current mode, full-synchronous converter for all loads; without diode emulation.
< 0.4 V	**AUTO**: The regulator moves between PFM and PWM as the load current changes, using diode-emulation mode to allow DCM (see the *Glossary*).

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8.4.1 AUTO Mode

In AUTO mode the device moves between PWM and PFM as the load changes. At light loads, the regulator operates in PFM. At higher loads, the mode changes to PWM. The load currents at which the mode changes can be found in the 节 9.2.2.3.

In PWM, the converter operates as a constant frequency, current mode, full synchronous converter using PWM to regulate the output voltage. While operating in this mode the output voltage is regulated by switching at a constant frequency and modulating the duty cycle to control the power to the load. This provides excellent line and load regulation and low output voltage ripple. When in PWM, the converter synchronizes to any valid clock signal on the SYNC input (see 节 8.3.6); during PFM operation, the SYNC input is ignored.

In PFM, the high-side FET is turned on in a burst of one or more cycles to provide energy to the load. The frequency of these bursts is adjusted to regulate the output, while diode emulation is used to maximize efficiency (see the *Glossary*). This mode provides high light-load efficiency by reducing the amount of input supply current required to regulate the output voltage at small loads. A small increase in the output voltage occurs in PFM. This trades off very good light load efficiency for larger output voltage ripple and variable switching frequency. The actual switching frequency and output voltage ripple depend on the input voltage, output voltage, and load. See the 节 9.2.2.3 for output voltage variation in AUTO mode. A typical switching waveform for PFM is shown in 图 8-7.

A unique feature of this device is that a minimum input voltage is required for the regulator to switch from PWM to PFM at light load. This feature is a consequence of the advanced architecture employed to provide high efficiency at light loads. 图 8-8 indicates typical values of input voltage required to switch modes at no load. Also, once the regulator switches to PFM at light load, it remains in that mode if the input voltage is reduced.

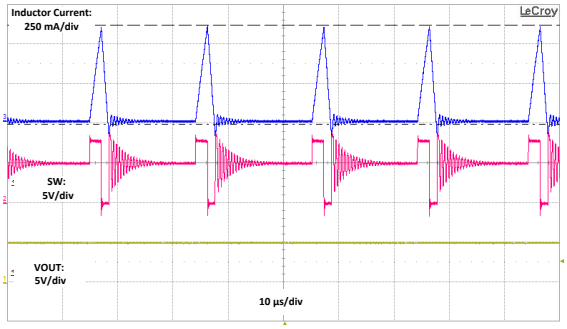

图 8-7. Typical PFM Switching Waveforms

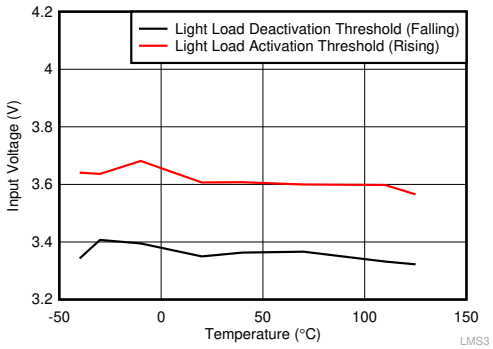

图 8-8. Input Voltage for Mode Change — 3.3-V Output, 10-µH Inductor

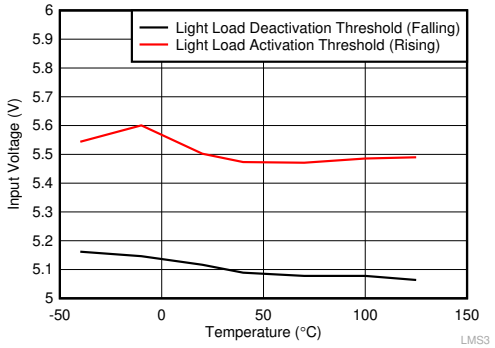

图 8-9. Input Voltage for Mode Change — 5-V Output, 10-µH Inductor

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8.4.2 FPWM Mode

With a logic high on the FPWM input, the device is locked in PWM mode. CCM operation is maintained, even at no load, by allowing the inductor current to reverse its normal direction. To prevent frequency foldback behavior at low duty cycles, provide a 200-mA load. This mode trades off reduced light load efficiency for low output voltage ripple, tight output voltage regulation, and constant switching frequency. In this mode, a negative current limit of I_{NEG} is imposed to prevent damage to the low-side FET of the regulator. When in PWM, the converter synchronizes to any valid clock signal on the SYNC input (see 节 *8.3.6*).

When constant frequency operation is more important than light load efficiency, pull the LMS36x5-Q1 FPWM input high or provide a valid synchronization input. Once activated, the diode emulation feature is turned off in this mode. This means that the device remains in CCM under light loads. Under conditions where the device must reduce the on time or off time below the ensured minimum, the frequency reduces to maintain the effective duty cycle required for regulation. This can occur for high input or output voltage ratios.

With the FPWM pin pulled low (*normal* mode), the diode emulation feature is activated. Device operation is the same as above; however, the regulator goes into DCM operation when the valley of the inductor current reaches zero.

This feature may be activated and deactivated while the part is regulating without removing the load. This feature activates and deactivates gradually preventing perturbation of output voltage. When in FPWM mode, a limited reverse current is allowed through the inductor allowing power to pass from the regulator's output to its input. In this case, ensure that a large enough input capacitor is used to absorb the reverse current.

Note

While FPWM is activated, larger currents pass through the inductor than in AUTO mode when lightly loaded. This may result in more EMI, though at a predictable frequency. Once loads are heavy enough to necessitate CCM operation, FPWM has no measurable effect on the operation of the regulator.

8.4.3 Dropout

The minimum off time influences the dropout performance of the buck regulator. As the input voltage is reduced, to near the output voltage, the off time of the high-side switch starts to approach the minimum value (see 节 *7.6*). Beyond this point the switching may become erratic or the output voltage falls out of regulation. To avoid this problem, the LMS36x5-Q1 automatically reduces the switching frequency to increase the effective duty cycle. This results in two specifications regarding dropout voltage, as shown in 节 *7.7*. One specification indicates when the switching frequency drops to 330 kHz. The other specification indicates when the output voltage has fallen to 3% of nominal. See the 节 *9.2.2.3* for typical dropout values. 图 8-10 and 图 8-11 show the overall dropout characteristic for the 5-V option. Additional dropout information is discussed in 节 *9.2.2.3* for 5-V output and in 节 *9.2.3.3* for 3.3-V output.

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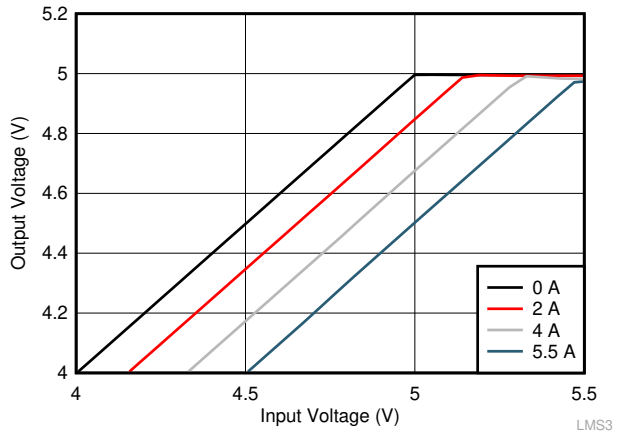

图 8-10. Overall Dropout Characteristics (V_{OUT} = 5 V)

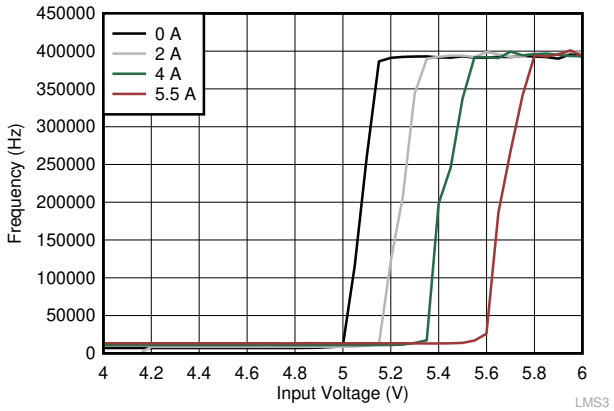

图 8-11. Frequency Dropout Characteristics (V_{OUT} = 5 V)

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8.4.4 Spread-Spectrum Operation

The spread spectrum is a factory option. In order to find which parts have spread spectrum enabled, see 节 5.

The purpose of the spread spectrum is to eliminate peak emissions at specific frequencies by spreading emissions across a wider range of frequencies. In most systems containing the LMS36x5-Q1 devices, low frequency conducted emissions from the first few harmonics of the switching frequency can be easily filtered. A more difficult design criterion is reduction of emissions at higher harmonics which fall in the FM band. These harmonics often couple to the environment through electric fields around the switch node. The LMS36x5-Q1 devices use a ±3% spread of frequencies which spread energy smoothly across the FM band but is small enough to limit sub-harmonic emissions below its switching frequency. Peak emissions at the switching frequency of the part are only reduced by slightly less than 1 dB, while peaks in the FM band are typically reduced by more than 6 dB.

The LMS36x5-Q1 devices use a cycle-to-cycle frequency hopping method based on a linear feedback shift register (LFSR). Intelligent pseudo random generator limits cycle to cycle frequency changes to limit output ripple. Pseudo random pattern repeats by approximately 1.2 Hz which is below the audio band.

The spread spectrum is only available while the clock of the LMS36x5-Q1 devices is free running at its natural frequency. Any of the following conditions overrides spread spectrum, turning it off:

- An external clock is applied to the SYNC/MODE terminal.
- The clock is slowed due to operation at low input voltage; this is operation in dropout.
- The clock is slowed under light load in AUTO mode; this is normally not seen above 200 mA of load. In FPWM mode, spread spectrum is active even if there is no load.

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9 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The LMS36x5-Q1 is a step-down DC-DC converter, typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 3.5 A or 5.5 A. The following design procedures can be used to select components for the LMS36x5-Q1. Alternately, the WEBENCH® Design Tool may be used to generate a complete design. This tool uses an iterative design procedure and has access to a comprehensive database of components. This allows the tool to create an optimized design and allows the user to experiment with various design options.

9.2 Typical Applications

9.2.1 General Application

图 9-1 shows a general application schematic. FPWM, SYNC, and EN are digital inputs. $\overline{\text{RESET}}$ is an open-drain output. FB connection is different for the fixed output options and the adjustable option.

- The FPWM pin can be connected to GND to enable light-load PFM operation. Select this option if current consumption at light load is critical. The pin can be connected to VCC or VIN for forced 400-kHz operation. Select this option if constant switching frequency is critical. The pin can also be driven by an external signal and can be toggled while the part is in operation (by an MCU, for example). Refer to the *节 8.4* for more details on the operation and signal requirements of the FPWM pin.
- The SYNC pin can be used to control the switching frequency and the phase of the converter. If the function is not needed, tie the SYNC pin to GND, VCC, or VIN.
- The $\overline{\text{RESET}}$ pin can be left floating or tied to ground if the function is not required. If the function is needed, the pin must be connected to a DC rail through a pullup resistor (100 kΩ is the typical recommended value). Check *节 8.3.1* for the details of the $\overline{\text{RESET}}$ pin function.
- If the device is a fixed-output version (3.3-V or 5-V output option), connect the FB pin directly to the output. In the case of an adjustable-output part, connect the output to the FB pin through a voltage divider. See *节 9.2.1.2* for details on component selection.
- The BIAS pin can be connected directly to the output voltage. In applications that can experience inductive shorts (such as cases with long leads on the output), a 3 Ω or so is necessary between the output and the BIAS pin, and a small capacitor to GND is necessary close to the BIAS pin (C_{BIAS}). Alternatively, a Schottky diode can be connected between OUT and GND to limit the negative voltage that can arise on the output during inductive shorts. In addition, BIAS can also be connected to an external rail if necessary and if available. The typical current into the bias pin is 15 mA when the device is operating in PWM mode at 400 kHz.
- Power components must be chosen carefully for proper operation of the converter. *节 9.2.1.2* discusses the details of the process of choosing the input capacitors, output capacitors, and inductor for the application.

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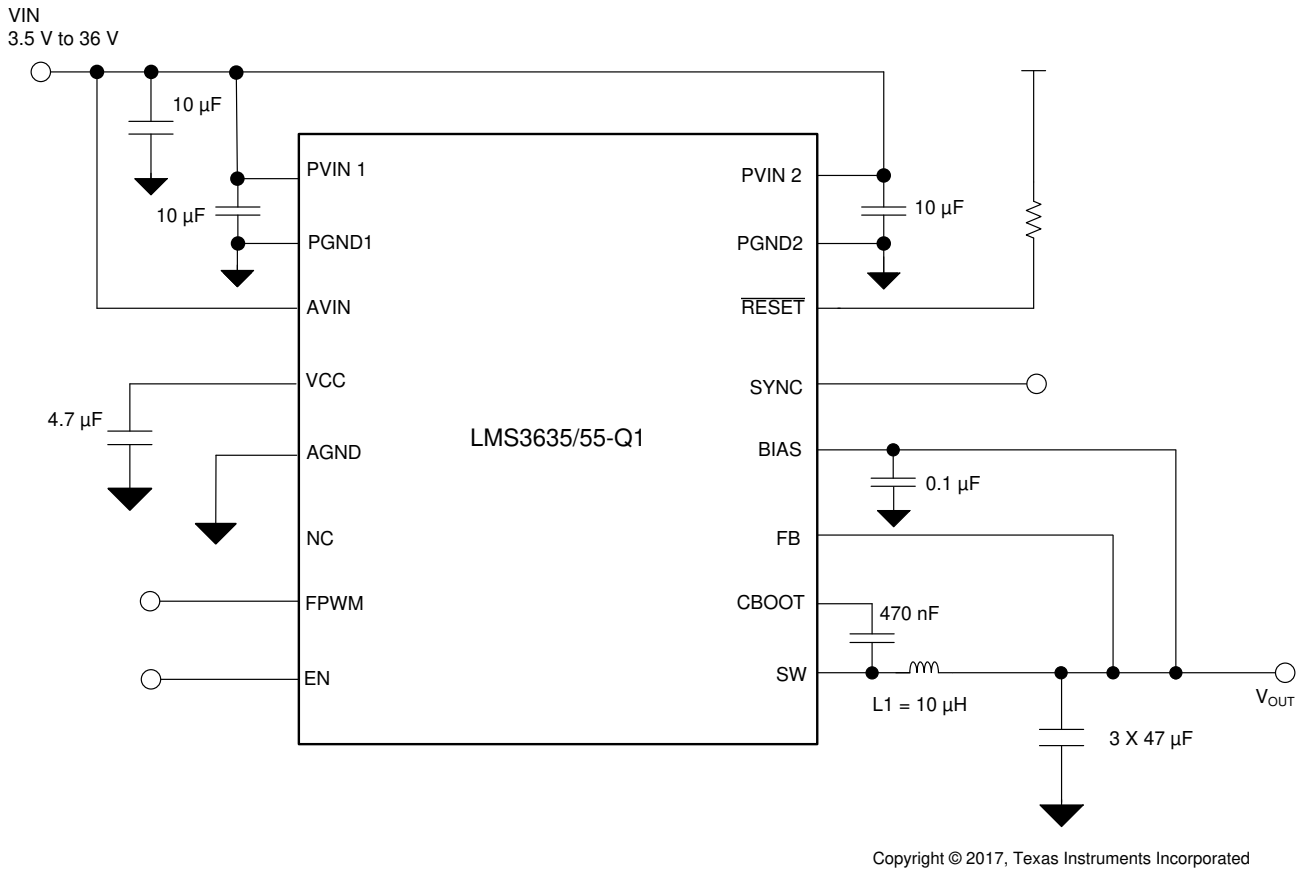

图 9-1. General Application Circuit

9.2.1.1 Design Requirements

Three sets of application-specific design requirements are outlined in 表 9-5, 表 9-6, and 表 9-7. The minimum input voltage shown in 图 9-1 is not the minimum operating voltage of the LMS36x5-Q1. Rather, it is a typical operating range for the systems. For the complete information regarding minimum input voltage see 节 *7.6*.

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMS3655-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

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9.2.1.2.2 External Components Selection

The device requires input capacitors and an output inductor-capacitor filter. These components are critical to the performance of the device.

9.2.1.2.2.1 Input Capacitors

The input capacitor supplies the AC switching current drawn from the switching action of the internal power FETs. The input current of a buck converter is discontinuous, so the ripple current supplied by the input capacitor is large. The input capacitor must be rated to handle both the RMS current and the dissipated power.

The device is designed to be used with ceramic capacitors on the input of the buck regulator. The recommended dielectric type of these capacitors is X7R rating to maintain proper tolerances over voltage and temperature.

The device requires a minimum of 20 µF of ceramic capacitance at the input. TI recommends 2 × 10 µF, 10 µF for PVIN1 and 10 µF for PVIN2. Place these capacitors close to the PVIN1, PGND1, PVIN2, and the PGND2 pads. The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying ripple current and isolating switching noise from other circuits. 表 9-1 shows the nominal and minimum values of total input capacitance recommended for the LMS36x5-Q1. Also shown are the measured values of *effective* capacitance for the indicated capacitor.

In addition, it is especially important to have small ceramic bypass capacitors of 10 nF to 100 nF very close to the PVIN1 and PVIN2 inputs to minimize ringing and EMI generation due to the high-speed switching of the device coupled with trace inductance. TI recommends that a small case size 10-nF ceramic capacitor be placed across the input, as close to the device as possible. Additional high-frequency capacitors can be used to help manage conducted EMI or voltage spike issues that may be encountered.

Many times it is desirable to use an additional electrolytic capacitor on the input, in parallel with the ceramics. This is especially true if long leads or traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by long power leads. The use of this additional capacitor also helps with voltage dips caused by input supplies with unusually high impedance.

表 9-1. Recommended Input Capacitors

NOMINAL INPUT CAPACITANCE		MINIMUM INPUT CAPACITANCE		PART NUMBER
RATED CAPACITANCE	MEASURED CAPACITANCE(1)	RATED CAPACITANCE	MEASURED CAPACITANCE(1)	
3 × 10 µF	22.5 µF	2 × 10 µF	15 µF	CL32B106KBJNNNE

(1) Measured at 14 V and 25°C.

9.2.1.2.2.2 Output Inductors and Capacitors

There are several design considerations related to the selection of output inductors and capacitors:

- Load transient response
- Stability
- Efficiency
- Output ripple voltage
- Overcurrent ruggedness

The device has been optimized for use with LC values as shown in the 图 9-1.

9.2.1.2.2.2.1 Inductor Selection

The LMS36x5-Q1 devices run in current mode and with internal compensation. The compensation of the fixed 5-V and 3.3-V configurations is stable with inductance between 6.5 µH and 20 µH. For most applications, the fixed 5-V and 3.3-V configurations of the LMS36x5-Q1 devices are optimized for a nominal inductance of 10 µH. This gives a ripple current that is approximately 20% to 30% of the full load current of 5.5 A. If applying a synchronization clock signal, the designer should appropriately size the inductor for the converter's operating switching frequency. For output voltages greater than 5 V, a proportionally larger inductor can be used, thus

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keeping the ratio of inductor current slope to internal compensating slope constant. Inductance that is too high is not recommended because it can result in poor load transient behavior and instability.

The inductor must be rated to handle the peak load current plus the ripple current—carefully review the different saturation current ratings specified by different manufacturers. Saturation current ratings are typically specified at 25°C, so ratings at maximum ambient temperature of the application should be requested from the manufacturer. For the LMS3635-Q1, TI recommends a saturation current of 7.5 A or higher, and for the LMS3655-Q1, a saturation current of 10 A or higher is recommended. Carefully review the inductor parasitic resistance; the inductor parasitic resistance must be as low as possible to minimize losses at heavy loads. The best way to obtain an optimum design is to use the Texas Instruments WEBENCH Design Tool.

表 9-2 gives a list of several possible inductors that can be used with the LMS36x5-Q1.

The designer should choose the inductors that best match the system requirements. A very wide range of inductors are available as regarding physical size, height, maximum current (thermally limited, and inductance loss limited), series resistance, maximum operating frequency, losses, and so forth. In general, inductors of smaller physical size have higher series resistance (DCR) and implicitly lower overall efficiency is achieved. Very low-profile inductors may have even higher series resistance. TI recommends finding the best compromise between system performance and cost.

表 9-2. Recommended Inductors

MANUFACTURER	PART NUMBER	SATURATION CURRENT	DC RESISTANCE
Würth	7443251000	8.5 A	16 mΩ
Würth	7447709100	10.5 A	21 mΩ
Coilcraft	DO3316T-222MLB	7.8 A	11 mΩ
Coiltronics	MPI4040R3-2R2-R	7.9 A	48 mΩ
Vishay	IHLP2525CZER2R2M01	8 A	18 mΩ
Vishay	IHLP4040DZER100M01	12 A	36.5 mΩ
Coilcraft	XAL6060-103MEC	7.6 A	27 mΩ
Coilcraft	XAL8080-103MED	10.9 A	21 mΩ

9.2.1.2.2.2.2 Output Capacitor Selection

The output capacitor of a switching converter absorbs the AC ripple current from the inductor, reduces the output voltage ripple, and provides the initial response to a load transient. The ripple voltage at the output of the converter is the product of the ripple current flowing through the output capacitor and the impedance of the capacitor. The impedance of the capacitor can be dominated by capacitive, resistive, or inductive elements within the capacitor, depending on the frequency of the ripple current. Ceramic capacitors have very low ESR and remain capacitive up to high frequencies. Their inductive component can be usually neglected at the operating frequency range of the converter.

The LMS36x5-Q1 is designed to work with low-ESR ceramic capacitors. For automotive applications, TI recommends X7R type capacitors. The *effective* value of these capacitors is defined as the actual capacitance under voltage bias and temperature. All ceramic capacitors have a large voltage coefficient, in addition to normal tolerances and temperature coefficients. Under DC bias, the capacitance value drops considerably. Larger case sizes or higher voltage capacitors are better in this regard. To help mitigate these effects, multiple small capacitors can be used in parallel to bring the minimum *effective* capacitance up to the desired value. This can also ease the RMS current requirements on a single capacitor. 表 9-3 shows the nominal and minimum values of total output ceramic capacitance recommended for the LMS36x5-Q1.The values shown also provide a starting point for other output voltages, when using the adjustable option. More output capacitance can be used to improve transient performance and reduce output voltage ripple.

In order to minimize ceramic capacitance, a low-ESR electrolytic capacitor can be used in parallel with minimal ceramic capacitance. As a starting point for designing with an output electrolytic capacitor, 表 9-4 shows the minimum ceramic capacitance recommended when paired with a 120-µF Aluminum-polymer (ESR = 25 mΩ) in

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order to maintain stable operation. Depending on load transient design requirements, the designer may choose to add additional capacitance.

In practice, the output capacitor has the most influence on the transient response and loop phase margin. Load transient testing and bode plots are the best way to validate any given design and should always be completed before the application goes into production. Make a careful study of temperature and bias voltage variation of any candidate ceramic capacitor in order to ensure that the minimum value of *effective* capacitance is provided. The best way to obtain an optimum design is to use the Texas Instruments WEBENCH Design Tool.

In adjustable applications the feed-forward capacitor, C_{FF}, provides another degree of freedom when stabilizing and optimizing the design. Refer to *Optimizing Transient Response of Internally Compensated DC-DC Converters With Feedforward Capacitor* (SLVA289) for helpful information when adjusting the feed-forward capacitor.

In addition to the capacitance shown in 表 9-3, a small ceramic capacitor placed on the output can help to reduce high frequency noise. Small case-size ceramic capacitors in the range of 1 nF to 100 nF can be very helpful in reducing spikes on the output caused by inductor parasitics.

Limit the maximum value of total output capacitance to between 800 µF and 1200 µF. Large values of output capacitance can prevent the regulator from starting up correctly and adversely effect the loop stability. If values greater than the given range are to be used, then a careful study of start-up at full load and loop stability must be performed.

表 9-3. Recommended Output Ceramic Capacitors

OUTPUT VOLTAGE	NOMINAL OUTPUT CERAMIC CAPACITANCE	MINIMUM OUTPUT CERAMIC CAPACITANCE	PART NUMBER
	RATED CAPACITANCE	RATED CAPACITANCE	
3.3 V (fixed option) (1)	5 × 47 µF	4 x 47µF	GRM32ER71A476KE15L
5 V (fixed option) (1)	4 × 47 µF	3 × 47µF	GRM32ER71A476KE15L
6 V(1)	4× 47 µF	3 × 47 µF	GRM32ER71A476KE15L
10 V(2)	4 × 47 µF	3 × 47 µF	GRM32ER71A476KE15L

(1) L = 10 µH
(2) L = 20 µH

表 9-4. Recommended Output Al-Polymer and Ceramic Capacitors

OUTPUT VOLTAGE	OUTPUT AL-POLYMER CAPACITANCE	PART NUMBER	MINIMUM OUTPUT CERAMIC CAPACITANCE
	RATED CAPACITANCE		RATED CAPACITANCE
3.3 V (fixed option) (1)	120 µF	APXE160ARA121MH70G	1 × 47µF + 1 x 20µF
5 V (fixed option) (1)	120 µF	APXE160ARA121MH70G	1 × 47µF

(1) L = 10 µH

Consult *Output Ripple Voltage for Buck Switching Regulator* (SLVA630) for more details on the estimation of the output voltage ripple for this converter.

9.2.1.2.3 Setting the Output Voltage

For the fixed output voltage versions, the FB input is connected directly to the output voltage node. Preferably, near the top of the output capacitor. If the feedback point is located further away from the output capacitors (that is, remote sensing), then a small 100-nF capacitor may be needed at the sensing point.

9.2.1.2.4 FB for Adjustable Output

The adjustable version of the LMS3635-Q1 and LMS3655-Q1 devices regulate output voltage to a level that results in the FB node being V_{REF}, which is approximately 1 V (see 节 7.6). Output voltage given a specific feedback divider can be calculated using 方程式 3:

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$$\text{Output Voltage} = V_{ref} \times \frac{R_{FBB} + R_{FBT}}{R_{FBB}} \quad (3)$$

To ensure proper behavior for all modes of operation, a 50-kΩ resistor is recommended for R_{FBT}. R_{FBB} can then be determined using 方程式 4:

$$R_{FBB} = \frac{V_{ref} \times R_{FBT}}{\text{Output Voltage} - V_{ref}} \quad (4)$$

In addition, a feed-forward capacitor C_{FF} may be required to optimize the transient response. For output voltages greater than 6 V, the WEBENCH Design Tool can be used to optimize the design.

9.2.1.2.5 VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the LMS36x5-Q1. This output requires a 4.7-µF, 10-V ceramic capacitor connected from VCC to GND for proper operation. X7R type is recommended for automotive applications. In general, this output must not be loaded with any external circuitry. However, the output can be used to supply a logic level to the FPWM input or for the pullup resistor used with the $\overline{\text{RESET}}$ output. The nominal output of the LDO is 3.15 V.

9.2.1.2.6 BIAS

The BIAS pin is the input to the internal LDO. As detailed in 节 8.3.8, this input is connected directly to V_{OUT} to provide the lowest possible supply current at light loads. Because this input is connected directly to the output, it must be protected from negative voltage transients. Such transients may occur when the output is shorted at the end of a long PCB trace or cable. If this is likely in a given application, then place a small resistor in series between the BIAS input and V_{OUT} .

Size the resistor to limit the current out of the BIAS pin to < 100 mA. Values in the range of 2 Ω to 5 Ω are typically sufficient. Values greater than 5 Ω are not recommended. As a rough estimate, assume that the full negative transient appears across R_{BIAS} and design for a current of < 100 mA. In severe cases, a Schottky diode can be placed in parallel with the output to limit the transient voltage and current.

When a resistor is used between the output and the BIAS pin, a 0.1-µF capacitor is required close to the BIAS pin. In general, TI recommends having a 0.1-µF capacitor near the BIAS pin, regardless of the presence of the resistor, unless the trace between the output capacitors and the BIAS pin is very short.

The typical current into the bias pin is 15 mA when the device is operating in PWM mode at 400 kHz.

9.2.1.2.7 CBOOT

The LMS36x5-Q1 requires a *boot-strap* capacitor between the CBOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the power MOSFETs. A ceramic capacitor of 0.47 µF, ⩾ 6.3 V is required.

9.2.1.2.8 Maximum Ambient Temperature

As with any power conversion device, the LMS36x5-Q1 dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature (T_J) is a function of the ambient temperature, the power loss, and the effective thermal resistance, $R_{\theta JA}$ of the device and PCB combination. The maximum internal die temperature for the LMS3655-Q1 is 150°C, thus establishing a limit on the maximum device power dissipation and therefore load current at high ambient temperatures. 方程式 5 shows the relationships between the important parameters.

$$I_{OUT} = \frac{(T_J - T_A)}{R_{\theta JA}} \cdot \frac{\eta}{(1-\eta)} \cdot \frac{1}{V_{OUT}} \quad (5)$$

The device uses an advanced package technology that uses the pads and pins as heat spreading paths. As a result, the pads must be connected to large copper areas to dissipate the heat from the IC. All pins provide some heat relief capability but the PVINs, PGNDs, and SW pins are of particular importance for proper heat dissipation. Utilization of all the board layers for heat dissipation and using vias as heat pipes is recommended. The 节 11.1 includes an example that shows layout for proper heat management.

9.2.1.3 Application Curves

These parameters are not tested and represent typical performance only. Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, T_A = 25°C. For the purpose of offering more information to the designer, information for the application with FPWM pin high (FPWM mode) and FPWM pin low (AUTO mode) is included, although the schematic shows the application running specifically in FPWM mode. The mode is specified under each following graph.

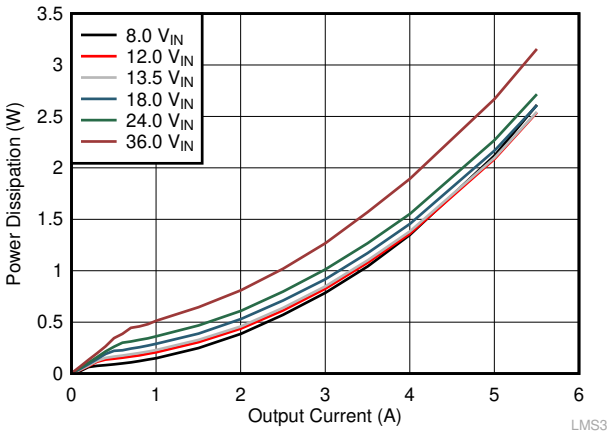

图 9-2. Power Dissipation 5-V Output

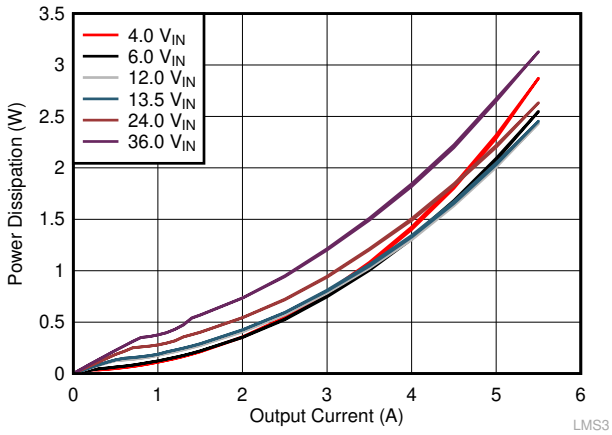

图 9-3. Power Dissipation 3.3-V Output

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9.2.2 Fixed 5-V Output for USB-Type Applications

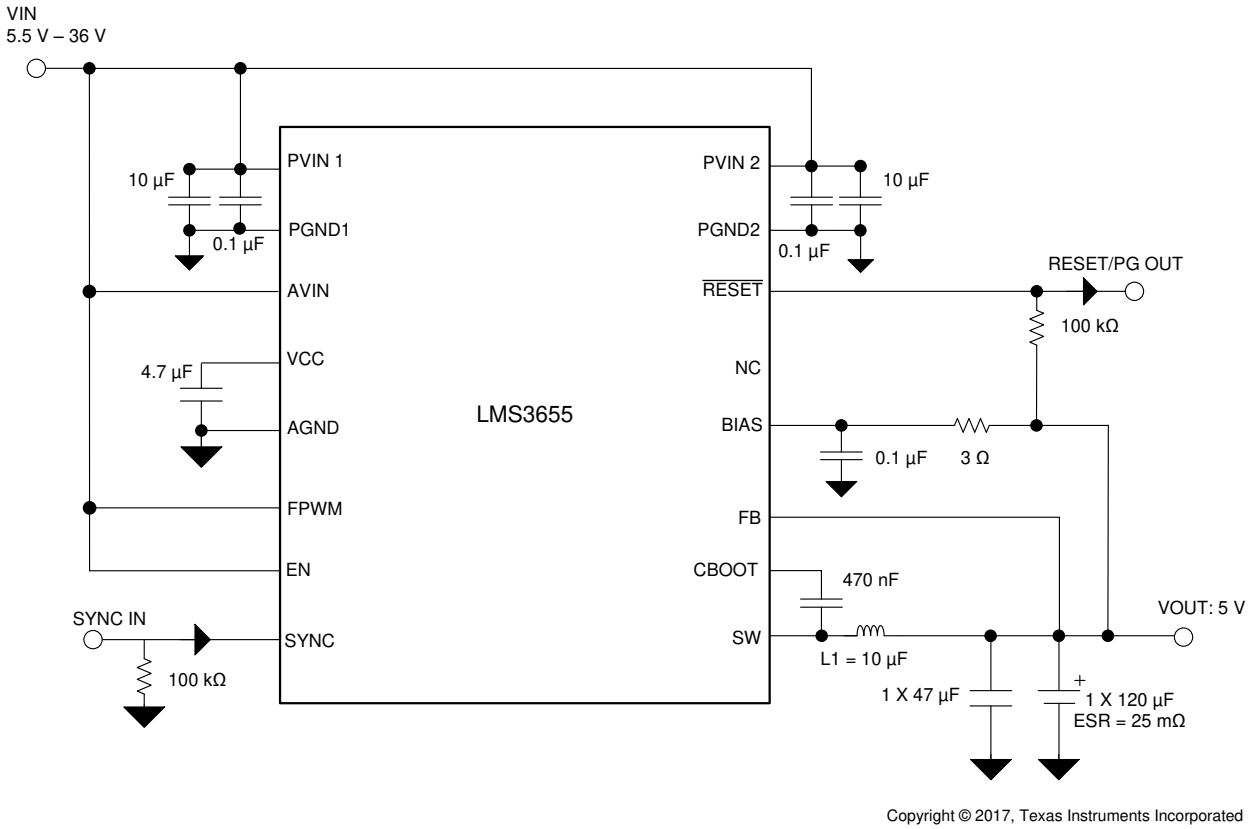

图 9-4. Fixed 5-V, 5.5-A Output Power Supply

9.2.2.1 Design Requirements

Example requirements for a typical 5-V application. The input voltages are here for illustration purposes only. See *节 7.6* for minimum operating input voltage. The minimum input voltage necessary to achieve proper output regulation depends on the components used. See 图 9-10 for typical drop-out behavior.

表 9-5. Example Requirements for 5-V Typical Application

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	8 V to 18 V steady-state, 5.5 V to 36 V transients
Output current	0 A to 5.5 A
Switching Frequency at 0-A load	Critical: must have > 250 kHz
Current Consumption at 0-A load	Not critical: < 100 mA acceptable
Synchronization	Yes: 300 kHz supplied by MCU

9.2.2.2 Detailed Design Procedure

- BIAS is connected to the output. This example assumes that the load is connected to the output through long wires so a 3-Ω resistor is inserted to minimize risks of damage to the part during load shorts. In addition 0.1-µF capacitor is required close to the bias pin.
- FB is connected directly to the output. BIAS and FB are connected to the output through separate traces. This is important to reduce noise and achieve good performances. See *节 11.1* for more details on the proper layout method.
- SYNC is connected to ground through a pulldown resistor, and an external synchronization signal can be applied. The pulldown resistor ensures that the pin is not floating when the SYNC pin is not driven by any source.

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- EN is connected to VIN so the device operates as soon as the input voltage rises above the $V_{IN-OPERATE}$ threshold.
- FPWM is connected to VIN. This causes the device to operate in FPWM mode. In this mode, the device remains in CCM operation regardless of the output current and is ensured to be within the boundaries set by F_{SW}. To prevent frequency foldback behavior at low duty cycles, provide a 200-mA load. The drawback is that the efficiency is not optimized for light loads. See 节 *8.4* for more details.
- A 4.7-µF capacitor is connected between VCC and GND close to the VCC pin. This ensures stable operation of the internal LDO.
- $\overline{\text{RESET}}$ is biased to the output in this example. A pullup resistor is necessary. A 100-kΩ is selected for this application and is generally sufficient. The value can be selected to match the needs of the application but must not lead to excessive current into the $\overline{\text{RESET}}$ pin when $\overline{\text{RESET}}$ is in a low state. Consult 节 *7.1* for the maximum current allowed. In addition, a low pullup resistor could lead to an incorrect logic level due to the value of R_{RESET}. Consult 节 *7.6* for details on the $\overline{\text{RESET}}$ pin.
- Input capacitor selection is detailed in 节 *9.2.1.2.2.1*. It is important to connect small high-frequency capacitors C_{IN_HF1} and C_{IN_HF2} as close to both inputs PVIN1 and PVIN2 as possible.
- Output capacitor selection is detailed in 节 *9.2.1.2.2.2.2*.
- Inductor selection is detailed in 节 *9.2.1.2.2.2.1*. In general, a 10-µH inductor is recommended for the fixed output options. For the adjustable output configurations, the inductance can vary with the output voltage due to ripple and current limit requirements.

9.2.2.3 Application Curves

The following characteristics apply only to the circuit of 节 *9.2.2*. *These parameters are not tested and represent typical performance only.* Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, T_A = 25°C. For the purpose of offering more information to the designer, information for the application with FPWM pin high (FPWM mode) and FPWM pin low (AUTO mode) is included, although the schematic shows the application running specifically in FPWM mode. The mode is specified under each following graph.

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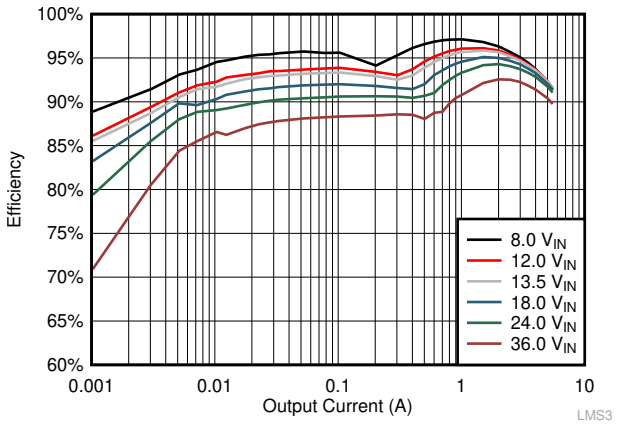
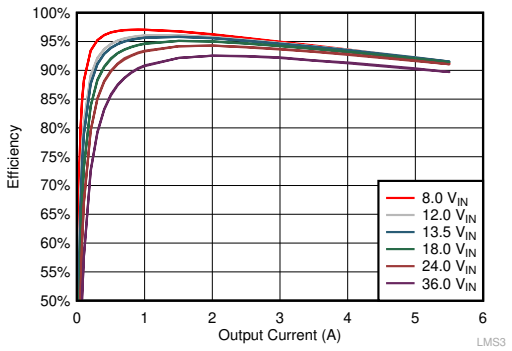


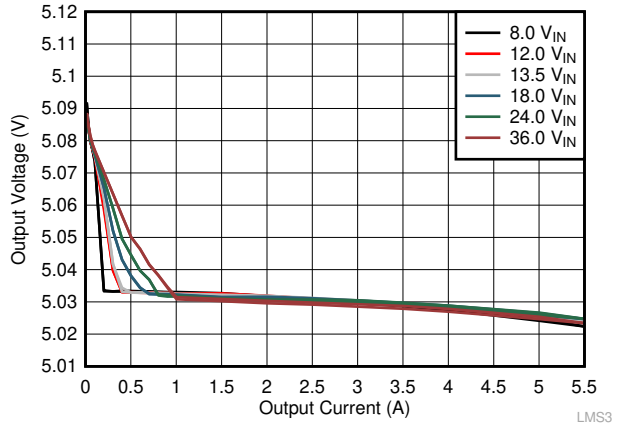
V_{OUT} = 5 V AUTO

图 9-5. Efficiency



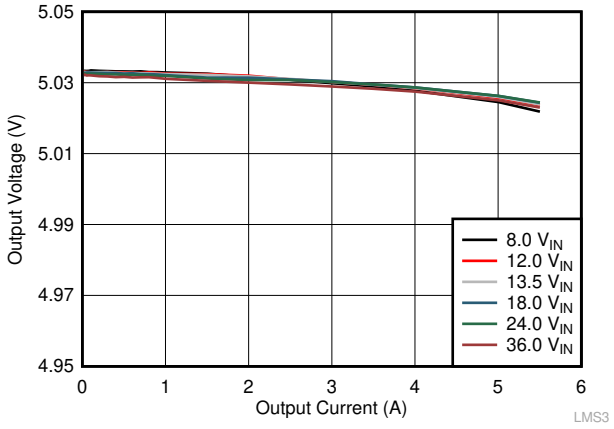
V_{OUT} = 5 V FPWM

图 9-6. Efficiency



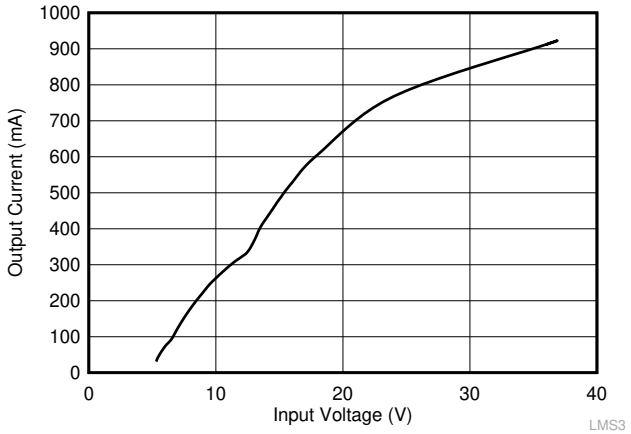
V_{OUT} = 5 V AUTO

图 9-7. Load and Line Regulation



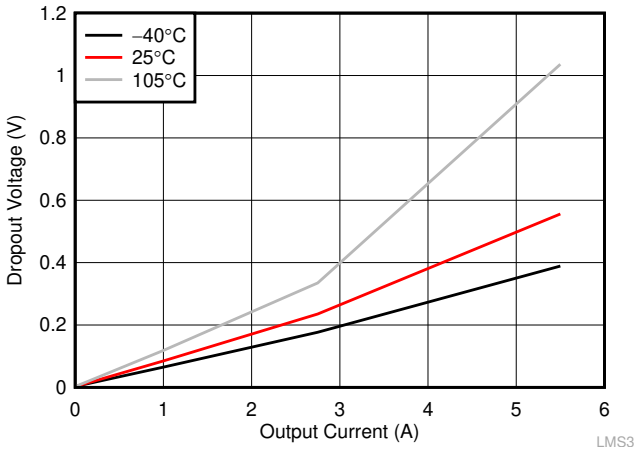
V_{OUT} = 5 V FPWM

图 9-8. Load and Line Regulation



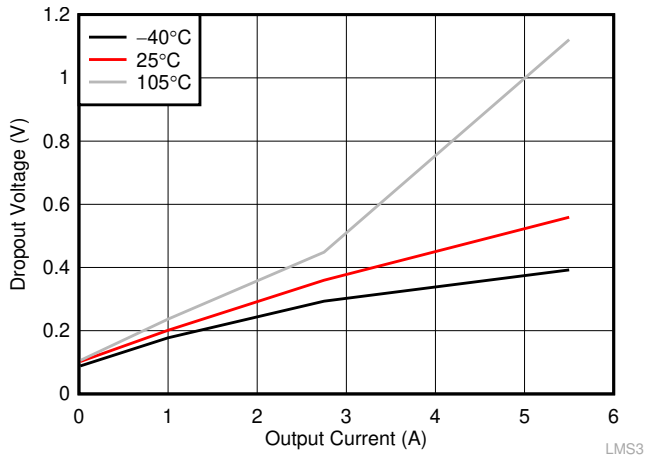
V_{OUT} = 5 V

图 9-9. Load Current for PFM-to-PWM Transition



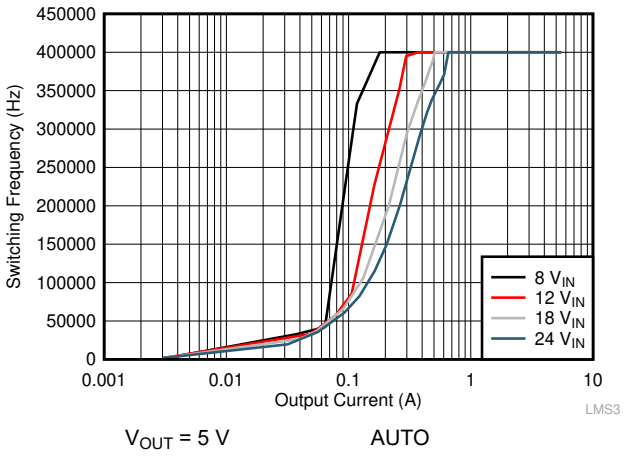
V_{OUT} = 5 V

图 9-10. Dropout for –3% Regulation



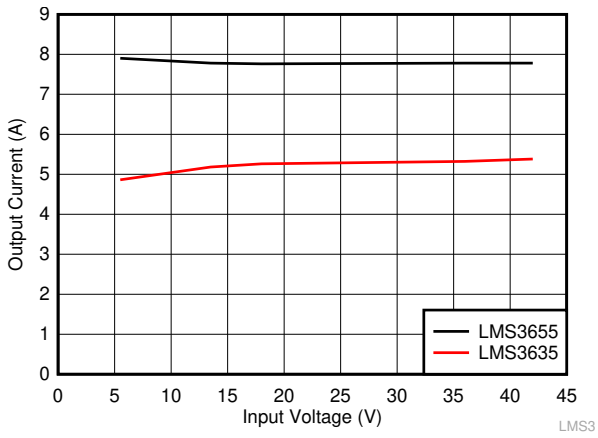
V_{OUT} = 5 V

图 9-11. Dropout for ⩾ 330 kHz



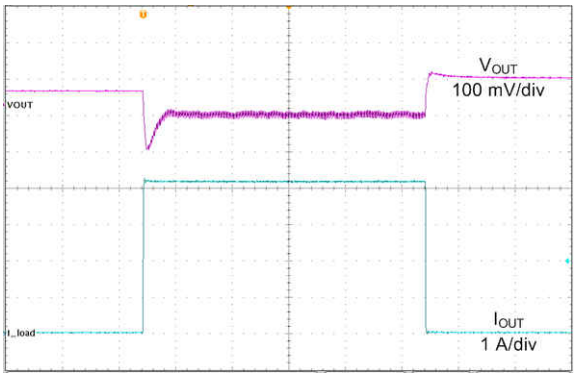
V_{OUT} = 5 V AUTO

图 9-12. Switching Frequency vs Load Current



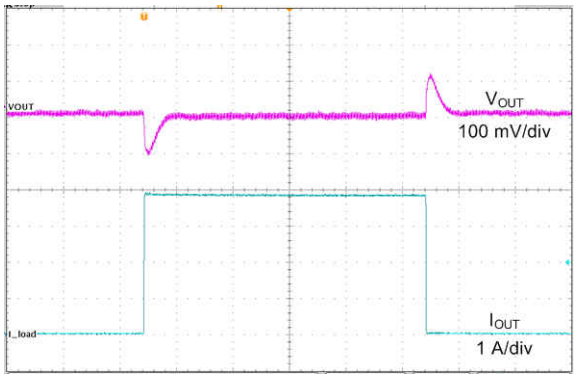
V_{OUT} = 5 V L = 10 µH

图 9-13. Output Current Level Limit Before Overcurrent Protection



AUTO V_{OUT} = 5 V L = 10 µH
C_{OUT} = 170 µF I_{OUT} = 10 mA to 3.5 A $T_R = T_F$ = 1 µs

图 9-14. Load Transients



FPWM V_{OUT} = 5 V L = 10 µH
C_{OUT} = 170 µF I_{OUT} = 0 A to 3.5 A $T_R = T_F$ = 1 µs

图 9-15. Load Transient

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9.2.3 Fixed 3.3-V Output

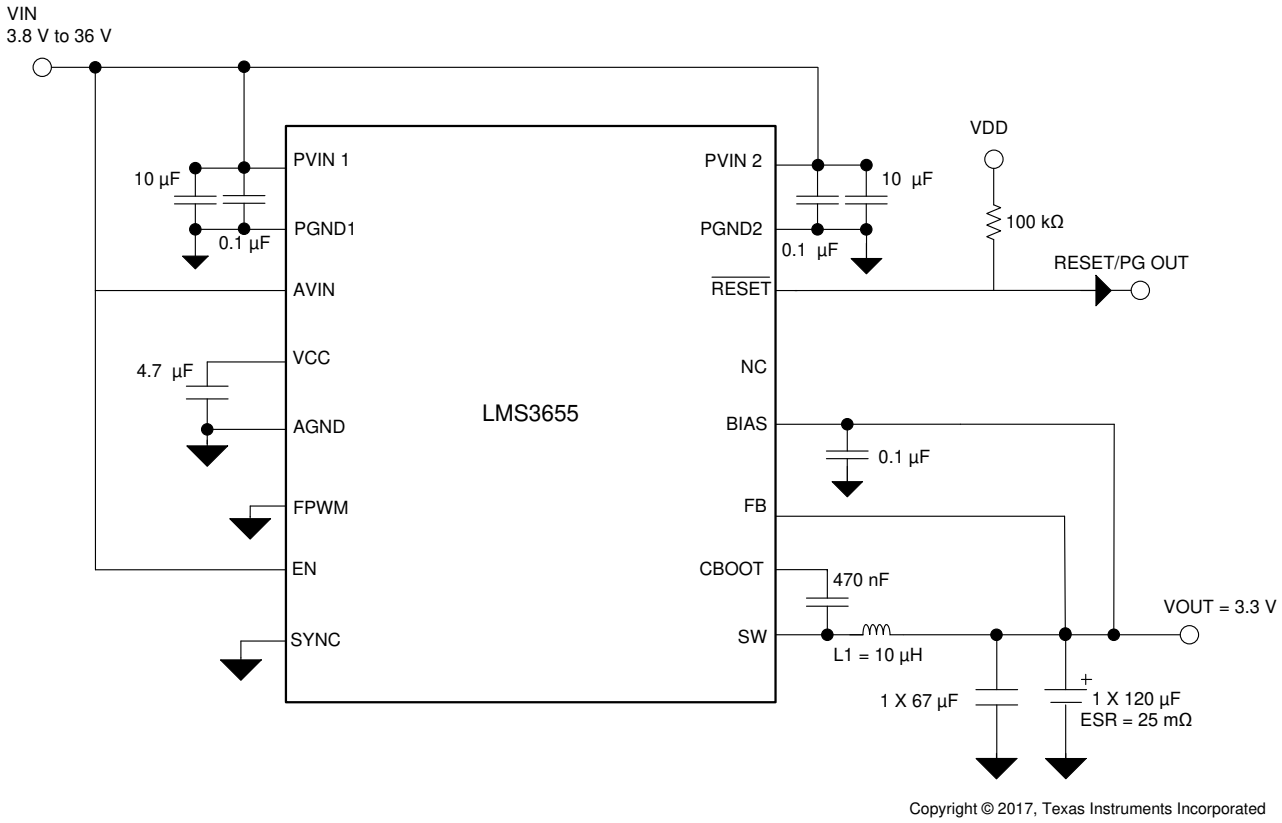

图 9-16. Fixed 3.3-V, 5.5-A Output Power Supply

9.2.3.1 Design Requirements

Example requirements for a typical 3.3-V application. The input voltages are here for illustration purposes only. See *节 7.6* for minimum operating input voltage. The minimum input voltage necessary to achieve proper output regulation depends on the components used. See 图 9-23 for typical drop-out behavior.

表 9-6. Example Requirements for 3.3-V Application

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	8-V to 18-V steady-state, 4.0-V to 36-V transients
Output current	0 A to 5.5 A
Switching Frequency at 0-A load	Not critical: Need >330 kHz at high load only
Current Consumption at 0-A load	Critical: Need to ensure low current consumption to reduce battery drain
Synchronization	No

9.2.3.2 Detailed Design Procedure

- BIAS is connected to the output. This example assumes that the load is close to the output so no bias resistance is necessary. A 0.1-µF capacitor is still recommended close to the bias pin.
- FB is connected directly to the output. BIAS and FB are connected to the output through separate traces. This is important to reduce noise and achieve good performances. See *节 11.1* for more details on the proper layout method.
- SYNC is connected to ground directly as there is no need for this function in this application.
- EN is connected to VIN so the device operates as soon as the input voltage rises above the $V_{IN-OPERATE}$ threshold.

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- FPWM is connected to GND. This causes the device to operate in AUTO mode. In this mode, the switching frequency is adjusted at light loads to optimize efficiency. As a result the switching frequency changes with the output current until medium load is reached. The part will then switch at the frequency defined by F_{SW}. See 节 *8.4* for more details.
- A 4.7-µF capacitor is connected between VCC and GND close to the VCC pin. This ensures stable operation of the internal LDO.
- $\overline{\text{RESET}}$ is biased to an external rail in this example. A pullup resistor is necessary. A 100-kΩ pullup resistor is selected for this application and is generally sufficient. The value can be selected to match the needs of the application but must not lead to excessive current into the $\overline{\text{RESET}}$ pin when $\overline{\text{RESET}}$ is in a low state. Consult 节 *7.1* for the maximum current allowed. In addition, a low pullup resistor could lead to an incorrect logic level due to the value of R_{RESET}. Consult 节 *7.6* for details on the $\overline{\text{RESET}}$ pin.
- It is important to connect small high frequency capacitors C_{IN_HF1} and C_{IN_HF2} as close to both inputs PVIN1 and PVIN2 as possible. For the detailed process of choosing input capacitors, refer to 节 *9.2.1.2.2.1*.
- Output capacitor selection is detailed in 节 *9.2.1.2.2.2*.
- Inductor selection is detailed in 节 *9.2.1.2.2.1*. In general, a 10-µH inductor is recommended for the fixed output options. For the adjustable output configurations, the inductance can vary with the output voltage due to ripple and current limit requirements.

9.2.3.3 Application Curves

The following characteristics apply only to the circuit of 图 9-16. *These parameters are not tested and represent typical performance only.* Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, T_A = 25°C. For the purpose of offering more information to the designer, information for the application with FPWM pin high (FPWM mode) and FPWM pin low (AUTO mode) is included, although the schematic shows the application running specifically in AUTO mode. The mode is specified under each of the following graphs.

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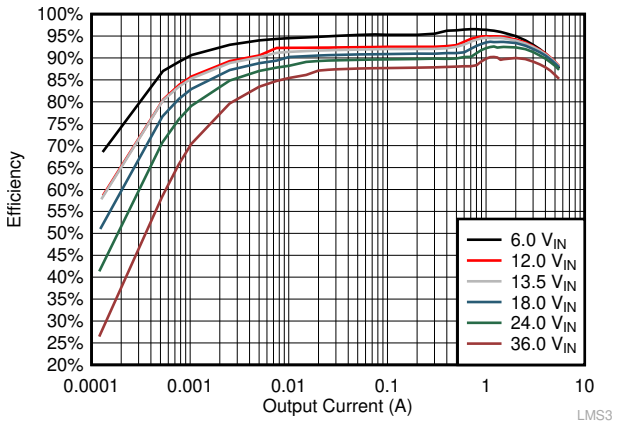
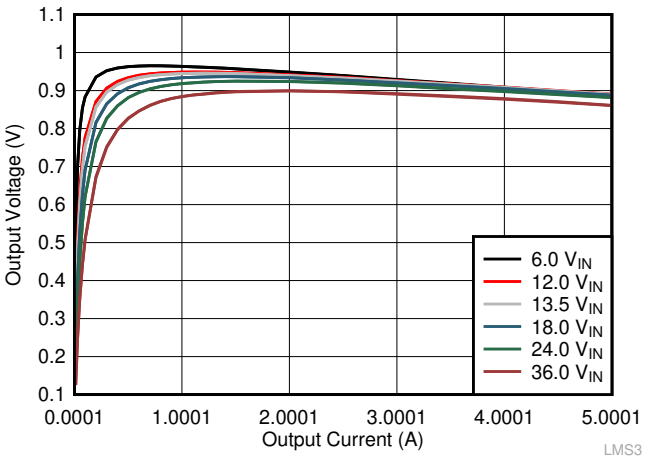


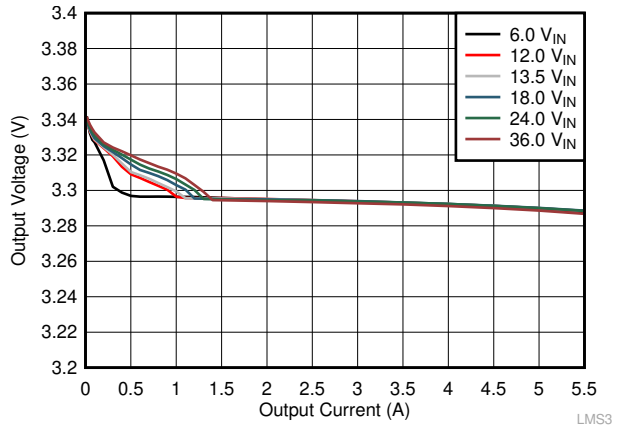
V_{OUT} = 3.3 V AUTO

图 9-17. Efficiency



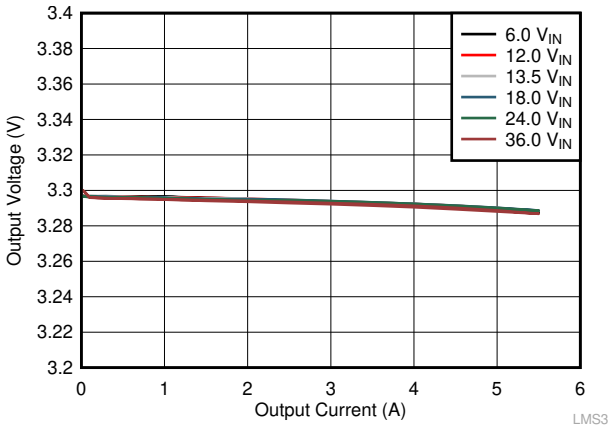
V_{OUT} = 3.3 V FPWM

图 9-18. Efficiency



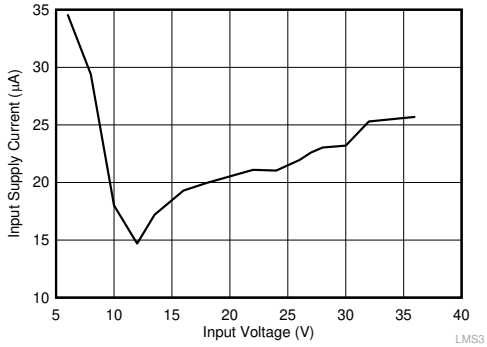
V_{OUT} = 3.3 V AUTO

图 9-19. Load and Line Regulation



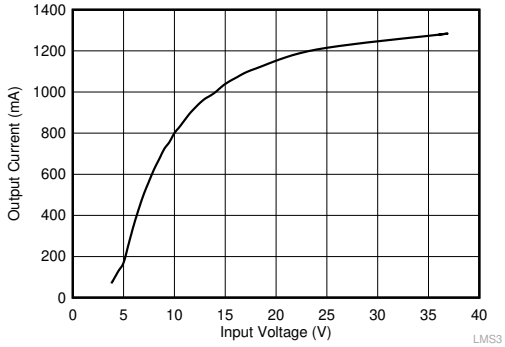
V_{OUT} = 3.3 V FPWM

图 9-20. Load and Line Regulation



V_{OUT} = 3.3 V AUTO I_{OUT} = 0 A

图 9-21. Input Supply Current (Includes Leakage Current of Capacitor)



V_{OUT} = 3.3 V

图 9-22. Load Current for PFM-to-PWM Transition

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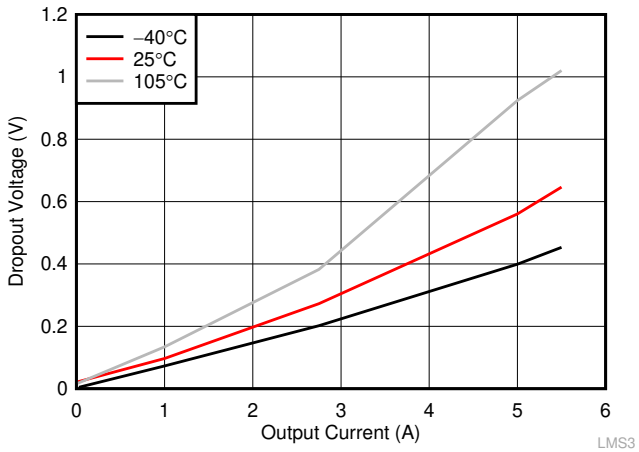
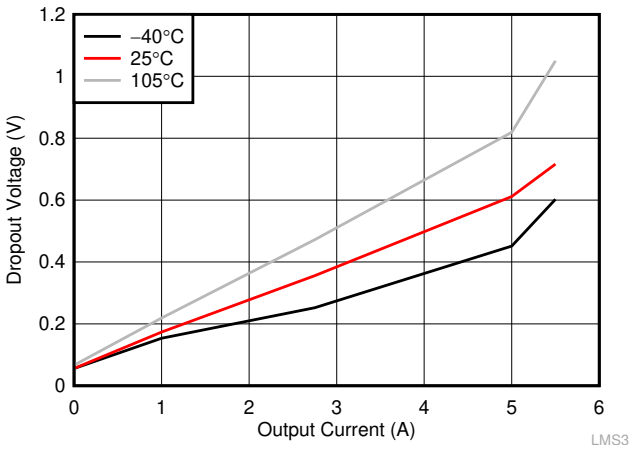


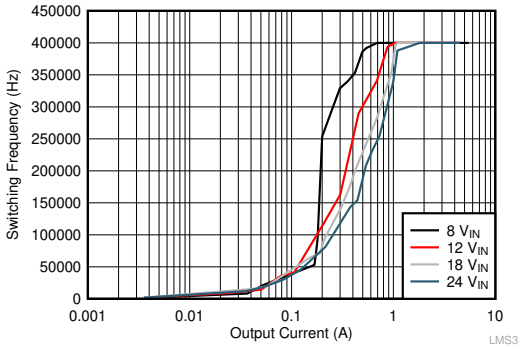
V_{OUT} = 3.3 V

图 9-23. Dropout for –3% Regulation



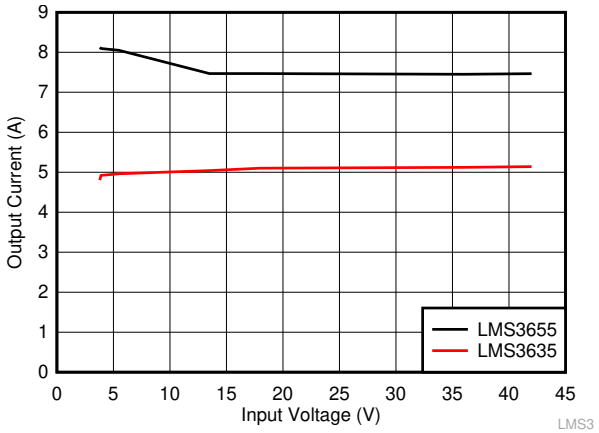
V_{OUT} = 3.3 V

图 9-24. Dropout for ≥ 330 kHz



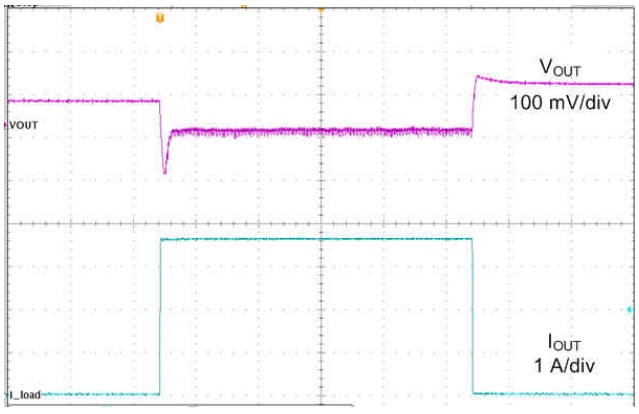
V_{OUT} = 3.3 V AUTO

图 9-25. Switching Frequency vs Load Current



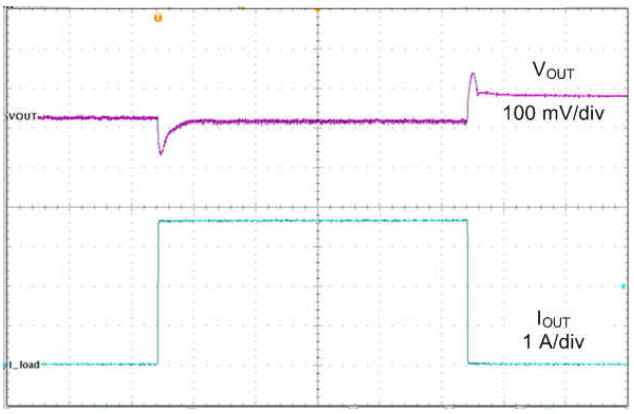
V_{OUT} = 3.3 V L = 10 µH

图 9-26. Output Current Level for Overcurrent Protection Trip



AUTO V_{OUT} = 3.3 V L = 10 µH,
C_{OUT} = 190 µF I_{OUT} = 0 A to 3.5 A $T_R = T_F$ = 1 µs

图 9-27. Load Transient



FPWM V_{OUT} = 3.3 V L = 10 µH,
C_{OUT} = 190 µF I_{OUT} = 0 A to 3.5 A $T_R = T_F$ = 1 µs

图 9-28. Load Transient

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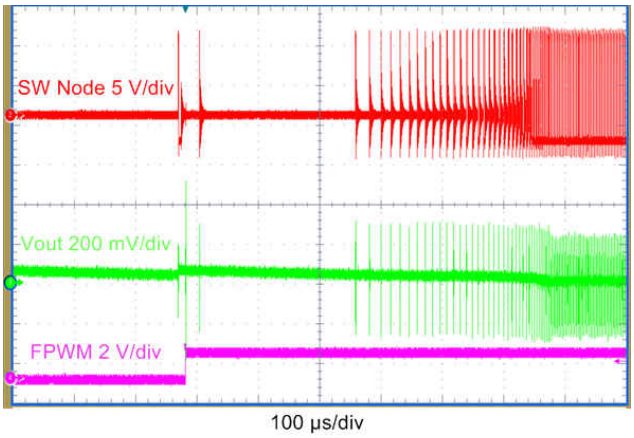

V_{OUT} = 3.3 V I_{OUT} = 10 mA

图 9-29. Mode Change Transient AUTO to FPWM mode

9.2.4 6-V Adjustable Output

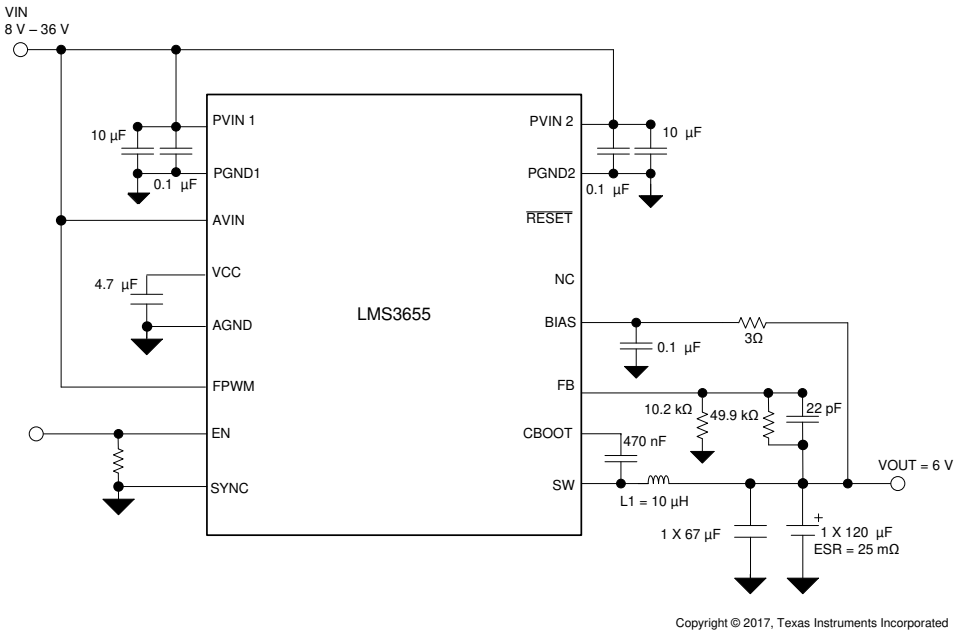

图 9-30. 6-V Output Power Supply

9.2.4.1 Design Requirements

The application highlighted in this section is for a typical 6-V system but can be used as a basis for the implementation of the adjustable version of the LMS36x5-Q1 for other output voltages as well. The input voltages are here for illustration purposes only. See *节 7.6* for minimum operating input voltage.

表 9-7. Example Requirements for 6-V Application

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	8-V to 18-V steady-state
Output current	0 A to 5.5 A
Switching Frequency at 0-A load	> 250 kHz preferred
Current Consumption at 0-A load	Not critical
Synchronization	No

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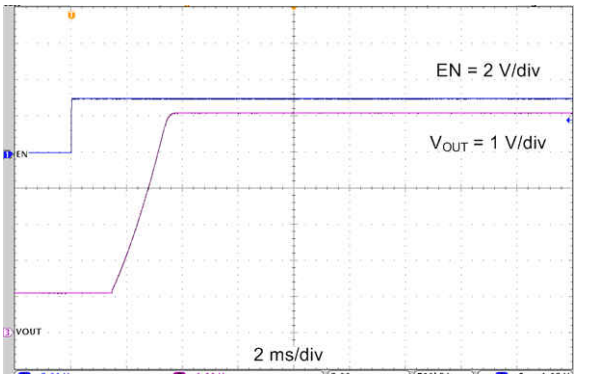
9.2.4.2 Detailed Design Procedure

- BIAS is connected to the output. This example assumes that inductive shorts are a risk for this application so a 3-Ω resistor is added between BIAS and the output. A 0.1-µF capacitor is added close to the BIAS pin.
- FB is connected to the output through a voltage divider in order to create a voltage of 1 V at the FB pin when the output is at 6 V. A 22-pF capacitance is added in parallel with the top feedback resistor in order to improve transient behavior. BIAS and FB are connected to the output through separate traces. This is important to reduce noise and achieve good performances. See 节 *11.1* for more details on the proper layout method.
- SYNC is connected to ground directly as there is no need for this function in this application.
- EN is toggled by an external device (like an MCU for example). A pulldown resistor is placed to ensure the part does not turn on if the external source is not driving the pin (Hi-Z condition).
- FPWM is connected to VIN. This causes the device to operate in FPWM mode. To prevent frequency foldback behavior at low duty cycles, provide a 200mA load. In this mode, the device remains in CCM operation regardless of the output current and is ensured to be within the boundaries set by F_{SW}. The drawback is that the efficiency is not optimized for light loads. See 节 *8.4* for more details.
- A 4.7-µF capacitor is connected between VCC and GND close to the VCC pin. This ensure stable operation of the internal LDO.
- $\overline{\text{RESET}}$ is not used in this example so the pin has been left floating. Other possible connections can be seen in the previous typical applications and in 节 *8.3.1*.
- Power components (input capacitor, output capacitor, and inductor) selection can be found here in 节 *9.2.1.2.2*.

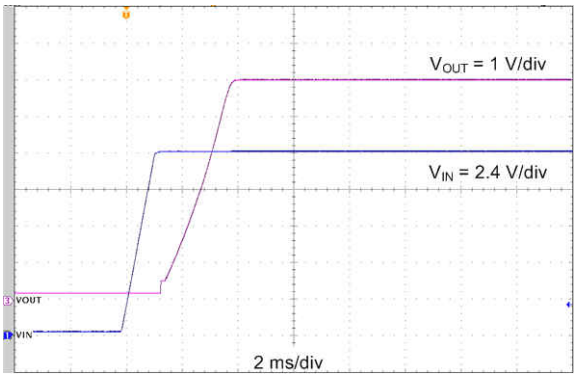
9.2.4.3 Application Curves

The following characteristics apply only to the circuit of 图 9-30. *These parameters are not tested and represent typical performance only.* Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, T_A = 25°C.



V_{OUT} = 6 V (ADJ part) FPWM I_{OUT} = 0 A

图 9-31. Start-Up Waveform



V_{OUT} = 6 V (ADJ part) FPWM I_{OUT} = 0 A

图 9-32. Start-Up Waveform (EN Tied to VIN)

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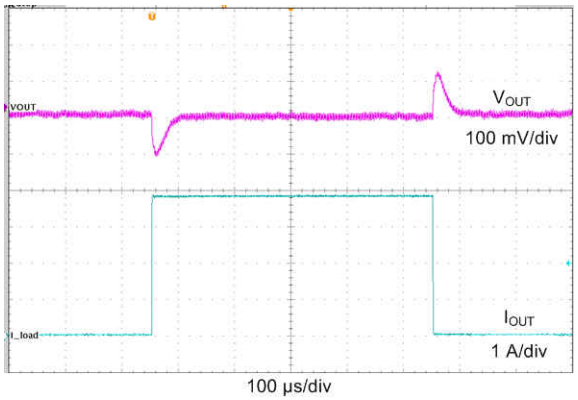

FPWM V_{OUT} = 6 V (ADJ) L = 10 µH,
C_{OUT} = 190 µF I_{OUT} = 0 A to 3.5 A $T_R = T_F$ = 1 µs

图 9-33. Load Transient

9.3 Do's and Don't's

- **Don't:** Exceed the 节 7.1.
- **Don't:** Exceed the 节 7.3.
- **Don't:** Allow the EN, FPWM or SYNC input to float.
- **Don't:** Allow the output voltage to exceed the input voltage, nor go below ground.
- **Don't:** Use the thermal data given in the 节 7.4 table to design your application.
- **Do:** Follow all of the guidelines and/or suggestions found in this data sheet before committing a design to production. TI Application Engineers are ready to help critique designs and PCB layouts to help ensure successful projects.
- **Do:** Refer to the helpful documents found in 节 12.2.1.

10 Power Supply Recommendations

The characteristics of the input supply must be compatible with the 节 7.1 and 节 7.3 found in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with 方程式 6:

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \tag{6}$$

where

- η is the efficiency

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR ceramic input capacitors, can form an under-damped resonant circuit. This circuit may cause overvoltage transients at the VIN pin, each time the input supply is cycled on and off. The parasitic resistance causes the voltage at the VIN pin to dip when the load on the regulator is switched on or exhibits a transient. If the regulator is operating close to the minimum input voltage, this dip may cause the device to shut down or reset. The best way to solve these kinds of issues is to reduce the distance from the input supply to the regulator or use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of these types of capacitors helps to damp the input resonant circuit and reduce any voltage overshoots. A value in the range of 20 µF to 100 µF is usually sufficient to provide input damping and help to hold the input voltage steady during large load transients.

Sometimes, for other system considerations, an input filter is used in front of the regulator. This can lead to instability, as well as some of the effects mentioned above, unless it is designed carefully. *LP3913 Power Management IC for Flash Memory Based Portable Media Players* (SNVA489) provides helpful suggestions when designing an input filter for any switching regulator.

In some cases a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a *snap-back* V-I characteristic (thyristor type). The use of a device with this type of characteristic is not recommend. When the TVS fires, the clamping voltage drops to a very low value. If this holding voltage is less than the output voltage of the regulator, the output capacitors are discharged through the regulator back to the input. This uncontrolled current flow could damage the regulator.

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11 Layout

11.1 Layout Guidelines

The PCB layout of a DC-DC converter is critical for optimal performance of the application. For a buck converter the input loop formed by the input capacitors and power grounds are very critical. The input loop carries fast transient currents that cause larger transient voltages when reacting with a parasitic loop inductance. The IC uses two input loops in parallel IN1 and IN2 as shown in 图 11-1 that cuts the parasitic input inductance in half. To get the minimum input loop area two small high frequency capacitors CIN1 and CIN2 are placed as close as possible.

To further reduce inductance, an input current return path should be placed underneath the loops IN1 and IN2. The closest metal plane is MID1 Layer2, and there is a solid copper plane placed right under the IN1 and IN2 loop the parasitic loop inductance is minimized. Connecting this MID1 Layer2 plane to GND provides a nice bridge connection between GND1 and GND2 as well. Minimizing the parasitic input loop inductance will minimize switch node ringing and EMI.

The output current loop can be optimized as well by using two ceramic output caps COUT1 and COUT2, one on each side. They form two parallel ground return paths OUT1 from COUT1 back to the low-side FET PGND1 pins 5, 6, 7, 8, and a second symmetric ground return path OUT2 from COUT2 back to low-side FET PGND2 pins 10, 11, 12, and 13. Having two parallel ground return paths yield reduced ground bouncing and reduced sensitivity of surrounding circuits.

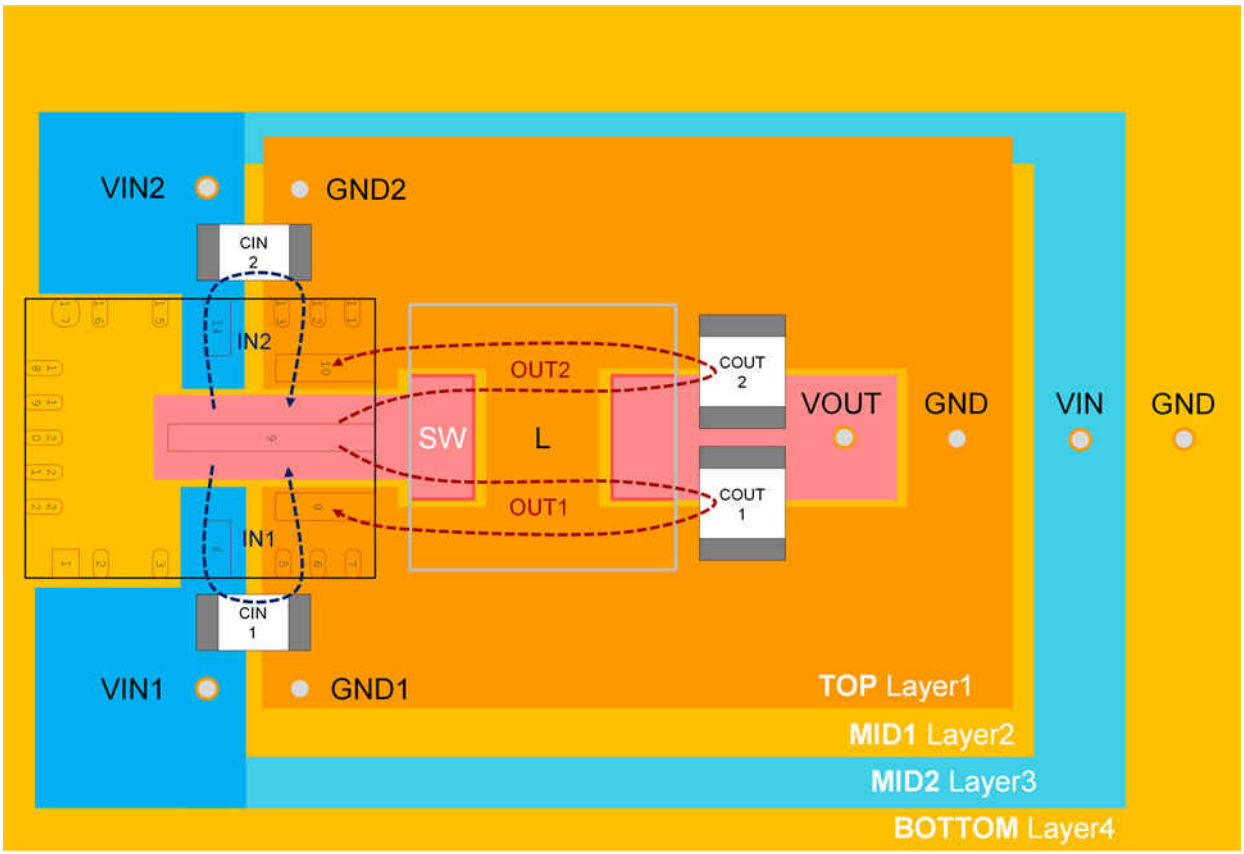

图 11-1. Layout of the Power Components and Current Flow

Providing adequate thermal paths to dissipate heat is critical for operation at full current. The recommended method for heat dissipation is to use large solid 2-oz copper planes well connected to the power pins VIN1, VIN2, GND1, and GND2 which transfer the heat out of the IC over the TOP Layer1 copper planes. It is important to leave the TOP Layer1 copper planes as unbroken as possible so that heat is not trapped near the IC. The heat flow can be further optimized by thermally connecting the TOP Layer1 plane to large BOTTOM Layer 4 2-oz

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copper planes with vias. MID2 Layer3 is then open for all other signal routing. A fully filled or solid BOTTOM Layer4 ground plane without any interruptions or ground splitting is beneficial for EMI as well. Most important for low EMI is to use the smallest possible switch node copper area. The switch node including the C_{BOOT} cap has the largest dV/dt signal causing common-mode noise coupling. Using any kind of grounded shield around the switch node *shortens* and reduces this e-field.

All these DC-DC converter descriptions can be transformed into layout guidelines:

1. Place two 0.047-µF, 50-V high frequency input capacitors C_{IN1} and C_{IN2} as close as possible to the VIN1, VIN2, PGND1, PGND2 pins to minimize switch node ringing.
2. Place bypass capacitors for VCC and BIAS close to their respective pins. Make sure AGND pin *sees* the C_{VCC} and C_{BIAS} capacitors first before a connection to PGND.
3. Place C_{BOOT} capacitor with smallest parasitic loop. Shielding the C_{BOOT} capacitor and switch node has the biggest impact to reduce common-mode noise. Placing a small R_{BOOT} resistor (less than 3 Ω is recommended) in series to C_{BOOT} slows down the dV/dt of the switch node and reduce EMI.
4. Place the feedback resistor divider for adjustable parts as close as possible to the FB pin and to AGND pin of the device. Use a dedicated feedback trace, and route away from switch node and C_{BOOT} capacitor to avoid any cross coupling into sensitive analog feedback.
5. Use a dedicated BIAS trace to avoid noise into feedback trace.
6. Use a 3-Ω to 5-Ω resistor between the output and BIAS if the load is far from the output of the converter or inductive shorts on the output are possible.
7. Use well connected large 2-oz. TOP and BOTTOM copper planes for all power pins VIN1/2 and PGND1/2.
8. Minimize switch node and C_{BOOT} area for lowest EMI common mode noise.
9. Place input and output wires on the same side of the PCB using an EMI filter and away from the switch node for lowest EMI.

The resources in 节 12 provide additional important guidelines.

11.2 Layout Example

This example layout is the one used in the LMS36x5-Q1 EVM. It shows the C_{IN} and C_{IN_HF} capacitors placed symmetrically on either side of the device.

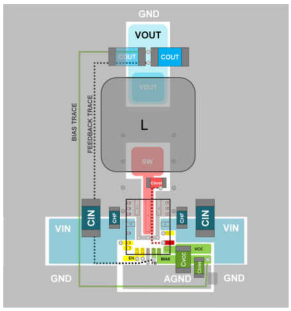

图 11-2. Recommended Layout for LMS36x5-Q1

The evaluation module solution size is 17.8 mm by 43.2 mm. This is a typical of an automotive layout, as pictured in 图 11-3.

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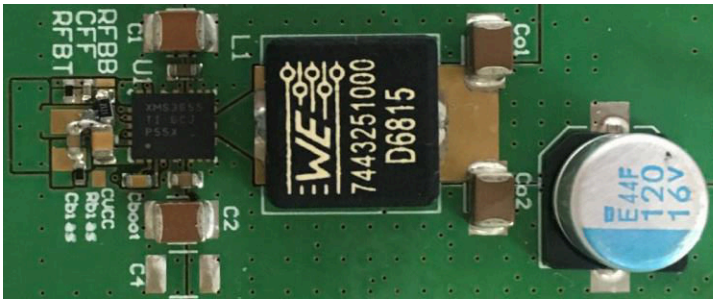

图 11-3. LMS3655MQEVM Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 第三方产品免责声明

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12.1.2 Development Support

12.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMS3635-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

12.2 Documentation Support

12.2.1 Related Documentation

For additional information, see the following:

- *Optimizing Transient Response of Internally Compensated DC-DC Converters With Feedforward Capacitor* (SLVA289)
- *Output Ripple Voltage for Buck Switching Regulator* (SLVA630)
- *AN-1149 Layout Guidelines for Switching Power Supplies* (SNVA021)
- *AN-1229 Simple Switcher® PCB Layout Guidelines* (SNVA054)
- *Constructing Your Power Supply- Layout Considerations* (SLUP230)
- *AN-2020 Thermal Design By Insight, Not Hindsight* (SNVA419)
- *Semiconductor and IC Package Thermal Metrics* (SPRA953)

12.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMS36353QRNLRQ1	ACTIVE	VQFN-HR	RNL	22	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	LM36353	Samples
LMS36353QRNLTQ1	ACTIVE	VQFN-HR	RNL	22	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	LM36353	Samples
LMS36355QRNLRQ1	ACTIVE	VQFN-HR	RNL	22	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	LM36355	Samples
LMS36355QRNLTQ1	ACTIVE	VQFN-HR	RNL	22	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	LM36355	Samples
LMS3635AQRNLRQ1	ACTIVE	VQFN-HR	RNL	22	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	LM3635A	Samples
LMS3635AQRNLTQ1	ACTIVE	VQFN-HR	RNL	22	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	LM3635A	Samples
LMS3635LQRNLRQ1	ACTIVE	VQFN-HR	RNL	22	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	LM3635L	Samples
LMS3635LQRNLTQ1	ACTIVE	VQFN-HR	RNL	22	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	LM3635L	Samples
LMS3635LQURNLRQ1	ACTIVE	VQFN-HR	RNL	22	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	UM3635L	Samples
LMS3635MQRNLRQ1	ACTIVE	VQFN-HR	RNL	22	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	LM3635M	Samples
LMS3635MQRNLTQ1	ACTIVE	VQFN-HR	RNL	22	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	LM3635M	Samples
LMS3635MQURNLRQ1	ACTIVE	VQFN-HR	RNL	22	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	UM3635M	Samples
LMS3635NQRNLRQ1	ACTIVE	VQFN-HR	RNL	22	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	LM3635N	Samples
LMS3635NQRNLTQ1	ACTIVE	VQFN-HR	RNL	22	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	LM3635N	Samples
LMS36553QRNLRQ1	ACTIVE	VQFN-HR	RNL	22	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	LM36553	Samples
LMS36553QRNLTQ1	ACTIVE	VQFN-HR	RNL	22	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	LM36553	Samples
LMS36555QRNLRQ1	ACTIVE	VQFN-HR	RNL	22	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	LM36555	Samples
LMS36555QRNLTQ1	ACTIVE	VQFN-HR	RNL	22	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	LM36555	Samples
LMS3655AQRNLRQ1	ACTIVE	VQFN-HR	RNL	22	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	LM3655A	Samples
LMS3655AQRNLTQ1	ACTIVE	VQFN-HR	RNL	22	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	LM3655A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMS3655LQRNLRQ1	ACTIVE	VQFN-HR	RNL	22	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	LM3655L	Samples
LMS3655LQRNLTQ1	ACTIVE	VQFN-HR	RNL	22	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	LM3655L	Samples
LMS3655MQRNLRQ1	ACTIVE	VQFN-HR	RNL	22	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	LM3655M	Samples
LMS3655MQRNLTQ1	ACTIVE	VQFN-HR	RNL	22	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	LM3655M	Samples
LMS3655MQURNLRQ1	ACTIVE	VQFN-HR	RNL	22	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	UM3655M	Samples
LMS3655NQRNLRQ1	ACTIVE	VQFN-HR	RNL	22	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	LM3655N	Samples
LMS3655NQRNLTQ1	ACTIVE	VQFN-HR	RNL	22	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	LM3655N	Samples
LMS3655NQURNLRQ1	ACTIVE	VQFN-HR	RNL	22	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 150	UM3655N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LMS3655-Q1 :

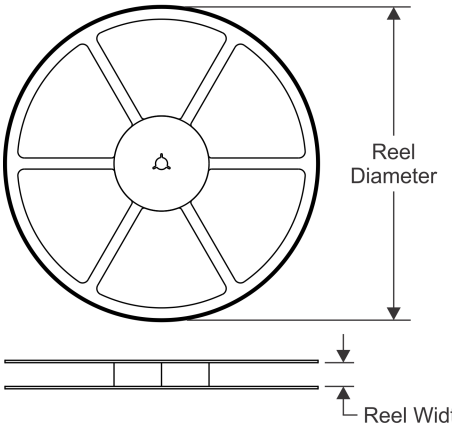
- Catalog : LMS3655

NOTE: Qualified Version Definitions:

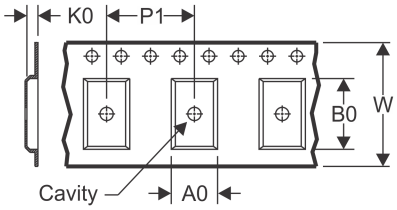
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

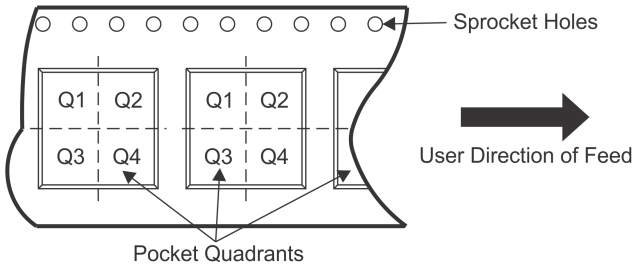


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

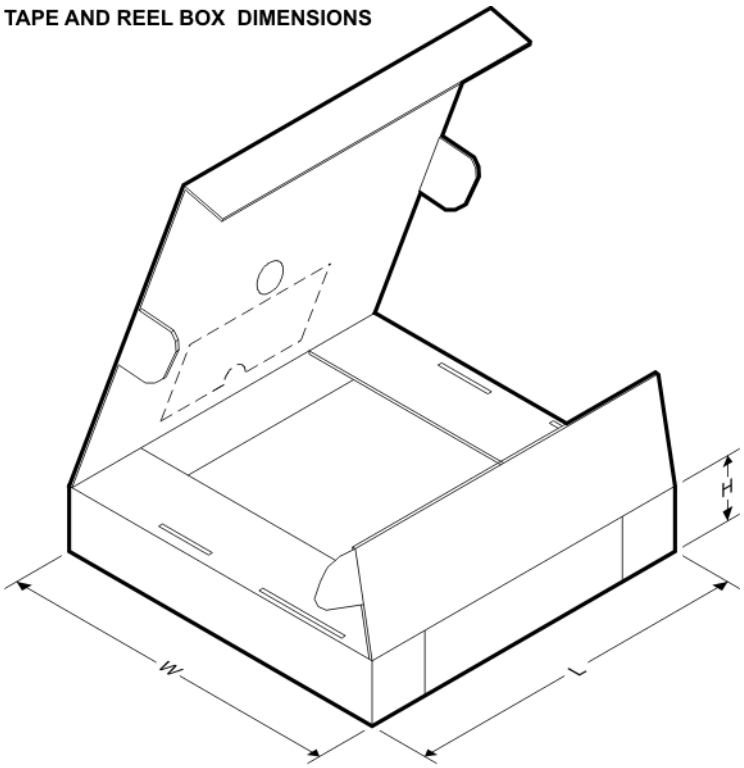
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMS3635LQURNLRQ1	VQFN-HR	RNL	22	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LMS3635MQURNLRQ1	VQFN-HR	RNL	22	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LMS3655MQURNLRQ1	VQFN-HR	RNL	22	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LMS3655NQURNLRQ1	VQFN-HR	RNL	22	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMS3635LQURNLRQ1	VQFN-HR	RNL	22	3000	367.0	367.0	38.0
LMS3635MQURNLRQ1	VQFN-HR	RNL	22	3000	367.0	367.0	38.0
LMS3655MQURNLRQ1	VQFN-HR	RNL	22	3000	367.0	367.0	38.0
LMS3655NQURNLRQ1	VQFN-HR	RNL	22	3000	367.0	367.0	38.0

GENERIC PACKAGE VIEW

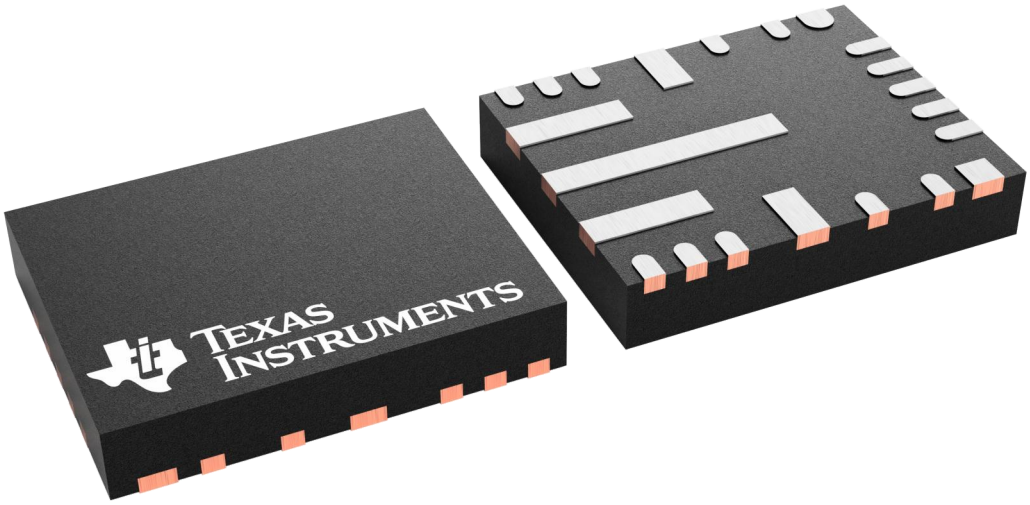
RNL 22

VQFN-HR - 1 mm max height

5 X 4, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



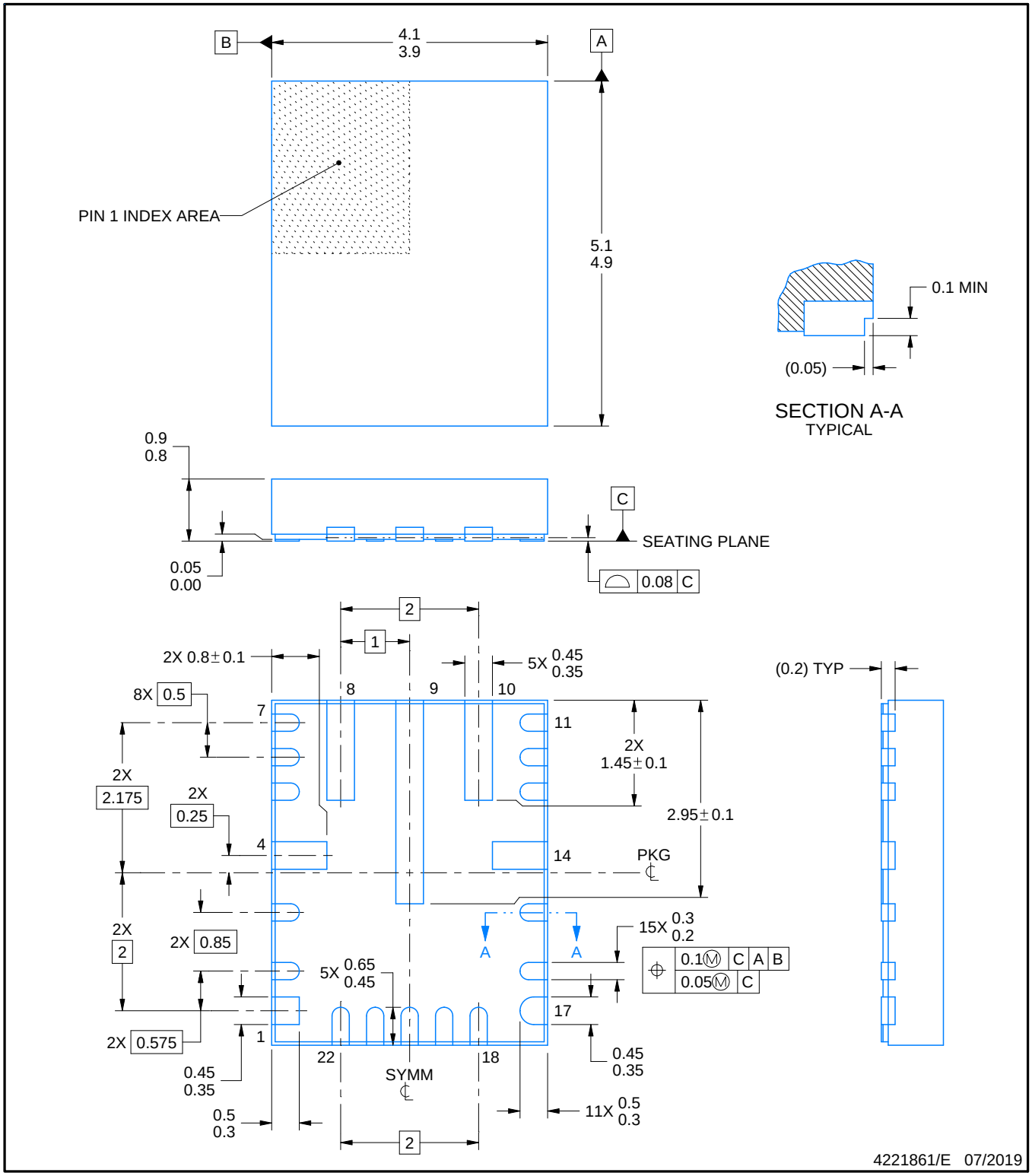
4226989/A

PACKAGE OUTLINE

RNL0022A

VQFN-HR - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

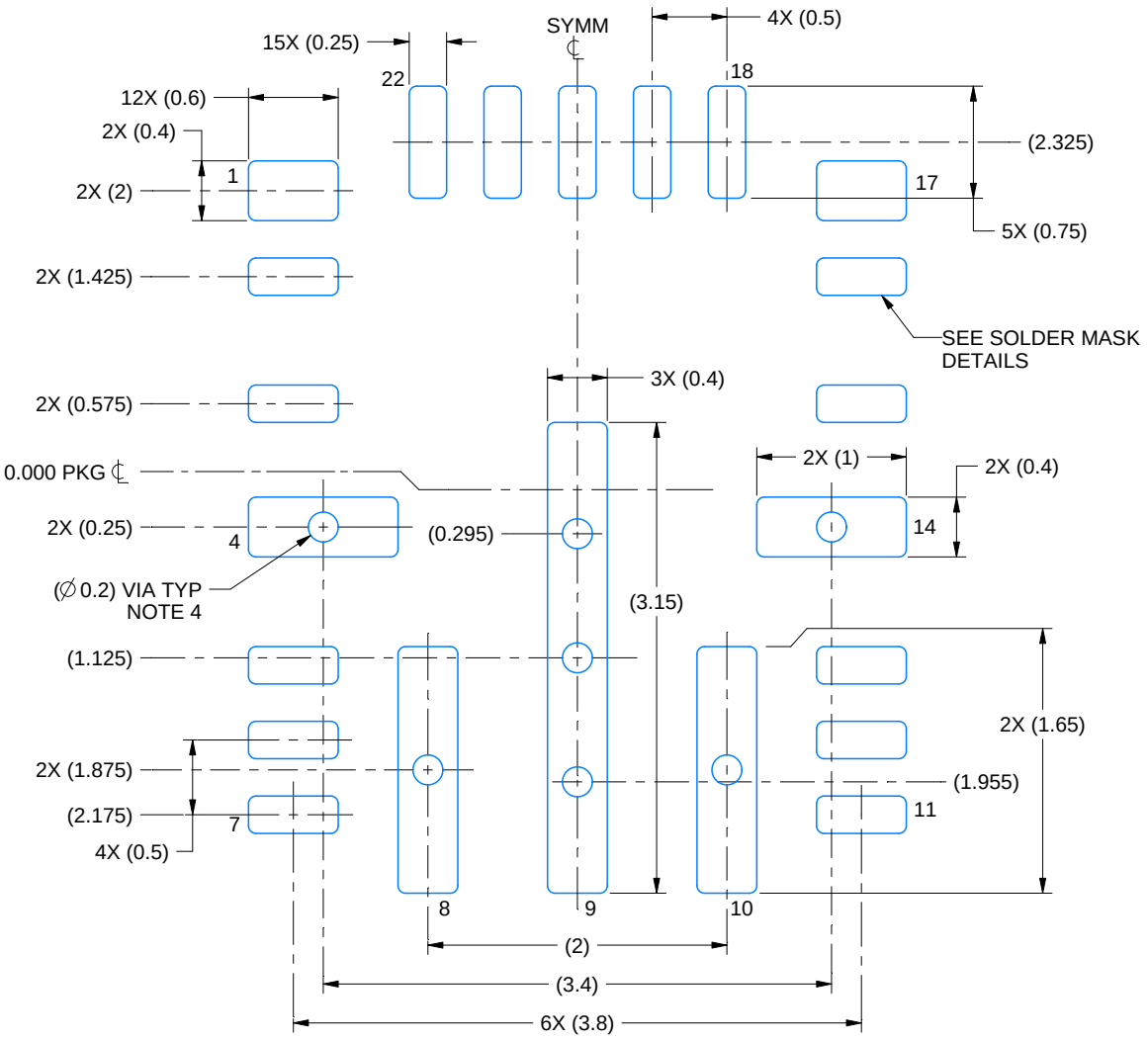
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

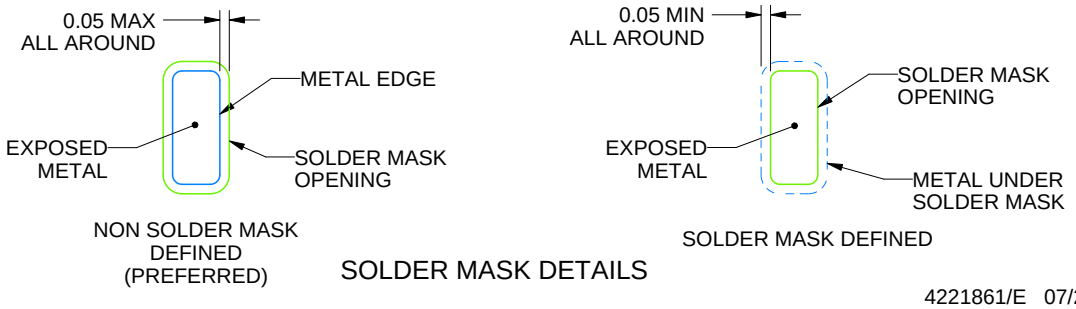
RNL0022A

VQFN-HR - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4221861/E 07/2019

NOTES: (continued)

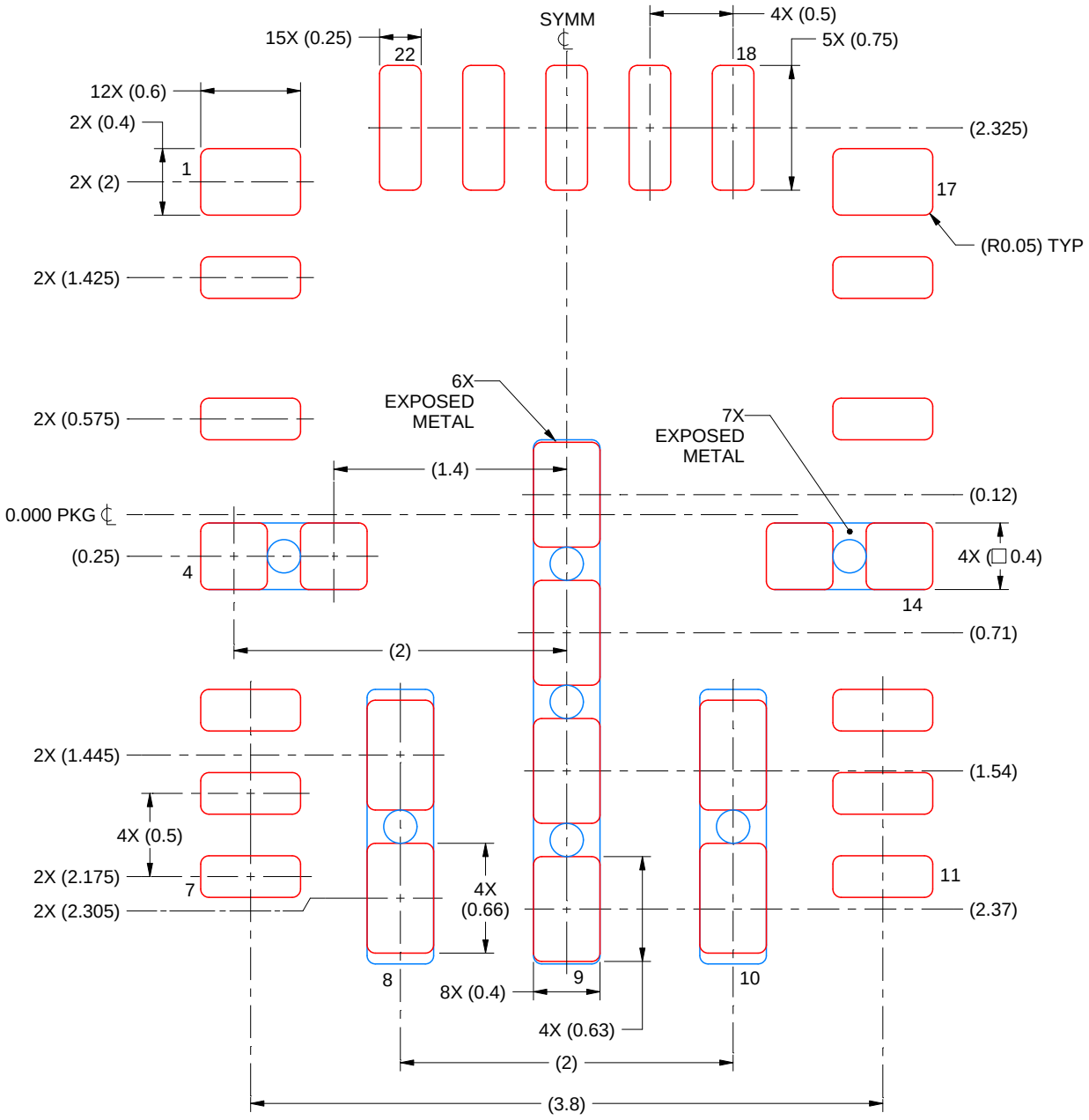
3. This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RNL0022A

VQFN-HR - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

FOR PADS 4,8,9,10 & 14
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4221861/E 07/2019

NOTES: (continued)

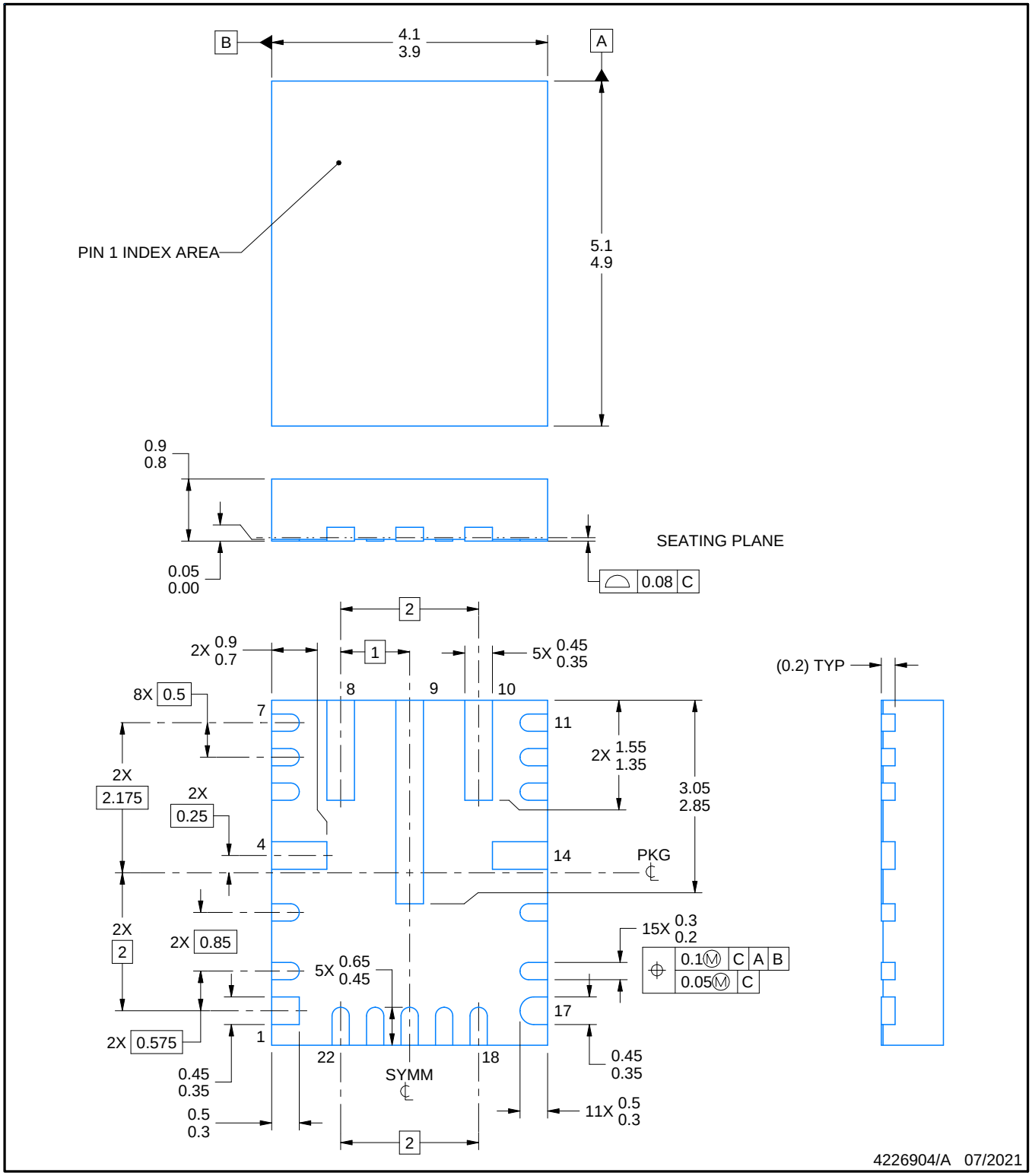
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

RNL0022B

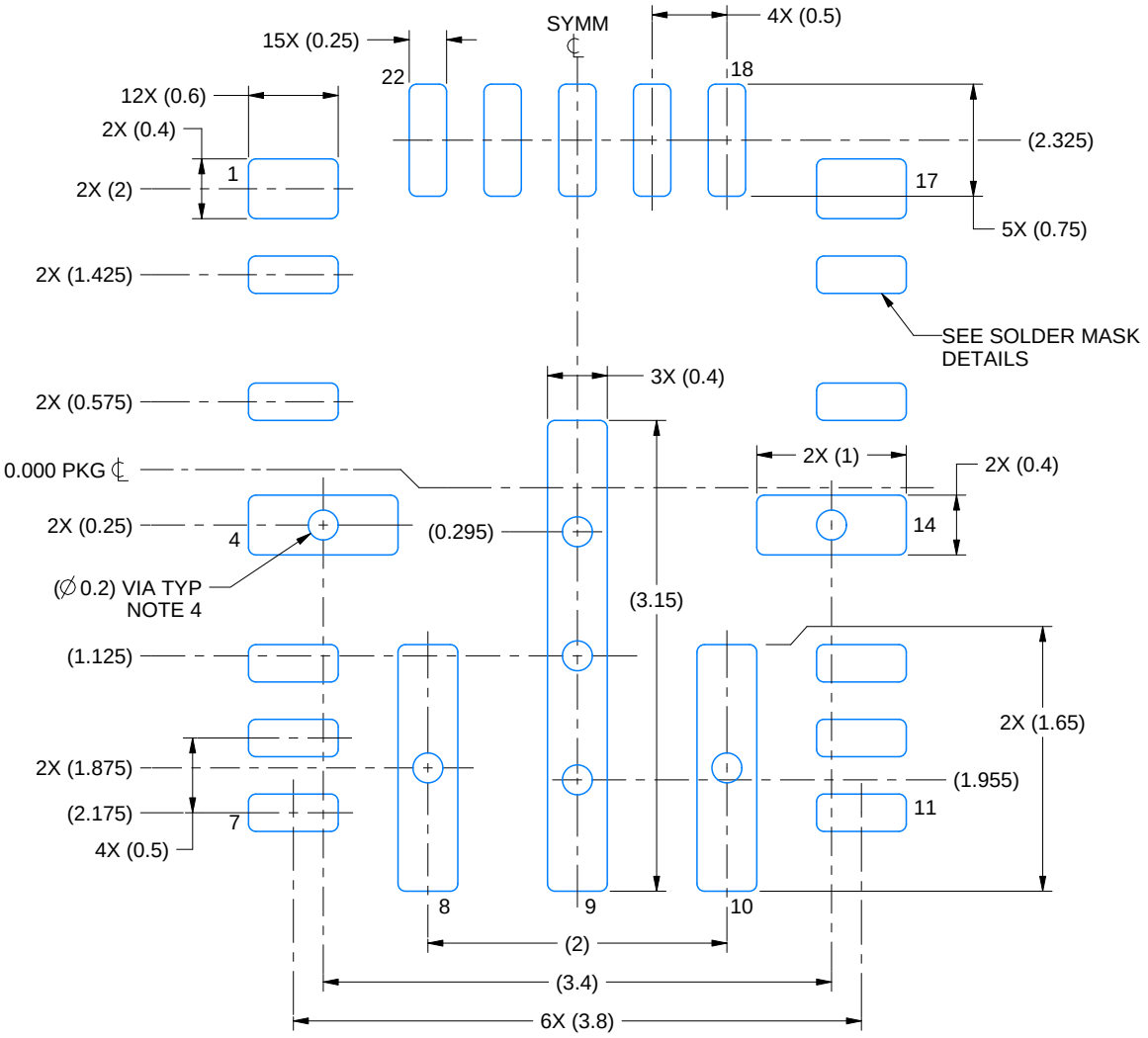
VQFN-HR - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

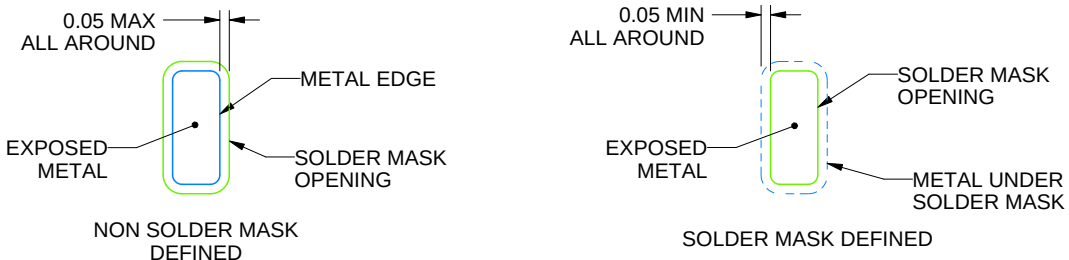


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4226904/A 07/2021

NOTES: (continued)

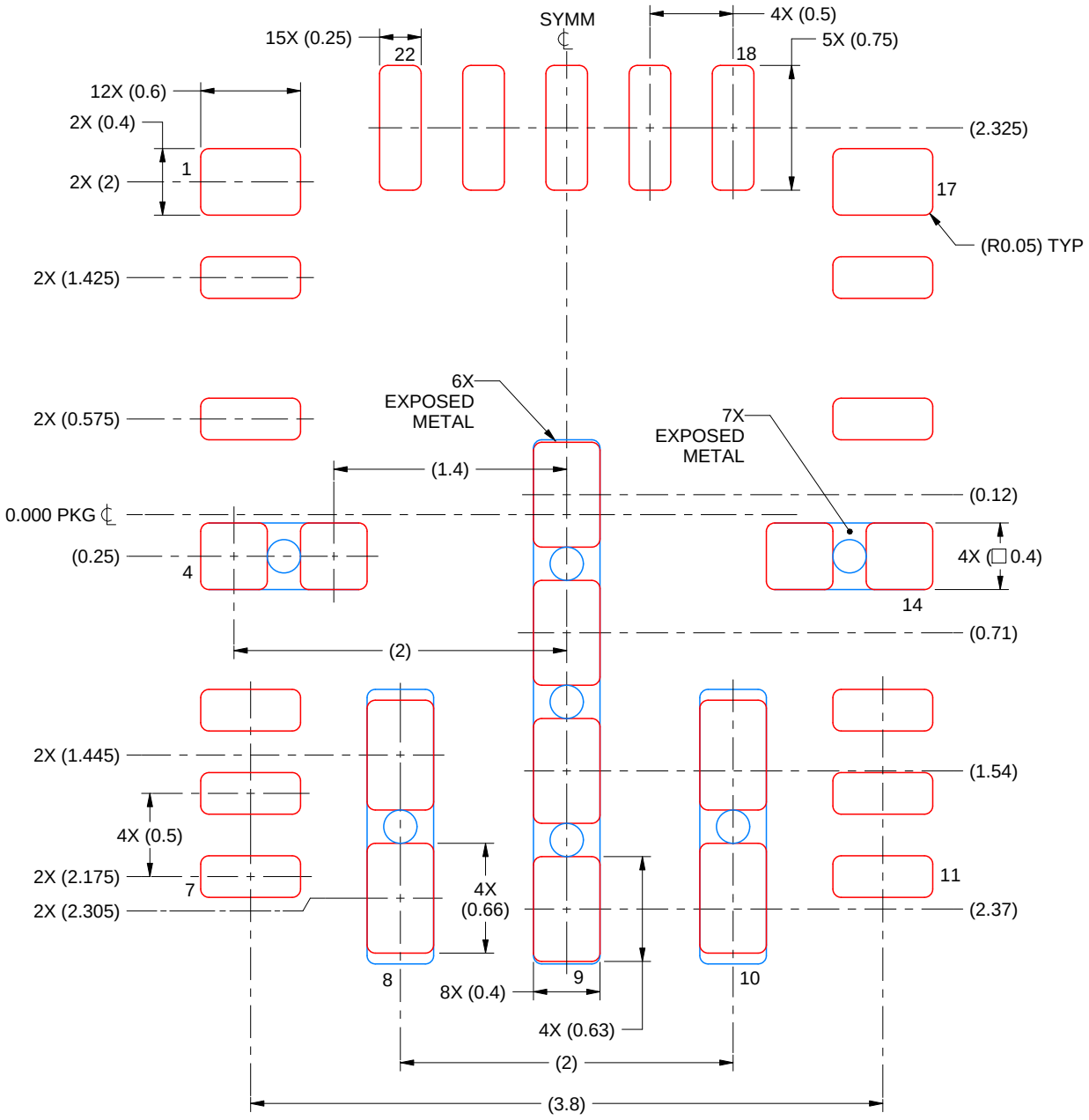
3. This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RNL0022B

VQFN-HR - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

FOR PADS 4,8,9,10 & 14
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4226904/A 07/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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