LP396x 800-mA Fast Ultra-Low-Dropout Linear Regulators

1 Features

- Input Supply Voltage: 2.5 V to 7 V
- Ultra-Low Dropout Voltage
- Low Ground Pin Current
- Load Regulation of 0.02%
- 15-µA Quiescent Current in Shutdown Mode
- Specified Output Current of 0.8-A DC
- Output Voltage Accuracy ±1.5%
- $\overline{\text{ERROR}}$ Flag Indicates Output Status (LP3961)
- Sense Option Improves Better Load Regulation (LP3964)
- Extremely Low Output Capacitor Requirements
- Overtemperature and Overcurrent Protection
- −40°C to 125°C Junction Temperature Range

2 Applications

- Microprocessor Power Supplies
- GTL, GTL+, BTL, and SSTL Bus Terminators
- Power Supplies for DSPs
- SCSI Terminator
- Post Regulators
- High-Efficiency Linear Regulators
- Battery Chargers
- Other Battery-Powered Applications

3 Description

The LP396x series of fast ultra-low-dropout linear regulators operate from a 2.5-V to 7-V input supply. A wide range of preset output voltage options are available. These ultra-low dropout linear regulators respond very fast to step changes in load which makes them suitable for low-voltage microprocessor applications. The LP3961 and LP3964 are developed on a CMOS process which allows low quiescent current operation independent of output load current, as well as operation under extremely low dropout conditions.

Dropout Voltage: Ultra-low dropout voltage; typically 24 mV at 80-mA load current and 240 mV at 800-mA load current.

Ground Pin Current: Typically 4 mA at 800-mA load current.

$\overline{\text{ERROR}}$ Flag: $\overline{\text{ERROR}}$ flag goes low when the output voltage drops 10% below nominal value (for LP3961).

SENSE: SENSE pin improves regulation at remote loads (for LP3964).

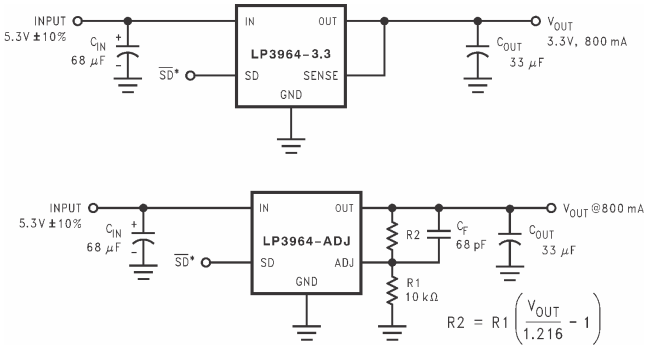
Precision Output Voltage: Multiple output voltage options are available ranging from 1.2 V to 5 V and adjustable (LP3964), with a specified accuracy of ±1.5% at room temperature, and ±3% over all conditions (varying line, load, and temperature).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP3961 LP3964	SOT-223 (5)	6.50 mm × 3.56 mm
	TO-263 (5)	10.16 mm × 8.42 mm
LP3964	TO-220 (5)	14.986 mm × 10.16 mm

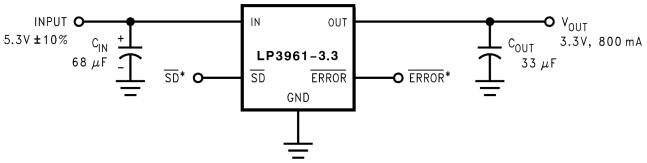
(1) For all available packages, see the orderable addendum at the end of the data sheet.

LP3964 Typical Application Circuits



*See note A on *LP3961 Typical Application Circuit*.

LP3961 Typical Application Circuit



A. *$\overline{\text{SD}}$ and $\overline{\text{ERROR}}$ pins must be pulled high through a 10-kΩ pullup resistor. Connect the $\overline{\text{ERROR}}$ pin to ground if this function is not used.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configurations and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Typical Characteristics ... 7
7 Detailed Description ... 10
7.1 Overview ... 10
7.2 Functional Block Diagram ... 10
7.3 Feature Description ... 11
7.4 Device Functional Modes ... 13
8 Application and Implementation ... 14
8.1 Application Information ... 14
8.2 Typical Applications ... 14
9 Power Supply Recommendations ... 19
10 Layout ... 19
10.1 Layout Guidelines ... 19
10.2 Layout Example ... 19
10.3 Heatsinking TO-220 Packages ... 20
11 Device and Documentation Support ... 21
11.1 Related Links ... 21
11.2 Community Resources ... 21
11.3 Trademarks ... 21
11.4 Electrostatic Discharge Caution ... 21
11.5 Glossary ... 21
12 Mechanical, Packaging, and Orderable Information ... 21

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (December 2014) to Revision J — **Page**

- Changed pin names to conform to TI nomenclature (V_{OUT} to OUT, V_{IN} to IN) ... 1
- Changed "I" to "O" to correct I/O type for $\overline{\text{ERROR}}$ flag ... 3
- Deleted Lead temperature row - info in POA ... 4
- Deleted heatsinking sections re TO-263 and SOT-223 packages; not consistent with updated thermal metrics ... 20

Changes from Revision H (April 2013) to Revision I — **Page**

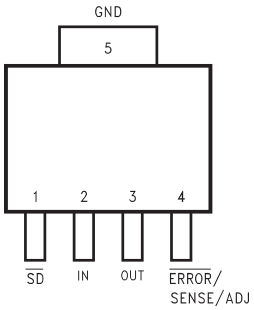
- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision G (April 2013) to Revision H — **Page**

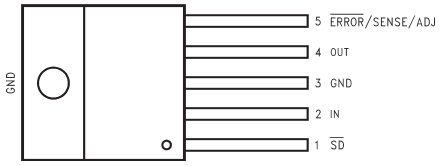
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5 Pin Configurations and Functions

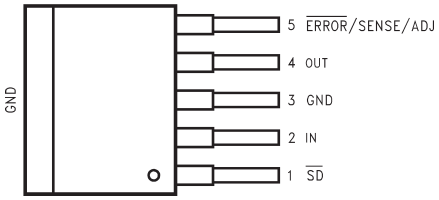
5-Pin NDC
SOT-223 Package
Top View



5-Pin NDH
TO-220 Package (LP3964)
Top View



5-Pin KTT
SFM/TO-263 Package
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	NO.				
	LP3961	LP3964			
		SOT-223	TO-220 SFM/TO-263		
$\overline{\text{ERROR}}$	4	—	—	O	$\overline{\text{ERROR}}$ flag
GND	5	5	3	—	Ground
IN	2	2	2	I	Input supply
OUT	3	3	4	O	Output voltage
$\overline{\text{SD}}$	1	1	1	I	Shutdown
SENSE/ADJ	—	4	5	I	Remote sense pin or output adjust pin

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6 Specifications

6.1 Absolute Maximum Ratings[1][2]

	MIN	MAX	UNIT
Power dissipation[3]	Internally Limited		
Input Supply Voltage (Survival)	−0.3	7.5	V
Shutdown Input Voltage (Survival)	−0.3	V_{IN} + 0.3	V
Output Voltage (Survival)[4], [5]	−0.3	7.5	V
I_{OUT} (Survival)	Short-Circuit Protected		
Maximum Voltage for $\overline{\text{ERROR}}$ pin		V_{IN} + 0.3	V
Maximum Voltage for SENSE pin		V_{OUT} + 0.3	V
Storage temperature, T_{stg}	–65	150	°C

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. *Recommended Operating Conditions* indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and test conditions, see *Electrical Characteristics*. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) If Military- or Aerospace-specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{(MAX)} = (T_{J(MAX)} – T_A) / R_{\theta JA}$.
(4) If used in a dual-supply system where the regulator load is returned to a negative supply, the LP396X output must be diode-clamped to ground.
(5) The output PMOS structure contains a diode between the IN and OUT pins. This diode is normally reverse biased. This diode will get forward biased if the voltage at the OUT pin is forced to be higher than the voltage at the IN pin. This diode can typically withstand 200 mA of DC current and 1 A of peak current.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process..

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Input supply voltage (operating)[1]	2.5	7	V
Shutdown input voltage (operating)	−0.3	V_{IN} + 0.3	V
Maximum operating current (DC)		0.8	A
Operating junction temperature	−40	125	°C

(1) The minimum operating value for V_{IN} is equal to either [$V_{OUT(NOM)}$ + $V_{DROPOUT}$] or 2.5 V, whichever is greater.

6.4 Thermal Information

THERMAL METRIC[1]		LP3961, LP3964		LP3964	UNIT
		NDC	KTT	NDH	
		5 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.2	40.3	32.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.2	43.4	43.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	9.9	23.1	18.7	
ψ_{JT}	Junction-to-top characterization parameter	3.4	11.5	8.8	
ψ_{JB}	Junction-to-board characterization parameter	9.7	22.1	18.0	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	1.0	1.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

Unless otherwise specified: T_J = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, I_L = 10 mA, C_{OUT} = 33 µF, V_{SD} = V_{IN} – 0.3 V.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
V_O	Output voltage tolerance(3)	10 mA ≤ I_L ≤ 800 mA, V_{OUT} + 1 ≤ V_{IN} ≤ 7 V	–1.5%	0%	1.5%	
		10 mA ≤ I_L ≤ 800 mA, V_{OUT} + 1 ≤ V_{IN} ≤ 7 V, –40°C ≤ T_J ≤ 125°C	–3%		3%	
V_{ADJ}	Adjust pin voltage (ADJ version)	10 mA ≤ I_L ≤ 800 mA, V_{OUT} + 1.5 V ≤ V_{IN} ≤ 7 V	1.198	1.216	1.234	V
		10 mA ≤ I_L ≤ 800 mA, V_{OUT} + 1.5 V ≤ V_{IN} ≤ 7 V, –40°C ≤ T_J ≤ 125°C	1.180		1.253	
ΔV_{OL}	Output voltage line regulation(3)	V_{OUT} + 1 V < V_{IN} < 7 V		0.02%		
		V_{OUT} + 1 V < V_{IN} < 7 V, –40°C ≤ T_J ≤ 125°C		0.06%		
ΔV_O / ΔI_{OUT}	Output voltage load regulation(3)	10 mA < I_L < 800 mA		0.02%		
		10 mA < I_L < 800 mA, –40°C ≤ T_J ≤ 125°C		0.08%		
$V_{IN} – V_{OUT}$	Dropout voltage(4)	I_L = 80 mA		24	30	mV
		I_L = 80 mA, –40°C ≤ T_J ≤ 125°C			35	
		I_L = 800 mA		240	300	
		I_L = 800 mA, –40°C ≤ T_J ≤ 125°C			350	
I_{GND}	Ground pin current in normal operation mode	I_L = 80 mA		3	9	mA
		I_L = 80 mA, –40°C ≤ T_J ≤ 125°C			10	
		I_L = 800 mA		4	14	
		I_L = 800 mA, –40°C ≤ T_J ≤ 125°C			15	
I_{GND}	Ground pin current in shutdown mode(5)	V_{SD} ≤ 0.2 V		15	25	µA
		V_{SD} ≤ 0.2 V, –40°C ≤ T_J ≤ 125°C			75	
$I_{O(PK)}$	Peak output current	See(6)	1.2	1.5		A
		See(6), –40°C ≤ T_J ≤ 125°C	1.1			
SHORT-CIRCUIT PROTECTION						
I_{SC}	Short-circuit current			2.8		A
OVERTEMPERATURE PROTECTION						
Tsh(t)	Shutdown threshold			165		°C
Tsh(h)	Thermal shutdown hysteresis			10		°C
SHUTDOWN INPUT						
V_{SDT}	Shutdown threshold	Output = High		V_{IN}		V
		Output = High, –40°C ≤ T_J ≤ 125°C	V_{IN} – 0.3			
		Output = Low		0		
		Output = Low, –40°C ≤ T_J ≤ 125°C			0.2	

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate TI's Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely parametric norm.
(3) Output voltage line regulation is defined as the change in output voltage from the nominal value due to change in the input line voltage. Output voltage load regulation is defined as the change in output voltage from the nominal value due to change in load current. The line and load regulation specification contains only the typical number. However, the limits for line and load regulation are included in the output voltage tolerance specification.
(4) Dropout voltage is defined as the minimum input-to-output differential voltage at which the output drops 2% below the nominal value. Dropout voltage specification applies only to output voltages of 2.5 V and above. For output voltages below 2.5 V, the drop-out voltage is nothing but the input-to-output differential voltage because the minimum input voltage is 2.5 V.
(5) This specification has been tested for –40°C ≤ T_J ≤ 85°C because the temperature rise of the device is negligible under shutdown conditions.
(6) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{(MAX)} = (T_{J(MAX)} – T_A) / R_{\theta JA}$.

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Electrical Characteristics (continued)

Unless otherwise specified: T_J = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, I_L = 10 mA, C_{OUT} = 33 µF, V_{SD} = V_{IN} – 0.3 V.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
T_{dOFF}	Turnoff delay	I_L = 800 mA		20		µs
T_{dON}	Turnon delay	I_L = 800 mA		25		µs
I_{SD}	$\overline{SD}$ input current	V_{SD} = V_{IN}		1		nA
ERROR FLAG COMPARATOR						
V_T	Threshold	See(7)		10%		
		See(7), –40°C ≤ T_J ≤ 125°C	5%		16%	
V_{TH}	Threshold hysteresis	See(7)		5%		
		See(7), –40°C ≤ T_J ≤ 125°C	2%		8%	
$V_{EF(Sat)}$	$\overline{ERROR}$ flag saturation	I_{sink} = 100 µA		0.02		V
		I_{sink} = 100 µA			0.1	
T_d	Flag reset delay			1		µs
I_{lk}	$\overline{ERROR}$ flag pin leakage current			1		nA
I_{max}	$\overline{ERROR}$ flag pin sink current	V_{ERROR} = 0.5 V (overtemperature)		1		mA
AC PARAMETERS						
PSRR	Ripple rejection	V_{IN} = V_{OUT} + 1.5 V, C_{OUT} = 100 µF, V_{OUT} = 3.3 V		60		dB
		V_{IN} = V_{OUT} + 0.3 V, C_{OUT} = 100 µF, V_{OUT} = 3.3 V		40		
$\rho_{n(l/f)}$	Output noise density	f = 120 Hz		0.8		µV
e_n	Output noise voltage (rms)	BW = 10 Hz to 100 kHz		150		μV_{RMS}
		BW = 300 Hz to 300 kHz		100		

(7) $\overline{ERROR}$ flag threshold and hysteresis are specified as percentage of regulated output voltage.

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6.6 Typical Characteristics

Unless otherwise specified, $V_{IN} = V_{O(NOM)} + 1$ V, $V_{OUT} = 2.5$ V, $C_{OUT} = 33$ µF, $I_{OUT} = 10$ mA, $C_{IN} = 68$ µF, $V_{SDT} = V_{IN}$, and $T_A = 25°C$.

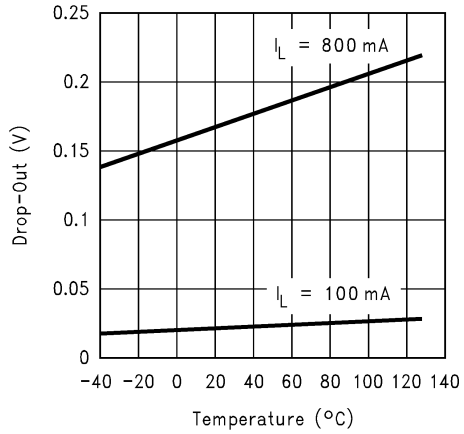


Figure 1. Drop-Out Voltage vs Temperature for Different Load Currents

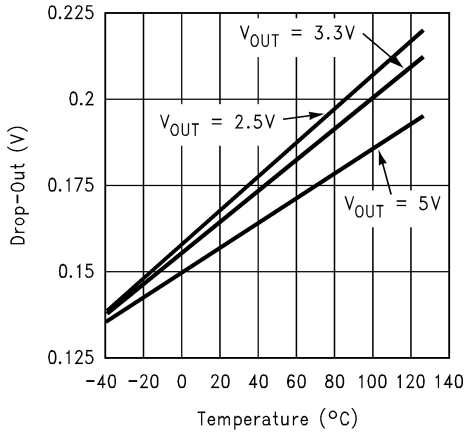


Figure 2. Drop-Out Voltage vs Temperature for Different Output Voltages (I_{OUT} = 800 mA)

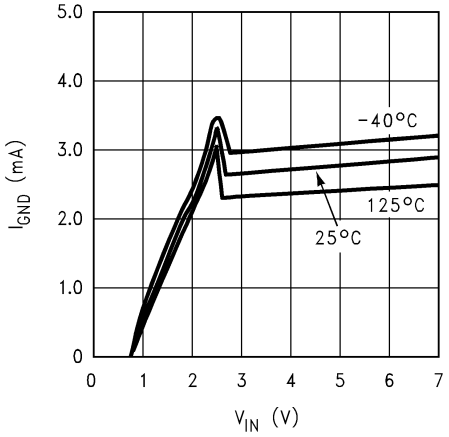


Figure 3. Ground Pin Current vs Input Voltage ($V_{SD} = V_{IN}$)

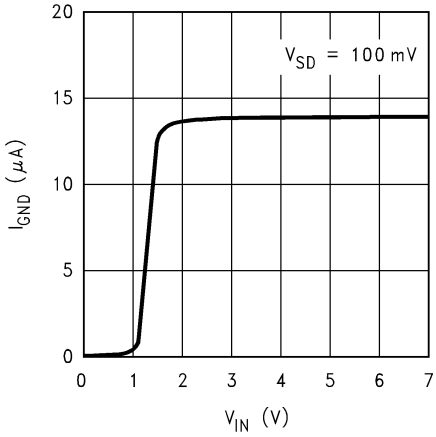


Figure 4. Ground Pin Current vs Input Voltage (V_{SD} = 100 mV)

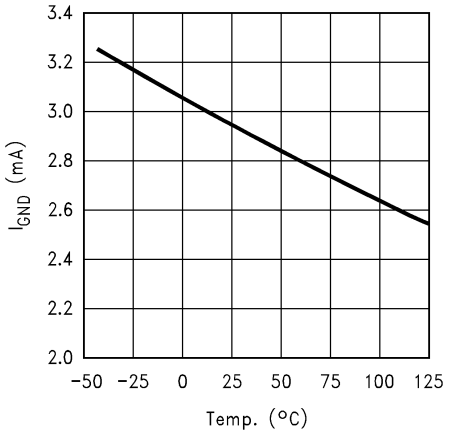


Figure 5. Ground Current vs Temperature ($V_{SD} = V_{IN}$)

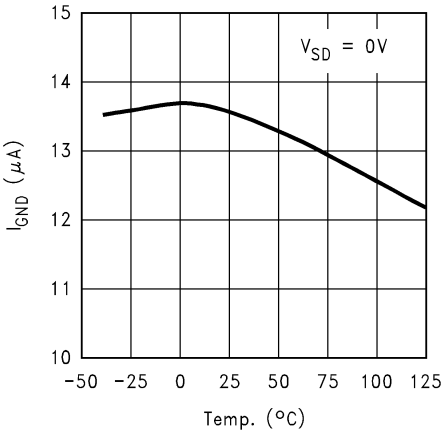


Figure 6. Ground Current vs Temperature (V_{SD} = 0 V)

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Typical Characteristics (continued)

Unless otherwise specified, $V_{IN} = V_{O(NOM)} + 1$ V, $V_{OUT} = 2.5$ V, $C_{OUT} = 33$ µF, $I_{OUT} = 10$ mA, $C_{IN} = 68$ µF, $V_{SDT} = V_{IN}$, and $T_A = 25°C$.

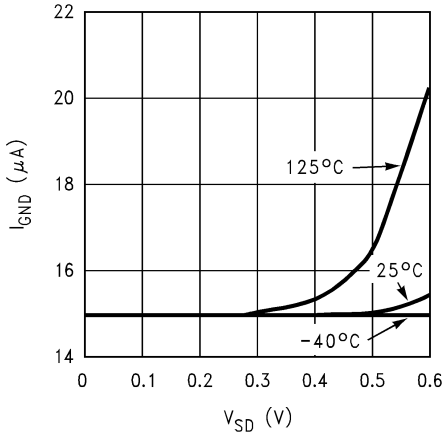


Figure 7. Ground Pin Current vs Shutdown Pin Voltage

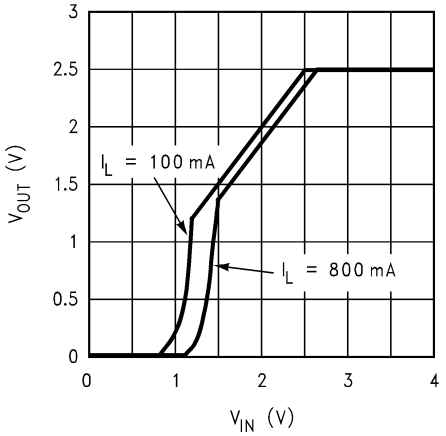


Figure 8. Input Voltage vs Output Voltage

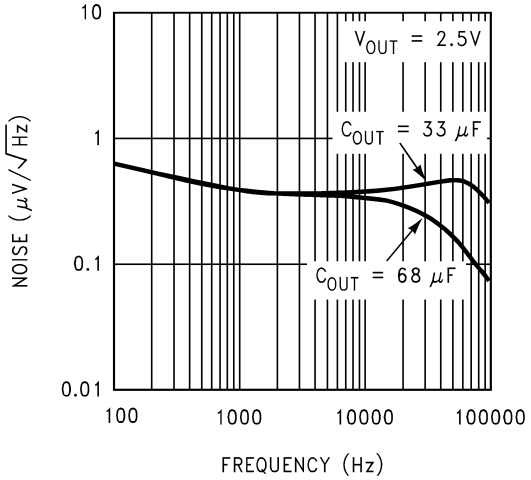


Figure 9. Output Noise Density, V_{OUT} = 2.5 V

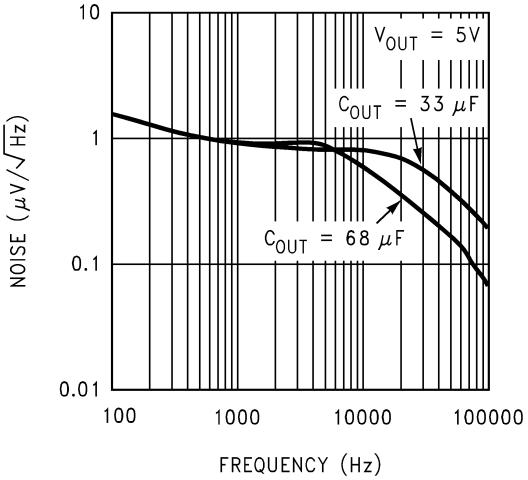


Figure 10. Output Noise Density, V_{OUT} = 5 V

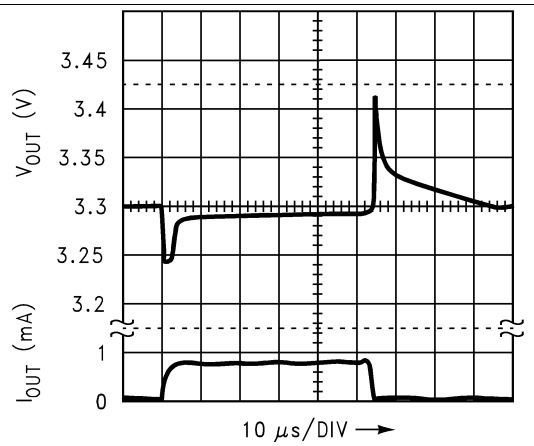


Figure 11. Load Transient Response

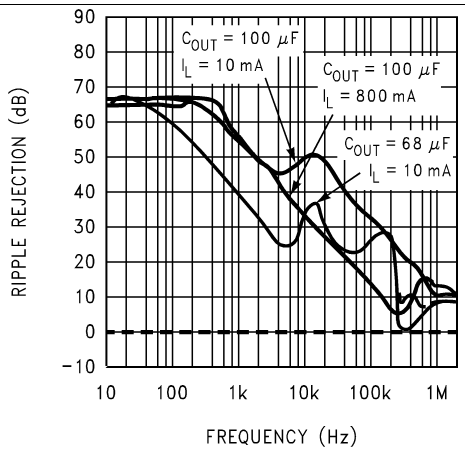


Figure 12. Ripple Rejection vs Frequency

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Typical Characteristics (continued)

Unless otherwise specified, $V_{IN} = V_{O(NOM)} + 1$ V, $V_{OUT} = 2.5$ V, $C_{OUT} = 33$ µF, $I_{OUT} = 10$ mA, $C_{IN} = 68$ µF, $V_{SDT} = V_{IN}$, and $T_A = 25°C$.

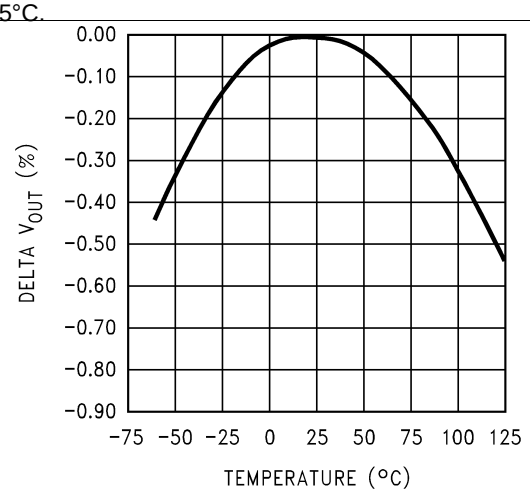


Figure 13. δV_{OUT} vs Temperature

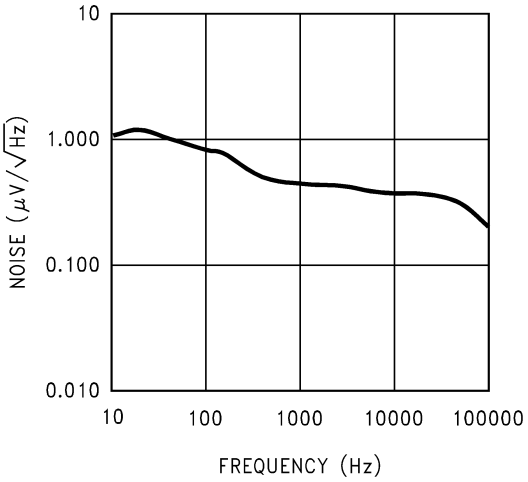


Figure 14. Noise Density $V_{IN} = 3.5$ V, $V_{OUT} = 2.5$ V, $I_L = 10$ mA

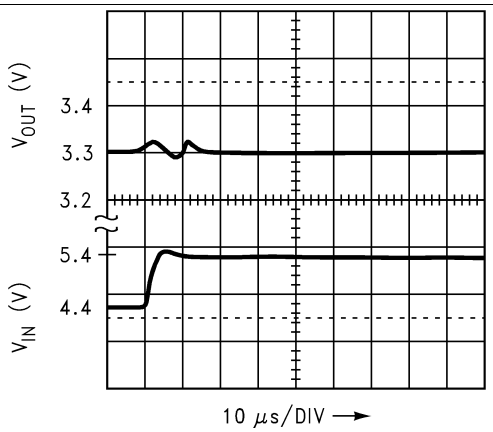


Figure 15. Line Transient Response

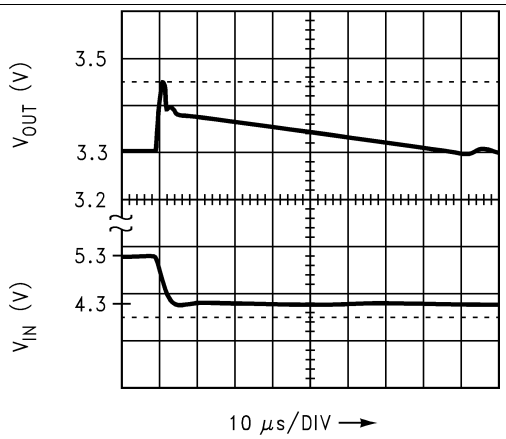


Figure 16. Line Transient Response

7 Detailed Description

7.1 Overview

The LP3961/LP3964 are a series of ultra-low dropout linear regulators. Fixed output products have output voltage options from 1.2 V to 5 V, adjustable output voltage is only available for LP3964. These regulators can provide maximum 800-mA load current. The device can operate under extremely low dropout conditions.

The LP3961 has an $\overline{\text{ERROR}}$ flag pin, this pin will go low when the output voltage drops 10% below nominal value. The LP3964 (fixed output products) provides a SENSE pin. The SENSE pin can improve regulation at remote loads. The LP3961, LP3964 also provide short-circuit protection and reverse current path. The devices can be operated with shutdown ($\overline{\text{SD}}$) pin control.

7.2 Functional Block Diagram

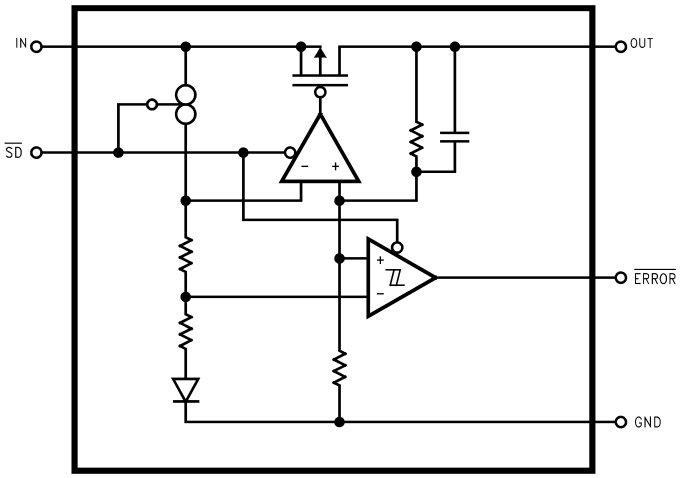


Figure 17. LP3961 Block Diagram

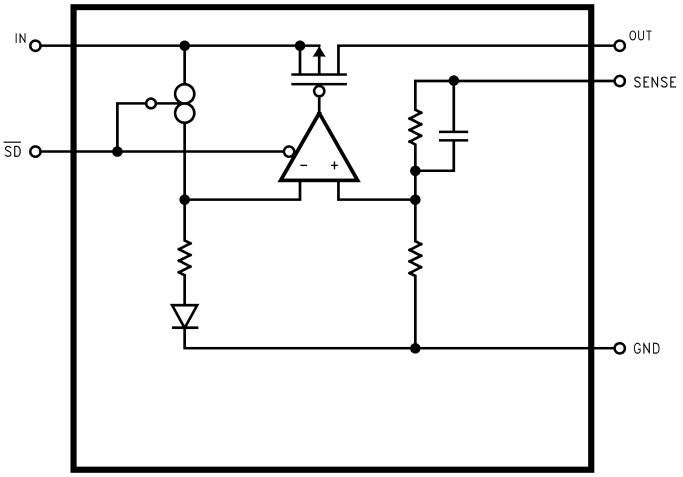


Figure 18. LP3964 Block Diagram

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Functional Block Diagram (continued)

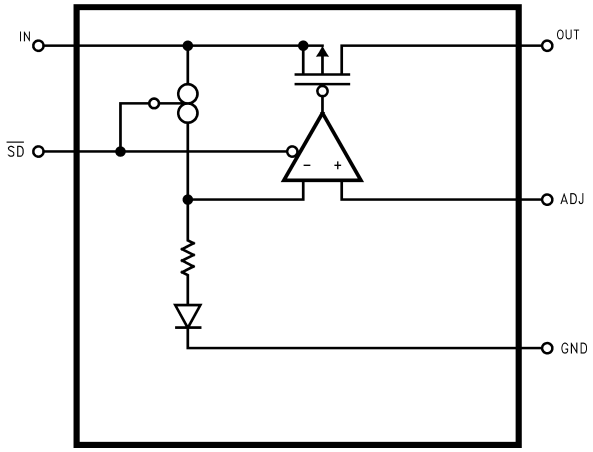


Figure 19. LP3964 Adjustable Version Block Diagram

7.3 Feature Description

7.3.1 Short-Circuit Protection

The LP3961 and LP3964 are short-circuit protected and in the event of a peak overcurrent condition, the short-circuit control loop will rapidly drive the output PMOS pass element off. Once the power pass element shuts down, the control loop will rapidly cycle the output on and off until the average power dissipation causes the thermal shutdown circuit to respond to servo the on/off cycling to a lower frequency. Please refer to the section on thermal information for power dissipation calculations.

7.3.2 $\overline{\text{ERROR}}$ Flag Operation

The LP3961 produces a logic low signal at the $\overline{\text{ERROR}}$ flag pin when the output drops out of regulation due to low input voltage, current limiting, or thermal limiting. This flag has a built-in hysteresis. The timing diagram in Figure 20 shows the relationship between the $\overline{\text{ERROR}}$ pin and the output voltage. In this example, the input voltage is changed to demonstrate the functionality of the $\overline{\text{ERROR}}$ flag.

The internal $\overline{\text{ERROR}}$ flag comparator has an open drain output stage. Hence, the $\overline{\text{ERROR}}$ pin should be pulled high through a pull-up resistor. Although the $\overline{\text{ERROR}}$ pin can sink current of 1 mA, this current is an energy drain from the input supply. Hence, the value of the pull-up resistor should be in the range of 100 kΩ to 1 MΩ. The $\overline{\text{ERROR}}$ pin must be connected to ground if this function is not used. It should also be noted that when the $\overline{\text{SD}}$ pin is pulled low, the $\overline{\text{ERROR}}$ pin is forced to be invalid for reasons of saving power in shutdown mode.

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Feature Description (continued)

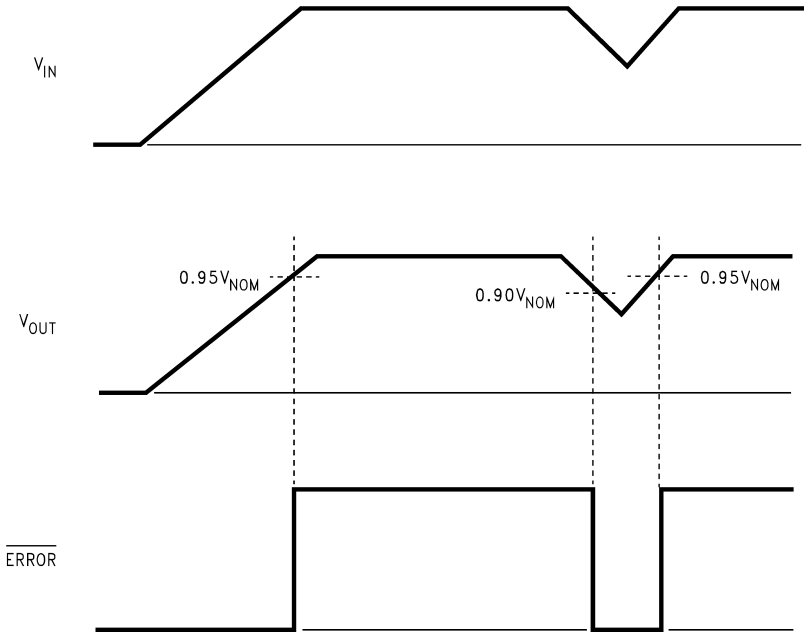


Figure 20. $\overline{ERROR}$ Flag Operation

7.3.3 SENSE Pin

In applications where the regulator output is not very close to the load, LP3964 can provide better remote load regulation using the SENSE pin. Figure 21 depicts the advantage of the SENSE option. LP3961 regulates the voltage at the OUT pin. Hence, the voltage at the remote load will be the regulator output voltage minus the drop across the trace resistance. For example, in the case of a 3.3-V output, if the trace resistance is 100 mΩ, the voltage at the remote load will be 3.22 V with 800 mA of load current, I_{LOAD}. The LP3964 regulates the voltage at the SENSE pin. Connecting the SENSE pin to the remote load will provide regulation at the remote load, as shown in Figure 21. If the sense option pin is not required, the SENSE pin must be connected to the OUT pin.

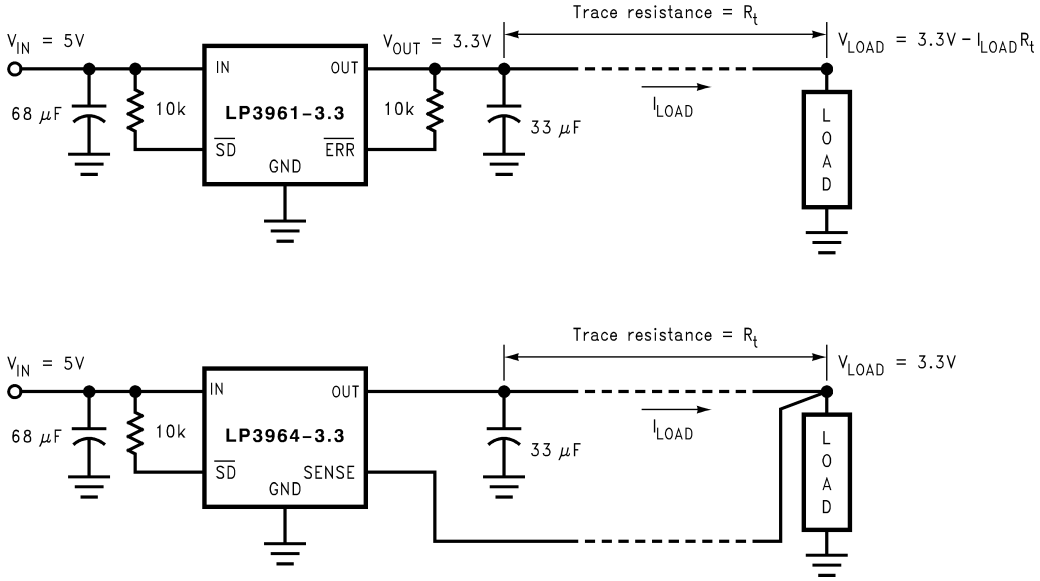


Figure 21. Improving Remote Load Regulation Using LP3964

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Feature Description (continued)

7.3.4 Dropout Voltage

The dropout voltage of a regulator is defined as the minimum input-to-output differential required to stay within 2% of the output voltage. The LP3961 and LP3964 use an internal MOSFET with an Rds(on) of 240 mΩ (typically). For CMOS LDOs, the dropout voltage is the product of the load current and the Rds(on) of the internal MOSFET.

7.3.5 Reverse Current Path

The internal MOSFET in LP3961 and LP3964 has an inherent parasitic diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, if the output is pulled above the input in an application, then current flows from the output to the input as the parasitic diode gets forward biased. The output can be pulled above the input as long as the current in the parasitic diode is limited to 200-mA continuous and 1-A peak.

7.4 Device Functional Modes

7.4.1 Operation With $V_{OUT(TARGET)}$ + 0.35 V ≤ V_{IN} ≤ 7 V

For the fixed output voltage products, the devices operate if the input voltage is equal to or exceeds V_{OUT}(TARGET) + 0.35 V. At input voltages below the minimum V_{IN} requirement, the devices do not operate correctly and output voltage may not reach target value.

7.4.2 Operation With Shutdown ($\overline{SD}$) Pin Control

A CMOS logic low level signal at the shutdown ($\overline{SD}$) pin will turn off the regulator. The $\overline{SD}$ pin must be actively terminated through a 10-kΩ pullup resistor for a proper operation. This pin must be tied to the IN pin if not used .

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP3961, LP3964 products can provide 800-mA output current with 2.5-V to 7-V input voltage. An input capacitor of at least 68-uF is required. A minimum 33-uF output capacitor is required for loop stability. Pin $\overline{SD}$ must be tied to input if not used. For LP3961, the $\overline{ERROR}$ pin should be pulled high through a pull up resistor; if this function is not used, $\overline{ERROR}$ pin must be connected to ground . For LP3964, if the sense option is not required, the SENSE pin must be connected to the OUT pin.

8.2 Typical Applications

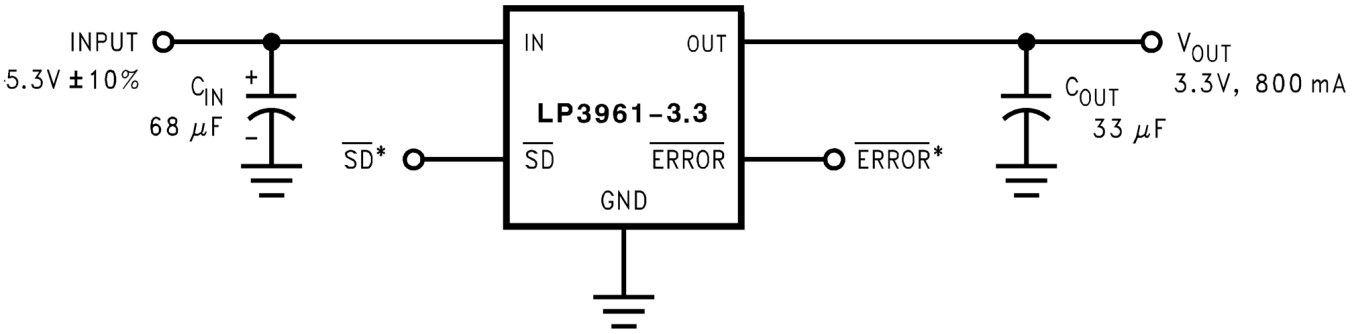


Figure 22. LP3961 Typical Application Circuit

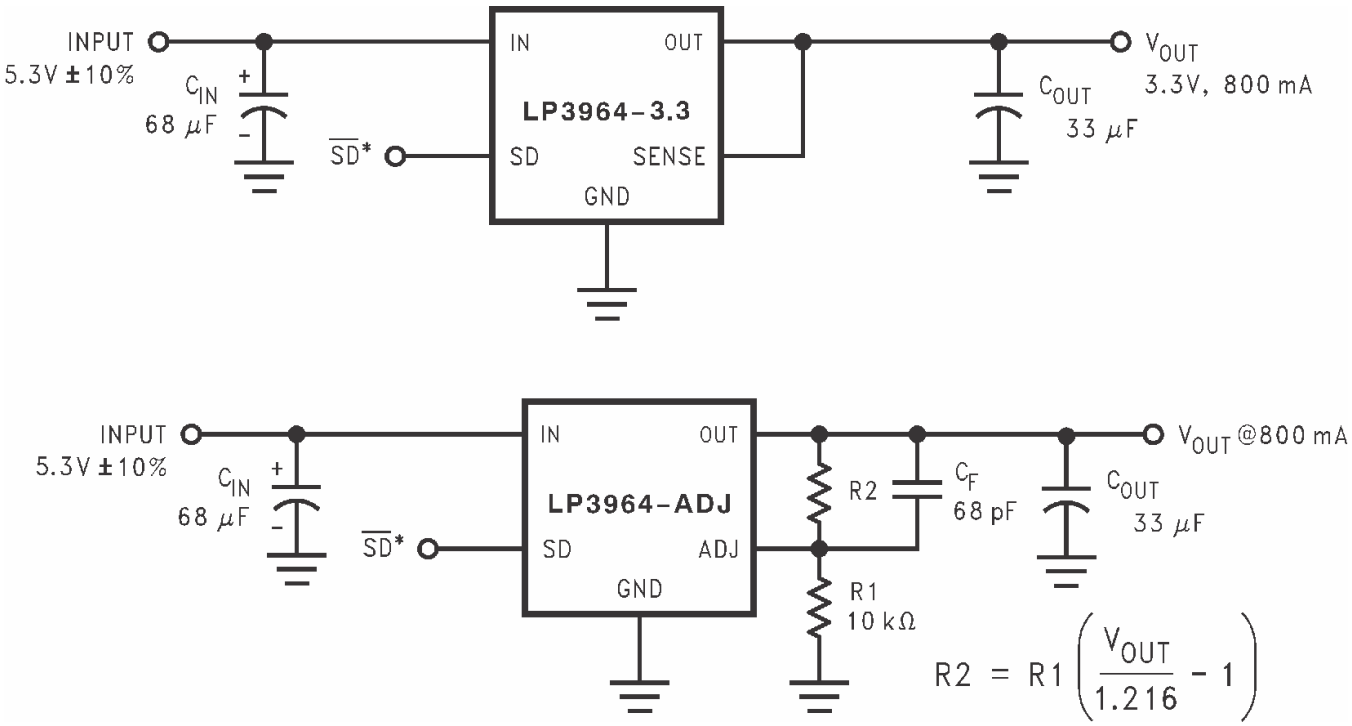


Figure 23. LP3964 Typical Application Circuits

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Typical Applications (continued)

8.2.1 Design Requirements

DESIGN PARAMETERS	VALUE
Input voltage	5.3 V, ±10%
Output voltage	3.3 V, ±3%
Output current	800 mA (maximum)
Input capacitor	68 uF (minimum)
Output capacitor	33 uF (minimum)
$\overline{\text{ERROR}}$ pullup resistor (LP3964 only)	10 kΩ

8.2.2 Detailed Design Procedure

8.2.2.1 External Capacitors

Like any low-dropout regulator, external capacitors are required to assure stability. these capacitors must be correctly selected for proper performance.

8.2.2.1.1 Input Capacitor

The LP3961 or LP3964 requires a low source impedance to maintain regulator stability because the internal bias circuitry is connected directly to the IN pin. The input capacitor must be located less than 1 cm from the LP3961 or LP3964 device and connected directly to the IN and GND pins using traces which have no other currents flowing through them (see the *Layout Guidelines* section).

The minimum allowable input capacitance for a given application depends on the type of the capacitor and equivalent series resistance (ESR). A lower ESR capacitor allows the use of less capacitance, while higher ESR types (like aluminum electrolytics) require more capacitance.

The lowest value of input capacitance that can be used for stable full-load operation is 68 µF (assuming it is a ceramic or low-ESR Tantalum with ESR less than 100 mΩ).

To determine the minimum input capacitance amount and ESR value, an approximation is used:

$$C_{IN}\ \text{ESR}\ (m\Omega) / C_{IN}\ (\mu F) \leq 1.5 \quad (1)$$

This shows that input capacitors with higher ESR values can be used if sufficient total capacitance is provided. Capacitor types (aluminum, ceramic, and tantalum) can be mixed in parallel, but the total equivalent input capacitance/ESR must be defined as above to assure stable operation.

IMPORTANT: The input capacitor must maintain its ESR and capacitance in the stable range over the entire temperature range of the application to assure stability (see the *Capacitor Characteristics* section).

8.2.2.1.2 Output Capacitor

An output capacitor is also required for loop stability. It must be located less than 1 cm from the LP3961 or LP3964 device and connected directly to the OUT and GND pins using traces which have no other currents flowing through them (see the *Layout Guidelines* section).

The minimum value of the output capacitance that can be used for stable full-load operation is 33 µF, but it may be increased without limit. The ESR of the output capacitor is critical because it forms a zero to provide phase lead which is required for loop stability. The ESR must fall within the specified range:

$$0.2\ \Omega \leq C_{OUT}\ \text{ESR} \leq 5\ \Omega \quad (2)$$

The lower limit of 200 mΩ means that ceramic capacitors are not suitable for use as LP3961 or LP3964 output capacitors (but can be used on the input). Some ceramic capacitance can be used on the output if the total equivalent ESR is in the stable range: when using a 100-µF Tantalum as the output capacitor, approximately 3 µF of ceramic capacitance can be applied before stability becomes marginal.

IMPORTANT: The output capacitor must meet the requirements for minimum amount of capacitance and also have an appropriate ESR value over the full temperature range of the application to assure stability (see the *Capacitor Characteristics* section).

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8.2.2.2 Selecting a Capacitor

It is important to note that capacitance tolerance and variation with temperature must be taken into consideration when selecting a capacitor so that the minimum required amount of capacitance is provided over the full operating temperature range. In general, a good Tantalum capacitor will show very little capacitance variation with temperature, but a ceramic may not be as good (depending on dielectric type). Aluminum electrolytics also typically have large temperature variation of capacitance value.

Equally important to consider is a capacitor's ESR change with temperature: this is not an issue with ceramics, as their ESR is extremely low. However, it is very important in Tantalum and aluminum electrolytic capacitors. Both show increasing ESR at colder temperatures, but the increase in aluminum electrolytic capacitors is so severe they may not be feasible for some applications (see the *Capacitor Characteristics* section).

8.2.2.3 Capacitor Characteristics

8.2.2.3.1 Ceramic

For values of capacitance in the 10- to 100-µF range, ceramics are usually larger and more costly than Tantalums but give superior AC performance for bypassing high-frequency noise because of very low ESR (typically less than 10 mΩ). However, some dielectric types do not have good capacitance characteristics as a function of voltage and temperature.

Z5U and Y5V dielectric ceramics have capacitance that drops severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it. The Z5U and Y5V also exhibit a severe temperature effect, losing more than 50% of nominal capacitance at high and low limits of the temperature range.

X7R and X5R dielectric ceramic capacitors are strongly recommended if ceramics are used, as they typically maintain a capacitance range within ±20% of nominal over full operating ratings of temperature and voltage. Of course, they are typically larger and more costly than Z5U/Y5U types for a given voltage and capacitance.

8.2.2.3.2 Tantalum

Solid Tantalum capacitors are recommended for use on the output because their typical ESR is very close to the ideal value required for loop compensation. They also work well as input capacitors if selected to meet the ESR requirements previously listed.

Tantalums also have good temperature stability: a good quality Tantalum will typically show a capacitance value that varies less than 10 to 15% across the full temperature range of 125°C to −40°C. ESR will vary only about 2X going from the high to low temperature limits.

The increasing ESR at lower temperatures can cause oscillations when marginal quality capacitors are used (if the ESR of the capacitor is near the upper limit of the stability range at room temperature).

8.2.2.3.3 Aluminum

This capacitor type offers the most capacitance for the money. The disadvantages are that they are larger in physical size, not widely available in surface mount, and have poor AC performance (especially at higher frequencies) due to higher ESR and ESL.

Compared by size, the ESR of an aluminum electrolytic is higher than either Tantalum or ceramic, and it also varies greatly with temperature. A typical aluminum electrolytic can exhibit an ESR increase of as much as 50X when going from 25°C down to −40°C.

It should also be noted that many aluminum electrolytics only specify impedance at a frequency of 120 Hz, which indicates they have poor high-frequency performance. Only aluminum electrolytics that have an impedance specified at a higher frequency (from 20 kHz to 100 kHz) should be used for the LP396X. Derating must be applied to the manufacturer's ESR specification, because it is typically only valid at room temperature.

Any applications using aluminum electrolytics should be thoroughly tested at the lowest ambient operating temperature where ESR is maximum.

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8.2.2.4 RFI and EMI Susceptibility

Radio frequency interference (RFI) and electromagnetic interference (EMI) can degrade the performance of any integrated circuit because of the small dimensions of the geometries inside the device. In applications where circuit sources are present which generate signals with significant high-frequency energy content (> 1 MHz), care must be taken to ensure that this does not affect the IC regulator.

If RFI and EMI noise is present on the input side of the LP396x regulator (such as applications where the input source comes from the output of a switching regulator), good ceramic bypass capacitors must be used at the input pin of the LP396x.

If a load is connected to the LP396x output which switches at high speed (such as a clock), the high-frequency current pulses required by the load must be supplied by the capacitors on the LP396x output. Because the bandwidth of the regulator loop is less than 100 kHz, the control circuitry cannot respond to load changes above that frequency. The means the effective output impedance of the LP396x at frequencies above 100 kHz is determined only by the output capacitors.

In applications where the load is switching at high speed, the output of the LP396x may need RF isolation from the load. It is recommended that some inductance be placed between the LP396x output capacitor and the load, and good RF bypass capacitors be placed directly across the load.

PCB layout is also critical in high-noise environments, because RFI and EMI is easily radiated directly into PC traces. Noisy circuitry should be isolated from clean circuits where possible, and grounded through a separate path. At MHz frequencies, ground planes begin to look inductive and RFI/EMI can cause ground bounce across the ground plane.

In multilayer PCB applications, care should be taken in layout so that noisy power and ground planes do not radiate directly into adjacent layers which carry analog power and ground.

8.2.2.5 Output Adjustment

An adjustable output device has output voltage range of 1.216 V to 5.1 V. To obtain a desired output voltage, the following equation can be used with R1 always a 10-kΩ resistor.

$$R2 = R1\left(\frac{V_{OUT}}{1.216} - 1\right) \tag{3}$$

For output stability, C_F must be between 68 pF and 100 pF.

8.2.2.6 Turnon Characteristics for Output Voltages Programmed to 2.0 V or Below

As V_{IN} increases during start-up, the regulator output will track the input until V_{IN} reaches the minimum operating voltage (typically about 2.2 V). For output voltages programmed to 2 V or below, the regulator output may momentarily exceed its programmed output voltage during start up. Outputs programmed to voltages above 2 V are not affected by this behavior.

8.2.2.7 Output Noise

Noise is specified in two ways:

- Spot noise or output noise density is the RMS sum of all noise sources, measured at the regulator output, at a specific frequency (measured with a 1-Hz bandwidth). This type of noise is usually plotted on a curve as a function of frequency.
- Total output noise or broadband noise is the RMS sum of spot noise over a specified bandwidth, usually several decades of frequencies.

Attention should be paid to the units of measurement. Spot noise is measured in units $\mu V/\sqrt{Hz}$ or $nV/\sqrt{Hz}$ and total output noise is measured in $\mu V_{(rms)}$.

The primary source of noise in low-dropout regulators is the internal reference. In CMOS regulators, noise has a low-frequency component and a high-frequency component, which depend strongly on the silicon area and quiescent current. Noise can be reduced in two ways: by increasing the transistor area or by increasing the current drawn by the internal reference. Increasing the area will decrease the chance of fitting the die into a smaller package. Increasing the current drawn by the internal reference increases the total supply current (ground pin current). Using an optimized trade-off of ground pin current and die size, LP396x achieves low noise performance and low quiescent current operation.

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The total output noise specification for LP396x is presented in the *Electrical Characteristics* table. The output noise density at different frequencies is represented by a curve under typical performance characteristics.

8.2.2.8 Shutdown Operation

A CMOS logic level signal at the shutdown ($\overline{SD}$) pin will turnoff the regulator. Pin $\overline{SD}$ must be actively terminated through a 10-kΩ pullup resistor for a proper operation. If this pin is driven from a source that actively pulls high and low (such as a CMOS rail-to-rail comparator), the pull-up resistor is not required. This pin must be tied to the IN pin if not used.

8.2.2.9 Maximum Output Current Capability

LP3961 and LP3964 can deliver a continuous current of 800 mA over the full operating temperature range. A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible conditions, the junction temperature must be within the range specified under operating conditions. The total power dissipation of the device is given by:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (4)$$

where I_{GND} is the operating ground current of the device (specified under the *Electrical Characteristics* table).

The maximum allowable temperature rise (T_{Rmax}) depends on the maximum ambient temperature (T_{Amax}) of the application, and the maximum allowable junction temperature (T_{Jmax}):

$$T_{Rmax} = T_{Jmax} - T_{Amax} \quad (5)$$

The maximum allowable value for junction to ambient Thermal Resistance, $R_{\theta JA}$, can be calculated using the formula:

$$R_{\theta JA} = T_{Rmax} / P_D \quad (6)$$

LP3961 and LP3964 are available in TO-220, SFM/TO-263, and SOT-223 packages. The thermal resistance depends on amount of copper area or heat sink, and on air flow.

8.2.3 Application Curves

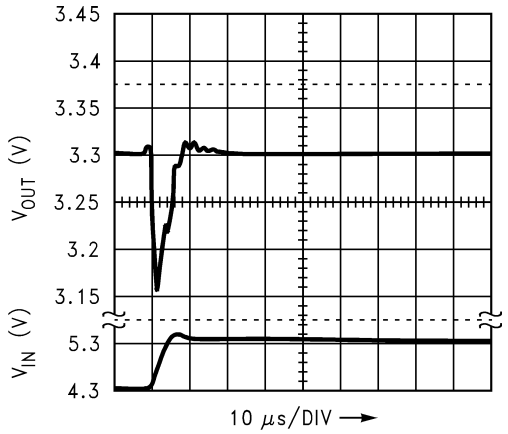


Figure 24. Line Transient Response (I_{OUT} = 800 mA)

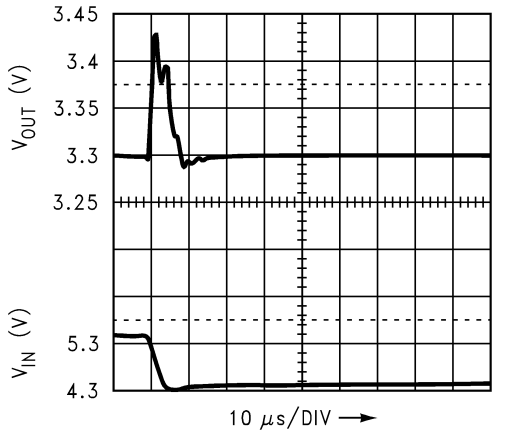


Figure 25. Line Transient Response (I_{OUT} = 800 mA)

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9 Power Supply Recommendations

The LP396x devices are designed to operate from an input voltage supply range between 2.5 V and 7 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. An input capacitor of at least 68 µF is required.

10 Layout

10.1 Layout Guidelines

Good PC layout practices must be used or instability can be induced because of ground loops and voltage drops. The input and output capacitors must be directly connected to the IN, OUT, and GND pins of the LP396x using traces which do not have other currents flowing in them (Kelvin connect).

The best way to do this is to lay out C_{IN} and C_{OUT} near the device with short traces to the IN, OUT, and GND pins. The regulator ground pin should be connected to the external circuit ground so that the regulator and its capacitors have a single-point ground.

It should be noted that stability problems have been seen in applications where vias to an internal ground plane were used at the ground points of the LP396x IC and the input and output capacitors. This was caused by varying ground potentials at these nodes resulting from current flowing through the ground plane. Using a single-point ground technique for the regulator and its capacitors fixed the problem.

Because high current flows through the traces going into the IN pin and coming from the OUT pin, Kelvin connect the capacitor leads to these pins so there is no voltage drop in series with the input and output capacitors.

10.2 Layout Example

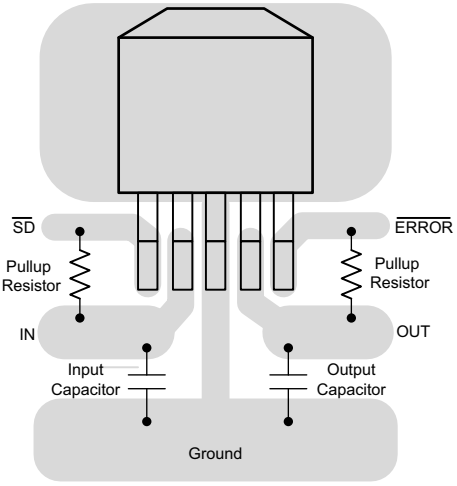


Figure 26. LP3961 TO-263 Package Typical Layout

Layout Example (continued)

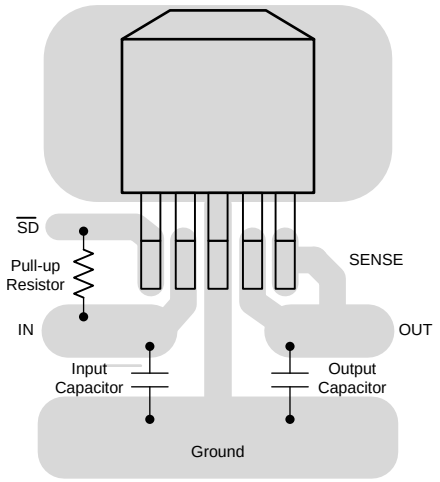


Figure 27. LP3964 TO-263 Package Typical Layout

10.3 Heatsinking TO-220 Packages

The thermal resistance of a TO-220 package can be reduced by attaching it to a heatsink or a copper plane on a PC board.

The heatsink to be used in the application should have a heatsink-to-ambient thermal resistance,

$$R_{\theta HA} \leq R_{\theta JA} - R_{\theta CH} - R_{\theta JC} \quad (7)$$

In this equation, $R_{\theta CH}$ is the thermal resistance from the junction to the surface of the heatsink and $R_{\theta JC}$ is the thermal resistance from the junction to the surface of the case.

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11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LP3961	Click here	Click here	Click here	Click here	Click here
LP3964	Click here	Click here	Click here	Click here	Click here

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3961EMP-1.8/NOPB	ACTIVE	SOT-223	NDC	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LBAB	Samples
LP3961EMP-2.5	NRND	SOT-223	NDC	5	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	LBBB	
LP3961EMP-2.5/NOPB	ACTIVE	SOT-223	NDC	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LBBB	Samples
LP3961EMP-3.3	NRND	SOT-223	NDC	5	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	LAZB	
LP3961EMP-3.3/NOPB	ACTIVE	SOT-223	NDC	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LAZB	Samples
LP3961EMP-5.0	NRND	SOT-223	NDC	5	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	LBSB	
LP3961EMP-5.0/NOPB	ACTIVE	SOT-223	NDC	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LBSB	Samples
LP3961EMPX-1.8/NOPB	ACTIVE	SOT-223	NDC	5	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LBAB	Samples
LP3961EMPX-2.5/NOPB	ACTIVE	SOT-223	NDC	5	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LBBB	Samples
LP3961EMPX-3.3	NRND	SOT-223	NDC	5	2000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	LAZB	
LP3961ES-1.8	NRND	DDPAK/ TO-263	KTT	5	45	Non-RoHS & Green	Call TI	Level-3-235C-168 HR	-40 to 125	LP3961ES -1.8	
LP3961ES-1.8/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LP3961ES -1.8	Samples
LP3961ES-2.5/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LP3961ES -2.5	Samples
LP3961ES-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LP3961ES -3.3	Samples
LP3961ESX-2.5/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LP3961ES -2.5	Samples
LP3961ESX-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LP3961ES -3.3	Samples
LP3964EMP-1.8/NOPB	ACTIVE	SOT-223	NDC	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LBFB	Samples
LP3964EMP-2.5/NOPB	ACTIVE	SOT-223	NDC	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LBHB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3964EMP-3.3/NOPB	ACTIVE	SOT-223	NDC	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LBJB	Samples
LP3964EMP-ADJ	NRND	SOT-223	NDC	5	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	LBPB	
LP3964EMP-ADJ/NOPB	ACTIVE	SOT-223	NDC	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LBPB	Samples
LP3964EMPX-2.5/NOPB	ACTIVE	SOT-223	NDC	5	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LBHB	Samples
LP3964EMPX-ADJ/NOPB	ACTIVE	SOT-223	NDC	5	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LBPB	Samples
LP3964ES-1.8	NRND	DDPAK/ TO-263	KTT	5	45	Non-RoHS & Green	Call TI	Level-3-235C-168 HR	-40 to 125	LP3964ES -1.8	
LP3964ES-1.8/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LP3964ES -1.8	Samples
LP3964ES-2.5/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LP3964ES -2.5	Samples
LP3964ES-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LP3964ES -3.3	Samples
LP3964ES-ADJ	NRND	DDPAK/ TO-263	KTT	5	45	Non-RoHS & Green	Call TI	Level-3-235C-168 HR	-40 to 125	LP3964ES -ADJ	
LP3964ES-ADJ/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LP3964ES -ADJ	Samples
LP3964ESX-2.5/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LP3964ES -2.5	Samples
LP3964ESX-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LP3964ES -3.3	Samples
LP3964ESX-ADJ/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LP3964ES -ADJ	Samples
LP3964ET-ADJ/NOPB	ACTIVE	TO-220	NDH	5	45	RoHS & Green	SN	Level-1-NA-UNLIM	-40 to 125	LP3964ET -ADJ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

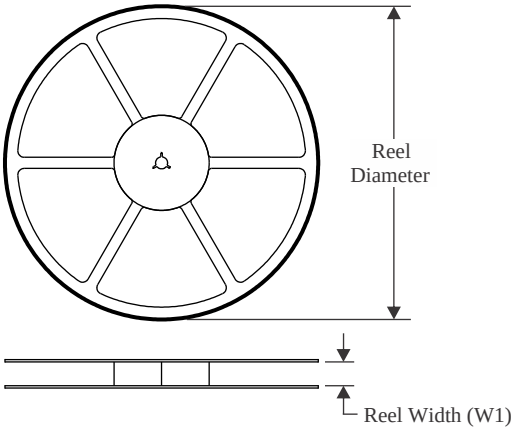
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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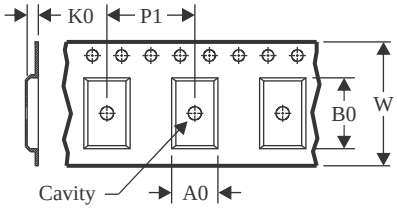
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

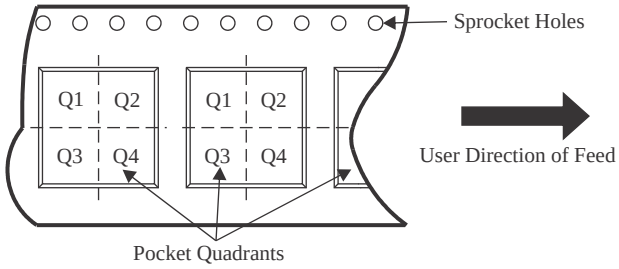


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

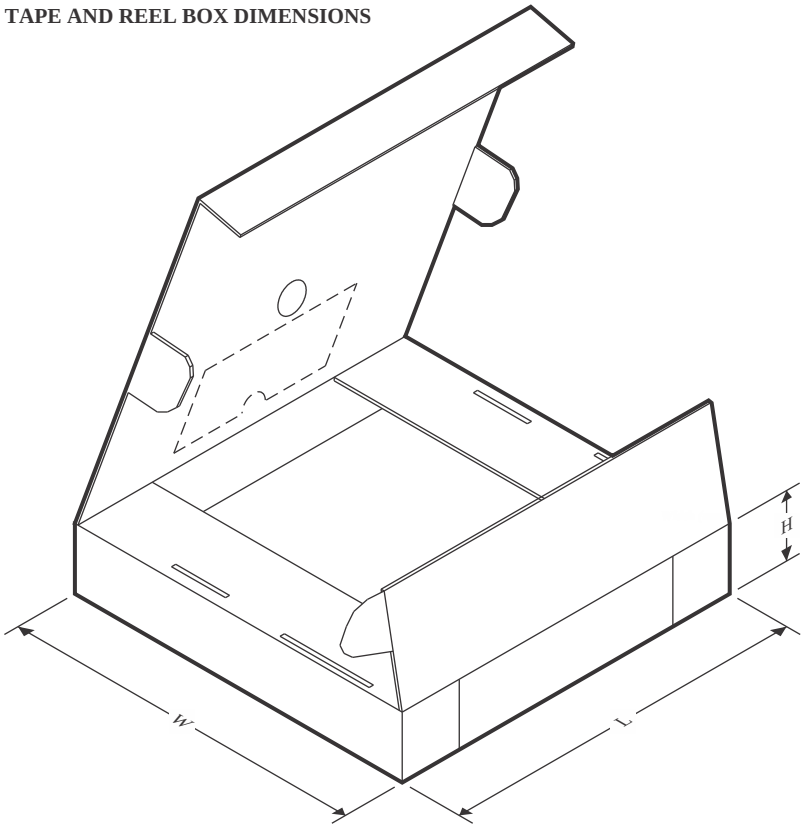


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3961EMP-1.8/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3961EMP-2.5	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3961EMP-2.5/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3961EMP-3.3	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3961EMP-3.3/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3961EMP-5.0	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3961EMP-5.0/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3961EMPX-1.8/NOPB	SOT-223	NDC	5	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3961EMPX-2.5/NOPB	SOT-223	NDC	5	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3961EMPX-3.3	SOT-223	NDC	5	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3961ESX-2.5/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3961ESX-3.3/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3964EMP-1.8/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3964EMP-2.5/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3964EMP-3.3/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3964EMP-ADJ	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3964EMP-ADJ/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3964EMPX-2.5/NOPB	SOT-223	NDC	5	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3964EMPX-ADJ/NOPB	SOT-223	NDC	5	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3964ESX-2.5/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3964ESX-3.3/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3964ESX-ADJ/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS

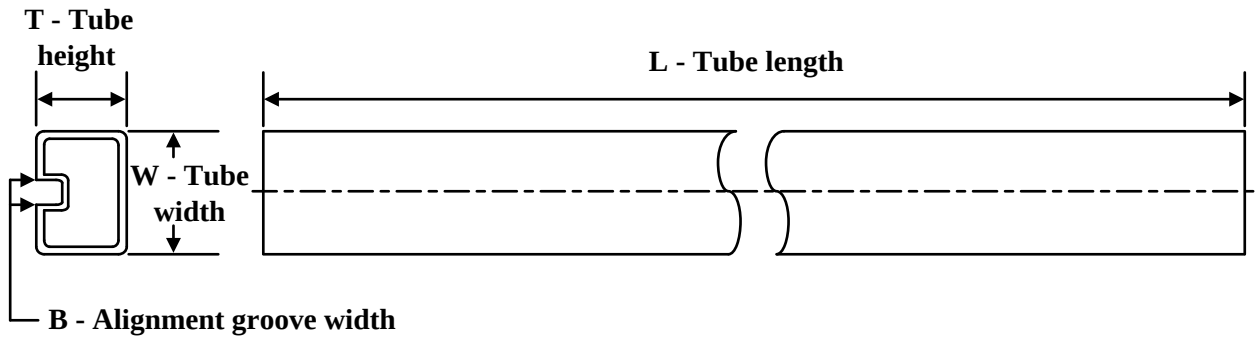


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3961EMP-1.8/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3961EMP-2.5	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3961EMP-2.5/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3961EMP-3.3	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3961EMP-3.3/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3961EMP-5.0	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3961EMP-5.0/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3961EMPX-1.8/NOPB	SOT-223	NDC	5	2000	367.0	367.0	35.0
LP3961EMPX-2.5/NOPB	SOT-223	NDC	5	2000	367.0	367.0	35.0
LP3961EMPX-3.3	SOT-223	NDC	5	2000	367.0	367.0	35.0
LP3961ESX-2.5/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LP3961ESX-3.3/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LP3964EMP-1.8/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3964EMP-2.5/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3964EMP-3.3/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3964EMP-ADJ	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3964EMP-ADJ/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3964EMPX-2.5/NOPB	SOT-223	NDC	5	2000	367.0	367.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3964EMPX-ADJ/NOPB	SOT-223	NDC	5	2000	367.0	367.0	35.0
LP3964ESX-2.5/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LP3964ESX-3.3/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LP3964ESX-ADJ/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0

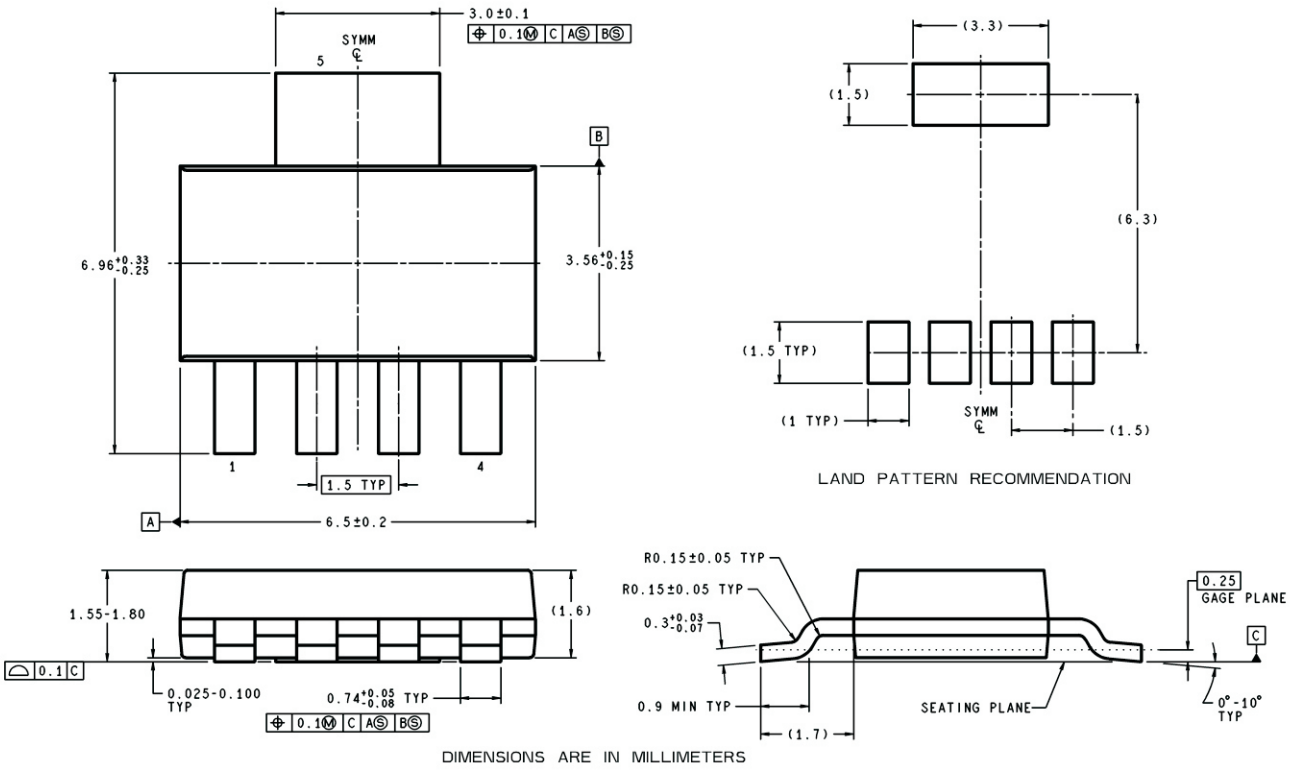
TUBE



*All dimensions are nominal

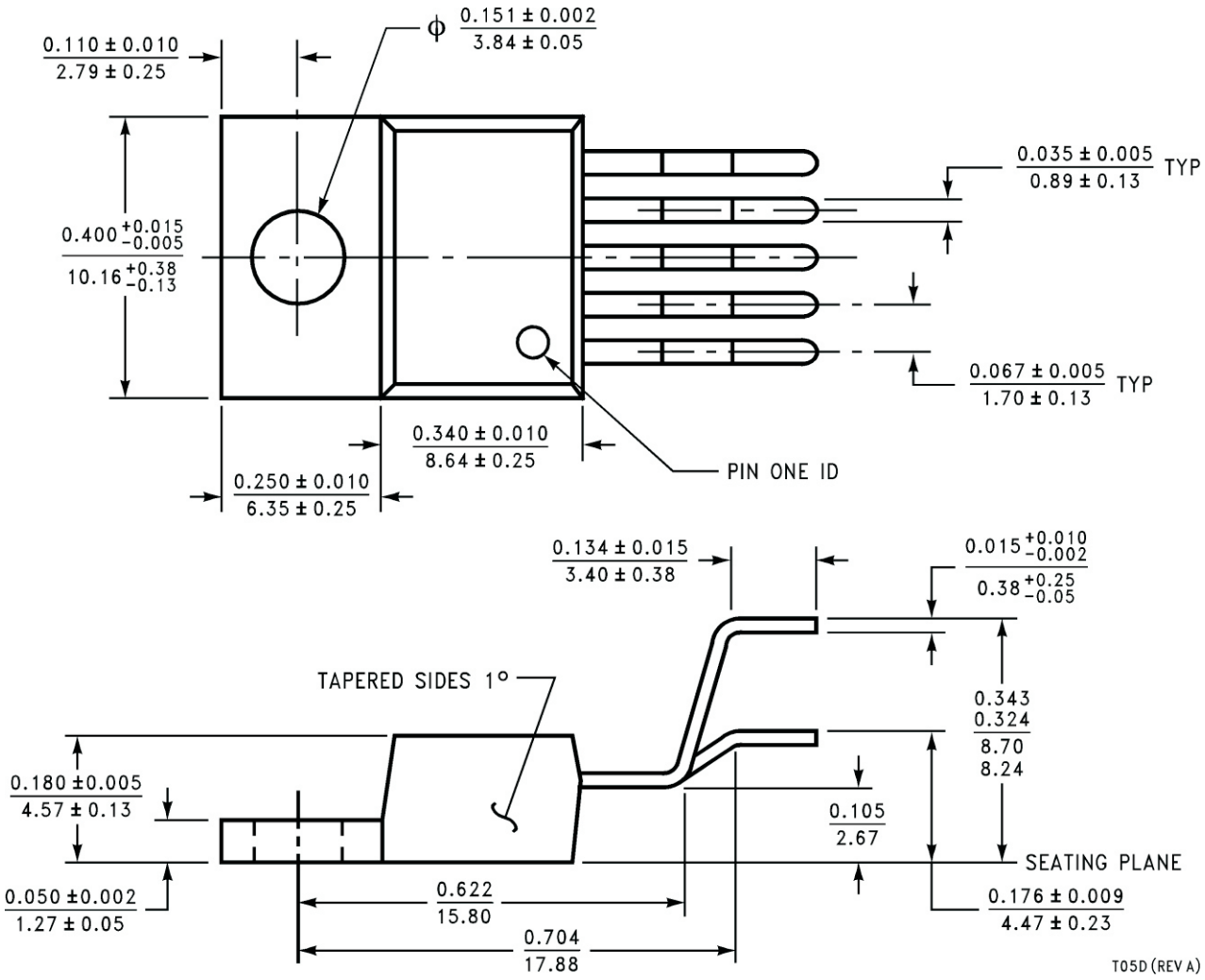
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LP3961ES-1.8	KTT	TO-263	5	45	502	25	8204.2	9.19
LP3961ES-1.8	KTT	TO-263	5	45	502	25	8204.2	9.19
LP3961ES-1.8/NOPB	KTT	TO-263	5	45	502	25	8204.2	9.19
LP3961ES-2.5/NOPB	KTT	TO-263	5	45	502	25	8204.2	9.19
LP3961ES-3.3/NOPB	KTT	TO-263	5	45	502	25	8204.2	9.19
LP3964ES-1.8	KTT	TO-263	5	45	502	25	8204.2	9.19
LP3964ES-1.8	KTT	TO-263	5	45	502	25	8204.2	9.19
LP3964ES-1.8/NOPB	KTT	TO-263	5	45	502	25	8204.2	9.19
LP3964ES-2.5/NOPB	KTT	TO-263	5	45	502	25	8204.2	9.19
LP3964ES-3.3/NOPB	KTT	TO-263	5	45	502	25	8204.2	9.19
LP3964ES-ADJ	KTT	TO-263	5	45	502	25	8204.2	9.19
LP3964ES-ADJ	KTT	TO-263	5	45	502	25	8204.2	9.19
LP3964ES-ADJ/NOPB	KTT	TO-263	5	45	502	25	8204.2	9.19
LP3964ET-ADJ/NOPB	NDH	TO-220	5	45	502	30	30048.2	10.74

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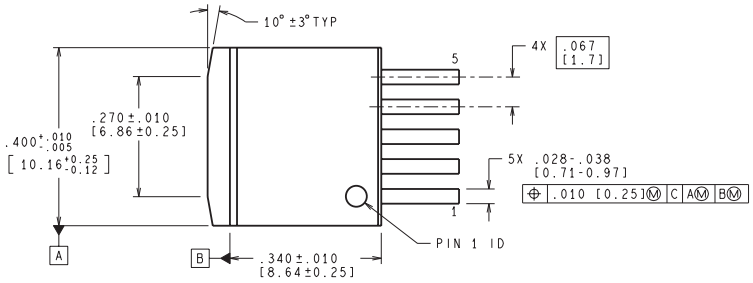


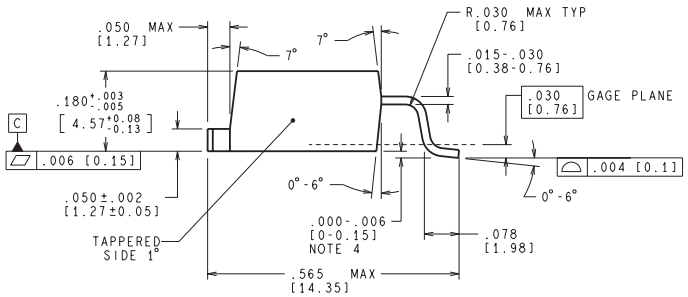
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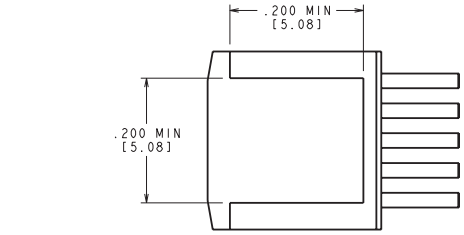
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0.110 ± 0.010
2.79 ± 0.25
ϕ 0.151 ± 0.002
3.84 ± 0.05
0.035 ± 0.005
0.89 ± 0.13
TYP
0.400 +0.015 −0.005
10.16 +0.38 −0.13
0.067 ± 0.005
1.70 ± 0.13
TYP
0.340 ± 0.010
8.64 ± 0.25
PIN ONE ID
0.250 ± 0.010
6.35 ± 0.25
0.134 ± 0.015
3.40 ± 0.38
0.015 +0.010 −0.002
0.38 +0.25 −0.05
TAPERED SIDES 1°
0.343
0.324
8.70
8.24
0.180 ±0.005
4.57 ± 0.13
0.105
2.67
SEATING PLANE
0.050 ±0.002
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15.80
0.176 ± 0.009
4.47 ± 0.23
0.704
17.88
T05D (REV A)

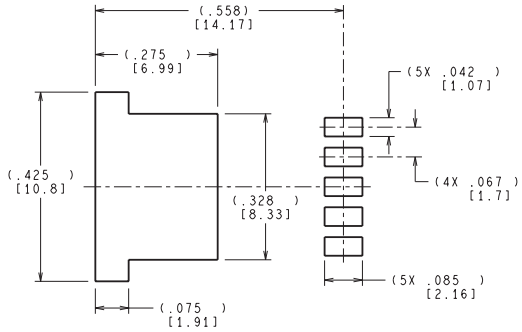
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DIMENSIONS IN ( ) FOR REFERENCE ONLY

TS5B (Rev D)

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