MAX3221E 具有 ±15kV IEC ESD 保护功能的 3V 至 5.5V 单通道 RS-232 线路驱动器/接收器

1 特性

- 为 RS-232 引脚提供 ESD 保护
  - ±15kV 人体放电模型 (HBM)
  - ±8kV（IEC 61000-4-2，接触放电）
  - ±15kV（IEC 61000-4-2，空气间隙放电）
- 符合或超出 TIA/EIA-232-F 和 ITU v.28 标准的要求
- 由 3V 至 5.5V V_{CC} 电源供电
- 速率高达 250kbit/s
- 一个驱动器和一个接收器
- 低待机电流：1μA（典型值）
- 接受 5V 逻辑输入及 3.3V 电源
- 自动断电功能可自动禁用驱动器来节省能耗
- 备选高速器件 (1Mbit/s)
  - SN75C3221E 和 SN65C3221E

2 应用

- 工业 PC
- 有线网络
- 数据中心和企业级计算
- 电池供电型系统
- PDA
- 笔记本电脑
- 便携式计算机
- 掌上电脑
- 手持设备

3 说明

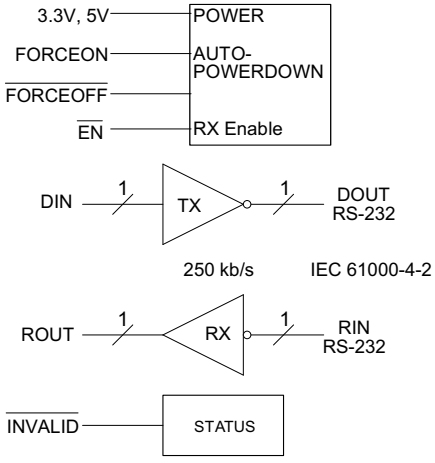
MAX3221E 是一个单驱动器、单接收器 RS-232 解决方案，通过单个 V_{CC} 电源供电。RS-232 引脚提供 IEC 61000-4-2 ESD 保护。该器件符合 TIA/EIA-232-F 的要求并在异步通信控制器与串行端口连接器之间提供电气接口。电荷泵和四个小型外部电容器支持由 3V 至 5.5V 单电源供电。这些器件以高达 250kbit/s 的数据信号传输速率和最高为 30V/μs 的驱动器输出压摆率运行。

可提供灵活的电源管理控制选项。当接收器断开连接或远程驱动器断电时，自动断电功能会禁用驱动器和电荷泵。可以手动启用或禁用驱动器。当接收器输入断开或断电时，$\overline{\text{INVALID}}$ 输出变为低电平。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
MAX3221ECDB、MAX3221EIDB	SSOP (16)	6.20mm x 5.30mm
MAX3221ECPW、MAX3221EIPW	TSSOP (16)	5.00mm × 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



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方框图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (March 2016) to Revision C (July 2021)	Page
• 更改了*应用*列表	1
• Added *ESD ratings IEC Specifications* table and added a table note for the minimum requirement to meet the IEC ESD level	4
• Changed values in the *Thermal Information* table for DB and PW packages	5

Changes from Revision A (May 2006) to Revision B (March 2016)	Page
• 添加了 *ESD 等级*表、*特性说明*部分、*器件功能模式*、*应用和实施*部分、*电源相关建议*部分、*布局*部分、*器件和文档支持*部分以及*机械、封装和可订购信息*部分	1
• 删除了*订购信息*表；请参阅数据表末尾的 POA	1
• Changed $R_{\theta JA}$ thermal values: 82 to 92 for DB package and 108 to 100.3 for PW Package	5

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5 Pin Configuration and Functions

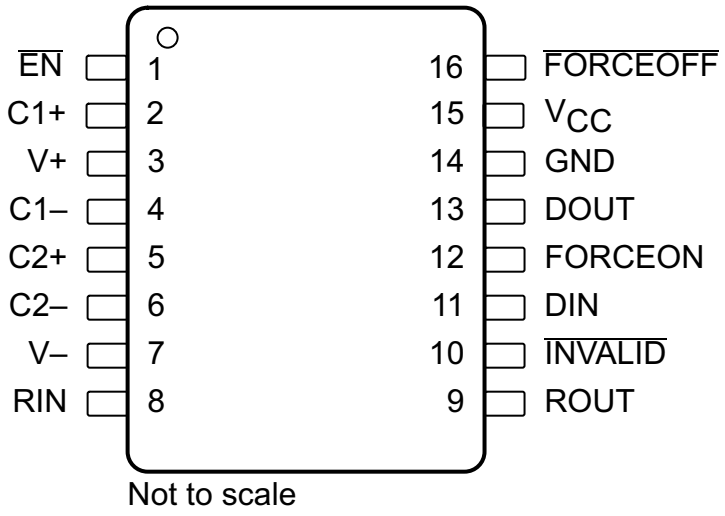


图 5-1. DB or PW Package, 16-Pin SSOP or TSSOP, Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
C1+	2	—	Positive terminals of the voltage-doubler charge pump capacitors
C2+	5		
C1–	4	—	Negative terminals of the voltage-doubler charge pump capacitors
C2–	6		
DIN	11	I	Driver input
DOUT	13	O	RS-232 driver output
$\overline{EN}$	1	I	Low input enables receiver ROUT output. High input sets ROUT to high impedance.
$\overline{FORCEOFF}$	16	I	Automatic power-down control input
FORCEON	12	I	Automatic power-down control input
GND	14	—	Ground
$\overline{INVALID}$	10	O	Invalid output pin. Output low when RIN input is unpowered.
RIN	8	I	RS-232 receiver input
ROUT	9	O	Receiver output
V_{CC}	15	—	3-V to 5.5-V supply voltage
V+	3	O	5.5-V supply generated by the charge pump
V–	7	O	–5.5-V supply generated by the charge pump

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		– 0.3	6	V
V+	Positive output supply voltage(2)		– 0.3	7	V
V –	Negative output supply voltage(2)		0.3	– 7	V
V+ – V –	Supply voltage difference(2)			13	V
V_I	Input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON, $\overline{\text{EN}}$	– 0.3	6	V
		RIN	– 25	25	
V_O	Output voltage	DOUT	– 13.2	13.2	V
		ROUT, $\overline{\text{INVALID}}$	– 0.3	V_{CC} + 0.3	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature		– 65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to network GND.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Pins 8 and 11	±15000	V
			All other pins	±2000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	All pins	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings - IEC Specifications

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, DOUT and RIN (1)	Pins 8 and 11	±8000	V
		IEC 61000-4-2 Air-Gap Discharge, DOUT and RIN (1)		±15000	

(1) A minimum of 1-µF capacitor is required between VCC and GND to meet the specified IEC-ESD level.

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6.4 Recommended Operating Conditions

See 图 9-1 (1)

				MIN	NOM	MAX	UNIT
	Supply voltage		V_{CC} = 3.3 V	3	3.3	3.6	V
			V_{CC} = 5 V	4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, $\overline{FORCEOFF}$, FORCEON, $\overline{EN}$	V_{CC} = 3.3 V	2			V
			V_{CC} = 5 V	2.4			
V_{IL}	Driver and control low-level input voltage	DIN, $\overline{FORCEOFF}$, FORCEON, $\overline{EN}$				0.8	V
V_I	Driver and control input voltage	DIN, $\overline{FORCEOFF}$, FORCEON		0		5.5	V
V_I	Receiver input voltage			–25		25	V
T_A	Operating free-air temperature	MAX3221EC		0		70	°C
		MAX3221EI		–40		85	

(1) Test conditions are C1 – C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2 – C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

6.5 Thermal Information

THERMAL METRIC(1)		MAX3221E		UNIT
		DB (SSOP)	PW (TSSOP)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105.8	110.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.9	41.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.6	57.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.1	4.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.8	56.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(2)

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_I	Input leakage current	$\overline{FORCEOFF}$, FORCEON, $\overline{EN}$				±0.01	±1	µA
I_{CC}	Supply current	Auto-power down disabled	V_{CC} = 3.3 V or 5 V, T_A = 25°C	No load, $\overline{FORCEOFF}$ and FORCEON at V_{CC}		0.3	1	mA
		Powered off		No load, $\overline{FORCEOFF}$ at GND		1	10	µA
		Auto-power down enabled		No load, $\overline{FORCEOFF}$ at V_{CC}, FORCEON at GND, All RIN are open or grounded		1	10	

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Test conditions are C1 – C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2 – C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

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6.7 Electrical Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(3)

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = GND		5	5.4		V
V_{OL}	Low-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = V_{CC}		–5	–5.4		V
I_{IH}	High-level input current	V_I = V_{CC}				±0.01	±1	µA
I_{IL}	Low-level input current	V_I = GND				±0.01	±1	µA
I_{OS}	Short-circuit output current(2)	V_{CC} = 3.6 V,	V_O = 0 V			±35	±60	mA
		V_{CC} = 5.5 V,	V_O = 0 V			±35	±60	
r_o	Output resistance	V_{CC}, V+, and V– = 0 V,	V_O = ±2 V		300	10M		Ω
I_{off}	Output leakage current	$\overline{FORCEOFF}$ = GND	V_O = ±12 V,	V_{CC} = 3 V to 3.6 V			±25	µA
			V_O = ±10 V,	V_{CC} = 4.5 V to 5.5 V			±25	

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.
(3) Test conditions are C1 – C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2 – C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

6.8 Electrical Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA	V_{CC} – 0.6	V_{CC} – 0.1		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.3 V		1.6	2.4	V
		V_{CC} = 5 V		1.9	2.4	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 3.3 V	0.6	1.1		V
		V_{CC} = 5 V	0.8	1.4		
V_{hys}	Input hysteresis (V_{IT+} – V_{IT-})			0.5		V
I_{off}	Output leakage current	$\overline{EN}$ = V_{CC}		±0.05	±10	µA
r_i	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Test conditions are C1 – C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2 – C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

6.9 Electrical Characteristics: Auto-Power Down

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{T+(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}		2.7	V
$V_{T-(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	–2.7		V
$V_{T(invalid)}$	Receiver input threshold for I $\overline{NVALID}$ low-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	–0.3	0.3	V
V_{OH}	$\overline{INVALID}$ high-level output voltage	I_{OH} = –1 mA, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	V_{CC} – 0.6		V
V_{OL}	$\overline{INVALID}$ low-level output voltage	I_{OL} = 1.6 mA, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}		0.4	V

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6.10 Switching Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(3)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
	Maximum data rate	C_L = 1000 pF,	R_L = 3 kΩ,	150	250		kbit/s
$t_{sk(p)}$	Pulse skew(2)	C_L = 150 pF to 2500 pF,	R_L = 3 kΩ to 7 kΩ, See 图 7-2		100		ns
SR(tr)	Slew rate, transition region (see 图 7-1)	V_{CC} = 3.3 V, R_L = 3 kΩ to 7 kΩ	C_L = 150 pF to 1000 pF	6		30	V/µs
			C_L = 150 pF to 2500 pF	4		30	

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Test conditions are C1 – C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2 – C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

6.11 Switching Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(3)

PARAMETER		TEST CONDITIONS	TYP(1)	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF, See 图 7-3	150	ns
t_{PHL}	Propagation delay time, high- to low-level output	C_L = 150 pF, See 图 7-3	150	ns
t_{en}	Output enable time	C_L = 150 pF, R_L = 3 kΩ, See 图 7-4	200	ns
t_{dis}	Output disable time	C_L = 150 pF, R_L = 3 kΩ, See 图 7-4	200	ns
$t_{sk(p)}$	Pulse skew(2)	See 图 7-3	50	ns

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Test conditions are C1 – C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2 – C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

6.12 Switching Characteristics: Auto-Power Down

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TYP(1)	UNIT
t_{valid}	Propagation delay time, low- to high-level output	1	µs
$t_{invalid}$	Propagation delay time, high- to low-level output	30	µs
t_{en}	Supply enable time	100	µs

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

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6.13 Typical Characteristics

T_A = 25° C; V_{CC} = 3.3V

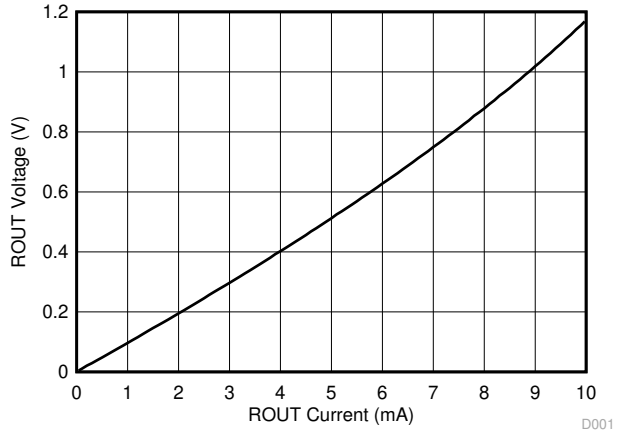


图 6-1. Receiver VOL vs Load Current

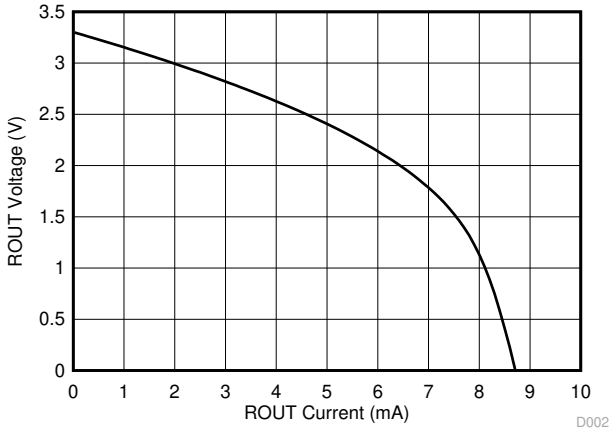


图 6-2. Receiver VOH vs Load Current

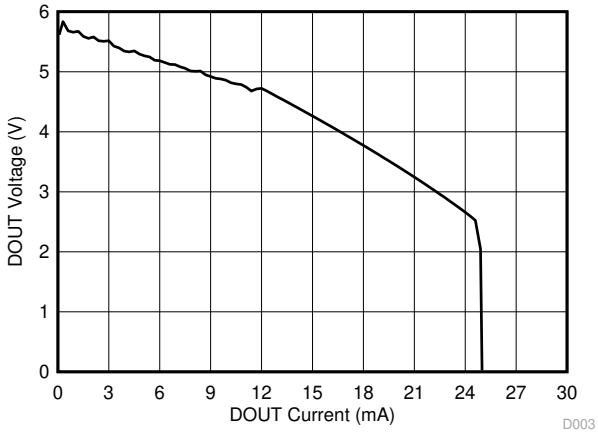


图 6-3. Driver VOH vs Load Current

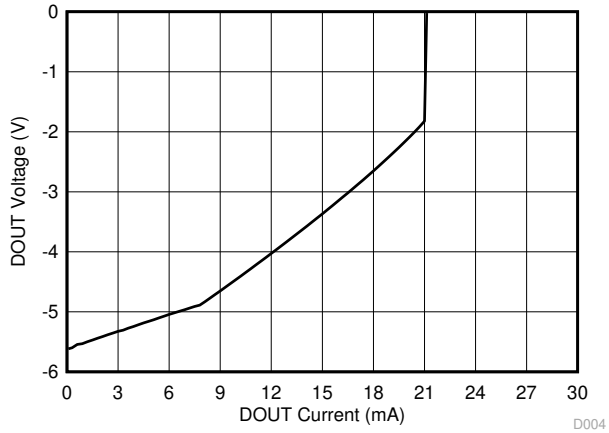
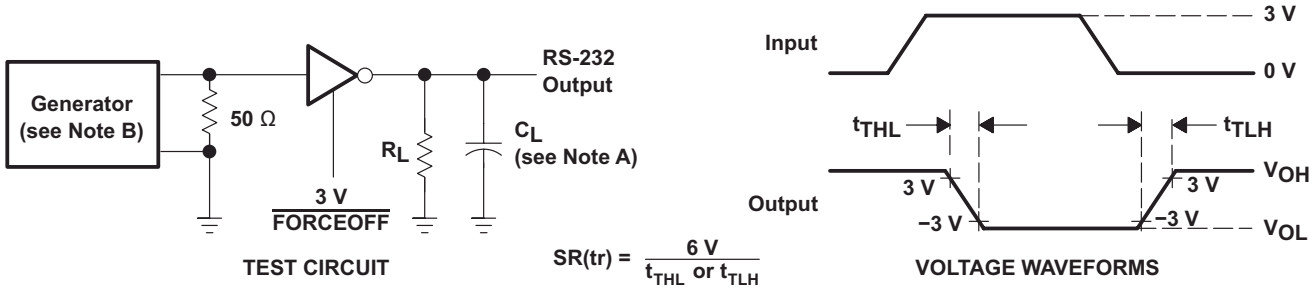


图 6-4. Driver VOL vs Load Current

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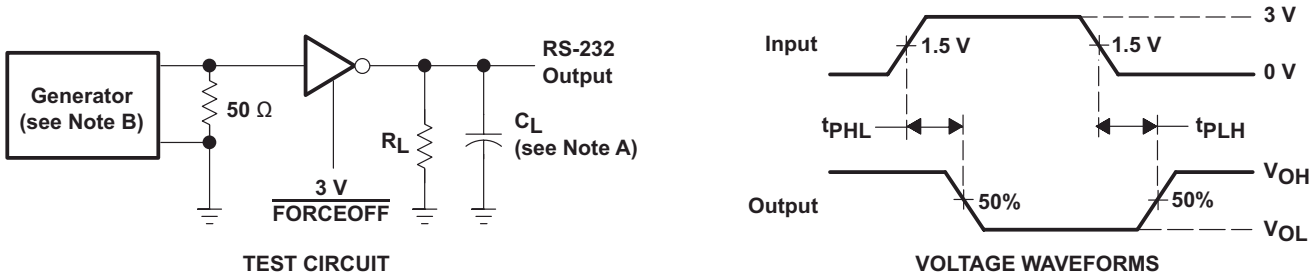
7 Parameter Measurement Information



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbps, Z_O = 50 Ω, 50% duty cycle, $t_r \leqslant$ 10 ns, $t_f \leqslant$ 10 ns.

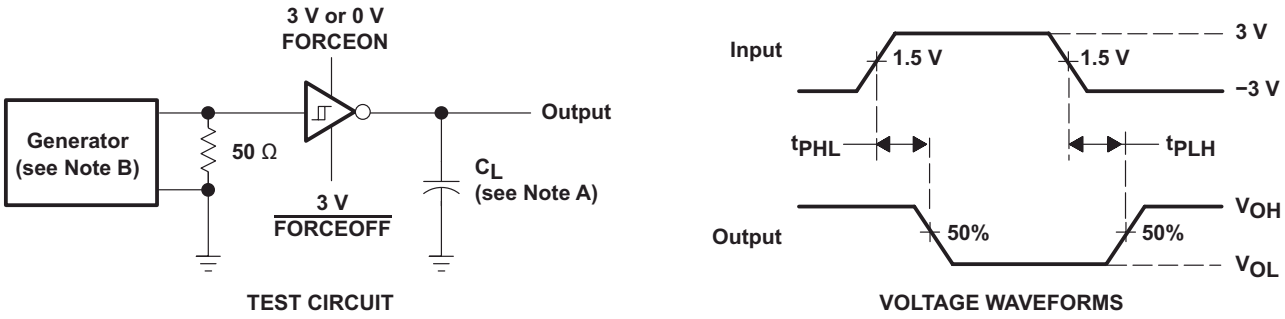
图 7-1. Driver Slew Rate



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbps, Z_O = 50 Ω, 50% duty cycle, $t_r \leqslant$ 10 ns, $t_f \leqslant$ 10 ns.

图 7-2. Driver Pulse Skew

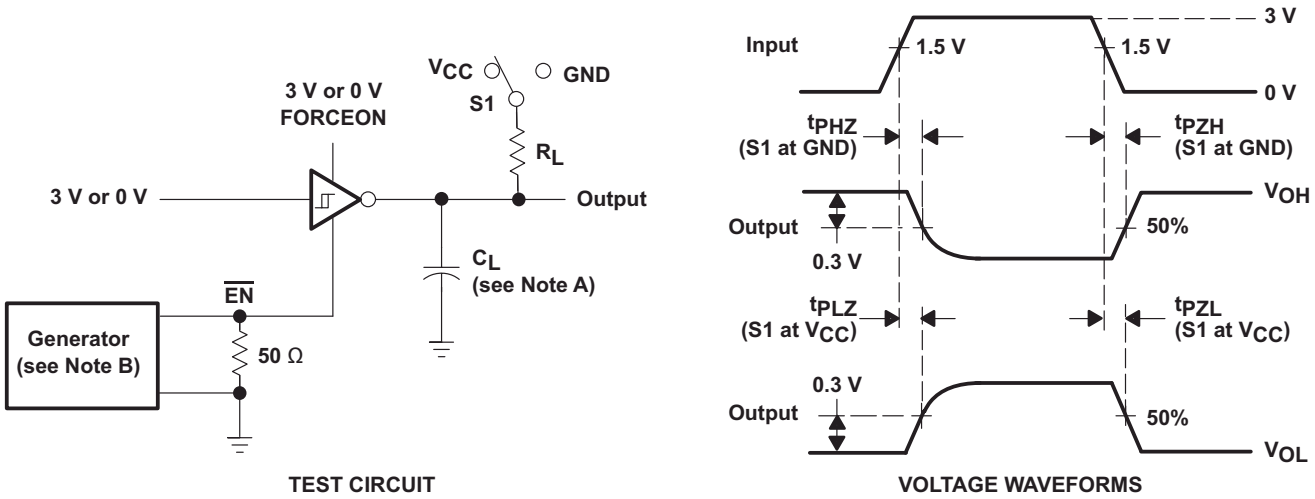


A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \leqslant$ 10 ns, $t_f \leqslant$ 10 ns.

图 7-3. Receiver Propagation Delay Times

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A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \leqslant$ 10 ns, $t_f \leqslant$ 10 ns.

C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

D. t_{PZL} and t_{PZH} are the same as t_{en}.

图 7-4. Receiver Enable and Disable Times

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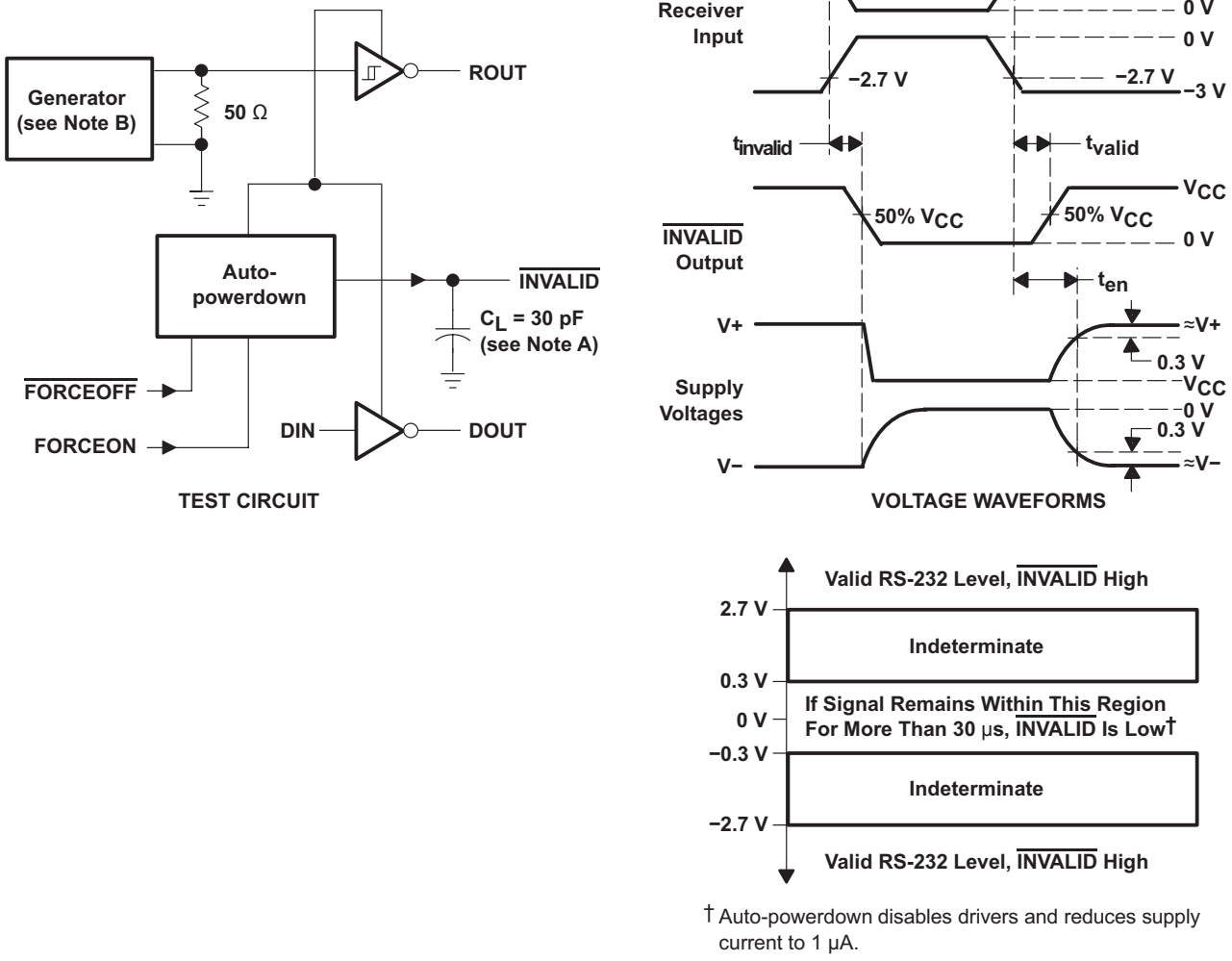


图 7-5. INVALID Propagation Delay Times and Driver Enabling Time

8 Detailed Description

8.1 Overview

The MAX3221E is a single driver, single receiver RS-232 solution operating from a single V_{CC} supply. The RS-232 pins provide IEC 61000-4-2 ESD protection. The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. These devices operate at data signaling rates up to 250 kbit/s and a maximum of 30-V/µs driver output slew rate.

Flexible control options for power management are available when the serial port is inactive. The auto-power-down feature functions when FORCEON is low and $\overline{\text{FORCEOFF}}$ is high. During this mode of operation, if the device does not sense a valid RS-232 signal on the receiver input, the driver output is disabled. If $\overline{\text{FORCEOFF}}$ is set low and $\overline{\text{EN}}$ is high, both the driver and receiver are shut off, and the supply current is reduced to 1 µA. Disconnecting the serial port or turning off the peripheral drivers causes the auto-power-down condition to occur. Auto-power down can be disabled when FORCEON and $\overline{\text{FORCEOFF}}$ are high. With auto-power down enabled, the device is activated automatically when a valid signal is applied to the receiver input. The $\overline{\text{INVALID}}$ output notifies the user if an RS-232 signal is present at the receiver input. $\overline{\text{INVALID}}$ is high (valid data) if the receiver input voltage is greater than 2.7 V or less than –2.7 V, or has been between –0.3 V and 0.3 V for less than 30 µs. $\overline{\text{INVALID}}$ is low (invalid data) if the receiver input voltage is between –0.3 V and 0.3 V for more than 30 µs. See 图 7-1 for receiver input levels.

8.2 Functional Block Diagram

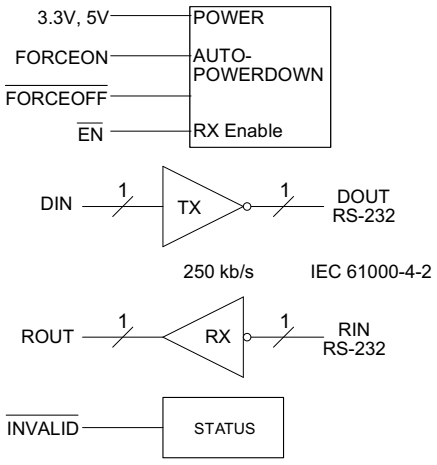


图 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

8.3.1 Power

The power block increases, inverts, and regulates voltage at V+ and V- pins using a charge pump that requires four external capacitors. Auto-power-down feature for driver is controlled by FORCEON and $\overline{\text{FORCEOFF}}$ inputs. Receiver is controlled by $\overline{\text{EN}}$ input. When MAX3221E is unpowered, it can be safely connected to an active remote RS-232 device.

8.3.2 RS-232 Driver

One driver interfaces standard logic levels to RS-232 levels. DIN input must be valid high or low.

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8.3.3 RS-232 Receiver

One receiver interfaces RS-232 levels to standard logic levels. An open input results in a high output on ROUT. RIN input includes an internal standard RS-232 load. A logic high input on the $\overline{EN}$ pin shuts down the receiver output.

8.3.4 RS-232 Status

The $\overline{INVALID}$ output goes low when RIN input is unpowered for more than 30 µs. The $\overline{INVALID}$ output goes high when receiver has a valid input. The $\overline{INVALID}$ output is active when V_{cc} is powered irregardless of FORCEON and $\overline{FORCEOFF}$ inputs (see 表 8-3).

8.4 Device Functional Modes

表 8-1, 表 8-2, and 表 8-3 show the behavior of the driver, receiver, and $\overline{INVALID}$ features under all possible relevant combinations of inputs.

表 8-1. Function Tables Each Driver(1)

INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	$\overline{FORCEOFF}$	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-power down disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-power down enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-power down feature
H	L	H	No	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

表 8-2. Each Receiver(1)

INPUTS			OUTPUT ROUT
RIN	$\overline{EN}$	VALID RIN RS-232 LEVEL	
L	L	X	H
H	L	X	L
X	H	X	Z
Open	L	No	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = disconnected input or connected driver off

表 8-3. $\overline{INVALID}$ (1)

INPUTS				OUTPUT
RIN	FORCEON	$\overline{FORCEOFF}$	$\overline{EN}$	$\overline{INVALID}$
L	X	X	X	H
H	X	X	X	H
Open	X	X	X	L

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

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9 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

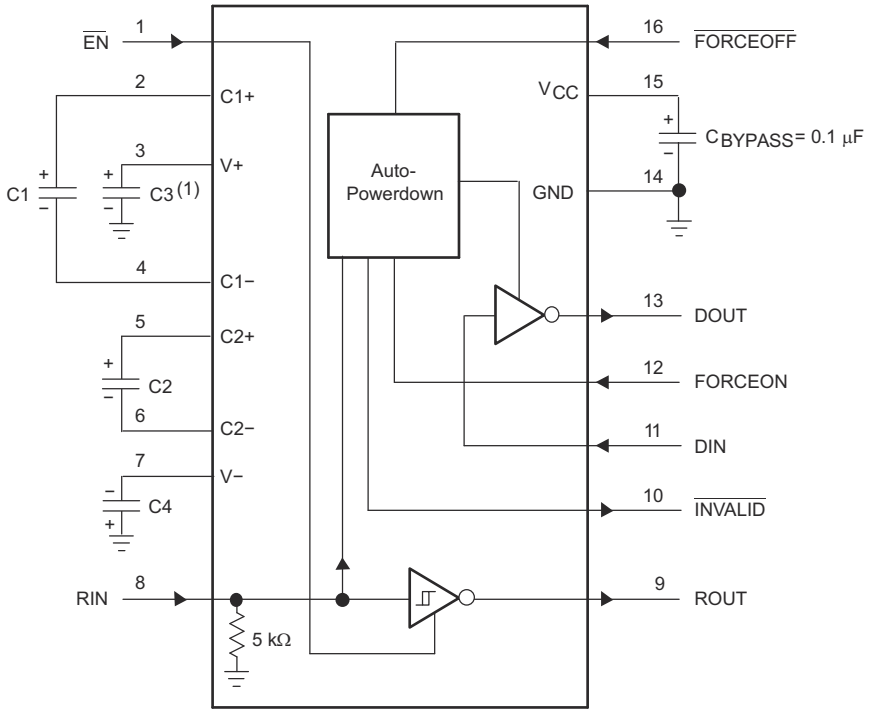
9.1 Application Information

The MAX3221E line driver and receiver is a specialized device for 3-V to 5.5-V RS-232 communication applications. This application is a generic implementation of this device with all required external components. For proper operation, add capacitors as shown in 图 9-1.

9.2 Typical Application

ROUT and DIN connect to UART or general purpose logic lines. FORCEON and $\overline{\text{FORCEOFF}}$ may be connected general purpose logic lines or tied to ground or V_{CC}. $\overline{\text{INVALID}}$ may be connected to a general purpose logic line or left unconnected. RIN and DOUT lines connect to a RS-232 connector or cable. DIN, FORCEON, and $\overline{\text{FORCEOFF}}$ inputs must not be left unconnected.

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(1) C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 µF	0.1 µF
5 V ± 0.5 V	0.047 µF	0.33 µF
3 V to 5.5 V	0.1 µF	0.47 µF

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图 9-1. Typical Operating Circuit and Capacitor Values

9.2.1 Design Requirements

- Recommended V_{CC} is 3.3 V or 5 V.
  - 3 V to 5.5 V is also possible
- Maximum recommended bit rate is 250 kbps.
- Use capacitors as shown in 图 9-1.

9.2.2 Detailed Design Procedure

- DIN, $\overline{\text{FORCEOFF}}$ and FORCEON inputs must be connected to valid low or high logic levels.
- Select capacitor values based on VCC level for best performance.

9.2.3 Application Curves

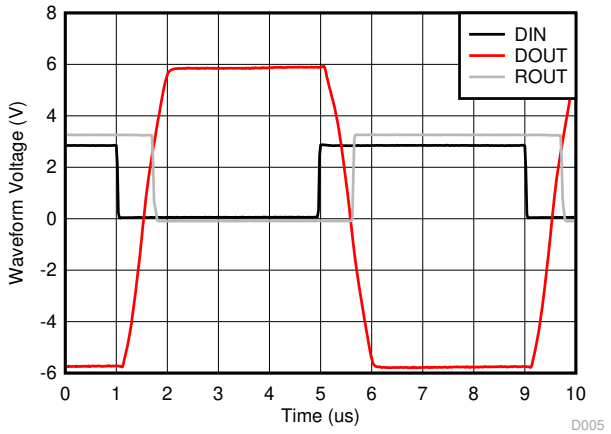


图 9-2. Loopback Waveforms V_{CC} = 3.3 V, Data Rate 250 kbit/s

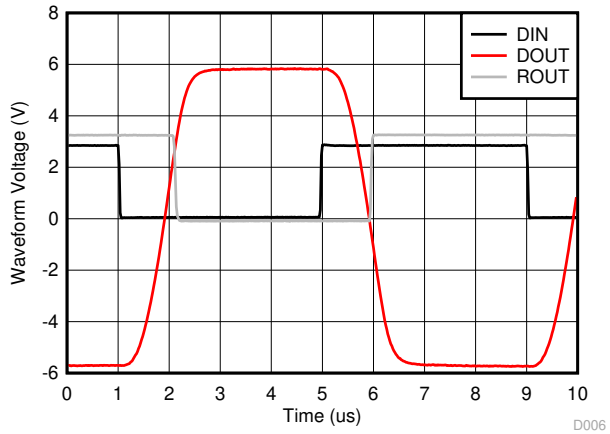


图 9-3. Loopback Waveforms with 1-nF load V_{CC} = 3.3 V, Data Rate 250 kbit/s

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10 Power Supply Recommendations

TI recommends a 0.1-µF capacitor to filter noise on the power supply pin. For additional filter capability, a 0.01-µF capacitor may be added in parallel as well. Power supply input voltage is recommended to be any valid level in 节 6.4.

11 Layout

11.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times. Make the impedance from MAX3221E ground pin and circuit board's ground plane as low as possible for best ESD performance. Use wide metal and multiple vias on both sides of ground pin.

11.2 Layout Example

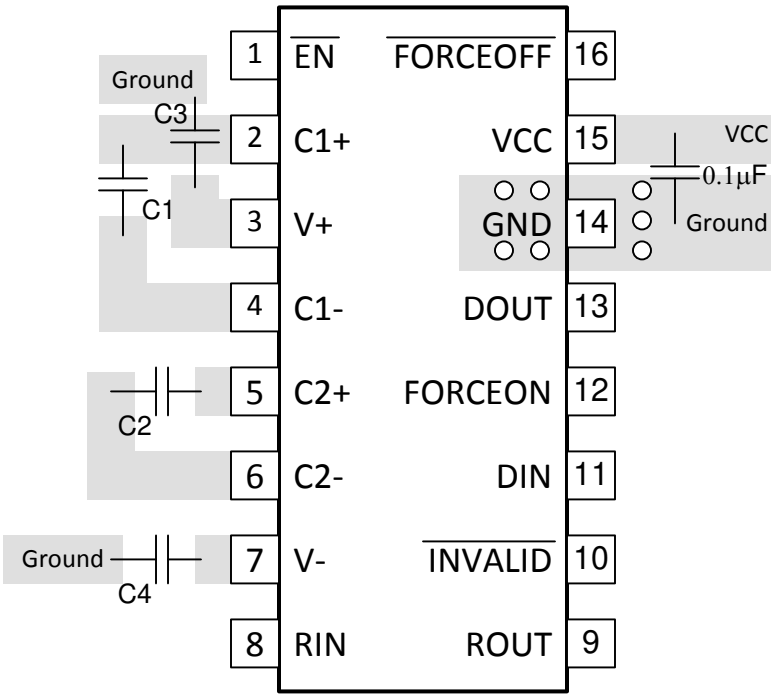


图 11-1. MAX3221E Layout Example

12 Device and Documentation Support

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.3 Trademarks

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12.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX3221ECDB	NRND	SSOP	DB	16	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP221EC	
MAX3221ECDBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP221EC	Samples
MAX3221ECDBRG4	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP221EC	Samples
MAX3221ECPW	NRND	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP221EC	
MAX3221ECPWE4	NRND	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP221EC	
MAX3221ECPWG4	NRND	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP221EC	
MAX3221ECPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP221EC	Samples
MAX3221EIDB	NRND	SSOP	DB	16	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EI	
MAX3221EIDBG4	NRND	SSOP	DB	16	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EI	
MAX3221EIDBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EI	Samples
MAX3221EIDBRG4	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EI	Samples
MAX3221EIPW	NRND	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EI	
MAX3221EIPWE4	NRND	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EI	
MAX3221EIPWG4	NRND	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EI	
MAX3221EIPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	MP221EI	Samples
MAX3221EIPWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

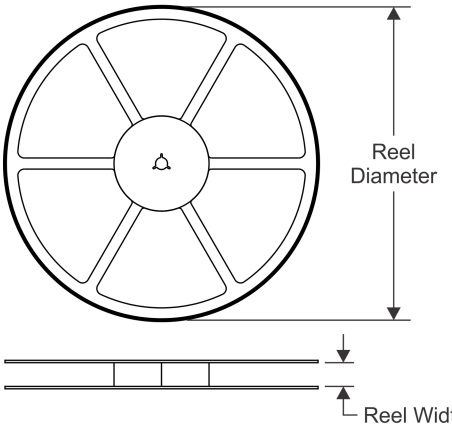
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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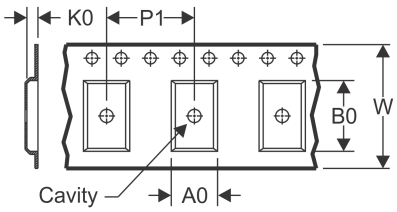
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

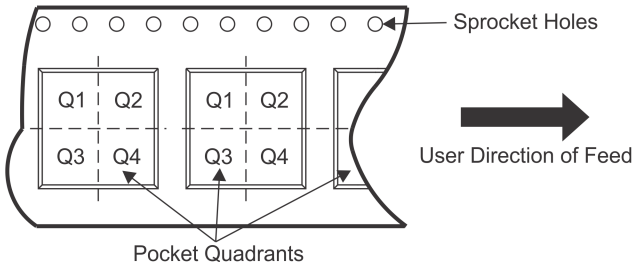


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

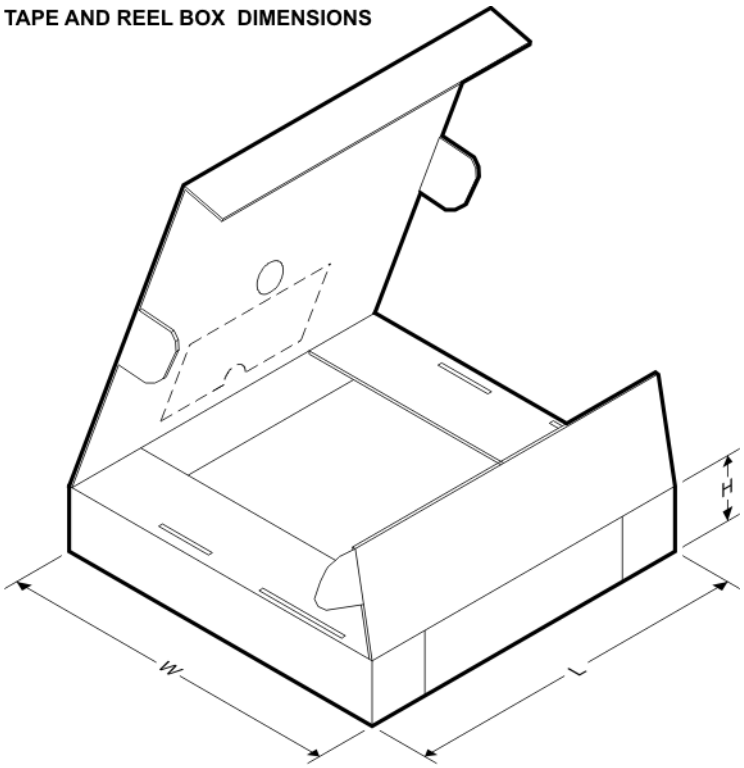
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX3221ECDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
MAX3221ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3221ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3221EIDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
MAX3221EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3221EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3221EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3221EIPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3221EIPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

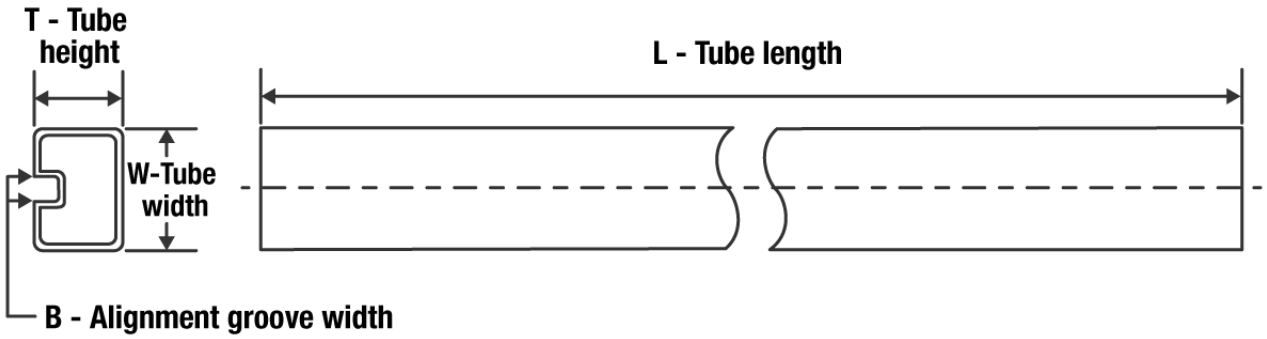
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX3221ECDBR	SSOP	DB	16	2000	853.0	449.0	35.0
MAX3221ECPWR	TSSOP	PW	16	2000	853.0	449.0	35.0
MAX3221ECPWR	TSSOP	PW	16	2000	853.0	449.0	35.0
MAX3221EIDBR	SSOP	DB	16	2000	853.0	449.0	35.0
MAX3221EIPWR	TSSOP	PW	16	2000	364.0	364.0	27.0
MAX3221EIPWR	TSSOP	PW	16	2000	853.0	449.0	35.0
MAX3221EIPWR	TSSOP	PW	16	2000	853.0	449.0	35.0
MAX3221EIPWRG4	TSSOP	PW	16	2000	853.0	449.0	35.0
MAX3221EIPWRG4	TSSOP	PW	16	2000	853.0	449.0	35.0

TUBE



*All dimensions are nominal

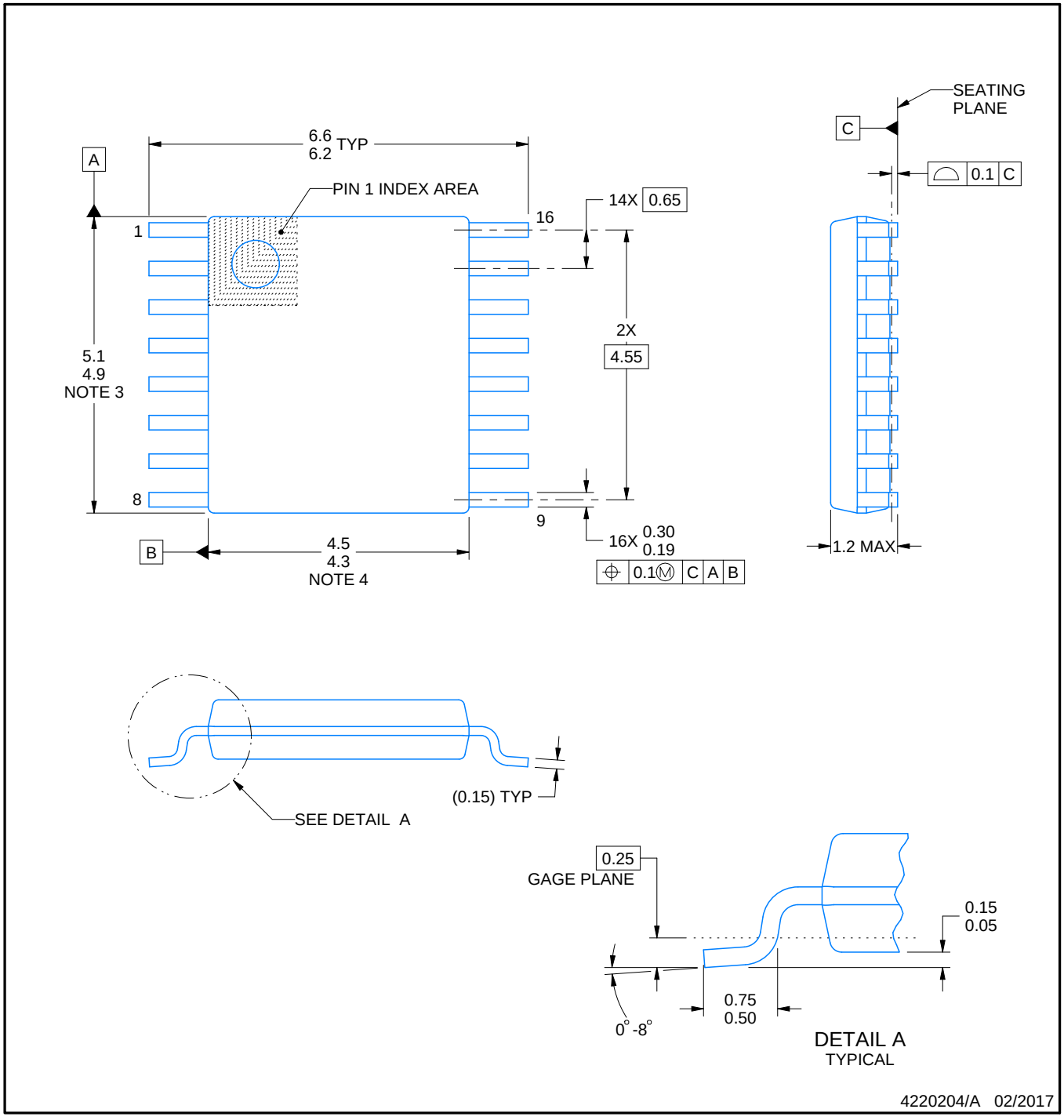
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MAX3221ECDB	DB	SSOP	16	80	530	10.5	4000	4.1
MAX3221ECPW	PW	TSSOP	16	90	530	10.2	3600	3.5
MAX3221ECPWE4	PW	TSSOP	16	90	530	10.2	3600	3.5
MAX3221ECPWG4	PW	TSSOP	16	90	530	10.2	3600	3.5
MAX3221EIDB	DB	SSOP	16	80	530	10.5	4000	4.1
MAX3221EIDBG4	DB	SSOP	16	80	530	10.5	4000	4.1
MAX3221EIPW	PW	TSSOP	16	90	530	10.2	3600	3.5
MAX3221EIPWE4	PW	TSSOP	16	90	530	10.2	3600	3.5
MAX3221EIPWG4	PW	TSSOP	16	90	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0016A

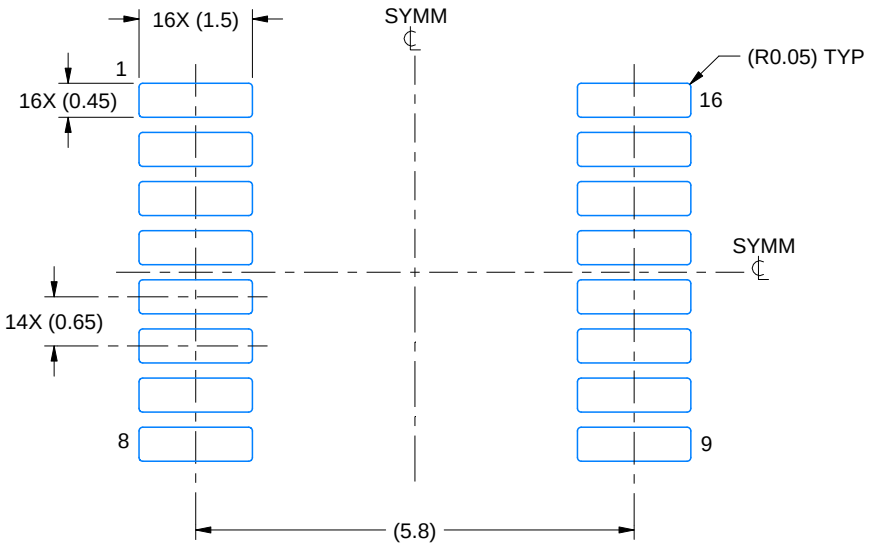
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

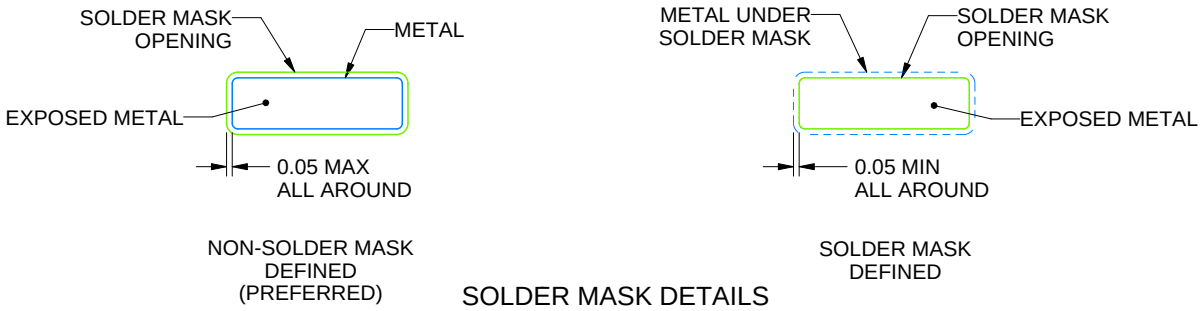


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

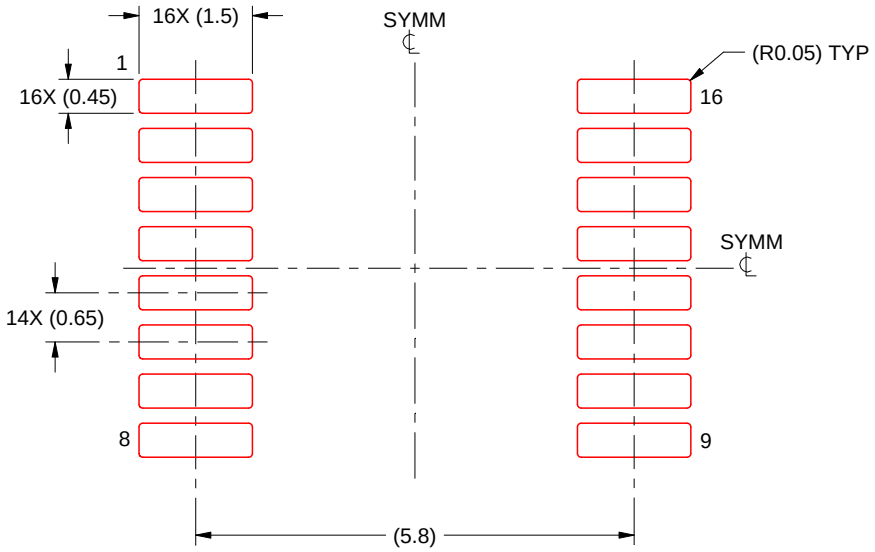


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

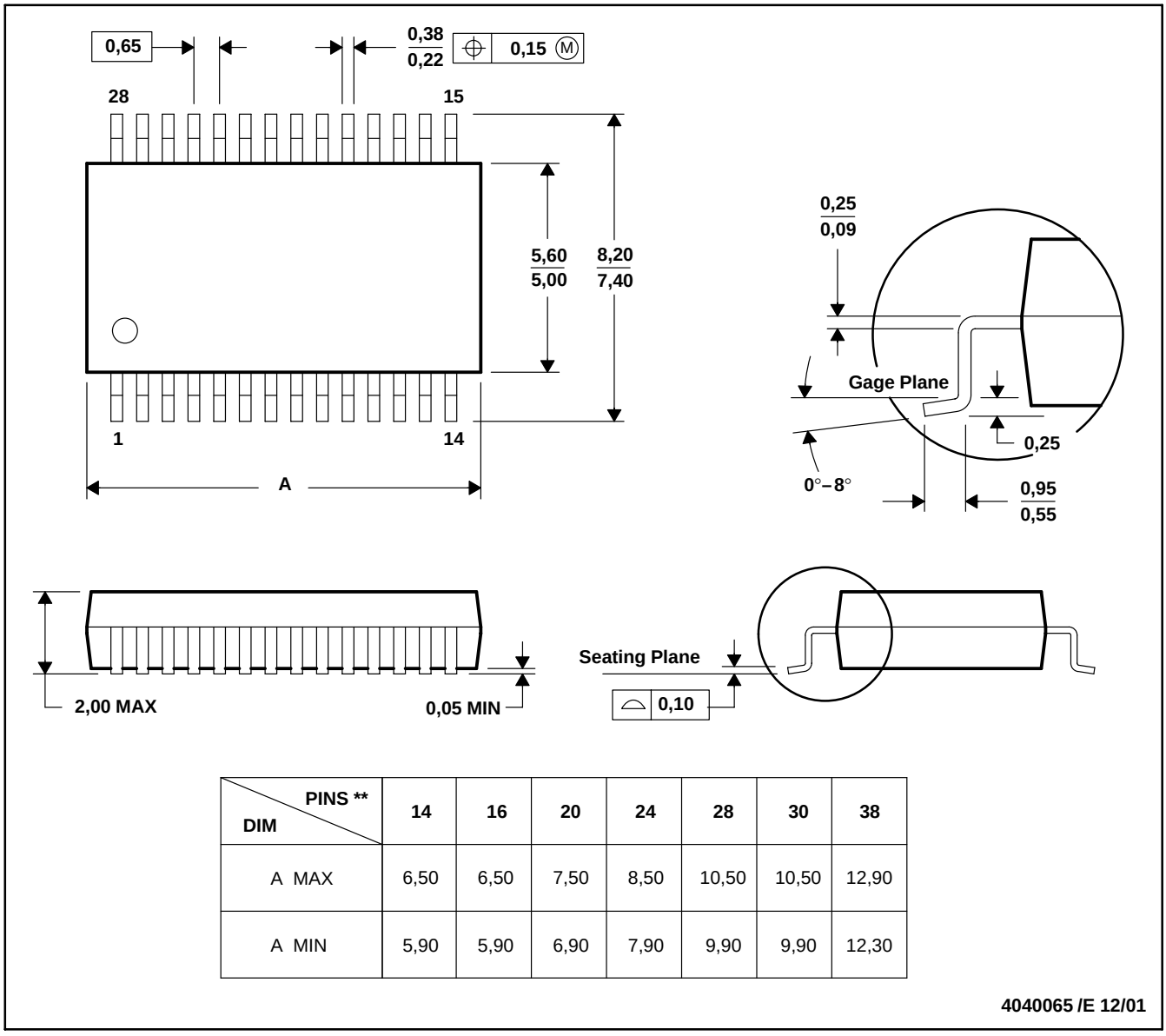
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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