MSP430F67791, MSP430F67781, MSP430F67771, MSP430F67761, MSP430F67751
MSP430F67691, MSP430F67681, MSP430F67671, MSP430F67661, MSP430F67651
MSP430F67491, MSP430F67481, MSP430F67471, MSP430F67461, MSP430F67451
ZHCSAU6D – NOVEMBER 2012 – REVISED SEPTEMBER 2018

# MSP430F677x1、MSP430F676x1、MSP430F674x1 多相位计量 SoC

## 1 器件概述

### 1.1 特性

- 相位电流在超过 2000:1 的动态范围内精度 < 0.1%
- 符合或者超过美国国家标准学会 (ANSI) C12.20 和国际电工委员会 (IEC) 62053 标准
- 支持诸如电流变压器、罗式线圈或分流器等多种传感器
- 针对高达 3 相位加上中线相位的电源管理
- 为校准提供有源能量和无功能量的专用脉冲输出引脚
- 每相位或累加相位的四象限测量
- 精确相位角测量
- 针对电流变压器的数字相位校正
- 温度补偿电能测量
- 使用单一校准的 40Hz 至 70Hz 线路频率范围
- 支持自动切换的灵活电源选项
- AC 主电源故障期间，显示运行在极低功耗下：LMP3 时 为 3μA
- 具有高达 320 段对比度控制的 LCD 驱动器
- 具有晶振偏移校准和温度补偿功能的受密码保护的实时时钟 (RTC)
- 集成安全模块以支持防篡改
- 用于智能仪表实施的多个通信接口
- 具有 32 位复用器的高性能 25MHz CPU
- 宽输入电源电压范围：3.6V 到低至 1.8V
- 能量管理期间超低功耗
  - 10MHz 运行时 (3V) 为 2.9mW
- 多个低功耗模式
  - 待机模式 (LPM3)：3V 时为 2.1μA，在不到 5μs 的时间内唤醒
  - RTC 模式 (LPM3.5)：3V 时为 0.34μA
  - 关断模式 (LPM4.5)：3V 时为 0.18μA
- 高达 512KB 的单周期闪存
- 高达 32KB 支持单周期访问的 RAM
- 多达 7 个支持差分输入和可变增益的独立 24 位 Σ-Δ ADC
- 系统 10 位 200ksps ADC
  - 6 条电源和温度传感器测量增强型通道
- 6 个增强型通信端口
  - 可在 4 个异步收发器 (UART)，6 个串行外设接口 (SPI) 和 2 个 I²C 接口间配置
- 4 个 16 位计时器，共有 9 个捕捉/比较寄存器
- 具有 90 个 I/O 引脚的 128 引脚薄型方形扁平 (LQFP)(PEU) 封装
- 具有 62 个 I/O 引脚的 100 引脚 LQFP (PZ) 封装
- -40°C 至 85°C 的工业温度范围
- 三相电子电表开发工具（另请参阅 工具与软件）
  - EVM430-F6779 和应用手册
  - 适用于 MSP430™ MCU 的电能测量设计中心

### 1.2 应用

- 三相电子电表
- 公用事业仪表计量
- 能量监控

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

## 1.3 说明

TI MSP430F677x1 系列多相位计量 SoC 是用于收费仪表的功能强大的高度集成解决方案，这些解决方案使用很少的外部组件即可提供精准计量并实现低系统成本。F677x1 系列器件使用具有 32 位乘法器的低功耗 MSP430 CPU 来执行所有能量计算、计量 应用 （如费率管理以及与 AMR 和 AMI 模块的通信）。

F677x1 器件采用 TI 的 24 位 Σ-Δ 转换器技术，其精度优于 0.1%。系列产品成员包括高达 512KB 的闪存、32KB 的 RAM 以及一个最高支持 320 段的 LCD 控制器。

F677x1 器件的超低功耗属性意味着可以最大限度地减小系统电源，以降低总体成本。最低待机功率意味着可以最大限度地减少备用电能存储，并在主电源发生故障时更长时间地保留关键数据。

F677x1 系列器件执行 TI 电能测量软件库，该软件库计算所有相关电能和功率结果。电能测量软件库随 F677x1 器件一起免费提供。还提供工业标准开发工具与软件平台，以在全球范围内加快符合所有 ANSI 和 IEC 标准的仪表的开发。

有关完整的模块说明，请参阅*《MSP430F5xx 和 MSP430F6xx 系列用户指南》*

器件信息(1)

| 器件型号 | 封装 | 封装尺寸(2) |
|---|---|---|
| MSP430F67791IPEU | LQFP (128) | 20mm × 14mm |
| MSP430F67791IPZ | LQFP (100) | 14mm x 14mm |

(1) 要获得最新的器件、封装和订购信息，请参见*封装选项附录*（节 8），或者访问 TI 网站 www.ti.com.cn。
(2) 这里显示的尺寸为近似值。要获得包含误差值的封装尺寸，请参见*机械数据*（节 8）。


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## 1.4 应用图

图 1-1 显示了典型应用图。

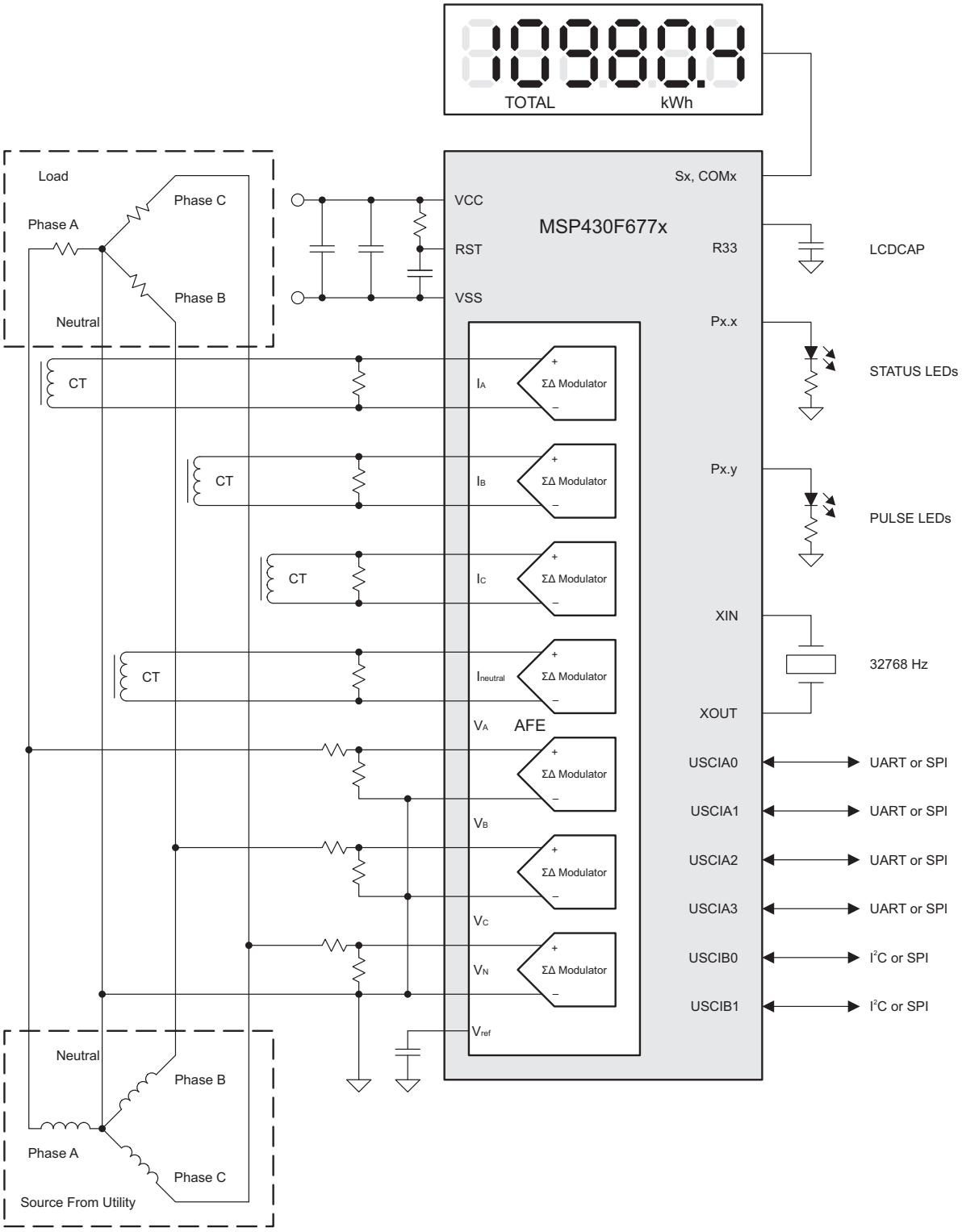



图 **1-1.** 使用**MSP430F677x1** 的三相四线制星形连接

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## 2 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

**Changes from December 19, 2013 to September 28, 2018** **Page**

- 通篇更改了文档格式，其中包括添加章节编号 ..... 1
- 在 *中更新了指向开发工具和设计中心的链接特性* ..... 1
- 添加了 *器件信息 表* ..... 2
- Added Section 3, *Device Comparison*, and moved Table 3-1 to it ..... 7
- Added Section 3.1, *Related Products* ..... 8
- Added Section 4 and moved pinouts and terminal functions tables to it ..... 9
- Corrected the port number (P4.2) on pin 61 in Figure 4-2, *100-Pin PZ Package (Top View)* ..... 11
- Added note to P1.3/ADC10CLK/A3 (pin 8) in Table 4-3, *Terminal Functions – PEU Package* ..... 13
- Added typical conditions statements at the beginning of Section 5, *Specifications* ..... 26
- Moved all electrical specifications to Section 5 ..... 26
- Added SD24_B input pins and AUXVCCx pins to exception list on "Voltage applied to pins" parameter, and added SD24_B input pin limits in "Diode current at pins" parameter in Section 5.1, *Absolute Maximum Ratings* ..... 26
- Added Section 5.2, *ESD Ratings* ..... 26
- Added note to $C_{VCORE}$ ..... 26
- Added Section 5.7, *Thermal Packaging Characteristics* ..... 31
- Changed the TYP value of the $C_{L,eff}$ parameter with Test Conditions of "XTS = 0, XCAPx = 0" from 2 pF to 1 pF in Section 5.16, *Crystal Oscillator, XT1, Low-Frequency Mode* ..... 36
- Updated notes (1) and (2) and added note (3) in Section 5.26, *Wake-up Times From Low-Power Modes and Reset* ..... 41
- Corrected the names of the AUXVCC1, AUXVCC2, and AUXVCC3 pins in Auxiliary Supplies tables ..... 42
- Corrected the bit name in the Test Conditions of the $R_{CHARGE}$ parameter (changed CHCx to AUXCHCx) in Section 5.34, *Auxiliary Supplies, Charge Limiting Resistor* ..... 43
- Replaced $f_{Frame}$ parameter with $f_{LCD}$, $f_{FRAME,4mux}$, and $f_{FRAME,8mux}$ parameters in Section 5.46, *LCD_C Recommended Operating Conditions* ..... 50
- On the $V_{ID,FS}$ parameter in Section 5.48, *SD24_B Power Supply and Recommended Operating Conditions*: Changed the MIN value from "$V_{REF}$/GAIN" to "–$V_{REF}$/GAIN"; Removed "Unipolar mode" test condition (mode is not supported) ..... 52
- Removed ADC10DIV from the formula for the TYP value in the second row of the $t_{CONVERT}$ parameter in Section 5.57, *10-Bit ADC Switching Characteristics*, because ADC10CLK is after division ..... 58
- Changed Test Conditions for all parameters in Section 5.58, *10-Bit ADC Linearity Parameters*: Removed "$V_{REF-}$"; Changed from "$(V_{eREF+} – V_{eREF-})$min ≤ $(V_{eREF+} – V_{eREF-})$" to "1.4 V ≤ $(V_{eREF+} – V_{eREF-})$"; Changed from "$C_{VREF+}$ = 20 pF" to "$C_{VeREF+}$ = 20 pF"; Added "$C_{VeREF+}$ = 20 pF" to $E_I$; Added "ADC10SREFx = 11b" to $E_T$ and $E_G$ .. 59
- Removed "$V_{REF-}$" from the Test Conditions for the $V_{eREF+}$, $V_{eREF-}$, and $(V_{eREF+} – V_{eREF-})$ parameters in Section 5.59, *10-Bit ADC External Reference* ..... 59
- Changed MIN value of $AV_{CC(min)}$ parameter with Test Conditions of "REFVSEL = {0} for 1.5 V" from 2.2 V to 1.8 V in Section 5.60, *REF Built-In Reference* ..... 60
- Changed the MAX value of the $t_{EN_CMP}$ parameter with Test Conditions of "CBPWRMD = 10" from 50 µs to 100 µs in Section 5.61, *Comparator_B* ..... 61
- Throughout document, changed all instances of "bootstrap loader" to "bootloader" ..... 72
- Corrected spelling of NMIIFG in Table 6-13, *System Module Interrupt Vector Registers* ..... 78
- 添加了节 7并将 *开发工具支持*、*器件和开发工具命名规则* 和 *商标* 部分移到这里 ..... 157
- 将先前的 *开发工具支持* 部分替换为节 7.3 *工具与软件* ..... 159
- 增加了节 8，*机械，封装和可订购信息* ..... 165


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# 3 Device Comparison

Table 3-1 summarizes the available family members.

**Table 3-1. Device Comparison(1)(2)**

| DEVICE | FLASH (KB) | SRAM (KB) | SD24_B CONVERTERS | ADC10_A CHANNELS | Timer_A(3) | eUSCI_A: UART, IrDA, SPI | eUSCI_B: SPI, I²C | I/Os | PACKAGE |
|---|---|---|---|---|---|---|---|---|---|
| MSP430F67791IPEU | 512 | 32 | 7 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67781IPEU | 512 | 16 | 7 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67771IPEU | 256 | 32 | 7 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67761IPEU | 256 | 16 | 7 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67751IPEU | 128 | 16 | 7 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67691IPEU | 512 | 32 | 6 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67681IPEU | 512 | 16 | 6 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67671IPEU | 256 | 32 | 6 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67661IPEU | 256 | 16 | 6 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67651IPEU | 128 | 16 | 6 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67491IPEU | 512 | 32 | 4 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67481IPEU | 512 | 16 | 4 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67471IPEU | 256 | 32 | 4 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67461IPEU | 256 | 16 | 4 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67451IPEU | 128 | 16 | 4 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 90 | 128 PEU |
| MSP430F67791IPZ | 512 | 32 | 7 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |
| MSP430F67781IPZ | 512 | 16 | 7 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |
| MSP430F67771IPZ | 256 | 32 | 7 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |
| MSP430F67761IPZ | 256 | 16 | 7 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |
| MSP430F67751IPZ | 128 | 16 | 7 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |
| MSP430F67691IPZ | 512 | 32 | 6 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |
| MSP430F67681IPZ | 512 | 16 | 6 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |
| MSP430F67671IPZ | 256 | 32 | 6 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |
| MSP430F67661IPZ | 256 | 16 | 6 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |
| MSP430F67651IPZ | 128 | 16 | 6 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |
| MSP430F67491IPZ | 512 | 32 | 4 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |
| MSP430F67481IPZ | 512 | 16 | 4 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |
| MSP430F67471IPZ | 256 | 32 | 4 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |
| MSP430F67461IPZ | 256 | 16 | 4 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |
| MSP430F67451IPZ | 128 | 16 | 4 | 6 ext, 2 int | 3, 2, 2, 2 | 4 | 2 | 62 | 100 PZ |

(1) For the most current device, package, and ordering information, see the *Package Option Addendum* in 节 8, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.

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## 3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

**Products for TI Microcontrollers** TI's low-power and high-performance MCUs, with wired and wireless connectivity options, are optimized for a broad range of applications.

**Products for MSP430 Ultra-Low-Power Microcontrollers** One platform. One ecosystem. Endless possibilities. Enabling the connected world with innovations in ultra-low-power microcontrollers with advanced peripherals for precise sensing and measurement.

**Companion Products for MSP430F67791** Review products that are frequently purchased or used with this product.

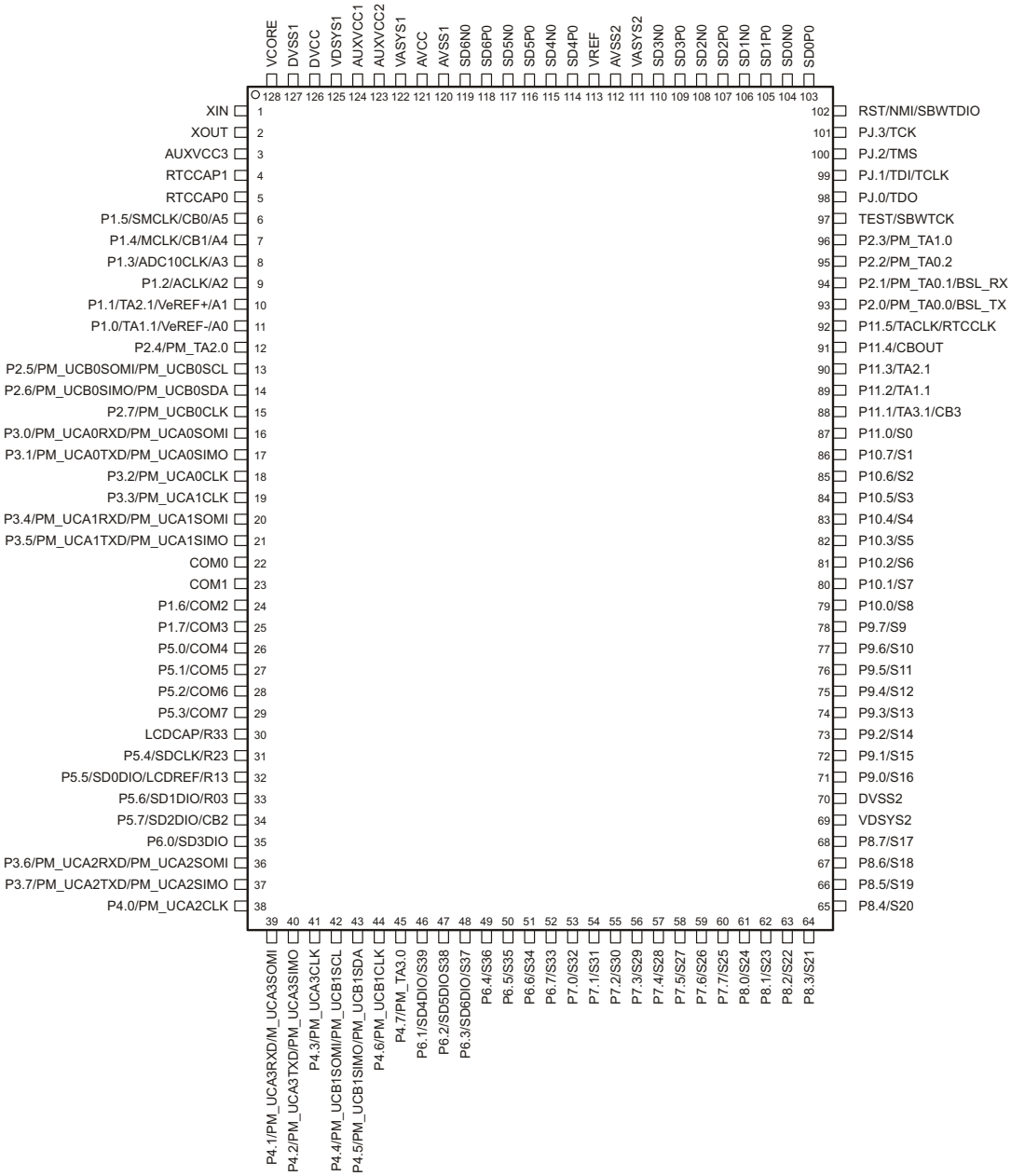
**Reference Designs for MSP430F67791** The TI Designs Reference Design Library is a robust reference design library that spans analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market.


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# 4 Terminal Configuration and Functions

## 4.1 Pin Diagrams

Figure 4-1 shows the pinout for the MSP430F677x1 devices in the 128-pin PEU package. Table 4-1 lists the differences among the pinouts for the MSP430F677x1, MSP430F676x1, and MSP430F674x1 devices.




A. The secondary digital functions on Ports P2, P3 and P4 are fully mappable. This pinout shows only the default mapping. See Table 6-11 for details.

B. The pair of pins VDSYS1 and VDSYS2, VASYS1 and VASYS2 must be connected externally on the board for proper device operation.

C. **CAUTION:** The LCDCAP/R33 pin must be connected to DVSS if it is not used.

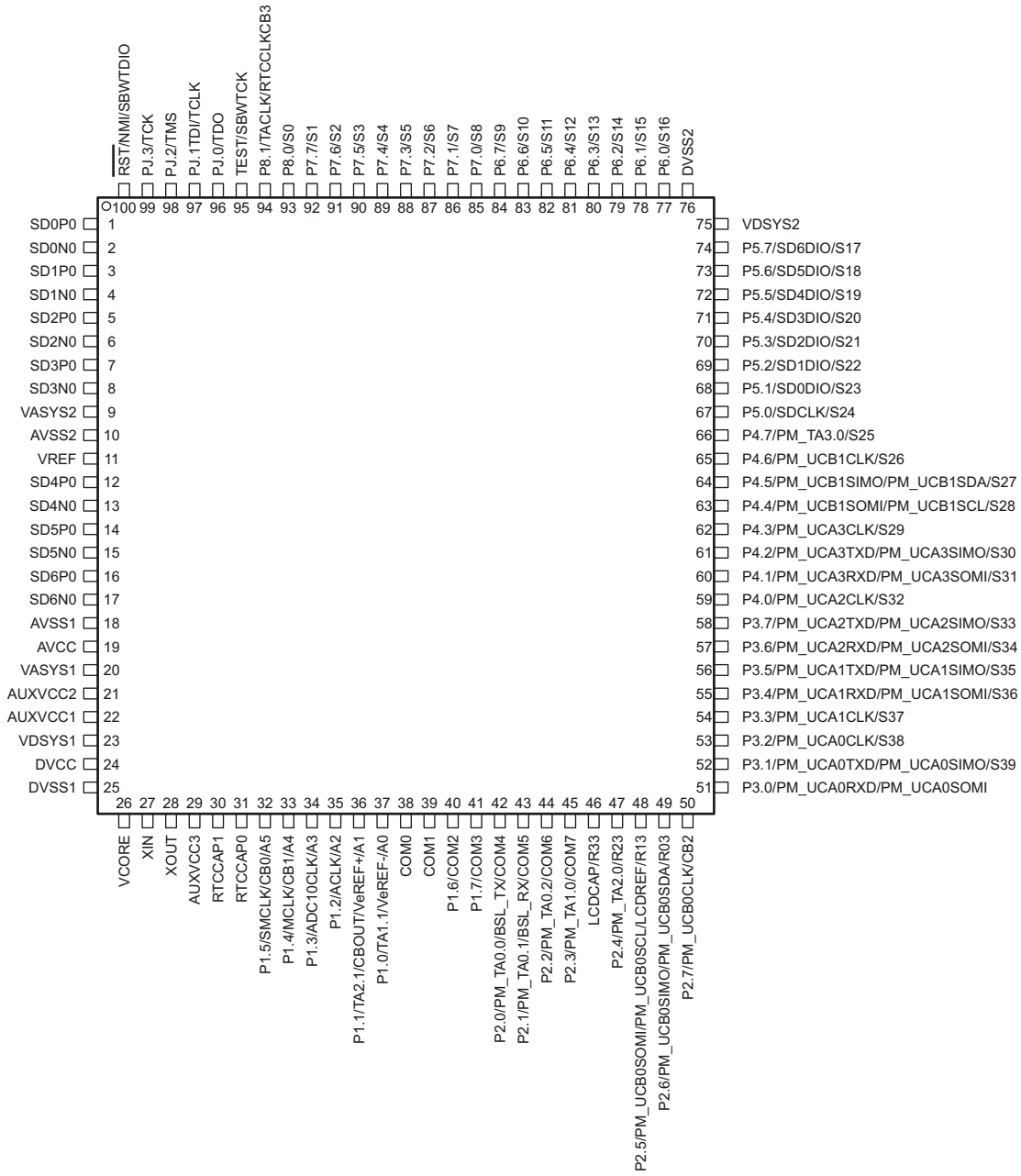
**Figure 4-1. 128-Pin PEU Package (Top View)**

**Table 4-1. Pinout Differences for MSP430F677x1IPEU, MSP430F676x1IPEU, and MSP430F674x1IPEU**

| PIN NUMBER | PIN NAME | | |
|---|---|---|---|
| | MSP430F677x1IPEU | MSP430F676x1IPEU | MSP430F674x1IPEU |
| 46 | P6.1/SD4DIO/S39 | P6.1/SD4DIO/S39 | P6.1/S39 |
| 47 | P6.2/SD5DIO/S38 | P6.2/SD5DIO/S38 | P6.2/S38 |
| 48 | P6.3/SD6DIO/S37 | P6.3/S37 | P6.3/S37 |
| 113 | VREF | VREF | VREF |
| 114 | SD4P0 | SD4P0 | NC |
| 115 | SD4N0 | SD4N0 | NC |
| 116 | SD5P0 | SD5P0 | NC |
| 117 | SD5N0 | SD5NO | NC |
| 118 | SD6P0 | NC | NC |
| 119 | SD6N0 | NC | NC |


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Figure 4-2 shows the pinout for the MSP430F677x1 devices in the 100-pin PZ package. Table 4-2 lists the differences among the pinouts for the MSP430F677x1, MSP430F676x1, and MSP430F674x1 devices.




A. The secondary digital functions on Ports P2, P3 and P4 are fully mappable. This pinout shows only the default mapping. See Table 6-11 for details.

B. The pair of pins VDSYS1 and VDSYS2, VASYS1 and VASYS2 must be connected externally on the board for proper device operation.

C. **CAUTION:** The LCDCAP/R33 pin must be connected to DVSS if it is not used.

**Figure 4-2. 100-Pin PZ Package (Top View)**

**Table 4-2. Pinout Differences for MSP430F677x1IPZ, MSP430F676x1IPZ, and MSP430F674x1IPZ**

| PIN NUMBER | PIN NAME | | |
|---|---|---|---|
| | MSP430F677x1IPZ | MSP430F676x1IPZ | MSP430F674x1IPZ |
| 11 | VREF | VREF | VREF |
| 12 | SD4P0 | SD4P0 | NC |
| 13 | SD4N0 | SD4N0 | NC |
| 14 | SD5P0 | SD5P0 | NC |
| 15 | SD5N0 | SD5NO | NC |
| 16 | SD6P0 | NC | NC |
| 17 | SD6N0 | NC | NC |
| 72 | P5.5/SD4DIO/S19 | P5.5/SD4DIO/S19 | P5.5/S19 |
| 73 | P5.6/SD5DIO/S18 | P5.6/SD5DIO/S18 | P5.6/S18 |
| 74 | P5.7/SD6DIO/S17 | P5.7/S17 | P5.7/S17 |


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## 4.2 Signal Descriptions

Table 4-3 describes the signals for devices in the PEU package. See Table 4-4 for the PZ package signal descriptions.

**Table 4-3. Terminal Functions – PEU Package**

| TERMINAL | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| | PEU | | |
| XIN | 1 | I/O | Input terminal for crystal oscillator |
| XOUT | 2 | I/O | Output terminal for crystal oscillator |
| AUXVCC3 | 3 | | Auxiliary power supply AUXVCC3 for back up subsystem |
| RTCCAP1 | 4 | I | External time capture pin 1 for RTC_C |
| RTCCAP0 | 5 | I | External time capture pin 0 for RTC_C |
| P1.5/SMCLK/CB0/A5 | 6 | I/O | General-purpose digital I/O with port interrupt<br>SMCLK clock output<br>Comparator_B input CB0<br>Analog input A5 for 10-bit ADC |
| P1.4/MCLK/CB1/A4 | 7 | I/O | General-purpose digital I/O with port interrupt<br>MCLK clock output<br>Comparator_B input CB1<br>Analog input A4 for 10-bit ADC |
| P1.3/ADC10CLK/A3(2) | 8 | I/O | General-purpose digital I/O with port interrupt<br>ADC10_A clock output<br>Analog input A3 for 10-bit ADC |
| P1.2/ACLK/A2 | 9 | I/O | General-purpose digital I/O with port interrupt<br>ACLK clock output<br>Analog input A2 for 10-bit ADC |
| P1.1/TA2.1/VeREF+/A1 | 10 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA2 CCR1 capture: CCI1A input, compare: Out1 output<br>Positive terminal for the ADC reference voltage for an external applied reference voltage<br>Analog input A1 for 10-bit ADC |
| P1.0/TA1.1/VeREF-/A0 | 11 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA1 CCR1 capture: CCI1A input, compare: Out1 output<br>Negative terminal for the ADC reference voltage for an external applied reference voltage<br>Analog input A0 for 10-bit ADC |
| P2.4/PM_TA2.0 | 12 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: Timer TA2 capture CCR0: CCI0A input, compare: Out0 output |
| P2.5/PM_UCB0SOMI/<br>PM_UCB0SCL | 13 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_B0 SPI slave out master in<br>Default mapping: eUSCI_B0 $I^2C$ clock |
| P2.6/PM_UCB0SIMO/<br>PM_UCB0SDA | 14 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_B0 SPI slave in master out<br>Default mapping: eUSCI_B0 $I^2C$ data |
| P2.7/PM_UCB0CLK | 15 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_B0 clock input/output |

(1) I = input, O = output
(2) Before enabling the analog function (A3), pull this pin low by setting the port function to output low or to input with the internal pulldown resistor enabled.

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**Table 4-3. Terminal Functions – PEU Package (continued)**

| TERMINAL | | I/O[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| | PEU | | |
| P3.0/PM_UCA0RXD/ PM_UCA0SOMI | 16 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_A0 UART receive data<br>Default mapping: eUSCI_A0 SPI slave out master in |
| P3.1/PM_UCA0TXD/ PM_UCA0SIMO | 17 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_A0 UART transmit data<br>Default mapping: eUSCI_A0 SPI slave in master out |
| P3.2/PM_UCA0CLK | 18 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_A0 clock input/output |
| P3.3/PM_UCA1CLK | 19 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_A1 clock input/output |
| P3.4/PM_UCA1RXD/ PM_UCA1SOMI | 20 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_A1 UART receive data<br>Default mapping: eUSCI_A1 SPI slave out master in |
| P3.5/PM_UCA1TXD/ PM_UCA1SIMO | 21 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_A1 UART transmit data<br>Default mapping: eUSCI_A1 SPI slave in master out |
| COM0 | 22 | O | LCD common output COM0 for LCD backplane |
| COM1 | 23 | O | LCD common output COM1 for LCD backplane |
| P1.6/COM2 | 24 | I/O | General-purpose digital I/O with port interrupt<br>LCD common output COM2 for LCD backplane |
| P1.7/COM3 | 25 | I/O | General-purpose digital I/O with port interrupt<br>LCD common output COM3 for LCD backplane |
| P5.0/COM4 | 26 | I/O | General-purpose digital I/O<br>LCD common output COM4 for LCD backplane |
| P5.1/COM5 | 27 | I/O | General-purpose digital I/O<br>LCD common output COM5 for LCD backplane |
| P5.2/COM6 | 28 | I/O | General-purpose digital I/O<br>LCD common output COM6 for LCD backplane |
| P5.3/COM7 | 29 | I/O | General-purpose digital I/O<br>LCD common output COM7 for LCD backplane |
| LCDCAP/R33 | 30 | I/O | LCD capacitor connection<br>Input/output port of most positive analog LCD voltage (V1)<br>**CAUTION**: This pin must be connected to DVSS if not used. |
| P5.4/SDCLK/R23 | 31 | I/O | General-purpose digital I/O<br>SD24_B bit stream clock input/output<br>Input/output port of second most positive analog LCD voltage (V2) |
| P5.5/SD0DIO/ LCDREF/R13 | 32 | I/O | General-purpose digital I/O<br>SD24_B converter 0 bit stream data input/output<br>External reference voltage input for regulated LCD voltage<br>Input/output port of third most positive analog LCD voltage (V3 or V4) |


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**Table 4-3. Terminal Functions – PEU Package (continued)**

| TERMINAL | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| | PEU | | |
| P5.6/SD1DIO/R03 | 33 | I/O | General-purpose digital I/O<br>SD24_B converter 1 bit stream data input/output<br>Input/output port of lowest analog LCD voltage (V5) |
| P5.7/SD2DIO/CB2 | 34 | I/O | General-purpose digital I/O<br>SD24_B converter 2 bit stream data input/output<br>Comparator_B input CB2 |
| P6.0/SD3DIO | 35 | I/O | General-purpose digital I/O<br>SD24_B converter 3 bit stream data input/output |
| P3.6/PM_UCA2RXD/<br>PM_UCA2SOMI | 36 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_A2 UART receive data<br>Default mapping: eUSCI_A2 SPI slave out master in |
| P3.7/PM_UCA2TXD/<br>PM_UCA2SIMO | 37 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_A2 UART transmit data<br>Default mapping: eUSCI_A2 SPI slave in master out |
| P4.0/PM_UCA2CLK | 38 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_A2 clock input/output |
| P4.1/PM_UCA3RXD/<br>PM_UCA3SOMI | 39 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_A3 UART receive data<br>Default mapping: eUSCI_A3 SPI slave out master in |
| P4.2/PM_UCA3TXD/<br>PM_UCA3SIMO | 40 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_A3 UART transmit data<br>Default mapping: eUSCI_A3 SPI slave in master out |
| P4.3/PM_UCA3CLK | 41 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_A3 clock input/output |
| P4.4/PM_UCB1SOMI/<br>PM_UCB1SCL | 42 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_B1 SPI slave out, master in<br>Default mapping: eUSCI_B1 $I^2C$ clock |
| P4.5/PM_UCB1SIMO/<br>PM_UCB1SDA | 43 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_B1 SPI slave in, master out<br>Default mapping: eUSCI_B1 $I^2C$ data |
| P4.6/PM_UCB1CLK | 44 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_B1 clock input/output |
| P4.7/PM_TA3.0 | 45 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: Timer TA3 capture CCR0: CCI0A input, compare: Out0 output |
| P6.1/SD4DIO/S39 | 46 | I/O | General-purpose digital I/O<br>SD24_B converter 4 bit stream data input/output (not available in F674x devices)<br>LCD segment output S39 |
| P6.2/SD5DIO/S38 | 47 | I/O | General-purpose digital I/O<br>SD24_B converter 5 bit stream data input/output (not available in F674x devices)<br>LCD segment output S38 |

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**Table 4-3. Terminal Functions – PEU Package (continued)**

| TERMINAL | | I/O[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. PEU | | |
| P6.3/SD6DIO/S37 | 48 | I/O | General-purpose digital I/O<br>SD24_B converter 6 bit stream data input/output (not available in F674x, F676x devices)<br>LCD segment output S37 |
| P6.4/S36 | 49 | I/O | General-purpose digital I/O<br>LCD segment output S36 |
| P6.5/S35 | 50 | I/O | General-purpose digital I/O<br>LCD segment output S35 |
| P6.6/S34 | 51 | I/O | General-purpose digital I/O<br>LCD segment output S34 |
| P6.7/S33 | 52 | I/O | General-purpose digital I/O<br>LCD segment output S33 |
| P7.0/S32 | 53 | I/O | General-purpose digital I/O<br>LCD segment output S32 |
| P7.1/S31 | 54 | I/O | General-purpose digital I/O<br>LCD segment output S31 |
| P7.2/S30 | 55 | I/O | General-purpose digital I/O<br>LCD segment output S30 |
| P7.3/S29 | 56 | I/O | General-purpose digital I/O<br>LCD segment output S29 |
| P7.4/S28 | 57 | I/O | General-purpose digital I/O<br>LCD segment output S28 |
| P7.5/S27 | 58 | I/O | General-purpose digital I/O<br>LCD segment output S27 |
| P7.6/S26 | 59 | I/O | General-purpose digital I/O<br>LCD segment output S26 |
| P7.7/S25 | 60 | I/O | General-purpose digital I/O<br>LCD segment output S25 |
| P8.0/S24 | 61 | I/O | General-purpose digital I/O<br>LCD segment output S24 |
| P8.1/S23 | 62 | I/O | General-purpose digital I/O<br>LCD segment output S23 |
| P8.2/S22 | 63 | I/O | General-purpose digital I/O<br>LCD segment output S22 |
| P8.3/S21 | 64 | I/O | General-purpose digital I/O<br>LCD segment output S21 |
| P8.4/S20 | 65 | I/O | General-purpose digital I/O<br>LCD segment output S20 |
| P8.5/S19 | 66 | I/O | General-purpose digital I/O<br>LCD segment output S19 |
| P8.6/S18 | 67 | I/O | General-purpose digital I/O<br>LCD segment output S18 |


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**Table 4-3. Terminal Functions – PEU Package (continued)**

| TERMINAL | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. PEU | | |
| P8.7/S17 | 68 | I/O | General-purpose digital I/O<br>LCD segment output S17 |
| VDSYS2(3) | 69 | | Digital power supply for I/Os |
| DVSS2 | 70 | | Digital ground supply |
| P9.0/S16 | 71 | I/O | General-purpose digital I/O<br>LCD segment output S16 |
| P9.1/S15 | 72 | I/O | General-purpose digital I/O<br>LCD segment output S15 |
| P9.2/S14 | 73 | I/O | General-purpose digital I/O<br>LCD segment output S14 |
| P9.3/S13 | 74 | I/O | General-purpose digital I/O<br>LCD segment output S13 |
| P9.4/S12 | 75 | I/O | General-purpose digital I/O<br>LCD segment output S12 |
| P9.5/S11 | 76 | I/O | General-purpose digital I/O<br>LCD segment output S11 |
| P9.6/S10 | 77 | I/O | General-purpose digital I/O<br>LCD segment output S10 |
| P9.7/S9 | 78 | I/O | General-purpose digital I/O<br>LCD segment output S9 |
| P10.0/S8 | 79 | I/O | General-purpose digital I/O<br>LCD segment output S8 |
| P10.1/S7 | 80 | I/O | General-purpose digital I/O<br>LCD segment output S7 |
| P10.2/S6 | 81 | I/O | General-purpose digital I/O<br>LCD segment output S6 |
| P10.3/S5 | 82 | I/O | General-purpose digital I/O<br>LCD segment output S5 |
| P10.4/S4 | 83 | I/O | General-purpose digital I/O<br>LCD segment output S4 |
| P10.5/S3 | 84 | I/O | General-purpose digital I/O<br>LCD segment output S3 |
| P10.6/S2 | 85 | I/O | General-purpose digital I/O<br>LCD segment output S2 |
| P10.7/S1 | 86 | I/O | General-purpose digital I/O<br>LCD segment output S1 |
| P11.0/S0 | 87 | I/O | General-purpose digital I/O<br>LCD segment output S0 |
| P11.1/TA3.1/CB3 | 88 | I/O | General-purpose digital I/O<br>Timer TA3 capture CCR1: CCI1A input, compare: Out1 output<br>Comparator_B input CB3 |

(3) The pins VDSYS1 and VDSYS2 must be connected externally on board for proper device operation.

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**Table 4-3. Terminal Functions – PEU Package (continued)**

| TERMINAL | | I/O[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| | PEU | | |
| P11.2/TA1.1 | 89 | I/O | General-purpose digital I/O<br>Timer TA1 capture CCR1: CCI1A input, compare: Out1 output |
| P11.3/TA2.1 | 90 | I/O | General-purpose digital I/O<br>Timer TA2 capture CCR1: CCI1A input, compare: Out1 output |
| P11.4/CBOUT | 91 | I/O | General-purpose digital I/O<br>Comparator_B Output |
| P11.5/TACLK/RTCCLK | 92 | I/O | General-purpose digital I/O<br>Timer clock input TACLK for TA0, TA1, TA2, TA3<br>RTCCLK clock output |
| P2.0/PM_TA0.0/BSL_TX | 93 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: Timer TA0 capture CCR0: CCI0A input, compare: Out0 output<br>Bootloader: Data transmit |
| P2.1/PM_TA0.1/BSL_RX | 94 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: Timer TA0 capture CCR1: CCI1A input, compare: Out1 output<br>Bootloader: Data receive |
| P2.2/PM_TA0.2 | 95 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: Timer TA0 capture CCR2: CCI2A input, compare: Out2 output |
| P2.3/PM_TA1.0 | 96 | I/O | General-purpose digital I/O port interrupt and with mappable secondary function<br>Default mapping: Timer TA1 capture CCR0: CCI0A input, compare: Out0 output |
| TEST/SBWTCK | 97 | I | Test mode pin – select digital I/O on JTAG pins<br>Spy-Bi-Wire input clock |
| PJ.0/TDO | 98 | I/O | General-purpose digital I/O<br>Test data output |
| PJ.1/TDI/TCLK | 99 | I/O | General-purpose digital I/O<br>Test data input or Test clock input |
| PJ.2/TMS | 100 | I/O | General-purpose digital I/O<br>Test mode select |
| PJ.3/TCK | 101 | I/O | General-purpose digital I/O<br>Test clock |
| $\overline{\text{RST}}$/NMI/SBWTDIO | 102 | I/O | Reset input active low[4]<br>Nonmaskable interrupt input<br>Spy-By-Wire data input/output |
| SD0P0 | 103 | I | SD24_B positive analog input for converter 0[5] |
| SD0N0 | 104 | I | SD24_B negative analog input for converter 0[5] |
| SD1P0 | 105 | I | SD24_B positive analog input for converter 1[5] |
| SD1N0 | 106 | I | SD24_B negative analog input for converter 1[5] |
| SD2P0 | 107 | I | SD24_B positive analog input for converter 2[5] |
| SD2N0 | 108 | I | SD24_B negative analog input for converter 2[5] |
| SD3P0 | 109 | I | SD24_B positive analog input for converter 3[5] |
| SD3N0 | 110 | I | SD24_B negative analog input for converter 3[4] |
| VASYS2 | 111 | | Analog power supply selected between AVCC, AUXVCC1, AUXVCC2. Connect recommended capacitor value of $C_{VSYS}$ |

(4) When this pin is configured as reset, the internal pullup resistor is enabled by default.
(5) Short unused analog input pairs and connect them to analog ground.


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**Table 4-3. Terminal Functions – PEU Package (continued)**

| TERMINAL | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| | PEU | | |
| AVSS2 | 112 | | Analog ground supply |
| VREF | 113 | I | SD24_B external reference voltage |
| SD4P0 | 114 | I | SD24_B positive analog input for converter 4(5) (not available on F674x1 devices) |
| SD4N0 | 115 | I | SD24_B negative analog input for converter 4(5) (not available on F674x1 devices) |
| SD5P0 | 116 | I | SD24_B positive analog input for converter 5(5) (not available on F674x1 devices) |
| SD5N0 | 117 | I | SD24_B negative analog input for converter 5(5) (not available on F674x1 devices) |
| SD6P0 | 118 | I | SD24_B positive analog input for converter 6(5) (not available on F676x1, F674x1 devices) |
| SD6N0 | 119 | I | SD24_B negative analog input for converter 6(5) (not available on F676x1, F674x1 devices) |
| AVSS1 | 120 | | Analog ground supply |
| AVCC | 121 | | Analog power supply |
| VASYS1 | 122 | | Analog power supply selected between AVCC, AUXVCC1, AUXVCC2. Connect recommended capacitor value of $C_{VSYS}$. |
| AUXVCC2 | 123 | | Auxiliary power supply AUXVCC2 |
| AUXVCC1 | 124 | | Auxiliary power supply AUXVCC1 |
| VDSYS1(3) | 125 | | Digital power supply selected between DVCC, AUXVCC1, AUXVCC2. Connect recommended capacitor value of $C_{VSYS}$. |
| DVCC | 126 | | Digital power supply |
| DVSS1 | 127 | | Digital ground supply |
| VCORE(6) | 128 | | Regulated core power supply (internal use only, no external current loading) |

(6) VCORE is for internal use only. No external current loading is possible. VCORE should only be connected to the recommended capacitor value, $C_{VCORE}$.

Table 4-4 describes the signals for devices in the PZ package. See Table 4-3 for the PEU package signal descriptions.

**Table 4-4. Terminal Functions – PZ Package**

| TERMINAL | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| | PZ | | |
| SD0P0 | 1 | I | SD24_B positive analog input for converter 0(2) |
| SD0N0 | 2 | I | SD24_B negative analog input for converter 0(2) |
| SD1P0 | 3 | I | SD24_B positive analog input for converter 1(2) |
| SD1N0 | 4 | I | SD24_B negative analog input for converter 1(2) |
| SD2P0 | 5 | I | SD24_B positive analog input for converter 2(2) |
| SD2N0 | 6 | I | SD24_B negative analog input for converter 2(2) |
| SD3P0 | 7 | I | SD24_B positive analog input for converter 3(2) |
| SD3N0 | 8 | I | SD24_B negative analog input for converter 3(2) |
| VASYS2 | 9 | | Analog power supply selected between AVCC, AUXVCC1, AUXVCC2. Connect recommended capacitor value of $C_{VSYS}$. |
| AVSS2 | 10 | | Analog ground supply |
| VREF | 11 | I | SD24_B external reference voltage |
| SD4P0 | 12 | I | SD24_B positive analog input for converter 4(2) (not available on F674x devices) |
| SD4N0 | 13 | I | SD24_B negative analog input for converter 4(2) (not available on F674x1 devices) |
| SD5P0 | 14 | I | SD24_B positive analog input for converter 5(2) (not available on F674x1 devices) |
| SD5N0 | 15 | I | SD24_B negative analog input for converter 5(2) (not available on F674x1 devices) |
| SD6P0 | 16 | I | SD24_B positive analog input for converter 6(2) (not available on F676x1, F674x1 devices) |
| SD6N0 | 17 | I | SD24_B negative analog input for converter 6(2) (not available on F676x1, F674x1 devices) |
| AVSS1 | 18 | | Analog ground supply |
| AVCC | 19 | | Analog power supply |
| VASYS1 | 20 | | Analog power supply selected between AVCC, AUXVCC1, AUXVCC2. Connect recommended capacitor value of $C_{VSYS}$ |
| AUXVCC2 | 21 | | Auxiliary power supply AUXVCC2 |
| AUXVCC1 | 22 | | Auxiliary power supply AUXVCC1 |
| VDSYS1 (3) | 23 | | Digital power supply selected between DVCC, AUXVCC1, AUXVCC2. Connect recommended capacitor value of $C_{VSYS}$. |
| DVCC | 24 | | Digital power supply |
| DVSS1 | 25 | | Digital ground supply |
| VCORE (4) | 26 | | Regulated core power supply (internal use only, no external current loading) |
| XIN | 27 | I/O | Input terminal for crystal oscillator |
| XOUT | 28 | I/O | Output terminal for crystal oscillator |
| AUXVCC3 | 29 | | Auxiliary power supply AUXVCC3 for back up subsystem |
| RTCCAP1 | 30 | I | External time capture pin 1 for RTC_C |
| RTCCAP0 | 31 | I | External time capture pin 0 for RTC_C |
| P1.5/SMCLK/CB0/A5 | 32 | I/O | General-purpose digital I/O with port interrupt<br>SMCLK clock output<br>Comparator_B input CB0<br>Analog input A5 for 10-bit ADC |

(1) I = input, O = output
(2) Short unused analog input pairs and connect them to analog ground.
(3) The pins VDSYS1 and VDSYS2 must be connected externally on board for proper device operation.
(4) VCORE is for internal use only. No external current loading is possible. VCORE should only be connected to the recommended capacitor value, $C_{VCORE}$.


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**Table 4-4. Terminal Functions – PZ Package (continued)**

| TERMINAL | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| | PZ | | |
| P1.4/MCLK/CB1/A4 | 33 | I/O | General-purpose digital I/O with port interrupt<br>MCLK clock output<br>Comparator_B input CB1<br>Analog input A4 for 10-bit ADC |
| P1.3/ADC10CLK/A3 | 34 | I/O | General-purpose digital I/O with port interrupt<br>ADC10_A clock output<br>Analog input A3 for 10-bit ADC |
| P1.2/ACLK/A2 | 35 | I/O | General-purpose digital I/O with port interrupt<br>ACLK clock output<br>Analog input A2 for 10-bit ADC |
| P1.1/TA2.1/CBOUT/<br>VeREF+/A1 | 36 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA2 CCR1 capture: CCI1A input, compare: Out1 output<br>Comparator_B Output<br>Positive terminal for the ADC reference voltage for an external applied reference voltage<br>Analog input A1 for 10-bit ADC |
| P1.0/TA1.1/VeREF-/A0 | 37 | I/O | General-purpose digital I/O with port interrupt<br>Timer TA1 CCR1 capture: CCI1A input, compare: Out1 output<br>Negative terminal for the ADC reference voltage for an external applied reference voltage<br>Analog input A0 for 10-bit ADC |
| COM0 | 38 | I/O | LCD common output COM0 for LCD backplane |
| COM1 | 39 | I/O | LCD common output COM1 for LCD backplane |
| P1.6/COM2 | 40 | I/O | General-purpose digital I/O with port interrupt<br>LCD common output COM2 for LCD backplane |
| P1.7/COM3 | 41 | I/O | General-purpose digital I/O with port interrupt<br>LCD common output COM3 for LCD backplane |
| P2.0/PM_TA0.0/<br>BSL_TX/COM4 | 42 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default Mapping: Timer TA0 CCR0 capture: CCI0A input, compare: Out0 output<br>Bootloader: Data transmit<br>LCD common output COM4 for LCD backplane |
| P2.1/PM_TA0.1/<br>BSL_RX/COM5 | 43 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default Mapping: Timer TA0 CCR1 capture: CCI1A input, compare: Out1 output<br>Bootloader: Data receive<br>LCD common output COM5 for LCD backplane |
| P2.2/PM_TA0.2/COM6 | 44 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default Mapping: Timer TA0 CCR0 capture: CCI2A input, compare: Out2 output<br>LCD common output COM6 for LCD backplane |
| P2.3/PM_TA1.0/COM7 | 45 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default Mapping: Timer TA1 CCR0 capture: CCI0A input, compare: Out0 output<br>LCD common output COM7 for LCD backplane |

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**Table 4-4. Terminal Functions – PZ Package (continued)**

| TERMINAL | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| | PZ | | |
| LCDCAP/R33 | 46 | I/O | LCD capacitor connection<br>Input/output port of most positive analog LCD voltage (V1)<br>**CAUTION**: This pin must be connected to DVSS if not used. |
| P2.4/PM_TA2.0/R23 | 47 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default Mapping: Timer TA2 CCR0 capture: CCI0A input, compare: Out0 output<br>Input/output port of second most positive analog LCD voltage (V2) |
| P2.5/PM_UCB0SOMI/<br>PM_UCB0SCL/LCDREF/<br>R13 | 48 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_B0 SPI slave out, master in<br>Default mapping: eUSCI_B0 $I^2C$ clock<br>External reference voltage input for regulated LCD voltage<br>Input/output port of third most positive analog LCD voltage (V3 or V4) |
| P2.6/PM_UCB0SIMO/<br>PM_UCB0SDA/R03 | 49 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_B0 SPI slave in, master out<br>Default mapping: eUSCI_B0 $I^2C$ data<br>Input/output port of lowest analog LCD voltage (V5) |
| P2.7/PM_UCB0CLK/CB2 | 50 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_B0 clock input/output<br>Comparator_B input CB2 |
| P3.0/PM_UCA0RXD/<br>PM_UCA0SOMI | 51 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_A0 UART receive data<br>Default mapping: eUSCI_A0 SPI slave out, master in |
| P3.1/PM_UCA0TXD/<br>PM_UCA0SIMO/S39 | 52 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_A0 UART transmit data<br>Default mapping: eUSCI_A0 SPI slave in, master out<br>LCD segment output S39 |
| P3.2/PM_UCA0CLK/S38 | 53 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_A0 clock input/output<br>LCD segment output S38 |
| P3.3/PM_UCA1CLK/S37 | 54 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_A1 clock input/output<br>LCD segment output S37 |
| P3.4/PM_UCA1RXD/<br>PM_UCA1SOMI/S36 | 55 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_A1 UART receive data<br>Default mapping: eUSCI_A1 SPI slave out, master in<br>LCD segment output S36 |
| P3.5/PM_UCA1TXD/<br>PM_UCA1SIMO/S35 | 56 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_A1 UART transmit data<br>Default mapping: eUSCI_A1 SPI slave in, master out<br>LCD segment output S35 |


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**Table 4-4. Terminal Functions – PZ Package (continued)**

| TERMINAL | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| | PZ | | |
| P3.6/PM_UCA2RXD/ PM_UCA2SOMI/S34 | 57 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_A2 UART receive data<br>Default mapping: eUSCI_A2 SPI slave out, master in<br>LCD segment output S34 |
| P3.7/PM_UCA2TXD/ PM_UCA2SIMO/S33 | 58 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_A2 UART transmit data<br>Default mapping: eUSCI_A2 SPI slave in, master out<br>LCD segment output S33 |
| P4.0/PM_UCA2CLK/S32 | 59 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_A2 clock input/output<br>LCD segment output S32 |
| P4.1/PM_UCA3RXD/ PM_UCA3SOMI/S31 | 60 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_A3 UART receive data<br>Default mapping: eUSCI_A3 SPI slave out, master in<br>LCD segment output S31 |
| P4.2/PM_UCA3TXD/ PM_UCA3SIMO/S30 | 61 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_A3 UART transmit data<br>Default mapping: eUSCI_A3 SPI slave in, master out<br>LCD segment output S30 |
| P4.3/PM_UCA3CLK/S29 | 62 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_A3 clock input/output<br>LCD segment output S29 |
| P4.4/PM_UCB1SOMI/ PM_UCB1SCL/S28 | 63 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_B1 SPI slave out, master in<br>Default mapping: eUSCI_B1 $I^2C$ clock<br>LCD segment output S28 |
| P4.5/PM_UCB1SIMO/ PM_UCB1SDA/S27 | 64 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_B1 SPI slave in, master out<br>Default mapping: eUSCI_B1 $I^2C$ data<br>LCD segment output S27 |
| P4.6/PM_UCB1CLK/S26 | 65 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: eUSCI_B1 clock input/output<br>LCD segment output S26 |
| P4.7/PM_TA3.0/S25 | 66 | I/O | General-purpose digital I/O with mappable secondary function<br>Default Mapping: Timer TA3 CCR0 capture: CCI0A input, compare: Out0 output<br>LCD segment output S25 |
| P5.0/SDCLK/S24 | 67 | I/O | General-purpose digital I/O<br>SD24_B bit stream clock input/output<br>LCD segment output S24 |

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**Table 4-4. Terminal Functions – PZ Package (continued)**

| TERMINAL | | I/O[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| | PZ | | |
| P5.1/PM_SD0DIO/S23 | 68 | I/O | General-purpose digital I/O<br>Default mapping: SD24_B converter 0 bit stream data input/output<br>LCD segment output S23 |
| P5.2/PM_SD1DIO/S22 | 69 | I/O | General-purpose digital I/O<br>Default mapping: SD24_B converter 1 bit stream data input/output<br>LCD segment output S22 |
| P5.3/PM_SD2DIO/S21 | 70 | I/O | General-purpose digital I/O<br>Default mapping: SD24_B converter 2 bit stream data input/output<br>LCD segment output S21 |
| P5.4/PM_SD3DIO/S20 | 71 | I/O | General-purpose digital I/O<br>Default mapping: SD24_B converter 3 bit stream data input/output<br>LCD segment output S20 |
| P5.5/PM_SD4DIO/S19 | 72 | I/O | General-purpose digital I/O<br>Default mapping: SD24_B converter 4 bit stream data input/output (not available on F674x1 devices)<br>LCD segment output S19 |
| P5.6/PM_SD5DIO/S18 | 73 | I/O | General-purpose digital I/O<br>Default mapping: SD24_B converter 5 bit stream data input/output (not available on F674x1 devices)<br>LCD segment output S18 |
| P5.7/PM_SD6DIO/S17 | 74 | I/O | General-purpose digital I/O<br>Default mapping: SD24_B converter 4 bit stream data input/output (not available on F676x1, F674x1 devices)<br>LCD segment output S17 |
| VDSYS2[5] | 75 | | Digital power supply for I/Os |
| DVSS2 | 76 | | Digital ground supply |
| P6.0/S16 | 77 | I/O | General-purpose digital I/O<br>LCD segment output S16 |
| P6.1/S15 | 78 | I/O | General-purpose digital I/O<br>LCD segment output S15 |
| P6.2/S14 | 79 | I/O | General-purpose digital I/O<br>LCD segment output S14 |
| P6.3/S13 | 80 | I/O | General-purpose digital I/O<br>LCD segment output S13 |
| P6.4/S12 | 81 | I/O | General-purpose digital I/O<br>LCD segment output S12 |
| P6.5/S11 | 82 | I/O | General-purpose digital I/O<br>LCD segment output S11 |
| P6.6/S10 | 83 | I/O | General-purpose digital I/O<br>LCD segment output S10 |
| P6.7/S9 | 84 | I/O | General-purpose digital I/O<br>LCD segment output S9 |

(5) The pins VDSYS1 and VDSYS2 must be connected externally on board for proper device operation.


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**Table 4-4. Terminal Functions – PZ Package (continued)**

| TERMINAL | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| | PZ | | |
| P7.0/S8 | 85 | I/O | General-purpose digital I/O<br>LCD segment output S8 |
| P7.1/S7 | 86 | I/O | General-purpose digital I/O<br>LCD segment output S7 |
| P7.2/S6 | 87 | I/O | General-purpose digital I/O<br>LCD segment output S6 |
| P7.3/S5 | 88 | I/O | General-purpose digital I/O<br>LCD segment output S5 |
| P7.4/S4 | 89 | I/O | General-purpose digital I/O<br>LCD segment output S4 |
| P7.5/S3 | 90 | I/O | General-purpose digital I/O<br>LCD segment output S3 |
| P7.6/S2 | 91 | I/O | General-purpose digital I/O<br>LCD segment output S2 |
| P7.7/S1 | 92 | I/O | General-purpose digital I/O<br>LCD segment output S1 |
| P8.0/S0 | 93 | I/O | General-purpose digital I/O<br>LCD segment output S0 |
| P8.1/TACLK/RTCCLK/CB3 | 94 | I/O | General-purpose digital I/O<br>Timer clock input TACLK for TA0, TA1, TA2, TA3<br>RTCCLK clock output<br>Comparator_B input CB3 |
| TEST/SBWTCK | 95 | I | Test mode pin – select digital I/O on JTAG pins<br>Spy-By-Wire input clock |
| PJ.0/TDO | 96 | I/O | General-purpose digital I/O<br>Test data output |
| PJ.1/TDI/TCLK | 97 | I/O | General-purpose digital I/O<br>Test data input or Test clock input |
| PJ.2/TMS | 98 | I/O | General-purpose digital I/O<br>Test mode select |
| PJ.3/TCK | 99 | I/O | General-purpose digital I/O<br>Test clock |
| $\overline{\text{RST}}$/NMI/SBWTDIO | 100 | I/O | Reset input, active low(6)<br>Nonmaskable interrupt input<br>Spy-By-Wire data input/output |

(6) When this pin is configured as reset, the internal pullup resistor is enabled by default.

# 5 Specifications

All graphs in this section are for typical conditions, unless otherwise noted.

Typical (TYP) values are specified at $V_{CC}$ = 3.3 V and $T_A$ = 25°C, unless otherwise noted.

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage applied at DVCC to DVSS | | –0.3 | 4.1 | V |
| Voltage applied to pins(2) | All pins except VCORE, SD24_B input pins (SDxN0, SDxP0)(3), AUXVCC1, AUXVCC2, and AUXVCC3(4) | –0.3 | $V_{CC}$ + 0.3 | V |
| Diode current at pins | All pins except SD24_B input pins (SDxN0, SDxP0) | | ±2 | mA |
| | SD0N0, SD0P0, SD1N0, SD1P0, SD2N0, SD2P0, SD3N0, SD3P0, SD4N0, SD4P0, SD5N0, SD5P0, SD6N0, SD6P0(5) | | 2 | |
| Maximum junction temperature, $T_J$ | | | 95 | °C |
| Storage temperature, $T_{stg}$(6) | | –55 | 105 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to $V_{SS}$ = $V_{DVSS}$ = $V_{AVSS}$.
(3) See Section 5.48 for SD24_B specifications.
(4) See Section 5.27 for AUX specifications.
(5) A protection diode is connected to $V_{CC}$ for the SD24_B input pins. No protection diode is connected to $V_{SS}$.
(6) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±1000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±250 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

## 5.3 Recommended Operating Conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage during program execution and flash programming. $V_{AVCC}$ = $V_{DVCC}$ = $V_{CC}$(1)(2) | PMMCOREVx = 0 | 1.8 | | 3.6 | V |
| | | PMMCOREVx = 0, 1 | 2.0 | | 3.6 | |
| | | PMMCOREVx = 0, 1, 2 | 2.2 | | 3.6 | |
| | | PMMCOREVx = 0, 1, 2, 3 | 2.4 | | 3.6 | |
| $V_{SS}$ | Supply voltage $V_{AVSS}$ = $V_{DVSS}$ = $V_{SS}$ | | | 0 | | V |
| $T_A$ | Operating free-air temperature | I version | –40 | | 85 | °C |
| $T_J$ | Operating junction temperature | I version | –40 | | 85 | °C |
| $C_{VCORE}$ | Recommended capacitor at VCORE(3) | | | 470 | | nF |
| $C_{DVCC}$/ $C_{VCORE}$ | Capacitor ratio of DVCC to VCORE | | 10 | | | |

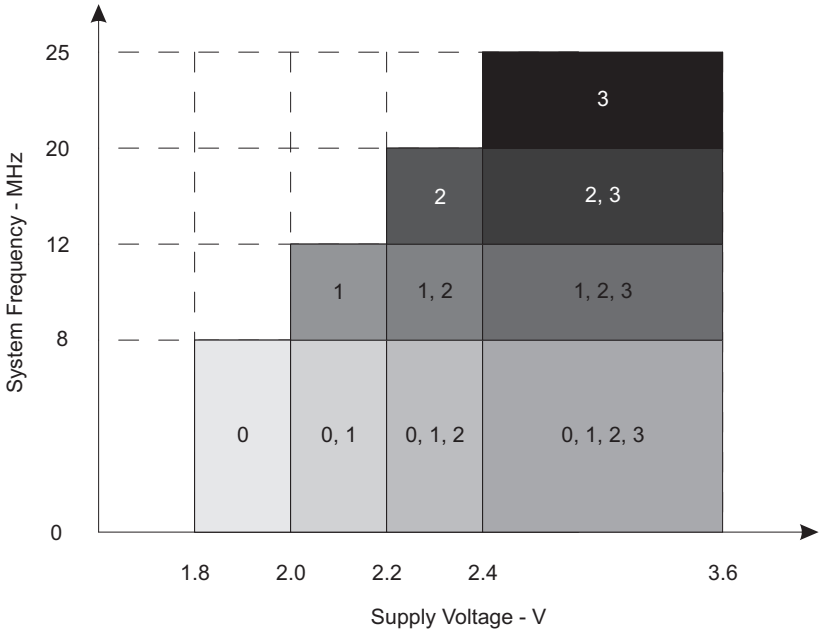
(1) TI recommends powering AVCC and DVCC from the same source. A maximum difference of 0.3 V between $V_{AVCC}$ and $V_{DVCC}$ can be tolerated during power up and operation.
(2) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the threshold parameters in Section 5.22 for the exact values and more details.
(3) A capacitor tolerance of ±20% or better is required.


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## Recommended Operating Conditions *(continued)*

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SYSTEM}$ | Processor frequency (maximum MCLK frequency)(4) (5) (see Figure 5-1) | PMMCOREVx = 0, 1.8 V ≤ $V_{CC}$ ≤ 3.6 V (default condition) | 0 | | 8.0 | MHz |
| | | PMMCOREVx = 1, 2 V ≤ $V_{CC}$ ≤ 3.6 V | 0 | | 12.0 | |
| | | PMMCOREVx = 2, 2.2 V ≤ $V_{CC}$ ≤ 3.6 V | 0 | | 20.0 | |
| | | PMMCOREVx = 3, 2.4 V ≤ $V_{CC}$ ≤ 3.6 V | 0 | | 25.0 | |
| $I_{LOAD, DVCCD}$ | Maximum load current that can be drawn from DVCC for core and IO ($I_{LOAD} = I_{CORE} + I_{IO}$) | | | | 20 | mA |
| $I_{LOAD, AUX1D}$ | Maximum load current that can be drawn from AUXVCC1 for core and IO ($I_{LOAD} = I_{CORE} + I_{IO}$) | | | | 20 | mA |
| $I_{LOAD, AUX2D}$ | Maximum load current that can be drawn from AUXVCC2 for core and IO ($I_{LOAD} = I_{CORE} + I_{IO}$) | | | | 20 | mA |
| $I_{LOAD, AVCCA}$ | Maximum load current that can be drawn from AVCC for analog modules ($I_{LOAD} = I_{Modules}$) | | | | 10 | mA |
| $I_{LOAD, AUX1A}$ | Maximum load current that can be drawn from AUXVCC1 for analog modules ($I_{LOAD} = I_{Modules}$) | | | | 5 | mA |
| $I_{LOAD, AUX2A}$ | Maximum load current that can be drawn from AUXVCC2 for analog modules ($I_{LOAD} = I_{Modules}$) | | | | 5 | mA |
| $P_{INT}$ | Internal power dissipation | | | $V_{CC} \times I_{DVCC}$ | | W |
| $P_{IO}$ | I/O power dissipation of the I/O pins powered by DVCC | | | $(V_{CC} - V_{IOH}) \times I_{IOH} + V_{IOL} \times I_{IOL}$ | | W |
| $P_{MAX}$ | Maximum allowed power dissipation, $P_{MAX} > P_{IO} + P_{INT}$ | | | $(T_J - T_A)/\theta_{JA}$ | | W |

(4) The MSP430 CPU is clocked directly with MCLK. Both the high and low phases of MCLK must not exceed the pulse duration of the specified maximum frequency.
(5) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.




The numbers within the fields denote the supported PMMCOREVx settings.

**Figure 5-1. Maximum System Frequency**

## 5.4 Active Mode Supply Current Into $V_{CC}$ Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)(1)(2)(3)

| PARAMETER | EXECUTION MEMORY | $V_{CC}$ | PMM COREVx | FREQUENCY ($f_{DCO} = f_{MCLK} = f_{SMCLK}$) | | | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 1 MHz | | 8 MHz | | 12 MHz | | 20 MHz | | 25 MHz | | |
| | | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{AM, Flash}$ (4) | Flash | 3 V | 0 | 0.32 | 0.50 | 2.08 | 2.84 | | | | | | | mA |
| | | | 1 | 0.35 | | 2.35 | | 3.50 | 4.76 | | | | | |
| | | | 2 | 0.39 | | 2.68 | | 3.99 | | 6.61 | 8.3 | | | |
| | | | 3 | 0.41 | | 2.83 | | 4.22 | | 6.98 | | 8.67 | 11.75 | |
| $I_{AM, RAM}$ (5) | RAM | 3 V | 0 | 0.19 | | 1.04 | | | | | | | | mA |
| | | | 1 | 0.21 | | 1.20 | | 1.77 | | | | | | |
| | | | 2 | 0.23 | | 1.38 | | 2.04 | | 3.35 | | | | |
| | | | 3 | 0.24 | | 1.47 | | 2.18 | | 3.58 | | 4.44 | | |

(1) All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
(3) Characterized with program executing typical data processing.
$f_{ACLK}$ = 32786 Hz, $f_{DCO} = f_{MCLK} = f_{SMCLK}$ at specified frequency.
XTS = CPUOFF = SCG0 = SCG1 = OSCOFF = SMCLKOFF = 0.
(4) Active mode supply current when program executes in flash at a nominal supply voltage of 3 V.
(5) Active mode supply current when program executes in RAM at a nominal supply voltage of 3 V.


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## 5.5 Low-Power Mode Supply Currents (Into $V_{CC}$) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)(2)

| PARAMETER | | $V_{CC}$ | PMMCOREVx | TEMPERATURE ($T_A$) | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | –40°C | | 25°C | | 85°C | | |
| | | | | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM0,1MHz}$ | Low-power mode 0(3) (4) | 2.2 V | 0 | 70 | | 75 | | 86 | | µA |
| | | 3 V | 3 | 81 | | 87 | 105 | 100 | 130 | |
| $I_{LPM2}$ | Low-power mode 2(5) (4) | 2.2 V | 0 | 5.9 | | 6.5 | | 12.5 | | µA |
| | | 3 V | 3 | 6.7 | | 7.3 | 18 | 13.8 | 30 | |
| $I_{LPM3,XT1LF}$ | Low-power mode 3, crystal mode(6) (4) | 2.2 V | 0 | 1.50 | | 2.0 | | 7.8 | | µA |
| | | | 1 | 1.65 | | 2.2 | | 8.3 | | |
| | | | 2 | 1.80 | | 2.4 | | 8.6 | | |
| | | | 3 | 1.84 | | 2.4 | | 8.6 | | |
| $I_{LPM3,XT1LF}$ | Low-power mode 3, crystal mode(6) (4) | 3 V | 0 | 2.0 | | 2.5 | | 8.5 | | µA |
| | | | 1 | 2.1 | | 2.7 | | 9.0 | | |
| | | | 2 | 2.3 | | 2.9 | | 9.3 | | |
| | | | 3 | 2.3 | | 2.9 | | 9.3 | 25 | |
| $I_{LPM3,VLO}$ | Low-power mode 3, VLO mode(7) (4) | 3 V | 0 | 1.3 | | 1.7 | | 7.5 | | µA |
| | | | 1 | 1.3 | | 1.8 | | 7.9 | | |
| | | | 2 | 1.4 | | 1.9 | | 8.2 | | |
| | | | 3 | 1.4 | | 1.9 | | 8.2 | 25.0 | |
| $I_{LPM4}$ | Low-power mode 4(8) (4) | 3 V | 0 | 1.2 | | 1.6 | | 7.4 | | µA |
| | | | 1 | 1.2 | | 1.7 | | 7.8 | | |
| | | | 2 | 1.3 | | 1.7 | | 7.9 | | |
| | | | 3 | 1.3 | | 1.7 | | 8.0 | 23.0 | |
| $I_{LPM3.5}$ | Low-power mode 3.5, RTC active on AUXVCC3(9) | 2.2 V | | 0.7 | | 0.9 | | 1.4 | | µA |
| | | 3 V | | 1.0 | | 1.2 | 1.5 | 1.8 | 3.0 | |
| $I_{LPM4.5}$ | Low-power mode 4.5(10) | 3 V | | 0.6 | | 0.7 | 1.0 | 1.2 | 2.0 | µA |

(1) All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
(3) Current for watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0), $f_{ACLK}$ = 32768 Hz, $f_{MCLK}$ = 0 MHz, $f_{SMCLK}$ = $f_{DCO}$ = 1 MHz
(4) Current for brownout and high-side supervisor ($SVS_H$) normal mode included. Low-side supervisor ($SVS_L$) and low-side monitor ($SVM_L$) disabled. High-side monitor ($SVM_H$) disabled. RAM retention enabled.
(5) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2), $f_{ACLK}$ = 32768 Hz, $f_{MCLK}$ = 0 MHz, $f_{SMCLK}$ = $f_{DCO}$ = 0 MHz, DCO setting = 1 MHz operation, DCO bias generator enabled.
(6) Current for watchdog timer and RTC clocked by low-frequency clock included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), $f_{ACLK}$ = 32768 Hz, $f_{MCLK}$ = $f_{SMCLK}$ = $f_{DCO}$ = 0 MHz
(7) Current for watchdog timer and RTC clocked by low-frequency clock included. ACLK = VLO. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), $f_{ACLK}$ = $f_{VLO}$, $f_{MCLK}$ = $f_{SMCLK}$ = $f_{DCO}$ = 0 MHz
(8) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4), $f_{DCO}$ = $f_{ACLK}$ = $f_{MCLK}$ = $f_{SMCLK}$ = 0 MHz
(9) $f_{DCO}$ = $f_{MCLK}$ = $f_{SMCLK}$ = 0 MHz, $f_{ACLK}$ = 32768 Hz, PMMREGOFF = 1, RTC active on AUXVCC3 supply
(10) $f_{DCO}$ = $f_{MCLK}$ = $f_{SMCLK}$ = 0 MHz, $f_{ACLK}$ = 0 Hz, PMMREGOFF = 1

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## 5.6 Low-Power Mode With LCD Supply Currents (Into $V_{CC}$) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)(2)

| PARAMETER | | $V_{CC}$ | PMMCOREVx | TEMPERATURE ($T_A$) | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | –40°C | | 25°C | | 85°C | | |
| | | | | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM3}$ LCD, ext. bias | Low-power mode 3 (LPM3) current, LCD 4-mux mode, external biasing(3) (4) | 3 V | 0 | 2.5 | | 3.1 | | 9.1 | | µA |
| | | | 1 | 2.6 | | 3.3 | | 9.5 | | |
| | | | 2 | 2.8 | | 3.5 | | 9.9 | | |
| | | | 3 | 2.8 | | 3.5 | 6.0 | 10.0 | 25.0 | |
| $I_{LPM3}$ LCD, int. bias | Low-power mode 3 (LPM3) current, LCD 4-mux mode, internal biasing, charge pump disabled(3) (5) | 3 V | 0 | 2.9 | | 3.5 | | 9.7 | | µA |
| | | | 1 | 3.1 | | 3.7 | | 10.1 | | |
| | | | 2 | 3.2 | | 4.0 | | 10.5 | | |
| | | | 3 | 3.3 | | 4.0 | 5.5 | 10.5 | 25.0 | |
| $I_{LPM3}$ LCD,CP | Low-power mode 3 (LPM3) current, LCD 4-mux mode, internal biasing, charge pump enabled(3) (6) | 2.2 V | 0 | 2.2 | | 2.8 | | 8.8 | | µA |
| | | | 1 | 2.3 | | 3.0 | | 9.1 | | |
| | | | 2 | 2.5 | | 3.2 | | 9.5 | | |
| | | 3 V | 0 | 2.6 | | 3.2 | | 9.3 | | |
| | | | 1 | 2.8 | | 3.4 | | 9.7 | | |
| | | | 2 | 2.9 | | 3.6 | | 10.1 | | |
| | | | 3 | 3.0 | | 3.7 | | 10.2 | | |

(1) All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
(3) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), $f_{ACLK}$ = 32768 Hz, $f_{MCLK} = f_{SMCLK} = f_{DCO}$ = 0 MHz
Current for brownout, high-side supervisor ($SVS_H$) normal mode included. Low-side supervisor and monitors disabled ($SVS_L$, $SVM_L$). High-side monitor ($SVM_H$) disabled. RAM retention enabled.
(4) LCDMx = 11 (4-mux mode), LCDREXT = 1, LCDEXTBIAS = 1 (external biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 0 (charge pump disabled), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 ($f_{LCD}$ = 32768 Hz / 32 / 4 = 256 Hz)
Current through external resistors not included (voltage levels are supplied by test equipment).
Even segments S0, S2, ... = 0, odd segments S1, S3, ... = 1. No LCD panel load.
(5) LCDMx = 11 (4-mux mode), LCDREXT = 0, LCDEXTBIAS = 0 (internal biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 0 (charge pump disabled), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 ($f_{LCD}$ = 32768 Hz / 32 / 4 = 256 Hz)
Even segments S0, S2, ... = 0, odd segments S1, S3, ... = 1. No LCD panel load.
(6) LCDMx = 11 (4-mux mode), LCDREXT = 0, LCDEXTBIAS = 0 (internal biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 1 (charge pump enabled), VLCDx = 1000 ($V_{LCD}$ = 3 V, typical), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 ($f_{LCD}$ = 32768 Hz / 32 / 4 = 256 Hz)
Even segments S0, S2, ... = 0, odd segments S1, S3, ... = 1. No LCD panel load.


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## 5.7 Thermal Packaging Characteristics

| THERMAL METRIC(1) (2) | | | VALUE | UNIT |
|---|---|---|---|---|
| $R\theta_{JA}$ | Junction-to-ambient thermal resistance, still air | LQFP 128 (PEU) | 44.4 | °C/W |
| | | LQFP 100 (PZ) | 42.9 | |
| $R\theta_{JC(TOP)}$ | Junction-to-case (top) thermal resistance | LQFP 128 (PEU) | 10.5 | °C/W |
| | | LQFP 100 (PZ) | 9.3 | |
| $R\theta_{JC(BOTTOM)}$ | Junction-to-case (bottom) thermal resistance | LQFP 128 (PEU) | N/A(3) | °C/W |
| | | LQFP 100 (PZ) | N/A | |
| $R\theta_{JB}$ | Junction-to-board thermal resistance | LQFP 128 (PEU) | 23.1 | °C/W |
| | | LQFP 100 (PZ) | 20.6 | |
| $\Psi_{JT}$ | Junction-to-package-top thermal characterization parameter | LQFP 128 (PEU) | 0.4 | °C/W |
| | | LQFP 100 (PZ) | 0.3 | |
| $\Psi_{JB}$ | Junction-to-board thermal characterization parameter | LQFP 128 (PEU) | 22.8 | °C/W |
| | | LQFP 100 (PZ) | 20.3 | |

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(3) N/A = not applicable

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## 5.8 Schmitt-Trigger Inputs – General-Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going input threshold voltage | | 1.8 V | 0.80 | | 1.40 | V |
| | | | 3 V | 1.50 | | 2.10 | |
| $V_{IT-}$ | Negative-going input threshold voltage | | 1.8 V | 0.45 | | 1.00 | V |
| | | | 3 V | 0.75 | | 1.65 | |
| $V_{hys}$ | Input voltage hysteresis ($V_{IT+} - V_{IT-}$) | | 1.8 V | 0.3 | | 0.85 | V |
| | | | 3 V | 0.4 | | 1.0 | |
| $R_{Pull}$ | Pullup or pulldown resistor(1) | For pullup: $V_{IN} = V_{SS}$, For pulldown: $V_{IN} = V_{CC}$ | | 20 | 35 | 50 | kΩ |
| $C_I$ | Input capacitance | $V_{IN} = V_{SS}$ or $V_{CC}$ | | | 5 | | pF |

(1) Also applies to $\overline{RST}$ pin when pullup or pulldown resistor is enabled.

## 5.9 Inputs – Ports P1 and P2(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{(int)}$ | External interrupt timing(2) | Port P1 and P2: P1.x to P2.x, external trigger pulse duration to set interrupt flag | 2.2 V, 3 V | 20 | | ns |

(1) Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.
(2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It may be set by trigger signals shorter than $t_{(int)}$.

## 5.10 Leakage Current – General-Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{lkg(Px.y)}$ | High-impedance leakage current | See (1)(2) | 1.8 V, 3 V | –50 | +50 | nA |

(1) The leakage current is measured with $V_{SS}$ or $V_{CC}$ applied to the corresponding pins, unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.


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## 5.11 Outputs – General-Purpose I/O (Full Drive Strength)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (also see Figure 5-6 through Figure 5-9)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{(OHmax)}$ = –3 mA (1) | 1.8 V | 1.55 | 1.80 | V |
| | | $I_{(OHmax)}$ = –10 mA (1) | | 1.20 | 1.80 | |
| | | $I_{(OHmax)}$ = –5 mA (1) | 3 V | 2.75 | 3.00 | |
| | | $I_{(OHmax)}$ = –15 mA (1) | | 2.40 | 3.00 | |
| $V_{OL}$ | Low-level output voltage | $I_{(OLmax)}$ = 3 mA (2) | 1.8 V | 0.00 | 0.25 | V |
| | | $I_{(OLmax)}$ = 10 mA (3) | | 0.00 | 0.60 | |
| | | $I_{(OLmax)}$ = 5 mA (2) | 3 V | 0.00 | 0.25 | |
| | | $I_{(OLmax)}$ = 15 mA (3) | | 0.00 | 0.60 | |

(1) The maximum total current, $I_{(OHmax)}$, for all outputs combined should not exceed ±20 mA to hold the maximum voltage drop specified. See Section 5.3 for more details.
(2) The maximum total current, $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(3) The maximum total current, $I_{(OLmax)}$, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.

## 5.12 Outputs – General-Purpose I/O (Reduced Drive Strength)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1) (also see Figure 5-2 through Figure 5-5)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{(OHmax)}$ = –1 mA (2) | 1.8 V | 1.55 | 1.80 | V |
| | | $I_{(OHmax)}$ = –3 mA (2) | | 1.20 | 1.80 | |
| | | $I_{(OHmax)}$ = –2 mA (2) | 3 V | 2.75 | 3.00 | |
| | | $I_{(OHmax)}$ = –6 mA (2) | | 2.40 | 3.00 | |
| $V_{OL}$ | Low-level output voltage | $I_{(OLmax)}$ = 1 mA (3) | 1.8 V | 0.00 | 0.25 | V |
| | | $I_{(OLmax)}$ = 3 mA (4) | | 0.00 | 0.60 | |
| | | $I_{(OLmax)}$ = 2 mA (3) | 3 V | 0.00 | 0.25 | |
| | | $I_{(OLmax)}$ = 6 mA (4) | | 0.00 | 0.60 | |

(1) Selecting reduced drive strength may reduce EMI.
(2) The maximum total current, $I_{(OHmax)}$, for all outputs combined should not exceed ±20 mA to hold the maximum voltage drop specified. See Section 5.3 for more details.
(3) The maximum total current, $I_{(OLmax)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
(4) The maximum total current, $I_{(OLmax)}$, for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.

## 5.13 Output Frequency – General-Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{Px.y}$ | Port output frequency (with load) | See (1) (2) | $V_{CC}$ = 1.8 V, PMMCOREVx = 0 | | 16 | MHz |
| | | | $V_{CC}$ = 3 V, PMMCOREVx = 3 | | 25 | |
| $f_{Port_CLK}$ | Clock output frequency | ACLK, SMCLK, or MCLK, $C_L$ = 20 pF (2) | $V_{CC}$ = 1.8 V, PMMCOREVx = 0 | | 16 | MHz |
| | | | $V_{CC}$ = 3 V, PMMCOREVx = 3 | | 25 | |

(1) A resistive divider with 2 × R1 between $V_{CC}$ and $V_{SS}$ is used as load. The output is connected to the center tap of the divider. For full drive strength, R1 = 550 Ω. For reduced drive strength, R1 = 1.6 kΩ. $C_L$ = 20 pF is connected to the output to $V_{SS}$.
(2) The output voltage reaches at least 10% and 90% $V_{CC}$ at the specified toggle frequency.

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## 5.14 Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

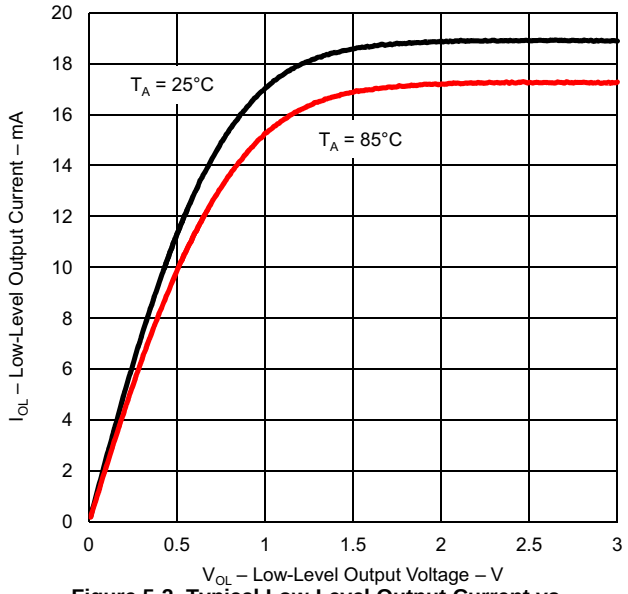



**Figure 5-2. Typical Low-Level Output Current vs Low-Level Output Voltage**

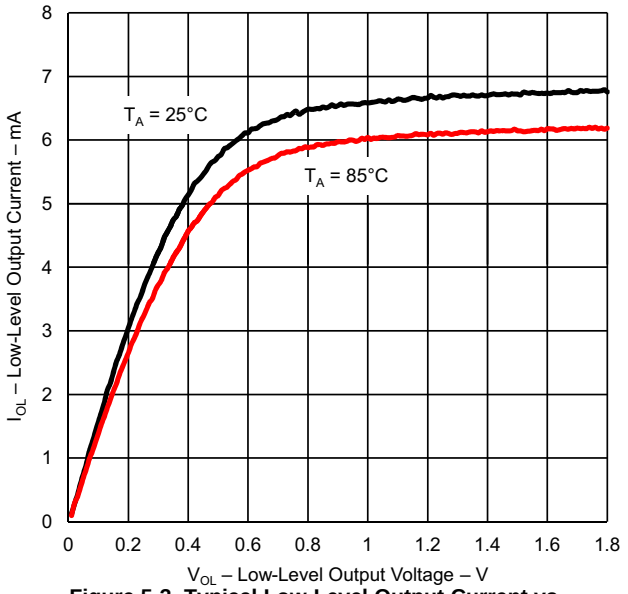



**Figure 5-3. Typical Low-Level Output Current vs Low-Level Output Voltage**

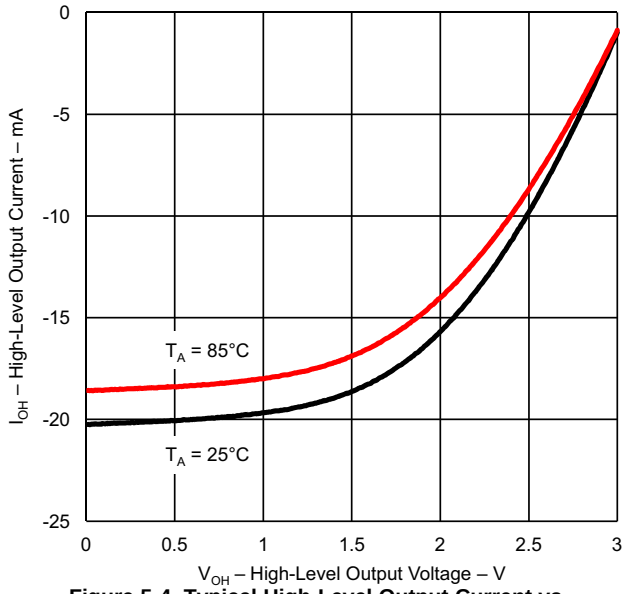



**Figure 5-4. Typical High-Level Output Current vs High-Level Output Voltage**

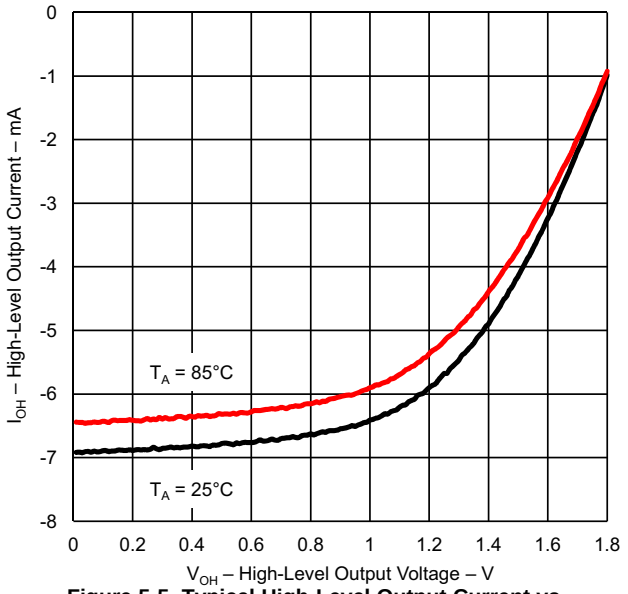



**Figure 5-5. Typical High-Level Output Current vs High-Level Output Voltage**


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## 5.15 Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

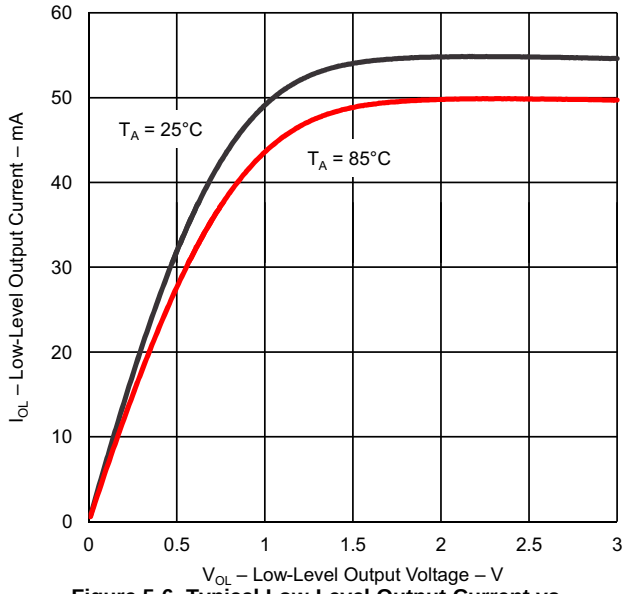



**Figure 5-6. Typical Low-Level Output Current vs Low-Level Output Voltage**

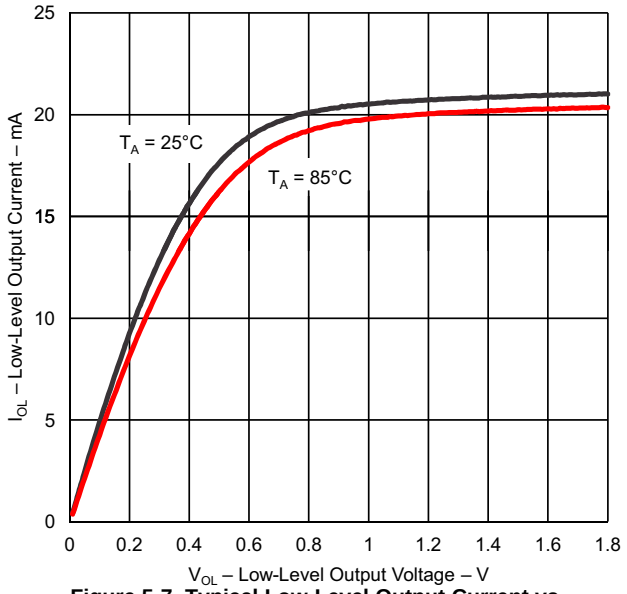



**Figure 5-7. Typical Low-Level Output Current vs Low-Level Output Voltage**

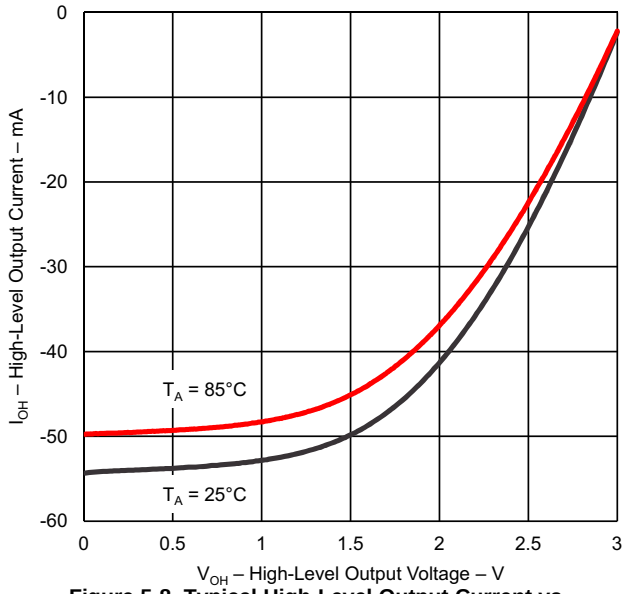



**Figure 5-8. Typical High-Level Output Current vs High-Level Output Voltage**

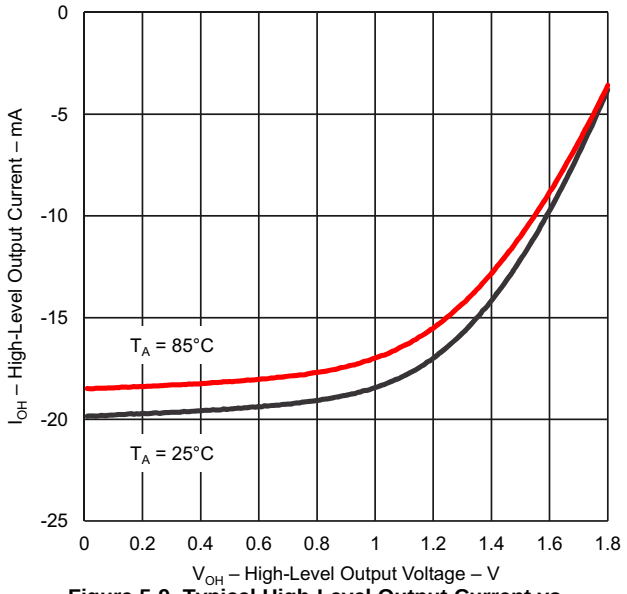



**Figure 5-9. Typical High-Level Output Current vs High-Level Output Voltage**

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## 5.16 Crystal Oscillator, XT1, Low-Frequency Mode(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $\Delta I_{DVCC.LF}$ | Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, $T_A$ = 25°C | 3 V | | 0.075 | | µA |
| | | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 2, $T_A$ = 25°C | | | 0.170 | | |
| | | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, $T_A$ = 25°C | | | 0.290 | | |
| $f_{XT1,LF0}$ | XT1 oscillator crystal frequency, LF mode | XTS = 0, XT1BYPASS = 0 | | | 32768 | | Hz |
| $f_{XT1,LF,SW}$ | XT1 oscillator logic-level square-wave input frequency, LF mode | XTS = 0, XT1BYPASS = 1(2) (3) | | 10 | 32.768 | 50 | kHz |
| $OA_{LF}$ | Oscillation allowance for LF crystals(4) | XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF | | | 210 | | kΩ |
| | | XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF | | | 300 | | |
| $C_{L,eff}$ | Integrated effective load capacitance, LF mode(5) | XTS = 0, XCAPx = 0(6) | | | 1 | | pF |
| | | XTS = 0, XCAPx = 1 | | | 5.5 | | |
| | | XTS = 0, XCAPx = 2 | | | 8.5 | | |
| | | XTS = 0, XCAPx = 3 | | | 12.0 | | |
| | Duty cycle, LF mode | XTS = 0, Measured at ACLK, $f_{XT1,LF}$ = 32768 Hz | | 30% | | 70% | |
| $f_{Fault,LF}$ | Oscillator fault frequency, LF mode(7) | XTS = 0(8) | | 10 | | 10000 | Hz |
| $t_{START,LF}$ | Start-up time, LF mode | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, $T_A$ = 25°C, $C_{L,eff}$ = 6 pF | 3 V | | 1000 | | ms |
| | | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, $T_A$ = 25°C, $C_{L,eff}$ = 12 pF | | | 500 | | |

(1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet.

(3) Maximum frequency of operation of the entire device cannot be exceeded.

(4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVEx settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
- For XT1DRIVEx = 0, $C_{L,eff} \le 6$ pF.
- For XT1DRIVEx = 1, 6 pF $\le C_{L,eff} \le$ 9 pF.
- For XT1DRIVEx = 2, 6 pF $\le C_{L,eff} \le$ 10 pF.
- For XT1DRIVEx = 3, $C_{L,eff} \ge 6$ pF.

(5) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

(6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX might set the flag.

(8) Measured with logic-level input frequency but also applies to operation with crystals.


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## 5.17 Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{VLO}$ | VLO frequency | Measured at ACLK | 1.8 V to 3.6 V | 6 | 9.6 | 15 | kHz |
| $df_{VLO}/d_T$ | VLO frequency temperature drift | Measured at ACLK | 1.8 V to 3.6 V | | 0.5 | | %/°C |
| $df_{VLO}/dV_{CC}$ | VLO frequency supply voltage drift | Measured at ACLK | 1.8 V to 3.6 V | | 4 | | %/V |
| | Duty cycle | Measured at ACLK | 1.8 V to 3.6 V | 40% | 50% | 60% | |

## 5.18 Internal Reference, Low-Frequency Oscillator (REFO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{REFO}$ | REFO oscillator current consumption | $T_A$ = 25°C | 1.8 V to 3.6 V | | 3 | | µA |
| $f_{REFO}$ | REFO frequency calibrated | Measured at ACLK | 1.8 V to 3.6 V | | 32768 | | Hz |
| | REFO absolute tolerance calibrated | Full temperature range | 1.8 V to 3.6 V | –3.5% | | +3.5% | |
| | | $T_A$ = 25°C | 3 V | –1.5% | | +1.5% | |
| $df_{REFO}/d_T$ | REFO frequency temperature drift | Measured at ACLK | 1.8 V to 3.6 V | | 0.01 | | %/°C |
| $df_{REFO}/dV_{CC}$ | REFO frequency supply voltage drift | Measured at ACLK | 1.8 V to 3.6 V | | 1.0 | | %/V |
| | Duty cycle | Measured at ACLK | 1.8 V to 3.6 V | 40% | 50% | 60% | |
| $t_{START}$ | REFO start-up time | 40%/60% duty cycle | 1.8 V to 3.6 V | | 25 | | µs |

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## 5.19 DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-10)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{DCO(0,0)}$ | DCO frequency (0, 0)(1) | DCORSELx = 0, DCOx = 0, MODx = 0 | 0.07 | | 0.20 | MHz |
| $f_{DCO(0,31)}$ | DCO frequency (0, 31)(1) | DCORSELx = 0, DCOx = 31, MODx = 0 | 0.70 | | 1.70 | MHz |
| $f_{DCO(1,0)}$ | DCO frequency (1, 0)(1) | DCORSELx = 1, DCOx = 0, MODx = 0 | 0.15 | | 0.36 | MHz |
| $f_{DCO(1,31)}$ | DCO frequency (1, 31)(1) | DCORSELx = 1, DCOx = 31, MODx = 0 | 1.47 | | 3.45 | MHz |
| $f_{DCO(2,0)}$ | DCO frequency (2, 0)(1) | DCORSELx = 2, DCOx = 0, MODx = 0 | 0.32 | | 0.75 | MHz |
| $f_{DCO(2,31)}$ | DCO frequency (2, 31)(1) | DCORSELx = 2, DCOx = 31, MODx = 0 | 3.17 | | 7.38 | MHz |
| $f_{DCO(3,0)}$ | DCO frequency (3, 0)(1) | DCORSELx = 3, DCOx = 0, MODx = 0 | 0.64 | | 1.51 | MHz |
| $f_{DCO(3,31)}$ | DCO frequency (3, 31)(1) | DCORSELx = 3, DCOx = 31, MODx = 0 | 6.07 | | 14.0 | MHz |
| $f_{DCO(4,0)}$ | DCO frequency (4, 0)(1) | DCORSELx = 4, DCOx = 0, MODx = 0 | 1.3 | | 3.2 | MHz |
| $f_{DCO(4,31)}$ | DCO frequency (4, 31)(1) | DCORSELx = 4, DCOx = 31, MODx = 0 | 12.3 | | 28.2 | MHz |
| $f_{DCO(5,0)}$ | DCO frequency (5, 0)(1) | DCORSELx = 5, DCOx = 0, MODx = 0 | 2.5 | | 6.0 | MHz |
| $f_{DCO(5,31)}$ | DCO frequency (5, 31)(1) | DCORSELx = 5, DCOx = 31, MODx = 0 | 23.7 | | 54.1 | MHz |
| $f_{DCO(6,0)}$ | DCO frequency (6, 0)(1) | DCORSELx = 6, DCOx = 0, MODx = 0 | 4.6 | | 10.7 | MHz |
| $f_{DCO(6,31)}$ | DCO frequency (6, 31)(1) | DCORSELx = 6, DCOx = 31, MODx = 0 | 39.0 | | 88.0 | MHz |
| $f_{DCO(7,0)}$ | DCO frequency (7, 0)(1) | DCORSELx = 7, DCOx = 0, MODx = 0 | 8.5 | | 19.6 | MHz |
| $f_{DCO(7,31)}$ | DCO frequency (7, 31)(1) | DCORSELx = 7, DCOx = 31, MODx = 0 | 60 | | 135 | MHz |
| $S_{DCORSEL}$ | Frequency step between range DCORSEL and DCORSEL + 1 | $S_{RSEL} = f_{DCO(DCORSEL+1,DCO)}/f_{DCO(DCORSEL,DCO)}$ | 1.2 | | 2.3 | ratio |
| $S_{DCO}$ | Frequency step between tap DCO and DCO + 1 | $S_{DCO} = f_{DCO(DCORSEL,DCO+1)}/f_{DCO(DCORSEL,DCO)}$ | 1.02 | | 1.12 | ratio |
| | Duty cycle | Measured at SMCLK | 40% | 50% | 60% | |
| $df_{DCO}/dT$ | DCO frequency temperature drift | $f_{DCO}$ = 1 MHz | | 0.1 | | %/°C |
| $df_{DCO}/dV_{CORE}$ | DCO frequency voltage drift | $f_{DCO}$ = 1 MHz | | 1.9 | | %/V |

(1) When selecting the proper DCO frequency range (DCORSELx), the target DCO frequency, $f_{DCO}$, should be set to reside within the range of $f_{DCO(n,\ 0),MAX} \le f_{DCO} \le f_{DCO(n,\ 31),MIN}$, where $f_{DCO(n,\ 0),MAX}$ represents the maximum frequency specified for the DCO frequency, range n, tap 0 (DCOx = 0) and $f_{DCO(n,31),MIN}$ represents the minimum frequency specified for the DCO frequency, range n, tap 31 (DCOx = 31). This ensures that the target DCO frequency resides within the range selected. It should also be noted that if the actual $f_{DCO}$ frequency for the selected range causes the FLL or the application to select tap 0 or 31, the DCO fault flag is set to report that the selected range is at its minimum or maximum tap setting.




**Figure 5-10. Typical DCO Frequency**


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## 5.20 PMM, Brownout Reset (BOR)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{(DVCC_BOR_IT-)}$ | $BOR_H$ on voltage, $DV_{CC}$ falling level | $\lvert dDV_{CC}/d_t \rvert < 3$ V/s | | | 1.45 | V |
| $V_{(DVCC_BOR_IT+)}$ | $BOR_H$ off voltage, $DV_{CC}$ rising level | $\lvert dDV_{CC}/d_t \rvert < 3$ V/s | 0.80 | 1.20 | 1.50 | V |
| $V_{(DVCC_BOR_hys)}$ | $BOR_H$ hysteresis | | 50 | | 250 | mV |
| $t_{RESET}$ | Pulse duration required at $\overline{RST}$/NMI pin to accept a reset | | 2 | | | µs |

## 5.21 PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CORE3}$(AM) | Core voltage, active mode, PMMCOREV = 3 | 2.4 V ≤ $DV_{CC}$ ≤ 3.6 V | | 1.91 | | V |
| $V_{CORE2}$(AM) | Core voltage, active mode, PMMCOREV = 2 | 2.2 V ≤ $DV_{CC}$ ≤ 3.6 V | | 1.81 | | V |
| $V_{CORE1}$(AM) | Core voltage, active mode, PMMCOREV = 1 | 2 V ≤ $DV_{CC}$ ≤ 3.6 V | | 1.61 | | V |
| $V_{CORE0}$(AM) | Core voltage, active mode, PMMCOREV = 0 | 1.8 V ≤ $DV_{CC}$ ≤ 3.6 V | | 1.41 | | V |
| $V_{CORE3}$(LPM) | Core voltage, low-current mode, PMMCOREV = 3 | 2.4 V ≤ $DV_{CC}$ ≤ 3.6 V | | 1.94 | | V |
| $V_{CORE2}$(LPM) | Core voltage, low-current mode, PMMCOREV = 2 | 2.2 V ≤ $DV_{CC}$ ≤ 3.6 V | | 1.92 | | V |
| $V_{CORE1}$(LPM) | Core voltage, low-current mode, PMMCOREV = 1 | 2 V ≤ $DV_{CC}$ ≤ 3.6 V | | 1.73 | | V |
| $V_{CORE0}$(LPM) | Core voltage, low-current mode, PMMCOREV = 0 | 1.8 V ≤ $DV_{CC}$ ≤ 3.6 V | | 1.52 | | V |

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## 5.22 PMM, SVS High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{(SVSH)}$ | SVS current consumption | SVSHE = 0, $DV_{CC}$ = 3.6 V | | 0 | | nA |
| | | SVSHE = 1, $DV_{CC}$ = 3.6 V, SVSHFP = 0 | | 200 | | |
| | | SVSHE = 1, $DV_{CC}$ = 3.6 V, SVSHFP = 1 | | 1.5 | | µA |
| $V_{(SVSH_IT-)}$ | $SVS_H$ on voltage level | SVSHE = 1, SVSHRVL = 0 | 1.60 | 1.65 | 1.75 | V |
| | | SVSHE = 1, SVSHRVL = 1 | 1.77 | 1.84 | 1.95 | |
| | | SVSHE = 1, SVSHRVL = 2 | 1.93 | 2.00 | 2.12 | |
| | | SVSHE = 1, SVSHRVL = 3 | 2.09 | 2.16 | 2.29 | |
| $V_{(SVSH_IT+)}$ | $SVS_H$ off voltage level | SVSHE = 1, SVSMHRRL = 0 | 1.65 | 1.75 | 1.85 | V |
| | | SVSHE = 1, SVSMHRRL = 1 | 1.85 | 1.95 | 2.05 | |
| | | SVSHE = 1, SVSMHRRL = 2 | 2.05 | 2.15 | 2.25 | |
| | | SVSHE = 1, SVSMHRRL = 3 | 2.15 | 2.25 | 2.35 | |
| | | SVSHE = 1, SVSMHRRL = 4 | 2.30 | 2.40 | 2.55 | |
| | | SVSHE = 1, SVSMHRRL = 5 | 2.57 | 2.70 | 2.83 | |
| | | SVSHE = 1, SVSMHRRL = 6 | 2.90 | 3.05 | 3.20 | |
| | | SVSHE = 1, SVSMHRRL = 7 | 2.90 | 3.05 | 3.20 | |
| $t_{pd(SVSH)}$ | $SVS_H$ propagation delay | SVSHE = 1, $dV_{DVCC}/dt$ = 10 mV/µs, SVSHFP = 1 | | 2.5 | | µs |
| | | SVSHE = 1, $dV_{DVCC}/dt$ = 1 mV/µs, SVSHFP = 0 | | 20 | | |
| $t_{(SVSH)}$ | $SVS_H$ on or off delay time | SVSHE = 0 → 1, $dV_{DVCC}/dt$ = 10 mV/µs, SVSHFP = 1 | | 12.5 | | µs |
| | | SVSHE = 0 → 1, $dV_{DVCC}/dt$ = 1 mV/µs, SVSHFP = 0 | | 100 | | |
| $dV_{DVCC}/dt$ | DVCC rise time | | 0 | | 1000 | V/s |

## 5.23 PMM, SVM High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{(SVMH)}$ | $SVM_H$ current consumption | SVMHE = 0, $DV_{CC}$ = 3.6 V | | 0 | | nA |
| | | SVMHE = 1, $DV_{CC}$ = 3.6 V, SVMHFP = 0 | | 200 | | |
| | | SVMHE = 1, $DV_{CC}$ = 3.6 V, SVMHFP = 1 | | 1.5 | | µA |
| $V_{(SVMH)}$ | $SVM_H$ on or off voltage level[1] | SVMHE = 1, SVSMHRRL = 0 | 1.63 | 1.73 | 1.83 | V |
| | | SVMHE = 1, SVSMHRRL = 1 | 1.83 | 1.93 | 2.03 | |
| | | SVMHE = 1, SVSMHRRL = 2 | 2.03 | 2.13 | 2.23 | |
| | | SVMHE = 1, SVSMHRRL = 3 | 2.13 | 2.23 | 2.33 | |
| | | SVMHE = 1, SVSMHRRL = 4 | 2.28 | 2.40 | 2.53 | |
| | | SVMHE = 1, SVSMHRRL = 5 | 2.55 | 2.70 | 2.81 | |
| | | SVMHE = 1, SVSMHRRL = 6 | 2.88 | 3.02 | 3.18 | |
| | | SVMHE = 1, SVSMHRRL = 7 | 2.88 | 3.02 | 3.18 | |
| | | SVMHE = 1, SVMHOVPE = 1 | | 3.77 | | |
| $t_{pd(SVMH)}$ | $SVM_H$ propagation delay | SVMHE = 1, $dV_{DVCC}/dt$ = 10 mV/µs, SVMHFP = 1 | | 2.5 | | µs |
| | | SVMHE = 1, $dV_{DVCC}/dt$ = 1 mV/µs, SVMHFP = 0 | | 20 | | |
| $t_{(SVMH)}$ | $SVM_H$ on or off delay time | SVMHE = 0 → 1, $dV_{DVCC}/dt$ = 10 mV/µs, SVMHFP = 1 | | 12.5 | | µs |
| | | SVMHE = 0 → 1, $dV_{DVCC}/dt$ = 1 mV/µs, SVMHFP = 0 | | 100 | | |

(1) The $SVM_H$ settings available depend on the VCORE (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* on recommended settings and use.


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## 5.24 PMM, SVS Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{(SVSL)}$ | $SVS_L$ current consumption | SVSLE = 0, PMMCOREV = 2 | | 0 | | nA |
| | | SVSLE = 1, PMMCOREV = 2, SVSLFP = 0 | | 200 | | |
| | | SVSLE = 1, PMMCOREV = 2, SVSLFP = 1 | | 1.5 | | µA |
| $t_{pd(SVSL)}$ | $SVS_L$ propagation delay | SVSLE = 1, $dV_{CORE}/dt$ = 10 mV/µs, SVSLFP = 1 | | 2.5 | | µs |
| | | SVSLE = 1, $dV_{CORE}/dt$ = 1 mV/µs, SVSLFP = 0 | | 20 | | |
| $t_{(SVSL)}$ | $SVS_L$ on or off delay time | SVSLE = 0 → 1, $dV_{CORE}/dt$ = 10 mV/µs, SVSLFP = 1 | | 12.5 | | µs |
| | | SVSLE = 0 → 1, $dV_{CORE}/dt$ = 1 mV/µs, SVSLFP = 0 | | 100 | | |

## 5.25 PMM, SVM Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{(SVML)}$ | $SVM_L$ current consumption | SVMLE = 0, PMMCOREV = 2 | | 0 | | nA |
| | | SVMLE = 1, PMMCOREV = 2, SVMLFP = 0 | | 200 | | |
| | | SVMLE = 1, PMMCOREV = 2, SVMLFP = 1 | | 1.5 | | µA |
| $t_{pd(SVML)}$ | $SVM_L$ propagation delay | SVMLE = 1, $dV_{CORE}/dt$ = 10 mV/µs, SVMLFP = 1 | | 2.5 | | µs |
| | | SVMLE = 1, $dV_{CORE}/dt$ = 1 mV/µs, SVMLFP = 0 | | 20 | | |
| $t_{(SVML)}$ | $SVM_L$ on or off delay time | SVMLE = 0 → 1, $dV_{CORE}/dt$ = 10 mV/µs, SVMLFP = 1 | | 12.5 | | µs |
| | | SVMLE = 0 → 1, $dV_{CORE}/dt$ = 1 mV/µs, SVMLFP = 0 | | 100 | | |

## 5.26 Wake-up Times From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{WAKE-UP-FAST}$ | Wake-up time from LPM2, LPM3, or LPM4 to active mode(1) | PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 1 | $f_{MCLK} \geq 4.0$ MHz | | | 5 | µs |
| | | | $f_{MCLK} < 4.0$ MHz | | | 10 | |
| $t_{WAKE-UP-SLOW}$ | Wake-up time from LPM2, LPM3, or LPM4 to active mode(2)(3) | PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 0 | | | 150 | 165 | µs |
| $t_{WAKE-UP-LPM4.5}$ | Wake-up time from LPM4.5 to active mode(4) | | | | 2 | 3 | ms |
| $t_{WAKE-UP-RESET}$ | Wake-up time from $\overline{RST}$ or BOR event to active mode(4) | | | | 2 | 3 | ms |

(1) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor ($SVS_L$) and low-side monitor ($SVM_L$). $t_{WAKE-UP-FAST}$ is possible with $SVS_L$ and $SVM_L$ in full performance mode or disabled. For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the *MSP430x5xx and MSP430x6xx Family User's Guide*.

(2) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor ($SVS_L$) and low-side monitor ($SVM_L$). $t_{WAKE-UP-SLOW}$ is set with $SVS_L$ and $SVM_L$ in normal mode (low current mode). For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the *MSP430x5xx and MSP430x6xx Family User's Guide*.

(3) The wake-up times from LPM0 and LPM1 to AM are not specified. They are proportional to MCLK cycle time but are not affected by the performance mode settings as for LPM2, LPM3, and LPM4.

(4) This value represents the time from the wake-up event to the reset vector execution.

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## 5.27 Auxiliary Supplies Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range for all supplies at pins DVCC, AVCC, AUXVCC1, AUXVCC2, AUXVCC3 | | 1.8 | | 3.6 | V |
| $V_{DSYS}$ | Digital system supply voltage range, $V_{DSYS} = V_{CC} – R_{ON} \times I_{LOAD}$ | PMMCOREVx = 0 | 1.8 | | 3.6 | V |
| | | PMMCOREVx = 1 | 2.0 | | 3.6 | |
| | | PMMCOREVx = 2 | 2.2 | | 3.6 | |
| | | PMMCOREVx = 3 | 2.4 | | 3.6 | |
| $V_{ASYS}$ | Analog system supply voltage range, $V_{ASYS} = V_{CC} – R_{ON} \times I_{LOAD}$ | | See module specifications | | | V |
| $T_A$ | Ambient temperature range | | –40 | | 85 | °C |
| $T_{A,HTOL}$ | Ambient temperature during HTOL (module should be functional during HTOL) | | | | 150 | °C |
| $C_{VCC}$, $C_{AUX1/2}$ | Recommended capacitor at pins DVCC, AVCC, AUXVCC1, AUXVCC2 | | | 4.7 | | µF |
| $C_{VSYS}$ | Recommended capacitor at pins VDSYS1, VDSYS2 and VASYS1, VASYS2 | | | 4.7 | | µF |
| $C_{VCORE}$ | Recommended capacitance at pin VCORE | | | 0.47 | | µF |
| $C_{AUX3}$ | Recommended capacitor at pin AUXVCC3 | | | 0.47 | | µF |

## 5.28 Auxiliary Supplies, AUXVCC3 (Backup Subsystem) Currents

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{AUX3,RTCon}$ | AUXVCC3 current with RTC enabled | RTC and 32-kHz oscillator in backup subsystem enabled | 3 V | 25°C | | 0.86 | µA |
| | | | | 85°C | | 1.2 | |
| $I_{AUX3,RTCoff}$ | AUXVCC3 current with RTC disabled | RTC and 32-kHz oscillator in backup subsystem disabled | 3 V | 25°C | | 120 | nA |
| | | | | 85°C | | 220 | |

## 5.29 Auxiliary Supplies, Auxiliary Supply Monitor

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{CC,Monitor}$ | Average supply current for monitoring circuitry drawn from VDSYS | LOCKAUX = 0, AUXMRx = 0 AUX0MD = 0, AUX1MD = 0, AUX2MD = 1, VDSYS = DVCC, VASYS = AVCC, Current measured at VDSYS | | | 1.10 | µA |
| $I_{Meas,Montior}$ | Average current drawn from monitored supply during measurement cycle | LOCKAUX = 0, AUXMRx = 0 AUX0MD = 0, AUX1MD = 0, AUX2MD = 1, VDSYS = DVCC, VASYS = AVCC, Current measured at AUXVCC1 | | | 0.13 | µA |
| $V_{Monitor}$ | Auxiliary supply threshold level (same as high-side SVM) | General | $V_{SVMH}$ (SVSMHRRLx = AUXLVLx) | $V_{SVMH}$ (SVSMHRRLx = AUXLVLx) | $V_{SVMH}$ (SVSMHRRLx = AUXLVLx) | V |
| | | | X – 5% | | X + 5% | |
| | | AUXLVLx = 0 | 1.65 | 1.75 | 1.85 | |
| | | AUXLVLx = 1 | 1.85 | 1.95 | 2.05 | |
| | | AUXLVLx = 2 | 2.05 | 2.15 | 2.25 | |
| | | AUXLVLx = 3 | 2.15 | 2.25 | 2.35 | |
| | | AUXLVLx = 4 | 2.30 | 2.40 | 2.55 | |
| | | AUXLVLx = 5 | 2.57 | 2.70 | 2.83 | |
| | | AUXLVLx = 6 | 2.90 | 3.00 | 3.20 | |
| | | AUXLVLx = 7 | 2.90 | 3.00 | 3.20 | |


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## 5.30 Auxiliary Supplies, Switch ON-Resistance

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $R_{ON,DVCC}$ | ON-resistance of switch between DVCC and VDSYS | $I_{LOAD} = I_{CORE} + I_{IO} = 10\ mA + 10\ mA = 20\ mA$ | | 5 | Ω |
| $R_{ON,DAUX1}$ | ON-resistance of switch between AUXVCC1 and VDSYS | $I_{LOAD} = I_{CORE} + I_{IO} = 10\ mA + 10\ mA = 20\ mA$ | | 5 | Ω |
| $R_{ON,DAUX2}$ | ON-resistance of switch between AUXVCC2 and VDSYS | $I_{LOAD} = I_{CORE} + I_{IO} = 10\ mA + 10\ mA = 20\ mA$ | | 5 | Ω |
| $R_{ON,AVCC}$ | ON-resistance of switch between AVCC and $V_{ASYS}$ | $I_{LOAD} = I_{Modules} = 10\ mA$ | | 5 | Ω |
| $R_{ON,AAUX1}$ | ON-resistance of switch between AUXVCC1 and $V_{ASYS}$ | $I_{LOAD} = I_{Modules} = 5\ mA$ | | 20 | Ω |
| $R_{ON,AAUX2}$ | ON-resistance of switch between AUXVCC2 and $V_{ASYS}$ | $I_{LOAD} = I_{Modules} = 5\ mA$ | | 20 | Ω |

## 5.31 Auxiliary Supplies, Switching Time

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{Switch}$ | Time from occurrence of trigger (SVM or software) to "new" supply connected to system supplies | | 100 | ns |
| $t_{Recover}$ | "Recovery time" after a switch over took place. During that time no further switching takes place. | 170 | 480 | µs |

## 5.32 Auxiliary Supplies, Switch Leakage

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{SW,Lkg}$ | Current into DVCC, AVCC, AUXVCC1, or AUXVCC2 if not selected | Per supply (but not the highest supply) | | 75 | 250 | nA |
| $I_{Vmax}$ | Current drawn from highest supply | | | 500 | 700 | nA |

## 5.33 Auxiliary Supplies, Auxiliary Supplies to ADC10_A

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_3$ | Supply voltage divider, $V_3 = V_{Supply}/3$ | | | 1.8 V | 0.57 | 0.6 | 0.63 | V |
| | | | | 3 V | 0.95 | 1.0 | 1.05 | |
| | | | | 3.6 V | 1.14 | 1.2 | 1.26 | |
| $R_{V3}$ | Load resistance | AUXADCRx = 0 | | | | | 15 | kΩ |
| | | AUXADCRx = 1 | | | | | 1.5 | |
| | | AUXADCRx = 2 | | | | | 0.6 | |
| $t_{Sample,V3}$ | Sampling time required if $V_3$ selected | Error of conversion result ≤ 1 LSB | AUXADCRx = 0 | | 1000 | | | ns |
| | | | AUXADCRx = 1 | | 1000 | | | |
| | | | AUXADCRx = 2 | | 1000 | | | |

## 5.34 Auxiliary Supplies, Charge Limiting Resistor

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $R_{CHARGE}$ | Charge limiting resistor | AUXCHCx = 1 | 3 V | | | 5 | kΩ |
| | | AUXCHCx = 2 | 3 V | | | 10 | |
| | | AUXCHCx = 3 | 3 V | | | 20 | |

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## 5.35 Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{TA}$ | Timer_A input clock frequency | Internal: SMCLK or ACLK,<br>External: TACLK,<br>Duty cycle = 50% ±10% | 1.8 V, 3 V | | 25 | MHz |
| $t_{TA,cap}$ | Timer_A capture timing | All capture inputs, minimum pulse duration required for capture | 1.8 V, 3 V | 20 | | ns |

## 5.36 eUSCI (UART Mode) Clock Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{eUSCI}$ | eUSCI input clock frequency | Internal: SMCLK or ACLK,<br>External: UCLK,<br>Duty cycle = 50% ±10% | | $f_{SYSTEM}$ | MHz |
| $f_{BITCLK}$ | BITCLK clock frequency (equals baud rate in MBaud) | | | 5 | MHz |

## 5.37 eUSCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_t$ | UART receive deglitch time(1) | UCGLITx = 0 | 2 V, 3 V | 10 | 15 | 25 | ns |
| | | UCGLITx = 1 | | 30 | 50 | 85 | |
| | | UCGLITx = 2 | | 50 | 80 | 150 | |
| | | UCGLITx = 3 | | 70 | 120 | 200 | |

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To make sure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.


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## 5.38 eUSCI (SPI Master Mode) Clock Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{eUSCI}$ | eUSCI input clock frequency | Internal: SMCLK or ACLK,<br>Duty cycle = 50% ±10% | | $f_{SYSTEM}$ | MHz |

## 5.39 eUSCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{STE,LEAD}$ | STE lead time, STE low to clock | UCSTEM = 0, UCMODEx = 01 or 10 | 2 V, 3 V | 150 | | ns |
| | | UCSTEM = 1, UCMODEx = 01 or 10 | 2 V, 3 V | 150 | | |
| $t_{STE,LAG}$ | STE lag time, Last clock to STE high | UCSTEM = 0, UCMODEx = 01 or 10 | 2 V, 3 V | 200 | | ns |
| | | UCSTEM = 1, UCMODEx = 01 or 10 | 2 V, 3 V | 200 | | |
| $t_{STE,ACC}$ | STE access time, STE low to SIMO data out | UCSTEM = 0, UCMODEx = 01 or 10 | 2 V | | 50 | ns |
| | | | 3 V | | 30 | |
| | | UCSTEM = 1, UCMODEx = 01 or 10 | 2 V | | 50 | |
| | | | 3 V | | 30 | |
| $t_{STE,DIS}$ | STE disable time, STE high to SIMO high impedance | UCSTEM = 0, UCMODEx = 01 or 10 | 2 V | | 40 | ns |
| | | | 3 V | | 25 | |
| | | UCSTEM = 1, UCMODEx = 01 or 10 | 2 V | | 40 | |
| | | | 3 V | | 25 | |
| $t_{SU,MI}$ | SOMI input data setup time | | 2 V | 50 | | ns |
| | | | 3 V | 30 | | |
| $t_{HD,MI}$ | SOMI input data hold time | | 2 V | 0 | | ns |
| | | | 3 V | 0 | | |
| $t_{VALID,MO}$ | SIMO output data valid time(2) | UCLK edge to SIMO valid,<br>$C_L$ = 20 pF | 2 V | | 9 | ns |
| | | | 3 V | | 5 | |
| $t_{HD,MO}$ | SIMO output data hold time(3) | $C_L$ = 20 pF | 2 V | 0 | | ns |
| | | | 3 V | 0 | | |

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} = \max(t_{VALID,MO(eUSCI)} + t_{SU,SI(Slave)}, t_{SU,MI(eUSCI)} + t_{VALID,SO(Slave)})$
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.

(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-11 and Figure 5-12.

(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in Figure 5-11 and Figure 5-12.

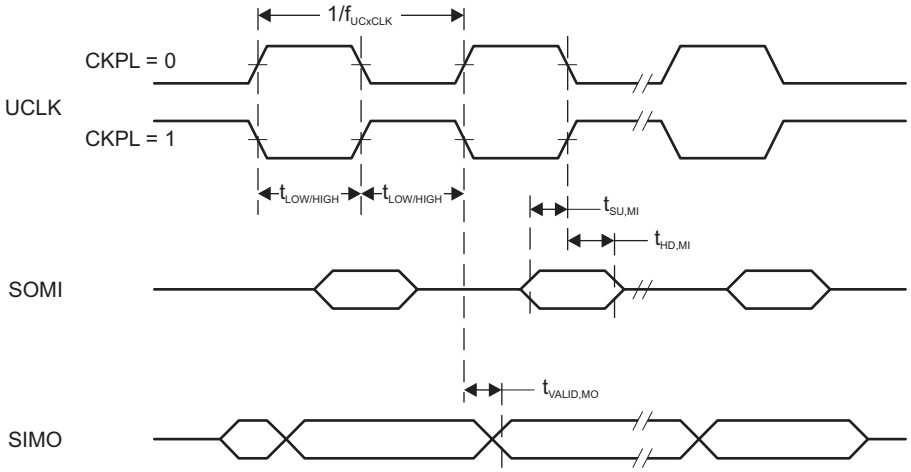



**Figure 5-11. SPI Master Mode, CKPH = 0**

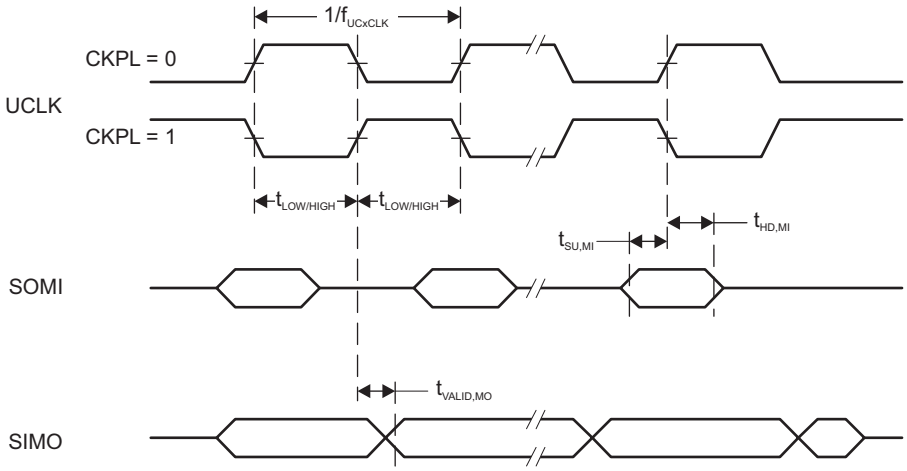



**Figure 5-12. SPI Master Mode, CKPH = 1**

## 5.40 eUSCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{STE,LEAD}$ | STE lead time, STE low to clock | | 2 V | 4 | | ns |
| | | | 3 V | 3 | | |
| $t_{STE,LAG}$ | STE lag time, Last clock to STE high | | 2 V | 0 | | ns |
| | | | 3 V | 0 | | |
| $t_{STE,ACC}$ | STE access time, STE low to SOMI data out | | 2 V | | 46 | ns |
| | | | 3 V | | 24 | |
| $t_{STE,DIS}$ | STE disable time, STE high to SOMI high impedance | | 2 V | | 38 | ns |
| | | | 3 V | | 25 | |
| $t_{SU,SI}$ | SIMO input data setup time | | 2 V | 2 | | ns |
| | | | 3 V | 1 | | |
| $t_{HD,SI}$ | SIMO input data hold time | | 2 V | 2 | | ns |
| | | | 3 V | 2 | | |
| $t_{VALID,SO}$ | SOMI output data valid time(2) | UCLK edge to SOMI valid, $C_L$ = 20 pF | 2 V | | 55 | ns |
| | | | 3 V | | 32 | |
| $t_{HD,SO}$ | SOMI output data hold time(3) | $C_L$ = 20 pF | 2 V | 24 | | ns |
| | | | 3 V | 16 | | |

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.
(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-13 and Figure 5-14.
(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in Figure 5-13 and Figure 5-14.


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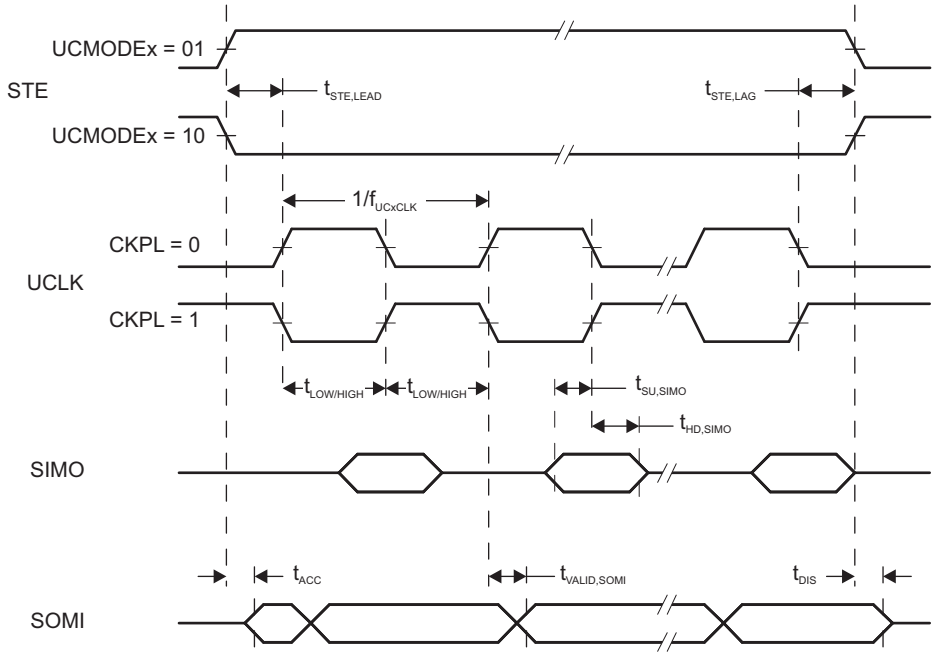



**Figure 5-13. SPI Slave Mode, CKPH = 0**

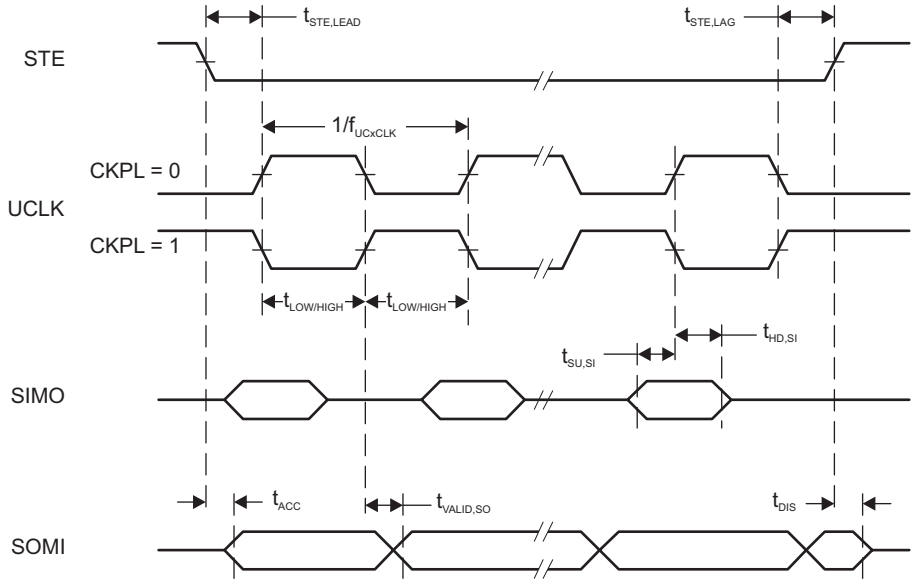



**Figure 5-14. SPI Slave Mode, CKPH = 1**

## 5.41 eUSCI (I²C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-15)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{eUSCI}$ | eUSCI input clock frequency | Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ±10% | | | | $f_{SYSTEM}$ | MHz |
| $f_{SCL}$ | SCL clock frequency | | 2 V, 3 V | 0 | | 400 | kHz |
| $t_{HD,STA}$ | Hold time (repeated) START | $f_{SCL}$ = 100 kHz | 2 V, 3 V | 5.1 | | | µs |
| | | $f_{SCL}$ > 100 kHz | | 1.5 | | | |
| $t_{SU,STA}$ | Setup time for a repeated START | $f_{SCL}$ = 100 kHz | 2 V, 3 V | 5.1 | | | µs |
| | | $f_{SCL}$ > 100 kHz | | 1.4 | | | |
| $t_{HD,DAT}$ | Data hold time | | 2 V, 3 V | 0.4 | | | µs |
| $t_{SU,DAT}$ | Data setup time | $f_{SCL}$ = 100 kHz | 2 V, 3 V | 5.0 | | | µs |
| | | $f_{SCL}$ > 100 kHz | | 1.3 | | | |
| $t_{SU,STO}$ | Setup time for STOP | $f_{SCL}$ = 100 kHz | 2 V, 3 V | 5.2 | | | µs |
| | | $f_{SCL}$ > 100 kHz | | 1.7 | | | |
| $t_{SP}$ | Pulse duration of spikes suppressed by input filter | UCGLITx = 0 | 2 V, 3 V | 75 | | 220 | ns |
| | | UCGLITx = 1 | | 35 | | 120 | |
| | | UCGLITx = 2 | | 30 | | 60 | |
| | | UCGLITx = 3 | | 20 | | 35 | |
| $t_{TIMEOUT}$ | Clock low time-out | UCCLTOx = 1 | 2 V, 3 V | | 30 | | ms |
| | | UCCLTOx = 2 | | | 33 | | |
| | | UCCLTOx = 3 | | | 37 | | |

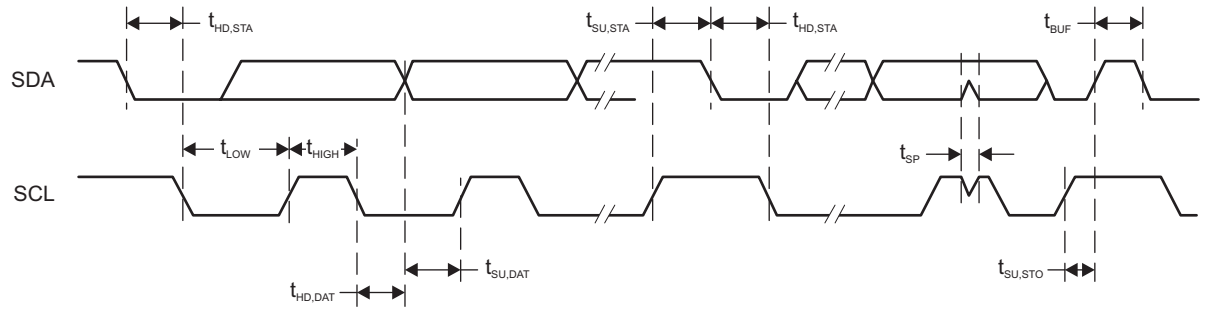



**Figure 5-15. I²C Mode Timing**


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## 5.42 Schmitt-Trigger Inputs, RTC Tamper Detect Pin

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | AUXVCC3 | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going input threshold voltage | | 1.8 V | 0.80 | | 1.40 | V |
| | | | 3 V | 1.50 | | 2.10 | |
| $V_{IT-}$ | Negative-going input threshold voltage | | 1.8 V | 0.45 | | 1.00 | V |
| | | | 3 V | 0.75 | | 1.65 | |
| $V_{hys}$ | Input voltage hysteresis ($V_{IT+} – V_{IT-}$) | | 1.8 V | 0.3 | | 0.85 | V |
| | | | 3 V | 0.4 | | 1.0 | |
| $R_{Pull}$ | Pullup or pulldown resistor | For pullup: $V_{IN} = V_{SS}$<br>For pulldown: $V_{IN}$ = AUXVCC3 | | 20 | 35 | 50 | kΩ |
| $C_I$ | Input capacitance | $V_{IN} = V_{SS}$ or AUXVCC3 | | | 5 | | pF |

## 5.43 Inputs, RTC Tamper Detect Pin(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | AUXVCC3 | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{(int)}$ | External interrupt timing(2) | Port P1, P2: P1.x to P2.x,<br>external trigger pulse duration to set interrupt flag | 2.2 V, 3 V | 20 | | ns |

(1) Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.
(2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It may be set by trigger signals shorter than $t_{(int)}$.

## 5.44 Leakage Current, RTC Tamper Detect Pin

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | AUXVCC3 | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{lkg(Px.y)}$ | High-impedance leakage current | See (1) (2) | 1.8 V, 3 V | –50 | +50 | nA |

(1) The leakage current is measured with $V_{SS}$ or $V_{CC}$ applied to the corresponding pins, unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

## 5.45 Outputs, RTC Tamper Detect Pin

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | AUXVCC3 | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{(OHmax)}$ = –100 µA(1) | 1.8 V | 1.50 | 1.80 | V |
| | | $I_{(OHmax)}$ = –200 µA(1) | | 1.20 | 1.80 | |
| | | $I_{(OHmax)}$ = –100 µA(1) | 3 V | 2.70 | 3.00 | |
| | | $I_{(OHmax)}$ = –200 µA(1) | | 2.40 | 3.00 | |
| $V_{OL}$ | Low-level output voltage | $I_{(OLmax)}$ = 100 µA(1) | 1.8 V | 0.00 | 0.25 | V |
| | | $I_{(OLmax)}$ = 200 µA(1) | | 0.00 | 0.60 | |
| | | $I_{(OLmax)}$ = 100 µA(1) | 3 V | 0.00 | 0.25 | |
| | | $I_{(OLmax)}$ = 200 µA(1) | | 0.00 | 0.60 | |

(1) The maximum total current, $I_{(OHmax)}$, for all outputs combined should not exceed ±20 mA to hold the maximum voltage drop specified. See Section 5.3 for more details.

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## 5.46 LCD_C Recommended Operating Conditions

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC,LCD_C,CP\ en,3.6}$ | Supply voltage range, charge pump enabled, $V_{LCD} \le 3.6$ V | LCDCPEN = 1, 0000 < VLCDx ≤ 1111 (charge pump enabled, $V_{LCD} \le 3.6$ V) | 2.2 | | 3.6 | V |
| $V_{CC,LCD_C,CP\ en,3.3}$ | Supply voltage range, charge pump enabled, $V_{LCD} \le 3.3$ V | LCDCPEN = 1, 0000 < VLCDx ≤ 1100 (charge pump enabled, $V_{LCD} \le 3.3$ V) | 2.0 | | 3.6 | V |
| $V_{CC,LCD_C,int.\ bias}$ | Supply voltage range, internal biasing, charge pump disabled | LCDCPEN = 0, VLCDEXT = 0 | 2.4 | | 3.6 | V |
| $V_{CC,LCD_C,ext.\ bias}$ | Supply voltage range, external biasing, charge pump disabled | LCDCPEN = 0, VLCDEXT = 0 | 2.4 | | 3.6 | V |
| $V_{CC,LCD_C,VLCDEXT}$ | Supply voltage range, external LCD voltage, internal or external biasing, charge pump disabled | LCDCPEN = 0, VLCDEXT = 1 | 2.0 | | 3.6 | V |
| $V_{LCDCAP/R33}$ | External LCD voltage at LCDCAP/R33, internal or external biasing, charge pump disabled | LCDCPEN = 0, VLCDEXT = 1 | 2.4 | | 3.6 | V |
| $C_{LCDCAP}$ | Capacitor on LCDCAP when charge pump enabled | LCDCPEN = 1, VLCDx > 0000 (charge pump enabled) | 4.7 | 4.7 | 10 | µF |
| $f_{LCD}$ | LCD frequency range | $f_{FRAME} = 1/(2 \times mux) \times f_{LCD}$ with mux = 1 (static) to 8 | 0 | | 1024 | Hz |
| $f_{FRAME,4mux}$ | LCD frame frequency range | $f_{FRAME,4mux}(MAX) = 1/(2 \times 4) \times f_{LCD}(MAX) = 1/(2 \times 4) \times 1024$ Hz | | | 128 | Hz |
| $f_{FRAME,8mux}$ | LCD frame frequency range | $f_{FRAME,8mux}(MAX) = 1/(2 \times 4) \times f_{LCD}(MAX) = 1/(2 \times 8) \times 1024$ Hz | | | 64 | Hz |
| $f_{ACLK,in}$ | ACLK input frequency range | | 30 | 32 | 40 | kHz |
| $C_{Panel}$ | Panel capacitance | 100-Hz frame frequency | | | 10000 | pF |
| $V_{R33}$ | Analog input voltage at R33 | LCDCPEN = 0, VLCDEXT = 1 | 2.4 | | $V_{CC}$ + 0.2 | V |
| $V_{R23,1/3bias}$ | Analog input voltage at R23 | LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 0 | $V_{R13}$ | $V_{R03}$ + 2/3 × ($V_{R33}$ – $V_{R03}$) | $V_{R33}$ | V |
| $V_{R13,1/3bias}$ | Analog input voltage at R13 with 1/3 biasing | LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 0 | $V_{R03}$ | $V_{R03}$ + 1/3 × ($V_{R33}$ – $V_{R03}$) | $V_{R23}$ | V |
| $V_{R13,1/2bias}$ | Analog input voltage at R13 with 1/2 biasing | LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 1 | $V_{R03}$ | $V_{R03}$ + 1/2 × ($V_{R33}$ – $V_{R03}$) | $V_{R33}$ | V |
| $V_{R03}$ | Analog input voltage at R03 | R0EXT = 1 | $V_{SS}$ | | | V |
| $V_{LCD}$-$V_{R03}$ | Voltage difference between $V_{LCD}$ and R03 | LCDCPEN = 0, R0EXT = 1 | 2.4 | | $V_{CC}$ + 0.2 | V |
| $V_{LCDREF/R13}$ | External LCD reference voltage applied at LCDREF/R13 | VLCDREFx = 01 | 0.8 | 1.2 | 1.5 | V |


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## 5.47 LCD_C Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{LCD}$ | LCD voltage | VLCDx = 0000, VLCDEXT = 0 | 2.4 V to 3.6 V | | $V_{CC}$ | | V |
| | | LCDCPEN = 1, VLCDx = 0001 | 2 V to 3.6 V | | 2.60 | | |
| | | LCDCPEN = 1, VLCDx = 0010 | | | 2.66 | | |
| | | LCDCPEN = 1, VLCDx = 0011 | | | 2.72 | | |
| | | LCDCPEN = 1, VLCDx = 0100 | | | 2.78 | | |
| | | LCDCPEN = 1, VLCDx = 0101 | | | 2.84 | | |
| | | LCDCPEN = 1, VLCDx = 0110 | | | 2.90 | | |
| | | LCDCPEN = 1, VLCDx = 0111 | | | 2.96 | | |
| | | LCDCPEN = 1, VLCDx = 1000 | | | 3.02 | | |
| | | LCDCPEN = 1, VLCDx = 1001 | | | 3.08 | | |
| | | LCDCPEN = 1, VLCDx = 1010 | | | 3.14 | | |
| | | LCDCPEN = 1, VLCDx = 1011 | | | 3.20 | | |
| | | LCDCPEN = 1, VLCDx = 1100 | | | 3.26 | | |
| | | LCDCPEN = 1, VLCDx = 1101 | 2.2 V to 3.6 V | | 3.32 | | |
| | | LCDCPEN = 1, VLCDx = 1110 | | | 3.38 | | |
| | | LCDCPEN = 1, VLCDx = 1111 | | | 3.50 | 3.72 | |
| $I_{CC,Peak,CP}$ | Peak supply currents due to charge pump activities | LCDCPEN = 1, VLCDx = 1111 | 2.2 V | | 200 | | µA |
| $t_{LCD,CP,on}$ | Time to charge $C_{LCD}$ when discharged | $C_{LCD}$ = 4.7 µF, LCDCPEN = 0→1, VLCDx = 1111 | 2.2 V | | 100 | 500 | ms |
| $I_{CP,Load}$ | Maximum charge pump load current | LCDCPEN = 1, VLCDx = 1111 | 2.2 V | 50 | | | µA |
| $R_{LCD,Seg}$ | LCD driver output impedance, segment lines | LCDCPEN = 1, VLCDx = 1000, $I_{LOAD}$ = ±10 µA | 2.2 V | | | 10 | kΩ |
| $R_{LCD,COM}$ | LCD driver output impedance, common lines | LCDCPEN = 1, VLCDx = 1000, $I_{LOAD}$ = ±10 µA | 2.2 V | | | 10 | kΩ |

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## 5.48 SD24_B Power Supply and Recommended Operating Conditions

| | | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $AV_{CC}$ | Analog supply voltage | $AV_{CC}$ = $DV_{CC}$, $AV_{SS}$ = $DV_{SS}$ = 0 V | | 2.4 | | 3.6 | V |
| $T_A$ | Ambient temperature | | | –40 | | 85 | °C |
| $f_{SD}$ | Modulator clock frequency | | | 0.03 | | 2.3 | MHz |
| $V_I$ | Absolute input voltage range | | | $AV_{SS}$ – 1 | | $AV_{CC}$ | V |
| $V_{IC}$ | Common-mode input voltage range | | | $AV_{SS}$ – 1 | | $AV_{CC}$ | V |
| $V_{ID,FS}$ | Differential full-scale input voltage | Bipolar mode, $V_{ID}$ = $V_{I,A+}$ – $V_{I,A–}$ | | $–V_{REF}$/GAIN | | $+V_{REF}$/GAIN | mV |
| $V_{ID}$ | Differential input voltage for specified performance (1) | REFON = 1 | SD24GAINx = 1 | ±900 | ±930 | | mV |
| | | | SD24GAINx = 2 | ±450 | ±460 | | |
| | | | SD24GAINx = 4 | ±225 | ±230 | | |
| | | | SD24GAINx = 8 | ±112 | ±120 | | |
| | | | SD24GAINx = 16 | ±56 | ±60 | | |
| | | | SD24GAINx = 32 | ±28 | ±30 | | |
| | | | SD24GAINx = 64 | ±14 | ±14 | | |
| | | | SD24GAINx = 128 | ±7 | ±7.25 | | |
| $C_{REF}$ | VREF load capacitance (2) | SD24REFS = 1 | | | 100 | | nF |

(1) The full-scale range (FSR) is defined by $V_{FS+}$ = $+V_{REF}$/GAIN and $V_{FS–}$ = $–V_{REF}$/GAIN: FSR = $V_{FS+}$ – $V_{FS–}$ = 2 × $V_{REF}$/GAIN. If $V_{REF}$ is sourced externally, the analog input range should not exceed 80% of $V_{FS+}$ or $V_{FS–}$, that is, $V_{ID}$ = 0.8 $V_{FS–}$ to 0.8 $V_{FS+}$. If $V_{REF}$ is sourced internally, the given $V_{ID}$ ranges apply. MIN values are calculated based on a $V_{REF}$ of 1.125 V. TYP values are calculated based on a $V_{REF}$ of 1.16 V.
(2) There is no capacitance required on VREF. However, TI recommends a capacitance of 100 nF to reduce any reference voltage noise.

## 5.49 SD24_B Analog Input (1)

also see Figure 5-16

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $C_I$ | Input capacitance | SD24GAINx = 1 | | | | 5.0 | | pF |
| | | SD24GAINx = 2 | | | | 5.0 | | |
| | | SD24GAINx = 4 | | | | 5.0 | | |
| | | SD24GAINx = 8 | | | | 5.0 | | |
| | | SD24GAINx = 16 | | | | 5.0 | | |
| | | SD24GAINx = 32, 64, 128 | | | | 5.0 | | |
| $Z_I$ | Input impedance (pin A+ or A– to $AV_{SS}$) | $f_{SD24}$ = 1 MHz | SD24GAINx = 1 | 3 V | | 200 | | kΩ |
| | | | SD24GAINx = 8 | | | 200 | | |
| | | | SD24GAINx = 32 | | | 200 | | |
| $Z_{ID}$ | Differential input impedance (pin A+ to pin A–) | $f_{SD24}$ = 1 MHz | SD24GAINx = 1 | 3 V | 300 | 400 | | kΩ |
| | | | SD24GAINx = 8 | | | 400 | | |
| | | | SD24GAINx = 32 | | 300 | 400 | | |

(1) All parameters pertain to each SD24_B converter.


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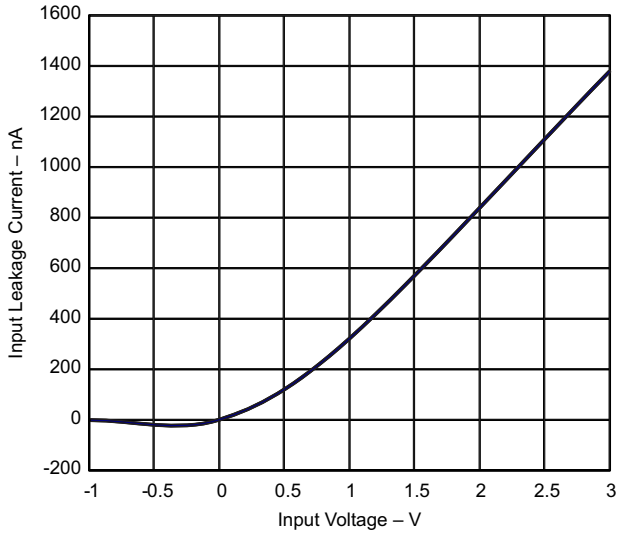



**Figure 5-16. Input Leakage Current vs Input Voltage (Modulator OFF)**

## 5.50 SD24_B Supply Currents

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_{SD,256}$ | Analog plus digital supply current per converter (reference not included) | $f_{SD24}$ = 1 MHz, SD24OSR = 256 | SD24GAIN: 1 | 3 V | | 490 | 600 | µA |
| | | | SD24GAIN: 2 | | | 490 | 600 | |
| | | | SD24GAIN: 4 | | | 490 | 600 | |
| | | | SD24GAIN: 8 | | | 559 | 700 | |
| | | | SD24GAIN: 16 | | | 559 | 700 | |
| | | | SD24GAIN: 32 | | | 627 | 800 | |
| | | | SD24GAIN: 64 | | | 627 | 800 | |
| | | | SD24GAIN: 128 | | | 627 | 800 | |
| $I_{SD,512}$ | Analog plus digital supply current per converter (reference not included) | $f_{SD24}$ = 2 MHz, SD24OSR = 512 | SD24GAIN: 1 | 3 V | | 600 | 700 | µA |
| | | | SD24GAIN: 8 | | | 677 | 800 | |
| | | | SD24GAIN: 32 | | | 740 | 900 | |

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## 5.51 SD24_B Performance

$f_{SD24}$ = 1 MHz, SD24OSRx = 256, SD24REFON = 1

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| INL | Integral nonlinearity, end-point fit | SD24GAIN: 1 | 3 V | –0.01 | | +0.01 | % FSR |
| | | SD24GAIN: 8 | | –0.01 | | +0.01 | |
| | | SD24GAIN: 32 | | –0.01 | | +0.01 | |
| $G_{nom}$ | Nominal gain | SD24GAIN: 1 | 3 V | | 1 | | |
| | | SD24GAIN: 2 | | | 2 | | |
| | | SD24GAIN: 4 | | | 4 | | |
| | | SD24GAIN: 8 | | | 8 | | |
| | | SD24GAIN: 16 | | | 16 | | |
| | | SD24GAIN: 32 | | | 32 | | |
| | | SD24GAIN: 64 | | | 64 | | |
| | | SD24GAIN: 128 | | | 128 | | |
| $E_G$ | Gain error (1) | SD24GAIN: 1, with external reference (1.2 V) | 3 V | –1% | | +1% | |
| | | SD24GAIN: 8, with external reference (1.2 V) | | –2% | | +2% | |
| | | SD24GAIN: 32, with external reference (1.2 V) | | –2% | | +2% | |
| $\Delta E_G/\Delta T$ | Gain error temperature coefficient (2), internal reference | SD24GAIN: 1, 8, or 32 (with internal reference) | 3 V | | | 80 | ppm/°C |
| $\Delta E_G/\Delta T$ | Gain error temperature coefficient (2), external reference | SD24GAIN: 1 (with external reference) | 3 V | | | 15 | ppm/°C |
| | | SD24GAIN: 8 (with external reference) | | | | 15 | |
| | | SD24GAIN: 32 (with external reference) | | | | 15 | |
| $\Delta E_G/\Delta V_{CC}$ | Gain error vs $V_{CC}$ (3) | SD24GAIN: 1 | 3 V | | 0.1 | | %/V |
| | | SD24GAIN: 8 | | | 0.1 | | |
| | | SD24GAIN: 32 | | | 0.4 | | |
| $E_{OS}$[V] | Offset error (4) | SD24GAIN: 1 (with Vdiff = 0 V) | 3 V | | | 2.3 | mV |
| | | SD24GAIN: 8 | | | | 1 | |
| | | SD24GAIN: 32 | | | | 0.5 | |
| $E_{OS}$[FS] | Offset error (4) | SD24GAIN: 1 (with Vdiff = 0 V) | 3 V | –0.2 | | +0.2 | % FS |
| | | SD24GAIN: 8 | | –0.7 | | +0.7 | |
| | | SD24GAIN: 32 | | –1.4 | | +1.4 | |
| $\Delta E_{OS}/\Delta T$ | Offset error temperature coefficient (5) | SD24GAIN: 1 | 3 V | | 2 | | µV/°C |
| | | SD24GAIN: 8 | | | 0.25 | | |
| | | SD24GAIN: 32 | | | 0.1 | | |

(1) The gain error $E_G$ specifies the deviation of the actual gain $G_{act}$ from the nominal gain $G_{nom}$: $E_G = (G_{act} – G_{nom})/G_{nom}$. It covers process, temperature, and supply voltage variations.

(2) The gain error temperature coefficient $\Delta E_G/\Delta T$ specifies the variation of the gain error $E_G$ over temperature ($E_G(T) = (G_{act}(T) – G_{nom})/G_{nom}$) using the box method (that is, minimum and maximum values):
$\Delta E_G/\Delta T = (MAX(E_G(T)) – MIN(E_G(T)) / (MAX(T) – MIN(T)) = (MAX(G_{act}(T)) – MIN(G_{act}(T)) / G_{nom} / (MAX(T) – MIN(T))$
with T ranging from –40°C to 85°C.

(3) The gain error vs $V_{CC}$ coefficient $\Delta E_G/\Delta V_{CC}$ specifies the variation of the gain error $E_G$ over supply voltage ($E_G(V_{CC}) = (G_{act}(V_{CC}) – G_{nom})/G_{nom}$) using the box method (that is, minimum and maximum values):
$\Delta E_G/\Delta V_{CC} = (MAX(E_G(V_{CC})) – MIN(E_G(V_{CC})) / (MAX(V_{CC}) – MIN(V_{CC})) = (MAX(G_{act}(V_{CC})) – MIN(G_{act}(V_{CC})) / G_{nom} / (MAX(V_{CC}) – MIN(V_{CC}))$
with $V_{CC}$ ranging from 2.4 V to 3.6 V.

(4) The offset error $E_{OS}$ is measured with shorted inputs in 2s-complement mode with +100% FS = $V_{REF}/G$ and –100% FS = $-V_{REF}/G$. Conversion between $E_{OS}$ [FS] and $E_{OS}$ [V] is as follows: $E_{OS}$ [FS] = $E_{OS}$ [V] × $G/V_{REF}$, $E_{OS}$ [V] = $E_{OS}$ [FS] × $V_{REF}/G$.

(5) The offset error temperature coefficient $\Delta E_{OS}/\Delta T$ specifies the variation of the offset error $E_{OS}$ over temperature using the box method (that is, minimum and maximum values):
$\Delta E_{OS}/\Delta T = (MAX(E_{OS}(T)) – MIN(E_{OS}(T)) / (MAX(T) – MIN(T))$
with T ranging from –40°C to 85°C.


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## SD24_B Performance *(continued)*

$f_{SD24}$ = 1 MHz, SD24OSRx = 256, SD24REFON = 1

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $\Delta E_{OS}/\Delta V_{CC}$ | Offset error vs $V_{CC}$ (6) | SD24GAIN: 1 | 3 V | | 500 | | µV/V |
| | | SD24GAIN: 8 | | | 125 | | |
| | | SD24GAIN: 32 | | | 50 | | |
| CMRR,DC | Common-mode rejection at DC (7) | SD24GAIN: 1 | 3 V | | –120 | | dB |
| | | SD24GAIN: 8 | | | –110 | | |
| | | SD24GAIN: 32 | | | –100 | | |
| CMRR,50 Hz | Common-mode rejection at 50 Hz (8) | SD24GAIN: 1, $f_{CM}$ = 50 Hz, $V_{CM}$ = 930 mV | 3 V | | –120 | | dB |
| | | SD24GAIN: 8, $f_{CM}$ = 50 Hz, $V_{CM}$ = 120 mV | | | –110 | | |
| | | SD24GAIN: 32, $f_{CM}$ = 50 Hz, $V_{CM}$ = 30 mV | | | –100 | | |
| AC PSRR,ext | AC power supply rejection ratio, external reference (9) | SD24GAIN: 1, $V_{CC}$ = 3 V + 50 mV × sin(2π × $f_{VCC}$ × t), $f_{VCC}$ = 50 Hz | | | –61 | | dB |
| | | SD24GAIN: 8, $V_{CC}$ = 3 V + 50 mV × sin(2π × $f_{VCC}$ × t), $f_{VCC}$ = 50 Hz | | | –75 | | |
| | | SD24GAIN: 32, $V_{CC}$ = 3 V + 50 mV × sin(2π × $f_{VCC}$ × t), $f_{VCC}$ = 50 Hz | | | –79 | | |
| AC PSRR,int | AC power supply rejection ratio, internal reference (9) | SD24GAIN: 1, $V_{CC}$ = 3 V + 50 mV × sin(2π × $f_{VCC}$ × t), $f_{VCC}$ = 50 Hz | | | –61 | | dB |
| | | SD24GAIN: 8, $V_{CC}$ = 3 V + 50 mV × sin(2π × $f_{VCC}$ × t), $f_{VCC}$ = 50 Hz | | | –75 | | |
| | | SD24GAIN: 32, $V_{CC}$ = 3 V + 50 mV × sin(2π × $f_{VCC}$ × t), $f_{VCC}$ = 50 Hz | | | –79 | | |
| XT | Crosstalk between converters (10) | Crosstalk source: SD24GAIN: 1, Sine-wave with maximum possible Vpp, $f_{IN}$ = 50 Hz or 100 Hz, Converter under test: SD24GAIN: 1 | 3 V | | –120 | | dB |
| | | Crosstalk source: SD24GAIN: 1, Sine-wave with maximum possible Vpp, $f_{IN}$ = 50 Hz or 100 Hz, Converter under test: SD24GAIN: 8 | | | –115 | | |
| | | Crosstalk source: SD24GAIN: 1, Sine-wave with maximum possible Vpp, $f_{IN}$ = 50 Hz or 100 Hz, Converter under test: SD24GAIN: 32 | | | –110 | | |

(6) The offset error vs $V_{CC}$ $\Delta E_{OS}$ / $\Delta V_{CC}$ specifies the variation of the offset error $E_{OS}$ over supply voltage using the box method (that is, minimum and maximum values):
$\Delta E_{OS}$ / $\Delta V_{CC}$ = (MAX($E_{OS}$($V_{CC}$)) – MIN($E_{OS}$($V_{CC}$)) ) / (MAX($V_{CC}$) – MIN($V_{CC}$))
with $V_{CC}$ ranging from 2.4 V to 3.6 V.

(7) The DC CMRR specifies the change in the measured differential input voltage value when the common-mode voltage varies:
DC CMRR = –20log($\Delta_{MAX}$ / FSR) with $\Delta_{MAX}$ being the difference between the minium value and the maximum value measured when sweeping the common-mode voltage.
The DC CMRR is measured with both inputs connected to the common-mode voltage (that is, no differential input signal is applied), and the common-mode voltage is swept from –1 V to $V_{CC}$.

(8) The AC CMRR is the difference between a hypothetical signal with the amplitude and frequency of the applied common-mode ripple applied to the inputs of the ADC and the actual common-mode signal spur visible in the FFT spectrum:
AC CMRR = Error Spur [dBFS] – 20log($V_{CM}$ / 1.2 V / G) [dBFS] with a common-mode signal of $V_{CM}$ × sin(2π × $f_{CM}$ × t) applied to the analog inputs.
The AC CMRR is measured with the both inputs connected to the common-mode signal; that is, no differential input signal is applied.
With the specified typical values the error spur is within the noise floor (as specified by the SINAD values).

(9) The AC PSRR is the difference between a hypothetical signal with the amplitude and frequency of the applied supply voltage ripple applied to the inputs of the ADC and the actual supply ripple spur visible in the FFT spectrum:
AC PSRR = Error Spur [dBFS] – 20log(50 mV / 1.2 V / G) [dBFS] with a signal of 50 mV × sin(2π × $f_{VCC}$ × t) added to $V_{CC}$.
The AC PSRR is measured with the inputs grounded; that is, no analog input signal is applied.
With the specified typical values the error spur is within the noise floor (as specified by the SINAD values).
SD24GAIN: 1 → Hypothetical signal: 20log(50 mV / 1.2 V / 1) = –27.6 dBFS
SD24GAIN: 8 → Hypothetical signal: 20log(50 mV / 1.2 V / 8) = –9.5 dBFS
SD24GAIN: 32 → Hypothetical signal: 20log(50 mV / 1.2 V / 32) = 2.5 dBFS

(10) The crosstalk (XT) is specified as the tone level of the signal applied to the crosstalk source seen in the spectrum of the converter under test. It is measured with the inputs of the converter under test being grounded.

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## 5.52 SD24_B, AC Performance

$f_{SD24}$ = 1 MHz, SD24OSRx = 256, SD24REFON = 1 (see Figure 5-17)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| SINAD | Signal-to-noise + distortion ratio | SD24GAIN: 1 | $f_{IN}$ = 50 Hz (1) | 3 V | 84 | 86 | | dB |
| | | SD24GAIN: 2 | | | | 85 | | |
| | | SD24GAIN: 4 | | | | 84 | | |
| | | SD24GAIN: 8 | | | 81 | 83 | | |
| | | SD24GAIN: 16 | | | | 80 | | |
| | | SD24GAIN: 32 | | | 71 | 73 | | |
| | | SD24GAIN: 64 | | | | 67 | | |
| | | SD24GAIN: 128 | | | | 61 | | |
| THD | Total harmonic distortion | SD24GAIN: 1 | $f_{IN}$ = 50 Hz (1) | 3 V | | 95 | | dB |
| | | SD24GAIN: 8 | | | | 90 | | |
| | | SD24GAIN: 32 | | | | 86 | | |

(1) The following voltages were applied to the SD24_B inputs: $V_{I,A+}(t) = 0\ V + V_{PP} / 2 \times \sin(2\pi \times f_{IN} \times t)$ and $V_{I,A-}(t) = 0\ V - V_{PP} / 2 \times \sin(2\pi \times f_{IN} \times t)$
resulting in a differential voltage of $V_{ID} = V_{I,A+}(t) - V_{I,A-}(t) = V_{PP} \times \sin(2\pi \times f_{IN} \times t)$ with $V_{PP}$ being selected as the maximum value allowed for a given range (according to SD24_B recommended operating conditions).

## 5.53 SD24_B, AC Performance

$f_{SD24}$ = 2 MHz, SD24OSRx = 512, SD24REFON = 1

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| SINAD | Signal-to-noise + distortion ratio | SD24GAIN: 1 | $f_{IN}$ = 50 Hz (1) | 3 V | | 87 | | dB |
| | | SD24GAIN: 2 | | | | 85 | | |
| | | SD24GAIN: 4 | | | | 84 | | |
| | | SD24GAIN: 8 | | | | 83 | | |
| | | SD24GAIN: 16 | | | | 81 | | |
| | | SD24GAIN: 32 | | | | 76 | | |
| | | SD24GAIN: 64 | | | | 71 | | |
| | | SD24GAIN: 128 | | | | 65 | | |

(1) The following voltages were applied to the SD24_B inputs: $V_{I,A+}(t) = 0\ V + V_{PP} / 2 \times \sin(2\pi \times f_{IN} \times t)$ and $V_{I,A-}(t) = 0\ V - V_{PP} / 2 \times \sin(2\pi \times f_{IN} \times t)$
resulting in a differential voltage of $V_{ID} = V_{I,A+}(t) - V_{I,A-}(t) = V_{PP} \times \sin(2\pi \times f_{IN} \times t)$ with $V_{PP}$ being selected as the maximum value allowed for a given range (according to SD24_B recommended operating conditions).

## 5.54 SD24_B, AC Performance

$f_{SD24}$ = 32 kHz, SD24OSRx = 512, SD24REFON = 1

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| SINAD | Signal-to-noise + distortion ratio | SD24GAIN: 1 | $f_{IN}$ = 50 Hz (1) | 3 V | | 89 | | dB |
| | | SD24GAIN: 2 | | | | 85 | | |
| | | SD24GAIN: 4 | | | | 84 | | |
| | | SD24GAIN: 8 | | | | 82 | | |
| | | SD24GAIN: 16 | | | | 80 | | |
| | | SD24GAIN: 32 | | | | 76 | | |
| | | SD24GAIN: 64 | | | | 67 | | |
| | | SD24GAIN: 128 | | | | 61 | | |

(1) The following voltages were applied to the SD24_B inputs: $V_{I,A+}(t) = 0\ V + V_{PP} / 2 \times \sin(2\pi \times fIN \times t)$ and $V_{I,A-}(t) = 0\ V - V_{PP} / 2 \times \sin(2\pi \times f_{IN} \times t)$
resulting in a differential voltage of $V_{ID} = V_{I,A+}(t) - V_{I,A-}(t) = V_{PP} \times \sin(2\pi \times f_{IN} \times t)$ with $V_{PP}$ being selected as the maximum value allowed for a given range (according to SD24_B recommended operating conditions) (also see Figure 5-18).


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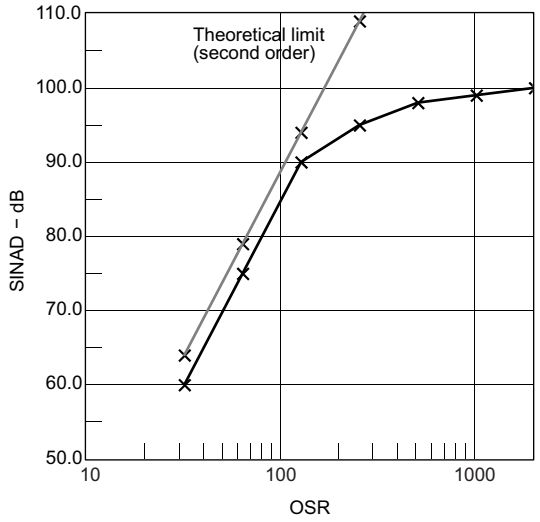



**Figure 5-17. SINAD vs OSR**
**($f_{SD24}$ = 1 MHz, SD24REFON = 1, SD24GAIN: 1)**

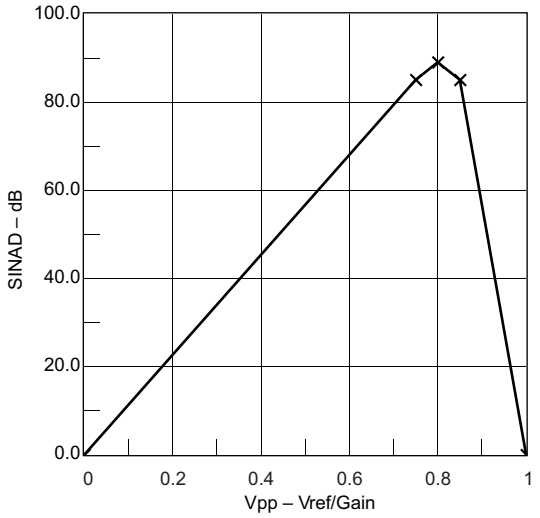



**Figure 5-18. SINAD vs $V_{PP}$**

## 5.55 SD24_B External Reference Input

ensure correct input voltage range according to $V_{REF}$

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{REF(I)}$ | Input voltage | SD24REFS = 0 | 3 V | 1.0 | 1.20 | 1.5 | V |
| $I_{REF(I)}$ | Input current | SD24REFS = 0 | 3 V | | | 50 | nA |

## 5.56 10-Bit ADC Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $AV_{CC}$ | Analog supply voltage | AVCC and DVCC are connected together, AVSS and DVSS are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V | | 1.8 | | 3.6 | V |
| $V_{(Ax)}$ | Analog input voltage range(1) | All ADC10_A pins | | 0 | | $AV_{CC}$ | V |
| $I_{ADC10_A}$ | Operating supply current into AVCC terminal, REF module and reference buffer off | $f_{ADC10CLK}$ = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 00 | 2.2 V | | 68 | 100 | µA |
| | | | 3 V | | 78 | 110 | |
| | Operating supply current into AVCC terminal, REF module on, reference buffer on | $f_{ADC10CLK}$ = 5 MHz, ADC10ON = 1, REFON = 1, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 01 | 3 V | | 124 | 180 | |
| | Operating supply current into AVCC terminal, REF module off, reference buffer on | $f_{ADC10CLK}$ = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 10, VEREF = 2.5 V | | | 105 | 160 | |
| | Operating supply current into AVCC terminal, REF module off, reference buffer off | $f_{ADC10CLK}$ = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 11, VEREF = 2.5 V | | | 72 | 110 | |
| $C_I$ | Input capacitance | Only one terminal Ax can be selected at one time from the pad to the ADC10_A capacitor array including wiring and pad. | 2.2 V | | 3.5 | | pF |
| $R_I$ | Input MUX ON resistance | $AV_{CC}$ > 2.0 V, 0 V ≤ $V_{Ax}$ ≤ $AV_{CC}$ | | | | 36 | kΩ |
| | | 1.8 V < $AV_{CC}$ < 2.0 V, 0 V ≤ $V_{Ax}$ ≤ $AV_{CC}$ | | | | 96 | |

(1) The analog input voltage range must be within the selected reference voltage range $V_{R+}$ to $V_{R-}$ for valid conversion results. The external reference voltage requires decoupling capacitors. Two decoupling capacitors, 10 µF and 100 nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC10_A. Also see the *MSP430x5xx and MSP430x6xx Family User's Guide*.

## 5.57 10-Bit ADC Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{ADC10CLK}$ | | For specified performance of ADC10_A linearity parameters | 2.2 V, 3 V | 0.45 | 5 | 5.5 | MHz |
| $f_{ADC10OSC}$ | Internal ADC10_A oscillator(1) | ADC10DIV = 0, $f_{ADC10CLK}$ = $f_{ADC10OSC}$ | 2.2 V, 3 V | 4.4 | 4.9 | 5.6 | MHz |
| $t_{CONVERT}$ | Conversion time | REFON = 0, Internal oscillator, 12 ADC10CLK cycles, 10-bit mode, $f_{ADC10OSC}$ = 4 MHz to 5 MHz | 2.2 V, 3 V | 2.4 | | 3.0 | µs |
| | | External $f_{ADC10CLK}$ from ACLK, MCLK, or SMCLK, ADC10SSEL ≠ 0 | | | 12 × 1 / $f_{ADC10CLK}$ | | |
| $t_{ADC10ON}$ | Turnon settling time of the ADC | See (2) | | | | 100 | ns |
| $t_{Sample}$ | Sampling time | $R_S$ = 1000 Ω, $R_I$ = 96 kΩ, $C_I$ = 3.5 pF(3) | 1.8 V | 3 | | | µs |
| | | $R_S$ = 1000 Ω, $R_I$ = 36 kΩ, $C_I$ = 3.5 pF(3) | 3 V | 1 | | | |

(1) The ADC10OSC is sourced directly from MODOSC inside the UCS.
(2) The condition is that the error in a conversion started after $t_{ADC10ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.
(3) Approximately 8 Tau (τ) are needed to get an error of less than ±0.5 LSB


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## 5.58 10-Bit ADC Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $E_I$ | Integral linearity error | $1.4\ V \le (V_{eREF+} - V_{eREF-}) \le 1.6\ V$, $C_{VeREF+} = 20\ pF$ | 2.2 V, 3 V | –1.0 | +1.0 | LSB |
| | | $1.6\ V < (V_{eREF+} - V_{eREF-}) \le V_{AVCC}$, $C_{VeREF+} = 20\ pF$ | | –1.0 | +1.0 | |
| $E_D$ | Differential linearity error | $1.4\ V \le (V_{eREF+} - V_{eREF-})$, $C_{VeREF+} = 20\ pF$ | 2.2 V, 3 V | –1.0 | +1.0 | LSB |
| $E_O$ | Offset error | $1.4\ V \le (V_{eREF+} - V_{eREF-})$, $C_{VeREF+} = 20\ pF$<br>Internal impedance of source $R_S < 100\ \Omega$ | 2.2 V, 3 V | –1.0 | +1.0 | LSB |
| $E_G$ | Gain error | $1.4\ V \le (V_{eREF+} - V_{eREF-})$, $C_{VeREF+} = 20\ pF$,<br>ADC10SREFx = 11b | 2.2 V, 3 V | –1.0 | +1.0 | LSB |
| $E_T$ | Total unadjusted error | $1.4\ V \le (V_{eREF+} - V_{eREF-})$, $C_{VeREF+} = 20\ pF$,<br>ADC10SREFx = 11b | 2.2 V, 3 V | –2.0 | +2.0 | LSB |

## 5.59 10-Bit ADC External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{eREF+}$ | Positive external reference voltage input | $V_{eREF+} > V_{eREF-}$ (2) | | 1.4 | $AV_{CC}$ | V |
| $V_{eREF-}$ | Negative external reference voltage input | $V_{eREF+} > V_{eREF-}$ (3) | | 0 | 1.2 | V |
| $(V_{eREF+} - V_{eREF-})$ | Differential external reference voltage input | $V_{eREF+} > V_{eREF-}$ (4) | | 1.4 | $AV_{CC}$ | V |
| $I_{VeREF+}$, $I_{VeREF-}$ | Static input current | $1.4\ V \le V_{eREF+} \le V_{AVCC}$, $V_{eREF-} = 0\ V$,<br>$f_{ADC10CLK} = 5\ MHz$, ADC10SHTx = 0x0001,<br>Conversion rate 200 ksps | 2.2 V, 3 V | –26 | +26 | µA |
| | | $1.4\ V \le V_{eREF+} \le V_{AVCC}$, $V_{eREF-} = 0\ V$,<br>$f_{ADC10CLK} = 5\ MHZ$, ADC10SHTX = 0x1000,<br>Conversion rate 20 ksps | | –1 | +1 | |
| $C_{VREF+}$ | Capacitance at VREF+ terminal | See (5) | | 10 | | µF |

(1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, $C_I$, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
(3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
(5) Two decoupling capacitors, 10 µF and 100 nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC10_A. Also see the *MSP430x5xx and MSP430x6xx Family User's Guide*.

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## 5.60 REF Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{REF+}$ | Positive built-in reference voltage | REFVSEL = {2} for 2.5 V, REFON = 1 | 3 V | 2.47 | 2.51 | 2.55 | V |
| | | REFVSEL = {1} for 2 V, REFON = 1 | | 1.96 | 1.99 | 2.02 | |
| | | REFVSEL = {0} for 1.5 V, REFON = 1 | 2.2 V, 3 V | 1.48 | 1.5 | 1.52 | |
| $AV_{CC(min)}$ | AVCC minimum voltage, Positive built-in reference active | REFVSEL = {0} for 1.5 V | | 1.8 | | | V |
| | | REFVSEL = {1} for 2 V | | 2.2 | | | |
| | | REFVSEL = {2} for 2.5 V | | 2.7 | | | |
| $I_{REF+}$ | Operating supply current into AVCC terminal (1) | $f_{ADC10CLK}$ = 5.0 MHz, REFON = 1, REFBURST = 0, REFVSEL = {2} for 2.5 V | 3 V | | 18 | 24 | µA |
| | | $f_{ADC10CLK}$ = 5.0 MHz, REFON = 1, REFBURST = 0, REFVSEL = {1} for 2 V | | | 16.1 | 21 | |
| | | $f_{ADC10CLK}$ = 5.0 MHz, REFON = 1, REFBURST = 0, REFVSEL = {0} for 1.5 V | | | 14.4 | 21 | |
| $TC_{REF+}$ | Temperature coefficient of built-in reference (2) | $I_{VREF+}$ = 0 A, REFVSEL = {0, 1, 2}, REFON = 1 | | | <18 | 50 | ppm/°C |
| $I_{SENSOR}$ | Operating supply current into AVCC terminal (3) | REFON = 0, INCH = 0Ah, ADC10ON = N/A, $T_A$ = 30°C | 2.2 V | | 17 | 22 | µA |
| | | | 3 V | | 17 | 22 | |
| $V_{SENSOR}$ | See (4) | ADC10ON = 1, INCH = 0Ah, $T_A$ = 30°C | 2.2 V | | 770 | | mV |
| | | | 3 V | | 770 | | |
| $V_{MID}$ | $AV_{CC}$ divider at channel 11 | ADC10ON = 1, INCH = 0Bh, $V_{MID} \approx 0.5 \times V_{AVCC}$ | 2.2 V | 1.06 | 1.1 | 1.14 | V |
| | | | 3 V | 1.46 | 1.5 | 1.54 | |
| $t_{SENSOR(sample)}$ | Sample time required if channel 10 is selected (5) | ADC10ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB | | 30 | | | µs |
| $t_{VMID(sample)}$ | Sample time required if channel 11 is selected (6) | ADC10ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB | | 1 | | | µs |
| PSRR_DC | Power supply rejection ratio (DC) | $AV_{CC}$ = $AV_{CC(min)}$ to $AV_{CC(max)}$, $T_A$ = 25°C, REFVSEL = {0, 1, 2}, REFON = 1 | | | 120 | | µV/V |
| PSRR_AC | Power supply rejection ratio (AC) | $AV_{CC}$ = $AV_{CC(min)}$ to $AV_{CC(max)}$, $T_A$ = 25°C, f = 1 kHz, ΔVpp = 100 mV, REFVSEL = {0, 1, 2}, REFON = 1 | | | 6.4 | | mV/V |
| $t_{SETTLE}$ | Settling time of reference voltage (7) | $AV_{CC}$ = $AV_{CC(min)}$ to $AV_{CC(max)}$, REFVSEL = {0, 1, 2}, REFON = 0→1 | | | 75 | | µs |
| $V_{SD24REF}$ | SD24_B internal reference voltage | SD24REFS = 1 | 3 V | 1.151 | 1.1623 | 1.174 | V |
| $t_{ON}$ | SD24_B internal reference turnon time | SD24REFS = 0→1, $C_{REF}$ = 100 nF | 3 V | | 200 | | µs |

(1) The internal reference current is supplied from the AVCC terminal. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an analog-to-digital conversion.
(2) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C)).
(3) The sensor current $I_{SENSOR}$ is consumed if (ADC10ON = 1 and REFON = 1) or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, $I_{SENSOR}$ is already included in $I_{REF+}$.
(4) The temperature sensor offset can be significant. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.
(5) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
(6) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.
(7) The condition is that the error in a conversion started after $t_{REFON}$ is less than ±0.5 LSB.


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## 5.61 Comparator_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | 1.8 | | 3.6 | V |
| $I_{AVCC_COMP}$ | Comparator operating supply current into AVCC, excludes reference resistor ladder | CBPWRMD = 00, CBON = 1, CBRSx = 00 | 1.8 V | | | 40 | µA |
| | | | 2.2 V | | 22 | 50 | |
| | | | 3 V | | 32 | 65 | |
| | | CBPWRMD = 01, CBON = 1, CBRSx = 00 | 2.2 V, 3 V | | 10 | 30 | |
| | | CBPWRMD = 10, CBON = 1, CBRSx = 00 | | | 0.2 | 0.85 | |
| $I_{AVCC_REF}$ | Quiescent current of resistor ladder into AVCC, includes REF module current | CBREFACC = 1, CBREFLx = 01, CBRSx = 10, REFON = 0, CBON = 0 | 2.2 V, 3 V | | 10 | 22 | µA |
| | | CBREFACC = 0, CBREFLx = 01, CBRSx = 10, REFON = 0, CBON = 0 | | | 33 | 40 | |
| $V_{IC}$ | Common-mode input range | | | 0 | | $V_{CC}$ – 1 | V |
| $V_{OFFSET}$ | Input offset voltage | CBPWRMD = 00 | | –20 | | +20 | mV |
| | | CBPWRMD = 01, 10 | | –20 | | +20 | |
| $C_{IN}$ | Input capacitance | | | | 5 | | pF |
| $R_{SIN}$ | Series input resistance | On (switch closed) | | | 3 | 4 | kΩ |
| | | Off (switch open) | | 50 | | | MΩ |
| $t_{PD}$ | Propagation delay, response time | CBPWRMD = 00, CBF = 0 | | | | 450 | ns |
| | | CBPWRMD = 01, CBF = 0 | | | | 600 | |
| | | CBPWRMD = 10, CBF = 0 | | | | 50 | µs |
| $t_{PD,filter}$ | Propagation delay with filter active | CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 00 | | 0.30 | 0.6 | 1.5 | µs |
| | | CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 01 | | 0.5 | 1.0 | 1.8 | |
| | | CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 10 | | 0.8 | 1.8 | 3.4 | |
| | | CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 11 | | 1.5 | 3.4 | 6.5 | |
| $t_{EN_CMP}$ | Comparator enable time | CBON = 0 → 1, CBPWRMD = 00, 01 | | | 1 | 2 | µs |
| | | CBON = 0 → 1, CBPWRMD = 10 | | | | 100 | |
| $t_{EN_REF}$ | Resistor reference enable time | CBON = 0 → 1 | | | 1.0 | 1.5 | µs |
| $TC_{REF}$ | Temperature coefficient reference | | | | | 50 | ppm/°C |
| $V_{CB_REF}$ | Reference voltage for a given tap | VIN = reference into resistor ladder, n = 0 to 31 | | VIN × (n + 1.5) / 32 | VIN × (n + 1) / 32 | VIN × (n + 0.5) / 32 | V |

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## 5.62 Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | $T_J$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $DV_{CC(PGM/ERASE)}$ | Program and erase supply voltage | | 1.8 | | 3.6 | V |
| $I_{PGM}$ | Average supply current from DVCC during program | | | 3 | 5 | mA |
| $I_{ERASE}$ | Average supply current from DVCC during erase | | | 6 | 15 | mA |
| $I_{MERASE}$, $I_{BANK}$ | Average supply current from DVCC during mass erase or bank erase | | | 6 | 15 | mA |
| $t_{CPT}$ | Cumulative program time(1) | | | | 16 | ms |
| | Program and erase endurance | | $10^4$ | $10^5$ | | cycles |
| $t_{Retention}$ | Data retention duration | 25°C | 100 | | | years |
| $t_{Word}$ | Word or byte program time(2) | | 64 | | 85 | µs |
| $t_{Block, 0}$ | Block program time for first byte or word(2) | | 49 | | 65 | µs |
| $t_{Block, 1–(N–1)}$ | Block program time for each additional byte or word, except for last byte or word(2) | | 37 | | 49 | µs |
| $t_{Block, N}$ | Block program time for last byte or word(2) | | 55 | | 73 | µs |
| $t_{Erase}$ | Erase time for segment erase, mass erase, and bank erase when available(2) | | 23 | | 32 | ms |
| $f_{MCLK,MGR}$ | MCLK frequency in marginal read mode (FCTL4.MGR0 = 1 or FCTL4. MGR1 = 1) | | 0 | | 1 | MHz |

(1) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word or byte write and block write modes.
(2) These values are hardwired into the state machine of the flash controller.

## 5.63 JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SBW}$ | Spy-Bi-Wire input frequency | 2.2 V, 3 V | 0 | | 20 | MHz |
| $t_{SBW,Low}$ | Spy-Bi-Wire low clock pulse duration | 2.2 V, 3 V | 0.025 | | 15 | µs |
| $t_{SBW, En}$ | Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge)(1) | 2.2 V, 3 V | | | 1 | µs |
| $t_{SBW,Rst}$ | Spy-Bi-Wire return to normal operation time | | 15 | | 100 | µs |
| $f_{TCK}$ | TCK input frequency for 4-wire JTAG(2) | 2.2 V | 0 | | 5 | MHz |
| | | 3 V | 0 | | 10 | MHz |
| $R_{internal}$ | Internal pulldown resistance on TEST | 2.2 V, 3 V | 45 | 60 | 80 | kΩ |

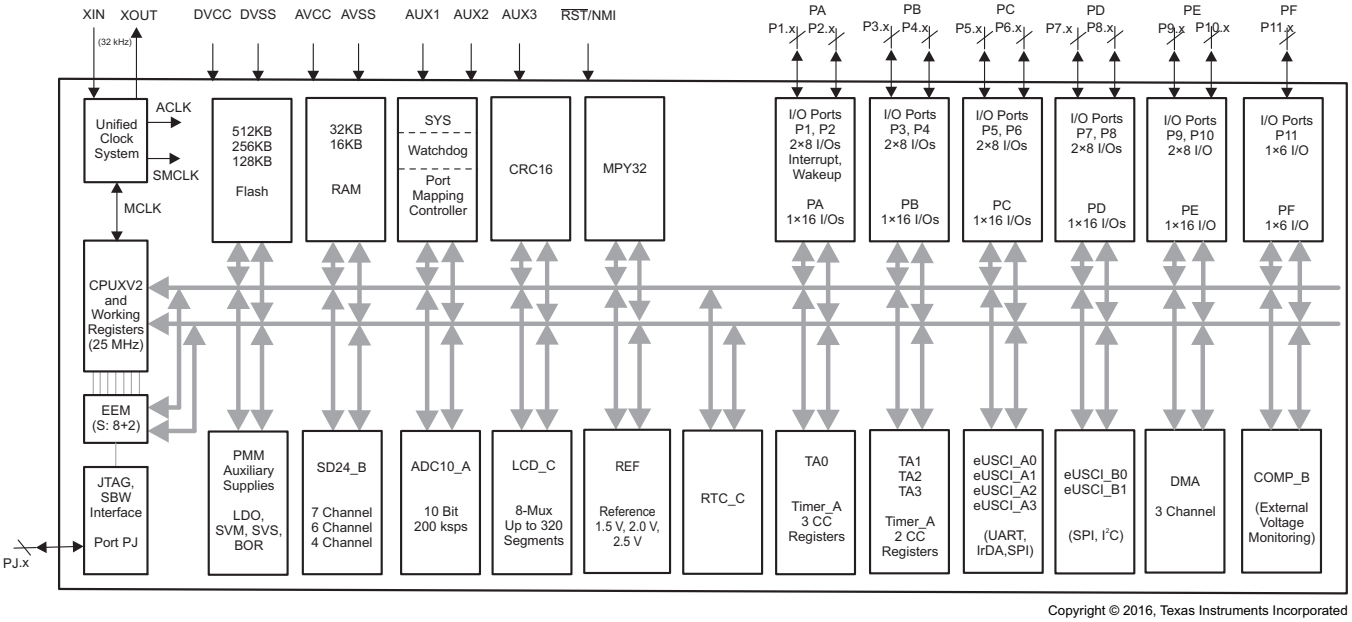
(1) Tools that access the Spy-Bi-Wire interface must wait for the minimum $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
(2) $f_{TCK}$ may be restricted to meet the timing requirements of the module selected.


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# 6 Detailed Description

## 6.1 Functional Block Diagrams

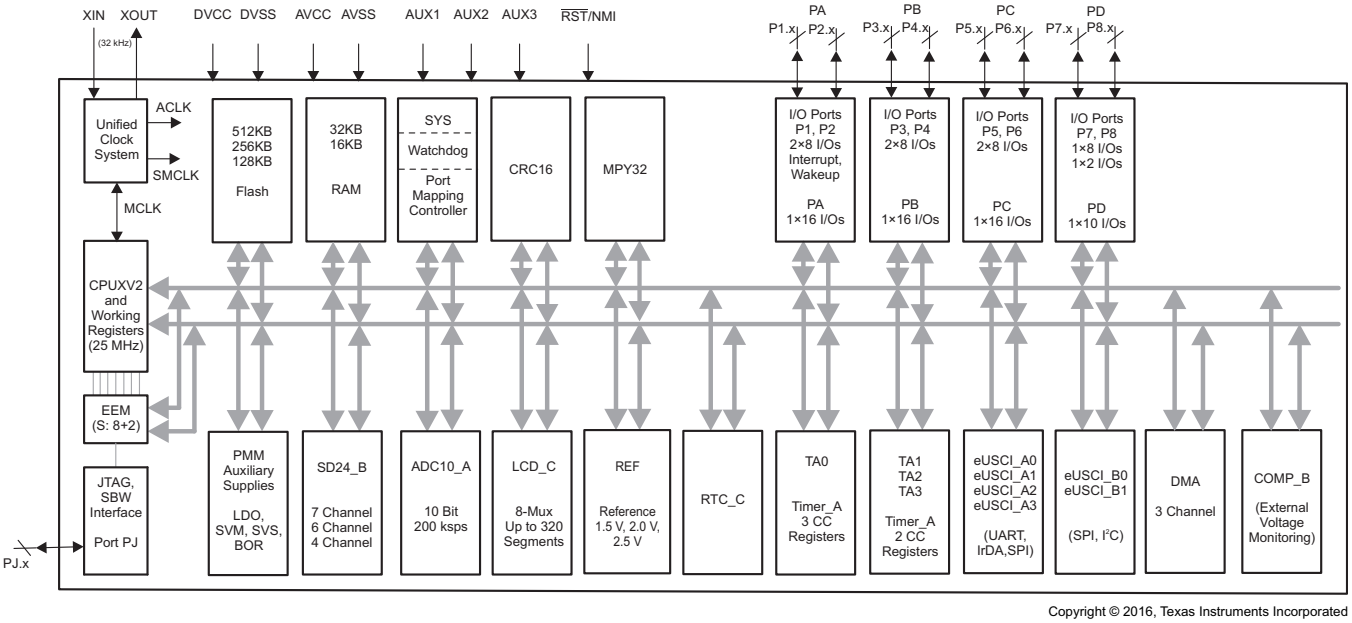
Figure 6-1 shows the functional block diagram for all devices in the PEU package.




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**Figure 6-1. Functional Block Diagram – MSP430F677x1IPEU, MSP430F676x1IPEU, and MSP430F674x1IPEU**

Figure 6-2 shows the functional block diagram for all devices in the PZ package.




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**Figure 6-2. Functional Block Diagram – MSP430F677x1IPZ, MSP430F676x1IPZ, and MSP430F674x1IPZ**

## 6.2 CPU (Link to User's Guide)

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock. Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers (see Figure 6-3).

Peripherals are connected to the CPU using data, address, and control buses. Peripherals can be managed with all instructions.

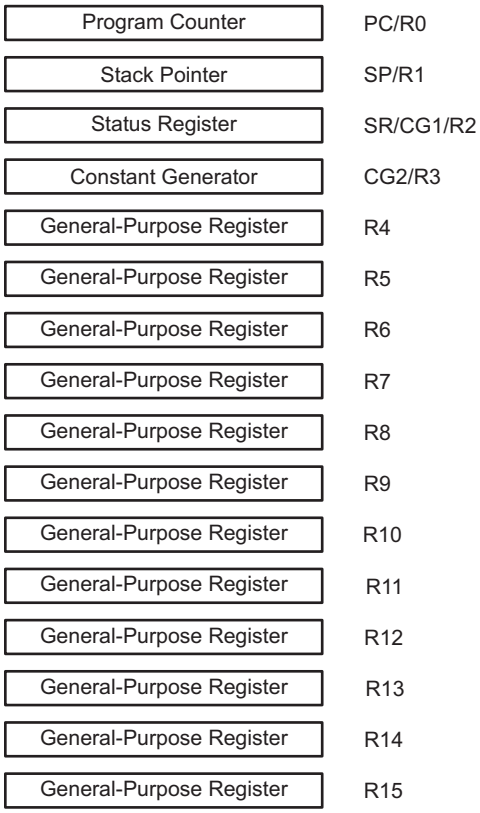



**Figure 6-3. CPU Registers**


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## 6.3 Instruction Set

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data. Table 6-1 lists examples of the three types of instruction formats. Table 6-2 lists the address modes.

**Table 6-1. Instruction Word Formats**

| INSTRUCTION WORD FORMAT | EXAMPLE | OPERATION |
|---|---|---|
| Dual operands, source and destination | ADD R4,R5 | R4 + R5 → R5 |
| Single operands, destination only | CALL R8 | PC → (TOS), R8 → PC |
| Relative jump, unconditional or conditional | JNE | Jump-on-equal bit = 0 |

**Table 6-2. Address Mode Descriptions**

| ADDRESS MODE | S(1) | D(1) | SYNTAX | EXAMPLE | OPERATION |
|---|---|---|---|---|---|
| Register | + | + | MOV Rs,Rd | MOV R10,R11 | R10 → R11 |
| Indexed | + | + | MOV X(Rn),Y(Rm) | MOV 2(R5),6(R6) | M(2+R5) → M(6+R6) |
| Symbolic (PC relative) | + | + | MOV EDE,TONI | | M(EDE) → M(TONI) |
| Absolute | + | + | MOV & MEM, & TCDAT | | M(MEM) → M(TCDAT) |
| Indirect | + | | MOV @Rn,Y(Rm) | MOV @R10,Tab(R6) | M(R10) → M(Tab+R6) |
| Indirect autoincrement | + | | MOV @Rn+,Rm | MOV @R10+,R11 | M(R10) → R11<br>R10 + 2 → R10 |
| Immediate | + | | MOV #X,TONI | MOV #45,TONI | #45 → M(TONI) |

(1) S = source, D = destination

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## 6.4 Operating Modes

These microcontrollers have one active mode and seven software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

Software can configure the following operating modes:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
  - FLL loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - FLL loop control is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK and FLL loop control and DCOCLK are disabled
  - DC generator of the DCO remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO is disabled
  - Crystal oscillator is stopped
  - Complete data retention
- Low-power mode 3.5 (LPM3.5)
  - Internal regulator disabled
  - No RAM retention, backup RAM retained
  - I/O pad state retention
  - RTC clocked by low-frequency oscillator
  - Wake-up input from $\overline{\text{RST}}$/NMI, RTC_C events, Ports P1 and P2
- Low-power mode 4.5 (LPM4.5)
  - Internal regulator disabled
  - No RAM retention, backup RAM retained
  - RTC is disabled
  - I/O pad state retention
  - Wake-up input from $\overline{\text{RST}}$/NMI, Ports P1 and P2


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## 6.5 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FF80h (see Table 6-3). The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

**Table 6-3. Interrupt Sources, Flags, and Vectors**

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|---|---|---|---|
| **System Reset**<br>Power up<br>External reset<br>Watchdog time-out, key violation<br>Flash memory key violation | WDTIFG, KEYV (SYSRSTIV)(1) (2) | Reset | 0FFFEh | 63, highest |
| **System NMI**<br>PMM<br>Vacant memory access<br>JTAG mailbox | SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VLRLIFG, VLRHIFG, VMAIFG, JMBNIFG, JMBOUTIFG (SYSSNIV) (1) (3) | (Non)maskable | 0FFFCh | 62 |
| **User NMI**<br>NMI<br>Oscillator fault<br>Flash memory access violation<br>Supply switched | NMIIFG, OFIFG, ACCVIFG, AUXSWGIFG (SYSUNIV)(1) (3) | (Non)maskable | 0FFFAh | 61 |
| Watchdog Timer_A interval timer mode | WDTIFG | Maskable | 0FFF8h | 60 |
| eUSCI_A0 receive or transmit | UCA0RXIFG, UCA0TXIFG (UCA0IV)(1) (4) | Maskable | 0FFF6h | 59 |
| eUSCI_B0 receive or transmit | UCB0RXIFG, UCB0TXIFG (UCB0IV)(1) (4) | Maskable | 0FFF4h | 58 |
| ADC10_A | ADC10IFG0, ADC10INIFG, ADC10LOIFG, ADC10HIIFG, ADC10TOVIFG, ADC10OVIFG (ADC10IV)(1) (4) | Maskable | 0FFF2h | 57 |
| SD24_B | SD24_B Interrupt Flags (SD24IV)(1) (4) | Maskable | 0FFF0h | 56 |
| Timer TA0 | TA0CCR0 CCIFG0(4) | Maskable | 0FFEEh | 55 |
| Timer TA0 | TA0CCR1 CCIFG1, TA0CCR2 CCIFG2, TA0IFG (TA0IV)(1) (4) | Maskable | 0FFECh | 54 |
| eUSCI_A1 receive or transmit | UCA1RXIFG, UCA1TXIFG (UCA1IV)(1) (4) | Maskable | 0FFEAh | 53 |
| eUSCI_A2 receive or transmit | UCA2RXIFG, UCA2TXIFG (UCA2IV)(1) (4) | Maskable | 0FFE8h | 52 |
| Auxiliary supplies | AUXSWGIFG, AUXIFG0, AUXIFG1, AUXIFG2 (AUXIV)(1) (4) | Maskable | 0FFE6h | 51 |
| DMA | DMA0IFG, DMA1IFG, DMA2IFG (DMAIV)(1) (4) | Maskable | 0FFE4h | 50 |
| Timer TA1 | TA1CCR0 CCIFG0(4) | Maskable | 0FFE2h | 49 |
| Timer TA1 | TA1CCR1 CCIFG1, TA1IFG (TA1IV)(1) (4) | Maskable | 0FFE0h | 48 |
| eUSCI_A3 receive or transmit | UCA3RXIFG, UCA3TXIFG (UCA3IV)(1) (4) | Maskable | 0FFDEh | 47 |
| eUSCI_B1 receive or transmit | UCB1RXIFG, UCB1TXIFG (UCB1IV)(1) (4) | Maskable | 0FFDCh | 46 |
| I/O port P1 | P1IFG.0 to P1IFG.7 (P1IV)(1) (4) | Maskable | 0FFDAh | 45 |
| Timer TA2 | TA2CCR0 CCIFG0(4) | Maskable | 0FFD8h | 44 |
| Timer TA2 | TA2CCR1 CCIFG1, TA2IFG (TA2IV)(1) (4) | Maskable | 0FFD6h | 43 |
| I/O port P2 | P2IFG.0 to P2IFG.7 (P2IV)(1) (4) | Maskable | 0FFD4h | 42 |
| Timer TA3 | TA3CCR0 CCIFG0(4) | Maskable | 0FFD2h | 41 |
| Timer TA3 | TA3CCR1 CCIFG1, TA3IFG (TA3IV)(1) (4) | Maskable | 0FFD0h | 40 |
| LCD_C | LCD_C Interrupt Flags (LCDCIV)(1) (4) | Maskable | 0FFCEh | 39 |

(1) Multiple source flags
(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space.
(3) (Non)maskable: the individual interrupt enable bit can disable an interrupt event, but the general interrupt enable bit cannot disable it.
(4) Interrupt flags are in the module.

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**Table 6-3. Interrupt Sources, Flags, and Vectors (continued)**

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|---|---|---|---|
| RTC_C | RTCOFIFG, RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG (RTCIV)(1) (4) | Maskable | 0FFCCh | 38 |
| Comparator_B | Comparator_B Interrupt Flags (CBIV) (1) | Maskable | 0FFCAh | 37 |
| Reserved | Reserved(5) | | 0FFC6h | 35 |
| | | | ⋮ | ⋮ |
| | | | 0FF80h | 0, lowest |

(5) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, TI recommends reserving these locations.


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## 6.6 Special Function Registers (SFRs)

The MSP430 SFRs are in the lowest address space and can be accessed in word or byte formats.

**Legend**

| | |
|---|---|
| rw | Bit can be read and written. |
| rw-0, rw-1 | Bit can be read and written. It is reset or set by PUC. |
| rw-(0), rw-(1) | Bit can be read and written. It is reset or set by POR. |
| rw-[0], rw-[1] | Bit can be read and written. It is reset or set by BOR. |
| – | SFR bit is not present in device. |

**Figure 6-4. Interrupt Enable 1 Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| – | – | – | – | – | – | AUXSWNMIE | – |
| | | | | | | rw-0 | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| JMBOUTIE | JMBINIE | ACCVIE | NMIIE | VMAIE | – | OFIE | WDTIE |
| rw-0 | rw-0 | rw-0 | rw-0 | rw-0 | | rw-0 | rw-0 |

**Table 6-4. Interrupt Enable 1 Register Description**

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 9 | AUXSWNMIE | RW | 0h | Supply switched nonmaskable interrupt enable |
| 7 | JMBOUTIE | RW | 0h | JTAG mailbox output interrupt enable |
| 6 | JMBINIE | RW | 0h | JTAG mailbox input interrupt enable |
| 5 | ACCVIE | RW | 0h | Flash access violation interrupt enable |
| 4 | NMIIE | RW | 0h | Nonmaskable interrupt enable |
| 3 | VMAIE | RW | 0h | Vacant memory access interrupt enable |
| 1 | OFIE | RW | 0h | Oscillator fault interrupt enable |
| 0 | WDTIE | RW | 0h | Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured as a general-purpose timer. |

**Figure 6-5. Interrupt Flag 1 Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| – | – | – | – | – | – | – | – |
| | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| JMBOUTIFG | JMBINIFG | – | NMIIFG | VMAIFG | – | OFIFG | WDTIFG |
| rw-[0] | rw-[0] | | rw-0 | rw-0 | | rw-0 | rw-0 |

**Table 6-5. Interrupt Flag 1 Register Description**

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7 | JMBOUTIFG | RW | 0h | Set on JTAG mailbox output register ready for next message |
| 6 | JMBINIFG | RW | 0h | Set on JTAG mailbox input message |
| 4 | NMIIFG | RW | 0h | Set by $\overline{\text{RST}}$/NMI pin |
| 3 | VMAIFG | RW | 0h | Set on vacant memory access |
| 1 | OFIFG | RW | 0h | Flag set on oscillator fault |
| 0 | WDTIFG | RW | 0h | Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on $V_{CC}$ power-on or a reset condition at the $\overline{\text{RST}}$/NMI pin in reset mode. |

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## 6.7 Memory Organization

Table 6-6 and Table 6-7 summarize the memory map for the devices.

**Table 6-6. Memory Organization**

| | | MSP430F67791<br>MSP430F67691<br>MSP430F67491 | MSP430F67781<br>MSP430F67681<br>MSP430F67481 | MSP430F67771<br>MSP430F67671<br>MSP430F67471 |
|---|---|---|---|---|
| Main memory (flash) | Total Size | 512KB | 512KB | 256KB |
| Main: interrupt vector | | 00FFFFh to 00FF80h | 00FFFFh to 00FF80h | 00FFFFh to 00FF80h |
| Main: code memory | Bank 3 | 128KB<br>08BFFFh to 06C000h | 128KB<br>08BFFFh to 06C000h | not available |
| | Bank 2 | 128KB<br>06BFFFh to 04C000h | 128KB<br>06BFFFh to 04C000h | not available |
| | Bank 1 | 128KB<br>04BFFFh to 02C000h | 128KB<br>04BFFFh to 02C000h | 128KB<br>04BFFFh to 02C000h |
| | Bank 0 | 128KB<br>02BFFFh to 00C000h | 128KB<br>02BFFFh to 00C000h | 128KB<br>02BFFFh to 00C000h |
| RAM | Total Size | 32KB | 16KB | 32KB |
| | Sector 7 | 4KB<br>009BFFh to 008C00h | not available | 4KB<br>009BFFh to 008C00h |
| | Sector 6 | 4KB<br>008BFFh to 007C00h | not available | 4KB<br>008BFFh to 007C00h |
| | Sector 5 | 4KB<br>007BFFh to 006C00h | not available | 4KB<br>007BFFh to 006C00h |
| | Sector 4 | 4KB<br>006BFFh to 005C00h | not available | 4KB<br>006BFFh to 005C00h |
| | Sector 3 | 4KB<br>005BFFh to 004C00h | 4KB<br>005BFFh to 004C00h | 4KB<br>005BFFh to 004C00h |
| | Sector 2 | 4KB<br>004BFFh to 003C00h | 4KB<br>004BFFh to 003C00h | 4KB<br>004BFFh to 003C00h |
| | Sector 1 | 4KB<br>003BFFh to 002C00h | 4KB<br>003BFFh to 002C00h | 4KB<br>003BFFh to 002C00h |
| | Sector 0 | 4KB<br>002BFFh to 001C00h | 4KB<br>002BFFh to 001C00h | 4KB<br>002BFFh to 001C00h |
| Device descriptor | | 128 B<br>001AFFh to 001A80h | 128 B<br>001AFFh to 001A80h | 128 B<br>001AFFh to 001A80h |
| | | 128 B<br>001A7Fh to 001A00h | 128 B<br>001A7Fh to 001A00h | 128 B<br>001A7Fh to 001A00h |
| Information memory (flash) | Info A | 128 B<br>0019FFh to 001980h | 128 B<br>0019FFh to 001980h | 128 B<br>0019FFh to 001980h |
| | Info B | 128 B<br>00197Fh to 001900h | 128 B<br>00197Fh to 001900h | 128 B<br>00197Fh to 001900h |
| | Info C | 128 B<br>0018FFh to 001880h | 128 B<br>0018FFh to 001880h | 128 B<br>0018FFh to 001880h |
| | Info D | 128 B<br>00187Fh to 001800h | 128 B<br>00187Fh to 001800h | 128 B<br>00187Fh to 001800h |
| Bootloader (BSL) memory (flash) | BSL 3 | 512 B<br>0017FFh to 001600h | 512 B<br>0017FFh to 001600h | 512 B<br>0017FFh to 001600h |
| | BSL 2 | 512 B<br>0015FFh to 001400h | 512 B<br>0015FFh to 001400h | 512 B<br>0015FFh to 001400h |
| | BSL 1 | 512 B<br>0013FFh to 001200h | 512 B<br>0013FFh to 001200h | 512 B<br>0013FFh to 001200h |
| | BSL 0 | 512 B<br>0011FFh to 001000h | 512 B<br>0011FFh to 001000h | 512 B<br>0011FFh to 001000h |
| Peripherals | | 4KB<br>000FFFh to 0h | 4KB<br>000FFFh to 0h | 4KB<br>000FFFh to 0h |


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**Table 6-7. Memory Organization**

| | | MSP430F67761<br>MSP430F67661<br>MSP430F67461 | MSP430F67751<br>MSP430F67651<br>MSP430F67451 |
|---|---|---|---|
| Main memory (flash) | Total Size | 256KB | 128KB |
| Main: interrupt vector | | 00FFFFh to 00FF80h | 00FFFFh to 00FF80h |
| Main: code memory | Bank 3 | not available | not available |
| | Bank 2 | not available | not available |
| | Bank 1 | 128KB<br>04BFFFh to 02C000h | not available |
| | Bank 0 | 128KB<br>02BFFFh to 00C000h | 128KB<br>02BFFFh to 00C000h |
| RAM | Total Size | 16KB | 16KB |
| | Sector 7 | not available | not available |
| | Sector 6 | not available | not available |
| | Sector 5 | not available | not available |
| | Sector 4 | not available | not available |
| | Sector 3 | 4KB<br>005BFFh to 004C00h | 4KB<br>005BFFh to 004C00h |
| | Sector 2 | 4KB<br>004BFFh to 003C00h | 4KB<br>004BFFh to 003C00h |
| | Sector 1 | 4KB<br>003BFFh to 002C00h | 4KB<br>003BFFh to 002C00h |
| | Sector 0 | 4KB<br>002BFFh to 001C00h | 4KB<br>002BFFh to 001C00h |
| Device descriptor | | 128 B<br>001AFFh to 001A80h | 128 B<br>001AFFh to 001A80h |
| | | 128 B<br>001A7Fh to 001A00h | 128 B<br>001A7Fh to 001A00h |
| Information memory (flash) | Info A | 128 B<br>0019FFh to 001980h | 128 B<br>0019FFh to 001980h |
| | Info B | 128 B<br>00197Fh to 001900h | 128 B<br>00197Fh to 001900h |
| | Info C | 128 B<br>0018FFh to 001880h | 128 B<br>0018FFh to 001880h |
| | Info D | 128 B<br>00187Fh to 001800h | 128 B<br>00187Fh to 001800h |
| Bootloader (BSL) memory (flash) | BSL 3 | 512 B<br>0017FFh to 001600h | 512 B<br>0017FFh to 001600h |
| | BSL 2 | 512 B<br>0015FFh to 001400h | 512 B<br>0015FFh to 001400h |
| | BSL 1 | 512 B<br>0013FFh to 001200h | 512 B<br>0013FFh to 001200h |
| | BSL 0 | 512 B<br>0011FFh to 001000h | 512 B<br>0011FFh to 001000h |
| Peripherals | | 4KB<br>000FFFh to 0h | 4KB<br>000FFFh to 0h |

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## 6.8 Bootloader (BSL)

The BSL lets users program the flash memory or RAM using various serial interfaces. Access to the device memory through the BSL is protected by an user-defined password. BSL entry requires a specific entry sequence on the $\overline{\text{RST}}$/NMI/SBWTDIO and TEST/SBWTCK pins. For a complete description of the features of the BSL and its implementation, see *MSP430™ Flash Device Bootloader (BSL) User's Guide*. Table 6-8 lists the BSL pin requirements.

**Table 6-8. UART BSL Pin Requirements and Functions**

| DEVICE SIGNAL | BSL FUNCTION |
|---|---|
| $\overline{\text{RST}}$/NMI/SBWTDIO | Entry sequence signal |
| TEST/SBWTCK | Entry sequence signal |
| P2.0 | Data transmit |
| P2.1 | Data receive |
| DVCC | Power supply |
| DVSS | Ground supply |

## 6.9 JTAG Operation

### 6.9.1 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RST}}$/NMI/SBWTDIO is required to interface with MSP430 development tools and device programmers. Table 6-9 lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*. For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming With the JTAG Interface*.

**Table 6-9. JTAG Pin Requirements and Functions**

| DEVICE SIGNAL | DIRECTION | FUNCTION |
|---|---|---|
| PJ.3/TCK | IN | JTAG clock input |
| PJ.2/TMS | IN | JTAG state control |
| PJ.1/TDI/TCLK | IN | JTAG data input, TCLK input |
| PJ.0/TDO | OUT | JTAG data output |
| TEST/SBWTCK | IN | Enable JTAG pins |
| $\overline{\text{RST}}$/NMI/SBWTDIO | IN | External reset |
| DVCC | | Power supply |
| DVSS | | Ground supply |


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### 6.9.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the 2-wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. Table 6-10 lists the Spy-Bi-Wire interface pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*. For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming With the JTAG Interface*.

**Table 6-10. Spy-Bi-Wire Pin Requirements and Functions**

| DEVICE SIGNAL | DIRECTION | FUNCTION |
|---|---|---|
| TEST/SBWTCK | IN | Spy-Bi-Wire clock input |
| $\overline{\text{RST}}$/NMI/SBWTDIO | IN, OUT | Spy-Bi-Wire data input and output |
| VCC | | Power supply |
| VSS | | Ground supply |

## 6.10 Flash Memory (Link to User's Guide)

The flash memory can be programmed through the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 128 bytes each. Each segment in main memory is 512 bytes.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n. Segments A to D are also called *information memory*.
- Segment A can be locked separately.

## 6.11 RAM (Link to User's Guide)

The RAM is made up of n sectors. Each sector can be completely powered down to save leakage; however, all data are lost. Features of the RAM include:

- RAM has n sectors of 4KB each.
- Each sector 0 to n can be completely disabled; however, data retention is lost.
- Each sector 0 to n automatically enters low-power retention mode when possible.

## 6.12 Backup RAM (Link to User's Guide)

The backup RAM provides a limited number of bytes of RAM that are retained during LPM3.5. This backup RAM is part of the backup subsystem that operates on dedicated power supply AUXVCC3. Eight bytes of backup RAM are available in this device. The backup RAM can be word-wise accessed through the registers BAKMEM0, BAKMEM1, BAKMEM2, and BAKMEM3. The backup RAM registers cannot be accessed by CPU when the high-side SVS is disabled by the user application.

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## 6.13 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. The peripherals can be managed using all instructions. For complete module descriptions, see the *MSP430x5xx and MSP430x6xx Family User's Guide*.

### 6.13.1 Oscillator and System Clock (Link to User's Guide)

The Unified Clock System (UCS) module includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), and an integrated internal digitally controlled oscillator (DCO). The UCS module is designed to meet the requirements of both low system cost and low power consumption. The UCS module features digital frequency-locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the selected FLL reference frequency. The internal DCO provides a fast turnon clock source and stabilizes in less than 5 µs. The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal, the internal low-frequency oscillator (VLO), or the trimmed low-frequency oscillator (REFO).
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

### 6.13.2 Power-Management Module (PMM) (Link to User's Guide)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry, as well as brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off. The SVS and SVM circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and core supply.

### 6.13.3 Auxiliary Supply System (Link to User's Guide)

The auxiliary supply system provides the option to operate the device from auxiliary supplies when the primary supply fails. Two auxiliary supplies (AUXVCC1 and AUXVCC2) are supported in the MSP430F67xx MCUs. The auxiliary supply system supports automatic and manual switching from primary supply to auxiliary supplies while maintaining full functionality. The auxiliary supply system allows threshold-based monitoring of primary and auxiliary supplies. The device can be started from primary supply or AUXVCC1, whichever is higher. Auxiliary supply system enables internal monitoring of voltage levels on primary and auxiliary supplies using ADC10_A. This module also implements a simple charger for backup capacitors.

### 6.13.4 Backup Subsystem

The backup subsystem operates on a dedicated power supply AUXVCC3. This subsystem includes a low-frequency oscillator, the RTC module, and backup RAM. The functionality of the backup subsystem is retained during LPM3.5. The backup subsystem module registers cannot be accessed by the CPU when the high-side SVS is disabled.


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### 6.13.5 Digital I/O (Link to User's Guide)

Up to eleven 8-bit I/O ports are implemented. For 128-pin options, ports P1 to P10 are complete, and port P11 is 6 bits wide. For 100-pin options, ports P1 to P7 are complete, port P8 is 2 bits wide, and ports P9, P10, and P11 are completely removed. Port PJ contains four individual I/O pins, common to all devices. All I/O bits are individually programmable.

- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Programmable drive strength on all ports.
- Edge-selectable interrupt and LPM3.5, LPM4.5 wake-up input capability available for all bits of ports P1 and P2.
- Read-write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise (P1 to P11) or word-wise in pairs (PA to PF).

### 6.13.6 Port Mapping Controller (Link to User's Guide)

The port mapping controller allows flexible and reconfigurable mapping of digital functions to ports P2, P3, and P4 (see Table 6-11). Table 6-12 lists the default settings for all pins that support port mapping.

**Table 6-11. Port Mapping Mnemonics and Functions**

| VALUE | PxMAPy MNEMONIC | INPUT PIN FUNCTION | OUTPUT PIN FUNCTION |
|---|---|---|---|
| 0 | PM_NONE | None | DVSS |
| 1 | PM_UCA0RXD | eUSCI_A0 UART RXD (direction controlled by eUSCI – Input) | |
| | PM_UCA0SOMI | eUSCI_A0 SPI slave out master in (direction controlled by eUSCI) | |
| 2 | PM_UCA0TXD | eUSCI_A0 UART TXD (direction controlled by eUSCI – Output) | |
| | PM_UCA0SIMO | eUSCI_A0 SPI slave in master out (direction controlled by eUSCI) | |
| 3 | PM_UCA0CLK | eUSCI_A0 clock input/output (direction controlled by eUSCI) | |
| 4 | PM_UCA0STE | eUSCI_A0 SPI slave transmit enable (direction controlled by eUSCI) | |
| 5 | PM_UCA1RXD | eUSCI_A1 UART RXD (direction controlled by eUSCI – Input) | |
| | PM_UCA1SOMI | eUSCI_A1 SPI slave out master in (direction controlled by eUSCI) | |
| 6 | PM_UCA1TXD | eUSCI_A1 UART TXD (direction controlled by eUSCI – Output) | |
| | PM_UCA1SIMO | eUSCI_A1 SPI slave in master out (direction controlled by eUSCI) | |
| 7 | PM_UCA1CLK | eUSCI_A1 clock input/output (direction controlled by eUSCI) | |
| 8 | PM_UCA1STE | eUSCI_A1 SPI slave transmit enable (direction controlled by eUSCI) | |
| 9 | PM_UCA2RXD | eUSCI_A2 UART RXD (direction controlled by eUSCI – Input) | |
| | PM_UCA2SOMI | eUSCI_A2 SPI slave out master in (direction controlled by eUSCI) | |
| 10 | PM_UCA2TXD | eUSCI_A2 UART TXD (direction controlled by eUSCI – Output) | |
| | PM_ UCA2SIMO | eUSCI_A2 SPI slave in master out (direction controlled by eUSCI) | |
| 11 | PM_UCA2CLK | eUSCI_A2 clock input/output (direction controlled by eUSCI) | |
| 12 | PM_UCA2STE | eUSCI_A2 SPI slave transmit enable (direction controlled by eUSCI) | |
| 13 | PM_UCA3RXD | eUSCI_A3 UART RXD (direction controlled by eUSCI – Input) | |
| | PM_UCA3SOMI | eUSCI_A3 SPI slave out master in (direction controlled by eUSCI) | |
| 14 | PM_UCA3TXD | eUSCI_A3 UART TXD (direction controlled by eUSCI – Output) | |
| | PM_ UCA3SIMO | eUSCI_A3 SPI slave in master out (direction controlled by eUSCI) | |
| 15 | PM_UCA3CLK | eUSCI_A3 clock input/output (direction controlled by eUSCI) | |
| 16 | PM_UCA3STE | eUSCI_A3 SPI slave transmit enable (direction controlled by eUSCI) | |
| 17 | PM_UCB0SIMO | eUSCI_B0 SPI slave in master out (direction controlled by eUSCI) | |
| | PM_UCB0SDA | eUSCI_B0 $I^2C$ data (open drain and direction controlled by eUSCI) | |
| 18 | PM_UCB0SOMI | eUSCI_B0 SPI slave out master in (direction controlled by eUSCI) | |
| | PM_UCB0SCL | eUSCI_B0 $I^2C$ clock (open drain and direction controlled by eUSCI) | |
| 19 | PM_UCB0CLK | eUSCI_B0 clock input/output (direction controlled by eUSCI) | |

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**Table 6-11. Port Mapping Mnemonics and Functions (continued)**

| VALUE | PxMAPy MNEMONIC | INPUT PIN FUNCTION | OUTPUT PIN FUNCTION |
|---|---|---|---|
| 20 | PM_UCB0STE | eUSCI_B0 SPI slave transmit enable (direction controlled by eUSCI) | |
| 21 | PM_UCB1SIMO | eUSCI_B1 SPI slave in master out (direction controlled by eUSCI) | |
| | PM_UCB1SDA | eUSCI_B1 $I^2C$ data (open drain and direction controlled by eUSCI) | |
| 22 | PM_UCB1SOMI | eUSCI_B1 SPI slave out master in (direction controlled by eUSCI) | |
| | PM_UCB1SCL | eUSCI_B1 $I^2C$ clock (open drain and direction controlled by eUSCI) | |
| 23 | PM_UCB1CLK | eUSCI_B1 clock input/output (direction controlled by eUSCI) | |
| 24 | PM_UCB1STE | eUSCI_B1 SPI slave transmit enable (direction controlled by eUSCI) | |
| 25 | PM_TA0.0 | TA0 CCR0 capture input CCI0A | TA0 CCR0 compare output Out0 |
| 26 | PM_TA0.1 | TA0 CCR1 capture input CCI1A | TA0 CCR1 compare output Out1 |
| 27 | PM_TA0.2 | TA0 CCR2 capture input CCI2A | TA0 CCR2 compare output Out2 |
| 28 | PM_TA1.0 | TA1 CCR0 capture input CCI0A | TA1 CCR0 compare output Out0 |
| 29 | PM_TA2.0 | TA2 CCR0 capture input CCI0A | TA2 CCR0 compare output Out0 |
| 30 | PM_TA3.0 | TA3 CCR0 capture input CCI0A | TA3 CCR0 compare output Out0 |
| 31(0FFh) (1) | PM_ANALOG | Disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. | |

(1) The value of the PM_ANALOG mnemonic is set to 0FFh. The port mapping registers are only 5 bits wide and the upper bits are ignored, which results in a read value of 31.

**Table 6-12. Default Port Mapping**

| PIN NAME | | PxMAPy MNEMONIC | INPUT PIN FUNCTION | OUTPUT PIN FUNCTION |
|---|---|---|---|---|
| PEU | PZ | | | |
| P2.0/PM_TA0.0 | P2.0/PM_TA0.0/COM4 | PM_TA0.0 | TA0 CCR0 capture input CCI0A | TA0 CCR0 compare output Out0 |
| P2.1/PM_TA0.1 | P2.1/PM_TA0.1/COM5 | PM_TA0.1 | TA0 CCR1 capture input CCI1A | TA0 CCR1 compare output Out1 |
| P2.2/PM_TA0.2 | P2.2/PM_TA0.2/COM6 | PM_TA0.2 | TA0 CCR2 capture input CCI2A | TA0 CCR2 compare output Out2 |
| P2.3/PM_TA1.0 | P2.3/PM_TA1.0/COM7 | PM_TA1.0 | TA1 CCR0 capture input CCI0A | TA1 CCR0 compare output Out0 |
| P2.4/PM_TA2.0 | P1.1/PM_TA2.0/R23 | PM_TA2.0 | TA2 CCR0 capture input CCI0A | TA2 CCR0 compare output Out0 |
| P2.5/PM_UCB0SOMI/ PM_UCB0SCL | P2.0/PM_UCB0SOMI/ PM_UCB0SCL/R13 | PM_UCB0SOMI / PM_UCB0SCL | eUSCI_B0 SPI slave out master in (direction controlled by eUSCI), eUSCI_B0 $I^2C$ clock (open drain and direction controlled by eUSCI) | |
| P2.6/PM_UCB0SIMO/ PM_UCB0SDA | P2.6/PM_UCB0SIMO/ PM_UCB0SDA/R03 | PM_UCB0SIMO / PM_UCB0SDA | eUSCI_B0 SPI slave in master out (direction controlled by eUSCI), eUSCI_B0 $I^2C$ data (open drain and direction controlled by eUSCI) | |
| P2.7/PM_UCB0CLK | P2.7/PM_UCB0CLK/CB2 | PM_UCB0CLK | eUSCI_B0 clock input/output (direction controlled by eUSCI) | |
| P3.0/PM_UCA0RXD/ PM_UCA0SOMI | P3.0/PM_UCA0RXD/ PM_UCA0SOMI | PM_UCA0RXD/ PM_UCA0SOMI | eUSCI_A0 UART RXD (direction controlled by eUSCI – input), eUSCI_A0 SPI slave out master in (direction controlled by eUSCI) | |
| P3.1/PM_UCA0TXD/ PM_UCA0SIMO | P3.1/PM_UCA0TXD/ PM_UCA0SIMO/S39 | PM_UCA0TXD/ PM_UCA0SIMO | eUSCI_A0 UART TXD (direction controlled by eUSCI – output), eUSCI_A0 SPI slave in master out (direction controlled by eUSCI) | |
| P3.2/PM_UCA0CLK | P3.2/PM_UCA0CLK/S38 | PM_UCA0CLK | eUSCI_A0 clock input/output (direction controlled by eUSCI) | |
| P3.3/PM_UCA1CLK | P3.3/PM_UCA1CLK/S37 | PM_UCA1CLK | eUSCI_A1 clock input/output (direction controlled by eUSCI) | |
| P3.4/PM_UCA1RXD/ PM_UCA1SOMI/ | P3.4/PM_UCA1RXD/ PM_UCA1SOMI/S36 | PM_UCA1RXD/ PM_UCA1SOMI | eUSCI_A1 UART RXD (direction controlled by eUSCI – input), eUSCI_A1 SPI slave out master in (direction controlled by eUSCI) | |
| P3.5/PM_UCA1TXD/ PM_UCA1SIMO | P3.5/PM_UCA1TXD/ PM_UCA1SIMO/S35 | PM_UCA1TXD/ PM_UCA1SIMO | eUSCI_A1 UART TXD (direction controlled by eUSCI – output), eUSCI_A1 SPI slave in master out (direction controlled by eUSCI) | |
| P3.6/PM_UCA2RXD/ PM_UCA2SOMI/ | P3.6/PM_UCA2RXD/ PM_UCA2SOMI/S34 | PM_UCA2RXD/ PM_UCA2SOMI | eUSCI_A2 UART RXD (direction controlled by eUSCI – input), eUSCI_A2 SPI slave out master in (direction controlled by eUSCI) | |
| P3.7/PM_UCA2TXD/ PM_UCA2SIMO | P3.7/PM_UCA2TXD/ PM_UCA2SIMO/S33 | PM_UCA2TXD/ PM_UCA2SIMO | eUSCI_A2 UART TXD (direction controlled by eUSCI – output), eUSCI_A2 SPI slave in master out (direction controlled by eUSCI) | |
| P4.0/PM_UCA2CLK | P4.0/PM_UCA2CLK/S32 | PM_UCA2CLK | eUSCI_A2 clock input/output (direction controlled by eUSCI) | |
| P4.1/PM_UCA3RXD/ PM_UCA3SOMI/ | P4.1/PM_UCA3RXD/ PM_UCA3SOMI/S31 | PM_UCA3RXD/ PM_UCA3SOMI | eUSCI_A3 UART RXD (direction controlled by eUSCI – input), eUSCI_A3 SPI slave out master in (direction controlled by eUSCI) | |
| P4.2/PM_UCA3TXD/ PM_UCA3SIMO | P4.2/PM_UCA3TXD/ PM_UCA3SIMO/S30 | PM_UCA3TXD/ PM_UCA3SIMO | eUSCI_A3 UART TXD (direction controlled by eUSCI – output), eUSCI_A3 SPI slave in master out (direction controlled by eUSCI) | |
| P4.3/PM_UCA3CLK | P4.3/PM_UCA3CLK/S29 | PM_UCA3CLK | eUSCI_A3 clock input/output (direction controlled by eUSCI) | |


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**Table 6-12. Default Port Mapping (continued)**

| PIN NAME | | PxMAPy MNEMONIC | INPUT PIN FUNCTION | OUTPUT PIN FUNCTION |
|---|---|---|---|---|
| PEU | PZ | | | |
| P4.4/PM_UCB1SOMI/ PM_UCB1SCL | P4.4/PM_UCB1SOMI/ PM_UCB1SCL/S28 | PM_UCB1SOMI / PM_UCB1SCL | eUSCI_B1 SPI slave out master in (direction controlled by eUSCI), eUSCI_B1 $I^2C$ clock (open drain and direction controlled by eUSCI) | |
| P4.5/PM_UCB1SIMO/ PM_UCB1SDA | P4.5/PM_UCB1SIMO/ PM_UCB1SDA/S27 | PM_UCB1SIMO / PM_UCB1SDA | eUSCI_B1 SPI slave in master out (direction controlled by eUSCI), eUSCI_B1 $I^2C$ data (open drain and direction controlled by eUSCI) | |
| P4.6/PM_UCB1CLK | P4.6/PM_UCB1CLK/S26 | PM_UCB1CLK | eUSCI_B1 clock input/output (direction controlled by eUSCI) | |
| P4.7/PM_TA3.0 | P4.7/PM_TA3.0/S25 | PM_TA3.0 | TA3 CCR0 capture input CCI0A | TA3 CCR0 compare output Out0 |

### 6.13.7 System Module (SYS) (Link to User's Guide)

The SYS module handles many of the system functions within the device. These include power-on reset (POR) and power-up clear (PUC) handling, NMI source selection and management, reset interrupt vector generators, bootloader entry mechanisms, and configuration management (device descriptors). The SYS module also includes a data exchange mechanism using JTAG called a JTAG mailbox that can be used in the application. Table 6-13 lists the SYS module interrupt vector registers.

**Table 6-13. System Module Interrupt Vector Registers**

| INTERRUPT VECTOR REGISTER | ADDRESS | INTERRUPT EVENT | VALUE | PRIORITY |
|---|---|---|---|---|
| SYSRSTIV, System Reset | 019Eh | No interrupt pending | 00h | |
| | | Brownout (BOR) | 02h | Highest |
| | | RST/NMI (POR) | 04h | |
| | | DoBOR (BOR) | 06h | |
| | | Wake up from LPMx.5 | 08h | |
| | | Security violation (BOR) | 0Ah | |
| | | SVSL (POR) | 0Ch | |
| | | SVSH (POR) | 0Eh | |
| | | SVML_OVP (POR) | 10h | |
| | | SVMH_OVP (POR) | 12h | |
| | | DoPOR (POR) | 14h | |
| | | WDT time-out (PUC) | 16h | |
| | | WDT key violation (PUC) | 18h | |
| | | KEYV flash key violation (PUC) | 1Ah | |
| | | Reserved | 1Ch | |
| | | Peripheral area fetch (PUC) | 1Eh | |
| | | PMM key violation (PUC) | 20h | |
| | | Reserved | 22h to 3Eh | Lowest |
| SYSSNIV, System NMI | 019Ch | No interrupt pending | 00h | |
| | | SVMLIFG | 02h | Highest |
| | | SVMHIFG | 04h | |
| | | DLYLIFG | 06h | |
| | | DLYHIFG | 08h | |
| | | VMAIFG | 0Ah | |
| | | JMBINIFG | 0Ch | |
| | | JMBOUTIFG | 0Eh | |
| | | VLRLIFG | 10h | |
| | | VLRHIFG | 12h | |
| | | Reserved | 14h to 1Eh | Lowest |

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**Table 6-13. System Module Interrupt Vector Registers (continued)**

| INTERRUPT VECTOR REGISTER | ADDRESS | INTERRUPT EVENT | VALUE | PRIORITY |
|---|---|---|---|---|
| SYSUNIV, User NMI | 019Ah | No interrupt pending | 00h | |
| | | NMIIFG | 02h | Highest |
| | | OFIFG | 04h | |
| | | ACCVIFG | 06h | |
| | | AUXSWGIFG | 08h | |
| | | Reserved | 0Ah to 1Eh | Lowest |

### 6.13.8 Watchdog Timer (WDT_A) (Link to User's Guide)

The primary function of the WDT_A is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the timer can be configured as an interval timer and can generate interrupts at selected time intervals.

### 6.13.9 DMA Controller (Link to User's Guide)

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can move data from the ADC10_A conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral. Table 6-14 lists the triggers that can start a DMA transfer.

**Table 6-14. DMA Trigger Assignments(1)**

| TRIGGER | CHANNEL | | |
|---|---|---|---|
| | 0 | 1 | 2 |
| 0 | DMAREQ | DMAREQ | DMAREQ |
| 1 | TA0CCR0 CCIFG | TA0CCR0 CCIFG | TA0CCR0 CCIFG |
| 2 | TA0CCR2 CCIFG | TA0CCR2 CCIFG | TA0CCR2 CCIFG |
| 3 | TA1CCR0 CCIFG | TA1CCR0 CCIFG | TA1CCR0 CCIFG |
| 4 | Reserved | Reserved | Reserved |
| 5 | TA2CCR0 CCIFG | TA2CCR0 CCIFG | TA2CCR0 CCIFG |
| 6 | Reserved | Reserved | Reserved |
| 7 | TA3CCR0 CCIFG | TA3CCR0 CCIFG | TA3CCR0 CCIFG |
| 8 | Reserved | Reserved | Reserved |
| 9 | Reserved | Reserved | Reserved |
| 10 | Reserved | Reserved | Reserved |
| 11 | Reserved | Reserved | Reserved |
| 12 | Reserved | Reserved | Reserved |
| 13 | SD24IFG | SD24IFG | SD24IFG |
| 14 | Reserved | Reserved | Reserved |
| 15 | Reserved | Reserved | Reserved |
| 16 | UCA0RXIFG | UCA0RXIFG | UCA0RXIFG |
| 17 | UCA0TXIFG | UCA0TXIFG | UCA0TXIFG |
| 18 | UCA1RXIFG | UCA1RXIFG | UCA1RXIFG |
| 19 | UCA1TXIFG | UCA1TXIFG | UCA1TXIFG |
| 20 | UCA2RXIFG | UCA2RXIFG | UCA2RXIFG |
| 21 | UCA2TXIFG | UCA2TXIFG | UCA2TXIFG |

(1) Reserved DMA triggers may be used by other devices in the family. Reserved DMA triggers do not cause any DMA trigger event when selected.


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**Table 6-14. DMA Trigger Assignments[1] (continued)**

| TRIGGER | CHANNEL | | |
|---|---|---|---|
| | 0 | 1 | 2 |
| 22 | UCB0RXIFG0 | UCB0RXIFG0 | UCB0RXIFG0 |
| 23 | UCB0TXIFG0 | UCB0TXIFG0 | UCB0TXIFG0 |
| 24 | ADC10IFG0 | ADC10IFG0 | ADC10IFG0 |
| 25 | UCA3RXIFG | UCA3RXIFG | UCA3RXIFG |
| 26 | UCA3TXIFG | UCA3TXIFG | UCA3TXIFG |
| 27 | UCB1RXIFG0 | UCB1RXIFG0 | UCB1RXIFG0 |
| 28 | UCB1TXIFG0 | UCB1TXIFG0 | UCB1TXIFG0 |
| 29 | MPY ready | MPY ready | MPY ready |
| 30 | DMA2IFG | DMA0IFG | DMA1IFG |
| 31 | Reserved | Reserved | Reserved |

### 6.13.10 CRC16 (Link to User's Guide)

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

### 6.13.11 Hardware Multiplier (Link to User's Guide)

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations.

### 6.13.12 Enhanced Universal Serial Communication Interface (eUSCI) (Links to User's Guide: UART Mode, SPI Mode, $I^2C$ Mode)

The eUSCI module is used for serial data communication. The eUSCI module supports synchronous communication protocols such as SPI (3- or 4-pin) and $I^2C$, and asynchronous communication protocols such as UART, enhanced UART with automatic baud-rate detection, and IrDA.

The eUSCI_An module provides support for SPI (3- or 4-pin), UART, enhanced UART, and IrDA.

The eUSCI_Bn module provides support for SPI (3- or 4-pin) and $I^2C$.

Four eUSCI_A and two eUSCI_B module are implemented in these devices.

### 6.13.13 ADC10_A (Link to User's Guide)

The ADC10_A module supports fast 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator, and a conversion results buffer. A window comparator with lower and upper limits allows CPU-independent result monitoring with three window comparator interrupt flags.

### 6.13.14 SD24_B (Link to User's Guide)

The SD24_B module integrates up to seven independent 24-bit sigma-delta analog-to-digital converters. Each converter is designed with a fully differential analog input pair and programmable gain amplifier input stage. Also the converters are based on second-order oversampling sigma-delta modulators and digital decimation filters. The decimation filters are comb filters with selectable oversampling ratios of up to 1024.

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### 6.13.15 TA0 (Link to User's Guide)

TA0 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. TA0 can support multiple capture/compares, PWM outputs, and interval timing (see Table 6-15). TA0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**Table 6-15. TA0 Signal Connections**

| DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---|---|---|---|---|
| PM_TACLK | TACLK | Timer | NA | NA |
| ACLK (internal) | ACLK | | | |
| SMCLK (internal) | SMCLK | | | |
| PM_TACLK | INCLK | | | |
| PM_TA0.0 | CCI0A | CCR0 | TA0 | PM_TA0.0 |
| CBOUT (internal) | CCI0B | | | |
| DVSS | GND | | | |
| DVCC | VCC | | | |
| PM_TA0.1 | CCI1A | CCR1 | TA1 | PM_TA0.1 |
| ACLK (internal) | CCI1B | | | ADC10_A (internal) ADC10SHSx = 001b |
| DVSS | GND | | | SD24_B (internal) SD24CHx.SD24SCSx = 001b |
| DVCC | VCC | | | |
| PM_TA0.2 | CCI2A | CCR2 | TA2 | PM_TA0.2 |
| DVSS | CCI2B | | | |
| DVSS | GND | | | |
| DVCC | VCC | | | |

### 6.13.16 TA1 (Link to User's Guide)

TA1 is a 16-bit timer/counter (Timer_A type) with two capture/compare registers. TA1 can support multiple capture/compares, PWM outputs, and interval timing (see Table 6-16). TA1 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**Table 6-16. TA1 Signal Connections**

| DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---|---|---|---|---|
| PM_TACLK | TACLK | Timer | NA | NA |
| ACLK (internal) | ACLK | | | |
| SMCLK (internal) | SMCLK | | | |
| PM_TACLK | INCLK | | | |
| PM_TA1.0 | CCI0A | CCR0 | TA0 | PM_TA1.0 |
| CBOUT (internal) | CCI0B | | | |
| DVSS | GND | | | |
| DVCC | VCC | | | |
| PM_TA1.1 | CCI1A | CCR1 | TA1 | PM_TA1.1 |
| ACLK (internal) | CCI1B | | | |
| DVSS | GND | | | |
| DVCC | VCC | | | |


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### 6.13.17 TA2 (Link to User's Guide)

TA2 is a 16-bit timer/counter (Timer_A type) with two capture/compare registers. TA2 can support multiple capture/compares, PWM outputs, and interval timing (see Table 6-17). TA2 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**Table 6-17. TA2 Signal Connections**

| DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---|---|---|---|---|
| PM_TACLK | TACLK | Timer | NA | NA |
| ACLK (internal) | ACLK | | | |
| SMCLK (internal) | SMCLK | | | |
| PM_TACLK | INCLK | | | |
| PM_TA2.0 | CCI0A | CCR0 | TA0 | PM_TA2.0 |
| CBOUT (internal) | CCI0B | | | |
| DVSS | GND | | | |
| DVCC | VCC | | | |
| PM_TA2.1 | CCI1A | CCR1 | TA1 | PM_TA2.1 |
| ACLK (internal) | CCI1B | | | SD24_B (internal) SD24CHx.SD24SCSx = 010b |
| DVSS | GND | | | |
| DVCC | VCC | | | |

### 6.13.18 TA3 (Link to User's Guide)

TA3 is a 16-bit timer/counter (Timer_A type) with two capture/compare registers. TA3 can support multiple capture/compares, PWM outputs, and interval timing (see Table 6-18). TA3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**Table 6-18. TA3 Signal Connections**

| DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---|---|---|---|---|
| PM_TACLK | TACLK | Timer | NA | |
| ACLK (internal) | ACLK | | | |
| SMCLK (internal) | SMCLK | | | |
| PM_TACLK | INCLK | | | |
| PM_TA3.0 | CCI0A | CCR0 | TA0 | PM_TA3.0 |
| CBOUT (internal) | CCI0B | | | ADC10_A (internal) ADC10SHSx = 010b |
| DVSS | GND | | | |
| DVCC | VCC | | | |
| PM_TA3.1 | CCI1A | CCR1 | TA1 | PM_TA3.1 |
| ACLK (internal) | CCI1B | | | SD24_B (internal) SD24CHx.SD24SCSx = 011b |
| DVSS | GND | | | |
| DVCC | VCC | | | |

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### 6.13.19 SD24_B Triggers

Table 6-19 lists the input trigger connections to SD24_B converters from Timer_A modules and output trigger pulse connection from SD24_B to ADC10_A.

**Table 6-19. SD24_B Input/Output Trigger Connections**

| DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---|---|---|---|---|
| TA0.1 (internal) | SD24_B SD24CHx.SD24SCSx = 001b | SD24_B | Trigger Pulse | ADC10_A (internal) ADC10SHSx = 011b |
| TA2.1 (internal) | SD24_B SD24CHx.SD24SCSx = 010b | | | |
| TA3.1 (internal) | SD24_B SD24CHx.SD24SCSx = 011b | | | |

### 6.13.20 ADC10_A Triggers

Table 6-20 lists the input trigger connections to ADC10_A from Timer_A modules and SD24_B.

**Table 6-20. ADC10_A Input Trigger Connections**

| DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK |
|---|---|---|
| TA0.1 (internal) | ADC10_A ADC10SHSx = 001b | ADC10_A |
| TA3.0 (internal) | ADC10_A ADC10SHSx = 010b | |
| SD24_B trigger pulse (internal) | ADC10_A ADC10SHSx = 011b | |

### 6.13.21 Real-Time Clock (RTC_C) *(Link to User's Guide)*

The RTC_C module can be configured for real-time clock (RTC) and calendar mode providing seconds, hours, day of week, day of month, month, and year. The RTC_C control and configuration registers are password protected to ensure clock integrity against runaway code. Calendar mode integrates an internal calendar that compensates for months with less than 31 days and includes leap year correction. The RTC_C also supports flexible alarm functions, offset calibration, temperature compensation and time capture on two external events. The RTC_C on this device operates on dedicated AUXVCC3 supply and supports operation in LPM3.5.

### 6.13.22 Reference Module (REF) Voltage Reference *(Link to User's Guide)*

The REF module generates all of the critical reference voltages that can be used by the various analog peripherals in the device. The analog peripherals include the ADC10_A, LCD_C, and SD24_B modules.

### 6.13.23 LCD_C *(Link to User's Guide)*

The LCD_C driver generates the segment and common signals required to drive a liquid crystal display (LCD). The LCD_C controller has dedicated data memories to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-mux, 3-mux, 4-mux, up to 8-mux LCDs are supported. The module can provide a LCD voltage independent of the supply voltage with its integrated charge pump. It is possible to control the level of the LCD voltage and thus contrast by software. The module also provides an automatic blinking capability for individual segments in static, 2-mux, 3-mux, and 4-mux modes.


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### 6.13.24 Comparator_B (Link to User's Guide)

The primary function of the Comparator_B module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

### 6.13.25 Embedded Emulation Module (EEM) (Link to User's Guide)

The EEM supports real-time in-system debugging. The L version of the EEM has the following features:

- Eight hardware triggers or breakpoints on memory access
- Two hardware triggers or breakpoints on CPU register write access
- Up to 10 hardware triggers that can be combined to form complex triggers or breakpoints
- Two cycle counters
- Sequencer
- State storage
- Clock control on module level

### 6.13.26 Peripheral File Map

Table 6-21 lists the base address and register offset addresses for all supported peripherals.

**Table 6-21. Peripherals**

| MODULE NAME | BASE ADDRESS | OFFSET ADDRESS RANGE |
|---|---|---|
| Special Functions (see Table 6-22) | 0100h | 000h to 01Fh |
| PMM (see Table 6-23) | 0120h | 000h to 01Fh |
| Flash Control (see Table 6-24) | 0140h | 000h to 00Fh |
| CRC16 (see Table 6-25) | 0150h | 000h to 007h |
| RAM Control (see Table 6-26) | 0158h | 000h to 001h |
| Watchdog (see Table 6-27) | 015Ch | 000h to 001h |
| UCS (see Table 6-28) | 0160h | 000h to 01Fh |
| SYS (see Table 6-29) | 0180h | 000h to 01Fh |
| Shared Reference (see Table 6-30) | 01B0h | 000h to 001h |
| Port Mapping Control (see Table 6-31) | 01C0h | 000h to 007h |
| Port Mapping Port P2 (see Table 6-32) | 01D0h | 000h to 007h |
| Port Mapping Port P3 (see Table 6-33) | 01D8h | 000h to 007h |
| Port Mapping Port P4 (see Table 6-34) | 01E0h | 000h to 007h |
| Port P1, P2 (see Table 6-35) | 0200h | 000h to 01Fh |
| Port P3, P4 (see Table 6-36) | 0220h | 000h to 00Bh |
| Port P5, P6 (see Table 6-37) | 0240h | 000h to 00Bh |
| Port P7, P8 (see Table 6-38) | 0260h | 000h to 00Bh |
| Port P9, P10 (see Table 6-39)<br>(Ports P9 and P10 not available in PZ package) | 0280h | 000h to 00Bh |
| Port P11 (see Table 6-40)<br>(Port P11 not available in PZ package) | 02A0h | 000h to 00Bh |
| Port PJ (see Table 6-41) | 0320h | 000h to 01Fh |
| Timer TA0 (see Table 6-42) | 0340h | 000h to 03Fh |
| Timer TA1 (see Table 6-43) | 0380h | 000h to 03Fh |
| Timer TA2 (see Table 6-44) | 0400h | 000h to 03Fh |
| Timer TA3 (see Table 6-45) | 0440h | 000h to 03Fh |
| Backup Memory (see Table 6-46) | 0480h | 000h to 00Fh |
| 32-Bit Hardware Multiplier (see Table 6-48) | 04C0h | 000h to 02Fh |

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**Table 6-21. Peripherals (continued)**

| MODULE NAME | BASE ADDRESS | OFFSET ADDRESS RANGE |
|---|---|---|
| DMA General Control (see Table 6-49) | 0500h | 000h to 00Fh |
| DMA Channel 0 (see Table 6-50) | 0500h | 010h to 01Fh |
| DMA Channel 1 (see Table 6-51) | 0500h | 020h to 02Fh |
| DMA Channel 2 (see Table 6-52) | 0500h | 030h to 03Fh |
| RTC_C (see Table 6-47) | 0C80h | 000h to 03Fh |
| eUSCI_A0 (see Table 6-53) | 05C0h | 000h to 01Fh |
| eUSCI_A1 (see Table 6-54) | 05E0h | 000h to 01Fh |
| eUSCI_A2 (see Table 6-55) | 0600h | 000h to 01Fh |
| eUSCI_A3 (see Table 6-56) | 0620h | 000h to 01Fh |
| eUSCI_B0 (see Table 6-57) | 0640h | 000h to 02Fh |
| eUSCI_B1 ( see Table 6-58 ) | 0680h | 000h to 02Fh |
| ADC10_A (see Table 6-59) | 0740h | 000h to 01Fh |
| SD24_B(see Table 6-60) | 0800h | 000h to 06Fh |
| Comparator_B (see Table 6-61 ) | 08C0h | 000h to 00Fh |
| Auxiliary Supply (see Table 6-62) | 09E0h | 000h to 01Fh |
| LCD_C (see Table 6-63) | 0A00h | 000h to 05Fh |


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**Table 6-22. Special Function Registers (Base Address: 0100h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| SFR interrupt enable | SFRIE1 | 00h |
| SFR interrupt flag | SFRIFG1 | 02h |
| SFR reset pin control | SFRRPCR | 04h |

**Table 6-23. PMM Registers (Base Address: 0120h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| PMM control 0 | PMMCTL0 | 00h |
| PMM control 1 | PMMCTL1 | 02h |
| SVS high-side control | SVSMHCTL | 04h |
| SVS low-side control | SVSMLCTL | 06h |
| PMM interrupt flags | PMMIFG | 0Ch |
| PMM interrupt enable | PMMIE | 0Eh |
| PMM power mode 5 control register 0 | PM5CTL0 | 10h |

**Table 6-24. Flash Control Registers (Base Address: 0140h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Flash control 1 | FCTL1 | 00h |
| Flash control 3 | FCTL3 | 04h |
| Flash control 4 | FCTL4 | 06h |

**Table 6-25. CRC16 Registers (Base Address: 0150h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| CRC data input | CRC16DI | 00h |
| CRC result | CRCINIRES | 04h |

**Table 6-26. RAM Control Registers (Base Address: 0158h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| RAM control 0 | RCCTL0 | 00h |

**Table 6-27. Watchdog Registers (Base Address: 015Ch)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Watchdog timer control | WDTCTL | 00h |

**Table 6-28. UCS Registers (Base Address: 0160h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| UCS control 0 | UCSCTL0 | 00h |
| UCS control 1 | UCSCTL1 | 02h |
| UCS control 2 | UCSCTL2 | 04h |
| UCS control 3 | UCSCTL3 | 06h |
| UCS control 4 | UCSCTL4 | 08h |
| UCS control 5 | UCSCTL5 | 0Ah |
| UCS control 6 | UCSCTL6 | 0Ch |
| UCS control 7 | UCSCTL7 | 0Eh |
| UCS control 8 | UCSCTL8 | 10h |

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**Table 6-29. SYS Registers (Base Address: 0180h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| System control | SYSCTL | 00h |
| Bootloader configuration area | SYSBSLC | 02h |
| JTAG mailbox control | SYSJMBC | 06h |
| JTAG mailbox input 0 | SYSJMBI0 | 08h |
| JTAG mailbox input 1 | SYSJMBI1 | 0Ah |
| JTAG mailbox output 0 | SYSJMBO0 | 0Ch |
| JTAG mailbox output 1 | SYSJMBO1 | 0Eh |
| Bus error vector generator | SYSBERRIV | 18h |
| User NMI vector generator | SYSUNIV | 1Ah |
| System NMI vector generator | SYSSNIV | 1Ch |
| Reset vector generator | SYSRSTIV | 1Eh |

**Table 6-30. Shared Reference Registers (Base Address: 01B0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Shared reference control | REFCTL | 00h |

**Table 6-31. Port Mapping Controller (Base Address: 01C0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port mapping password | PMAPPWD | 00h |
| Port mapping control | PMAPCTL | 02h |

**Table 6-32. Port Mapping for Port P2 (Base Address: 01D0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P2.0 mapping | P2MAP0 | 00h |
| Port P2.1 mapping | P2MAP1 | 01h |
| Port P2.2 mapping | P2MAP2 | 02h |
| Port P2.3 mapping | P2MAP3 | 03h |
| Port P2.4 mapping | P2MAP4 | 04h |
| Port P2.5 mapping | P2MAP5 | 05h |
| Port P2.6 mapping | P2MAP6 | 06h |
| Port P2.7 mapping | P2MAP7 | 07h |

**Table 6-33. Port Mapping for Port P3 (Base Address: 01D8h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P3.0 mapping | P3MAP0 | 00h |
| Port P3.1 mapping | P3MAP1 | 01h |
| Port P3.2 mapping | P3MAP2 | 02h |
| Port P3.3 mapping | P3MAP3 | 03h |
| Port P3.4 mapping | P3MAP4 | 04h |
| Port P3.5 mapping | P3MAP5 | 05h |
| Port P3.6 mapping | P3MAP6 | 06h |
| Port P3.7 mapping | P3MAP7 | 07h |


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**Table 6-34. Port Mapping for Port P4 (Base Address: 01E0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P4.0 mapping | P4MAP0 | 00h |
| Port P4.1 mapping | P4MAP1 | 01h |
| Port P4.2 mapping | P4MAP2 | 02h |
| Port P4.3 mapping | P4MAP3 | 03h |
| Port P4.4 mapping | P4MAP4 | 04h |
| Port P4.5 mapping | P4MAP5 | 05h |
| Port P4.6 mapping | P4MAP6 | 06h |
| Port P4.7 mapping | P4MAP7 | 07h |

**Table 6-35. Port P1, P2 Registers (Base Address: 0200h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P1 input | P1IN | 00h |
| Port P1 output | P1OUT | 02h |
| Port P1 direction | P1DIR | 04h |
| Port P1 resistor enable | P1REN | 06h |
| Port P1 drive strength | P1DS | 08h |
| Port P1 selection 0 | P1SEL0 | 0Ah |
| Port P1 selection 1 | P1SEL1 | 0Ch |
| Port P1 interrupt vector word | P1IV | 0Eh |
| Port P1 interrupt edge select | P1IES | 18h |
| Port P1 interrupt enable | P1IE | 1Ah |
| Port P1 interrupt flag | P1IFG | 1Ch |
| Port P2 input | P2IN | 01h |
| Port P2 output | P2OUT | 03h |
| Port P2 direction | P2DIR | 05h |
| Port P2 resistor enable | P2REN | 07h |
| Port P2 drive strength | P2DS | 09h |
| Port P2 selection 0 | P2SEL0 | 0Bh |
| Port P2 selection 1 (1) | P2SEL1 | 0Dh |
| Port P2 interrupt vector word | P2IV | 1Eh |
| Port P2 interrupt edge select | P2IES | 19h |
| Port P2 interrupt enable | P2IE | 1Bh |
| Port P2 interrupt flag | P2IFG | 1Dh |

(1) P2SEL1 is an empty control register to be consistent with P1SEL1 in 16-bit access.

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**Table 6-36. Port P3, P4 Registers (Base Address: 0220h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P3 input | P3IN | 00h |
| Port P3 output | P3OUT | 02h |
| Port P3 direction | P3DIR | 04h |
| Port P3 resistor enable | P3REN | 06h |
| Port P3 drive strength | P3DS | 08h |
| Port P3 selection 0 | P3SEL0 | 0Ah |
| Port P4 input | P4IN | 01h |
| Port P4 output | P4OUT | 03h |
| Port P4 direction | P4DIR | 05h |
| Port P4 resistor enable | P4REN | 07h |
| Port P4 drive strength | P4DS | 09h |
| Port P4 selection 0 | P4SEL0 | 0Bh |

**Table 6-37. Port P5, P6 Registers (Base Address: 0240h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P5 input | P5IN | 00h |
| Port P5 output | P5OUT | 02h |
| Port P5 direction | P5DIR | 04h |
| Port P5 resistor enable | P5REN | 06h |
| Port P5 drive strength | P5DS | 08h |
| Port P5 selection 0 | P5SEL0 | 0Ah |
| Port P5 selection 1 | P5SEL1 | 0Ch |
| Port P6 input | P6IN | 01h |
| Port P6 output | P6OUT | 03h |
| Port P6 direction | P6DIR | 05h |
| Port P6 resistor enable | P6REN | 07h |
| Port P6 drive strength | P6DS | 09h |
| Port P6 selection 0 | P6SEL0 | 0Bh |
| Port P6 selection 1 (1) | P6SEL1 | 0Dh |

(1) P6SEL1 is an empty control register to be consistent with P5SEL1 in 16-bit access.

**Table 6-38. Port P7, P8 Registers (Base Address: 0260h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P7 input | P7IN | 00h |
| Port P7 output | P7OUT | 02h |
| Port P7 direction | P7DIR | 04h |
| Port P7 resistor enable | P7REN | 06h |
| Port P7 drive strength | P7DS | 08h |
| Port P7 selection 0 | P7SEL0 | 0Ah |
| Port P8 input | P8IN | 01h |
| Port P8 output | P8OUT | 03h |
| Port P8 direction | P8DIR | 05h |
| Port P8 resistor enable | P8REN | 07h |
| Port P8 drive strength | P8DS | 09h |
| Port P8 selection 0 | P8SEL0 | 0Bh |


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**Table 6-39. Port P9, P10 Registers (Base Address: 0280h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P9 input | P9IN | 00h |
| Port P9 output | P9OUT | 02h |
| Port P9 direction | P9DIR | 04h |
| Port P9 resistor enable | P9REN | 06h |
| Port P9 drive strength | P9DS | 08h |
| Port P9 selection 0 | P9SEL0 | 0Ah |
| Port P10 input | P10IN | 01h |
| Port P10 output | P10OUT | 03h |
| Port P10 direction | P10DIR | 05h |
| Port P10 resistor enable | P10REN | 07h |
| Port P10 drive strength | P10DS | 09h |
| Port P10 selection 0 | P10SEL0 | 0Bh |

**Table 6-40. Port 11 Registers (Base Address: 02A0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P11 input | P11IN | 00h |
| Port P11 output | P11OUT | 02h |
| Port P11 direction | P11DIR | 04h |
| Port P11 resistor enable | P11REN | 06h |
| Port P11 drive strength | P11DS | 08h |
| Port P11 selection 0 | P11SEL0 | 0Ah |

**Table 6-41. Port J Registers (Base Address: 0320h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port PJ input | PJIN | 00h |
| Port PJ output | PJOUT | 02h |
| Port PJ direction | PJDIR | 04h |
| Port PJ resistor enable | PJREN | 06h |
| Port PJ drive strength | PJDS | 08h |
| Port PJ selection | PJSEL | 0Ah |

**Table 6-42. TA0 Registers (Base Address: 0340h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TA0 control | TA0CTL | 00h |
| Capture/compare control 0 | TA0CCTL0 | 02h |
| Capture/compare control 1 | TA0CCTL1 | 04h |
| Capture/compare control 2 | TA0CCTL2 | 06h |
| TA0 counter | TA0R | 10h |
| Capture/compare 0 | TA0CCR0 | 12h |
| Capture/compare 1 | TA0CCR1 | 14h |
| Capture/compare 2 | TA0CCR2 | 16h |
| TA0 expansion 0 | TA0EX0 | 20h |
| TA0 interrupt vector | TA0IV | 2Eh |

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**Table 6-43. TA1 Registers (Base Address: 0380h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TA1 control | TA1CTL | 00h |
| Capture/compare control 0 | TA1CCTL0 | 02h |
| Capture/compare control 1 | TA1CCTL1 | 04h |
| TA1 counter | TA1R | 10h |
| Capture/compare 0 | TA1CCR0 | 12h |
| Capture/compare 1 | TA1CCR1 | 14h |
| TA1 expansion 0 | TA1EX0 | 20h |
| TA1 interrupt vector | TA1IV | 2Eh |

**Table 6-44. TA2 Registers (Base Address: 0400h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TA2 control | TA2CTL | 00h |
| Capture/compare control 0 | TA2CCTL0 | 02h |
| Capture/compare control 1 | TA2CCTL1 | 04h |
| TA2 counter | TA2R | 10h |
| Capture/compare 0 | TA2CCR0 | 12h |
| Capture/compare 1 | TA2CCR1 | 14h |
| TA2 expansion 0 | TA2EX0 | 20h |
| TA2 interrupt vector | TA2IV | 2Eh |

**Table 6-45. TA3 Registers (Base Address: 0440h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TA3 control | TA3CTL | 00h |
| Capture/compare control 0 | TA3CCTL0 | 02h |
| Capture/compare control 1 | TA3CCTL1 | 04h |
| TA3 counter | TA3R | 10h |
| Capture/compare 0 | TA3CCR0 | 12h |
| Capture/compare 1 | TA3CCR1 | 14h |
| TA3 expansion 0 | TA3EX0 | 20h |
| TA3 interrupt vector | TA3IV | 2Eh |

**Table 6-46. Backup Memory Registers (Base Address: 0480h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Backup memory 0 | BAKMEM0 | 00h |
| Backup memory 1 | BAKMEM1 | 02h |
| Backup memory 2 | BAKMEM2 | 04h |
| Backup memory 3 | BAKMEM3 | 06h |


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**Table 6-47. RTC_C Registers (Base Address: 0C80h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| RTC control 0 | RTCCTL0 | 00h |
| RTC password | RTCPWD | 01h |
| RTC control 1 | RTCCTL1 | 02h |
| RTC control 3 | RTCCTL3 | 03h |
| RTC offset calibration | RTCOCAL | 04h |
| RTC temperature compensation | RTCTCMP | 06h |
| RTC prescaler 0 control | RTCPS0CTL | 08h |
| RTC prescaler 1 control | RTCPS1CTL | 0Ah |
| RTC prescaler 0 | RTCPS0 | 0Ch |
| RTC prescaler 1 | RTCPS1 | 0Dh |
| RTC interrupt vector word | RTCIV | 0Eh |
| RTC seconds | RTCSEC | 10h |
| RTC minutes | RTCMIN | 11h |
| RTC hours | RTCHOUR | 12h |
| RTC day of week | RTCDOW | 13h |
| RTC days | RTCDAY | 14h |
| RTC month | RTCMON | 15h |
| RTC year | RTCYEAR | 16h |
| RTC alarm minutes | RTCAMIN | 18h |
| RTC alarm hours | RTCAHOUR | 19h |
| RTC alarm day of week | RTCADOW | 1Ah |
| RTC alarm days | RTCADAY | 1Bh |
| Binary-to-BCD conversion | BIN2BCD | 1Ch |
| BCD-to-Binary conversion | BCD2BIN | 1Eh |
| Real-Time Clock Time Capture Control Register | RTCTCCTL | 20h |
| Tamper Detect Pin 0 Control Register | RTCCAP0CTL | 21h |
| Tamper Detect Pin 1 Control Register | RTCCAP1CTL | 22h |
| RTC seconds Backup Register 0 | RTCSECBAK0 | 30h |
| RTC minutes Backup Register 0 | RTCMINBAK0 | 31h |
| RTC hours Backup Register 0 | RTCHOURBAK0 | 32h |
| RTC days Backup Register 0 | RTCDAYBAK0 | 33h |
| RTC month Backup Register 0 | RTCMONBAK0 | 34h |
| RTC year Backup Register 0 | RTCYEARBAK0 | 36h |
| RTC seconds Backup Register 1 | RTCSECBAK1 | 38h |
| RTC minutes Backup Register 1 | RTCMINBAK1 | 39h |
| RTC hours Backup Register 1 | RTCHOURBAK1 | 3Ah |
| RTC days Backup Register 1 | RTCDAYBAK1 | 3Bh |
| RTC month Backup Register 1 | RTCMONBAK1 | 3Ch |
| RTC year Backup Register 1 | RTCYEARBAK1 | 3Eh |

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**Table 6-48. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| 16-bit operand 1 – multiply | MPY | 00h |
| 16-bit operand 1 – signed multiply | MPYS | 02h |
| 16-bit operand 1 – multiply accumulate | MAC | 04h |
| 16-bit operand 1 – signed multiply accumulate | MACS | 06h |
| 16-bit operand 2 | OP2 | 08h |
| 16 × 16 result low word | RESLO | 0Ah |
| 16 × 16 result high word | RESHI | 0Ch |
| 16 × 16 sum extension | SUMEXT | 0Eh |
| 32-bit operand 1 – multiply low word | MPY32L | 10h |
| 32-bit operand 1 – multiply high word | MPY32H | 12h |
| 32-bit operand 1 – signed multiply low word | MPYS32L | 14h |
| 32-bit operand 1 – signed multiply high word | MPYS32H | 16h |
| 32-bit operand 1 – multiply accumulate low word | MAC32L | 18h |
| 32-bit operand 1 – multiply accumulate high word | MAC32H | 1Ah |
| 32-bit operand 1 – signed multiply accumulate low word | MACS32L | 1Ch |
| 32-bit operand 1 – signed multiply accumulate high word | MACS32H | 1Eh |
| 32-bit operand 2 – low word | OP2L | 20h |
| 32-bit operand 2 – high word | OP2H | 22h |
| 32 × 32 result 0 – least significant word | RES0 | 24h |
| 32 × 32 result 1 | RES1 | 26h |
| 32 × 32 result 2 | RES2 | 28h |
| 32 × 32 result 3 – most significant word | RES3 | 2Ah |
| MPY32 control 0 | MPY32CTL0 | 2Ch |

**Table 6-49. DMA General Control Registers (Base Address: 0500h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| DMA module control 0 | DMACTL0 | 00h |
| DMA module control 1 | DMACTL1 | 02h |
| DMA module control 2 | DMACTL2 | 04h |
| DMA module control 3 | DMACTL3 | 06h |
| DMA module control 4 | DMACTL4 | 08h |
| DMA interrupt vector | DMAIV | 0Eh |

**Table 6-50. DMA Channel 0 Registers (Base Address: 0500h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| DMA channel 0 control | DMA0CTL | 10h |
| DMA channel 0 source address low | DMA0SAL | 12h |
| DMA channel 0 source address high | DMA0SAH | 14h |
| DMA channel 0 destination address low | DMA0DAL | 16h |
| DMA channel 0 destination address high | DMA0DAH | 18h |
| DMA channel 0 transfer size | DMA0SZ | 1Ah |


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**Table 6-51. DMA Channel 1 Registers (Base Address: 0500h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| DMA channel 1 control | DMA1CTL | 20h |
| DMA channel 1 source address low | DMA1SAL | 22h |
| DMA channel 1 source address high | DMA1SAH | 24h |
| DMA channel 1 destination address low | DMA1DAL | 26h |
| DMA channel 1 destination address high | DMA1DAH | 28h |
| DMA channel 1 transfer size | DMA1SZ | 2Ah |

**Table 6-52. DMA Channel 2 Registers (Base Address: 0500h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| DMA channel 2 control | DMA2CTL | 30h |
| DMA channel 2 source address low | DMA2SAL | 32h |
| DMA channel 2 source address high | DMA2SAH | 34h |
| DMA channel 2 destination address low | DMA2DAL | 36h |
| DMA channel 2 destination address high | DMA2DAH | 38h |
| DMA channel 2 transfer size | DMA2SZ | 3Ah |

**Table 6-53. eUSCI_A0 Registers (Base Address: 05C0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| USCI_A control word 0 | UCA0CTLW0 | 00h |
| USCI _A control word 1 | UCA0CTLW1 | 02h |
| USCI_A baud rate 0 | UCA0BR0 | 06h |
| USCI_A baud rate 1 | UCA0BR1 | 07h |
| USCI_A modulation control | UCA0MCTLW | 08h |
| USCI_A status | UCA0STAT | 0Ah |
| USCI_A receive buffer | UCA0RXBUF | 0Ch |
| USCI_A transmit buffer | UCA0TXBUF | 0Eh |
| USCI_A LIN control | UCA0ABCTL | 10h |
| USCI_A IrDA transmit control | UCA0IRTCTL | 12h |
| USCI_A IrDA receive control | UCA0IRRCTL | 13h |
| USCI_A interrupt enable | UCA0IE | 1Ah |
| USCI_A interrupt flags | UCA0IFG | 1Ch |
| USCI_A interrupt vector word | UCA0IV | 1Eh |

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**Table 6-54. eUSCI_A1 Registers (Base Address:05E0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| USCI_A control word 0 | UCA1CTLW0 | 00h |
| USCI _A control word 1 | UCA1CTLW1 | 02h |
| USCI_A baud rate 0 | UCA1BR0 | 06h |
| USCI_A baud rate 1 | UCA1BR1 | 07h |
| USCI_A modulation control | UCA1MCTLW | 08h |
| USCI_A status | UCA1STAT | 0Ah |
| USCI_A receive buffer | UCA1RXBUF | 0Ch |
| USCI_A transmit buffer | UCA1TXBUF | 0Eh |
| USCI_A LIN control | UCA1ABCTL | 10h |
| USCI_A IrDA transmit control | UCA1IRTCTL | 12h |
| USCI_A IrDA receive control | UCA1IRRCTL | 13h |
| USCI_A interrupt enable | UCA1IE | 1Ah |
| USCI_A interrupt flags | UCA1IFG | 1Ch |
| USCI_A interrupt vector word | UCA1IV | 1Eh |

**Table 6-55. eUSCI_A2 Registers (Base Address:0600h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| USCI_A control word 0 | UCA2CTLW0 | 00h |
| USCI _A control word 1 | UCA2CTLW1 | 02h |
| USCI_A baud rate 0 | UCA2BR0 | 06h |
| USCI_A baud rate 1 | UCA2BR1 | 07h |
| USCI_A modulation control | UCA2MCTLW | 08h |
| USCI_A status | UCA2STAT | 0Ah |
| USCI_A receive buffer | UCA2RXBUF | 0Ch |
| USCI_A transmit buffer | UCA2TXBUF | 0Eh |
| USCI_A LIN control | UCA2ABCTL | 10h |
| USCI_A IrDA transmit control | UCA2IRTCTL | 12h |
| USCI_A IrDA receive control | UCA2IRRCTL | 13h |
| USCI_A interrupt enable | UCA2IE | 1Ah |
| USCI_A interrupt flags | UCA2IFG | 1Ch |
| USCI_A interrupt vector word | UCA2IV | 1Eh |


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**Table 6-56. eUSCI_A3 Registers (Base Address: 0620h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| USCI_A control word 0 | UCA3CTLW0 | 00h |
| USCI _A control word 1 | UCA3CTLW1 | 02h |
| USCI_A baud rate 0 | UCA3BR0 | 06h |
| USCI_A baud rate 1 | UCA3BR1 | 07h |
| USCI_A modulation control | UCA3MCTLW | 08h |
| USCI_A status | UCA3STAT | 0Ah |
| USCI_A receive buffer | UCA3RXBUF | 0Ch |
| USCI_A transmit buffer | UCA3TXBUF | 0Eh |
| USCI_A LIN control | UCA3ABCTL | 10h |
| USCI_A IrDA transmit control | UCA3IRTCTL | 12h |
| USCI_A IrDA receive control | UCA3IRRCTL | 13h |
| USCI_A interrupt enable | UCA3IE | 1Ah |
| USCI_A interrupt flags | UCA3IFG | 1Ch |
| USCI_A interrupt vector word | UCA3IV | 1Eh |

**Table 6-57. eUSCI_B0 Registers (Base Address: 0640h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| USCI_B control word 0 | UCB0CTLW0 | 00h |
| USCI_B control word 1 | UCB0CTLW1 | 02h |
| USCI_B bit rate 0 | UCB0BR0 | 06h |
| USCI_B bit rate 1 | UCB0BR1 | 07h |
| USCI_B status word | UCB0STATW | 08h |
| USCI_B byte counter threshold | UCB0TBCNT | 0Ah |
| USCI_B receive buffer | UCB0RXBUF | 0Ch |
| USCI_B transmit buffer | UCB0TXBUF | 0Eh |
| USCI_B I2C own address 0 | UCB0I2COA0 | 14h |
| USCI_B I2C own address 1 | UCB0I2COA1 | 16h |
| USCI_B I2C own address 2 | UCB0I2COA2 | 18h |
| USCI_B I2C own address 3 | UCB0I2COA3 | 1Ah |
| USCI_B received address | UCB0ADDRX | 1Ch |
| USCI_B address mask | UCB0ADDMASK | 1Eh |
| USCI I2C slave address | UCB0I2CSA | 20h |
| USCI interrupt enable | UCB0IE | 2Ah |
| USCI interrupt flags | UCB0IFG | 2Ch |
| USCI interrupt vector word | UCB0IV | 2Eh |

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**Table 6-58. eUSCI_B1 Registers (Base Address: 0680h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| USCI_B control word 0 | UCB1CTLW0 | 00h |
| USCI_B control word 1 | UCB1CTLW1 | 02h |
| USCI_B bit rate 0 | UCB1BR0 | 06h |
| USCI_B bit rate 1 | UCB1BR1 | 07h |
| USCI_B status word | UCB1STATW | 08h |
| USCI_B byte counter threshold | UCB1TBCNT | 0Ah |
| USCI_B receive buffer | UCB1RXBUF | 0Ch |
| USCI_B transmit buffer | UCB1TXBUF | 0Eh |
| USCI_B I2C own address 0 | UCB1I2COA0 | 14h |
| USCI_B I2C own address 1 | UCB1I2COA1 | 16h |
| USCI_B I2C own address 2 | UCB1I2COA2 | 18h |
| USCI_B I2C own address 3 | UCB1I2COA3 | 1Ah |
| USCI_B received address | UCB1ADDRX | 1Ch |
| USCI_B address mask | UCB1ADDMASK | 1Eh |
| USCI I2C slave address | UCB1I2CSA | 20h |
| USCI interrupt enable | UCB1IE | 2Ah |
| USCI interrupt flags | UCB1IFG | 2Ch |
| USCI interrupt vector word | UCB1IV | 2Eh |

**Table 6-59. ADC10_A Registers (Base Address: 0740h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| ADC10_A control 0 | ADC10CTL0 | 00h |
| ADC10_A control 1 | ADC10CTL1 | 02h |
| ADC10_A control 2 | ADC10CTL2 | 04h |
| ADC10_A window comparator low threshold | ADC10LO | 06h |
| ADC10_A window comparator high threshold | ADC10HI | 08h |
| ADC10_A memory control 0 | ADC10MCTL0 | 0Ah |
| ADC10_A conversion memory | ADC10MCTL0 | 12h |
| ADC10_A interrupt enable | ADC10IE | 1Ah |
| ADC10_A interrupt flags | ADC10IGH | 1Ch |
| ADC10_A interrupt vector word | ADC10IV | 1Eh |


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**Table 6-60. SD24_B Registers (Base Address: 0800h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| SD24_B control 0 | SD24BCTL0 | 00h |
| SD24_B control 1 | SD24BCTL1 | 02h |
| SD24_B trigger control | SD24BTRGCTL | 04h |
| SD24_B trigger OSR control | SD24BTRGOSR | 06h |
| SD24_B trigger preload | SD24BTRGPRE | 08h |
| SD24_B interrupt flag | SD24BIFG | 0Ah |
| SD24_B interrupt enable | SD24BIE | 0Ch |
| SD24_B interrupt vector | SD24BIV | 0Eh |
| SD24_B converter 0 control | SD24BCCTL0 | 10h |
| SD24_B converter 0 input control | SD24BINCTL0 | 12h |
| SD24_B converter 0 OSR control | SD24BOSR0 | 14h |
| SD24_B converter 0 preload | SD24BPRE0 | 16h |
| SD24_B converter 1 control | SD24BCCTL1 | 18h |
| SD24_B converter 1 input control | SD24BINCTL1 | 1Ah |
| SD24_B converter 1 OSR control | SD24BOSR1 | 1Ch |
| SD24_B converter 1 preload | SD24BPRE1 | 1Eh |
| SD24_B converter 2 control | SD24BCCTL2 | 20h |
| SD24_B converter 2 input control | SD24BINCTL2 | 22h |
| SD24_B converter 2 OSR control | SD24BOSR2 | 24h |
| SD24_B converter 2 preload | SD24BPRE2 | 26h |
| SD24_B converter 3 control | SD24BCCTL3 | 28h |
| SD24_B converter 3 input control | SD24BINCTL3 | 2Ah |
| SD24_B converter 3 OSR control | SD24BOSR3 | 2Ch |
| SD24_B converter 3 preload | SD24BPRE3 | 2Eh |
| SD24_B converter 4 control | SD24BCCTL4 | 30h |
| SD24_B converter 4 input control | SD24BINCTL4 | 32h |
| SD24_B converter 4 OSR control | SD24BOSR4 | 34h |
| SD24_B converter 4 preload | SD24BPRE4 | 36h |
| SD24_B converter 5 control | SD24BCCTL5 | 38h |
| SD24_B converter 5 input control | SD24BINCTL5 | 3Ah |
| SD24_B converter 5 OSR control | SD24BOSR5 | 3Ch |
| SD24_B converter 5 preload | SD24BPRE5 | 3Eh |
| SD24_B converter 6 control | SD24BCCTL6 | 40h |
| SD24_B converter 6 input control | SD24BINCTL6 | 42h |
| SD24_B converter 6 OSR control | SD24BOSR6 | 44h |
| SD24_B converter 6 preload | SD24BPRE6 | 46h |
| SD24_B converter 0 conversion memory low word | SD24BMEML0 | 50h |
| SD24_B converter 0 conversion memory high word | SD24BMEMH0 | 52h |
| SD24_B converter 1 conversion memory low word | SD24BMEML1 | 54h |
| SD24_B converter 1 conversion memory high word | SD24BMEMH1 | 56h |
| SD24_B converter 2 conversion memory low word | SD24BMEML2 | 58h |
| SD24_B converter 2 conversion memory high word | SD24BMEMH2 | 5Ah |
| SD24_B converter 3 conversion memory low word | SD24BMEML3 | 5Ch |
| SD24_B converter 3 conversion memory high word | SD24BMEMH3 | 5Eh |
| SD24_B converter 4 conversion memory low word | SD24BMEML4 | 60h |
| SD24_B converter 4 conversion memory high word | SD24BMEMH4 | 62h |
| SD24_B converter 5 conversion memory low word | SD24BMEML5 | 64h |

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**Table 6-60. SD24_B Registers (Base Address: 0800h) (continued)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| SD24_B converter 5 conversion memory high word | SD24BMEMH5 | 66h |
| SD24_B converter 6 conversion memory low word | SD24BMEML6 | 68h |
| SD24_B converter 6 conversion memory high word | SD24BMEMH6 | 6Ah |

**Table 6-61. Comparator_B Register (Base Address: 08C0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Comp_B control 0 | CBCTL0 | 00h |
| Comp_B control 1 | CBCTL1 | 02h |
| Comp_B control 2 | CBCTL2 | 04h |
| Comp_B control 3 | CBCTL3 | 06h |
| Comp_B interrupt | CBINT | 0Ch |
| Comp_B interrupt vector word | CBIV | 0Eh |

**Table 6-62. Auxiliary Supply Registers (Base Address: 09E0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Auxiliary supply control 0 | AUXCTL0 | 00h |
| Auxiliary supply control 1 | AUXCTL1 | 02h |
| Auxiliary supply control 2 | AUXCTL2 | 04h |
| AUX2 charger control | AUX2CHCTL | 12h |
| AUX3 charger control | AUX3CHCTL | 14h |
| AUX ADC control | AUXADCCTL | 16h |
| AUX interrupt flag | AUXIFG | 1Ah |
| AUX interrupt enable | AUXIE | 1Ch |
| AUX interrupt vector word | AUXIV | 1Eh |


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**Table 6-63. LCD_C Registers (Base Address: 0A00h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| LCD_C control 0 | LCDCCTL0 | 000h |
| LCD_C control 1 | LCDCCTL1 | 002h |
| LCD_C blinking control | LCDCBLKCTL | 004h |
| LCD_C memory control | LCDCMEMCTL | 006h |
| LCD_C voltage control | LCDCVCTL | 008h |
| LCD_C port control 0 | LCDCPCTL0 | 00Ah |
| LCD_C port control 1 | LCDCPCTL1 | 00Ch |
| LCD_C port control 2 | LCDCPCTL2 | 00Eh |
| LCD_C charge pump control | LCDCCPCTL | 012h |
| LCD_C interrupt vector | LCDCIV | 01Eh |
| **Static and 2 to 4 mux modes** | | |
| LCD_C memory 1 | LCDM1 | 020h |
| LCD_C memory 2 | LCDM2 | 021h |
| ⋮ | ⋮ | ⋮ |
| LCD_C memory 20 | LCDM20 | 033h |
| LCD_C blinking memory 1 | LCDBM1 | 040h |
| LCD_C blinking memory 2 | LCDBM2 | 041h |
| ⋮ | ⋮ | ⋮ |
| LCD_C blinking memory 20 | LCDBM20 | 053h |
| **5 to 8 mux modes** | | |
| LCD_C memory 1 | LCDM1 | 020h |
| LCD_C memory 2 | LCDM2 | 021h |
| ⋮ | ⋮ | ⋮ |
| LCD_C memory 40 | LCDM40 | 047h |

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## 6.14 Input/Output Diagrams

### 6.14.1 Port P1 (P1.0 to P1.3) Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

Figure 6-6 shows the port diagram. Table 6-64 summarizes the selection of the pin functions.

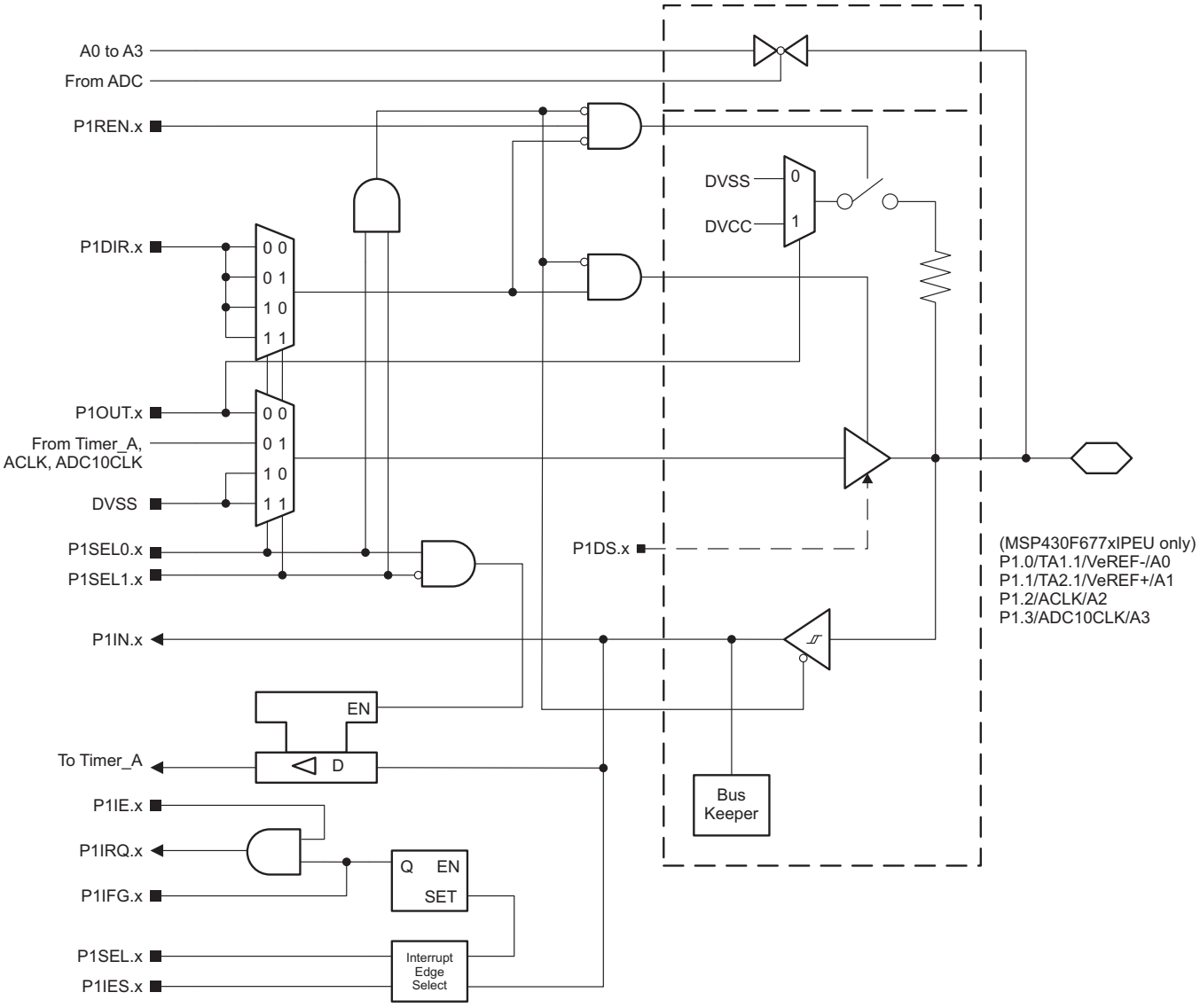



**Figure 6-6. Port P1 (P1.0 to P1.3) Diagram (MSP430F677xIPEU Only)**


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**Table 6-64. Port P1 (P1.0 to P1.3) Pin Functions (MSP430F677xIPEU Only)**

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P1DIR.x | P1SEL1.x | P1SEL0.x |
| P1.0/TA1.1/VeREF-/A0 | 0 | P1.0 (I/O) | I:0; O:1 | 0 | 0 |
| | | TA1.CCI1A | 0 | 0 | 1 |
| | | TA1.1 | 1 | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | VeREF-/A0 | X | 1 | 1 |
| P1.1/TA2.1/VeREF+/A1 | 1 | P1.1 (I/O) | I:0; O:1 | 0 | 0 |
| | | TA2.CCI1A | 0 | 0 | 1 |
| | | TA2.1 | 1 | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | VeREF+/A1 | X | 1 | 1 |
| P1.2/ACLK/A2 | 2 | P1.2 (I/O) | I:0; O:1 | 0 | 0 |
| | | ACLK | 1 | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | A2 | X | 1 | 1 |
| P1.3/ADC10CLK/A3 | 3 | P1.3 (I/O) | I:0; O:1 | 0 | 0 |
| | | ADC10CLK | 1 | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | A3 | X | 1 | 1 |

(1) X = don't care

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### 6.14.2 Port P1 (P1.0 to P1.3) Input/Output With Schmitt Trigger (MSP430F677xIPZ Only)

Figure 6-7 shows the port diagram. Table 6-65 summarizes the selection of the pin functions.

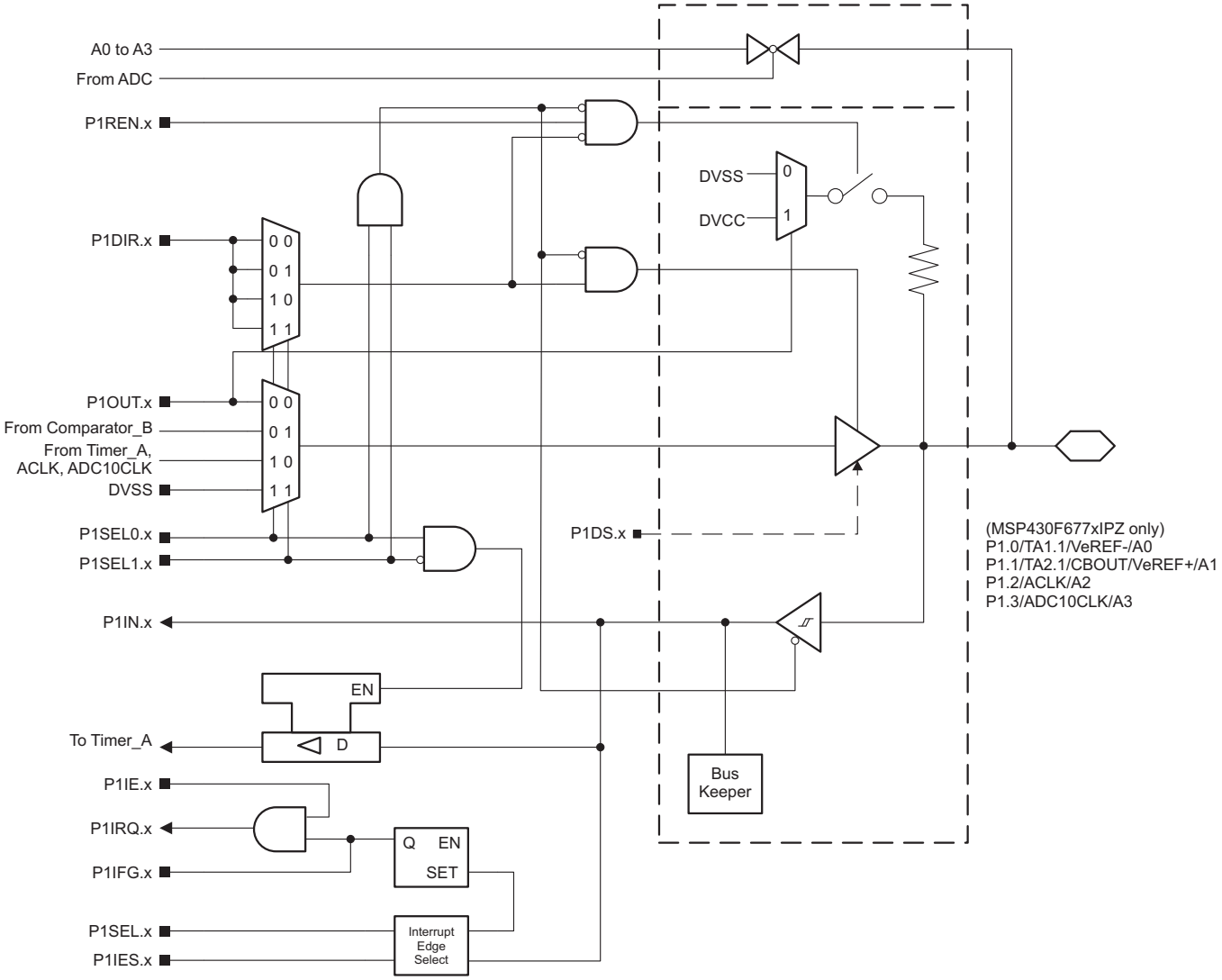



**Figure 6-7. Port P1 (P1.0 to P1.3) Diagram (MSP430F677xIPZ Only)**


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**Table 6-65. Port P1 (P1.0 to P1.3) Pin Functions (MSP430F677xIPZ Only)**

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P1DIR.x | P1SEL1.x | P1SEL0.x |
| P1.0/TA1.1/VeREF-/A0 | 0 | P1.0 (I/O) | I:0; O:1 | 0 | 0 |
| | | TA1.CCI1A | 0 | 0 | 1 |
| | | TA1.1 | 1 | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | VeREF-/A0 | X | 1 | 1 |
| P1.1/TA2.1/CBOUT/VeREF+/A1 | 1 | P1.1 (I/O) | I:0; O:1 | 0 | 0 |
| | | TA2.CCI1A | 0 | 0 | 1 |
| | | TA2.1 | 1 | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | CBOUT | 1 | 1 | 0 |
| | | VeREF+/A1 | X | 1 | 1 |
| P1.2/ACLK/A2 | 2 | P1.2 (I/O) | I:0; O:1 | 0 | 0 |
| | | ACLK | 1 | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | A2 | X | 1 | 1 |
| P1.3/ADC10CLK/A3 | 3 | P1.3 (I/O) | I:0; O:1 | 0 | 0 |
| | | ADC10CLK | 1 | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | A3 | X | 1 | 1 |

(1) X = don't care

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### 6.14.3 Port P1 (P1.4 and P1.5) Input/Output With Schmitt Trigger (MSP430F677xIPEU and MSP430F677xIPZ)

Figure 6-8 shows the port diagram. Table 6-66 summarizes the selection of the pin functions.

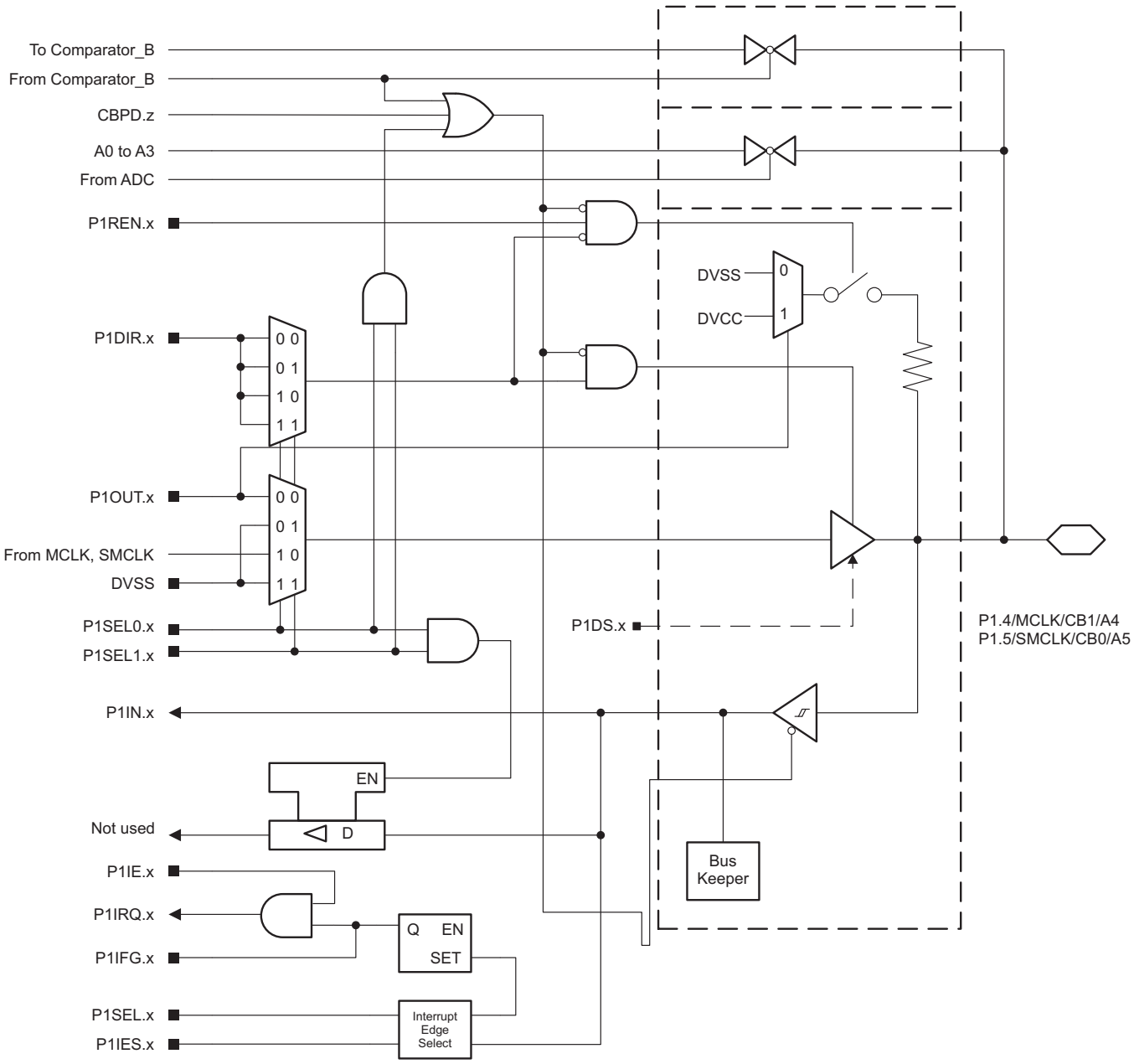



**Figure 6-8. Port P1 (P1.4 and P1.5) Diagram (MSP430F677xIPEU and MSP430F677xIPZ)**


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**Table 6-66. Port P1 (P1.4 and P1.5) Pin Functions (MSP430F677xIPEU and MSP430F677xIPZ)**

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | | |
|---|---|---|---|---|---|---|
| | | | P1DIR.x | P1SEL1.x | P1SEL0.x | CPBD.z |
| P1.4/MCLK/CB1/A4 | 4 | P1.4 (I/O) | I:0; O:1 | 0 | 0 | 0 |
| | | MCLK | 1 | 0 | 1 | 0 |
| | | N/A | 0 | 1 | 0 | 0 |
| | | DVSS | 1 | 1 | 0 | 0 |
| | | A4 | X | 1 | 1 | 0 |
| | | CB1 | X | X | X | 1 (z = 1) |
| P1.5/SMCLK/CB0/A5 | 5 | P1.5 (I/O) | I:0; O:1 | 0 | 0 | 0 |
| | | SMCLK | 1 | 0 | 1 | 0 |
| | | N/A | 0 | 1 | 0 | 0 |
| | | DVSS | 1 | 1 | 0 | 0 |
| | | A5 | X | 1 | 1 | 0 |
| | | CB0 | X | X | X | 1 (z = 0) |

(1) X = don't care

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### 6.14.4 Port P1 (P1.6 and P1.7) Input/Output With Schmitt Trigger (MSP430F677xIPEU and MSP430F677xIPZ)

Figure 6-9 shows the port diagram. Table 6-67 summarizes the selection of the pin functions.

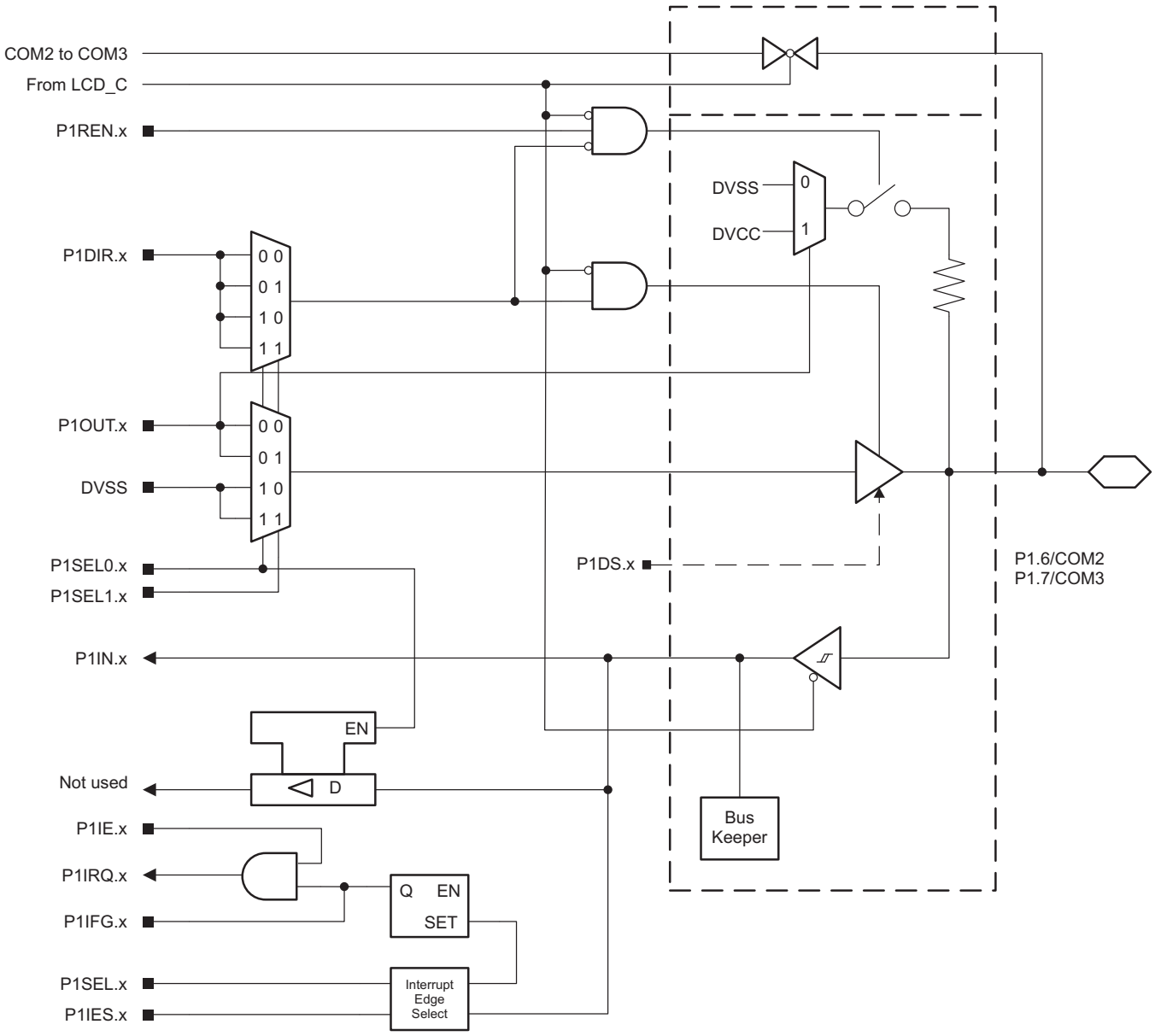



**Figure 6-9. Port P1 (P1.6 and P1.7) Diagram (MSP430F677xIPEU and MSP430F677xIPZ)**


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**Table 6-67. Port P1 (P1.6 and P1.7) Pin Functions (MSP430F677xIPEU and MSP430F677xIPZ)**

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | | |
|---|---|---|---|---|---|---|
| | | | P1DIR.x | P1SEL1.x | P1SEL0.x | COM Enable |
| P1.6/COM2 | 6 | P1.6 (I/O) | I:0; O:1 | X | 0 | 0 |
| | | N/A | 0 | X | 1 | 0 |
| | | DVSS | 1 | X | 1 | 0 |
| | | COM2 | X | X | X | 1 |
| P1.7/COM3 | 7 | P1.7 (I/O) | I:0; O:1 | X | 0 | 0 |
| | | N/A | 0 | X | 1 | 0 |
| | | DVSS | 1 | X | 1 | 0 |
| | | COM3 | X | X | X | 1 |

(1) X = don't care

### 6.14.5 Port P2 (P2.0 to P2.7) Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

Figure 6-10 shows the port diagram. Table 6-68 summarizes the selection of the pin functions.

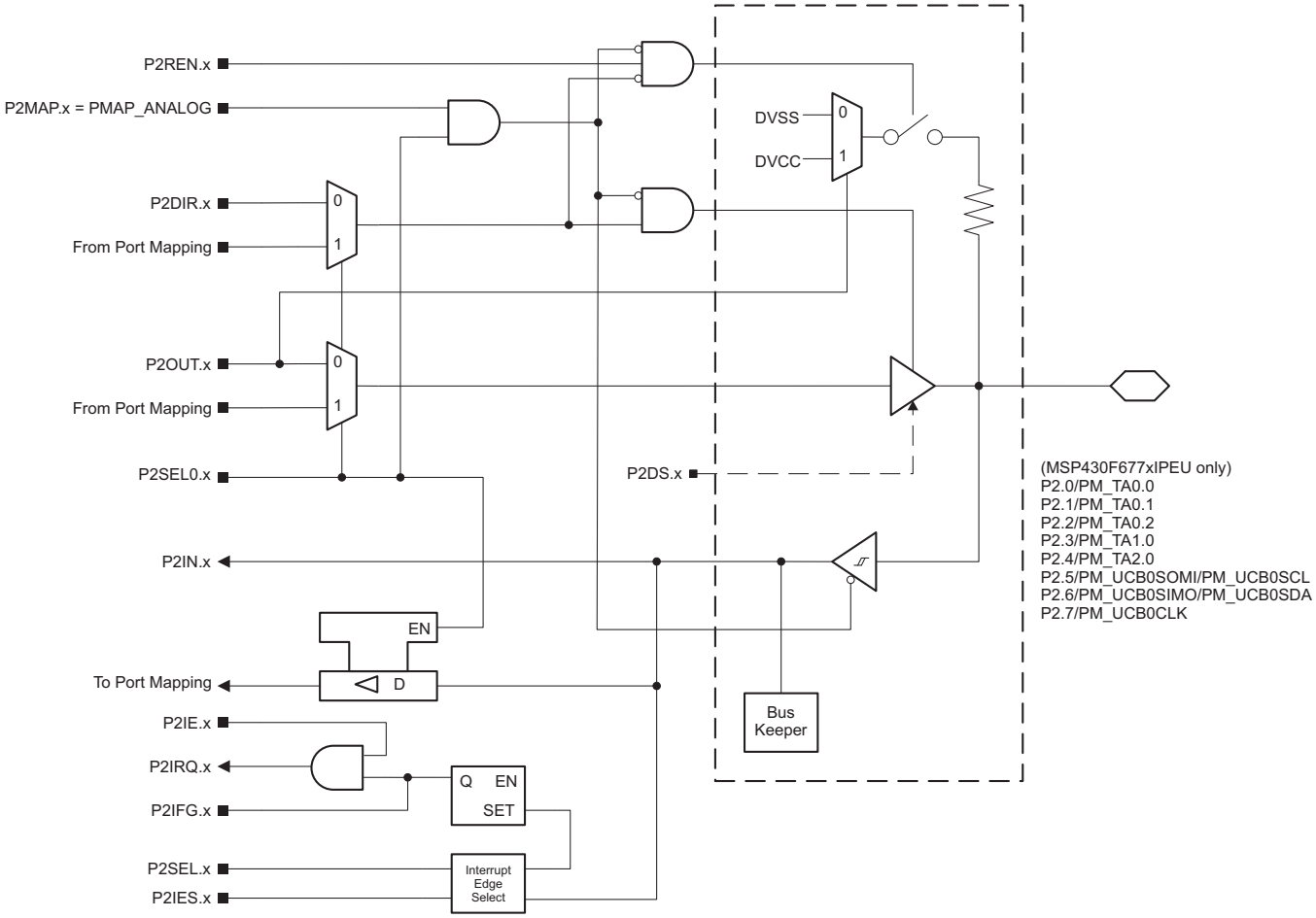



**Figure 6-10. Port P2 (P2.0 to P2.7) Diagram (MSP430F677xIPEU Only)**


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**Table 6-68. Port P2 (P2.0 to P2.7) Pin Functions (MSP430F677xIPEU Only)**

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P2DIR.x | P2SEL0.x | P2MAP.x |
| P2.0/PM_TA0.0 | 0 | P2.0 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P2.1/PM_TA0.1 | 1 | P2.1 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P2.2/PM_TA0.2 | 2 | P2.2 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P2.3/PM_TA1.0 | 3 | P2.3 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P2.4/PM_TA2.0 | 4 | P2.4 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P2.5/PM_UCB0SOMI/ PM_UCB0SCL | 5 | P2.5 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P2.6/PM_UCB0SIMO/ PM_UCB0SDA | 6 | P2.6 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P2.7/PM_UCB0CLK | 7 | P2.7 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |

(1) X = don't care

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### 6.14.6 Port P2 (P2.0 to P2.3) Input/Output With Schmitt Trigger (MSP430F677xIPZ Only)

Figure 6-11 shows the port diagram. Table 6-69 summarizes the selection of the pin functions.

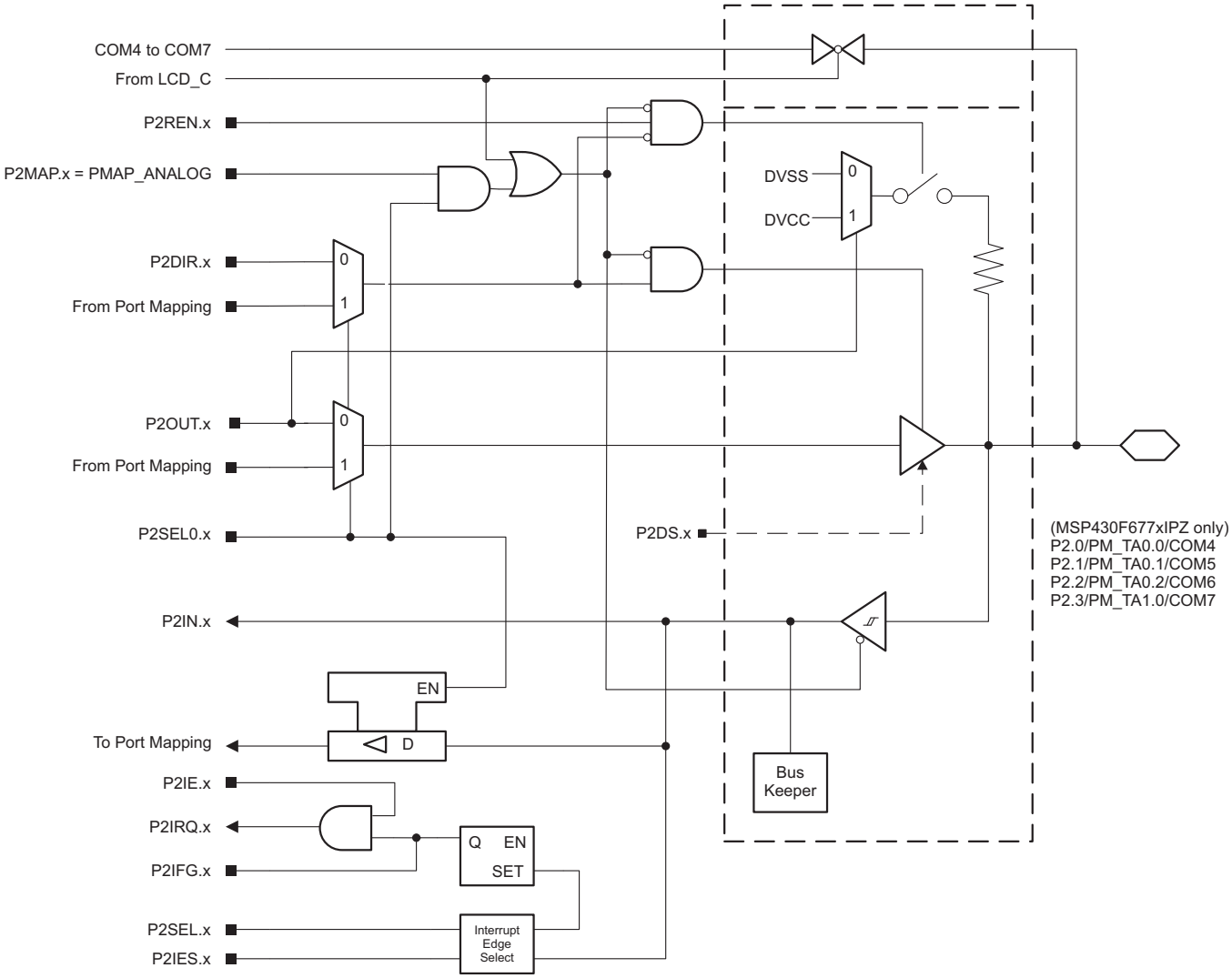



**Figure 6-11. Port P2 (P2.0 to P2.3) Diagram (MSP430F677xIPZ Only)**


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**Table 6-69. Port P2 (P2.0 to P2.3) Pin Functions (MSP430F677xIPZ Only)**

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | | |
|---|---|---|---|---|---|---|
| | | | P2DIR.x | P2SEL0.x | P2MAP.x | COM Enable |
| P2.0/PM_TA0.0/ COM4 | 0 | P2.0 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | COM4 | X | X | X | 1 |
| P2.1/PM_TA0.1/ COM5 | 1 | P2.1 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | COM5 | X | X | X | 1 |
| P2.2/PM_TA0.2/ COM6 | 2 | P2.2 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | COM6 | X | X | X | 1 |
| P2.3/PM_TA1.0/ COM7 | 3 | P2.3 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | COM7 | X | X | X | 1 |

(1) X = don't care

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### 6.14.7 Port P2 (P2.4 and P2.6) Input/Output With Schmitt Trigger (MSP430F677xIPZ Only)

Figure 6-12 shows the port diagram. Table 6-70 summarizes the selection of the pin functions.

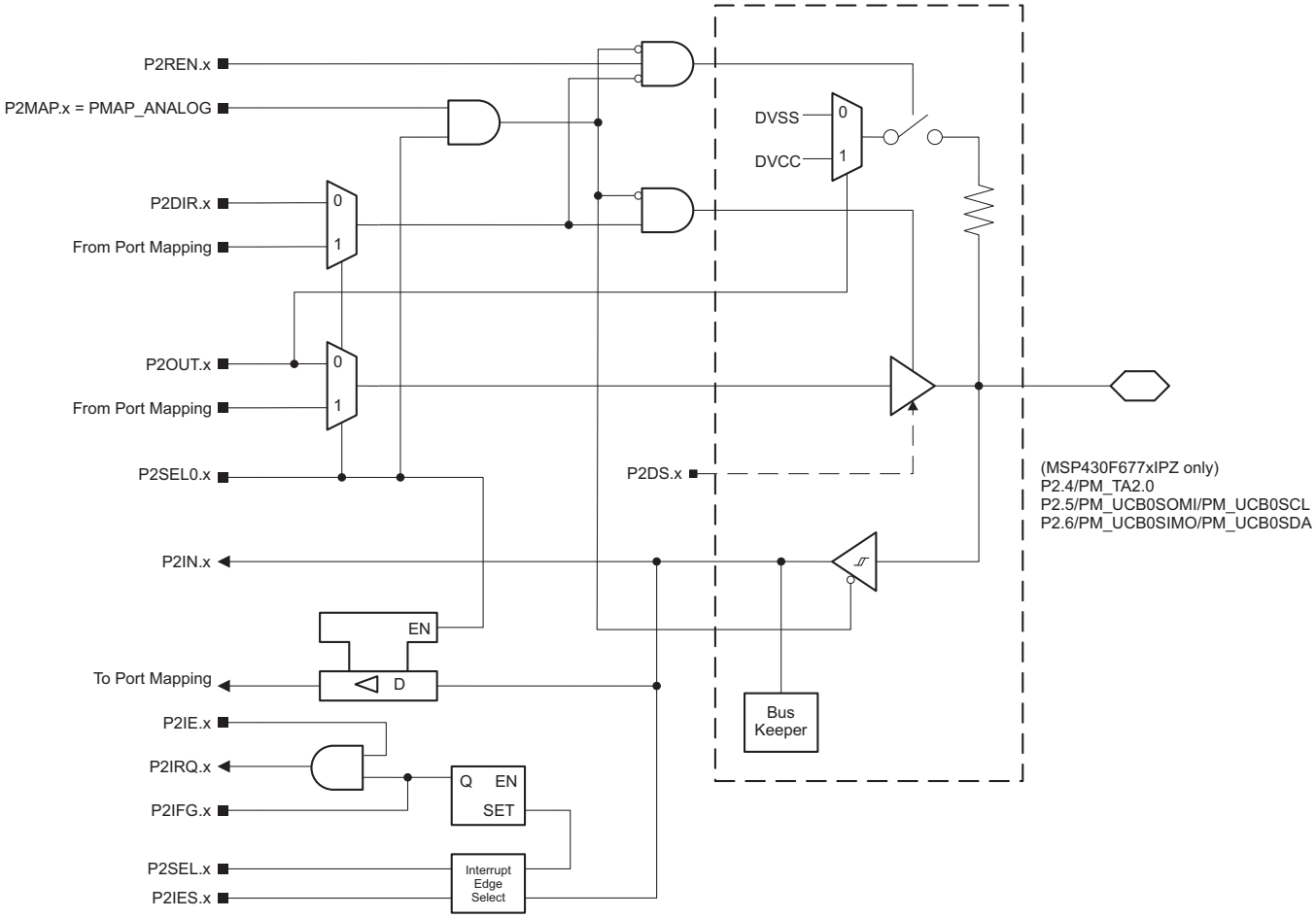



**Figure 6-12. Port P2 (P2.4 and P2.6) Diagram (MSP430F677xIPZ Only)**

**Table 6-70. Port P2 (P2.4 and P2.6) Pin Functions (MSP430F677xIPZ Only)**

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P2DIR.x | P2SEL0.x | P2MAP.x |
| P2.4/PM_TA2.0/R23 | 4 | P2.4 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | R23 | X | 1 | = 31 |
| P2.5/PM_UCB0SOMI/ PM_UCB0SCL/R13 | 5 | P2.5 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | R13 | X | 1 | = 31 |
| P2.6/PM_UCB0SIMO/ PM_UCB0SDA/R03 | 6 | P2.6 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | R03 | X | 1 | = 31 |

(1) X = don't care


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### 6.14.8 Port P2 (P2.7) Input/Output With Schmitt Trigger (MSP430F677xIPZ Only)

Figure 6-13 shows the port diagram. Table 6-71 summarizes the selection of the pin functions.

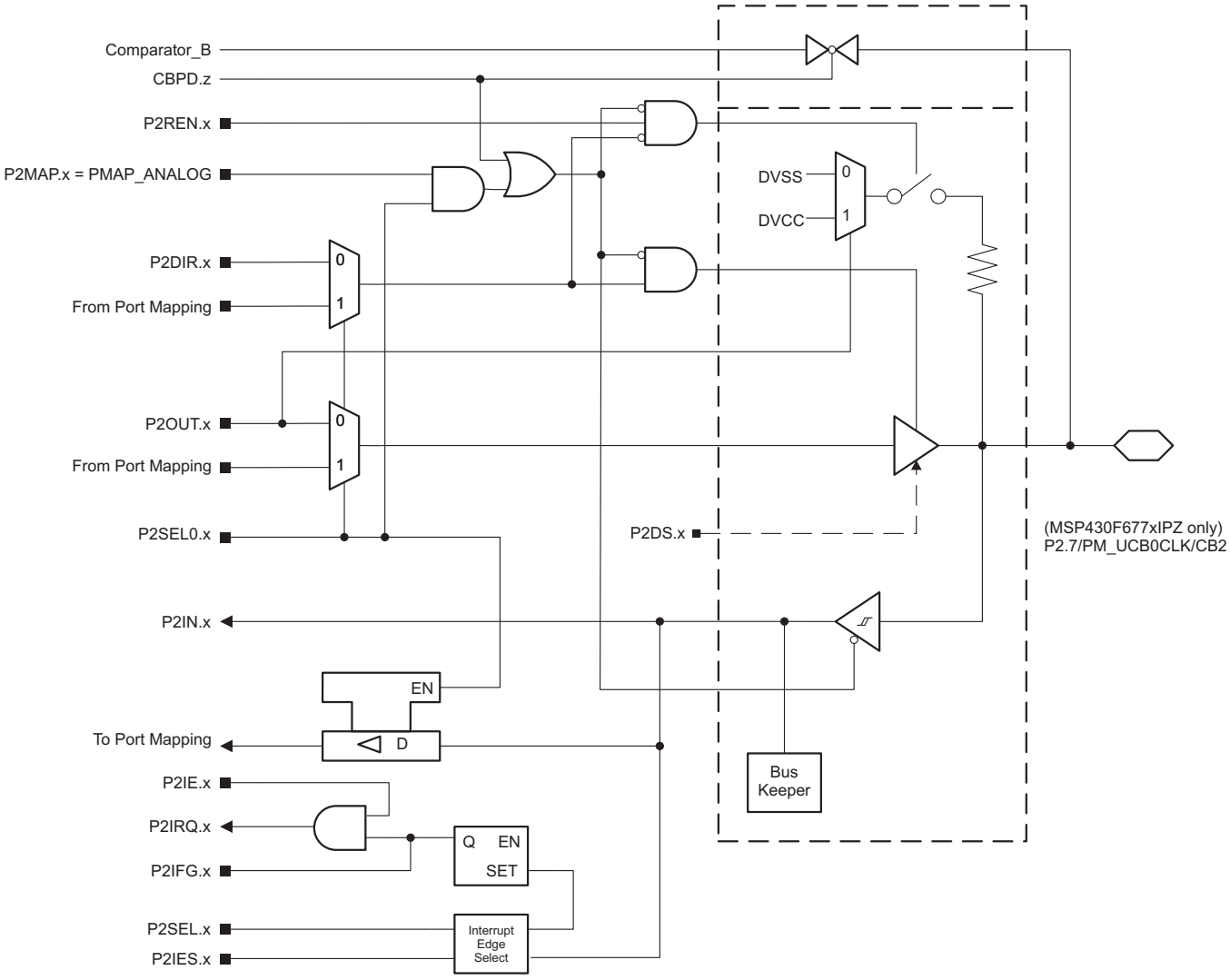



**Figure 6-13. Port P2 (P2.7) Diagram (MSP430F677xIPZ Only)**

**Table 6-71. Port P2 (P2.7) Pin Functions (MSP430F677xIPZ Only)**

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | | |
|---|---|---|---|---|---|---|
| | | | P2DIR.x | P2SEL0.x | P2MAP.x | CBPD.z |
| P2.7/PM_UCB0CLK/ CB2 | 7 | P2.7 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | CB2 | X | X | X | 1 (z = 2) |

(1) X = don't care

### 6.14.9 Ports P3 (P3.0 to P3.7) Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

Figure 6-14 shows the port diagram. Table 6-72 summarizes the selection of the pin functions.

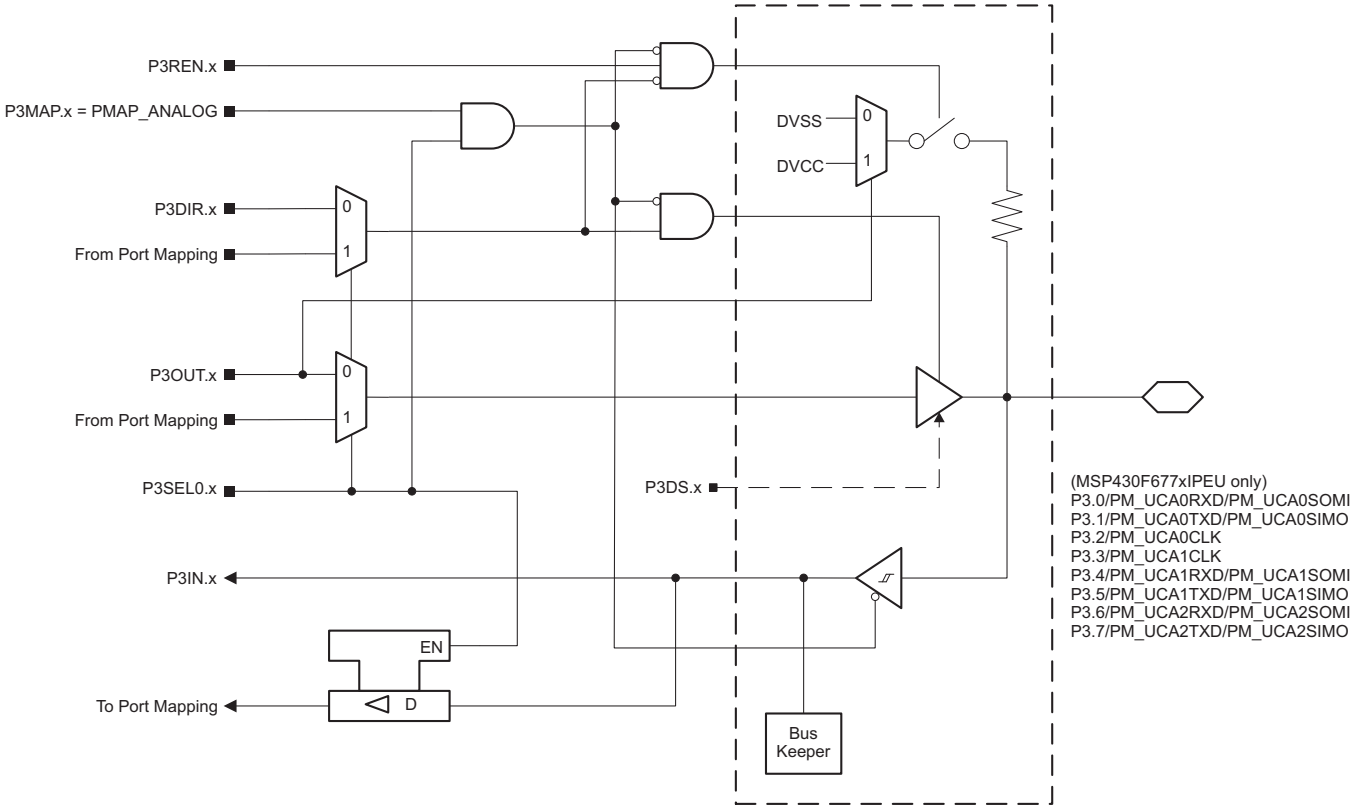



**Figure 6-14. Ports P3 (P3.0 to P3.7) Diagram (MSP430F677xIPEU Only)**


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**Table 6-72. Ports P3 (P3.0 to P3.7) Pin Functions (MSP430F677xIPEU Only)**

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P3DIR.x | P3SEL0.x | P3MAP.x |
| P3.0/PM_UCA0RXD/ PM_UCA0SOMI | 0 | P3.0 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P3.1/PM_UCA0TXD/ PM_UCA0SIMO | 1 | P3.1 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P3.2/PM_UCA0CLK | 2 | P3.2 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P3.3/PM_UCA1CLK | 3 | P3.3 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P3.4/PM_UCA1RXD/ PM_UCA1SOMI | 4 | P3.4 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P3.5/PM_UCA1TXD/ PM_UCA1SIMO | 5 | P3.5 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P3.6/PM_UCA2RXD/ PM_UCA2SOMI | 6 | P3.6 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P3.7/PM_UCA2TXD/ PM_UCA2SIMO | 7 | P3.7 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |

(1) X = don't care

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### 6.14.10 Ports P3 (P3.0) Input/Output With Schmitt Trigger (MSP430F677xIPZ Only)

Figure 6-15 shows the port diagram. Table 6-73 summarizes the selection of the pin functions.

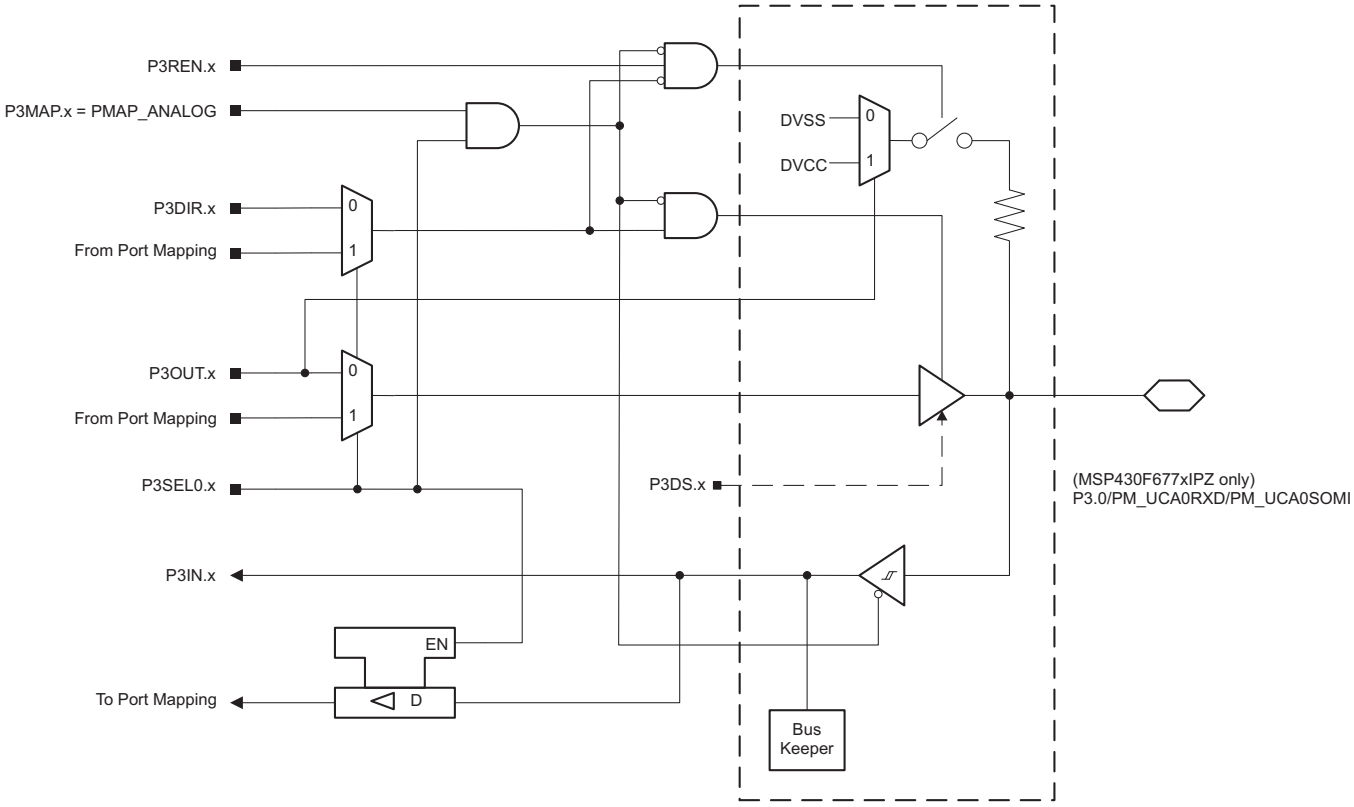



**Figure 6-15. Ports P3 (P3.0) Diagram (MSP430F677xIPZ Only)**

**Table 6-73. Ports P3 (P3.0) Pin Functions (MSP430F677xIPZ Only)**

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P3DIR.x | P3SEL0.x | P3MAP.x |
| P3.0/PM_UCA0RXD/ PM_UCA0SOMI | 0 | P3.0 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |

(1) X = don't care


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### 6.14.11 Ports P3 (P3.1 to P3.7) Input/Output With Schmitt Trigger (MSP430F677xIPZ Only)

Figure 6-16 shows the port diagram. Table 6-74 summarizes the selection of the pin functions.

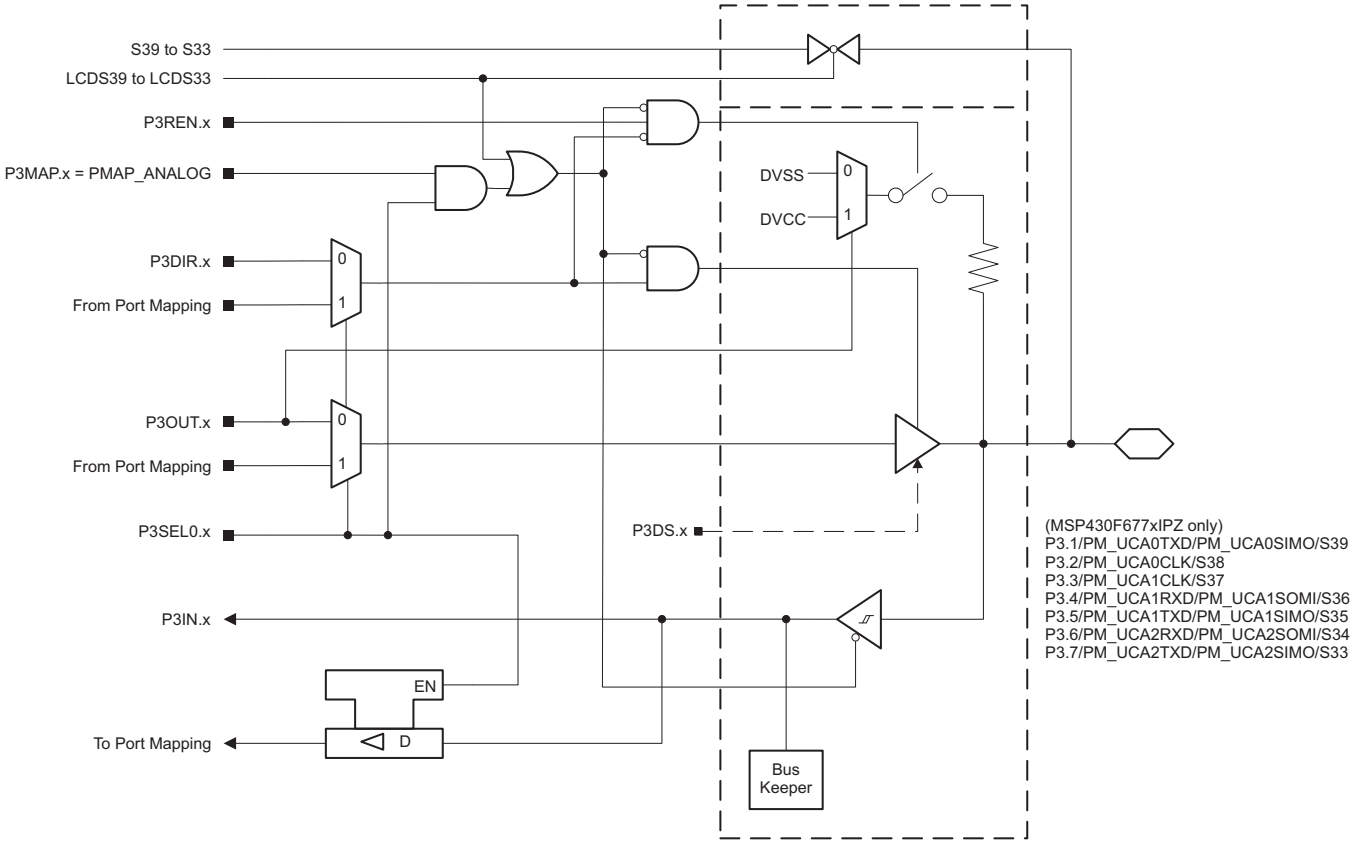



**Figure 6-16. Ports P3 (P3.1 to P3.7) Diagram (MSP430F677xIPZ Only)**

**Table 6-74. Ports P3 (P3.1 to P3.7) Pin Functions (MSP430F677xIPZ Only)**

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | | |
|---|---|---|---|---|---|---|
| | | | P3DIR.x | P3SEL0.x | P3MAP.x | LCD39 to LCD33 |
| P3.1/PM_UCA0TXD/ PM_UCA0SIMO/S39 | 1 | P3.1 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S39 | X | X | X | 1 |
| P3.2/PM_UCA0CLK/ S38 | 2 | P3.2 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S38 | X | X | X | 1 |
| P3.3/PM_UCA1CLK/ S37 | 3 | P3.3 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S37 | X | X | X | 1 |
| P3.4/PM_UCA1RXD/ PM_UCA1SOMI/S36 | 4 | P3.4 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S36 | X | X | X | 1 |
| P3.5/PM_UCA1TXD/ PM_UCA1SIMO/S35 | 5 | P3.5 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S35 | X | X | X | 1 |
| P3.6/PM_UCA2RXD/ PM_UCA2SOMI/S34 | 6 | P3.6 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S34 | X | X | X | 1 |
| P3.7/PM_UCA2TXD/ PM_UCA2SIMO/S33 | 7 | P3.7 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S33 | X | X | X | 1 |

(1) X = don't care


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### 6.14.12 Port P4 (P4.0 to P4.7) Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

Figure 6-17 shows the port diagram. Table 6-75 summarizes the selection of the pin functions.

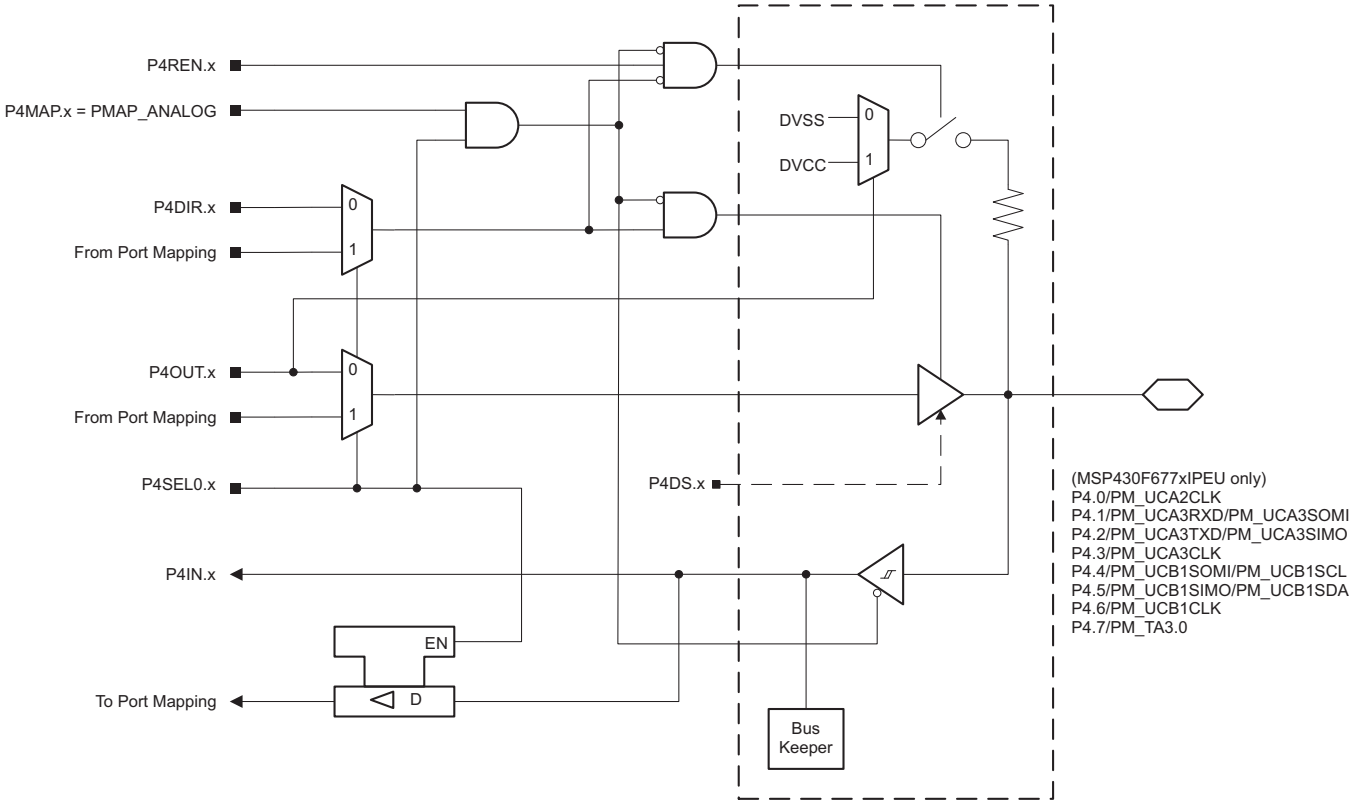



**Figure 6-17. Port P4 (P4.0 to P4.7) Diagram (MSP430F677xIPEU Only)**

**Table 6-75. Port P4 (P4.0 to P4.7) Pin Functions (MSP430F677xIPEU Only)**

| PIN NAME (P4.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P4DIR.x | P4SEL0.x | P4MAP.x |
| P4.0/PM_UCA2CLK | 0 | P4.0 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P4.1/PM_UCA3RXD/ PM_UCA3SOMI | 1 | P4.1 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P4.2/PM_UCA3TXD/ PM_UCA3SIMO | 2 | P4.2 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P4.3/PM_UCA3CLK | 3 | P4.3 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P4.4/PM_UCB1SOMI/ PM_UCB1SCL | 4 | P4.4 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P4.5/PM_UCB1SIMO/ PM_UCB1SDA | 5 | P4.5 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P4.6/PM_UCB1CLK | 6 | P4.6 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P4.7/PM_TA3.0 | 7 | P4.7 (I/O) | I:0; O:1 | 0 | X |
| | | Mapped secondary digital function | X | 1 | ≤ 30 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |

(1) X = don't care


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### 6.14.13 Port P4 (P4.0 to P4.7) Input/Output With Schmitt Trigger (MSP430F677xIPZ Only)

Figure 6-18 shows the port diagram. Table 6-76 summarizes the selection of the pin functions.

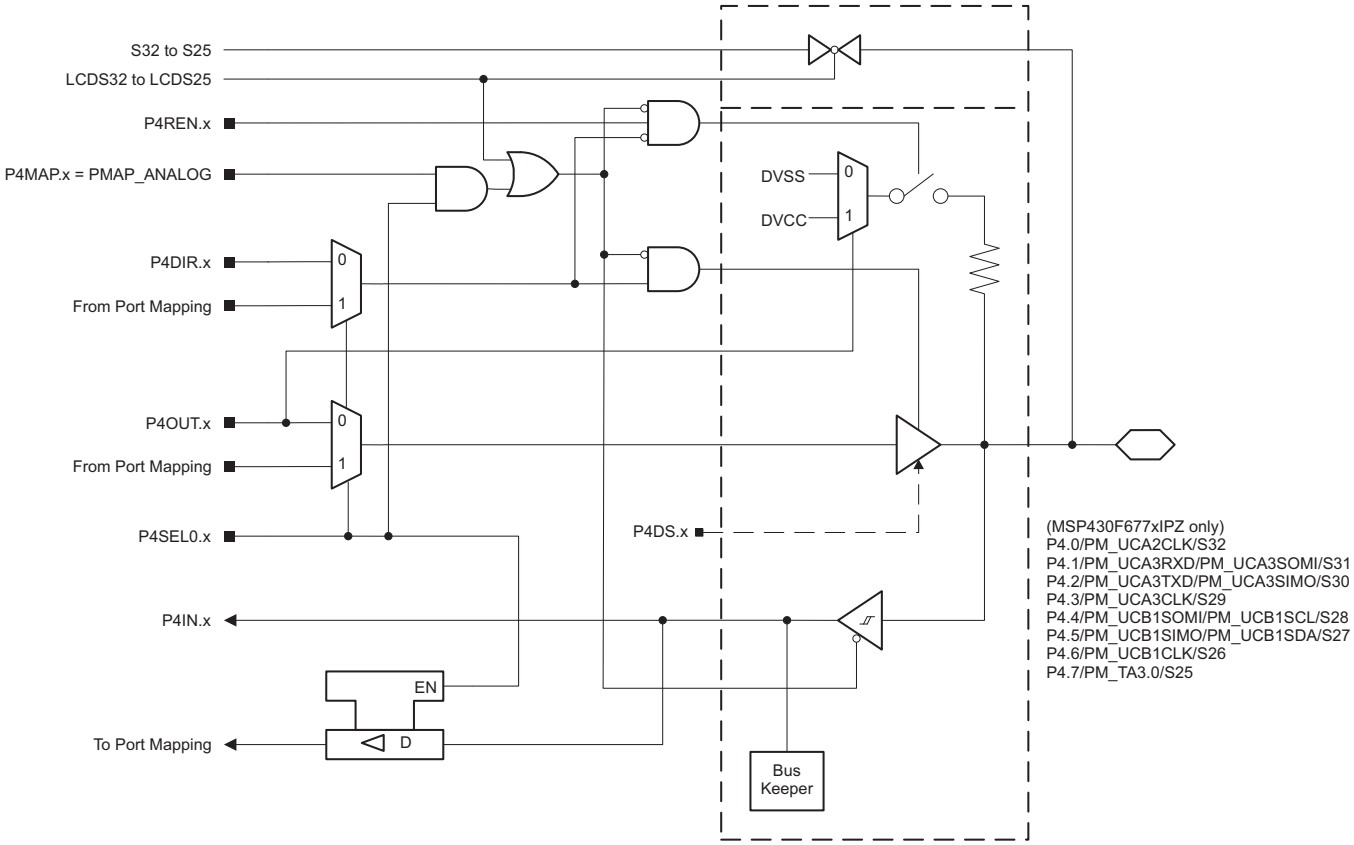



**Figure 6-18. Port P4 (P4.0 to P4.7) Diagram (MSP430F677xIPZ Only)**

**Table 6-76. Port P4 (P4.0 to P4.7) Pin Functions (MSP430F677xIPZ Only)**

| PIN NAME (P4.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | | |
|---|---|---|---|---|---|---|
| | | | P4DIR.x | P4SEL0.x | P4MAP.x | LCD32 to LCD25 |
| P4.0/PM_UCA2CLK/S32 | 0 | P4.0 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S32 | X | X | X | 1 |
| P4.1/PM_UCA3RXD/PM_UCA3SOMI/S31 | 1 | P4.1 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S31 | X | X | X | 1 |
| P4.2/PM_UCA3TXD/PM_UCA3SIMO/S30 | 2 | P4.2 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S30 | X | X | X | 1 |
| P4.3/PM_UCA3CLK/S29 | 3 | P4.3 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S29 | X | X | X | 1 |
| P4.4/PM_UCB1SOMI/PM_UCB1SCL/S28 | 4 | P4.4 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S28 | X | X | X | 1 |
| P4.5/PM_UCB1SIMO/PM_UCB1SDA/S27 | 5 | P4.5 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S27 | X | X | X | 1 |
| P4.6/PM_UCB1CLK/S26 | 6 | P4.6 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S26 | X | X | X | 1 |
| P4.7/PM_TA3.0/S25 | 7 | P4.7 (I/O) | I:0; O:1 | 0 | X | 0 |
| | | Mapped secondary digital function | X | 1 | ≤ 30 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S25 | X | X | X | 1 |

(1) X = don't care


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### 6.14.14 Port P5 (P5.0 to P5.3) Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

Figure 6-19 shows the port diagram. Table 6-77 summarizes the selection of the pin functions.

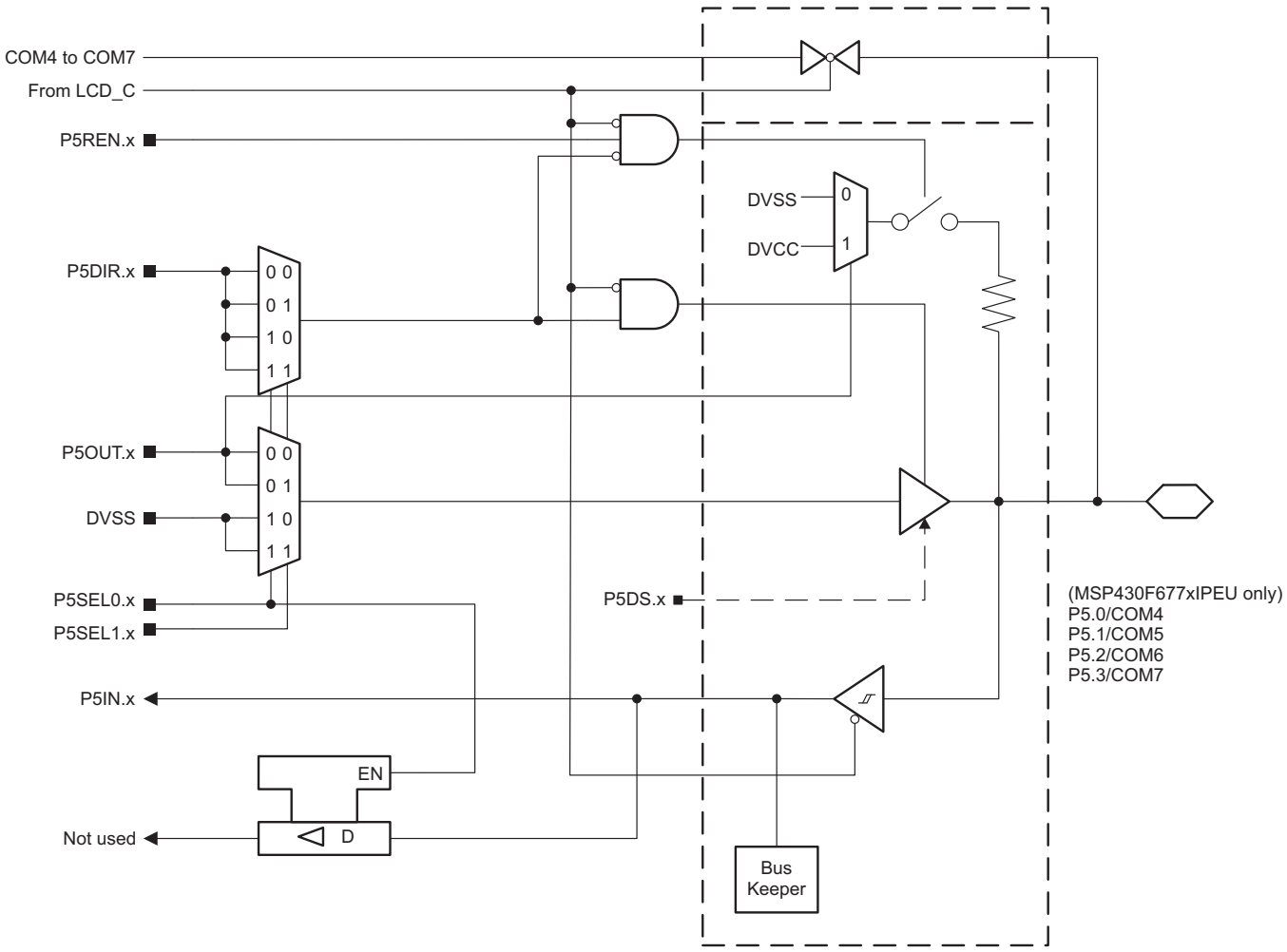



**Figure 6-19. Port P5 (P5.0 to P5.3) Diagram (MSP430F677xIPEU Only)**

**Table 6-77. Port P5 (P5.0 to P5.3) Pin Functions (MSP430F677xIPEU Only)**

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | | |
|---|---|---|---|---|---|---|
| | | | P5DIR.x | P5SEL1.x | P5SEL0.x | COM Enable |
| P5.0/COM4 | 0 | P5.0 (I/O) | I:0; O:1 | X | 0 | 0 |
| | | N/A | 0 | X | 1 | 0 |
| | | DVSS | 1 | X | 1 | 0 |
| | | COM4 | X | X | X | 1 |
| P5.1/COM5 | 1 | P5.1 (I/O) | I:0; O:1 | X | 0 | 0 |
| | | N/A | 0 | X | 1 | 0 |
| | | DVSS | 1 | X | 1 | 0 |
| | | COM5 | X | X | X | 1 |
| P5.2/COM6 | 2 | P5.2 (I/O) | I:0; O:1 | X | 0 | 0 |
| | | N/A | 0 | X | 1 | 0 |
| | | DVSS | 1 | X | 1 | 0 |
| | | COM6 | X | X | X | 1 |
| P5.3/COM7 | 3 | P5.3 (I/O) | I:0; O:1 | X | 0 | 0 |
| | | N/A | 0 | X | 1 | 0 |
| | | DVSS | 1 | X | 1 | 0 |
| | | COM7 | X | X | X | 1 |

(1) X = don't care


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### 6.14.15 Port P5 (P5.4 to P5.6) Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

Figure 6-20 shows the port diagram. Table 6-78 summarizes the selection of the pin functions.

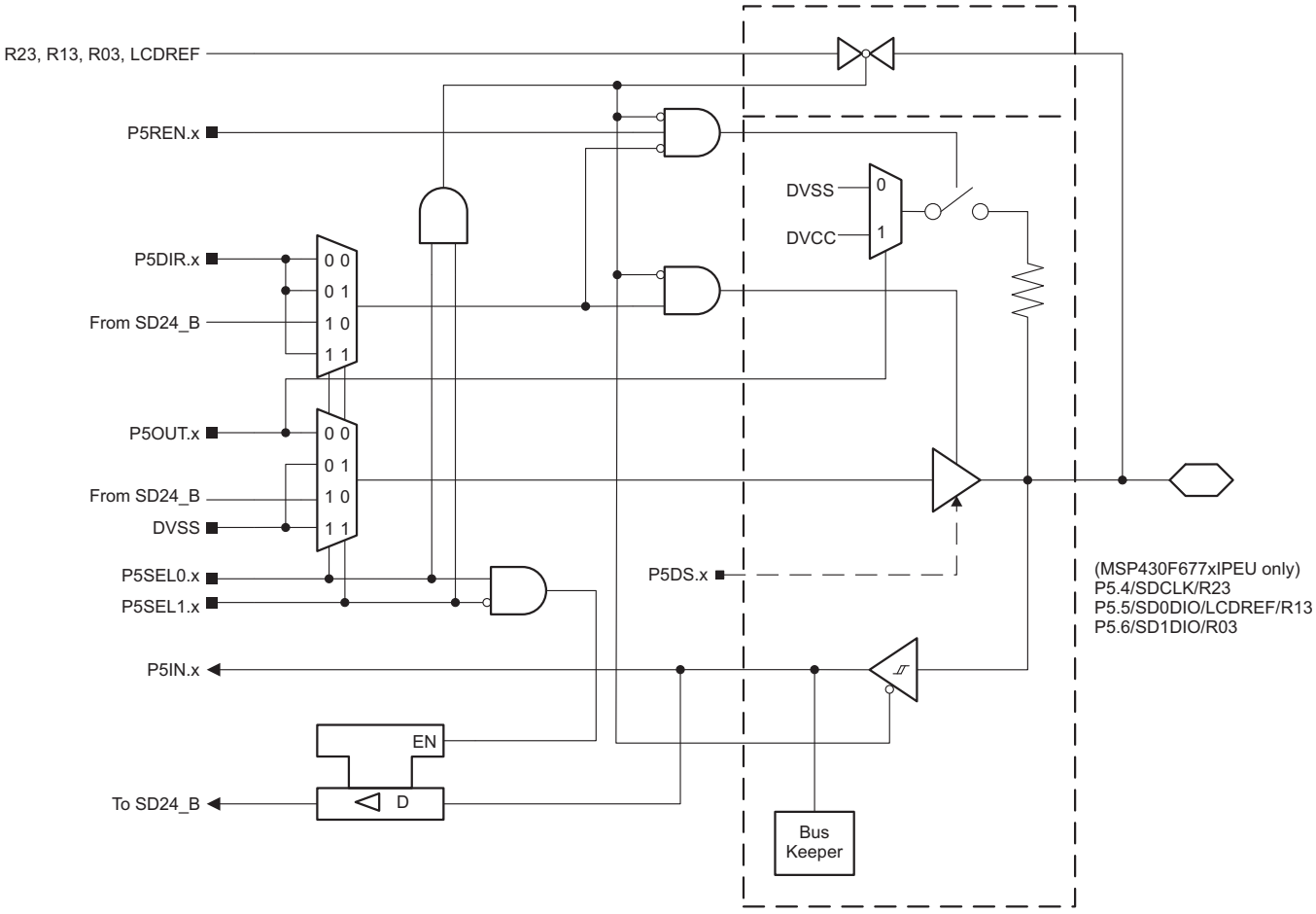



**Figure 6-20. Port P5 (P5.4 to P5.6) Diagram (MSP430F677xIPEU Only)**

**Table 6-78. Port P5 (P5.4 to P5.6) Pin Functions (MSP430F677xIPEU Only)**

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P5DIR.x | P5SEL1.x | P5SEL0.x |
| P5.4/SDCLK/R23 | 4 | P5.4 (I/O) | I:0; O:1 | 0 | 0 |
| | | Secondary digital function | X | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | R23 | X | 1 | 1 |
| P5.5/SD0DIO/LCDREF/R13 | 5 | P5.5 (I/O) | I:0; O:1 | 0 | 0 |
| | | Secondary digital function | X | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | LCDREF/R13 | X | 1 | 1 |
| PT.6/SD1DIO/R03 | 6 | P5.6 (I/O) | I:0; O:1 | 0 | 0 |
| | | Secondary digital function | X | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | R03 | X | 1 | 1 |

(1) X = don't care


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### 6.14.16 Port P5 (P5.7) Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

Figure 6-21 shows the port diagram. Table 6-79 summarizes the selection of the pin functions.

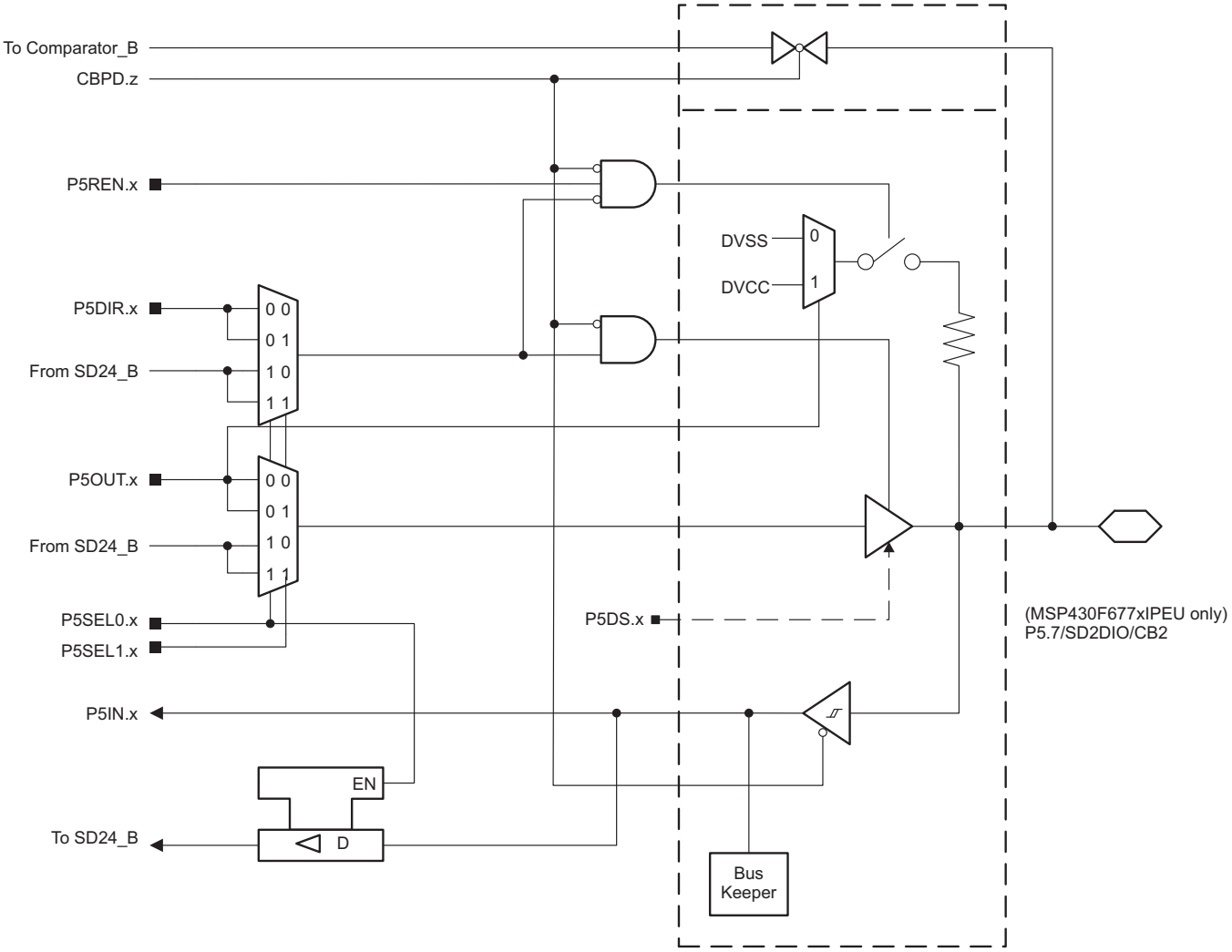



**Figure 6-21. Port P5 (P5.7) Diagram (MSP430F677xIPEU Only)**

**Table 6-79. Port P5 (P5.7) Pin Functions (MSP430F677xIPEU Only)**

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | | |
|---|---|---|---|---|---|---|
| | | | P5DIR.x | P5SEL1.x | P5SEL0.x | CBPD.z |
| P5.7/SD2DIO/CB2 | 7 | P5.7 (I/O) | I:0; O:1 | X | 0 | 0 |
| | | Secondary digital function | X | X | 1 | 0 |
| | | CB2 | X | X | X | 1 (z = 2) |

(1) X = don't care

### 6.14.17 Port P5 (P5.0 to P5.7) Input/Output With Schmitt Trigger (MSP430F677xIPZ Only)

Figure 6-22 shows the port diagram. Table 6-80 summarizes the selection of the pin functions.

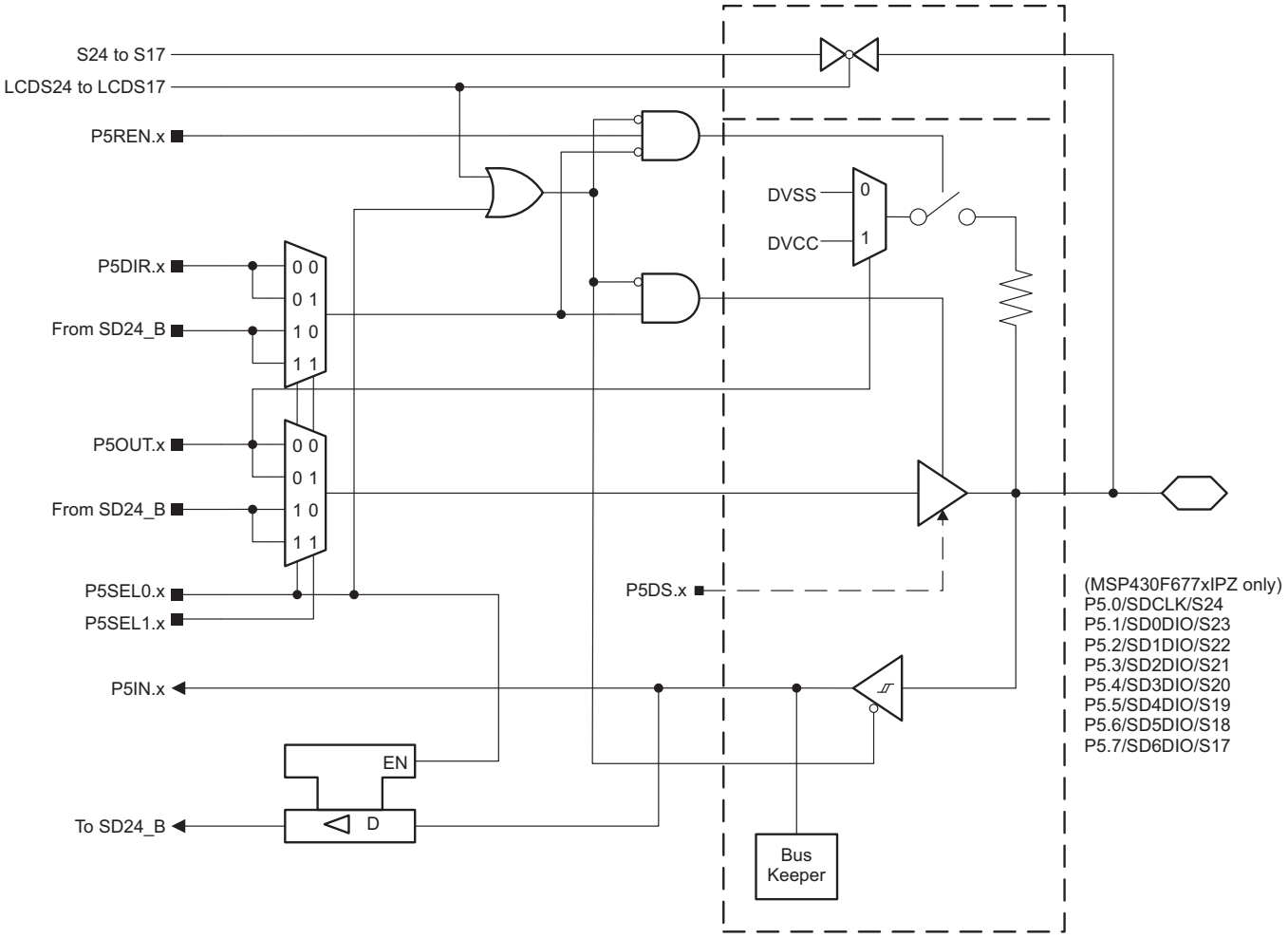



**Figure 6-22. Port P5 (P5.0 to P5.7) Diagram (MSP430F677xIPZ Only)**


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**Table 6-80. Port P5 (P5.0 to P5.7) Pin Functions (MSP430F677xIPZ Only)**

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | | |
|---|---|---|---|---|---|---|
| | | | P5DIR.x | P5SEL1.x | P5SEL0.x | LCD24 to LCD17 |
| P5.0/SDCLK/S24 | 0 | P5.0 (I/O) | I:0; O:1 | X | 0 | 0 |
| | | Secondary digital function | X | X | 1 | 0 |
| | | S24 | X | X | X | 1 |
| P5.1/SD0DIO/S23 | 1 | P5.1 (I/O) | I:0; O:1 | X | 0 | 0 |
| | | Secondary digital function | X | X | 1 | 0 |
| | | S23 | X | X | X | 1 |
| P5.2/SD1DIO/S22 | 2 | P5.2 (I/O) | I:0; O:1 | X | 0 | 0 |
| | | Secondary digital function | X | X | 1 | 0 |
| | | S22 | X | X | X | 1 |
| P5.3/SD2DIO/S21 | 3 | P5.3 (I/O) | I:0; O:1 | X | 0 | 0 |
| | | Secondary digital function | X | X | 1 | 0 |
| | | S21 | X | X | X | 1 |
| P5.4/SD3DIO/S20 | 4 | P5.4 (I/O) | I:0; O:1 | X | 0 | 0 |
| | | Secondary digital function | X | X | 1 | 0 |
| | | S20 | X | X | X | 1 |
| P5.5/SD4DIO/S19 | 5 | P5.5 (I/O) | I:0; O:1 | X | 0 | 0 |
| | | Secondary digital function | X | X | 1 | 0 |
| | | S19 | X | X | X | 1 |
| P5.6/SD5DIO/S18 | 6 | P5.6 (I/O) | I:0; O:1 | X | 0 | 0 |
| | | Secondary digital function | X | X | 1 | 0 |
| | | S18 | X | X | X | 1 |
| P5.7/SD6DIO/S17 | 7 | P5.7 (I/O) | I:0; O:1 | X | 0 | 0 |
| | | Secondary digital function | X | X | 1 | 0 |
| | | S17 | X | X | X | 1 |

(1) X = don't care

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### 6.14.18 Port P6 (P6.0) Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

Figure 6-23 shows the port diagram. Table 6-81 summarizes the selection of the pin functions.

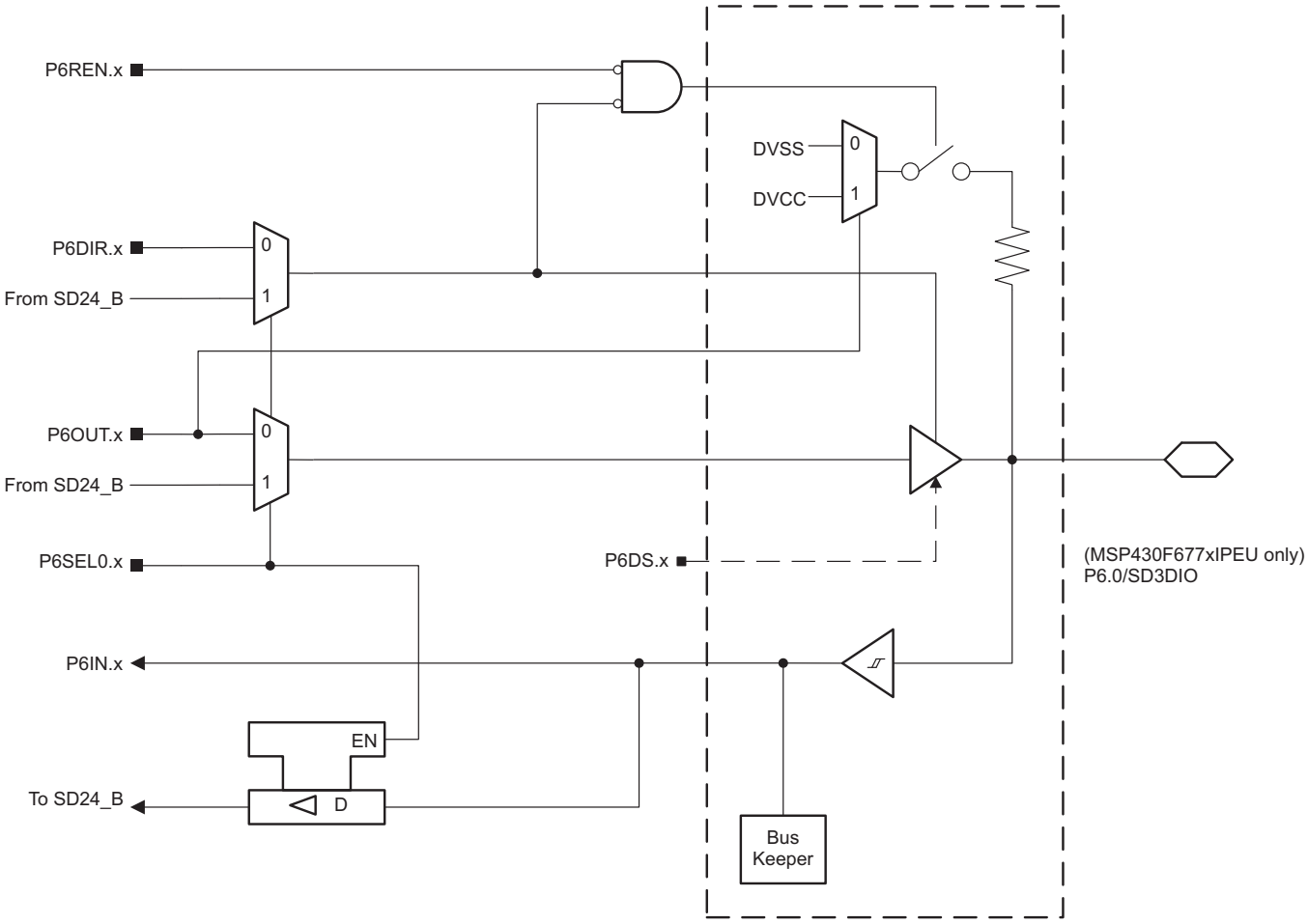



**Figure 6-23. Port P6 (P6.0) Diagram (MSP430F677xIPEU Only)**

**Table 6-81. Port P6 (P6.0) Pin Functions (MSP430F677xIPEU Only)**

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | |
|---|---|---|---|---|
| | | | P6DIR.x | P6SEL0.x |
| P6.0/SD3DIO | 0 | P6.0 (I/O) | I:0; O:1 | 0 |
| | | Secondary digital function | X | 1 |

(1) X = don't care


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### 6.14.19 Port P6 (P6.1 to P6.3) Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

Figure 6-24 shows the port diagram. Table 6-82 summarizes the selection of the pin functions.

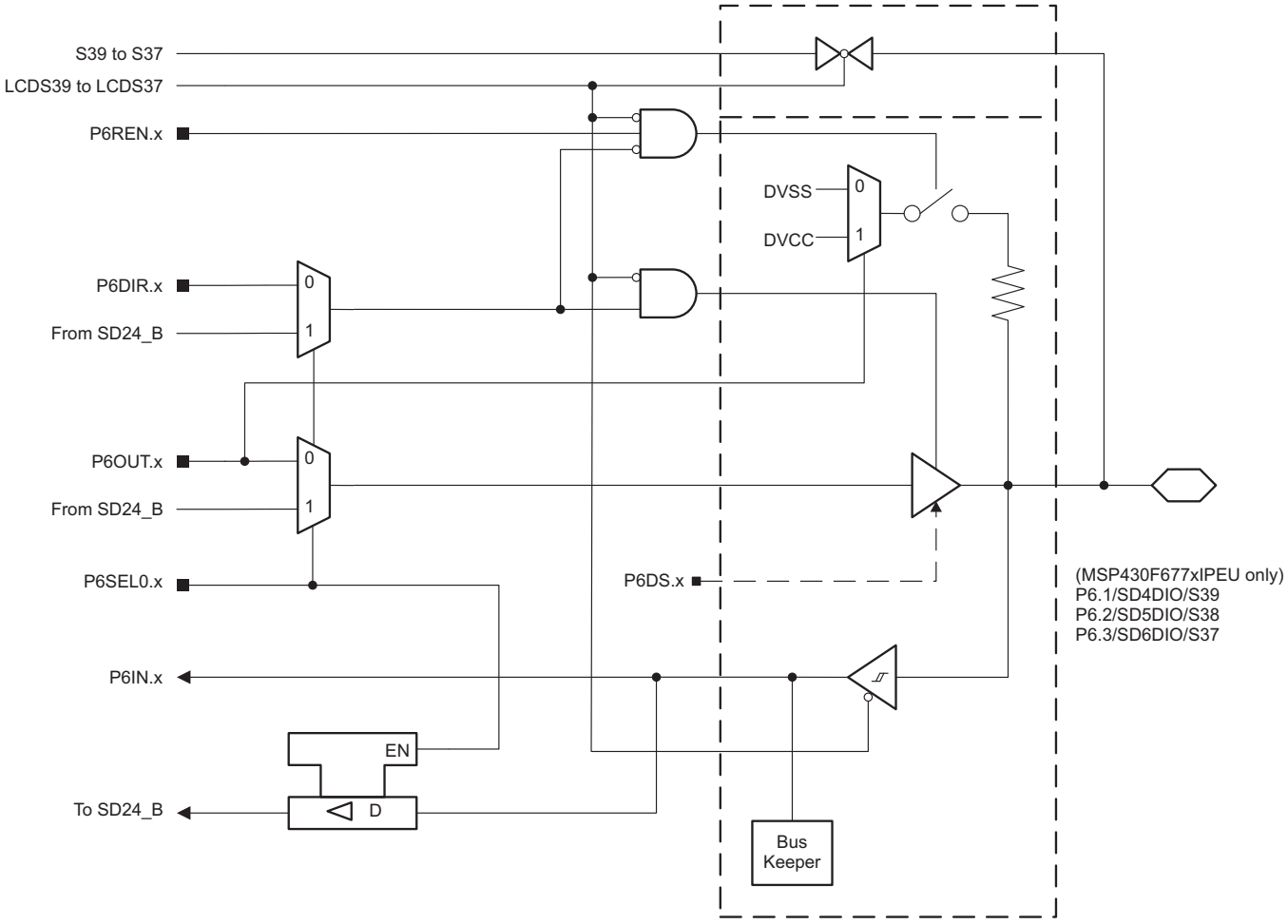



**Figure 6-24. Port P6 (P6.1 to P6.3) Diagram (MSP430F677xIPEU Only)**

**Table 6-82. Port P6 (P6.1 to P6.3) Pin Functions (MSP430F677xIPEU Only)**

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P6DIR.x | P6SEL0.x | LCD39 to LCD37 |
| P6.1/SD4DIO/S39 | 1 | P6.1 (I/O) | I:0; O:1 | 0 | 0 |
| | | Secondary digital function | X | 1 | 0 |
| | | S39 | X | X | 1 |
| P6.2/SD5DIO/S38 | 2 | P6.2 (I/O) | I:0; O:1 | 0 | 0 |
| | | Secondary digital function | X | 1 | 0 |
| | | S38 | X | X | 1 |
| P6.3/SD6DIO/S37 | 3 | P6.3 (I/O) | I:0; O:1 | 0 | 0 |
| | | Secondary digital function | X | 1 | 0 |
| | | S37 | X | X | 1 |

(1) X = don't care

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### 6.14.20 Port P6 (P6.4 to P6.7) Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

Figure 6-25 shows the port diagram. Table 6-83 summarizes the selection of the pin functions.

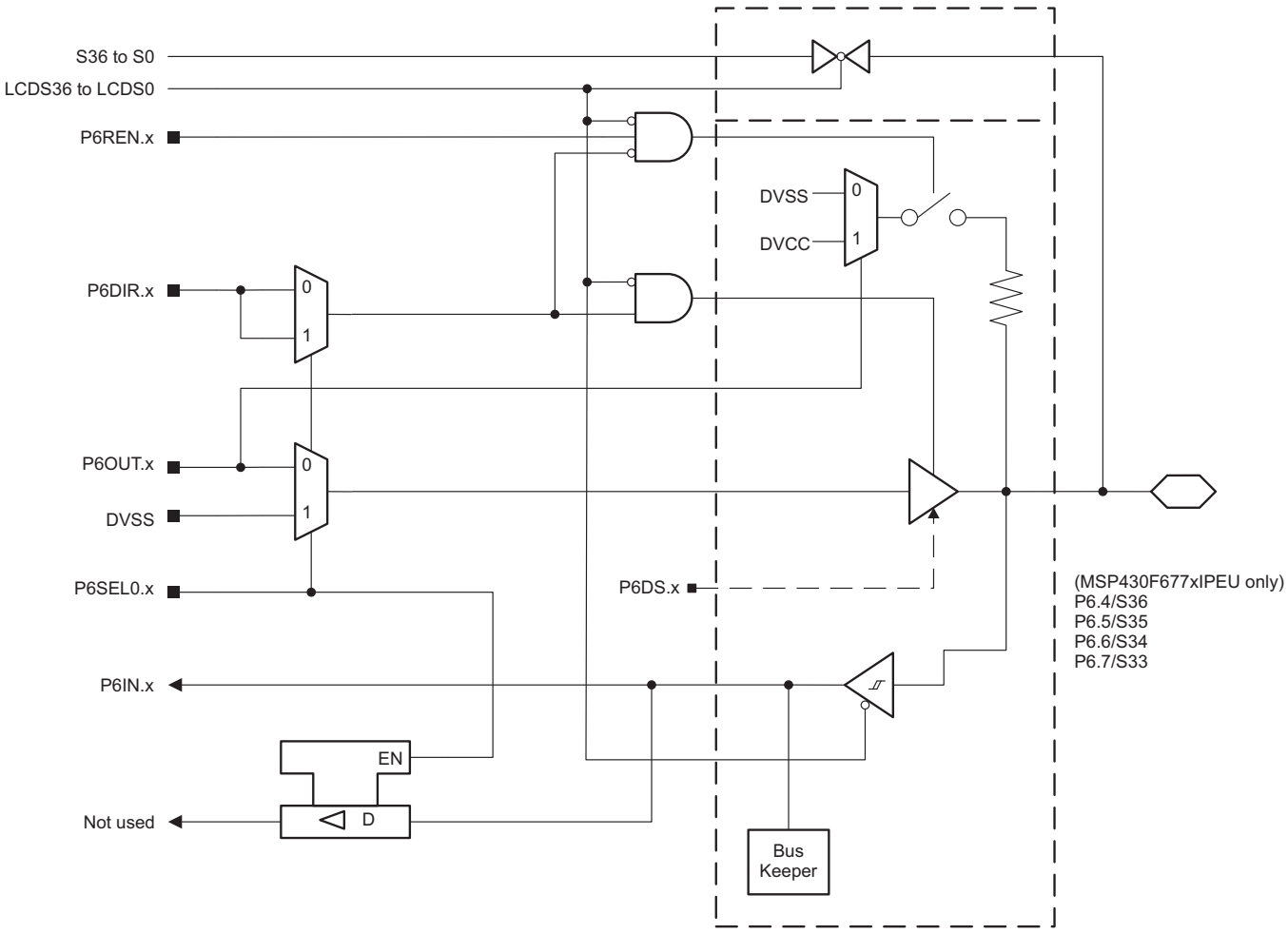



**Figure 6-25. Port P6 (P6.4 to P6.7) Diagram (MSP430F67xxIPEU Only)**


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**Table 6-83. Port P6 (P6.4 to P6.7) Pin Functions (MSP430F67xxIPEU Only)**

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P6DIR.x | P6SEL0.x | LCD36 to LCD33 |
| P6.4/S36 | 4 | P6.4 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S36 | X | X | 1 |
| P6.5/S35 | 5 | P6.5 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S35 | X | X | 1 |
| P6.6/S34 | 6 | P6.6(I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S34 | X | X | 1 |
| P6.7/S33 | 7 | P6.7 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S33 | X | X | 1 |

(1) X = don't care

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### 6.14.21 Port P6 (P6.0 to P6.7) Input/Output With Schmitt Trigger (MSP430F677xIPZ Only)

Figure 6-26 shows the port diagram. Table 6-84 summarizes the selection of the pin functions.

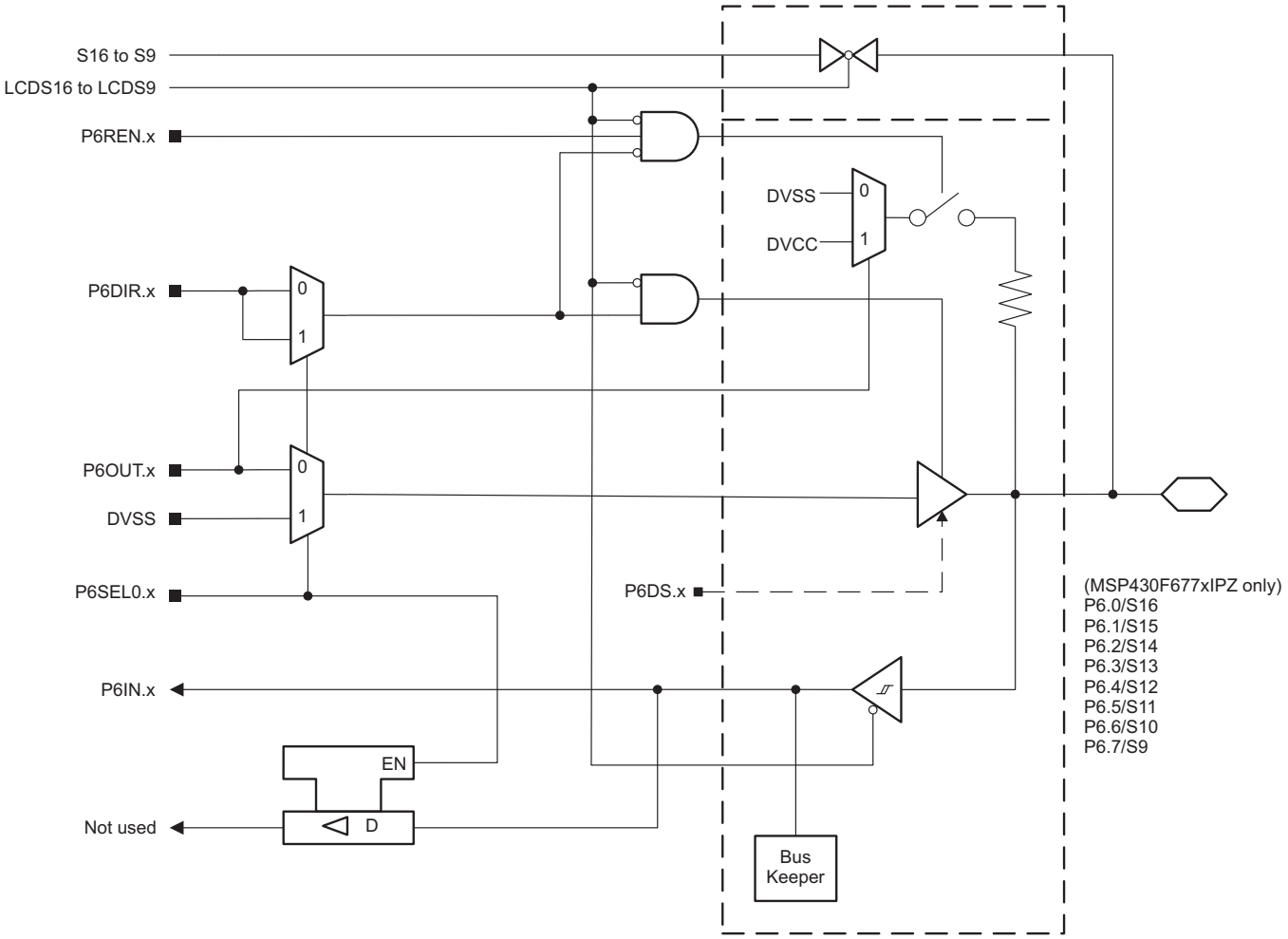



**Figure 6-26. Port P6 (P6.0 to P6.7) Diagram (MSP430F67xxIPZ Only)**


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**Table 6-84. Port P6 (P6.0 to P6.7) Pin Functions (MSP430F67xxIPZ Only)**

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P6DIR.x | P6SEL0.x | LCD16 to LCD9 |
| P6.0/S16 | 0 | P6.0 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S16 | X | X | 1 |
| P6.1/S15 | 1 | P6.1 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S15 | X | X | 1 |
| P6.2/S14 | 2 | P6.2 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S14 | X | X | 1 |
| P6.3/S13 | 3 | P6.3 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S13 | X | X | 1 |
| P6.4/S12 | 4 | P6.4 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S12 | X | X | 1 |
| P6.5/S11 | 5 | P6.5 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S11 | X | X | 1 |
| P6.6/S10 | 6 | P6.6 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S10 | X | X | 1 |
| P6.7/S9 | 7 | P6.7 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S9 | X | X | 1 |

(1) X = don't care

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### 6.14.22 Port P7 (P7.0 to P7.7) Input/Output With Schmitt Trigger (MSP430F67xxIPEU Only)

Figure 6-27 shows the port diagram. Table 6-85 summarizes the selection of the pin functions.

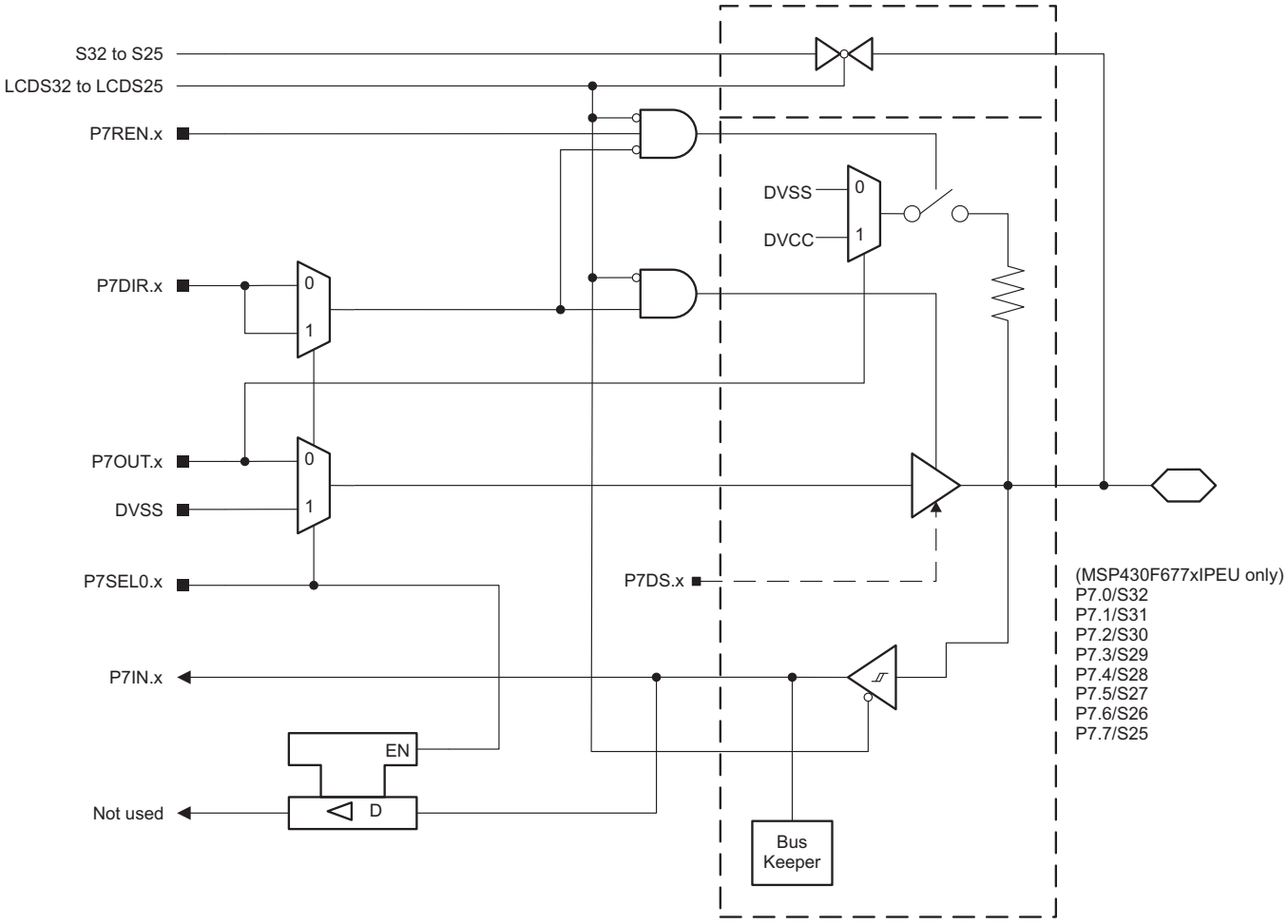



**Figure 6-27. Port P7 (P7.0 to P7.7) Diagram (MSP430F67xxIPEU Only)**


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**Table 6-85. Port P7 (P7.0 to P7.7) Pin Functions (MSP430F67xxIPEU Only)**

| PIN NAME (P7.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P7DIR.x | P7SEL0.x | LCD32 to LCD25 |
| P7.0/S32 | 0 | P7.0 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S32 | X | X | 1 |
| P7.1/S31 | 1 | P7.1 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S31 | X | X | 1 |
| P7.2/S30 | 2 | P7.2 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S30 | X | X | 1 |
| P7.3/S29 | 3 | P7.3 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S29 | X | X | 1 |
| P7.4/S28 | 4 | P7.4 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S28 | X | X | 1 |
| P7.5/S27 | 5 | P7.5 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S27 | X | X | 1 |
| P7.6/S26 | 6 | P7.6 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S26 | X | X | 1 |
| P7.7/S25 | 7 | P7.7 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S25 | X | X | 1 |

(1) X = don't care

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### 6.14.23 Port P7 (P7.0 to P7.7) Input/Output With Schmitt Trigger (MSP430F67xxIPZ Only)

Figure 6-28 shows the port diagram. Table 6-86 summarizes the selection of the pin functions.

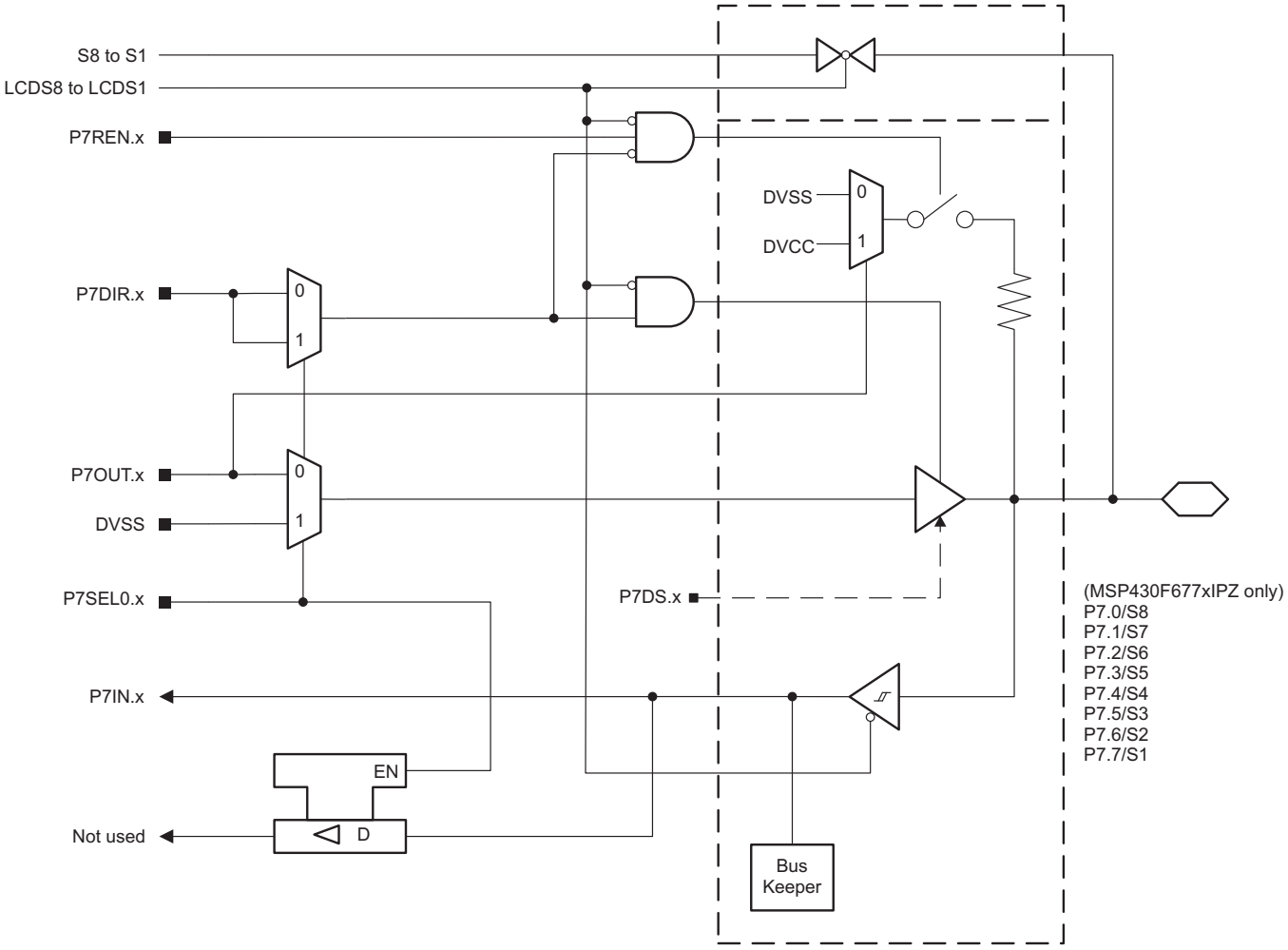



**Figure 6-28. Port P7 (P7.0 to P7.7) Diagram (MSP430F67xxIPZ Only)**


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**Table 6-86. Port P7 (P7.0 to P7.7) Pin Functions (MSP430F67xxIPZ Only)**

| PIN NAME (P7.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P7DIR.x | P7SEL0.x | LCD8 to LCD1 |
| P7.0/S8 | 0 | P7.0 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S8 | X | X | 1 |
| P7.1/S7 | 1 | P7.1 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S7 | X | X | 1 |
| P7.2/S6 | 2 | P7.2 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S6 | X | X | 1 |
| P7.3/S5 | 3 | P7.3 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S5 | X | X | 1 |
| P7.4/S4 | 4 | P7.4 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S4 | X | X | 1 |
| P7.5/S3 | 5 | P7.5 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S3 | X | X | 1 |
| P7.6/S2 | 6 | P7.6 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S2 | X | X | 1 |
| P7.7/S1 | 7 | P7.7 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S1 | X | X | 1 |

(1) X = don't care

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### 6.14.24 Port P8 (P8.0 to P8.7) Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

Figure 6-29 shows the port diagram. Table 6-87 summarizes the selection of the pin functions.

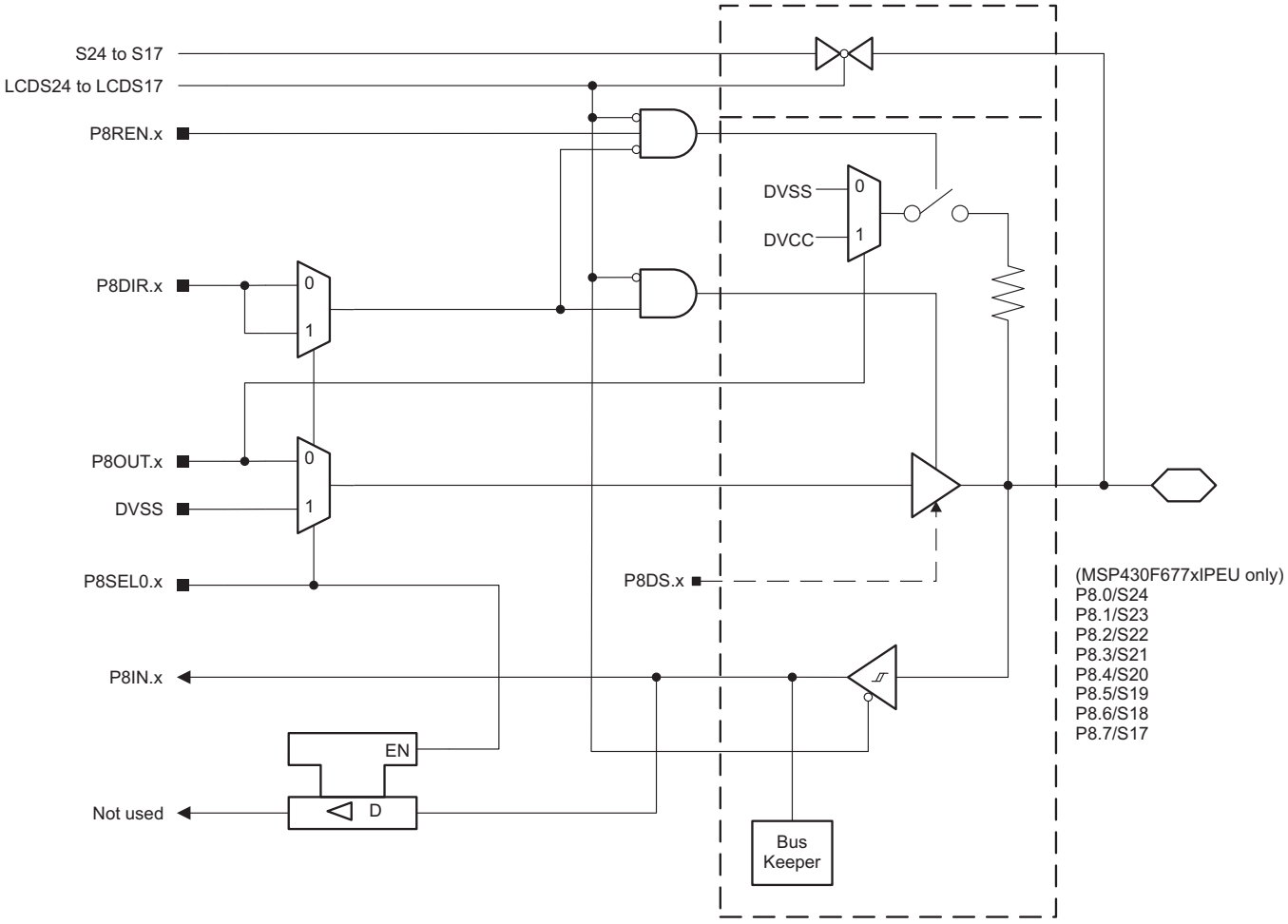



**Figure 6-29. Port P8 (P8.0 to P8.7) Diagram (MSP430F677xIPEU Only)**


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**Table 6-87. Port P8 (P8.0 to P8.7) Pin Functions (MSP430F677xIPEU Only)**

| PIN NAME (P8.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P8DIR.x | P8SEL0.x | LCD24 to LCD17 |
| P8.0/S24 | 0 | P8.0 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S24 | X | X | 1 |
| P8.1/S23 | 1 | P8.1 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S23 | X | X | 1 |
| P8.2/S22 | 2 | P8.2 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S22 | X | X | 1 |
| P8.3/S21 | 3 | P8.3 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S21 | X | X | 1 |
| P8.4/S20 | 4 | P8.4 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S20 | X | X | 1 |
| P8.5/S19 | 5 | P8.5 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S19 | X | X | 1 |
| P8.6/S18 | 6 | P8.6 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S18 | X | X | 1 |
| P8.7/S17 | 7 | P8.7 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S17 | X | X | 1 |

(1) X = don't care

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### 6.14.25 Port P8 (P8.0) Input/Output With Schmitt Trigger (MSP430F677xIPZ Only)

Figure 6-30 shows the port diagram. Table 6-88 summarizes the selection of the pin functions.

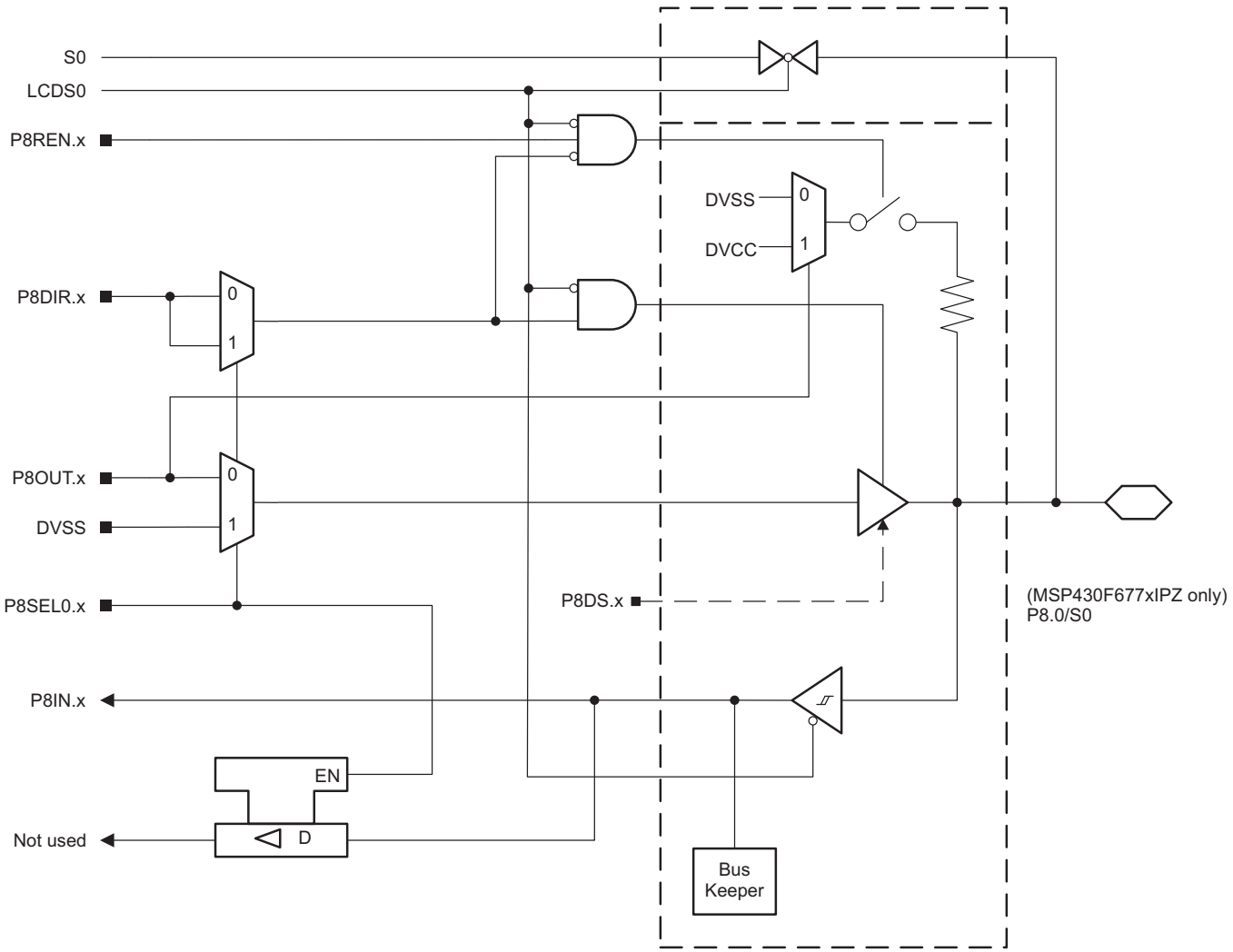



**Figure 6-30. Port P8 (P8.0) Diagram (MSP430F677xIPZ Only)**

**Table 6-88. Port P8 (P8.0) Pin Functions (MSP430F677xIPZ Only)**

| PIN NAME (P8.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P8DIR.x | P8SEL0.x | LCD0 |
| P8.0/S0 | 0 | P8.0 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S0 | X | X | 1 |

(1) X = don't care


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### 6.14.26 Port P8 (P8.1) Input/Output With Schmitt Trigger (MSP430F677xIPZ Only)

Figure 6-31 shows the port diagram. Table 6-89 summarizes the selection of the pin functions.

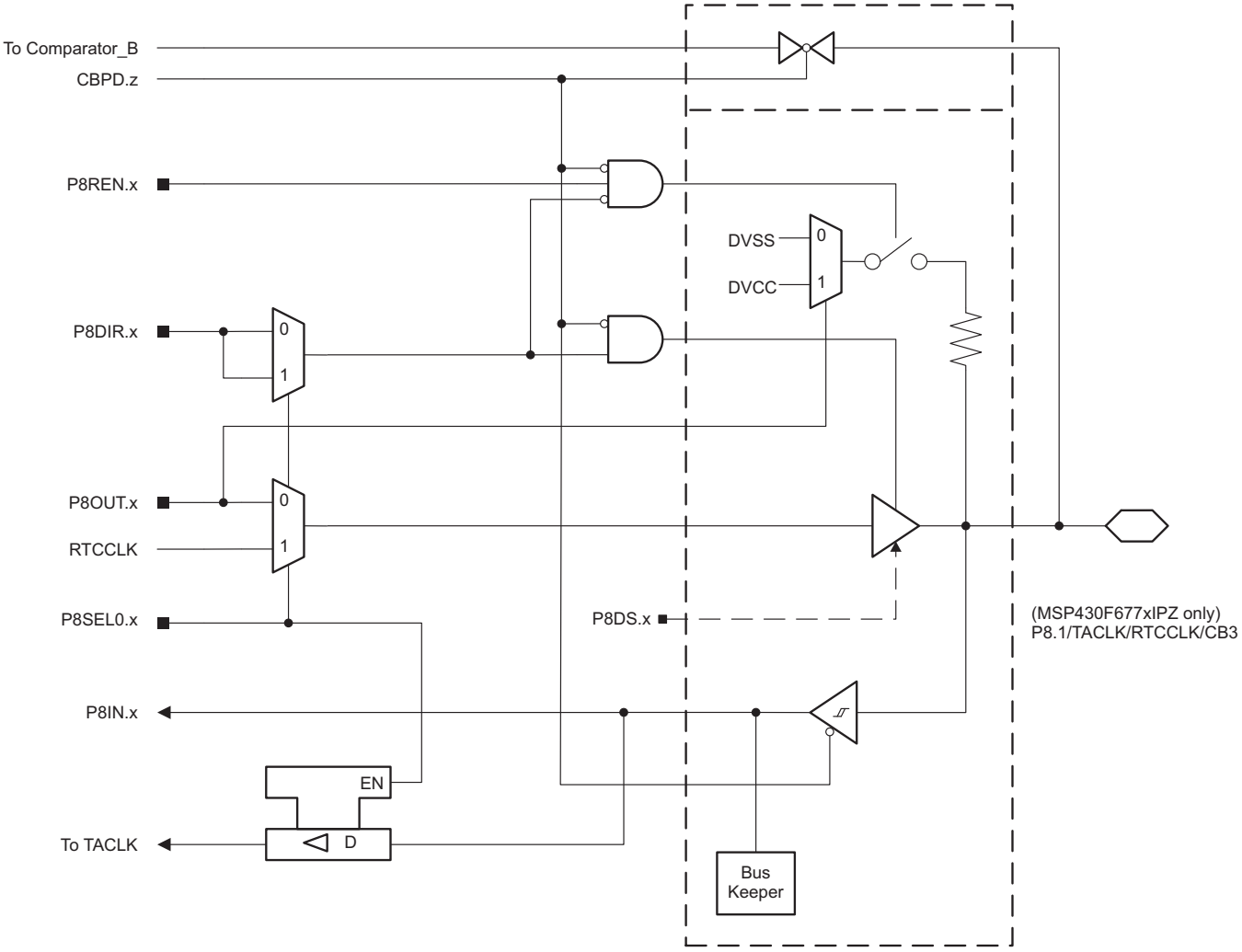



**Figure 6-31. Port P8 (P8.1) Diagram (MSP430F677xIPZ Only)**

**Table 6-89. Port P8 (P8.1) Pin Functions (MSP430F677xIPZ Only)**

| PIN NAME (P8.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P8DIR.x | P8SEL0.x | CBPD.z |
| P8.1/TACLK/RTCCLK/CB3 | 1 | P8.1 (I/O) | I:0; O:1 | 0 | 0 |
| | | TACLK | 0 | 1 | 0 |
| | | RTCCLK | 1 | 1 | 0 |
| | | CB3 | X | X | 1 (z = 3) |

(1) X = don't care

### 6.14.27 Port P9 (P9.0 to P9.7) Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

Figure 6-32 shows the port diagram. Table 6-90 summarizes the selection of the pin functions.

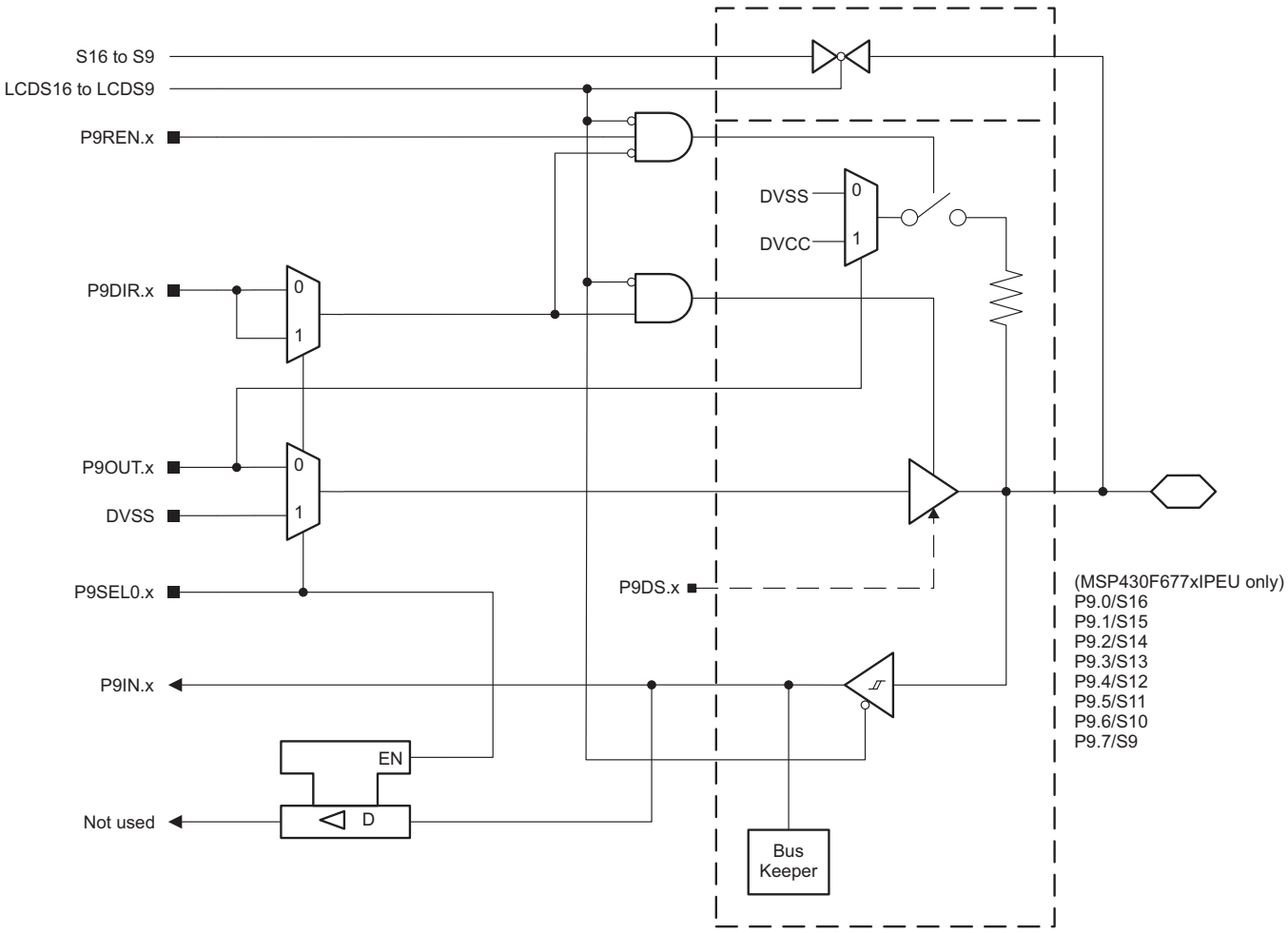



**Figure 6-32. Port P9 (P9.0 to P9.7) Diagram (MSP430F677xIPEU Only)**


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**Table 6-90. Port P9 (P9.0 to P9.7) Pin Functions (MSP430F677xIPEU Only)**

| PIN NAME (P9.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P9DIR.x | P9SEL0.x | LCD16 to LCD9 |
| P9.0/S16 | 0 | P9.0 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S16 | X | X | 1 |
| P9.1/S15 | 1 | P9.1 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S15 | X | X | 1 |
| P9.2/S14 | 2 | P9.2 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S14 | X | X | 1 |
| P9.3/S13 | 3 | P9.3 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S13 | X | X | 1 |
| P9.4/S12 | 4 | P9.4 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S12 | X | X | 1 |
| P9.5/S11 | 5 | P9.5 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S11 | X | X | 1 |
| P9.6/S10 | 6 | P9.6 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S10 | X | X | 1 |
| P9.7/S9 | 7 | P9.7 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S9 | X | X | 1 |

(1) X = don't care

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### 6.14.28 Port P10 (P10.0 to P10.7) Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

Figure 6-33 shows the port diagram. Table 6-91 summarizes the selection of the pin functions.

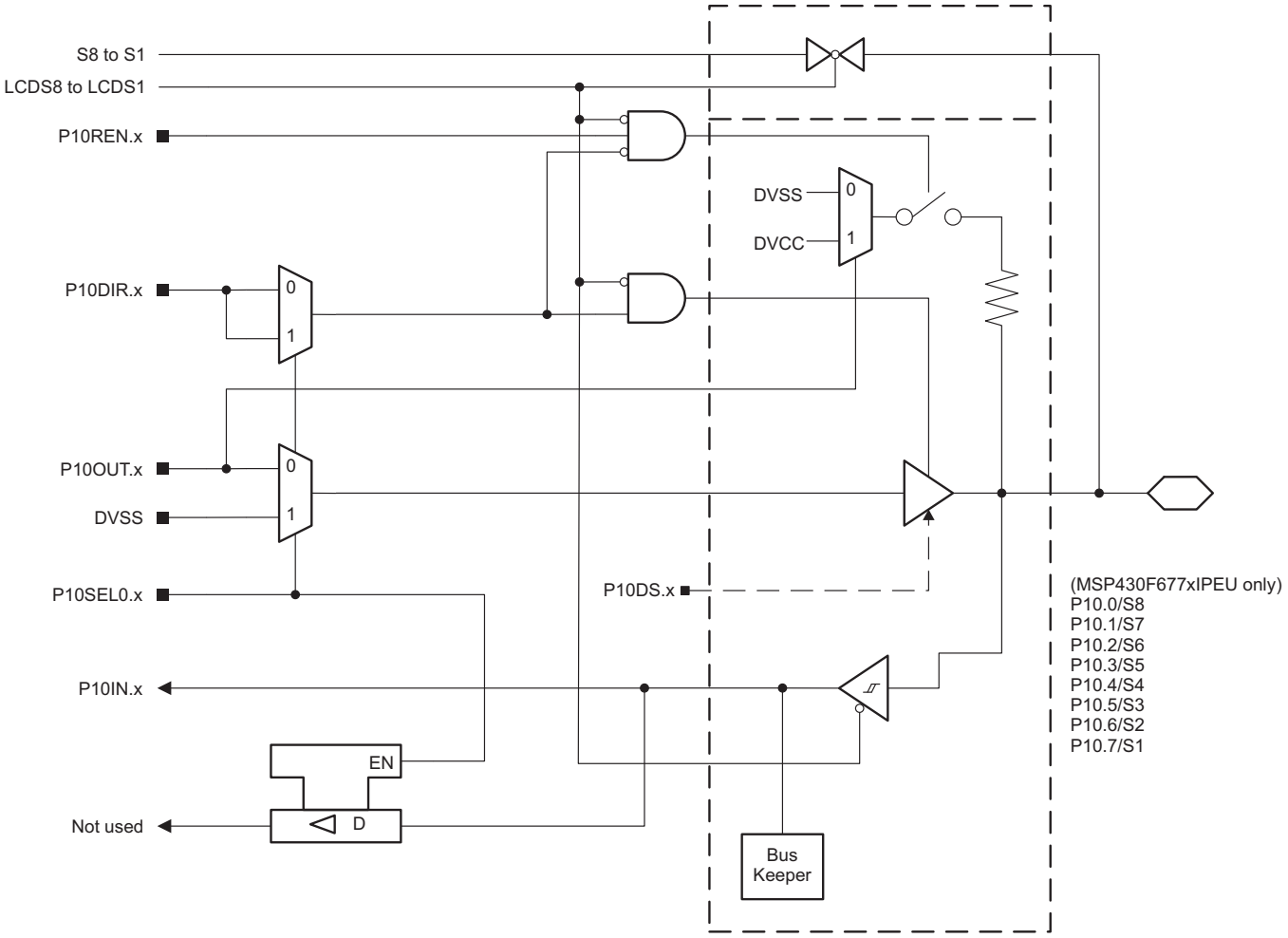



**Figure 6-33. Port P10 (P10.0 to P10.7) Diagram (MSP430F677xIPEU Only)**


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**Table 6-91. Port P10 (P10.0 to P10.7) Pin Functions (MSP430F677xIPEU Only)**

| PIN NAME (P10.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P10DIR.x | P10SEL0.x | LCD8 to LCD1 |
| P10.0/S8 | 0 | P10.0 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S8 | X | X | 1 |
| P10.1/S7 | 1 | P10.1 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S7 | X | X | 1 |
| P10.2/S6 | 2 | P10.2 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S6 | X | X | 1 |
| P10.3/S5 | 3 | P10.3 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S5 | X | X | 1 |
| P10.4/S4 | 4 | P10.4 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S4 | X | X | 1 |
| P10.5/S3 | 5 | P10.5 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S3 | X | X | 1 |
| P10.6/S2 | 6 | P10.6 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S2 | X | X | 1 |
| P10.7/S1 | 7 | P10.7 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S1 | X | X | 1 |

(1) X = don't care

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### 6.14.29 Port P11 (P11.0) Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

Figure 6-34 shows the port diagram. Table 6-92 summarizes the selection of the pin functions.

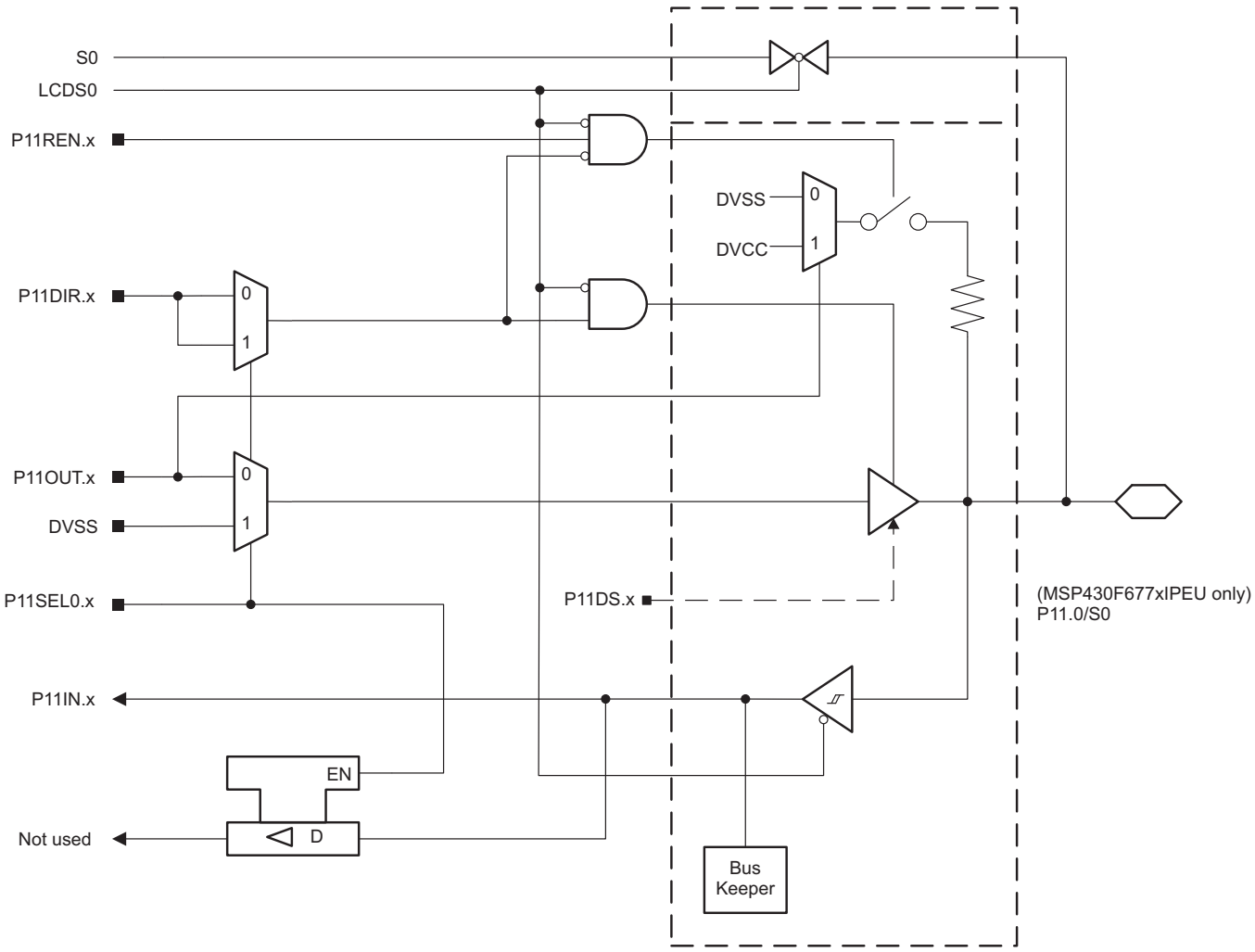



**Figure 6-34. Port P11 (P11.0) Diagram (MSP430F677xIPEU Only)**

**Table 6-92. Port P11 (P11.0) Pin Functions (MSP430F677xIPEU Only)**

| PIN NAME (P11.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P11DIR.x | P11SEL0.x | LCD0 |
| P11.0/S0 | 0 | P11.0 (I/O) | I:0; O:1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S0 | X | X | 1 |

(1) X = don't care


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### 6.14.30 Port P11 (P11.1) Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

Figure 6-35 shows the port diagram. Table 6-93 summarizes the selection of the pin functions.

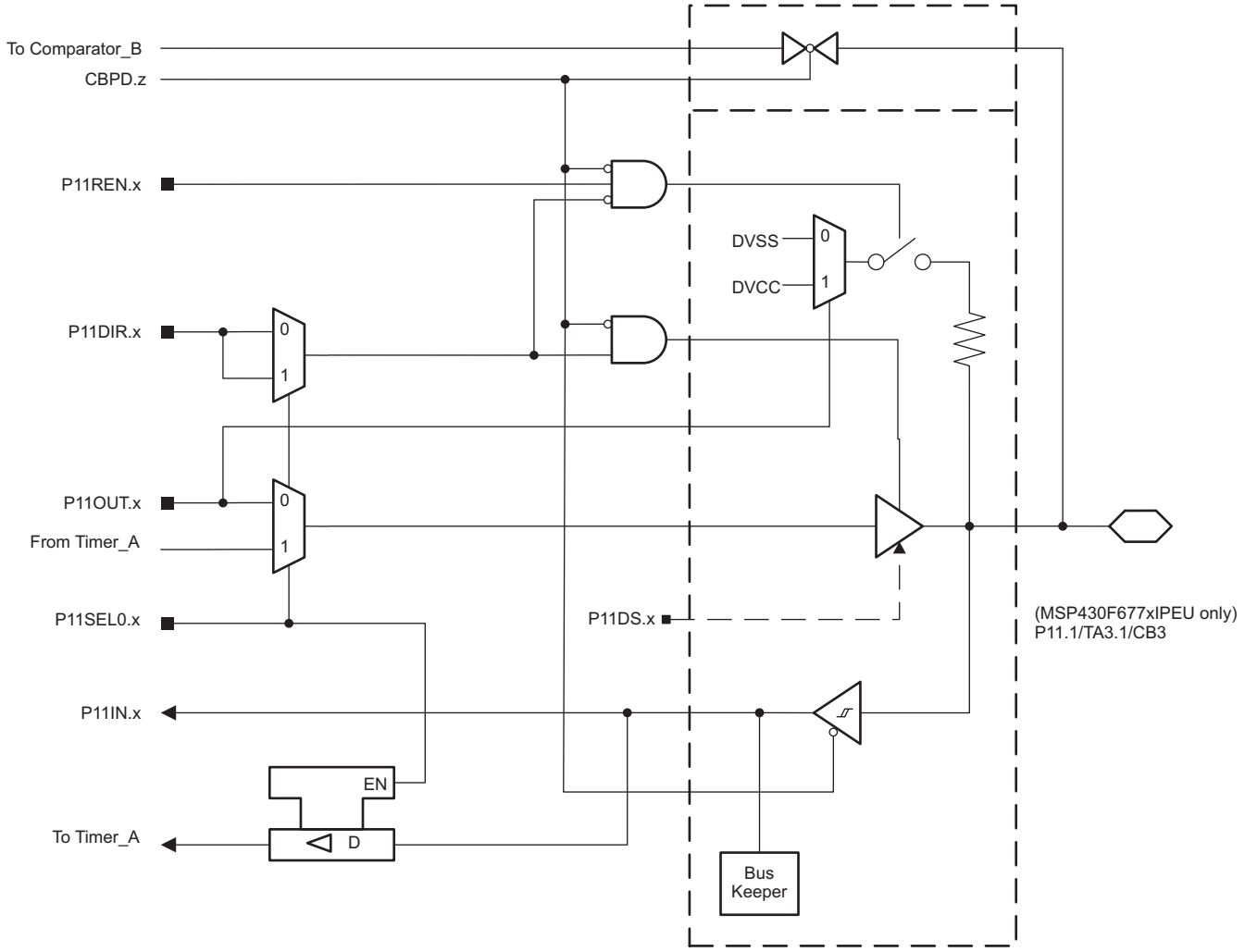



**Figure 6-35. Port P11 (P11.1) Diagram (MSP430F677xIPEU Only)**

**Table 6-93. Port P11 (P11.1) Pin Functions (MSP430F677xIPEU Only)**

| PIN NAME (P11.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P11DIR.x | P11SEL0.x | CBPD.z |
| P11.1/TA3.1/CB3 | 1 | P11.1 (I/O) | I:0; O:1 | 0 | 0 |
| | | TA3.CCI1A | 0 | 1 | 0 |
| | | TA3.1 | 1 | 1 | 0 |
| | | CB3 | X | X | 1 |

(1) X = don't care

### 6.14.31 Port P11 (P11.2 and P11.3) Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

Figure 6-36 shows the port diagram. Table 6-94 summarizes the selection of the pin functions.

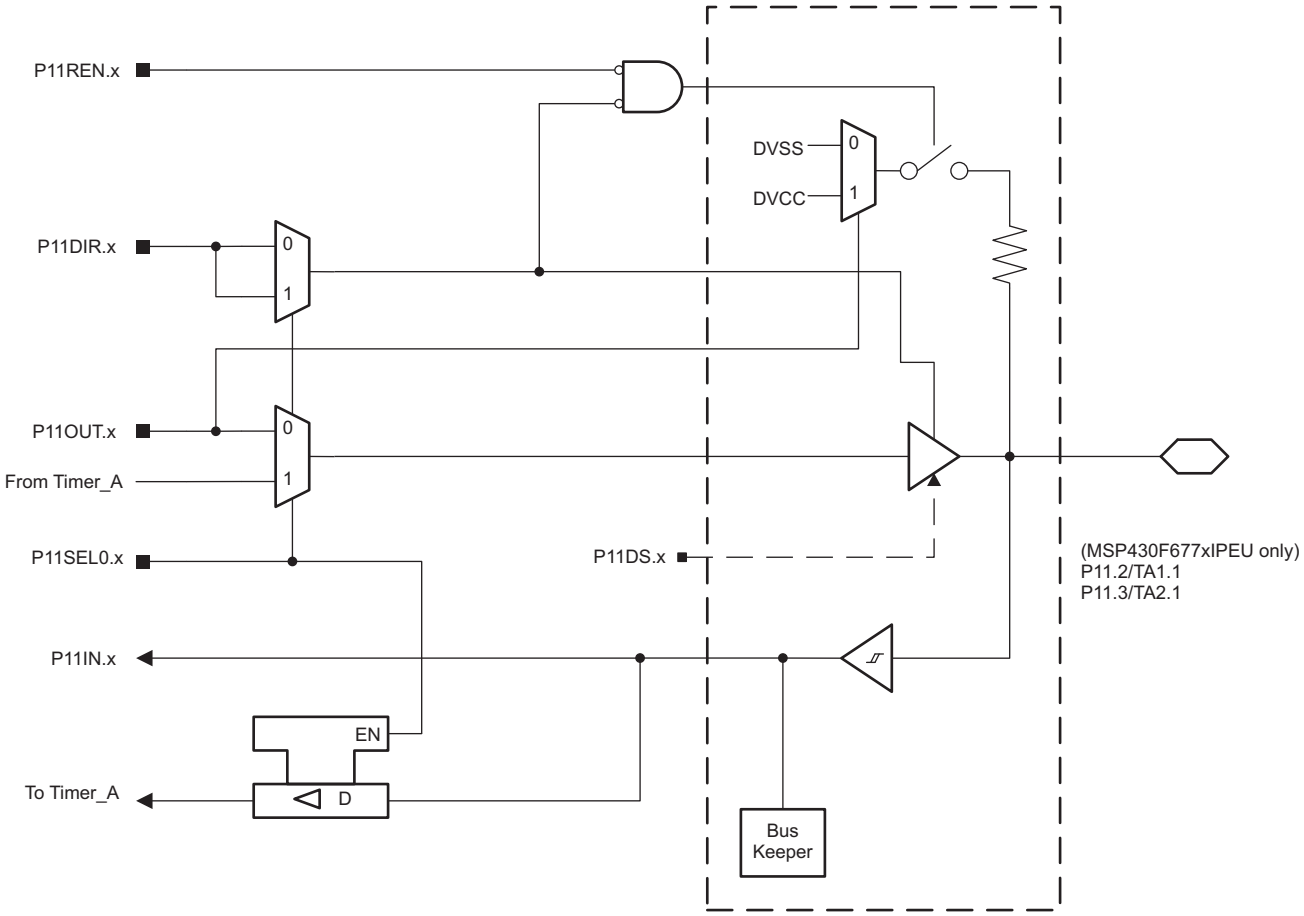



**Figure 6-36. Port P11 (P11.2 and P11.3) Diagram (MSP430F677xIPEU Only)**

**Table 6-94. Port P11 (P11.2 and P11.3) Pin Functions (MSP430F677xIPEU Only)**

| PIN NAME (P11.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | |
|---|---|---|---|---|
| | | | P11DIR.x | P11SEL0.x |
| P11.2/TA1.1 | 2 | P11.2 (I/O) | I:0; O:1 | 0 |
| | | TA1.CCI1A | 0 | 1 |
| | | TA1.1 | 1 | 1 |
| P11.3/TA2.1 | 3 | P11.3 (I/O) | I:0; O:1 | 0 |
| | | TA2.CCI1A | 0 | 1 |
| | | TA2.1 | 1 | 1 |


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### 6.14.32 Port P11 (P11.4 and P11.5) Input/Output With Schmitt Trigger (MSP430F677xIPEU Only)

Figure 6-37 shows the port diagram. Table 6-95 summarizes the selection of the pin functions.

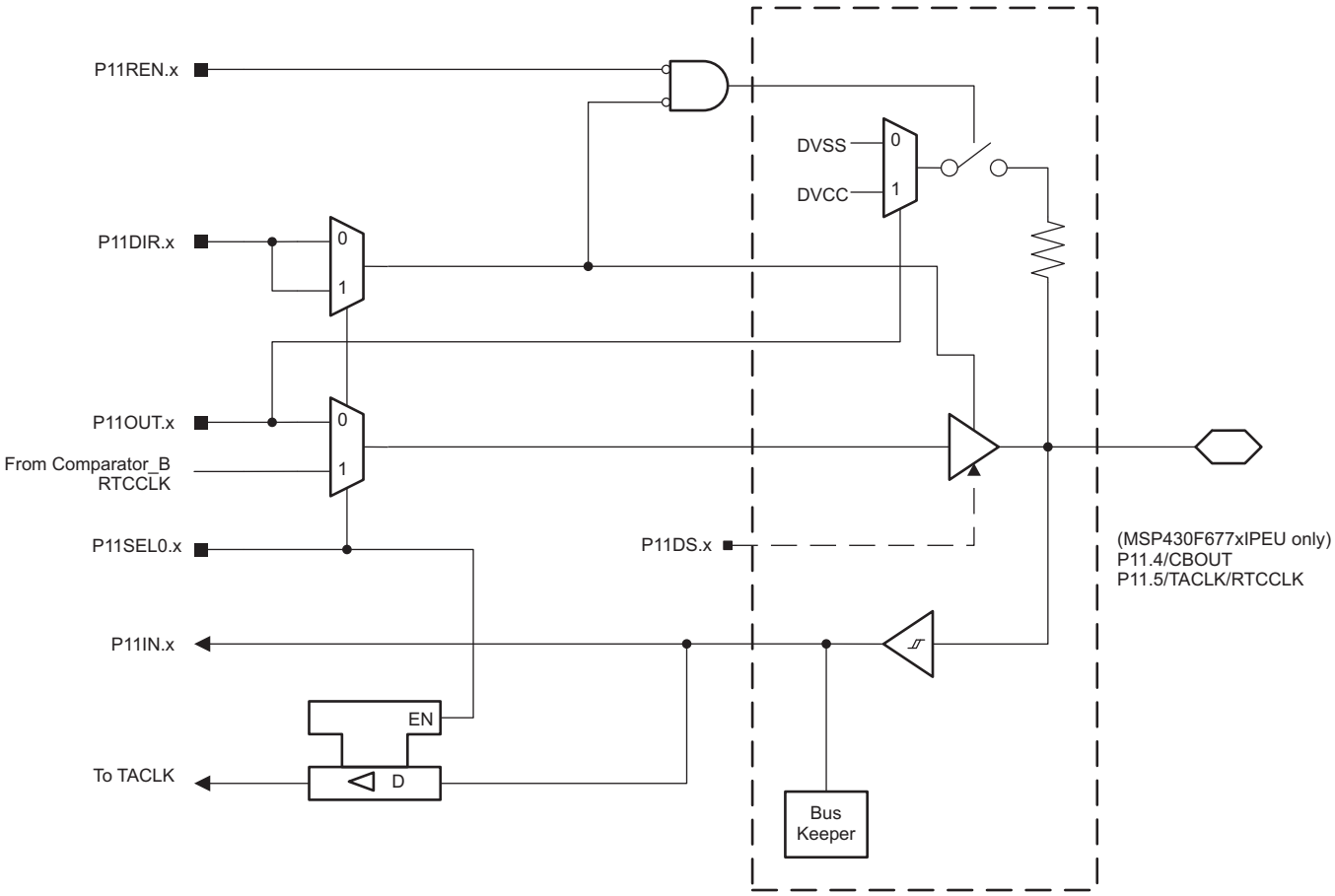



**Figure 6-37. Port P11 (P11.4 and P11.5) Diagram (MSP430F677xIPEU Only)**

**Table 6-95. Port P11 (P11.4 and P11.5) Pin Functions (MSP430F677xIPEU Only)**

| PIN NAME (P11.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | |
|---|---|---|---|---|
| | | | P11DIR.x | P11SEL0.x |
| P11.4/CBOUT | 4 | P11.4 (I/O) | I:0; O:1 | 0 |
| | | N/A | 0 | 1 |
| | | CBOUT | 1 | 1 |
| P11.5/TACLK/RTCCLK | 5 | P11.5 (I/O) | I:0; O:1 | 0 |
| | | TACLK | 0 | 1 |
| | | RTCCLK | 1 | 1 |

### 6.14.33 Port PJ (PJ.0) JTAG Pin TDO, Input/Output With Schmitt Trigger or Output

Figure 6-38 shows the port diagram. Table 6-96 summarizes the selection of the pin functions.

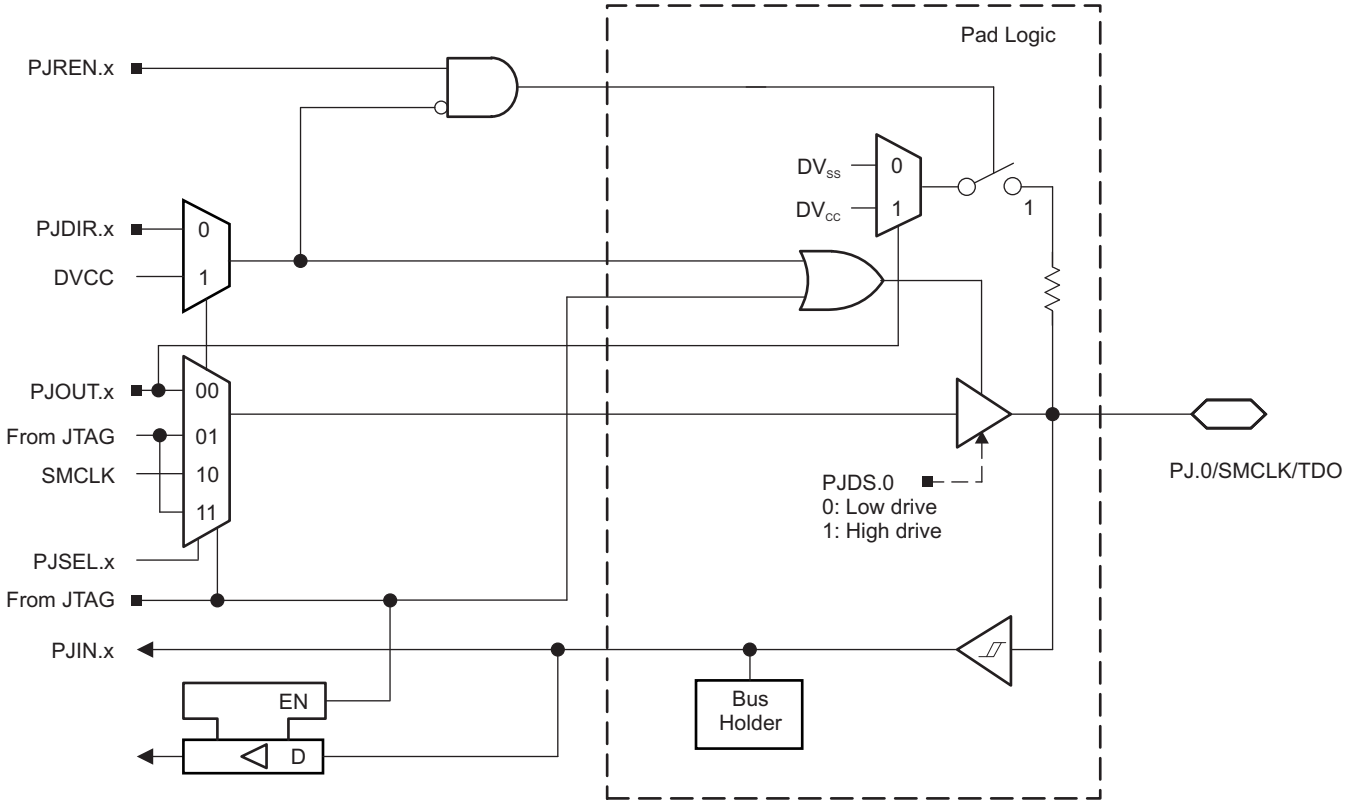



**Figure 6-38. Port PJ (PJ.0) Diagram**


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### 6.14.34 Port PJ (PJ.1 to PJ.3) JTAG Pins TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output

Figure 6-39 shows the port diagram. Table 6-96 summarizes the selection of the pin functions.

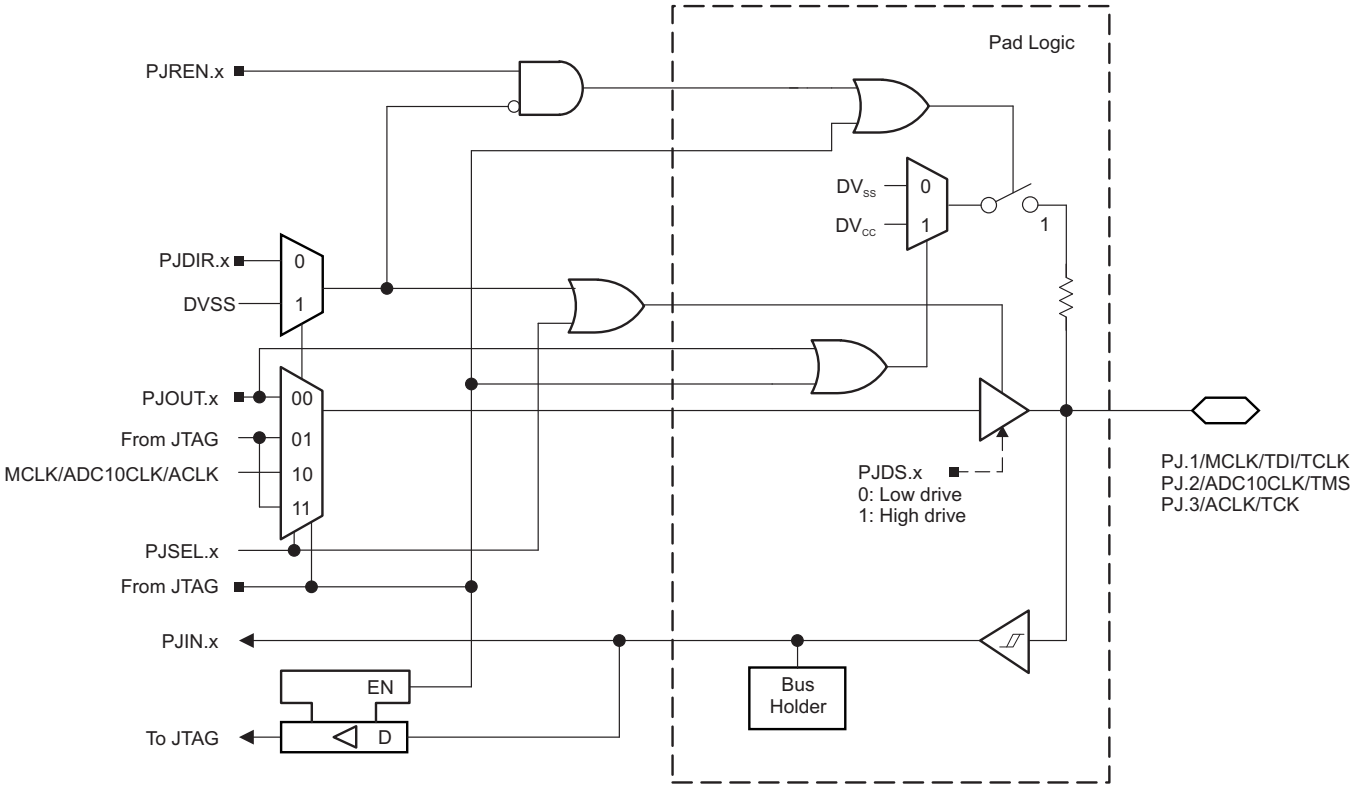



**Figure 6-39. Port PJ (PJ.1 to PJ.3) Diagram**

**Table 6-96. Port PJ (PJ.0 to PJ.3) Pin Functions**

| PIN NAME (PJ.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | PJDIR.x | PJSEL.x | JTAG MODE |
| PJ.0/SMCLK/TDO | 0 | PJ.0 (I/O)(2) | I: 0; O: 1 | 0 | 0 |
| | | SMCLK | 1 | 1 | 0 |
| | | TDO(3) | x | x | 1 |
| PJ.1/MCLK/TDI/TCLK | 1 | PJ.1 (I/O)(2) | I: 0; O: 1 | 0 | 0 |
| | | MCLK | 1 | 1 | 0 |
| | | TDI/TCLK(3) (4) | x | x | 1 |
| PJ.2/ADC10CLK/TMS | 2 | PJ.2 (I/O)(2) | I: 0; O: 1 | 0 | 0 |
| | | ADC10CLK | 1 | 1 | 0 |
| | | TMS(3) (4) | x | x | 1 |
| PJ.3/ACLK/TCK | 3 | PJ.3 (I/O)(2) | I: 0; O: 1 | 0 | 0 |
| | | ACLK | 1 | 1 | 0 |
| | | TCK(3) (4) | x | x | 1 |

(1) X = don't care
(2) Default condition
(3) The pin direction is controlled by the JTAG module.
(4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are don't care.

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## 6.15 Device Descriptors (TLV)

Table 6-97 lists the device descriptors for the MSP430F677x1 devices.

**Table 6-97. MSP430F677x1 Device Descriptors**

| DESCRIPTION | | ADDRESS | SIZE (BYTES) | VALUE | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | F67791IPEU F67791IPZ | F67781IPEU F67781IPZ | F67771IPEU F67771IPZ | F67761IPEU F67761IPZ | F67751IPEU F67751IPZ |
| Info Block | Info length | 1A00h | 1 | 06h | 06h | 06h | 06h | 06h |
| | CRC length | 1A01h | 1 | 06h | 06h | 06h | 06h | 06h |
| | CRC value | 1A02h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Device ID | 1A04h | 2 | 81A5h | 81A4h | 81A3h | 81A2h | 81A1h |
| | Hardware revision | 1A06h | 1 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Firmware revision | 1A07h | 1 | Per unit | Per unit | Per unit | Per unit | Per unit |
| Die Record | Die record tag | 1A08h | 1 | 08h | 08h | 08h | 08h | 08h |
| | Die record length | 1A09h | 1 | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah |
| | Lot ID | 1A0Ah | 4 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | X position | 1A0Eh | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Y position | 1A10h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Test record CP | 1A12h | 1 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Test record FT | 1A13h | 1 | Per unit | Per unit | Per unit | Per unit | Per unit |
| ADC10 Calibration | ADC calibration tag | 1A14h | 1 | 13h | 13h | 13h | 13h | 13h |
| | ADC calibration length | 1A15h | 1 | 10h | 10h | 10h | 10h | 10h |
| | ADC gain factor | 1A16h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC offset | 1A18h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 15T30 | 1A1Ah | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 15T85 | 1A1Ch | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 20T30 | 1A1Eh | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 20T85 | 1A20h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 25T30 | 1A22h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 25T85 | 1A24h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |


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Table 6-98 lists the device descriptors for the MSP430F676x1 devices.

**Table 6-98. MSP430F676x1 Device Descriptors**

| DESCRIPTION | | ADDRESS | SIZE (BYTES) | VALUE | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | F6769I1PEU F6769I1PZ | F67681IPEU F67681IPZ | F67671IPEU F67671IPZ | F67661IPEU F67661IPZ | F67651IPEU F67651IPZ |
| Info Block | Info length | 1A00h | 1 | 06h | 06h | 06h | 06h | 06h |
| | CRC length | 1A01h | 1 | 06h | 06h | 06h | 06h | 06h |
| | CRC value | 1A02h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Device ID | 1A04h | 2 | 81A0h | 819Fh | 819Eh | 819Dh | 819Ch |
| | Hardware revision | 1A06h | 1 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Firmware revision | 1A07h | 1 | Per unit | Per unit | Per unit | Per unit | Per unit |
| Die Record | Die record tag | 1A08h | 1 | 08h | 08h | 08h | 08h | 08h |
| | Die record length | 1A09h | 1 | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah |
| | Lot ID | 1A0Ah | 4 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | X position | 1A0Eh | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Y position | 1A10h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Test record CP | 1A12h | 1 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Test record FT | 1A13h | 1 | Per unit | Per unit | Per unit | Per unit | Per unit |
| ADC10 Calibration | ADC calibration tag | 1A14h | 1 | 13h | 13h | 13h | 13h | 13h |
| | ADC calibration length | 1A15h | 1 | 10h | 10h | 10h | 10h | 10h |
| | ADC gain factor | 1A16h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC offset | 1A18h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 15T30 | 1A1Ah | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 15T85 | 1A1Ch | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 20T30 | 1A1Eh | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 20T85 | 1A20h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 25T30 | 1A22h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 25T85 | 1A24h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |

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Table 6-99 lists the device descriptors for the MSP430F674x1 devices.

**Table 6-99. MSP430F674x1 Device Descriptor Table**

| DESCRIPTION | | ADDRESS | SIZE (BYTES) | VALUE | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | F67491IPEU F67491IPZ | F67481IPEU F67481IPZ | F67471IPEU F67471IPZ | F67461IPEU F67461IPZ | F67451IPEU F67451IPZ |
| Info Block | Info length | 1A00h | 1 | 06h | 06h | 06h | 06h | 06h |
| | CRC length | 1A01h | 1 | 06h | 06h | 06h | 06h | 06h |
| | CRC value | 1A02h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Device ID | 1A04h | 2 | 819Bh | 819Ah | 8199h | 8198h | 8197h |
| | Hardware revision | 1A06h | 1 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Firmware revision | 1A07h | 1 | Per unit | Per unit | Per unit | Per unit | Per unit |
| Die Record | Die record tag | 1A08h | 1 | 08h | 08h | 08h | 08h | 08h |
| | Die record length | 1A09h | 1 | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah |
| | Lot ID | 1A0Ah | 4 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | X position | 1A0Eh | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Y position | 1A10h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Test record CP | 1A12h | 1 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Test record FT | 1A13h | 1 | Per unit | Per unit | Per unit | Per unit | Per unit |
| ADC10 Calibration | ADC calibration tag | 1A14h | 1 | 13h | 13h | 13h | 13h | 13h |
| | ADC calibration length | 1A15h | 1 | 10h | 10h | 10h | 10h | 10h |
| | ADC gain factor | 1A16h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC offset | 1A18h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 15T30 | 1A1Ah | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 15T85 | 1A1Ch | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 20T30 | 1A1Eh | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 20T85 | 1A20h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 25T30 | 1A22h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 25T85 | 1A24h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit |


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# 7 器件和文档支持

## 7.1 入门和后续步骤

有关 MSP430™系列器件以及开发协助工具和库的更多信息，请访问入门页面。

## 7.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices. Each MSP MCU commercial family member has one of two prefixes: MSP or XMS. These prefixes represent evolutionary stages of product development from engineering prototypes (XMS) through fully qualified production devices (MSP).

**XMS** – Experimental device that is not necessarily representative of the final device's electrical specifications

**MSP** – Fully qualified production device

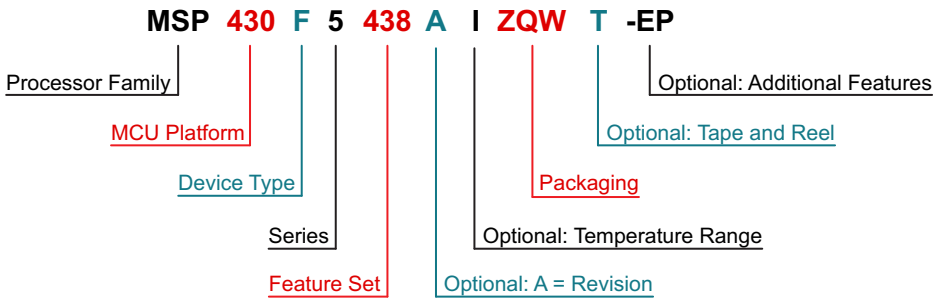
XMS devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. 图 7-1 provides a legend for reading the complete device name.




| | | |
|---|---|---|
| **Processor Family** | CC = Embedded RF Radio<br>MSP = Mixed-Signal Processor<br>XMS = Experimental Silicon<br>PMS = Prototype Device | |
| **MCU Platform** | 430 = MSP430 low-power microcontroller platform | |
| **Device Type** | **Memory Type**<br>C = ROM<br>F = Flash<br>FR = FRAM<br>G = Flash or FRAM (Value Line)<br>L = No Nonvolatile Memory | **Specialized Application**<br>AFE = Analog Front End<br>BQ = Contactless Power<br>CG = ROM Medical<br>FE = Flash Energy Meter<br>FG = Flash Medical<br>FW = Flash Electronic Flow Meter |
| **Series** | 1 = Up to 8 MHz<br>2 = Up to 16 MHz<br>3 = Legacy<br>4 = Up to 16 MHz with LCD | 5 = Up to 25 MHz<br>6 = Up to 25 MHz with LCD<br>0 = Low-Voltage Series |
| **Feature Set** | Various levels of integration within a series | |
| **Optional: A = Revision** | N/A | |
| **Optional: Temperature Range** | S = 0°C to 50°C<br>C = 0°C to 70°C<br>I = –40°C to 85°C<br>T = –40°C to 105°C | |
| **Packaging** | http://www.ti.com/packaging | |
| **Optional: Tape and Reel** | T = Small reel<br>R = Large reel<br>No markings = Tube or tray | |
| **Optional: Additional Features** | -EP = Enhanced Product (–40°C to 105°C)<br>-HT = Extreme Temperature Parts (–55°C to 150°C)<br>-Q1 = Automotive Q100 Qualified | |

图 **7-1. Device Nomenclature**


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## 7.3 工具与软件

所有 MSP 微控制器均受多种软件和硬件开发工具的支持。相关工具由 TI 以及多家第三方供应商提供。请参阅《MSP430 超低功耗 MCU – 工具与软件》，了解所有工具。

表 7-1 列出 了 MSP430F677x1、MSP430F676x1 和 MSP430F674x1 MCU 的调试功能。关于可用特性的详细信息，请参见《*适用于 MSP430 的 Code Composer Studio 用户指南*》。

**表 7-1. 硬件调试 特性**

| MSP430 架构 | 四线制 JTAG | 两线制 JTAG | 断点 (N) | 范围断点 | 时钟控制 | 状态序列发生器 | 跟踪缓冲器 | LPMx.5 调试支持 |
|---|---|---|---|---|---|---|---|---|
| MSP430Xv2 | 有 | 有 | 3 | 有 | 是 | 否 | 否 | 有 |

设计套件与评估模块

**EVM430-F6779 - 用于计量的三相电子电表** 该 EVM430-F6779 是一款基于 MSP430F6779 器件的三相电表评估板。该电表支持三种电压和三种电流的输入，具有可设置防篡改功能的附加连接。

**适用于 MSP430F6x MCU 的 128 引脚目标开发板和 MSP-FET 编程器捆绑包** MSP-FET430U128 是一款强大的闪存仿真工具，可在 MSP430 MCU 上快速开始应用开发。它包含 USB 调试接口，用于通过 JTAG 接口或节省引脚的 Spy-Bi-Wire（两线制 JTAG）协议在系统内对 MSP430 进行编程和调试。

软件

**MSP430Ware™ 软件** MSP430Ware 软件集合了所有 MSP430 器件的代码示例、数据表以及其他设计资源，打包提供给用户。除了提供已有 MSP430 设计资源的完整集合外，MSP430Ware 软件还包含名为 MSP 驱动程序库的高级 API。借助该库可以轻松地对 MSP430 硬件进行编程。MSP430Ware 软件以 CCS 组件或独立软件包两种形式提供。

**适用于 MSP430 MCU 的电能测量设计中心** 电能测量设计中心是一款快速开发工具，它使用 TI MSP430i20xx 和 MSP430F67xx 基于闪存的微控制器 (MCU) 实现电能测量。它包含能够在各种电源监控和电能测量应用（包括智能电网和楼宇自动化）中简化开发和加快设计的图形用户界面 (GUI)、文档、 软件库和示例。使用设计中心，您无需编写任何代码即可配置、校准并查看结果。

**IEC60730 软件包** IEC60730 MSP430 软件包经过专门开发，用于协助客户达到 IEC 60730-1:2010（家用及类似用途的自动化电气控制 - 第 1 部分：一般要求）B 类产品的要求。其中涵盖家用电器、电弧检测器、电源转换器、电动工具、电动自行车及其他诸多产品。IEC60730 MSP430 软件包可以嵌入在 MSP430 MCU 中 运行的客户应用， 从而帮助客户简化其消费类器件在功能安全方面遵循 IEC 60730-1:2010 B 类规范的认证工作。

**MSP 驱动程序库** MSP 驱动程序库的抽象 API 提供易用的函数调用，无需直接操纵 MSP430 硬件的位与字节。完整的文档通过具有帮助意义的 API 指南交付，其中包括有关每个函数调用和经过验证的参数的详细信息。开发人员可使用驱动程序库函数以尽可能低的费用编写全部项目。

**MSP430F677x(1)、MSP430F676x(1)、MSP430F674x(1) 代码示例** 根据不同应用需求配置各集成外设的每个 MSP 器件均具备相应的 C 代码示例。

**电容式触摸软件库** 可在 MSP430 MCU 启用电容触控功能的免费 C 代码库。MSP430 MCU 库版本 采用 多种电容触控实现方法，包括 RO 和 RC 方法。

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**MSP EnergyTrace™ 技术** 适用于 MSP430 微控制器的 EnergyTrace 技术是基于电能的代码分析工具，适用于测量和显示应用的电能系统配置并帮助优化应用以实现超低功耗。

**ULP（超低功耗）Advisor** ULP Advisor™软件是一款辅助工具，旨在指导开发人员编写更为高效的代码，从而充分利用 MSP430 和 MSP432 微控制器 独特 功能。ULP Advisor 的目标人群是微控制器的资深开发者和开发新手，可以根据详尽的 ULP 检验表检查代码，以便最大限度地减少应用程序的能耗。在编译时，ULP Advisor 会提供通知和备注以突出显示代码中可以进一步优化的区域，进而实现更低功耗。

适用于 **MSP** 的定点数学库 MSP IQmath 和 Qmath 库是为 C 语言开发者提供的一套经过高度优化的高精度数学运算函数集合，能够将浮点算法无缝嵌入 MSP430 和 MSP432 器件的定点代码中。这些例程通常用于计算密集型实时 应用， 而优化的执行速度、高精度以及超低能耗通常是影响这些实时应用的关键因素。与使用浮点数学算法编写的同等代码相比，使用 IQmath 和 Qmath 库可以大幅提高执行速度并显著降低能耗。

适用于 **MSP430** 的浮点数学运算库 TI 在低功耗和低成本微控制器领域锐意创新，为您提供 MSPMATHLIB。此标量函数的浮点数学运算库，能够充分利用器件的智能外设，使速度最高达到标准 MSP430 数学函数的 26 倍。Mathlib 能够轻松集成到您的设计中。该运算库免费使用并集成在 Code Composer Studio IDE 和 IAR Embedded Workbench IDE 中。

开发工具

适用于 **MSP** 微控制器的 **Code Composer Studio™** 集成开发环境 Code Composer Studio (CCS) 集成开发环境 (IDE) 支持所有 MSP 微控制器器件。CCS 包含一整套用于开发和调试嵌入式 应用的工具。它包含了优化的 C/C++ 编译器、源代码编辑器、项目构建环境、调试器、描述器以及其他多种 功能。

命令行编程器 MSP Flasher 是一款基于 shell 的开源接口，可使用 JTAG 或 Spy-Bi-Wire (SBW) 通信通过 FET 编程器或 eZ430 对 MSP 微控制器进行编程。MSP Flasher 可用于将二进制文件（.txt 或 .hex 文件）直接下载到 MSP 微控制器，而无需使用 IDE。

**MSP MCU** 编程器和调试器 MSP-FET 是一款强大的仿真开发工具（通常称为调试探针），可帮助用户在 MSP 低功耗微控制器 (MCU) 中快速开发应用。创建 MCU 软件通常需要将生成的二进制程序下载到 MSP 器件中，从而进行验证和调试。

**MSP-GANG** 生产编程器 MSP Gang 编程器是一款 MSP430 或 MSP432 器件编程器，可同时对多达八个完全相同的 MSP430 或 MSP432 闪存或 FRAM 器件进行编程。MSP Gang 编程器可使用标准的 RS-232 或 USB 连接与主机 PC 相连并提供灵活的编程选项，允许用户完全自定义流程。


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## 7.4 文档支持

以下文档对 MSP430F677x1、MSP430F676x1 和 MSP430F674x1 MCU 进行了介绍。www.ti.com.cn 网站上提供了这些文档的副本。

### 接收文档更新通知

要接收文档更新通知（包括芯片勘误表），请转至 ti.com.cn 上您的器件对应的产品文件夹（关于产品文件夹的链接，请参见节 7.5）。请单击右上角的“通知我”按钮。点击注册后，即可收到产品信息更改每周摘要（如有）。有关更改的详细信息，请查阅已修订文档的修订历史记录。

### 勘误

**《MSP430F67791 器件勘误表》** 介绍功能规格的已知例外情况。

**《MSP430F67781 器件勘误表》** 介绍功能规格的已知例外情况。

**《MSP430F67771 器件勘误表》** 介绍功能规格的已知例外情况。

**《MSP430F67761 器件勘误表》** 介绍功能规格的已知例外情况。

**《MSP430F67751 器件勘误表》** 介绍功能规格的已知例外情况。

**《MSP430F67691 器件勘误表》** 介绍功能规格的已知例外情况。

**《MSP430F67681 器件勘误表》** 介绍功能规格的已知例外情况。

**《MSP430F67671 器件勘误表》** 介绍功能规格的已知例外情况。

**《MSP430F67661 器件勘误表》** 介绍功能规格的已知例外情况。

**《MSP430F67651 器件勘误表》** 介绍功能规格的已知例外情况。

**《MSP430F67491 器件勘误表》** 介绍功能规格的已知例外情况。

**《MSP430F67481 器件勘误表》** 介绍功能规格的已知例外情况。

**《MSP430F67471 器件勘误表》** 介绍功能规格的已知例外情况。

**《MSP430F67461 器件勘误表》** 介绍功能规格的已知例外情况。

**《MSP430F67451 器件勘误表》** 介绍功能规格的已知例外情况。

### 用户指南

**《MSP430x5xx 和 MSP430x6xx 系列用户指南》** 详细介绍了该器件系列提供的模块和外设。

**《MSP430™ 闪存器件引导加载程序 (BSL) 用户指南》** MSP430 引导加载程序（bootloader，简称 BSL，以前称为 bootstrap loader）允许用户在原型设计、最终生产和投用阶段与 MSP430 微控制器中的嵌入式存储器进行通信。可编程存储器（闪存）和数据存储器 (RAM) 能够按照要求进行变更。不要将此处的引导加载程序与某些数字信号处理器 (DSP) 中将外部存储器中的程序代码（和数据）自动加载到 DSP 内部存储器的引导装载程序混为一谈。

**《通过 JTAG 接口对 MSP430 进行编程》** 此文档介绍了使用 JTAG 通信端口擦除、编程和验证基于 MSP430 闪存和 FRAM 的微控制器系列的存储器模块所需的功能。此外，该文档还介绍了如何编程所有 MSP430 器件上均具备的 JTAG 访问安全保险丝。此文档介绍了使用标准四线制 JTAG 接口和两线制 JTAG 接口（也称为 Spy-Bi-Wire (SBW)）的器件访问。

**《MSP430 硬件工具用户指南》** 此手册介绍了 TI MSP-FET430 闪存仿真工具 (FET) 的硬件。FET 是针对 MSP430 超低功耗微控制器的程序开发工具。文中对提供的接口类型，即并行端口接口和 USB 接口进行了说明。

应用报告

**《使用 MSP430F677x(A) 实施三相电子电表》** 该应用报告介绍了如何使用德州仪器 (TI) MSP430F677x(A) 计量处理器实现三相电子电表。该应用报告包含有关此单芯片实现的计量软件、硬件程序的必要信息。

**《使用 TI 的 DLMS COSEM 库》** 该应用报告详细介绍了如何使用德州仪器 (TI) 为在计量应用中使用 TI 微控制器的客户 开发的 DLMS COSEM 库。该库作为目标代码提供，具有易于使用的配置文件。可以通过联系区域销售和营销办事处获得该库。

**《MSP430F67xx 与 MSP430F67xxA 器件之间的差异》** 该应用报告介绍了非 A MSP430F67xx 器件对 MSP430F67xxA 器件的增强功能。该应用报告介绍了在 MSP430F67xxA 中修复的 MSP430F67xx 勘误表以及向 MSP430F67xxA 器件 添加的 其他功能。此外，还比较了计量结果，以进一步展示 MSP430F67xxA 器件中实现的更改不会影响计量性能。

**《MSP430 32kHz 晶体振荡器》** 对于稳定的晶体振荡器，选择合适的晶振、正确的负载电路和适当的电路板布局布线至关重要。该应用报告总结了晶体振荡器的功能，介绍了用于选择合适的晶体以实现 MSP430 超低功耗运行的参数。此外，还给出了正确电路板布局的提示和示例。此外，为了确保振荡器在大规模生产后能够稳定运行，还可能需要进行一些振荡器测试，该文档中提供了有关这些测试的详细信息。

**《MSP430 系统级 ESD 注意事项》** 随着硅晶技术向更低电压方向发展以及设计具有成本效益的超低功耗组件的需求的出现，系统级 ESD 要求变得越来越苛刻。该应用报告介绍了三个不同的 ESD 主题，旨在帮助电路板设计人员和 OEM 理解并设计出稳健耐用的系统级设计。

**《使用 MSP430 和段式 LCD 进行设计》** 从智能电表，到电子货架标签 (ESL)，再到医疗设备，各式各样的应用 都需要使用段式液晶显示屏 (LCD) 为用户 提供相关信息。部分 MSP430™ 微控制器系列内置低功耗 LCD 驱动电路，MSP430 MCU 借此能够直接控制段式 LCD 玻璃。本应用手册可帮助您理解段式 LCD 的工作原理、MSP430 MCU 系列各种 LCD 模块的不同特性， 并提供了 LCD 硬件布线技巧、编写高效易用的 LCD 驱动软件的相关指导以及 具有不同 LCD 特性的 MSP430 器件的 产品组合概述， 旨在协助您进行器件选型。


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## 7.5 相关链接

表 7-2 列出了快速访问链接。类别包括技术文档、支持与社区资源、工具与软件，以及申请样片或购买产品的快速链接。

表 7-2. 相关链接

| 器件 | 产品文件夹 | 立即订购 | 技术文档 | 工具与软件 | 支持和社区 |
|---|---|---|---|---|---|
| MSP430F67791 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430F67781 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430F67771 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430F67761 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430F67751 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430F67691 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430F67681 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430F67671 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430F67661 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430F67651 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430F67491 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430F67481 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430F67471 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430F67461 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430F67451 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |

## 7.6 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参见 TI 的 《使用条款》 。

TI E2E™ 社区
*TI 的工程师交流 (E2E) 社区*. 此社区的创建目的是为了促进工程师之间协作。在 e2e.ti.com 中，您可以提问、共享知识、拓展思路，在同领域工程师的帮助下解决问题。

TI 嵌入式处理器维基网页
*德州仪器 (TI) 嵌入式处理器维基网页*。此网站的建立是为了帮助开发人员熟悉德州仪器 (TI) 的嵌入式处理器，并且也为了促进与这些器件相关的硬件和软件的总体知识的创新和增长。

## 7.7 商标

MSP430, MSP430Ware, EnergyTrace, ULP Advisor, 适用于 MSP 微控制器的 Code Composer Studio, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

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## 7.8 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 7.9 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

## 7.10 Glossary

**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.


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# 8 机械，封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430F67451IPEU | ACTIVE | LQFP | PEU | 128 | 72 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67451 | Samples |
| MSP430F67451IPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67451 | Samples |
| MSP430F67461IPEU | ACTIVE | LQFP | PEU | 128 | 72 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67461 | Samples |
| MSP430F67461IPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67461 | Samples |
| MSP430F67471IPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67471 | Samples |
| MSP430F67471IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67471 | Samples |
| MSP430F67481IPEU | ACTIVE | LQFP | PEU | 128 | 72 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67481 | Samples |
| MSP430F67481IPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67481 | Samples |
| MSP430F67491IPEU | ACTIVE | LQFP | PEU | 128 | 72 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67491 | Samples |
| MSP430F67491IPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67491 | Samples |
| MSP430F67651IPEU | ACTIVE | LQFP | PEU | 128 | 72 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67651 | Samples |
| MSP430F67651IPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67651 | Samples |
| MSP430F67651IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67651 | Samples |
| MSP430F67661IPEU | ACTIVE | LQFP | PEU | 128 | 72 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67661 | Samples |
| MSP430F67661IPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67661 | Samples |
| MSP430F67671IPEU | ACTIVE | LQFP | PEU | 128 | 72 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67671 | Samples |
| MSP430F67671IPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67671 | Samples |
| MSP430F67681IPEU | ACTIVE | LQFP | PEU | 128 | 72 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67681 | Samples |
| MSP430F67681IPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67681 | Samples |
| MSP430F67681IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67681 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430F67691IPEU | ACTIVE | LQFP | PEU | 128 | 72 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67691 | Samples |
| MSP430F67691IPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67691 | Samples |
| MSP430F67691IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67691 | Samples |
| MSP430F67751IPEU | ACTIVE | LQFP | PEU | 128 | 72 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67751 | Samples |
| MSP430F67751IPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67751 | Samples |
| MSP430F67751IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67751 | Samples |
| MSP430F67761IPEU | ACTIVE | LQFP | PEU | 128 | 72 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67761 | Samples |
| MSP430F67761IPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67761 | Samples |
| MSP430F67771IPEU | ACTIVE | LQFP | PEU | 128 | 72 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67771 | Samples |
| MSP430F67771IPEUR | ACTIVE | LQFP | PEU | 128 | 750 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67771 | Samples |
| MSP430F67771IPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67771 | Samples |
| MSP430F67781IPEU | ACTIVE | LQFP | PEU | 128 | 72 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67781 | Samples |
| MSP430F67781IPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67781 | Samples |
| MSP430F67791IPEU | ACTIVE | LQFP | PEU | 128 | 72 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67791 | Samples |
| MSP430F67791IPEUR | ACTIVE | LQFP | PEU | 128 | 750 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67791 | Samples |
| MSP430F67791IPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67791 | Samples |
| MSP430F67791IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F67791 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2) RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

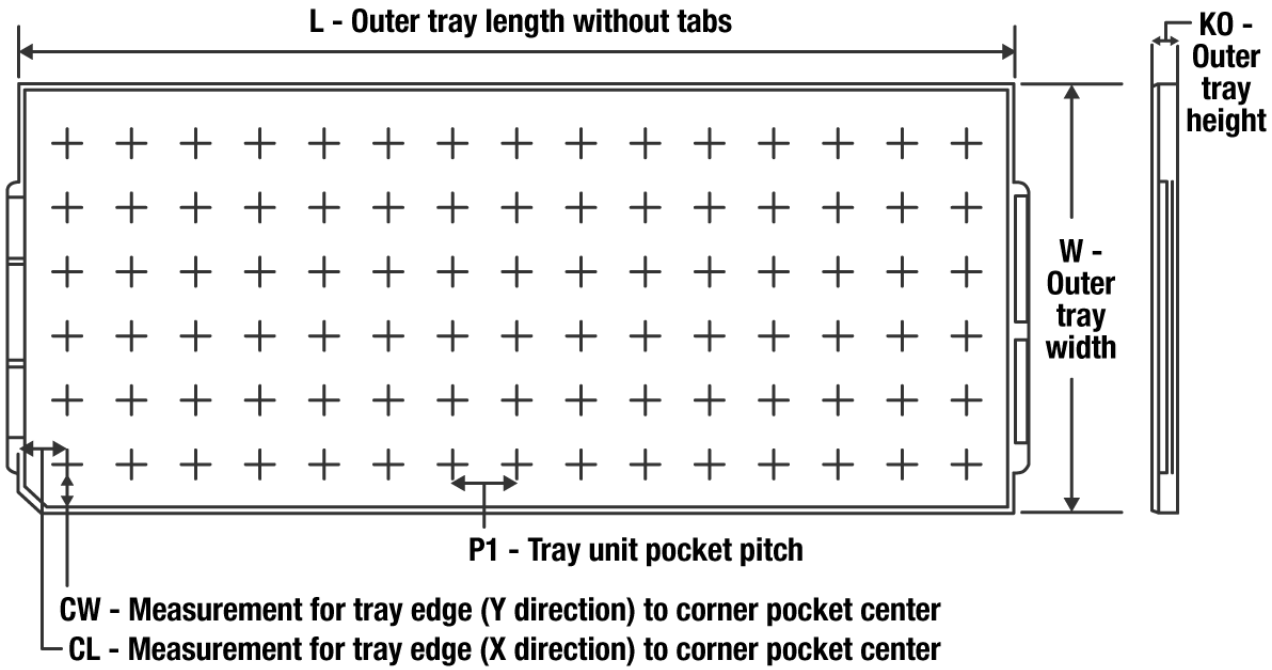
**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TRAY




Chamfer on Tray corner indicates Pin 1 orientation of packed units.

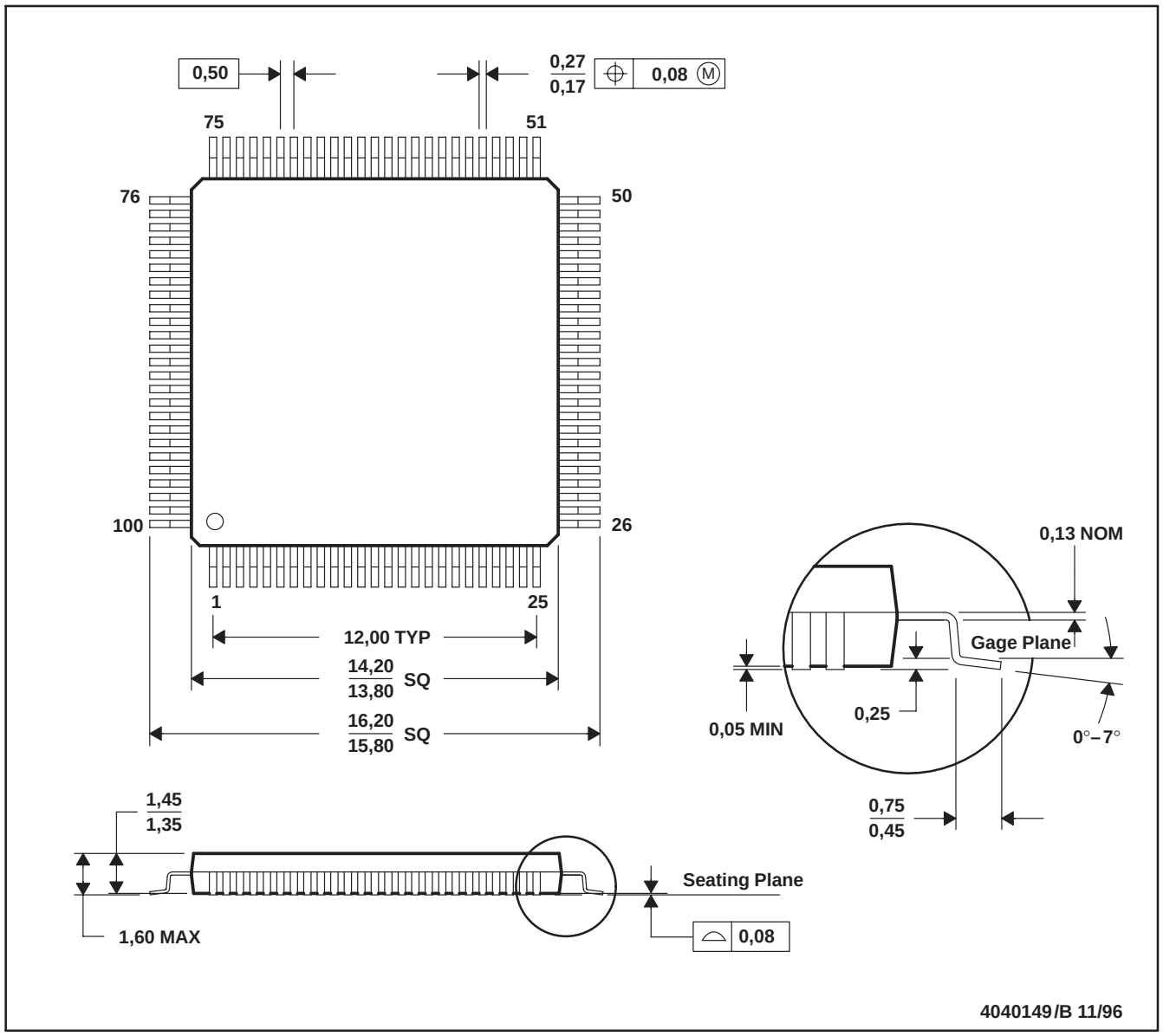
*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430F67451IPEU | PEU | LQFP | 128 | 72 | 6X12 | 150 | 315 | 135.9 | 7620 | 25.4 | 17.8 | 15.45 |
| MSP430F67451IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F67461IPEU | PEU | LQFP | 128 | 72 | 6X12 | 150 | 315 | 135.9 | 7620 | 25.4 | 17.8 | 15.45 |
| MSP430F67461IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F67471IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F67481IPEU | PEU | LQFP | 128 | 72 | 6X12 | 150 | 315 | 135.9 | 7620 | 25.4 | 17.8 | 15.45 |
| MSP430F67481IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F67491IPEU | PEU | LQFP | 128 | 72 | 6X12 | 150 | 315 | 135.9 | 7620 | 25.4 | 17.8 | 15.45 |
| MSP430F67491IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F67651IPEU | PEU | LQFP | 128 | 72 | 6X12 | 150 | 315 | 135.9 | 7620 | 25.4 | 17.8 | 15.45 |
| MSP430F67651IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F67661IPEU | PEU | LQFP | 128 | 72 | 6X12 | 150 | 315 | 135.9 | 7620 | 25.4 | 17.8 | 15.45 |
| MSP430F67661IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F67671IPEU | PEU | LQFP | 128 | 72 | 6X12 | 150 | 315 | 135.9 | 7620 | 25.4 | 17.8 | 15.45 |
| MSP430F67671IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F67681IPEU | PEU | LQFP | 128 | 72 | 6X12 | 150 | 315 | 135.9 | 7620 | 25.4 | 17.8 | 15.45 |
| MSP430F67681IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430F67691IPEU | PEU | LQFP | 128 | 72 | 6X12 | 150 | 315 | 135.9 | 7620 | 25.4 | 17.8 | 15.45 |
| MSP430F67691IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F67751IPEU | PEU | LQFP | 128 | 72 | 6X12 | 150 | 315 | 135.9 | 7620 | 25.4 | 17.8 | 15.45 |
| MSP430F67751IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F67761IPEU | PEU | LQFP | 128 | 72 | 6X12 | 150 | 315 | 135.9 | 7620 | 25.4 | 17.8 | 15.45 |
| MSP430F67761IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F67771IPEU | PEU | LQFP | 128 | 72 | 6X12 | 150 | 315 | 135.9 | 7620 | 25.4 | 17.8 | 15.45 |
| MSP430F67771IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F67781IPEU | PEU | LQFP | 128 | 72 | 6X12 | 150 | 315 | 135.9 | 7620 | 25.4 | 17.8 | 15.45 |
| MSP430F67781IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F67791IPEU | PEU | LQFP | 128 | 72 | 6X12 | 150 | 315 | 135.9 | 7620 | 25.4 | 17.8 | 15.45 |
| MSP430F67791IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |

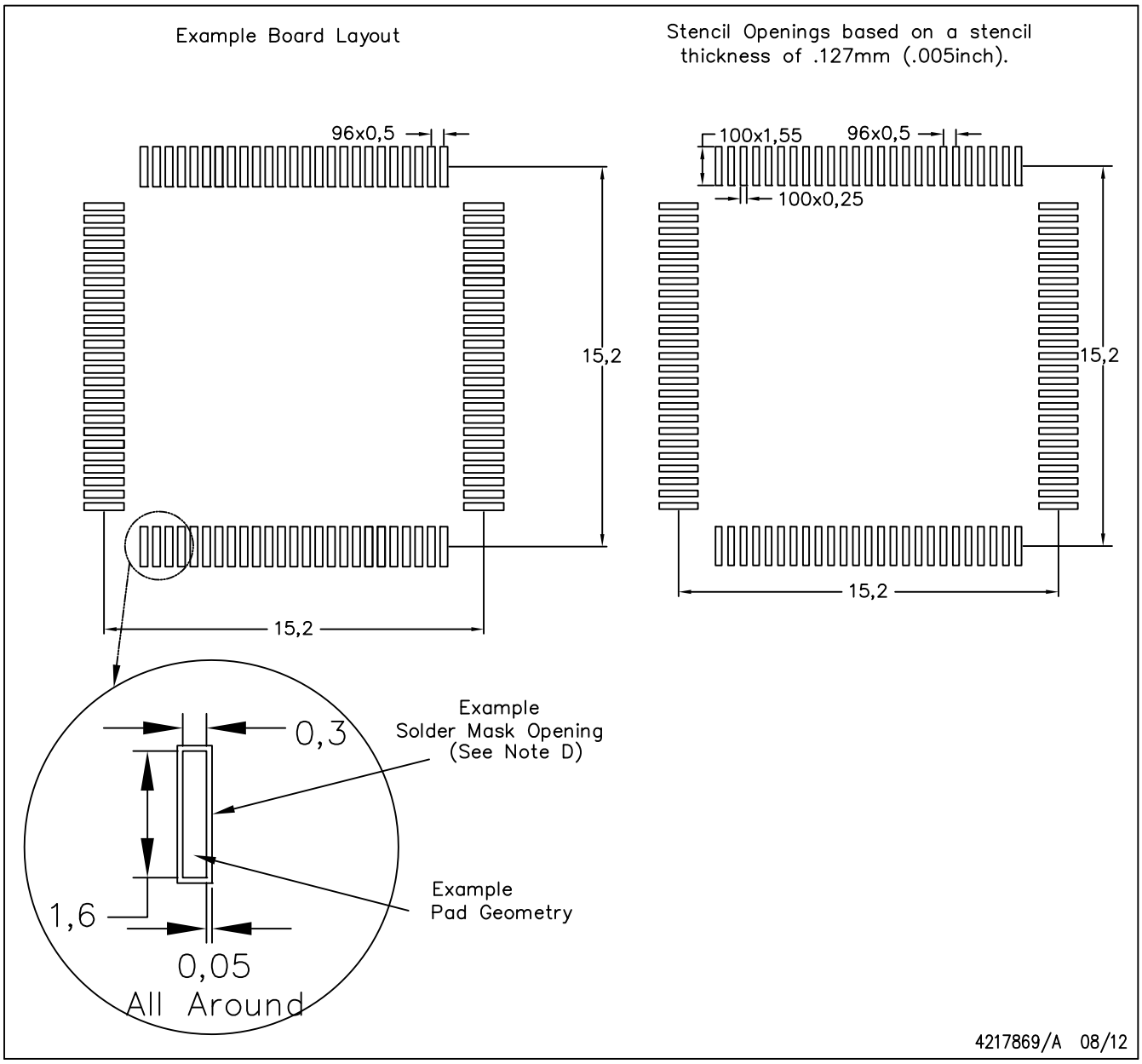
MTQF013A – OCTOBER 1994 – REVISED DECEMBER 1996

**PZ (S-PQFP-G100)** **PLASTIC QUAD FLATPACK**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

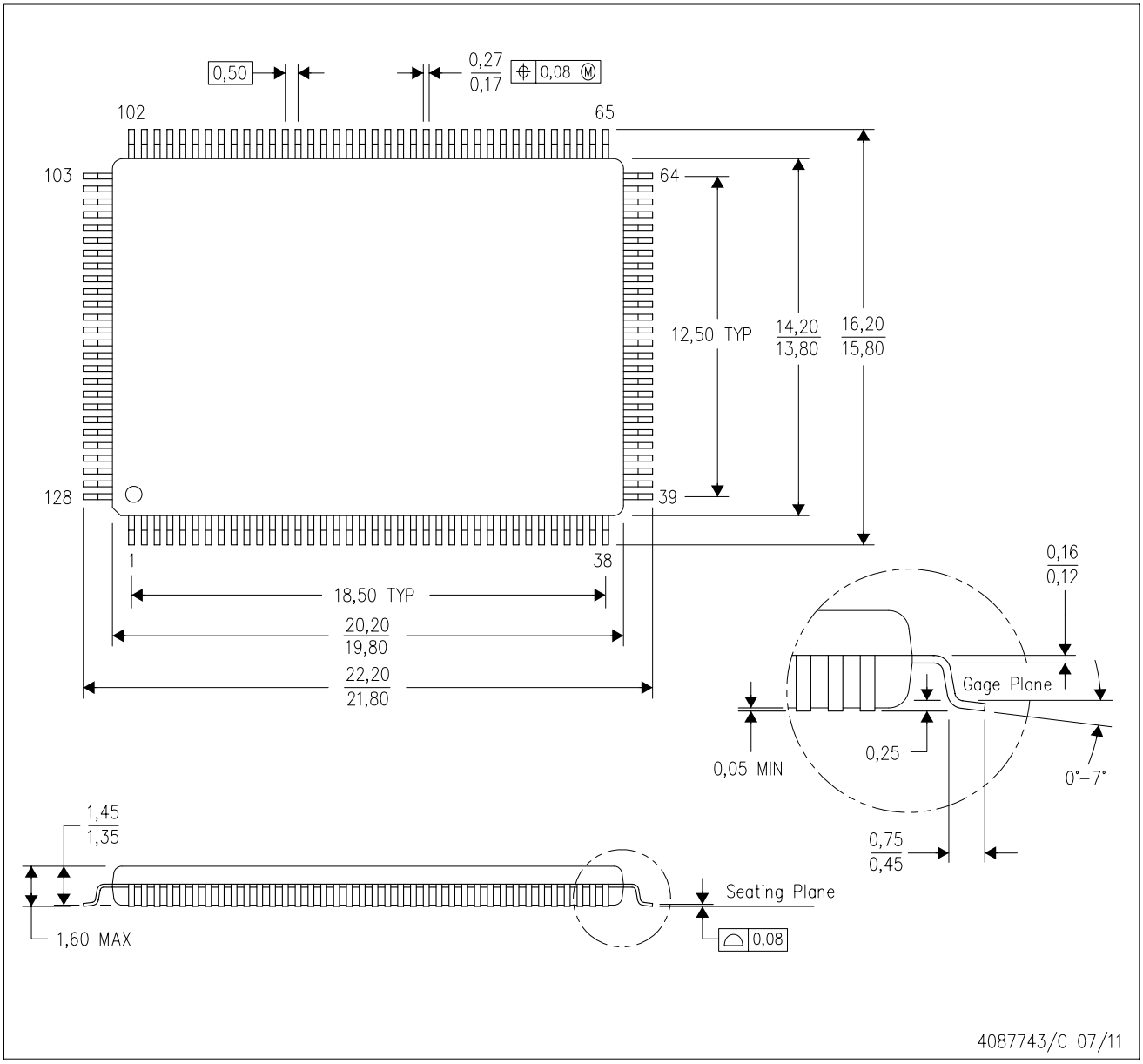
# PZ (S–PQFP–G100) PLASTIC QUAD FLAT PACK




NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PEU (R–PQFP–G128) PLASTIC QUAD FLATPACK




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–026

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