# MSP430FR235x、MSP430FR215x 混合信号微控制器

## 1 器件概述

### 1.1 特性

- 嵌入式微控制器
  - 16 位 RISC 架构，频率最高可达 24MHz
  - 扩展温度范围：–40°C 至 105°C
  - 3.6V 至 1.8V 的宽电源电压范围（工作电压受限于 SVS 电平，参阅 $V_{SVSH-}$ 和 $V_{SVSH+}$，见 *PMM、SVS 和 BOR*）
- 经优化的低功耗模式（3V）
  - 工作模式：142µA/MHz
  - 待机：
    - 具有 32768Hz 晶体的 LPM3：1.43µA（SVS 处于启用状态）
    - 具有 32768Hz 晶体的 LPM3.5：620nA（SVS 处于启用状态）
  - 关断 (LPM4.5)：42nA（SVS 处于启用状态）
- 低功耗铁电 RAM (FRAM)
  - 容量高达 32KB 的非易失性存储器
  - 内置错误修正码 (ECC)
  - 可配置的写保护
  - 对程序、常量和存储的统一存储
  - 耐写次数达 $10^{15}$ 次
  - 抗辐射和非磁性
- 易于使用
  - 20KB ROM 库包含驱动程序库和 FFT 库
- 高性能模拟
  - 一个 12 通道 12 位模数转换器 (ADC)
    - 内部共享基准（1.5、2.0 或 2.5V）
    - 采样与保持 200ksps
  - 两个增强型比较器 (eCOMP)
    - 集成 6 位数模转换器 (DAC) 作为基准电压
    - 可编程迟滞
    - 可配置的高功率和低功率模式
    - 一个具有 100ns 的快速响应时间
    - 一个具有 1µs 的响应时间以及 1.5µA 的低功耗
  - 四个智能模拟组合 (SAC-L3)（仅限 MSP430FR235x 器件）
    - 支持通用运算放大器 (OA)
    - 轨至轨输入和输出
    - 多个输入信号选项
    - 可配置的高功率和低功率模式
    - 可配置 PGA 模式支持
      - 同相模式：×1、×2、×3、×5、×9、×17、×26、×33
      - 反相模式：×1、×2、×4、×8、×16、×25、×32
    - 用于进行失调电压和偏置设置的内置 12 位基准 DAC
    - 具有可选基准电压的 12 位电压 DAC 模式
- 智能数字外设
  - 三个 16 位计时器，每个计时器有 3 个捕捉/比较寄存器 (Timer_B3)
  - 一个 16 位计时器，每个计时器有 7 个捕捉/比较寄存器 (Timer_B7)
  - 一个仅用作计数器的 16 位实时钟计数器 (RTC)
  - 16 位循环冗余校验器 (CRC)
  - 中断比较控制器 (ICC)，可启用嵌套硬件中断
  - 32 位硬件乘法器 (MPY32)
  - 曼彻斯特编解码器 (MFM)
- 增强型串行通信
  - 两个增强型 USCI_A (eUSCI_A) 模块支持 UART、IrDA 和 SPI
  - 两个增强型 USCI_B (eUSCI_B) 模块支持 SPI 和 $I^2C$
- 时钟系统 (CS)
  - 片上 32kHz RC 振荡器 (REFO)
  - 带有锁频环 (FLL) 的片上 24MHz 数控振荡器 (DCO)
    - 室温下的精度为 ±1%（具有片上基准）
  - 片上超低频 10kHz 振荡器 (VLO)
  - 片上高频调制振荡器 (MODOSC)
  - 外部 32kHz 晶振 (LFXT)
  - 外部高频晶体振荡器，频率最高可达 24MHz (HFXT)
  - 可编程 MCLK 预分频器（1 至 128）
  - 源自具有可编程预分频器（1、2、4 或 8）的 MCLK 的 SMCLK

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

- 通用输入/输出和引脚功能
  - 48 引脚封装上的 44 个 I/O
  - 32 个中断引脚（P1、P2、P3 和 P4）可以将 MCU 从 LPM 唤醒
- 开发工具和软件（另外请参阅 工具和软件）
  - LaunchPad™开发套件 (MSP-EXP430FR2355)
  - 目标开发板 (MSP-TS43048PT)
  - 免费的专业开发环境
- 系列成员（另请参阅 器件比较）
  - MSP430FR2355：32KB 的程序 FRAM、512B 的数据 FRAM、4KB 的 RAM
  - MSP430FR2353：16KB 的程序 FRAM、512B 的数据 FRAM、2KB 的 RAM
  - MSP430FR2155：32KB 的程序 FRAM、512B 的数据 FRAM、4KB 的 RAM
  - MSP430FR2153：16KB 的程序 FRAM、512B 的数据 FRAM、2KB 的 RAM
- 封装选项
  - 48 引脚：LQFP (PT)
  - 40 引脚：VQFN (RHA)
  - 38 引脚：TSSOP (DBT)
  - 32 引脚：VQFN (RSM)

## 1.2 应用

- 烟雾和热量探测器
- 传感器变送器
- 断路器
- 传感器信号调节
- 有线工业通信
- 光学模块
- 电池组管理
- 收费标签

## 1.3 说明

MSP430FR215x 和 MSP430FR235x 微控制器 (MCU) 均属于 MSP430™MCU 超值系列超低功耗低成本器件产品系列，该产品系列适用于检测和测量 应用。MSP430FR235x MCU 集成了四个称之为智能模拟组合的可配置信号链模块，每个组合均可用作 12 位 DAC 或可配置可编程增益运算放大器，以满足系统的特定需求，同时缩减 BOM 并减小 PCB 尺寸。该器件还包含一个 12 位 SAR ADC 和两个比较器。MSP430FR215x 和 MSP430FR235x MCU 都支持 –40° 至 105°C 的扩展温度范围，因此更高温度的工业应用 可从这些器件的 FRAM 数据记录功能受益。该扩展温度范围使开发人员可以满足烟雾探测器、传感器变送器和断路器等 应用 的要求。

MSP430FR215x 和 MSP430FR235x MCU 具有功能强大的 16 位 RISC CPU、16 位寄存器和常数发生器，有助于实现最大编码效率。数控振荡器 (DCO) 通常可以使器件在不到 10µs 的时间内从低功耗模式唤醒至激活模式。

MSP430 超低功耗 (ULP) FRAM 微控制器平台将独特的嵌入式 FRAM 和整体超低功耗系统架构相结合，从而使系统设计人员能够在降低能耗的情况下提升性能。FRAM 技术将 RAM 的低功耗快速写入、灵活性和耐用性与闪存的非易失性相结合。

MSP430FR215x 和 MSP430FR235x MCU 由广泛的硬件和软件生态系统提供支持，随附参考设计和代码示例，便于您快速开始设计。开发套件包括 MSP-EXP430FR2355 LaunchPad™开发套件和 MSP-TS430PT48 48 引脚目标开发板。TI 还提供免费的 MSP430Ware™ 软件，该软件以 Code Composer Studio™ IDE 台式机和云版本组件的形式提供（位于 TI Resource Explorer）。 E2E™ 支持论坛还为 MSP430 MCU 提供广泛的在线配套资料、培训和在线支持。

有关完整的模块说明，请参阅《MSP430FR4xx 和 MSP430FR2xx 系列器件用户指南》。


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器件信息(1)

| 器件型号 | 工作温度 | 封装 | 封装尺寸(2) |
|---|---|---|---|
| MSP430FR2355TPT | -40°C 至 105°C | LQFP (48) | 7mm × 7mm |
| MSP430FR2353TPT | | | |
| MSP430FR2155TPT | | | |
| MSP430FR2153TPT | | | |
| MSP430FR2355TRHA | -40°C 至 105°C | VQFN (40) | 6mm × 6mm |
| MSP430FR2353TRHA | | | |
| MSP430FR2155TRHA | | | |
| MSP430FR2153TRHA | | | |
| MSP430FR2355TDBT | -40°C 至 105°C | TSSOP (38) | 9.7mm × 4.4mm |
| MSP430FR2353TDBT | | | |
| MSP430FR2155TDBT | | | |
| MSP430FR2153TDBT | | | |
| MSP430FR2355TRSM | -40°C 至 105°C | VQFN (32) | 4mm × 4mm |
| MSP430FR2353TRSM | | | |
| MSP430FR2155TRSM | | | |
| MSP430FR2153TRSM | | | |

(1) 要获得最新的产品、封装和订购信息，请参见*封装选项附录*（节 9），或者访问德州仪器 (TI) 网站 www.ti.com.cn。
(2) 这里显示的尺寸为近似值。要获得包含误差值的封装尺寸，请参见*机械数据*（节 9中）。

**CAUTION**

系统级静电放电 (ESD) 保护必须符合器件级 ESD 规范，以防发生电气过载或对数据或代码存储器造成干扰。有关更多信息，请参阅《MSP430™ 系统级 ESD 注意事项》。

## 1.4 功能方框图

图 1-1 显示了 MSP430FR235x 功能方框图。

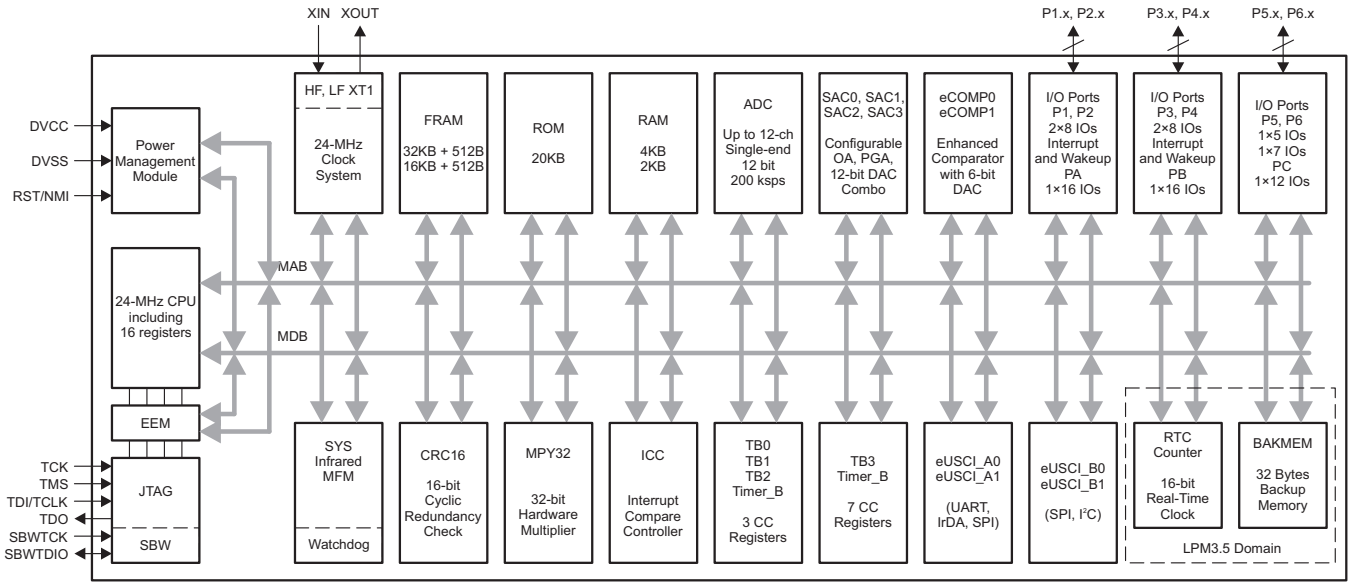



**图 1-1. MSP430FR235x 功能方框图**

图 1-2 显示了 MSP430FR215x 功能方框图。

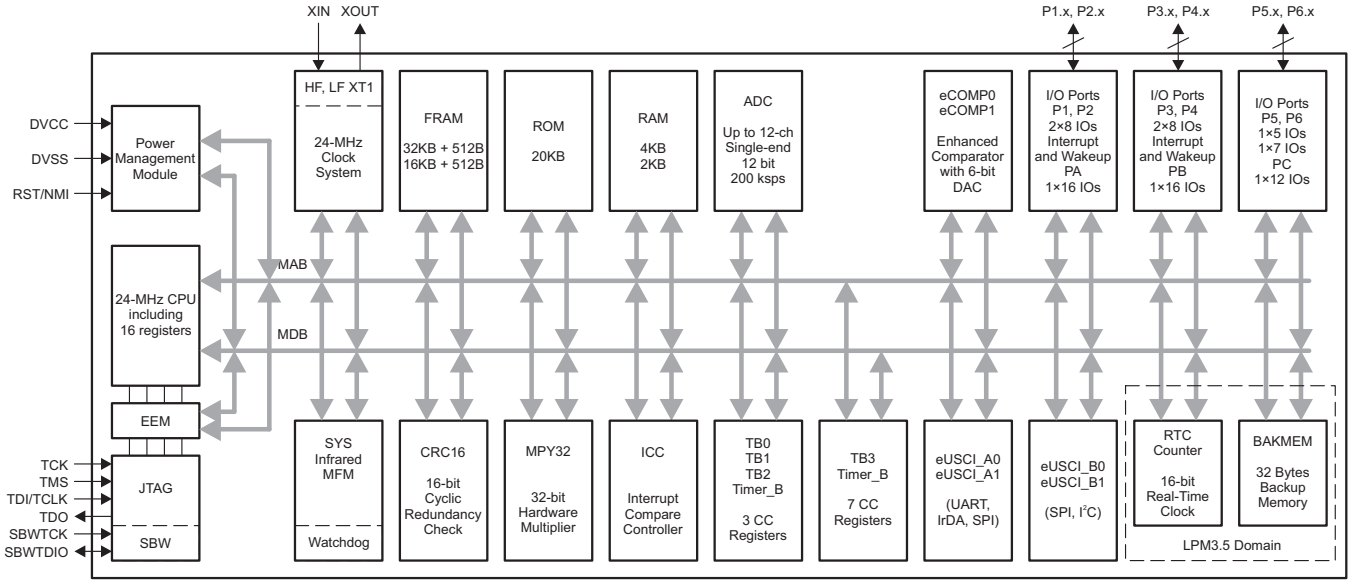



**图 1-2. MSP430FR215x 功能方框图**

- MCU 具有一个 DVCC 和 DVSS 引脚主电源对，用于为数字模块和模拟模块供电。推荐的旁路电容和去耦电容分别为 4.7µF 至 10µF 和 0.1µF，精度为 ±5%。
- P1、P2、P3 和 P4 具有引脚中断功能，可以将 MCU 从所有 LPM（包括 LPM4、LPM3.5 和 LPM4.5）唤醒。
- 每个 Timer_B3 具有三个捕捉/比较寄存器。仅 CCR1 和 CCR2 从外部连接。Timer_B7 有 7 个捕捉/比较寄存器。仅 CCR1 至 CCR6 从外部连接。CCR0 寄存器仅用于内部周期时序和中断生成。
- 在 LPM3.5 模式下，RTC 计数器与备用存储器可继续工作，而其余外设停止工作。


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## 2 修订历史记录

从修订版本 C 更改为修订版本 D

| Changes from March 6, 2019 to December 10, 2019 | Page |
|---|---|
| • 修正了 图 1-1 中的 ROM 规格*MSP430FR235x 功能方框图* 和 图 1-2 *MSP430FR215x 功能方框图* | 4 |
| • Added a note on all VQFN pinouts to indicate that the thermal pad should be connected to VSS | 11 |
| • Corrected 图 4-4, *32-Pin RSM (VQFN) (Top View) – MSP430FR235x* | 13 |
| • Changed the note that begins "Supply voltage changes faster than 0.2 V/µs can trigger a BOR reset..." in Section 5.3, *Recommended Operating Conditions* | 27 |
| • Added the note that begins "TI recommends that power to the DVCC pin must not exceed the limits..." in Section 5.3, *Recommended Operating Conditions* | 27 |
| • Changed the note that begins "A capacitor tolerance of ±20% or better is required..." in Section 5.3, *Recommended Operating Conditions* | 27 |
| • Combined former sections 5.8 and 5.10 into 节 5.9, *Production Distribution of LPM Supply Currents* | 31 |
| • Corrected the "SVS disabled" condition for 图 5-1 | 31 |
| • Added the note "See *MSP430 32-kHz Crystal Oscillators* for details on crystal section, layout, and testing" to 表 5-3, *XT1 Crystal Oscillator (Low Frequency)* | 35 |
| • Changed the note that begins "Requires external capacitors at both terminals..." in 表 5-3, *XT1 Crystal Oscillator (Low Frequency)* | 35 |
| • Added the $t_{TB,cap}$ parameter in 表 5-13, *Timer_B* | 45 |
| • Corrected the test conditions for the $R_I$ parameter in 表 5-20, *ADC, Power Supply and Input Range Conditions* | 51 |
| • Removed ADCDIV from the equation for the ADC conversion time because ADCCLK is after division in 表 5-21, *ADC, Timing Parameters* | 51 |
| • Added the note that begins "$t_{Sample} = \ln(2^{n+1}) \times \tau$ ..." in 表 5-21, *ADC, Timing Parameters* | 51 |
| • Changed the unit from "nV" to "µV" for the "Input noise voltage" in the 表 5-25, *SAC, OA* | 55 |
| • Changed the unit from "nv/Hz" to "nV/$\sqrt{Hz}$" for the "Input noise voltage density" in the 表 5-25, *SAC, OA* | 55 |
| • Removed the $I_{ref}$ trim parameter from 表 5-27, *FRAM* | 57 |
| • Changed the bitfield name from RTCCLK to RTCCKSEL in the table note on 表 6-9, *Clock Distribution* | 68 |
| • Added 节 6.10.17, *Cross-Chip Interconnection (SACx are MSP430FR235x Devices Only)* | 83 |
| • Added P1SELC information in 表 6-41, *Port P1, P2 Registers (Base Address: 0200h)* | 86 |
| • Added P2SELC information in 表 6-41, *Port P1, P2 Registers (Base Address: 0200h)* | 86 |
| • Added P3SELC information in 表 6-42, *Port P3, P4 Registers (Base Address: 0220h)* | 87 |
| • Added P4SELC information in 表 6-42, *Port P3, P4 Registers (Base Address: 0220h)* | 87 |
| • Added P5SELC information in 表 6-43, *Port P5, P6 Registers (Base Address: 0240h)* | 87 |
| • Added P6SELC information in 表 6-43, *Port P5, P6 Registers (Base Address: 0240h)* | 87 |
| • Changed CRC covered end address to 0x1AF7 in table note (1) in 表 6-70, *Device Descriptors* | 107 |

从修订版本 B 更改为修订版本 C

| Changes from July 3, 2018 to March 5, 2019 | Page |
|---|---|
| • 增加了 32 引脚 VQFN (RSM) 封装信息，见 节 1.1, *特性* | 2 |
| • 在器件信息表中增加了 32 引脚 VQFN (RSM) 封装信息，见 节 1.3（*说明部分*） | 3 |
| • Added 32-pin VQFN (RSM) package information in 表 3-1, *Device Comparison* | 8 |
| • Added 图 4-4, *32-Pin RSM (VQFN) (Top View) – MSP430FR235x* | 13 |
| • Added 图 4-8, *32-Pin RSM (VQFN) (Top View) – MSP430FR215x* | 17 |
| • Added 32-pin VQFN (RSM) package information in 节 4.2, *Pin Attributes* | 18 |
| • Added 32-pin VQFN (RSM) package information in 节 4.3, *Signal Descriptions* | 22 |
| • Added 32-pin VQFN (RSM) package information in Section 5.11, *Thermal Resistance Characteristics* | 32 |
| • Added the $t_{TB,cap}$ parameter in 表 5-13, *Timer_B* | 45 |
| • Removed the $I_{ref}$ trim parameter from 表 5-27, *FRAM* | 57 |


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从修订版本 A 更改为修订版本 B

| Changes from June 20, 2018 to July 2, 2018 | Page |
|---|---|
| • Added the $t_{TB,cap}$ parameter in 表 5-13, *Timer_B* | 45 |
| • Removed the $I_{ref}$ trim parameter from 表 5-27, *FRAM* | 57 |
| • 更新了节 8.3*工具和软件* | 116 |
| • 在节 8.4*文档支持* 中添加了勘误表 | 118 |

从初始发行版更改为修订版本 A

| Changes from May 11, 2018 to June 19, 2018 | Page |
|---|---|
| • 将文档状态更改为“生产数据” | 1 |
| • Added missing UCB0SCL signal to P1.3/UCB0SOMI/UCB0SCL/OA0+/A3 in pinout figures | 11 |
| • Added the $t_{TB,cap}$ parameter in 表 5-13, *Timer_B* | 45 |
| • Removed the $I_{ref}$ trim parameter from 表 5-27, *FRAM* | 57 |
| • Added row for "Driver library and FFT library" in 表 6-4, *Memory Organization* | 65 |
| • Added 节 7.3, *ROM Libraries* | 114 |
| • Corrected the title and link to reference design in 表 7-1, *Tools and Reference Designs* | 114 |

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# 3 Device Comparison

表 3-1 summarizes the features of the available family members.

**表 3-1. Device Comparison(1) (2)**

| DEVICE | PROGRAM FRAM | SRAM (bytes) | TB0, TB1, TB2 | TB3 | eUSCI_A | eUSCI_B | 12-BIT ADC CHANNELS | SAC | eCOMP | I/Os | PACKAGE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430FR2355PT | 32KB + 512B | 4096 | 3 × CCR(3) | 7 × CCR(3) | 2 | 2 | 12 | 4 | 2 | 44 | 48 PT (LQFP) |
| MSP430FR2353PT | 16KB + 512B | 2048 | 3 × CCR(3) | 7 × CCR(3) | 2 | 2 | 12 | 4 | 2 | 44 | 48 PT (LQFP) |
| MSP430FR2355RHA | 32KB + 512B | 4096 | 3 × CCR(3) | 7 × CCR(3) | 2 | 2 | 10 | 4 | 2 | 36 | 40 RHA (VQFN) |
| MSP430FR2353RHA | 16KB + 512B | 2048 | 3 × CCR(3) | 7 × CCR(3) | 2 | 2 | 10 | 4 | 2 | 36 | 40 RHA (VQFN) |
| MSP430FR2355DBT | 32KB + 512B | 4096 | 3 × CCR(3) | 7 × CCR(3) | 2 | 2 | 10 | 4 | 2 | 34 | 38 DBT (TSSOP) |
| MSP430FR2353DBT | 16KB + 512B | 2048 | 3 × CCR(3) | 7 × CCR(3) | 2 | 2 | 10 | 4 | 2 | 34 | 38 DBT (TSSOP) |
| MSP430FR2355RSM | 32KB + 512B | 4096 | 3 × CCR(3) | 7 × CCR(3) | 2 | 2(4) | 8 | 4 | 2 | 28 | 32 RSM (VQFN) |
| MSP430FR2353RSM | 16KB + 512B | 2048 | 3 × CCR(3) | 7 × CCR(3) | 2 | 2(4) | 8 | 4 | 2 | 28 | 32 RSM (VQFN) |
| MSP430FR2155PT | 32KB + 512B | 4096 | 3 × CCR(3) | 7 × CCR(3) | 2 | 2 | 12 | – | 2 | 44 | 48 PT (LQFP) |
| MSP430FR2153PT | 16KB + 512B | 2048 | 3 × CCR(3) | 7 × CCR(3) | 2 | 2 | 12 | – | 2 | 44 | 48 PT (LQFP) |
| MSP430FR2155RHA | 32KB + 512B | 4096 | 3 × CCR(3) | 7 × CCR(3) | 2 | 2 | 10 | – | 2 | 36 | 40 RHA (VQFN) |
| MSP430FR2153RHA | 16KB + 512B | 2048 | 3 × CCR(3) | 7 × CCR(3) | 2 | 2 | 10 | – | 2 | 36 | 40 RHA (VQFN) |
| MSP430FR2155DBT | 32KB + 512B | 4096 | 3 × CCR(3) | 7 × CCR(3) | 2 | 2 | 10 | – | 2 | 34 | 38 DBT (TSSOP) |
| MSP430FR2153DBT | 16KB + 512B | 2048 | 3 × CCR(3) | 7 × CCR(3) | 2 | 2 | 10 | – | 2 | 34 | 38 DBT (TSSOP) |
| MSP430FR2155RSM | 32KB + 512B | 4096 | 3 × CCR(3) | 7 × CCR(3) | 2 | 2(4) | 8 | – | 2 | 28 | 32 RSM (VQFN) |
| MSP430FR2153RSM | 16KB + 512B | 2048 | 3 × CCR(3) | 7 × CCR(3) | 2 | 2(4) | 8 | – | 2 | 28 | 32 RSM (VQFN) |

(1) For the most current device, package, and ordering information, see the *Package Option Addendum* in 节 9, or see the TI web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.
(3) A CCR register is a configurable register that provides internal and external capture or compare inputs, or internal and external PWM outputs. Not all CCR channels are package specific. See the definition in 节 4.3.
(4) eUSCI_B1 supports only $I^2C$ function.


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## 3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

TI 16-bit and 32-bit microcontrollers

High-performance, low-power solutions to enable the autonomous future

Products for MSP430 ultra-low-power sensing & measurement microcontrollers

One platform. One ecosystem. Endless possibilities.

Companion products for MSP430FR2355

Review products that are frequently purchased or used with this product.

Reference designs for MSP430FR2355

Find reference designs leveraging the best in TI technology to solve your system-level challenges.

# 4 Terminal Configuration and Functions

## 4.1 Pin Diagrams

图 4-1 shows the pinout of the 48-pin PT package for the MSP430FR235x MCUs.

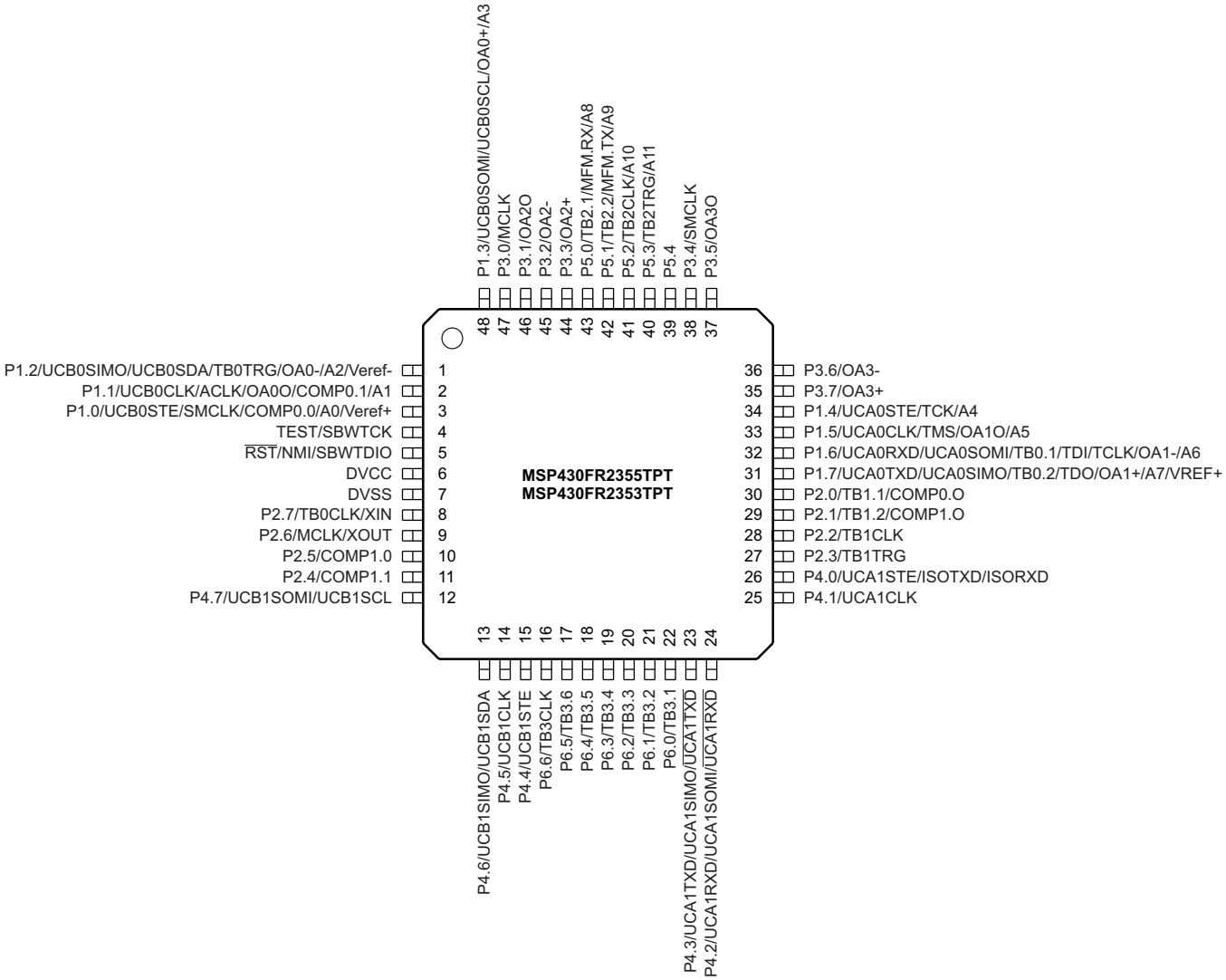
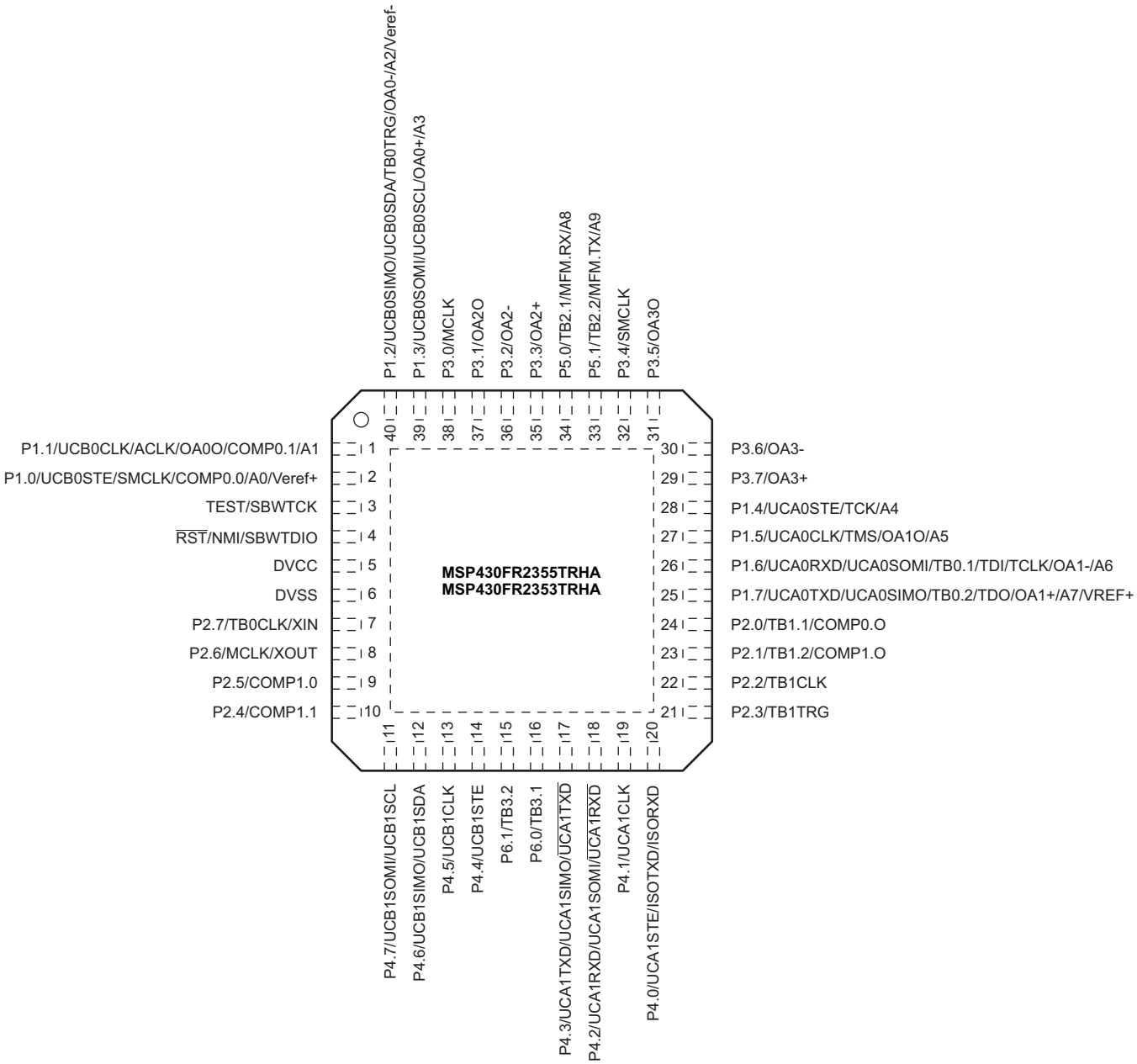



**图 4-1. 48-Pin PT (LQFP) (Top View) – MSP430FR235x**


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图 4-2 shows the pinout of the 40-pin RHA package for the MSP430FR235x MCUs.




NOTE: Connect the exposed thermal pad to VSS.

**图 4-2. 40-Pin RHA (VQFN) (Top View) – MSP430FR235x**

图 4-3 shows the pinout of the 38-pin DBT package for the MSP430FR235x MCUs.

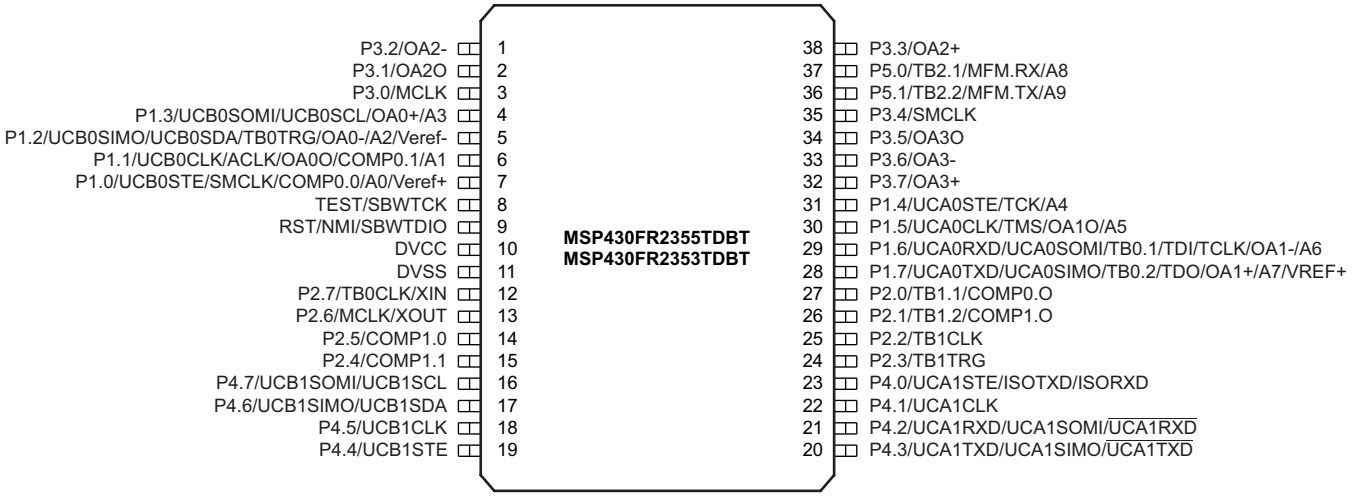
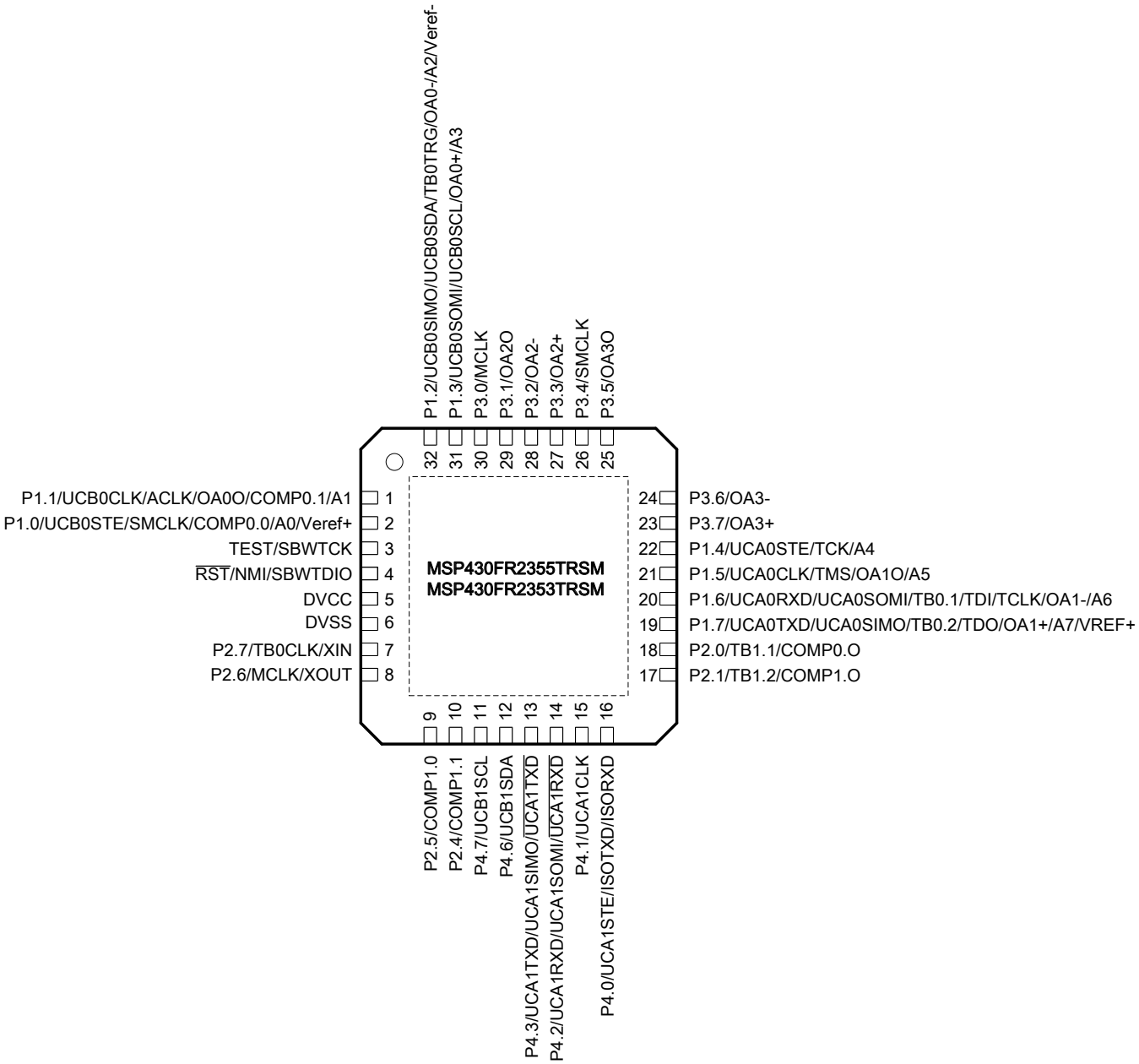



**图 4-3. 38-Pin DBT (TSSOP) (Top View) – MSP430FR235x**


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图 4-4 shows the pinout of the 32-pin RSM package for the MSP430FR235x MCUs.




NOTE: Connect the exposed thermal pad to VSS.

**图 4-4. 32-Pin RSM (VQFN) (Top View) – MSP430FR235x**

图 4-5 shows the pinout of the 48-pin PT package for the MSP430FR215x MCUs.

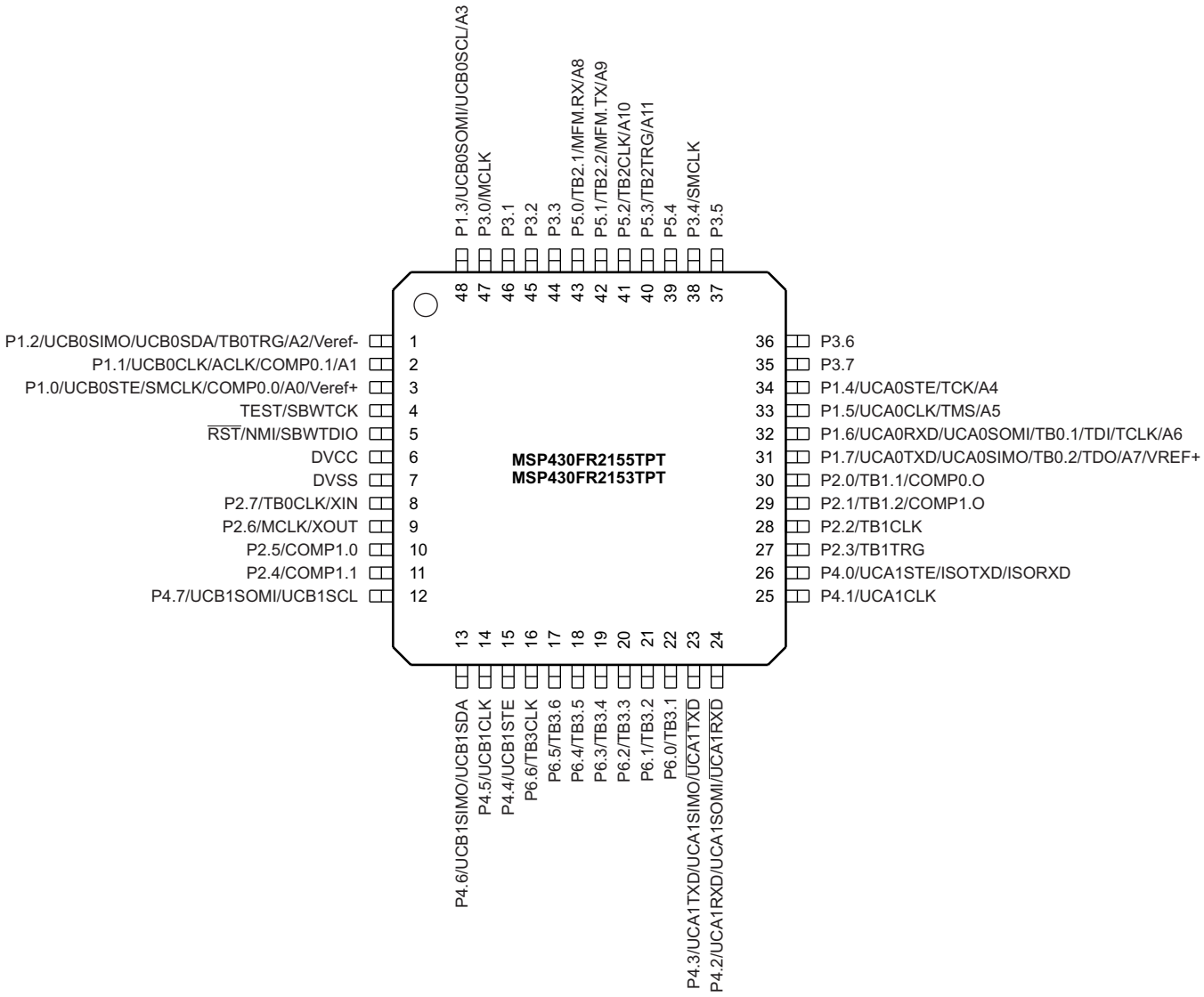
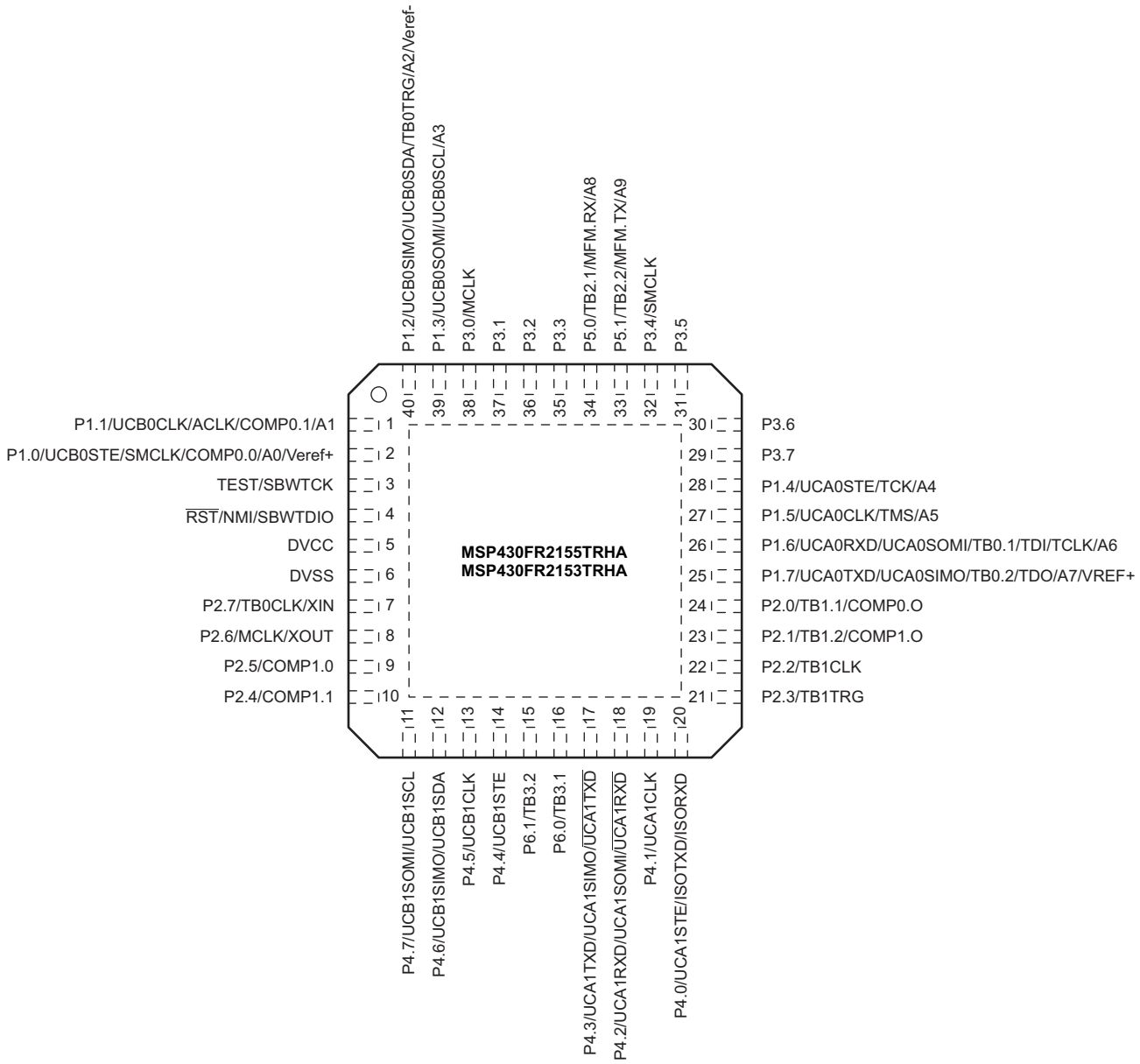



**图 4-5. 48-Pin PT (LQFP) (Top View) – MSP430FR215x**


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图 4-6 shows the pinout of the 40-pin RHA package for the MSP430FR215x MCUs.




NOTE: Connect the exposed thermal pad to VSS.

**图 4-6. 40-Pin RHA (VQFN) (Top View) – MSP430FR215x**

图 4-7 shows the pinout of the 38-pin DBT package for the MSP430FR215x MCUs.

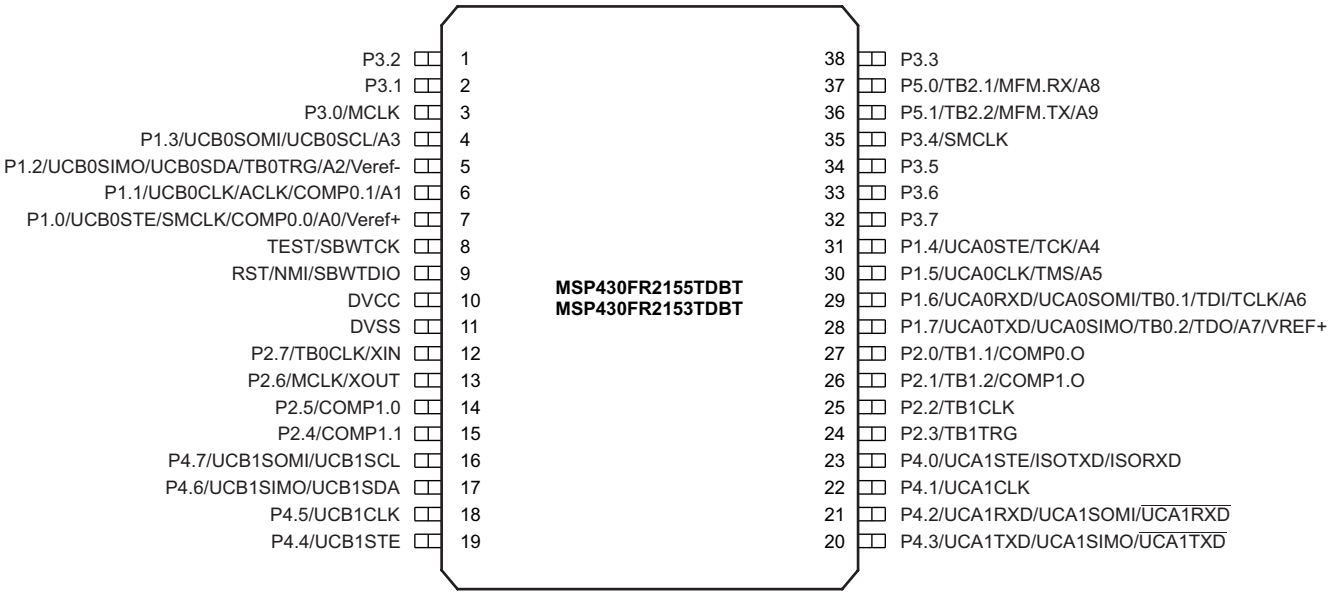
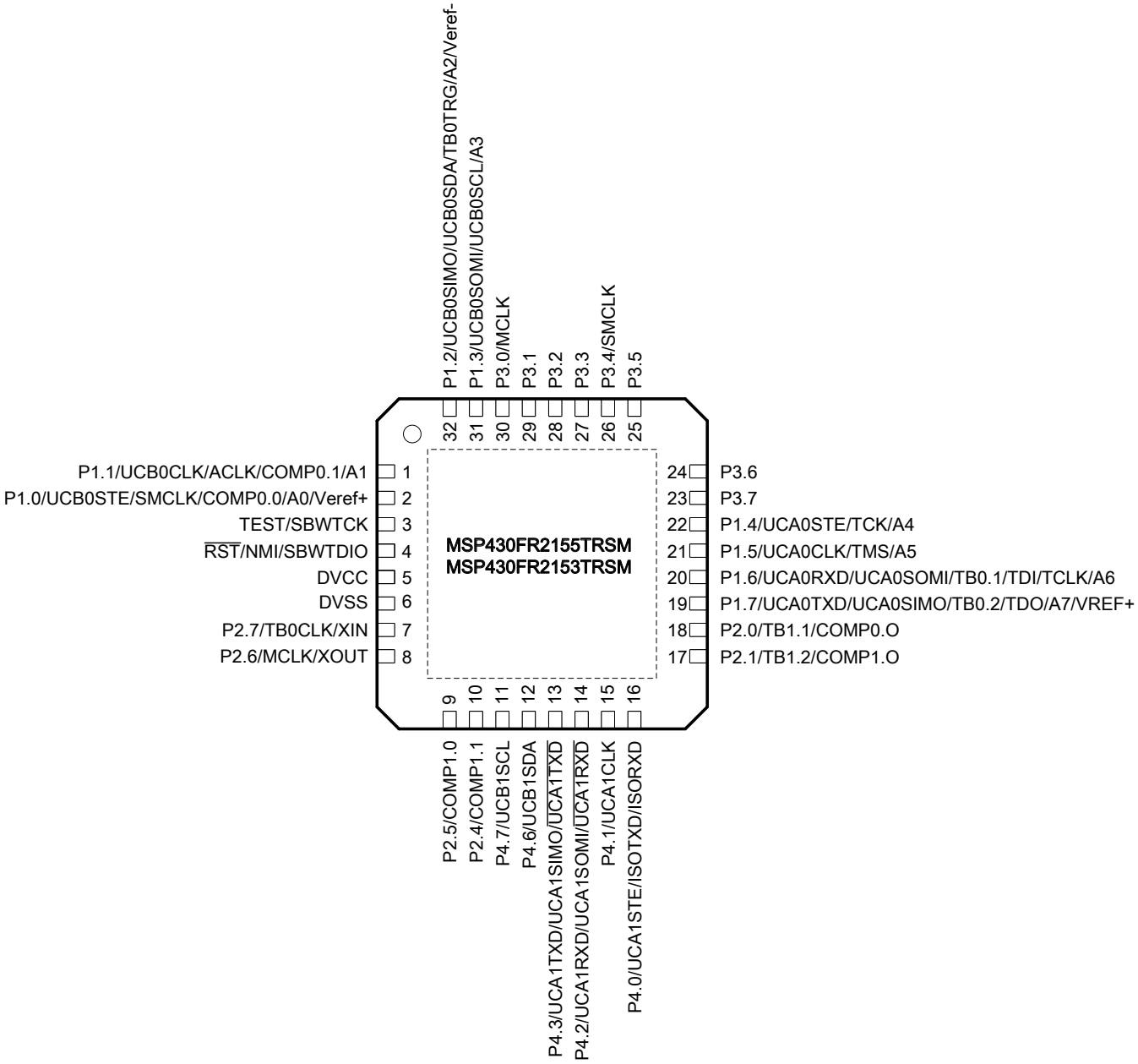



**图 4-7. 38-Pin DBT (TSSOP) (Top View) – MSP430FR215x**


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图 4-8 shows the pinout of the 32-pin RSM package for the MSP430FR215x MCUs.




NOTE: Connect the exposed thermal pad to VSS.

**图 4-8. 32-Pin RSM (VQFN) (Top View) – MSP430FR215x**

## 4.2 Pin Attributes

表 4-1 lists the attributes of all pins.

**表 4-1. Pin Attributes**

| PIN NUMBER | | | | SIGNAL NAME(1) (2) | SIGNAL TYPE(3) | BUFFER TYPE(4) | POWER SOURCE | RESET STATE AFTER BOR(5) |
|---|---|---|---|---|---|---|---|---|
| PT | RHA | DBT | RSM | | | | | |
| 1 | 40 | 5 | 32 | P1.2 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | UCB0SIMO | I/O | LVCMOS | DVCC | – |
| | | | | UCB0SDA | I/O | LVCMOS | DVCC | – |
| | | | | TB0TRG | I | LVCMOS | DVCC | – |
| | | | | OA0-(6) | I | Analog | DVCC | – |
| | | | | A2 | I | Analog | DVCC | – |
| | | | | Veref- | I | Analog | DVCC | – |
| 2 | 1 | 6 | 1 | P1.1 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | UCB0CLK | I/O | LVCMOS | DVCC | – |
| | | | | ACLK | O | LVCMOS | DVCC | – |
| | | | | OA0O(6) | O | Analog | DVCC | – |
| | | | | COMP0_1 | I | Analog | DVCC | – |
| | | | | A1 | I | Analog | DVCC | – |
| 3 | 2 | 7 | 2 | P1.0 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | UCB0STE | I/O | LVCMOS | DVCC | – |
| | | | | SMCLK | O | LVCMOS | DVCC | – |
| | | | | COMP0_0 | I | Analog | DVCC | – |
| | | | | A0 | I | Analog | DVCC | – |
| | | | | Veref+ | I | Analog | DVCC | – |
| 4 | 3 | 8 | 3 | TEST (RD) | I | LVCMOS | DVCC | OFF |
| | | | | SBWTCK | I | LVCMOS | DVCC | – |
| 5 | 4 | 9 | 4 | $\overline{\text{RST}}$ (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | NMI | I | LVCMOS | DVCC | – |
| | | | | SBWTDIO | I/O | LVCMOS | DVCC | – |
| 6 | 5 | 10 | 5 | DVCC | P | Power | DVCC | N/A |
| 7 | 6 | 11 | 6 | DVSS | P | Power | DVCC | N/A |
| 8 | 7 | 12 | 7 | P2.7 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | TB0CLK | I | LVCMOS | DVCC | – |
| | | | | XIN | I | LVCMOS | DVCC | – |
| 9 | 8 | 13 | 8 | P2.6 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | MCLK | O | LVCMOS | DVCC | – |
| | | | | XOUT | O | LVCMOS | DVCC | – |
| 10 | 9 | 14 | 9 | P2.5 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | COMP1.0 | I | Analog | DVCC | – |
| 11 | 10 | 15 | 10 | P2.4 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | COMP1.1 | I | Analog | DVCC | – |

(1) Signals names with (RD) denote the reset default pin name.
(2) To determine the pin mux encodings for each pin, see 节 6.11.
(3) Signal types: I = input, O = output, I/O = input or output
(4) Buffer types: LVCMOS, analog, or power
(5) Reset states:
OFF = High-impedance input with pullup or pulldown disabled (if available)
N/A = Not applicable
(6) MSP430FR235x devices only


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表 4-1. Pin Attributes (continued)

| PIN NUMBER | | | | SIGNAL NAME(1) (2) | SIGNAL TYPE(3) | BUFFER TYPE(4) | POWER SOURCE | RESET STATE AFTER BOR(5) |
|---|---|---|---|---|---|---|---|---|
| PT | RHA | DBT | RSM | | | | | |
| 12 | 11 | 16 | 11 | P4.7 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | UCB1SOMI(7) | I/O | LVCMOS | DVCC | – |
| | | | | UCB1SCL | I/O | LVCMOS | DVCC | – |
| 13 | 12 | 17 | 12 | P4.6 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | UCB1SIMO(7) | I/O | LVCMOS | DVCC | – |
| | | | | UCB1SDA | I/O | LVCMOS | DVCC | – |
| 14 | 13 | 18 | – | P4.5 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | UCB1CLK | I/O | LVCMOS | DVCC | – |
| 15 | 14 | 19 | – | P4.4 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | UCB1STE | I/O | LVCMOS | DVCC | – |
| 16 | – | – | – | P6.6 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | TB3CLK | I | LVCMOS | DVCC | – |
| 17 | – | – | – | P6.5 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | TB3.6 | I/O | LVCMOS | DVCC | – |
| 18 | – | – | – | P6.4 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | TB3.5 | I/O | LVCMOS | DVCC | – |
| 19 | – | – | – | P6.3 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | TB3.4 | I/O | LVCMOS | DVCC | – |
| 20 | – | – | – | P6.2 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | TB3.3 | I/O | LVCMOS | DVCC | – |
| 21 | 15 | – | – | P6.1 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | TB3.2 | I/O | LVCMOS | DVCC | – |
| 22 | 16 | – | – | P6.0 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | TB3.1 | I/O | LVCMOS | DVCC | – |
| 23 | 17 | 20 | 13 | P4.3 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | UCA1TXD | O | LVCMOS | DVCC | – |
| | | | | UCA1SIMO | I/O | LVCMOS | DVCC | – |
| | | | | $\overline{\text{UCA1TXD}}$ | O | LVCMOS | DVCC | – |
| 24 | 18 | 21 | 14 | P4.2 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | UCA1RXD | I | LVCMOS | DVCC | – |
| | | | | UCA1SOMI | I/O | LVCMOS | DVCC | – |
| | | | | $\overline{\text{UCA1RXD}}$ | I | LVCMOS | DVCC | – |
| 25 | 19 | 22 | 15 | P4.1 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | UCA1CLK | I/O | LVCMOS | DVCC | – |
| 26 | 20 | 23 | 16 | P4.0 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | UCA1STE | I/O | LVCMOS | DVCC | – |
| | | | | ISOTXD | O | LVCMOS | DVCC | – |
| | | | | ISORXD | I | LVCMOS | DVCC | – |
| 27 | 21 | 24 | – | P2.3 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | TB1TRG | I | LVCMOS | DVCC | – |
| 28 | 22 | 25 | – | P2.2 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | TB1CLK | I | LVCMOS | DVCC | – |
| 29 | 23 | 26 | 17 | P2.1(RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | TB1.2 | I/O | LVCMOS | DVCC | – |
| | | | | COMP1.O | O | LVCMOS | DVCC | – |

(7) Not applicable in RSM package.

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表 4-1. Pin Attributes (continued)

| PIN NUMBER | | | | SIGNAL NAME(1) (2) | SIGNAL TYPE(3) | BUFFER TYPE(4) | POWER SOURCE | RESET STATE AFTER BOR(5) |
|---|---|---|---|---|---|---|---|---|
| PT | RHA | DBT | RSM | | | | | |
| 30 | 24 | 27 | 18 | P2.0 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | TB1.1 | I/O | LVCMOS | DVCC | – |
| | | | | COMP0.O | O | LVCMOS | DVCC | – |
| 31 | 25 | 28 | 19 | P1.7 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | UCA0TXD | O | LVCMOS | DVCC | – |
| | | | | UCA0SIMO | I/O | LVCMOS | DVCC | – |
| | | | | TB0.2 | I/O | LVCMOS | DVCC | – |
| | | | | TDO | O | LVCMOS | DVCC | – |
| | | | | OA1+(6) | I | Analog | DVCC | – |
| | | | | A7 | I | Analog | DVCC | – |
| | | | | VREF+ | O | Analog | DVCC | – |
| 32 | 26 | 29 | 20 | P1.6 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | UCA0RXD | I | LVCMOS | DVCC | – |
| | | | | UCA0SOMI | I/O | LVCMOS | DVCC | – |
| | | | | TB0.1 | I/O | LVCMOS | DVCC | – |
| | | | | TDI | I | LVCMOS | DVCC | – |
| | | | | TCLK | I | LVCMOS | DVCC | – |
| | | | | OA1-(6) | I | Analog | DVCC | – |
| | | | | A6 | I | Analog | DVCC | – |
| 33 | 27 | 30 | 21 | P1.5 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | UCA0CLK | I/O | LVCMOS | DVCC | – |
| | | | | TMS | I | LVCMOS | DVCC | – |
| | | | | OA1O(6) | O | Analog | DVCC | - |
| | | | | A5 | I | Analog | DVCC | – |
| 34 | 28 | 31 | 22 | P1.4 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | UCA0STE | I/O | LVCMOS | DVCC | – |
| | | | | TCK | I | LVCMOS | DVCC | – |
| | | | | A4 | I | Analog | DVCC | – |
| 35 | 29 | 32 | 23 | P3.7 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | OA3+(6) | I | Analog | DVCC | – |
| 36 | 30 | 33 | 24 | P3.6 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | OA3-(6) | I | Analog | DVCC | – |
| 37 | 31 | 34 | 25 | P3.5 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | OA3O(6) | O | Analog | DVCC | – |
| 38 | 32 | 35 | 26 | P3.4 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | SMCLK | O | LVCMOS | DVCC | – |
| 39 | – | – | – | P5.4 (RD) | I/O | LVCMOS | DVCC | OFF |
| 40 | – | – | – | P5.3 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | TB2TRG | I | LVCMOS | DVCC | – |
| | | | | A11 | I | Analog | DVCC | – |
| 41 | – | – | – | P5.2 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | TB2CLK | I | LVCMOS | DVCC | – |
| | | | | A10 | I | Analog | DVCC | – |


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表 4-1. Pin Attributes (continued)

| PIN NUMBER | | | | SIGNAL NAME(1) (2) | SIGNAL TYPE(3) | BUFFER TYPE(4) | POWER SOURCE | RESET STATE AFTER BOR(5) |
|---|---|---|---|---|---|---|---|---|
| PT | RHA | DBT | RSM | | | | | |
| 42 | 33 | 36 | – | P5.1 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | TB2.2 | I/O | LVCMOS | DVCC | – |
| | | | | MFM.TX | O | LVCMOS | DVCC | – |
| | | | | A9 | I | Analog | DVCC | – |
| 43 | 34 | 37 | – | P5.0 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | TB2.1 | I/O | LVCMOS | DVCC | – |
| | | | | MFM.RX | I | LVCMOS | DVCC | – |
| | | | | A8 | I | Analog | DVCC | – |
| 44 | 35 | 38 | 27 | P3.3 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | OA2+(6) | I | Analog | DVCC | – |
| 45 | 36 | 1 | 28 | P3.2 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | OA2-(6) | I | Analog | DVCC | – |
| 46 | 37 | 2 | 29 | P3.1 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | OA2O(6) | O | Analog | DVCC | – |
| 47 | 38 | 3 | 30 | P3.0 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | MCLK | O | LVCMOS | DVCC | – |
| 48 | 39 | 4 | 31 | P1.3 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | | UCB0SOMI | I/O | LVCMOS | DVCC | – |
| | | | | UCB0SCL | I/O | LVCMOS | DVCC | – |
| | | | | OA0+(6) | I | Analog | DVCC | – |
| | | | | A3 | I | Analog | DVCC | – |

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## 4.3 Signal Descriptions

表 4-2 describes the signals for all device variants and package options.

**表 4-2. Signal Descriptions**

| FUNCTION | SIGNAL NAME | PIN NUMBER(1) | | | | PIN TYPE(2) | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| | | PT | RHA | DBT | RSM | | |
| ADC | A0 | 3 | 2 | 7 | 2 | I | Analog input A0 |
| | A1 | 2 | 1 | 6 | 1 | I | Analog input A1 |
| | A2 | 1 | 40 | 5 | 32 | I | Analog input A2 |
| | A3 | 48 | 39 | 4 | 31 | I | Analog input A3 |
| | A4 | 34 | 28 | 31 | 22 | I | Analog input A4 |
| | A5 | 33 | 27 | 30 | 21 | I | Analog input A5 |
| | A6 | 32 | 26 | 29 | 20 | I | Analog input A6 |
| | A7 | 31 | 25 | 28 | 19 | I | Analog input A7 |
| | A8 | 43 | 34 | 37 | – | I | Analog input A8 |
| | A9 | 42 | 33 | 36 | – | I | Analog input A9 |
| | A10 | 41 | – | – | – | I | Analog input A10 |
| | A11 | 40 | – | – | – | I | Analog input A11 |
| | Veref+ | 3 | 2 | 7 | 2 | I | ADC positive reference |
| | Veref- | 1 | 40 | 5 | 32 | I | ADC negative reference |
| eCOMP0 | C0 | 3 | 2 | 7 | 2 | I | Comparator input channel C0 |
| | C1 | 2 | 1 | 6 | 1 | I | Comparator input channel C1 |
| | COUT | 30 | 24 | 27 | 18 | O | Comparator output channel COUT |
| eCOMP1 | C0 | 10 | 9 | 14 | 9 | I | Comparator input channel C0 |
| | C1 | 11 | 10 | 15 | 10 | I | Comparator input channel C1 |
| | COUT | 29 | 23 | 26 | 17 | O | Comparator output channel COUT |
| SAC0(3) | OA0+ | 48 | 39 | 4 | 31 | I | SAC0, OA positive input |
| | OA0- | 1 | 40 | 5 | 32 | I | SAC0, OA negative input |
| | OA0O | 2 | 1 | 6 | 1 | O | SAC0, OA output |
| SAC1(3) | OA1+ | 31 | 25 | 28 | 19 | I | SAC1, OA positive input |
| | OA1- | 32 | 26 | 29 | 20 | I | SAC1, OA negative input |
| | OA1O | 33 | 27 | 30 | 21 | O | SAC1, OA output |
| SAC2(3) | OA2+ | 44 | 35 | 38 | 27 | I | SAC2, OA positive input |
| | OA2- | 45 | 36 | 1 | 28 | I | SAC2, OA negative input |
| | OA2O | 46 | 37 | 2 | 29 | O | SAC2, OA output |
| SAC3(3) | OA3+ | 35 | 29 | 32 | 23 | I | SAC3, OA positive input |
| | OA3- | 36 | 30 | 33 | 24 | I | SAC3, OA negative input |
| | OAO | 37 | 31 | 34 | 25 | O | SAC3, OA output |
| Clock | ACLK | 2 | 1 | 6 | 1 | O | ACLK output |
| | MCLK | 9 | 8 | 13 | 8 | O | MCLK output |
| | | 47 | 38 | 3 | 30 | O | |
| | SMCLK | 3 | 2 | 7 | 2 | O | SMCLK output |
| | | 38 | 32 | 35 | 26 | O | |
| | XIN | 8 | 7 | 12 | 7 | I | Input terminal for crystal oscillator |
| | XOUT | 9 | 8 | 13 | 8 | O | Output terminal for crystal oscillator |

(1) Any pin that is not bonded out in a smaller package must be initialized by software after reset to achieve the lowest leakage current.
(2) I = input, O = output, I/O = input/output, P = power
(3) MSP430FR235x devices only


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表 4-2. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NUMBER(1) | | | | PIN TYPE(2) | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| | | PT | RHA | DBT | RSM | | |
| Debug | SBWTCK | 4 | 3 | 8 | 3 | I | Spy-Bi-Wire input clock |
| | SBWTDIO | 5 | 4 | 9 | 4 | I/O | Spy-Bi-Wire data input/output |
| | TCK | 34 | 28 | 31 | 22 | I | Test clock |
| | TCLK | 32 | 26 | 29 | 20 | I | Test clock input |
| | TDI | 32 | 26 | 29 | 20 | I | Test data input |
| | TDO | 31 | 25 | 28 | 19 | O | Test data output |
| | TMS | 33 | 27 | 30 | 21 | I | Test mode select |
| | TEST | 4 | 3 | 8 | 3 | I | Test mode pin – selected digital I/O on JTAG pins |
| System | NMI | 5 | 4 | 9 | 4 | I | Nonmaskable interrupt input |
| | $\overline{\text{RST}}$ | 5 | 4 | 9 | 4 | I/O | Reset input, active-low |
| Power | DVCC | 6 | 5 | 10 | 5 | P | Power supply |
| | DVSS | 7 | 6 | 11 | 6 | P | Power ground |
| | VREF+ | 31 | 25 | 28 | 19 | P | Output of positive reference voltage with ground as reference |
| GPIO, Port 1 | P1.0 | 3 | 2 | 7 | 2 | I/O | General-purpose I/O |
| | P1.1 | 2 | 1 | 6 | 1 | I/O | General-purpose I/O |
| | P1.2 | 1 | 40 | 5 | 32 | I/O | General-purpose I/O |
| | P1.3 | 48 | 39 | 4 | 31 | I/O | General-purpose I/O |
| | P1.4 | 34 | 28 | 31 | 22 | I/O | General-purpose I/O (4) |
| | P1.5 | 33 | 27 | 30 | 21 | I/O | General-purpose I/O (4) |
| | P1.6 | 32 | 26 | 29 | 20 | I/O | General-purpose I/O(4) |
| | P1.7 | 31 | 25 | 28 | 19 | I/O | General-purpose I/O(4) |
| GPIO, Port 2 | P2.0 | 30 | 24 | 27 | 18 | I/O | General-purpose I/O |
| | P2.1 | 29 | 23 | 26 | 17 | I/O | General-purpose I/O |
| | P2.2 | 28 | 22 | 25 | – | I/O | General-purpose I/O |
| | P2.3 | 27 | 21 | 24 | – | I/O | General-purpose I/O |
| | P2.4 | 11 | 10 | 15 | 10 | I/O | General-purpose I/O |
| | P2.5 | 10 | 9 | 14 | 9 | I/O | General-purpose I/O |
| | P2.6 | 9 | 8 | 13 | 8 | I/O | General-purpose I/O |
| | P2.7 | 8 | 7 | 12 | 7 | I/O | General-purpose I/O |
| GPIO, Port 3 | P3.0 | 47 | 38 | 3 | 30 | I/O | General-purpose I/O |
| | P3.1 | 46 | 37 | 2 | 29 | I/O | General-purpose I/O |
| | P3.2 | 45 | 36 | 1 | 28 | I/O | General-purpose I/O |
| | P3.3 | 44 | 35 | 38 | 27 | I/O | General-purpose I/O |
| | P3.4 | 38 | 32 | 35 | 26 | I/O | General-purpose I/O |
| | P3.5 | 37 | 31 | 34 | 25 | I/O | General-purpose I/O |
| | P3.6 | 36 | 30 | 33 | 24 | I/O | General-purpose I/O |
| | P3.7 | 35 | 29 | 32 | 23 | I/O | General-purpose I/O |

(4) Because this pin is multiplexed with the JTAG function, TI recommends disabling the pin interrupt function while in JTAG debug to prevent collisions.
Functions shared with these four pins cannot be debugged if 4-wire JTAG is used for debug.

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表 4-2. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NUMBER(1) | | | | PIN TYPE(2) | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| | | PT | RHA | DBT | RSM | | |
| GPIO, Port 4 | P4.0 | 26 | 20 | 23 | 16 | I/O | General-purpose I/O |
| | P4.1 | 25 | 19 | 22 | 15 | I/O | General-purpose I/O |
| | P4.2 | 24 | 18 | 21 | 14 | I/O | General-purpose I/O |
| | P4.3 | 23 | 17 | 20 | 13 | I/O | General-purpose I/O |
| | P4.4 | 15 | 14 | 19 | – | I/O | General-purpose I/O |
| | P4.5 | 14 | 13 | 18 | – | I/O | General-purpose I/O |
| | P4.6 | 13 | 12 | 17 | 12 | I/O | General-purpose I/O |
| | P4.7 | 12 | 11 | 16 | 11 | I/O | General-purpose I/O |
| GPIO, Port 5 | P5.0 | 43 | 34 | 37 | – | I/O | General-purpose I/O |
| | P5.1 | 42 | 33 | 36 | – | I/O | General-purpose I/O |
| | P5.2 | 41 | – | – | – | I/O | General-purpose I/O |
| | P5.3 | 40 | – | – | – | I/O | General-purpose I/O |
| | P5.4 | 39 | – | – | – | I/O | General-purpose I/O |
| GPIO, Port 6 | P6.0 | 22 | 16 | – | – | I/O | General-purpose I/O |
| | P6.1 | 21 | 15 | – | – | I/O | General-purpose I/O |
| | P6.2 | 20 | – | – | – | I/O | General-purpose I/O |
| | P6.3 | 19 | – | – | – | I/O | General-purpose I/O |
| | P6.4 | 18 | – | – | – | I/O | General-purpose I/O |
| | P6.5 | 17 | – | – | – | I/O | General-purpose I/O |
| | P6.6 | 16 | – | – | – | I/O | General-purpose I/O |
| UART | UCA0TXD | 31 | 25 | 28 | 19 | O | eUSCI_A0 UART transmit data |
| | UCA0RXD | 32 | 26 | 29 | 20 | I | eUSCI_A0 UART receive data |
| | UCA1TXD | 23 | 17 | 20 | 13 | O | eUSCI_A1 UART transmit data |
| | UCA1RXD | 24 | 18 | 21 | 14 | I | eUSCI_A1 UART receive data |
| ISO | ISOTXD | 26 | 20 | 23 | 16 | O | ISO transmit data (the logical AND product of UCA1TXD and TB3.2B) |
| | ISORXD | 26 | 20 | 23 | 16 | I | ISO receive data (to UCA1RXD and TB3.CCI2B) |
| SPI | UCA0STE | 34 | 28 | 31 | 22 | I/O | eUSCI_A0 SPI slave transmit enable |
| | UCA0CLK | 33 | 27 | 30 | 21 | I/O | eUSCI_A0 SPI clock input/output |
| | UCA0SOMI | 32 | 26 | 29 | 20 | I/O | eUSCI_A0 SPI slave out/master in |
| | UCA0SIMO | 31 | 25 | 28 | 19 | I/O | eUSCI_A0 SPI slave in/master out |
| | UCA1STE | 26 | 20 | 23 | 16 | I/O | eUSCI_A1 SPI slave transmit enable |
| | UCA1CLK | 25 | 19 | 22 | 15 | I/O | eUSCI_A1 SPI clock input/output |
| | UCA1SOMI | 24 | 18 | 21 | 14 | I/O | eUSCI_A1 SPI slave out/master in |
| | UCA1SIMO | 23 | 17 | 20 | 13 | I/O | eUSCI_A1 SPI slave in/master out |
| | UCB0STE | 3 | 2 | 7 | 2 | I/O | eUSCI_B0 slave transmit enable |
| | UCB0CLK | 2 | 1 | 6 | 1 | I/O | eUSCI_B0 clock input/output |
| | UCB0SIMO | 1 | 40 | 5 | 32 | I/O | eUSCI_B0 SPI slave in/master out |
| | UCB0SOMI | 48 | 39 | 4 | 31 | I/O | eUSCI_B0 SPI slave out/master in |
| | UCB1STE | 15 | 14 | 19 | – | I/O | eUSCI_B1 slave transmit enable |
| | UCB1CLK | 14 | 13 | 18 | – | I/O | eUSCI_B1 clock input/output |
| | UCB1SIMO | 13 | 12 | 17 | – | I/O | eUSCI_B1 SPI slave in/master out |
| | UCB1SOMI | 12 | 11 | 16 | – | I/O | eUSCI_B1 SPI slave out/master in |
| $I^2C$ | UCB0SCL | 48 | 39 | 4 | 31 | I/O | eUSCI_B0 $I^2C$ clock |
| | UCB0SDA | 1 | 40 | 5 | 32 | I/O | eUSCI_B0 $I^2C$ data |
| | UCB1SCL | 12 | 11 | 16 | 11 | I/O | eUSCI_B1 $I^2C$ clock |
| | UCB1SDA | 13 | 12 | 17 | 12 | I/O | eUSCI_B1 $I^2C$ data |


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表 4-2. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NUMBER(1) | | | | PIN TYPE(2) | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| | | PT | RHA | DBT | RSM | | |
| Timer_B | TB0.1 | 32 | 26 | 29 | 20 | I/O | Timer TB0 CCR1<br>capture: CCI1A input, compare: Out1 output |
| | TB0.2 | 31 | 25 | 28 | 19 | I/O | Timer TB0 CCR2<br>capture: CCI2A input<br>compare: Out2 output |
| | TB0TRG | 1 | 40 | 5 | 32 | I | TB0 external trigger input for TB0OUTH |
| | TB0CLK | 8 | 7 | 12 | 7 | I | Timer clock input TBCLK for TB0 |
| | TB1.1 | 30 | 24 | 27 | 18 | I/O | Timer TB1 CCR1<br>capture: CCI1A input<br>compare: Out1 output |
| | TB1.2 | 29 | 23 | 26 | 17 | I/O | Timer TB1 CCR2<br>capture: CCI2A input<br>compare: Out2 output |
| | TB1CLK | 28 | 22 | 25 | – | I | Timer clock input TBCLK for TB1 |
| | TB1TRG | 27 | 21 | 24 | – | I | TB1 external trigger input for TB1OUTH |
| | TB2.1 | 43 | 34 | 37 | – | I/O | Timer TB2 CCR1<br>capture: CCI1A input<br>compare: Out1 output |
| | TB2.2 | 42 | 33 | 36 | – | I/O | Timer TB2 CCR2<br>capture: CCI2A input<br>compare: Out2 output |
| | TB2CLK | 41 | – | – | – | I | Timer clock input TBCLK for TB2 |
| | TB2TRG | 40 | – | – | – | I | TB2 external trigger input for TB2OUTH |
| | TB3.1 | 22 | 16 | – | – | I/O | Timer TB3 CCR1<br>capture: CCI1A input<br>compare: Out1 output |
| | TB3.2 | 21 | 15 | – | – | I/O | Timer TB3 CCR2<br>capture: CCI2A input<br>compare: Out2 output |
| | TB3.3 | 20 | – | – | – | I/O | Timer TB3 CCR3<br>capture: CCI3A input<br>compare: Out3 output |
| | TB3.4 | 19 | – | – | – | I/O | Timer TB3 CCR4<br>capture: CCI4A input<br>compare: Out4 output |
| | TB3.5 | 18 | – | – | – | I/O | Timer TB3 CCR5<br>capture: CCI5A input<br>compare: Out5 outputs |
| | TB3.6 | 17 | – | – | – | I/O | Timer TB3 CCR6<br>capture: CCI6A input<br>compare: Out6 output |
| | TB3CLK | 16 | – | – | – | I | Timer clock input TBCLK for TB3 |
| MFM | TX | 42 | 33 | 36 | – | O | Manchester function module transmit |
| | RX | 43 | 34 | 37 | – | I | Manchester function module receive |
| VQFN thermal pad | | – | Pad | – | Pad | – | Connect the exposed thermal pad to VSS. |

## 4.4 Pin Multiplexing

Pin multiplexing for these devices is controlled by both register settings and operating modes (for example, if the device is in test mode). For details of the settings for each pin and diagrams of the multiplexed ports, see 节 6.11.

## 4.5 Buffer Type

表 4-3 defines the pin buffer types that are listed in 表 4-1.

**表 4-3. Buffer Type**

| BUFFER TYPE (STANDARD) | NOMINAL VOLTAGE | HYSTERESIS | PU OR PD | NOMINAL PU OR PD STRENGTH (µA) | OUTPUT DRIVE STRENGTH (mA) | OTHER CHARACTERISTICS |
|---|---|---|---|---|---|---|
| LVCMOS | 3.0 V | Y (1) | Programmable | See 节 5.12.5 | See 节 5.12.5 | |
| Analog | 3.0 V | N | N/A | N/A | N/A | See the analog modules in 节 5 for details |
| Power (DVCC) | 3.0 V | N | N/A | N/A | N/A | SVS enables hysteresis on DVCC |
| Power (AVCC) | 3.0 V | N | N/A | N/A | N/A | |

(1) Only for input pins

## 4.6 Connection of Unused Pins

表 4-4 lists the correct termination of unused pins.

**表 4-4. Connection of Unused Pins(1)**

| PIN | POTENTIAL | COMMENT |
|---|---|---|
| Px.0 to Px.7 | Open | Set to port function, output direction (PxDIR.n = 1) |
| $\overline{\text{RST}}$/NMI | DVCC | 47-kΩ pullup or internal pullup selected with 10-nF (or 1.1-nF) pulldown(2) |
| TEST | Open | This pin always has an internal pulldown enabled. |

(1) Any unused pin with a secondary function that is shared with general-purpose I/O should follow the Px.0 to Px.7 unused pin connection guidelines.
(2) The pulldown capacitor should not exceed 1.1 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode with TI tools like FET interfaces or GANG programmers.


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# 5 Specifications

## 5.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | DEVICE GRADE | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage applied at DVCC pin to $V_{SS}$ | T | –0.3 | 4.1 | V |
| Voltage applied to any pin(2) | T | –0.3 | $V_{CC}$ + 0.3<br>4.1 V Max | V |
| Current across the whole chip including IO currents | T | | +50 | mA |
| Diode current at any device pin | T | | ±2 | mA |
| Maximum junction temperature, $T_J$ | T | | 115 | °C |
| Storage temperature, $T_{stg}$ (3) | T | –40 | 125 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) All voltages referenced to $V_{SS}$.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

## 5.2 ESD Ratings

over operating free-air temperature range (unless otherwise noted)

| | | | DEVICE GRADE | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | T | ±1000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | T | ±250 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±250 V may actually have higher performance.

## 5.3 Recommended Operating Conditions

| | | | DEVICE GRADE | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage applied at DVCC pin(1) (2)(3) (4) | | T | 1.8 | | 3.6 | V |
| $V_{SS}$ | Supply voltage applied at DVSS pin | | T | | 0 | | V |
| $T_A$ | Operating free-air temperature | | T | –40 | | 105 | °C |
| $T_J$ | Operating junction temperature | | T | –40 | | 115 | °C |
| $C_{DVCC}$ | Recommended capacitor at DVCC(5) | | T | 4.7 | 10 | | µF |
| $f_{SYSTEM}$ | Processor frequency (maximum MCLK frequency)(4)(6) | No FRAM wait states (NWAITSx = 0) | T | 0 | | 8 | MHz |
| | | With FRAM wait states (NWAITSx = 1)(7) | T | 0 | | 16 | |
| | | With FRAM wait states (NWAITSx = 2)(7) | T | 0 | | 24(8) | |

(1) Supply voltage changes faster than 0.2 V/µs can trigger a BOR reset even within the recommended supply voltage range. Following the data sheet recommendation for capacitor $C_{DVCC}$ limits the slopes accordingly.
(2) Modules can have a different supply voltage range specification. See the specification of the respective module in this data sheet.
(3) TI recommends that power to the DVCC pin must not exceed the limits specified in *Recommended Operating Conditions*. Exceeding the specified limits can cause malfunction of the device including erroneous writes to RAM and FRAM.
(4) The minimum supply voltage is defined by the SVS levels. See the SVS threshold parameters in 表 5-1.
(5) A capacitor tolerance of ±20% or better is required. A low-ESR ceramic capacitor of 100 nF (minimum) should be placed as close as possible (within a few millimeters) to the respective pin pair.
(6) Modules can have a different maximum input clock specification. See the specification of the respective module in this data sheet.
(7) Wait states only occur on actual FRAM accesses (that is, on FRAM cache misses). RAM and peripheral accesses are always executed without wait states.
(8) If clock sources such as HF crystals or the DCO with frequencies >24 MHz are used, the clock must be divided in the clock system to comply with this operating condition.

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## Recommended Operating Conditions *(continued)*

| | | DEVICE GRADE | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{ACLK}$ | Maximum ACLK frequency | T | | | 40 | kHz |
| $f_{SMCLK}$ | Maximum SMCLK frequency | T | | | 24 (8) | MHz |

## 5.4 Active Mode Supply Current Into $V_{CC}$ Excluding External Current

over operating free-air temperature range (unless otherwise noted) (1)

| PARAMETER | EXECUTION MEMORY | TEST CONDITIONS | DEVICE GRADE | Frequency ($f_{MCLK}$ = $f_{SMCLK}$) | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | 1 MHz 0 WAIT STATES (NWAITSx = 0) | 8 MHz 0 WAIT STATES (NWAITSx = 0) | 16 MHz 1 WAIT STATE (NWAITSx = 1) | 24 MHz 2 WAIT STATES (NWAITSx = 2) | |
| | | | | TYP MAX | TYP MAX | TYP MAX | TYP MAX | |
| $I_{AM,\ FRAM}$(0%) | FRAM 0% cache hit ratio | 3.0 V, 25°C | T | 555 | 3084 | 3411 | 3692 | µA |
| | | 3.0 V, 85°C | T | 575 | 3207 | 3519 | 3807 | |
| | | 3.0 V, 105°C | T | 583 | 3233 | 3545 | 3833 | |
| $I_{AM,\ FRAM}$(100%) | FRAM 100% cache hit ratio | 3.0 V, 25°C | T | 261 | 724 | 1245 | 1772 | µA |
| | | 3.0 V, 85°C | T | 272 | 742 | 1267 | 1800 | |
| | | 3.0 V, 105°C | T | 283 | 753 | 1281 | 1817 | |
| $I_{AM,\ RAM}$ (2) | RAM | 3.0 V, 25°C | T | 285 | 917 | 1627 | 2355 | µA |

(1) All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current. Characterized with program executing typical data processing.
$f_{ACLK}$ = 32768 Hz, $f_{MCLK}$ = $f_{SMCLK}$ = $f_{DCO}$ at specified frequency
Program and data entirely reside in FRAM. All execution is from FRAM.
(2) Program and data reside entirely in RAM. All execution is from RAM. No access to FRAM.

## 5.5 Active Mode Supply Current Per MHz

$V_{CC}$ = 3.0 V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | DEVICE GRADE | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $dI_{AM,FRAM}/df$ | Active mode current consumption per MHz, execution from FRAM, no wait states (1) | ($I_{AM,\ 75\%\ cache\ hit\ rate}$ at 8 MHz – $I_{AM,\ 75\%\ cache\ hit\ rate}$ at 1 MHz) / 7 MHz | T | | 142 | | µA/MHz |

(1) All peripherals are turned on in default settings.

## 5.6 Low-Power Mode LPM0 Supply Currents Into $V_{CC}$ Excluding External Current

$V_{CC}$ = 3.0 V, $T_A$ = 25°C (unless otherwise noted) (1) (2)

| PARAMETER | | $V_{CC}$ | DEVICE GRADE | FREQUENCY ($f_{SMCLK}$) | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | 1 MHz | 8 MHz | 16 MHz | 24 MHz | |
| | | | | TYP MAX | TYP MAX | TYP MAX | TYP MAX | |
| $I_{LPM0}$ | Low-power mode 0 supply current | 2.0 V | T | 199 | 312 | 437 | 637 | µA |
| | | 3.0 V | T | 211 | 324 | 449 | 649 | |

(1) All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current.
(2) Current for watchdog timer clocked by SMCLK included.
$f_{ACLK}$ = 32768 Hz, $f_{MCLK}$ = 0 MHz, $f_{SMCLK}$ at specified frequency.


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## 5.7 Low-Power Mode LPM3 and LPM4 Supply Currents (Into $V_{CC}$) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

| PARAMETER | | DEVICE GRADE | $V_{CC}$ | –40°C | | 25°C | | 85°C | | 105°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM3,XT1}$ | Low-power mode 3, includes SVS (2) (3) (4) | T | 3.0 V | 1.21 | | 1.49 | | 6.35 | 21.85 | 13.29 | 47.87 | µA |
| $I_{LPM3,XT1}$ | Low-power mode 3, includes SVS (2) (3) (4) | T | 2.0 V | 1.18 | | 1.45 | | 6.28 | | 13.17 | | µA |
| $I_{LPM3,VLO}$ | Low-power mode 3, VLO, excludes SVS (5) | T | 3.0 V | 1.01 | | 1.29 | | 6.15 | 21.65 | 13.1 | 47.67 | µA |
| $I_{LPM3,VLO}$ | Low-power mode 3, VLO, excludes SVS (5) | T | 2.0 V | 0.99 | | 1.26 | | 6.09 | | 12.98 | | µA |
| $I_{LPM3,\ RTC}$ | Low-power mode 3, RTC, excludes SVS (6) | T | 3.0 V | 1.15 | | 1.43 | | 6.29 | | 13.24 | | µA |
| $I_{LPM3,\ RTC}$ | Low-power mode 3, RTC, excludes SVS (6) | T | 2.0 V | 1.13 | | 1.41 | | 6.23 | | 13.13 | | µA |
| $I_{LPM4,\ SVS}$ | Low-power mode 4, includes SVS | T | 3.0 V | 0.74 | | 1.00 | | 5.83 | | 12.73 | | µA |
| $I_{LPM4,\ SVS}$ | Low-power mode 4, includes SVS | T | 2.0 V | 0.72 | | 0.98 | | 5.77 | | 12.62 | | µA |
| $I_{LPM4,}$ | Low-power mode 4, excludes SVS | T | 3.0 V | 0.56 | | 0.82 | | 5.64 | | 12.54 | | µA |
| $I_{LPM4,}$ | Low-power mode 4, excludes SVS | T | 2.0 V | 0.55 | | 0.81 | | 5.59 | | 12.45 | | µA |
| $I_{LPM4,\ RTC,\ VLO}$ | Low-power mode 4, RTC is sourced from VLO, excludes SVS (7) | T | 3.0 V | 0.66 | | 0.93 | | 5.76 | | 12.67 | | µA |
| $I_{LPM4,\ RTC,\ VLO}$ | Low-power mode 4, RTC is sourced from VLO, excludes SVS (7) | T | 2.0 V | 0.66 | | 0.92 | | 5.71 | | 12.58 | | µA |
| $I_{LPM4,\ RTC,\ XT1}$ | Low-power mode 4, RTC is sourced from XT1, excludes SVS (8) | T | 3.0 V | 1.06 | | 1.34 | | 6.21 | | 13.15 | | µA |
| $I_{LPM4,\ RTC,\ XT1}$ | Low-power mode 4, RTC is sourced from XT1, excludes SVS (8) | T | 2.0 V | 1.05 | | 1.33 | | 6.16 | | 13.05 | | µA |

(1) All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current
(2) Not applicable for devices with HF crystal oscillator only.
(3) Characterized with a Seiko Crystal SC-32S crystal with a load capacitance chosen to closely match the required load.
(4) Low-power mode 3, includes SVS test conditions:
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
$f_{XT1}$ = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(5) Low-power mode 3, VLO, excludes SVS test conditions:
Current for watchdog timer clocked by VLO included. RTC disabled. Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
$f_{XT1}$ = 32768 Hz, $f_{ACLK} = f_{MCLK} = f_{SMCLK}$ = 0 MHz
(6) RTC wakes every second with external 32768-Hz clock as source.
(7) Low-power mode 4, VLO, excludes SVS test conditions:
Current for RTC clocked by VLO included. RTC disabled. Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4),
$f_{XT1}$ = 32768 Hz, $f_{ACLK} = f_{MCLK} = f_{SMCLK}$ = 0 MHz
(8) Low-power mode 4, XT1, excludes SVS test conditions:
Current for RTC clocked by XT1 included. RTC disabled. Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPM4),
$f_{XT1}$ = 32768 Hz, $f_{ACLK} = f_{MCLK} = f_{SMCLK}$ = 0 MHz

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## 5.8 Low-Power Mode LPMx.5 Supply Currents (Into $V_{CC}$) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

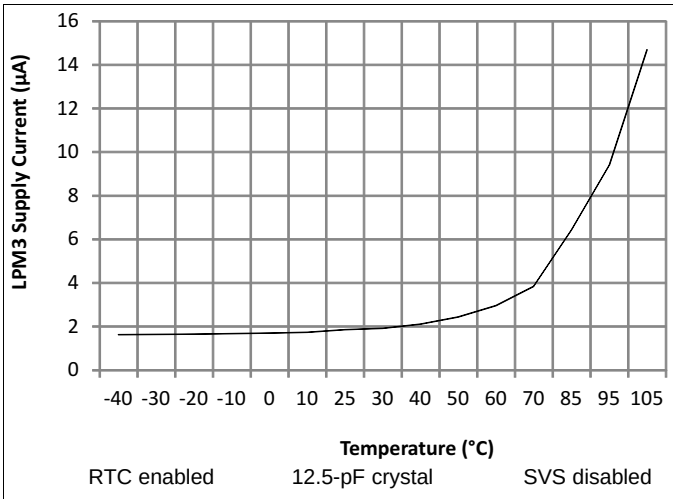
| PARAMETER | | DEVICE GRADE | $V_{CC}$ | –40°C | | 25°C | | 85°C | | 105°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM3.5,\ XT1}$ | Low-power mode 3.5, includes SVS(1) (2) (3) (also see 图 5-3) | T | 3.0 V | 0.57 | | 0.62 | | 0.89 | 2.06 | 1.27 | 3.21 | µA |
| $I_{LPM3.5,\ XT1}$ | Low-power mode 3.5, includes SVS(1) (2) (3) (also see 图 5-3) | T | 2.0 V | 0.55 | | 0.59 | | 0.84 | | 1.19 | | µA |
| $I_{LPM4.5,\ SVS}$ | Low-power mode 4.5, includes SVS(4) | T | 3.0 V | 0.27 | | 0.29 | | 0.41 | 0.63 | 0.61 | 1.13 | µA |
| $I_{LPM4.5,\ SVS}$ | Low-power mode 4.5, includes SVS(4) | T | 2.0 V | 0.25 | | 0.27 | | 0.37 | | 0.55 | | µA |
| $I_{LPM4.5}$ | Low-power mode 4.5, excludes SVS(5) | T | 3.0 V | 0.031 | | 0.042 | | 0.153 | 0.343 | 0.337 | 0.832 | µA |
| $I_{LPM4.5}$ | Low-power mode 4.5, excludes SVS(5) | T | 2.0 V | 0.025 | | 0.036 | | 0.128 | | 0.289 | | µA |

(1) Not applicable for devices with HF crystal oscillator only
(2) Characterized with a Seiko Crystal SC-32S crystal with a load capacitance chosen to closely match the required load.
(3) Low-power mode 3.5, includes SVS test conditions:
Current for RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
$f_{XT1}$ = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(4) Low-power mode 4.5, includes SVS test conditions:
Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
$f_{XT1}$ = 0 Hz, $f_{ACLK} = f_{MCLK} = f_{SMCLK}$ = 0 MHz
(5) Low-power mode 4.5, excludes SVS test conditions:
Current for brownout included. SVS disabled (SVSHE = 0). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
$f_{XT1}$ = 0 Hz, $f_{ACLK} = f_{MCLK} = f_{SMCLK}$ = 0 MHz


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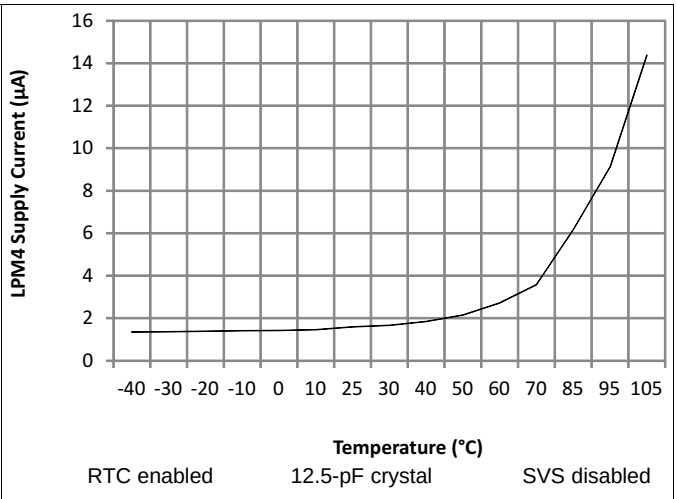
## 5.9 Production Distribution of LPM Supply Currents

$V_{CC}$ = 3 V



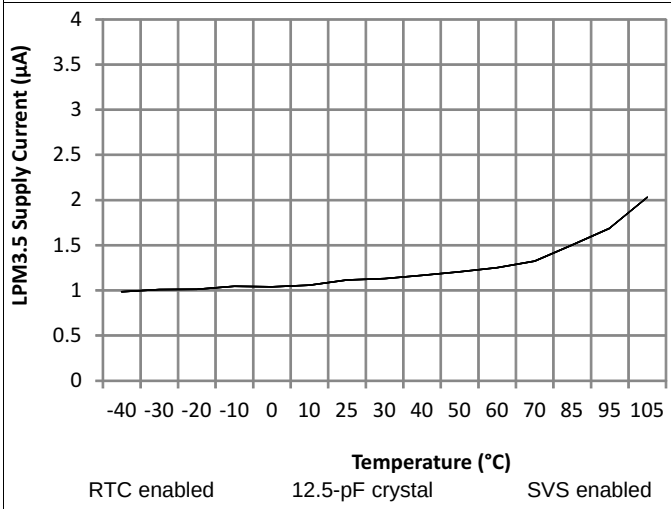

RTC enabled 12.5-pF crystal SVS disabled

**图 5-1. Population vs Low-Power Mode 3 Supply Current**



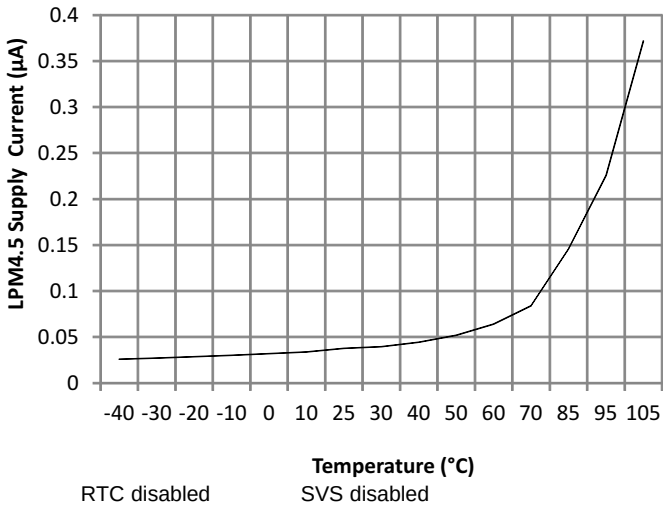

RTC enabled 12.5-pF crystal SVS disabled

**图 5-2. Population vs Low-Power Mode 4 Supply Current**




RTC enabled 12.5-pF crystal SVS enabled

**图 5-3. LPM3.5 Supply Current vs Temperature**




RTC disabled SVS disabled

**图 5-4. LPM4.5 Supply Current vs Temperature**

## 5.10 Typical Characteristics - Current Consumption Per Module

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| MODULE | TEST CONDITIONS | REFERENCE CLOCK | DEVICE GRADE | TYP | UNIT |
|---|---|---|---|---|---|
| Timer_B | | Module input clock | T | 5 | µA/MHz |
| eUSCI_A | UART mode | Module input clock | T | 7 | µA/MHz |
| eUSCI_A | SPI mode | Module input clock | T | 5 | µA/MHz |
| eUSCI_B | SPI mode | Module input clock | T | 5 | µA/MHz |
| eUSCI_B | $I^2C$ mode, 100 kbaud | Module input clock | T | 5 | µA/MHz |
| RTC | | 32 kHz | T | 85 | nA |
| CRC | From start to end of operation | MCLK | T | 8.5 | µA/MHz |

## 5.11 Thermal Resistance Characteristics

| THERMAL METRIC(1) | | | VALUE(2) | UNIT |
|---|---|---|---|---|
| $R\theta_{JA}$ | Junction-to-ambient thermal resistance, still air | QFP 48 pin (PT) | 67.6 | °C/W |
| | | QFN 40 pin (RHA) | 31.6 | |
| | | TSSOP 38 pin (DBT) | 67.0 | |
| | | QFN 32 pin (RSM) | 32.3 | |
| $R\theta_{JC}$ | Junction-to-case (top) thermal resistance | QFP 48 pin (PT) | 24.0 | °C/W |
| | | QFN 40 pin (RHA) | 24.1 | |
| | | TSSOP 38 pin (DBT) | 19.8 | |
| | | QFN 32 pin (RSM) | 27.8 | |
| $R\theta_{JB}$ | Junction-to-board thermal resistance | QFP 48 pin (PT) | 31.6 | °C/W |
| | | QFN 40 pin (RHA) | 12.6 | |
| | | TSSOP 38 pin (DBT) | 27.3 | |
| | | QFN 32 pin (RSM) | 11.8 | |

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC ($R\theta_{JC}$) value, which is based on a JEDEC-defined 1S0P system) and will change based on environment and application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*


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## 5.12 Timing and Switching Characteristics

### 5.12.1 Power Supply Sequencing

图 5-5 shows the power cycle and reset conditions.

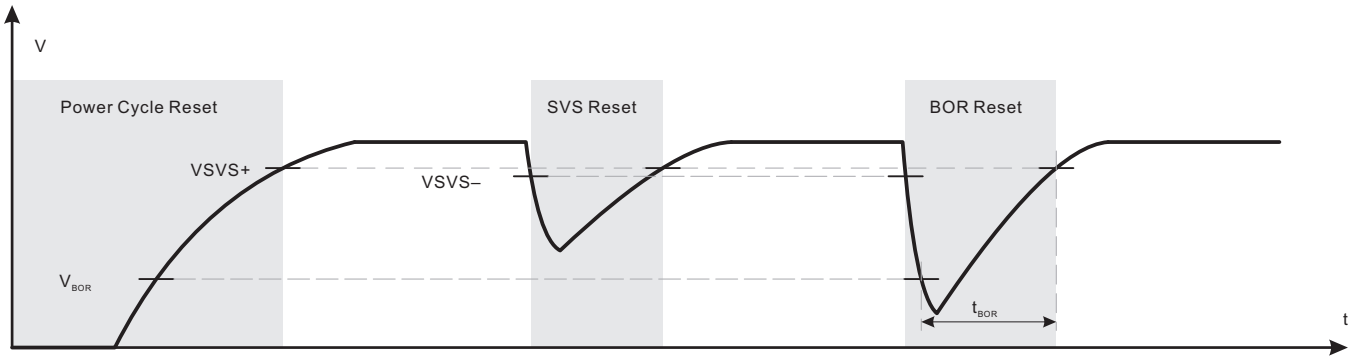



**图 5-5. Power Cycle, SVS, and BOR Reset Conditions**

表 5-1 lists the characteristics of the SVS and BOR.

**表 5-1. PMM, SVS and BOR**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | DEVICE GRADE | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{BOR, safe}$ | Safe BOR power-down level(1) | | T | 0.1 | | | V |
| $t_{BOR, safe}$ | Safe BOR reset delay(2) | | T | 10 | | | ms |
| $I_{SVSH,AM}$ | $SVS_H$ current consumption, active mode | $V_{CC}$ = 3.6 V | T | | | 1.5 | µA |
| $I_{SVSH,LPM}$ | $SVS_H$ current consumption, low-power modes | $V_{CC}$ = 3.6 V | T | | 240 | | nA |
| $V_{SVSH-}$ | $SVS_H$ power-down level(3) | | T | 1.71 | 1.80 | 1.87 | V |
| $V_{SVSH+}$ | $SVS_H$ power-up level(3) | | T | 1.76 | 1.88 | 1.99 | V |
| $V_{SVSH_hys}$ | $SVS_H$ hysteresis | | T | | 100 | | mV |
| $t_{PD,SVSH, AM}$ | $SVS_H$ propagation delay, active mode | | T | | | 10 | µs |
| $t_{PD,SVSH, LPM}$ | $SVS_H$ propagation delay, low-power modes | | T | | | 100 | µs |

(1) A safe BOR can only be correctly generated only if DVCC must drop below this voltage before it rises.
(2) When an BOR occurs, a safe BOR can only be correctly generated only if DVCC is kept low longer than this period before it reaches $V_{SVSH+}$.
(3) For additional information, see the Dynamic Voltage Scaling Power Solution for MSP430 Devices With Single-Channel LDO Reference Design.

### 5.12.2 Reset Timing

表 5-2 lists the device wake-up times.

**表 5-2. Wake-up Times From Low-Power Modes and Reset**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | DEVICE GRADE | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{WAKE-UP\ FRAM}$ | (Additional) wake-up time to activate the FRAM in AM if previously disabled through the FRAM controller or from a LPM if immediate activation is selected for wake-up (1) | | T | 3 V | | 10 | | µs |
| $t_{WAKE-UP\ LPM0}$ | Wake-up time from LPM0 to active mode (1) | | T | 3 V | | | 200 ns + 2.5 / $f_{DCO}$ | |
| $t_{WAKE-UP\ LPM3}$ | Wake-up time from LPM3 to active mode (1) | | T | 3 V | | 10 | | µs |
| $t_{WAKE-UP\ LPM4}$ | Wake-up time from LPM4 to active mode (2) | | T | 3 V | | 10 | | µs |
| $t_{WAKE-UP\ LPM3.5}$ | Wake-up time from LPM3.5 to active mode (2) | | T | 3 V | | 350 | | µs |
| $t_{WAKE-UP\ LPM4.5}$ | Wake-up time from LPM4.5 to active mode (2) | SVSHE = 1 | T | 3 V | | 350 | | µs |
| | | SVSHE = 0 | T | 3 V | | 1 | | ms |
| $t_{WAKE-UP-RESET}$ | Wake-up time from $\overline{RST}$ or BOR event to active mode (2) | | T | 3 V | | 1 | | ms |
| $t_{RESET}$ | Pulse duration required at $\overline{RST}$/NMI pin to accept a reset | | T | | 2 | | | µs |

(1) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) to the first externally observable MCLK clock edge.
(2) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) until the first instruction of the user program is executed.


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### 5.12.3 Clock Specifications

表 5-3 lists the characteristics of XT1 in low-frequency mode.

**表 5-3. XT1 Crystal Oscillator (Low Frequency)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)(2)

| PARAMETER | | TEST CONDITIONS | DEVICE GRADE | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{XT1,\ LF}$ | XT1 oscillator crystal, low frequency | LFXTBYPASS = 0 | T | | 32768 | | Hz |
| $DC_{XT1,\ LF}$ | XT1 oscillator LF duty cycle | Measured at MCLK, $f_{LFXT}$ = 32768 Hz | T | 30% | | 70% | |
| $f_{XT1,SW}$ | XT1 oscillator logic-level square-wave input frequency | LFXTBYPASS = 1(3)(4) | T | | 32768 | | Hz |
| $DC_{XT1,SW}$ | LFXT oscillator logic-level square-wave input duty cycle | LFXTBYPASS = 1 | T | 40% | | 60% | |
| $OA_{LFXT}$ | Oscillation allowance for LF crystals(5) | LFXTBYPASS = 0, LFXTDRIVE = {3}, $f_{LFXT}$ = 32768 Hz, $C_{L,eff}$ = 12.5 pF | T | | 200 | | kΩ |
| $C_{L,eff}$ | Integrated effective load capacitance(6) | (7) | T | | 1 | | pF |
| $t_{START,LFXT}$ | Start-up time(8) | $f_{OSC}$ = 32768 Hz, LFXTBYPASS = 0, LFXTDRIVE = {3}, $T_A$ = 25°C, $C_{L,eff}$ = 12.5 pF | T | | 1000 | | ms |
| $f_{Fault,LFXT}$ | Oscillator fault frequency(9) | XTS = 0(10) | T | 0 | | 3500 | Hz |

(1) To improve EMI on the LFXT oscillator, observe the following guidelines.
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) See MSP430 32-kHz Crystal Oscillators for details on crystal section, layout, and testing.
(3) When LFXTBYPASS is set, LFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger inputs section of this data sheet. Duty cycle requirements are defined by $DC_{LFXT,SW}$.
(4) Maximum frequency of operation of the entire device cannot be exceeded.
(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the LFXTDRIVE settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
- For LFXTDRIVE = {0}, $C_{L,eff}$ = 3.7 pF
- For LFXTDRIVE = {1}, 6 pF ≤ $C_{L,eff}$ ≤ 9 pF
- For LFXTDRIVE = {2}, 6 pF ≤ $C_{L,eff}$ ≤ 10 pF
- For LFXTDRIVE = {3}, 6 pF ≤ $C_{L,eff}$ ≤ 12 pF

(6) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
(7) Requires external capacitors at both terminals to meet the effective load capacitance specified by crystal manufacturers. Recommended effective load capacitance values supported are 3.7 pF, 6 pF, 9 pF, and 12.5 pF. Maximum shunt capacitance of 1.6 pF. The PCB adds additional capacitance, so it must also be considered in the overall capacitance. Verify that the recommended effective load capacitance of the selected crystal is met.
(8) Includes startup counter of 1024 clock cycles.
(9) Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag. A static condition or stuck at fault condition sets the flag.
(10) Measured with logic-level input frequency but also applies to operation with crystals.

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表 5-4 lists the characteristics of XT1 in high-frequency mode.

**表 5-4. XT1 Crystal Oscillator (High Frequency)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | DEVICE GRADE | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{HFXT}$ | HFXT oscillator crystal frequency, crystal mode | XT1BYPASS = 0, XTS = 1, XT1HFFREQ = 00 | T | 1 | | 4 | MHz |
| | | XT1BYPASS = 0, XTS = 1, XT1HFFREQ = 01 | T | 4.01 | | 6 | |
| | | XT1BYPASS = 0, XTS = 1, XT1HFFREQ = 10 | T | 6.01 | | 16 | |
| | | XT1BYPASS = 0, XTS = 1, XT1HFFREQ = 11 | T | 16.01 | | 24 | |
| $f_{HFXT,SW}$ | HFXT oscillator logic-level square-wave input frequency, bypass mode | XT1BYPASS = 1, XTS = 1 (2) (3) | T | 1 | | 24 | MHz |
| $DC_{HFXT}$ | HFXT oscillator duty cycle. | Measured at ACLK, $f_{HFXT,HF}$ = 4 MHz(4) | T | 40% | | 60% | |
| $DC_{HFXT,SW}$ | HFXT oscillator logic-level square-wave input duty cycle | XT1BYPASS = 1 | T | 40% | | 60% | |
| $OA_{HFXT}$ | Oscillation allowance for HFXT crystals(5) | XT1BYPASS = 0, XT1HFSEL = 1 $f_{HFXT,HF}$ = 24 MHz, $C_{L,eff}$ = 18 pF | T | | 3.1 | | Ω |
| $t_{START,HFXT}$ | Start-up time(6) | $f_{OSC}$ = 4 MHz, XTS = 1(4) XT1BYPASS = 0, XT1HFFREQ = 00, XT1DRIVE = 3, $T_A$ = 25°C, $C_{L,eff}$ = 18 pF | T | | 1.6 | | ms |
| | | $f_{OSC}$ = 24 MHz, XTS = 1(4) XT1BYPASS = 0, XT1HFFREQ = 00, XT1DRIVE = 3, $T_A$ = 25°C, $C_{L,eff}$ = 18 pF | T | | 1.1 | | |
| $C_{L,eff}$ | Integrated effective load capacitance(7) (8) | | T | | 1 | | pF |
| $f_{Fault,HFXT}$ | Oscillator fault frequency(9) (10) | | T | 0 | | 800 | kHz |

(1) To improve EMI on the HFXT oscillator, observe the following guidelines.
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) When XT1BYPASS is set, HFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this datasheet. Duty cycle requirements are defined by $DC_{HFXT,SW}$.
(3) Maximum frequency of operation of the entire device cannot be exceeded.
(4) The 4-MHz crystal used for lab characterization is the Abracon HC49/U AB-4.000MHZ-B2. The 16-MHz crystal used for lab characterization is the Abracon HC49/U AB-16.000MHZ-B2.
(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals.
(6) Includes startup counter of 4096 clock cycles.
(7) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Because the PCB adds additional capacitance, TI recommends verifying the correct load by measuring the oscillator frequency through MCLK or SMCLK. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
(8) Requires external capacitors at both terminals. Values are specified by crystal manufacturers. Recommended values supported are 14 pF, 16 pF, and 18 pF. The maximum shunt capacitance is 7 pF.
(9) Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag. A static condition or stuck at fault condition sets the flag.
(10) Measured with logic-level input frequency but also applies to operation with crystals.


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表 5-5 lists the frequency characteristics of the DCO FLL.

**表 5-5. DCO FLL, Frequency**

Over recommended operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | DEVICE GRADE | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $f_{DCO, FLL}$ | FLL lock frequency, 24 MHz, 25°C | Measured at MCLK, internal trimmed REFO as reference | T | 3.0 V | –1.0% | | 1.0% | |
| $f_{DCO, FLL}$ | FLL lock frequency, 24 MHz | Measured at MCLK, internal trimmed REFO as reference | T | 3.0 V | –2.0% | | 2.0% | |
| $f_{DCO, FLL}$ | FLL lock frequency, 24 MHz | Measured at MCLK, XT1 crystal as reference | T | 3.0 V | –0.5% | | 0.5% | |
| $f_{DUTY}$ | Duty cycle | Measured at MCLK, XT1 crystal as reference | T | 3.0 V | 40% | 50% | 60% | |
| $Jitter_{cc}$ | Cycle-to-cycle jitter, 24 MHz | Measured at MCLK, XT1 crystal as reference | T | 3.0 V | | 0.50% | | |
| $Jitter_{long}$ | Long-term Jitter, 24 MHz | Measured at MCLK, XT1 crystal as reference | T | 3.0 V | | 0.022% | | |
| $t_{FLL, lock}$ | FLL lock time | Measured at MCLK, XT1 crystal as reference | T | 3.0 V | | 200 | | ms |

表 5-6 lists the frequency characteristics of the DCO.

**表 5-6. DCO Frequency**

Over recommended operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | DEVICE GRADE | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $f_{DCO, 24MHz}$ | DCO frequency 24 MHz | DCORSEL = 111b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 0 | T | 3.0 V | | 12.6 | | MHz |
| | | DCORSEL = 111b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 511 | T | 3.0 V | | 20.5 | | |
| | | DCORSEL = 111b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 0 | T | 3.0 V | | 29.9 | | |
| | | DCORSEL = 111b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 511 | T | 3.0 V | | 48.2 | | |
| $f_{DCO, 20MHz}$ | DCO frequency 20 MHz | DCORSEL = 110b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 0 | T | 3.0 V | | 10.5 | | MHz |
| | | DCORSEL = 110b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 511 | T | 3.0 V | | 17.2 | | |
| | | DCORSEL = 110b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 0 | T | 3.0 V | | 25.1 | | |
| | | DCORSEL = 110b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 511 | T | 3.0 V | | 40.4 | | |
| $f_{DCO, 16MHz}$ | DCO frequency 16 MHz | DCORSEL = 101b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 0 | T | 3.0 V | | 8.3 | | MHz |
| | | DCORSEL = 101b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 511 | T | 3.0 V | | 13.6 | | |
| | | DCORSEL = 101b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 0 | T | 3.0 V | | 19.9 | | |
| | | DCORSEL = 101b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 511 | T | 3.0 V | | 32.2 | | |

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表 **5-6. DCO Frequency (continued)**

Over recommended operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | DEVICE GRADE | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $f_{DCO, 12MHz}$ | DCO frequency 12 MHz | DCORSEL = 100b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 0 | T | 3.0 V | | 6.2 | | MHz |
| | | DCORSEL = 100b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 511 | T | 3.0 V | | 10.2 | | |
| | | DCORSEL = 100b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 0 | T | 3.0 V | | 15 | | |
| | | DCORSEL = 100b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 511 | T | 3.0 V | | 24.3 | | |
| $f_{DCO, 8MHz}$ | DCO frequency 8 MHz | DCORSEL = 011b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 0 | T | 3.0 V | | 4.2 | | MHz |
| | | DCORSEL = 011b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 511 | T | 3.0 V | | 6.9 | | |
| | | DCORSEL = 011b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 0 | T | 3.0 V | | 10 | | |
| | | DCORSEL = 011b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 511 | T | 3.0 V | | 16.4 | | |
| $f_{DCO, 4MHz}$ | DCO frequency 4 MHz | DCORSEL = 010b,, DISMOD = 1b, DCOFTRIM = 000b, DCO = 0 | T | 3.0 V | | 2 | | MHz |
| | | DCORSEL = 010b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 511 | T | 3.0 V | | 3.4 | | |
| | | DCORSEL = 010b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 0 | T | 3.0 V | | 5 | | |
| | | DCORSEL = 010b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 511 | T | 3.0 V | | 8.2 | | |
| $f_{DCO, 2MHz}$ | DCO frequency 2 MHz | DCORSEL = 001b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 0 | T | 3.0 V | | 1 | | MHz |
| | | DCORSEL = 001b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 511 | T | 3.0 V | | 1.7 | | |
| | | DCORSEL = 001b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 0 | T | 3.0 V | | 2.5 | | |
| | | DCORSEL = 001b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 511 | T | 3.0 V | | 4.2 | | |
| $f_{DCO, 1MHz}$ | DCO frequency 1 MHz | DCORSEL = 000b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 0 | T | 3.0 V | | 0.5 | | MHz |
| | | DCORSEL = 000b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 511 | T | 3.0 V | | 0.85 | | |
| | | DCORSEL = 000b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 0 | T | 3.0 V | | 1.2 | | |
| | | DCORSEL = 000b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 511 | T | 3.0 V | | 2.1 | | |


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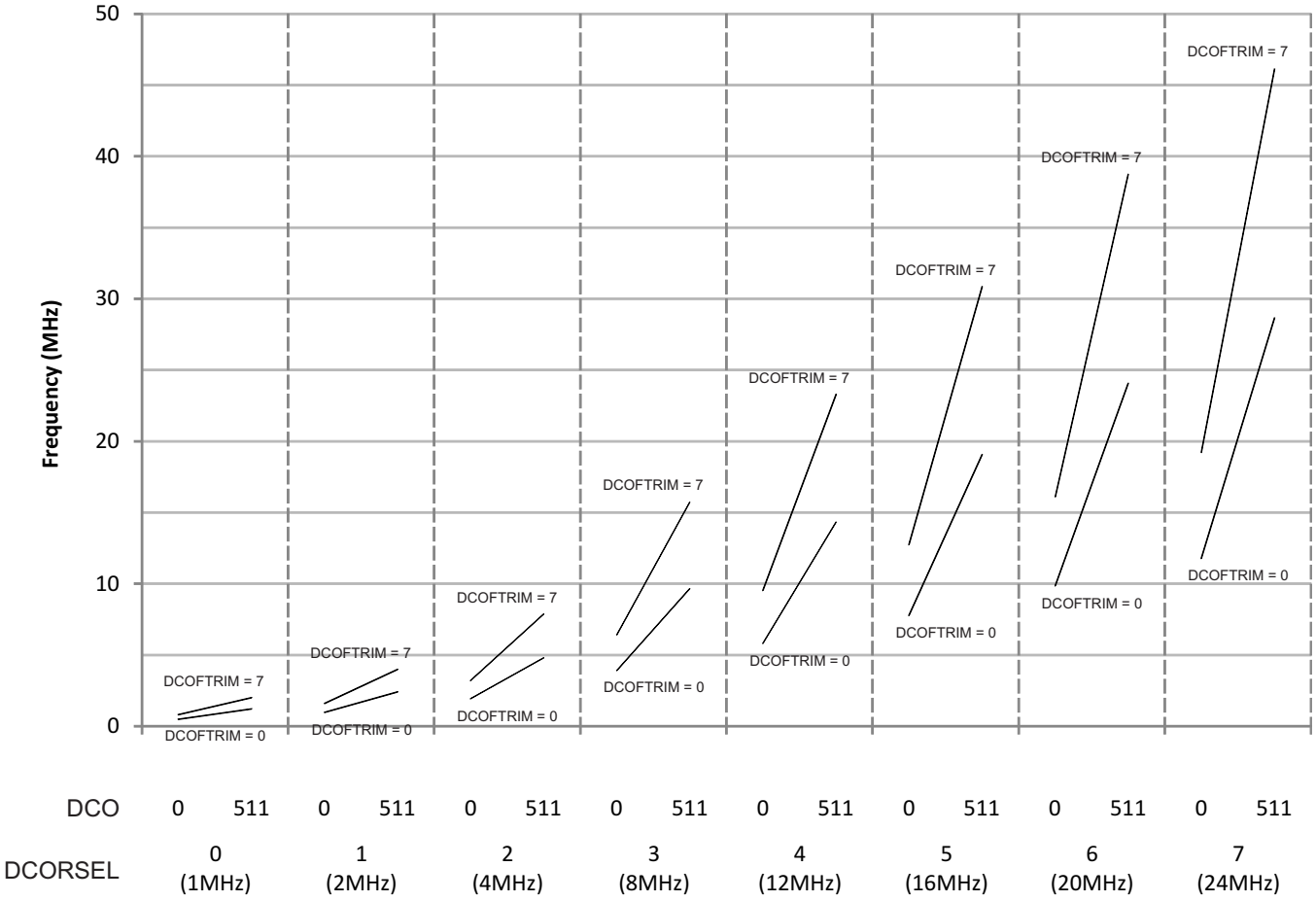



图 **5-6. Typical DCO Frequency**

表 5-7 lists the characteristics of the REFO.

**表 5-7. REFO**

over recommended operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | DEVICE GRADE | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_{REFO}$ | REFO oscillator current consumption | $T_A$ = 25°C, HP mode (REFLP = 0) | T | 3.0 V | | 15 | | µA |
| | REFO oscillator current consumption | $T_A$ = 25°C, LP mode (REFLP = 1) | T | 3.0 V | | 1 | | |
| $f_{REFO}$ | REFO calibrated frequency | Measured at MCLK | T | 3.0 V | | 32768 | | Hz |
| | REFO absolute calibrated tolerance | –40°C to 105°C | T | 1.8 V to 3.6 V | –3.5% | | +3.5% | |
| $df_{REFO}/d_T$ | REFO frequency temperature drift | Measured at MCLK (1) | T | 3.0 V | | 0.01 | | %/°C |
| $df_{REFO}/d_{VCC}$ | REFO frequency supply voltage drift | Measured at MCLK at 25°C (2) | T | 1.8 V to 3.6 V | | 1 | | %/V |
| $f_{DC}$ | REFO duty cycle | Measured at MCLK | T | 1.8 V to 3.6 V | 40% | 50% | 60% | |
| $t_{START}$ | REFO start-up time | 40% to 60% duty cycle, HP mode (REFLP = 0) | T | 3.0 V | | 72 | | µs |
| | | 40% to 60% duty cycle, LP mode (REFLP = 1) | T | 3.0 V | | 75 | | |

(1) Calculated using the box method: (MAX(–40°C to 105°C) – MIN(–40°C to 105°C)) / MIN(–40°C to 105°C) / (105°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

表 5-8 lists the characteristics of the VLO.

**表 5-8. Internal Very-Low-Power Low-Frequency Oscillator (VLO)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | DEVICE GRADE | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $f_{VLO}$ | VLO frequency | Measured at MCLK | T | 3.0 V | | 10 | | kHz |
| $df_{VLO}/d_T$ | VLO frequency temperature drift | Measured at MCLK (1) | T | 3.0 V | | 0.5 | | %/°C |
| $df_{VLO}/dV_{CC}$ | VLO frequency supply voltage drift | Measured at MCLK (2) | T | 1.8 V to 3.6 V | | 4 | | %/V |
| $f_{VLO,DC}$ | Duty cycle | Measured at MCLK | T | 3.0 V | | 50% | | |

(1) Calculated using the box method: (MAX(–40°C to 105°C) – MIN(–40°C to 105°C)) / MIN(–40°C to 105°C) / (105°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

注

The VLO clock frequency is reduced by 15% (typical) when the device switches from active mode to LPM3 or LPM4, because the reference changes. This lower frequency is not a violation of the VLO specifications (see 表 5-8).


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表 5-9 lists the characteristics of the MODOSC.

**表 5-9. Module Oscillator (MODOSC)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | DEVICE GRADE | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{MODOSC}$ | MODOSC frequency | T | 3.0 V | 3.0 | 3.8 | 4.6 | MHz |
| $f_{MODOSC}/dT$ | MODOSC frequency temperature drift(1) | T | 3.0 V | | 0.102 | | %/℃ |
| $f_{MODOSC}/dV_{CC}$ | MODOSC frequency supply voltage drift | T | 1.8 V to 3.6 V | | 1.17 | | %/V |
| $f_{MODOSC,DC}$ | Duty cycle | T | 3.0 V | 40% | 50% | 60% | |

(1) Calculated using the box method: (MAX(–40°C to 105°C) – MIN(–40°C to 105°C)) / MIN(–40°C to 105°C) / (105°C – (–40°C))

### 5.12.4 Internal Shared Reference

表 5-10 lists the characteristics of the internal shared reference.

**表 5-10. Internal Shared Reference**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | DEVICE GRADE | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{SENSOR}$ | Temperature sensor voltage | $T_J$ = 30℃ | T | 2.0 V, 3.0 V | | 788 | | mV |
| $TC_{SENSOR}$ | Temperature sensor coefficient | $T_J$ = 30℃ | T | | | 2.32 | | mV/°C |
| $V_{eCOMP, LP}$ | Low-power threshold for eCOMP | $T_J$ = 30℃ | T | 2.0 V, 3.0 V | | 1.20 | | V |
| $V_{REF+, Output}$ | Positive output reference at VREF+ pin | $T_J$ = 30℃ | T | 2.0 V, 3.0 V | | 1.20 | | V |
| The following parameters are for the 1.5-V, 2.0-V, and 2.5-V internal reference only and cannot be output to the VREF+ pin. | | | | | | | | |
| $V_{REF+, built-in}$ | Positive built-in reference voltage as internal reference | REFVSEL = {2} for 2.5 V, INTREFEN = 1 | T | 3.0 V | | 2.5 | ±1.5% | V |
| | | REFVSEL = {1} for 2.0 V, INTREFEN = 1 | T | 2.5 V | | 2.0 | ±1.5% | |
| | | REFVSEL = {0} for 1.5 V, INTREFEN = 1 | T | 1.8 V | | 1.5 | ±1.8% | |
| Noise | RMS noise at VREF (1) | From 0.1 Hz to 10 Hz, REFVSEL = {0} | T | | | 30 | 130 | µV |
| $V_{OS_BUF_INT}$ | VREF ADC BUF_INT buffer offset(2) | $T_A$ = 25 °C , ADC ON, REFVSEL = {0}, INTREFEN = 1, EXTREFEN=0 | T | | –16 | | +16 | mV |
| $V_{OS_BUF_EXT}$ | VREF ADC BUF_EXT buffer offset(3) | $T_A$ = 25 °C, REFVSEL = {0} , EXTREFEN = 1, INTREFEN = 1 or ADC ON | T | | –16 | | +16 | mV |
| $DV_{CC(min)}$ | DVCC minimum voltage, Positive built-in reference active | REFVSEL = {0} for 1.5 V | T | | 1.8 | | | V |
| | | REFVSEL = {1} for 2.0 V | T | | 2.2 | | | |
| | | REFVSEL = {2} for 2.5 V | T | | 2.7 | | | |
| $I_{REF+}$ | Operating supply current into DVCC terminal(4) | INTREFEN = 1 | T | 3 V | | 19 | 26 | µA |
| $I_{REF+_ADC_BUF}$ | Operating supply current into DVCC terminal(4) | ADC ON, EXTREFEN = 0, REFVSEL = {0, 1, 2} | T | 3 V | | 247 | 400 | µA |

(1) Internal reference noise affects ADC performance when ADC uses internal reference.
(2) Buffer offset affects ADC gain error and thus total unadjusted error.
(3) Buffer offset affects ADC gain error and thus total unadjusted error.
(4) The internal reference current is supplied through the DVCC terminal.

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表 **5-10. Internal Shared Reference (continued)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | DEVICE GRADE | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_{O(VREF+)}$ | VREF maximum load current, VREF+ terminal | REFVSEL = {0, 1, 2}, $DV_{CC} = DV_{CC(min)}$ for each reference level, INTREFEN = EXTREFEN = 1 | T | 3 V | –1000 | | +10 | µA |
| ΔVout/ ΔIo(VREF+) | Load-current regulation, VREF+ terminal | REFVSEL = {0, 1, 2}, $I_{O(VREF+)}$ = +10 µA or –1000 µA, $DV_{CC} = DV_{CC(min)}$ for each reference level, INTREFEN = EXTREFEN = 1 | T | 3 V | | | 1500 | µV/mA |
| $C_{VREF+/-}$ | Capacitance at VREF+ and VREF- terminals | INTREFEN = EXTREFEN = 1 | T | 3 V | 0 | | 100 | pF |
| $TC_{REF+}$ | Temperature coefficient of built-in reference | REFVSEL = {0, 1, 2}, INTREFEN = EXTREFEN = 1, $T_A$ = –40°C to 105°C (5) | T | 3 V | | 24 | 50 | ppm/K |
| PSRR_DC | Power supply rejection ratio (DC) | $DV_{CC} = DV_{CC\ (min)}$ to $DV_{CC(max)}$, $T_A$ = 25°C, REFVSEL = {0, 1, 2}, INTREFEN = EXTREFEN = 1 | T | 3 V | | 100 | 400 | µV/V |
| PSRR_AC | Power supply rejection ratio (ac) | $dDV_{CC}$= 0.1 V at 1 kHz | T | 3 V | | 3.0 | | mV/V |
| $t_{SETTLE}$ | Settling time of reference voltage (6) | $DV_{CC} = DV_{CC(min)}$ to $DV_{CC(max)}$, REFVSEL = {0, 1, 2}, INTREFEN = 0 → 1 | T | 3 V | | 75 | 100 | µs |

(5) Calculated using the box method: (MAX(–40°C to 105°C) – MIN(–40°C to 105°C)) / MIN(–40°C to 105°C) / (105°C – (–40°C))
(6) The condition is that the error in a conversion started after $t_{REFON}$ is less than ±0.5 LSB.


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### 5.12.5 General-Purpose I/Os

表 5-11 lists the characteristics of the digital inputs.

**表 5-11. Digital Inputs**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | DEVICE GRADE | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going input threshold voltage | | T | 2.0 V | 0.90 | | 1.50 | V |
| | | | T | 3.0 V | 1.35 | | 2.25 | |
| $V_{IT-}$ | Negative-going input threshold voltage | | T | 2.0 V | 0.50 | | 1.10 | V |
| | | | T | 3.0 V | 0.75 | | 1.65 | |
| $V_{hys}$ | Input voltage hysteresis ($V_{IT+} - V_{IT-}$) | | T | 2.0 V | 0.3 | | 0.8 | V |
| | | | T | 3.0 V | 0.4 | | 1.2 | |
| $R_{Pull}$ | Pullup or pulldown resistor | For pullup: $V_{IN} = V_{SS}$, For pulldown: $V_{IN} = V_{CC}$ | T | | 20 | 35 | 50 | kΩ |
| $C_{I,dig}$ | Input capacitance, digital only port pins | $V_{IN} = V_{SS}$ or $V_{CC}$ | T | | | 3 | | pF |
| $C_{I,ana}$ | Input capacitance, port pins with shared analog functions | $V_{IN} = V_{SS}$ or $V_{CC}$ | T | | | 5 | | pF |
| $I_{lkg(Px.y)}$ | High-impedance leakage current (1) (2) | | T | 2.0 V, 3.0 V | –30 | | +30 | nA |
| $t_{(int)}$ | External interrupt timing (external trigger pulse duration to set interrupt flag) (3) | Ports with interrupt capability (see block diagram and terminal function descriptions) | T | 2.0 V, 3.0 V | 50 | | | ns |

(1) The leakage current is measured with $V_{SS}$ or $V_{CC}$ applied to the corresponding pins, unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.
(3) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It can be set by trigger signals shorter than $t_{(int)}$.

表 5-12 lists the characteristics of the digital outputs.

**表 5-12. Digital Outputs**

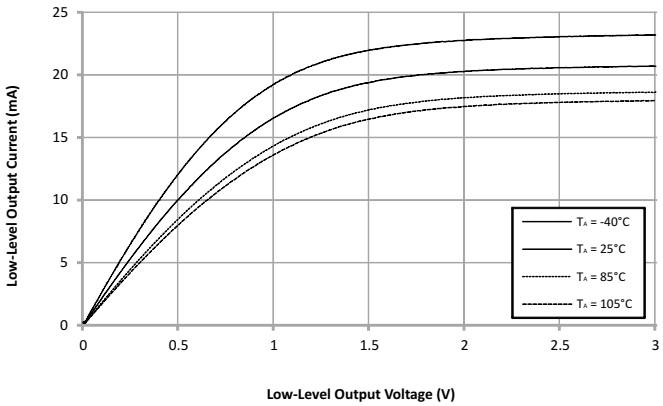
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | DEVICE GRADE | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{(OHmax)}$ = –3 mA (1) | T | 2.0 V | 1.4 | | 2.0 | V |
| | | $I_{(OHmax)}$ = –5 mA (1) | T | 3.0 V | 2.4 | | 3.0 | |
| $V_{OL}$ | Low-level output voltage | $I_{(OLmax)}$ = 3 mA (1) | T | 2.0 V | 0.0 | | 0.60 | V |
| | | $I_{(OLmax)}$ = 5 mA (1) | T | 3.0 V | 0.0 | | 0.60 | |
| $f_{Port_CLK}$ | Clock output frequency | Applicable to all IO ports, $C_L$ = 20 pF (2) | T | 2.0 V | 16 | | | MHz |
| | | | T | 3.0 V | 16 | | | |
| | | IOs multiplexed with MCLK and SMCLK, $C_L$ = 10 pF (2) | T | 2.0 V | 24 | | | |
| | | | T | 3.0 V | 24 | | | |
| $t_{rise,dig}$ | Port output rise time, digital only port pins | $C_L$ = 20 pF | T | 2.0 V | | 10 | | ns |
| | | | T | 3.0 V | | 7 | | |
| $t_{fall,dig}$ | Port output fall time, digital only port pins | $C_L$ = 20 pF | T | 2.0 V | | 10 | | ns |
| | | | T | 3.0 V | | 5 | | |

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The port can output frequencies at least up to the specified limit and might support higher frequencies.

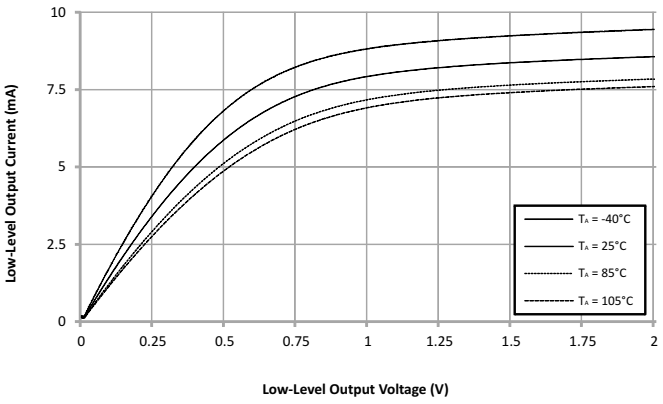
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### 5.12.6 Digital I/O Typical Characteristics



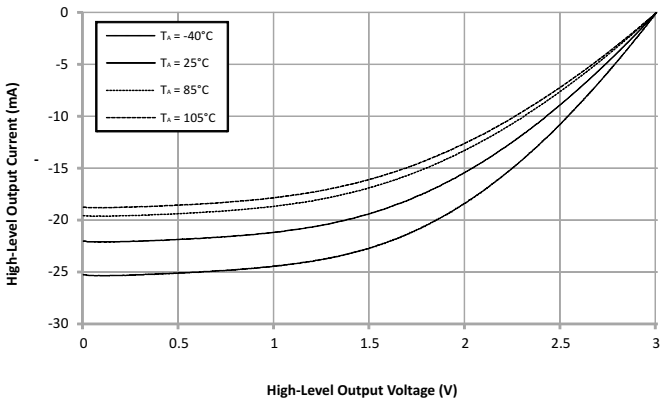

DVCC = 3 V

**图 5-7. Typical Low-Level Output Current vs Low-Level Output Voltage**



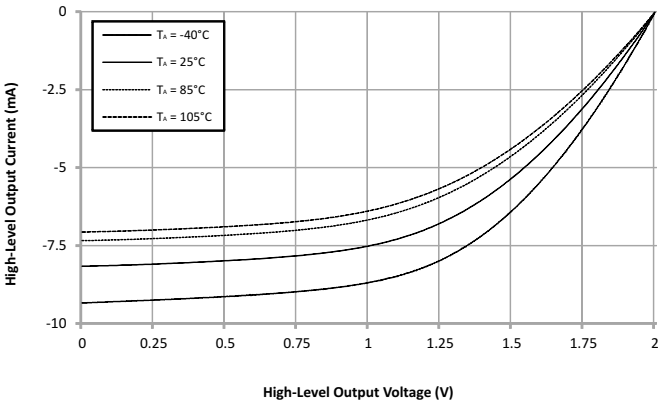

DVCC = 2 V

**图 5-8. Typical Low-Level Output Current vs Low-Level Output Voltage**




DVCC = 3 V

**图 5-9. Typical High-Level Output Current vs High-Level Output Voltage**




DVCC = 2 V

**图 5-10. Typical High-Level Output Current vs High-Level Output Voltage**


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### 5.12.7 Timer_B

表 5-13 lists the frequency characteristics of Timer_B.

**表 5-13. Timer_B**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | DEVICE GRADE | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $f_{TB}$ | Timer_B input clock frequency | Internal: SMCLK or ACLK,<br>External: TBCLK,<br>Duty cycle = 50% ±10% | T | 2.0 V,<br>3.0 V | | | 24 | MHz |
| $t_{TB,cap}$ | Timer_B capture timing | All capture inputs, minimum pulse duration required for capture | T | 2.0 V,<br>3.0 V | 20 | | | ns |

### 5.12.8 eUSCI

表 5-14 lists the supported frequencies of the eUSCI in UART mode.

**表 5-14. eUSCI (UART Mode) Clock Frequencies**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | DEVICE GRADE | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $f_{eUSCI}$ | eUSCI input clock frequency | Internal: SMCLK or MODCLK,<br>External: UCLK,<br>Duty cycle = 50% ±10% | T | 2.0 V,<br>3.0 V | | | 24 | MHz |
| $f_{BITCLK}$ | BITCLK clock frequency<br>(equals baud rate in Mbaud) | | T | 2.0 V,<br>3.0 V | | | 5 | MHz |

表 5-15 lists the switching characteristics of the eUSCI in UART mode.

**表 5-15. eUSCI (UART Mode) Switching Characteristics**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | DEVICE GRADE | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_t$ | UART receive deglitch time (1) | UCGLITx = 0 | T | 2.0 V,<br>3.0 V | | 12 | | ns |
| | | UCGLITx = 1 | | | | 40 | | |
| | | UCGLITx = 2 | | | | 68 | | |
| | | UCGLITx = 3 | | | | 110 | | |

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To make sure that pulses are correctly recognized their width should exceed the maximum specification of the deglitch time.

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表 5-16 lists the supported frequencies of the eUSCI in SPI master mode.

**表 5-16. eUSCI (SPI Master Mode) Clock Frequency**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | DEVICE GRADE | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $f_{eUSCI}$ | eUSCI input clock frequency | Internal: SMCLK, Duty cycle = 50% ±10% | T | | | | 8 | MHz |

表 5-17 lists the switching characteristics of the eUSCI in SPI master mode.

**表 5-17. eUSCI (SPI Master Mode) Switching Characteristics**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | DEVICE GRADE | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{STE,LEAD}$ | STE lead time, STE active to clock | UCSTEM = 1, UCMODEx = 01 or 10 | T | | 1 | | | UCxCLK cycles |
| $t_{STE,LAG}$ | STE lag time, Last clock to STE inactive | UCSTEM = 1, UCMODEx = 01 or 10 | T | | 1 | | | UCxCLK cycles |
| $t_{SU,MI}$ | SOMI input data setup time | | T | 2.0 V | 60 | | | ns |
| | | | | 3.0 V | 42 | | | |
| $t_{HD,MI}$ | SOMI input data hold time | | T | 2.0 V | 0 | | | ns |
| | | | | 3.0 V | 0 | | | |
| $t_{VALID,MO}$ | SIMO output data valid time(2) | UCLK edge to SIMO valid, $C_L$ = 20 pF | T | 2.0 V | | | 20 | ns |
| | | | | 3.0 V | | | 20 | |
| $t_{HD,MO}$ | SIMO output data hold time(3) | $C_L$ = 20 pF | T | 2.0 V | –9.0 | | | ns |
| | | | | 3.0 V | –6.0 | | | |

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} = \max(t_{VALID,MO(eUSCI)} + t_{SU,SI(Slave)}, t_{SU,MI(eUSCI)} + t_{VALID,SO(Slave)})$
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.

(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in 图 5-11 and 图 5-12.

(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in 图 5-11 and 图 5-12.


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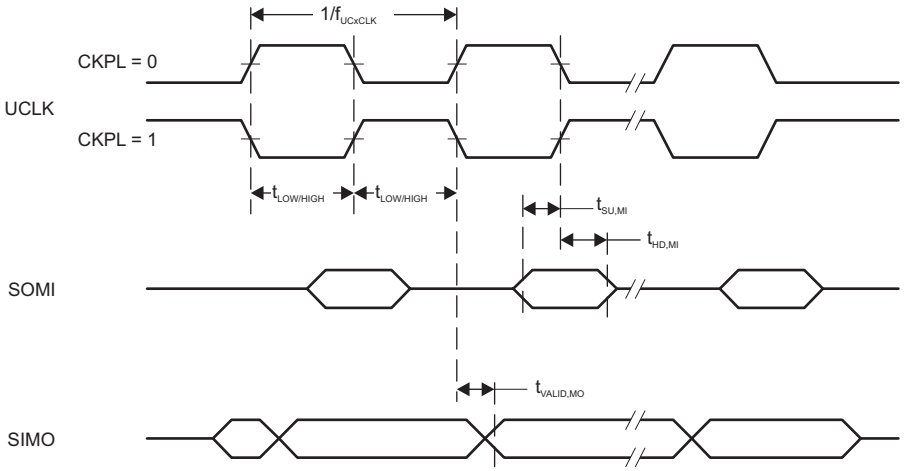



图 **5-11. SPI Master Mode, CKPH = 0**

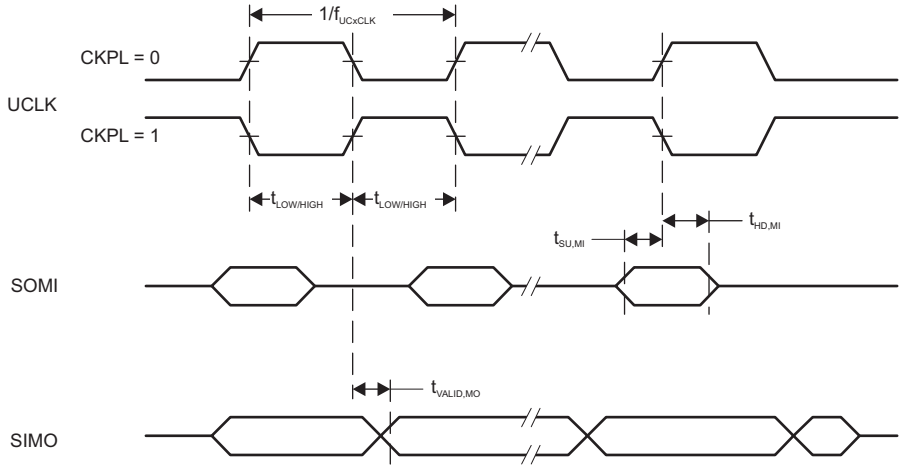



图 **5-12. SPI Master Mode, CKPH = 1**

表 5-18 lists the switching characteristics of the eUSCI in SPI slave mode.

**表 5-18. eUSCI (SPI Slave Mode) Switching Characteristics**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | DEVICE GRADE | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{STE,LEAD}$ | STE lead time, STE active to clock | | T | 2.0 V | 55 | | | ns |
| | | | | 3.0 V | 45 | | | |
| $t_{STE,LAG}$ | STE lag time, last clock to STE inactive | | T | 2.0 V | 20 | | | ns |
| | | | | 3.0 V | 20 | | | |
| $t_{STE,ACC}$ | STE access time, STE active to SOMI data out | | T | 2.0 V | | | 65 | ns |
| | | | | 3.0 V | | | 40 | |
| $t_{STE,DIS}$ | STE disable time, STE inactive to SOMI high impedance | | T | 2.0 V | | | 40 | ns |
| | | | | 3.0 V | | | 35 | |
| $t_{SU,SI}$ | SIMO input data setup time | | T | 2.0 V | 10 | | | ns |
| | | | | 3.0 V | 6 | | | |
| $t_{HD,SI}$ | SIMO input data hold time | | T | 2.0 V | 12 | | | ns |
| | | | | 3.0 V | 12 | | | |
| $t_{VALID,SO}$ | SOMI output data valid time(2) | UCLK edge to SOMI valid, $C_L$ = 20 pF | T | 2.0 V | | | 69 | ns |
| | | | | 3.0 V | | | 42 | |
| $t_{HD,SO}$ | SOMI output data hold time (3) | $C_L$ = 20 pF | T | 2.0 V | 5 | | | ns |
| | | | | 3.0 V | 5 | | | |

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.
(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in 图 5-13 and 图 5-14.
(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in 图 5-13 and 图 5-14.


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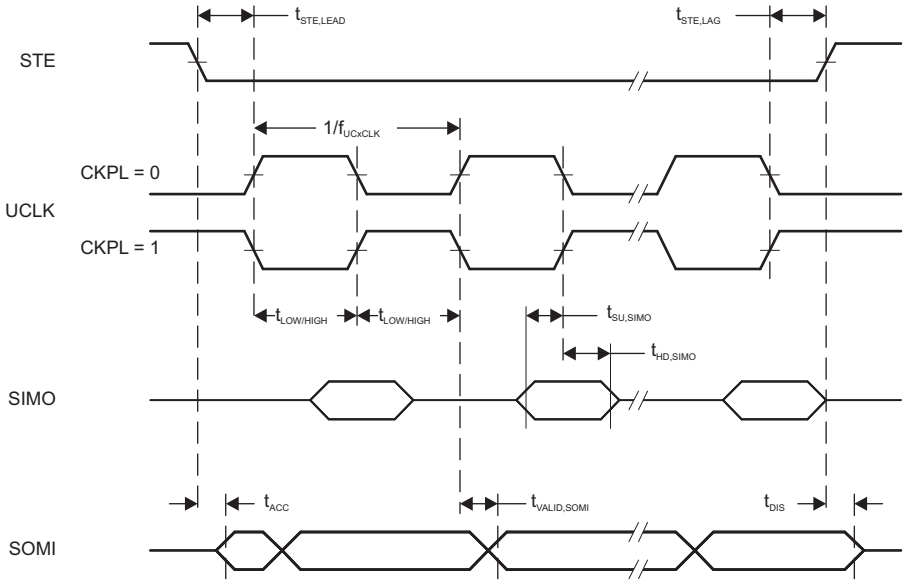



**图 5-13. SPI Slave Mode, CKPH = 0**

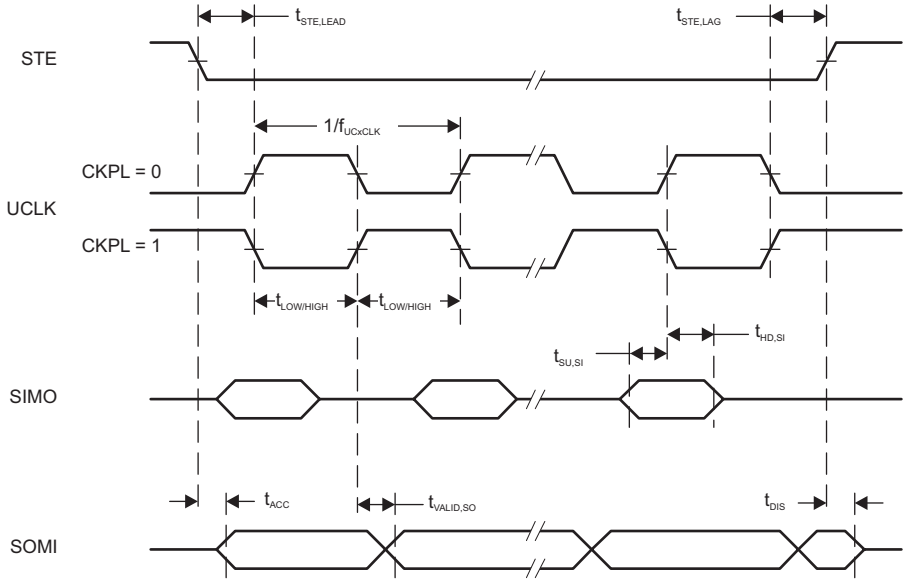



**图 5-14. SPI Slave Mode, CKPH = 1**

表 5-19 lists the switching characteristics of the eUSCI in I²C mode.

**表 5-19. eUSCI (I²C Mode) Switching Characteristics**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 5-15)

| PARAMETER | | TEST CONDITIONS | DEVICE GRADE | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $f_{eUSCI}$ | eUSCI input clock frequency | Internal: SMCLK or MODCLK, External: UCLK Duty cycle = 50% ±10% | T | 2.0 V, 3.0 V | | | 24 | MHz |
| $f_{SCL}$ | SCL clock frequency | | T | 2.0 V, 3.0 V | 0 | | 400 | kHz |
| $t_{HD,STA}$ | Hold time (repeated) START | $f_{SCL}$ = 100 kHz | T | 2.0 V, 3.0 V | 4.0 | | | µs |
| | | $f_{SCL}$ > 100 kHz | | | 0.6 | | | |
| $t_{SU,STA}$ | Setup time for a repeated START | $f_{SCL}$ = 100 kHz | T | 2.0 V, 3.0 V | 4.7 | | | µs |
| | | $f_{SCL}$ > 100 kHz | | | 0.6 | | | |
| $t_{HD,DAT}$ | Data hold time | | T | 2.0 V, 3.0 V | 0 | | | ns |
| $t_{SU,DAT}$ | Data setup time | | T | 2.0 V, 3.0 V | 250 | | | ns |
| $t_{SU,STO}$ | Setup time for STOP | $f_{SCL}$ = 100 kHz | T | 2.0 V, 3.0 V | 4.0 | | | µs |
| | | $f_{SCL}$ > 100 kHz | | | 0.6 | | | |
| $t_{SP}$ | Pulse duration of spikes suppressed by input filter | UCGLITx = 0 | T | 2.0 V, 3.0 V | 50 | | 600 | ns |
| | | UCGLITx = 1 | | | 25 | | 300 | |
| | | UCGLITx = 2 | | | 12.5 | | 150 | |
| | | UCGLITx = 3 | | | 6.3 | | 75 | |
| $t_{TIMEOUT}$ | Clock low time-out | UCCLTOx = 1 | T | 2.0 V, 3.0 V | | 36 | | ms |
| | | UCCLTOx = 2 | | | | 40 | | |
| | | UCCLTOx = 3 | | | | 44 | | |

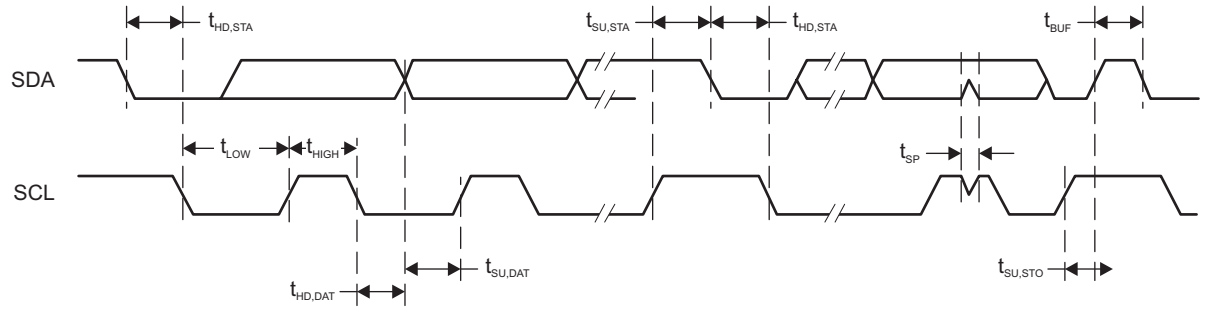



**图 5-15. I²C Mode Timing**


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### 5.12.9 ADC

表 5-20 lists the input characteristics of the ADC.

**表 5-20. ADC, Power Supply and Input Range Conditions**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | DEVICE GRADE | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $DV_{CC}$ | ADC supply voltage(1) | | T | | 2.0 | | 3.6 | V |
| $V_{(Ax)}$ | Analog input voltage range | All ADC pins | T | | 0 | | $DV_{CC}$ | V |
| $I_{ADC}$ | Operating supply current into DVCC terminal, reference current not included, repeat-single-channel mode | $f_{ADCCLK}$ = 5 MHz, ADCON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADCDIV = 0, ADCCONSEQx = 10b | T | 2.0 V | | 185 | | µA |
| | | | | 3.0 V | | 280 | | |
| $C_I$ | Input capacitance | Only one terminal Ax can be selected at one time from the pad to the ADC capacitor array, including wiring and pad | T | 2.2 V | | 4.5 | 5.5 | pF |
| $R_I$ | Input MUX ON resistance | $DV_{CC}$ = 2 V, 0 V ≤ $V_{Ax}$ ≤ $DV_{CC}$ | T | | | | 2 | kΩ |

(1) This specifies the ADC functional range with 8-bit resolution at 8-bit ENOB. 表 5-22 specifies 10- and 12-bit linearity parameters for better ENOB requirements.

表 5-21 lists the timing parameters of the ADC.

**表 5-21. ADC, Timing Parameters**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | DEVICE GRADE | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $f_{ADCCLK}$ | ADC clock frequency | ADC clock, 10-bit mode | T | 2.4 V to 3.6 V | | | 6.0 | MHz |
| | | ADC clock, 12-bit mode | | | | | 4.4 | |
| $t_{Settling}$ | Turn-on settling time of the ADC | The error in a conversion started after $t_{ADCON}$ is less than ±0.5 LSB, Reference and input signal already settled | T | | | | 100 | ns |
| $t_{Sample}$ | Sampling time(1) | $R_S$ = 1000 Ω, $R_I$ = 4000 Ω, $C_I$ = 5.5 pF, $C_{external}$ = 8.0 pF, Approximately 7.62 Tau (t) are required for an error of less than ±0.5 LSB, 10-bit mode(2) | T | 2.4 V to 3.6 V | 0.52 | | | µs |
| | | $R_S$ = 1000 Ω, $R_I$ = 4000 Ω, $C_I$ = 5.5 pF, $C_{external}$ = 8.0 pF, Approximately 9.01 Tau (t) are required for an error of less than ±0.5 LSB, 12-bit mode(2) | T | 2.4 V to 3.6 V | 0.61 | | | |

(1) This excludes the ADC conversion time. The ADC conversion time is specified as (N + 2) × $1/f_{ADCCLK}$.
(2) $t_{Sample} = \ln(2^{n+1}) \times \tau$, where n = ADC resolution, $\tau = (R_I + R_S) \times C_I$

表 5-22 lists the linearity parameters of the ADC.

**表 5-22. ADC, Linearity Parameters**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | DEVICE GRADE | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $E_I$ | Integral linearity error(12-bit mode) | Veref+ reference | T | 2.4 V to 3.6 V | –2.5 | | 2.5 | LSB |
| | Integral linearity error (10-bit mode) | Veref+ reference | | | –2 | | 2 | |
| $E_D$ | Differential linearity error(12-bit mode) | Veref+ reference | T | 2.4 V to 3.6 V | –1 | | 1 | LSB |
| | Differential linearity error (10-bit mode) | Veref+ reference | | | –1 | | 1 | |
| $E_O$ | Offset error(12-bit mode) | Veref+ reference | T | 2.4 V to 3.6 V | –1.5 | | 1.5 | mV |
| | Offset error (10-bit mode) | Veref+ reference | | | –6.0 | | 6.0 | |
| $E_G$ | Gain error (12-bit mode) | Veref+ as reference | T | 2.4 V to 3.6 V | –3.0 | | 3.0 | LSB |
| | Gain error (10-bit mode) | Veref+ as reference | | | –1.5 | | 1.5 | |
| $E_T$ | Total unadjusted error (12-bit mode) | Veref+ as reference | T | 2.4 V to 3.6 V | –4.0 | | 4.0 | LSB |
| | Total unadjusted error (10-bit mode) | Veref+ as reference | | | –2.0 | | 2.0 | |


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### 5.12.10 Enhanced Comparator (eCOMP)

表 5-23 lists the characteristics of eCOMP0.

**表 5-23. eCOMP0**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | DEVICE GRADE | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | T | 2.0 | | 3.6 | V |
| $V_{IC}$ | Common mode input range | | T | 0 | | $V_{CC}$ | V |
| $V_{HYS}$ | DC input hysteresis | CPEN = 1, CPHSEL= 00 | T | | 0 | | mV |
| | | CPEN = 1, CPHSEL= 01 | | | 10 | | |
| | | CPEN = 1, CPHSEL= 10 | | | 20 | | |
| | | CPEN = 1, CPHSEL= 11 | | | 30 | | |
| $V_{OFFSET}$ | Input offset voltage | CPEN = 1, CPMSEL = 0 | T | –30 | | +30 | mV |
| | | CPEN = 1, CPMSEL = 1 | | –40 | | +40 | |
| $I_{COMP}$ | Quiescent current draw from $V_{CC}$, only Comparator | $V_{IC}$ = $V_{CC}$/2, CPEN = 1, CPMSEL = 0 | T | | 24 | 35 | µA |
| | | $V_{IC}$ = $V_{CC}$/2, CPEN = 1, CPMSEL = 1 | | | 1.6 | 5 | |
| $C_{IN}$ | Input channel capacitance (1) | | T | | 1 | | pF |
| $R_{IN}$ | Input channel series resistance | On (switch closed) | T | | 10 | 20 | kΩ |
| | | Off (switch open) | | 50 | | | MΩ |
| $t_{PD}$ | Propagation delay, response time | CPMSEL = 0, CPFLT = 0, Overdrive = 20 mV | T | | | 1 | µs |
| | | CPMSEL = 1, CPFLT = 0, Overdrive = 20 mV | | | 3.2 | | |
| $t_{EN_CP}$ | Comparator enable time | CPEN = 0→1, CPMSEL = 0, V+ and V- from pads, Overdrive = 20 mV | T | | 8.5 | | µs |
| | | CPEN = 0→1, CPMSEL = 1, V+ and V- from pads, Overdrive = 20 mV | | | 1.4 | | |
| $t_{EN_CP_DAC}$ | Comparator with reference DAC enable time | CPEN = 0→1, CPDACEN = 0→1, CPMSEL = 0, CPDACREFS = 1, CPDACBUF1 = 0F, Overdrive = 20 mV | T | | 8.5 | | µs |
| | | CPEN = 0→1, CPDACEN = 0→1, CPMSEL = 1, CPDACREFS = 1, CPDACBUF1 = 0F, Overdrive = 20 mV | | | 101 | | |
| $t_{FDLY}$ | Propagation delay with analog filter active | CPMSEL = 0, CPFLTDY = 00, Overdrive = 20 mV, CPFLT = 1 | T | | 0.7 | | µs |
| | | CPMSEL = 0, CPFLTDY = 01, Overdrive = 20 mV, CPFLT = 1 | | | 1.1 | | |
| | | CPMSEL = 0, CPFLTDY = 10, Overdrive = 20 mV, CPFLT = 1 | | | 1.9 | | |
| | | CPMSEL = 0, CPFLTDY = 11, Overdrive = 20 mV, CPFLT = 1 | | | 3.4 | | |
| INL | Integral nonlinearity | | T | –0.5 | | 0.5 | LSB |
| DNL | Differential nonlinearity | | T | –0.5 | | 0.5 | LSB |

(1) For details on the eCOMP $C_{IN,}$ model , see 图 5-16.

表 5-24 lists the characteristics of eCOMP1.

**表 5-24. eCOMP1**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | DEVICE GRADE | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| VCC | Supply voltage | | T | 2.0 | | 3.6 | V |
| $V_{IC}$ | Common mode input range | | T | 0 | | $V_{CC}$ | V |
| $V_{HYS}$ | DC input hysteresis | CPEN = 1, CPHSEL= 00 | T | | 0 | | mV |
| | | CPEN = 1, CPHSEL= 01 | | | 10 | | |
| | | CPEN = 1, CPHSEL= 10 | | | 20 | | |
| | | CPEN = 1, CPHSEL= 11 | | | 30 | | |
| $V_{OFFSET}$ | Input offset voltage | CPEN = 1, CPMSEL = 0 | T | –30 | | +30 | mV |
| | | CPEN = 1, CPMSEL = 1 | | –40 | | +40 | |
| $I_{COMP}$ | Quiescent current draw from $V_{CC}$, only Comparator | $V_{IC}$ = $V_{CC}$/2, CPEN = 1, CPMSEL = 0 | T | | 162 | 209 | µA |
| | | $V_{IC}$ = $V_{CC}$/2, CPEN = 1, CPMSEL = 1 | | | 20 | 30 | |
| $C_{IN}$ | Input channel capacitance(1) | | T | | 1 | | pF |
| $R_{IN}$ | Input channel series resistance | On (switch closed) | T | | 1 | 5 | kΩ |
| | | Off (switch open) | | 50 | | | MΩ |
| $t_{PD}$ | Propagation delay, response time | CPMSEL = 0, CPFLT = 0, Overdrive = 20 mV, DVCC = 3.0 V | T | | | 0.1 | µs |
| | | CPMSEL = 1, CPFLT = 0, Overdrive = 20 mV | | | 0.32 | | |
| $t_{EN_CP}$ | Comparator enable time | CPEN = 0→1, CPMSEL = 0, V+ and V- from pads, Overdrive = 20 mV | T | | 8.5 | | µs |
| | | CPEN = 0→1, CPMSEL = 1, V+ and V- from pads, Overdrive = 20 mV | | | 4.8 | | |
| $t_{EN_CP_DAC}$ | Comparator with reference DAC enable time | CPEN = 0→1, CPDACEN = 0→1, CPMSEL = 0, CPDACREFS = 1, CPDACBUF1 = 0F, Overdrive = 20 mV | T | | 8.5 | | µs |
| | | CPEN = 0→1, CPDACEN = 0→1, CPMSEL = 1, CPDACREFS = 1, CPDACBUF1 = 0F, Overdrive = 20 mV | | | 101 | | |
| $t_{FDLY}$ | Propagation delay with analog filter active | CPMSEL = 0, CPFLTDY = 00, Overdrive = 20 mV, CPFLT = 1 | T | | 150 | | ns |
| | | CPMSEL = 0, CPFLTDY = 01, Overdrive = 20 mV, CPFLT = 1 | | | 350 | | |
| | | CPMSEL = 0, CPFLTDY = 10, Overdrive = 20 mV, CPFLT = 1 | | | 1000 | | |
| | | CPMSEL = 0, CPFLTDY = 11, Overdrive = 20 mV, CPFLT = 1 | | | 1900 | | |
| INL | Integral nonlinearity | | T | –0.5 | | 0.5 | LSB |
| DNL | Differential nonlinearity | | T | –0.5 | | 0.5 | LSB |

(1) For details on the eCOMP $C_{IN}$, model, see 图 5-16.

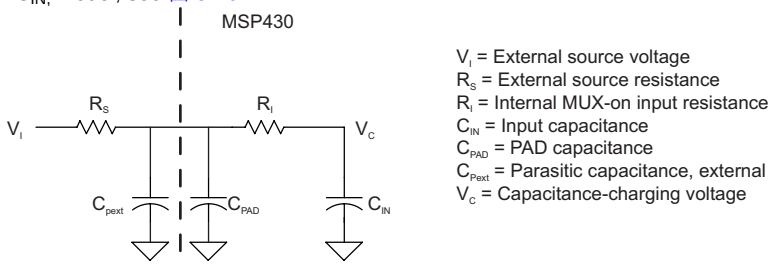



**图 5-16. eCOMP Input Circuit**


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### 5.12.11 Smart Analog Combo (SAC) (MSP430FR235x Devices Only)

表 5-25 lists the characteristics of the SAC OA.

**表 5-25. SAC, OA**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | DEVICE GRADE | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | T | 2.0 | | 3.6 | V |
| $V_{OS}$ | Input offset voltage | | T | –5 | | 5 | mV |
| $dV_{OS}/dT$ | Offset drift | OAPM = 0 (1) | T | | 3 | | µV/℃ |
| | | OAPM = 1 (1) | | | 5 | | |
| $I_B$ | Input bias current | | T | | 50 | | pA |
| $V_{CM}$ | Input voltage range | | T | –0.1 | | $V_{CC}$ + 0.1 | V |
| $I_{IDD}$ | Quiescent current | OAPM = 0 | T | | 350 | | µA |
| | | OAPM = 1 | | | 120 | | |
| $E_{NI}$ | Input noise voltage | f = 0.1 Hz to 10 Hz, Vin = $V_{CC}$/2, OAPM = 0 | T | | 40 | | µV |
| | Input noise voltage density | f = 1 kHz, Vin = $V_{CC}$/2, OAPM = 0 | | | 64 | | nV/√Hz |
| | | f = 10 kHz, Vin = $V_{CC}$/2, OAPM = 0 | | | 28 | | |
| CMRR | Common-mode rejection ratio | OAPM = 0 | T | | 70 | | dB |
| | | OAPM = 1 | | | 80 | | |
| PSRR | Power supply rejection ratio | OAPM = 0 | T | | 70 | | dB |
| | | OAPM = 1 | | | 80 | | |
| GBW | Gain-bandwidth | OAPM = 0 | T | | 2.8 | | MHz |
| | | OAPM = 1 | | | 1.0 | | |
| $A_{OL}$ | Open-loop voltage gain | OAPM = 0 | T | | 100 | | dB |
| | | OAPM = 1 | | | 100 | | |
| $\varphi_M$ | Phase margin | $C_L$ = 50 pF , $R_L$ = 2 kΩ | T | | 65 | | deg |
| | Positive slew rate | $C_L$ = 50 pF, OAPM = 0, step = 1 | T | | 3 | | V/µs |
| | | $C_L$ = 50 pF, OAPM = 1, step = 1 | | | 1 | | |
| $C_{in}$ | Input capacitance | Common mode | T | | 3 | | pF |
| $V_O$ | Voltage output swing from supply rails | $R_L$ = 10 kΩ | T | | 40 | 100 | mV |
| $t_{ST}$ | OA settling time | To 0.1% final value, G = +1, 1-V setup $C_L$ = 50 pF, OAPM = 0 | T | | 1 | | µs |
| | | To 0.1% final value, G = +1, 1-V setup $C_L$ = 50 pF, OAPM = 1 | | | 4.5 | | |
| THD | Total harmonic distortion | All gains | T | | –60 | | dB |

(1) Calculated using the box method: (MAX(–40°C to 105°C) – MIN(–40°C to 105°C)) / MIN(–40°C to 105°C) / (105°C – (–40°C))

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表 5-25. SAC, OA (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | DEVICE GRADE | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $G_{close\ loop}$ | PGA closed-loop gain | Gain = 1, inverting mode, follower mode | T | 0.99 | 1 | 1.01 | |
| | | Gain = 2, noninverting mode | T | 1.98 | 2 | 2.02 | |
| | | Gain = 2, inverting mode | T | 1.98 | 2 | 2.02 | |
| | | Gain = 3, noninverting mode | T | 2.97 | 3 | 3.03 | |
| | | Gain = 4, inverting mode | T | 3.96 | 4 | 4.04 | |
| | | Gain = 5, noninverting mode | T | 4.95 | 5 | 5.05 | |
| | | Gain = 8, inverting mode | T | 7.92 | 8 | 8.08 | |
| | | Gain = 9, noninverting mode | T | 8.91 | 9 | 9.09 | |
| | | Gain = 16, inverting mode | T | 15.84 | 16 | 16.16 | |
| | | Gain = 17, noninverting mode | T | 16.83 | 17 | 17.17 | |
| | | Gain = 25, inverting mode | T | 24.75 | 25 | 25.25 | |
| | | Gain = 26, noninverting mode | T | 25.74 | 26 | 26.26 | |
| | | Gain = 32, inverting mode | T | 31.68 | 32 | 32.32 | |
| | | Gain = 33, noninverting mode | T | 32.67 | 33 | 33.33 | |

表 5-26 lists the characteristics of the SAC DAC.

表 5-26. SAC, DAC

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | DEVICE GRADE | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | T | 2.4 | | 3.6 | V |
| $I_{IDDR}$ | Quiescent current of resistor ladder into $V_{REF_INT}$ | | | T | | 5 | | µA |
| $I_{IOAD}$ | OA + DAC output load current | Low-power mode | | T | | 0.2 | | mA |
| | | High-power mode | | | | 1 | | |
| $t_{ST(FS)}$ | OA + DAC settling time, full scale | DACDAT = 0x80h→0xF7Fh→0x80h | OAPM = 1 | T | | | 477 | µs |
| | | | OAPM = 0 | | | | 160 | |
| $t_{ST(C-C)}$ | OA + DAC settling time, code to code | DACDAT = 0x3F8h→408h→0x3F8h or DACDAT = 0xBF8h→C08h→0xBF8h | OAPM = 1 | T | | 2 | 10 | µs |
| | | | OAPM = 0 | | | 2 | 5 | |
| INL | OA + DAC integral nonlinearity | DACSREF = DVCC, DVCC = 3.0 V | | T | –4 | | 4 | LSB |
| DNL | OA + DAC differential nonlinearity | DACSREF = DVCC, DVCC = 3.0 V | | T | –1 | | 1 | LSB |
| $V_{OUT}$ | Output voltage range | No load, DACSREF = DVCC, DACDAT = 0 | | T | 0 | | 0.005 | V |
| | | $R_{LOAD}$ = 3 kΩ , DACSREF = DVCC, DACDAT = 0 | | | 0 | | 0.1 | |
| | | $R_{LOAD}$ = 3 kΩ , DACSREF = DVCC, DACDAT = 0FFFh | | | DVCC – 0.1 | | DVCC | |


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### 5.12.12 FRAM

表 5-27 lists the characteristics of the FRAM.

**表 5-27. FRAM**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | DEVICE GRADE | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | Read and write endurance | | T | $10^{15}$ | | | cycles |
| $t_{Retention}$ | Data retention duration | $T_J$ = 25°C | T | 100 | | | years |
| | | $T_J$ = 70°C | T | 40 | | | |
| | | $T_J$ = 115°C | T | 10 | | | |
| $I_{WRITE}$ | Current to write into FRAM | | T | $I_{READ}$ (1) | $I_{READ}$ (1) | $I_{READ}$ (1) | nA |
| $I_{ERASE}$ | Erase current | | T | N/A (2) | N/A (2) | N/A (2) | nA |
| $t_{WRITE}$ | Write time | | T | $t_{READ}$ (3) | $t_{READ}$ (3) | $t_{READ}$ (3) | ns |
| $T_{READ}$ | Read time | NWAITSx = 0 | T | $1/f_{SYSTEM}$ (4) | $1/f_{SYSTEM}$ (4) | $1/f_{SYSTEM}$ (4) | ns |
| | | NWAITSx = 1 | T | $2/f_{SYSTEM}$ (4) | $2/f_{SYSTEM}$ (4) | $2/f_{SYSTEM}$ (4) | |
| | | NWAITSx = 2 | T | $3/f_{SYSTEM}$ (4) | $3/f_{SYSTEM}$ (4) | $3/f_{SYSTEM}$ (4) | |

(1) Writing to FRAM does not require a setup sequence or additional power when compared to reading from FRAM. The FRAM read current $I_{READ}$ is included in the active mode current consumption $I_{AM, FRAM}$ parameters.
(2) FRAM does not require a special erase sequence.
(3) Writing into FRAM is as fast as reading.
(4) The maximum read (and write) speed is specified by $f_{SYSTEM}$ using the appropriate wait state settings (NWAITSx).

### 5.12.13 Emulation and Debug

表 5-28 lists the characteristics of the SBW interface.

**表 5-28. JTAG, Spy-Bi-Wire Interface**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 5-17)

| PARAMETER | | DEVICE GRADE | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{SBW}$ | Spy-Bi-Wire input frequency | T | 2.0 V, 3.0 V | 0 | | 8 | MHz |
| $t_{SBW,Low}$ | Spy-Bi-Wire low clock pulse duration | T | 2.0 V, 3.0 V | 0.028 | | 15 | µs |
| $t_{SU,SBWTDIO}$ | SBWTDIO setup time (before falling edge of SBWTCK in TMS and TDI slot Spy-Bi-Wire) | T | 2.0 V, 3.0 V | 4 | | | ns |
| $t_{HD,SBWTDIO}$ | SBWTDIO hold time (after rising edge of SBWTCK in TMS and TDI slot Spy-Bi-Wire) | T | 2.0 V, 3.0 V | 19 | | | ns |
| $t_{Valid,SBWTDIO}$ | SBWTDIO data valid time (after falling edge of SBWTCK in TDO slot Spy-Bi-Wire) | T | 2.0 V, 3.0 V | | | 31 | ns |
| $t_{SBW,\ En}$ | Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) (1) | T | 2.0 V, 3.0 V | | | 110 | µs |
| $t_{SBW,Ret}$ | Spy-Bi-Wire return to normal operation time (2) | T | 2.0 V, 3.0 V | 15 | | 100 | µs |
| $R_{internal}$ | Internal pulldown resistance on TEST | T | 2.0 V, 3.0 V | 20 | 35 | 50 | kΩ |

(1) Tools that access the Spy-Bi-Wire interface must wait for the $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
(2) Maximum $t_{SBW,Rst}$ time after pulling or releasing the TEST/SBWTCK pin low, the Spy-Bi-Wire pins revert from their Spy-Bi-Wire function to their application function. This time applies only if the Spy-Bi-Wire mode was selected.

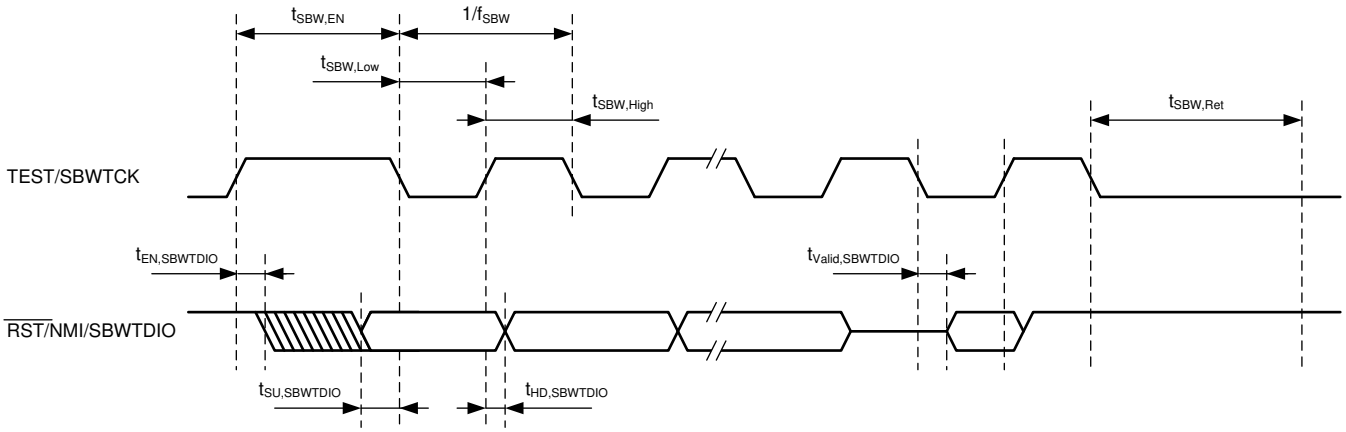



**图 5-17. JTAG Spy-Bi-Wire Timing**


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表 5-29 lists the characteristics of the 4-wire JTAG interface.

**表 5-29. JTAG, 4-Wire Interface**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 5-18)

| PARAMETER | | DEVICE GRADE | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{TCK}$ | TCK input frequency (1) | I, T | 2.0 V, 3.0 V | 0 | | 10 | MHz |
| $t_{TCK,Low}$ | Spy-Bi-Wire low clock pulse duration | I, T | 2.0 V, 3.0 V | 15 | | | ns |
| $t_{TCK,high}$ | Spy-Bi-Wire high clock pulse duration | I, T | 2.0 V, 3.0 V | 15 | | | ns |
| $t_{SU,TMS}$ | TMS setup time (before rising edge of TCK) | I, T | 2.0 V, 3.0 V | 11 | | | ns |
| $t_{HD,TMS}$ | TMS hold time (after rising edge of TCK) | I, T | 2.0 V, 3.0 V | 3 | | | ns |
| $t_{SU,TDI}$ | TDI setup time (before rising edge of TCK) | I, T | 2.0 V, 3.0 V | 13 | | | ns |
| $t_{HD,TDI}$ | TDI hold time (after rising edge of TCK) | I, T | 2.0 V, 3.0 V | 5 | | | ns |
| $t_{z\text{-}Valid,TDO}$ | TDO high impedance to valid output time (after falling edge of TCK) | I, T | 2.0 V, 3.0 V | | | 26 | ns |
| $t_{Valid,TDO}$ | TDO to new valid output time (after falling edge of TCK) | I, T | 2.0 V, 3.0 V | | | 26 | ns |
| $t_{Valid\text{-}Z,TDO}$ | TDO valid to high impedance output time (after falling edge of TCK) | I, T | 2.0 V, 3.0 V | | | 26 | ns |
| $t_{JTAG,Ret}$ | Spy-Bi-Wire return to normal operation time | I, T | 2.0 V, 3.0 V | 15 | | 100 | µs |
| $R_{internal}$ | Internal pulldown resistance on TEST | I, T | 2.0 V, 3.0 V | 20 | 35 | 50 | kΩ |

(1) Tools that access the Spy-Bi-Wire interface must wait for the $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.

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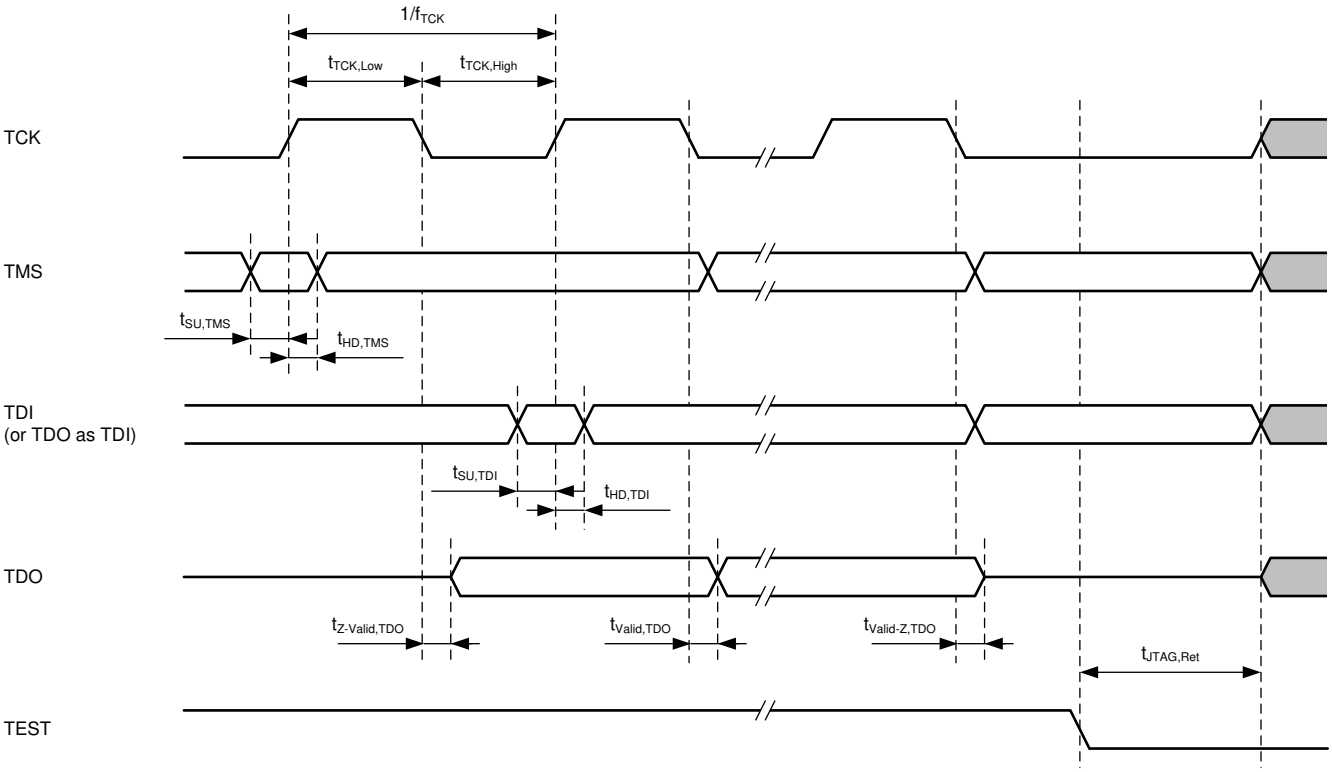



**图 5-18. JTAG 4-Wire Timing**


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# 6 Detailed Description

## 6.1 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter (PC), stack pointer (SP), status register (SR), and constant generator (CG), respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

## 6.2 Operating Modes

The MCUs have one active mode and several software-selectable low-power modes of operation. An interrupt event can wake the device from a low-power mode (LPM0, LPM3, or LPM4), service the request, and return to the low-power mode on return from the interrupt program. Low-power modes LPM3.5 and LPM4.5 disable the core supply to minimize power consumption.

**表 6-1. Operating Modes**

| MODE | | AM | LPM0 | LPM3 | LPM4 | LPM3.5 | LPM4.5 |
|---|---|---|---|---|---|---|---|
| | | ACTIVE MODE | CPU OFF | STANDBY | OFF | ONLY RTC COUNTER | SHUTDOWN |
| Maximum system clock | | 24 MHz | 24 MHz | 40 kHz | 0 | 40 kHz | 0 |
| Power consumption at 25°C, 3 V | | 142 µA/MHz | 40 µA/MHz | 1.43 µA with RTC counter only in LFXT | 0.82 µA without SVS | 620 nA with RTC counter only in LFXT | 42 nA without SVS |
| Wake-up time | | N/A | Instant | 10 µs | 10 µs | 350 µs | 350 µs |
| Wake-up events | | N/A | All | All | I/O | RTC counter, I/O | I/O |
| Power | Regulator | Full regulation | Full regulation | Partial power down | Partial power down | Partial power down | Power down |
| | SVS | On | On | Optional | Optional | Optional | Optional |
| | Brownout | On | On | On | On | On | On |
| Clock(1) | MCLK | Active | Off | Off | Off | Off | Off |
| | SMCLK | Optional | Active | Off | Off | Off | Off |
| | FLL | Optional | Optional | Off | Off | Off | Off |
| | DCO | Optional | Optional | Off | Off | Off | Off |
| | MODCLK | Optional | Optional | Off | Off | Off | Off |
| | REFO | Optional | Optional | Optional | Off | Off | Off |
| | ACLK | Optional | Optional | Active | Off | Off | Off |
| | XT1HFCLK(2) | Optional | Optional | Off | Off | Off | Off |
| | XT1LFCLK | Optional | Optional | Optional | Off | Optional | Off |
| | VLOCLK | Optional | Optional | Optional | Off | Optional | Off |
| Core | CPU | On | Off | Off | Off | Off | Off |
| | FRAM | On | On | Off | Off | Off | Off |
| | RAM | On | On | On | On | Off | Off |
| | Backup Memory(3) | On | On | On | On | On | Off |

(1) The status shown for LPM4 applies to internal clocks only.
(2) HFXT must be disabled before entering into LPM3, LPM4, or LPMx.5 mode.
(3) Backup memory contains one 32-byte register in the peripheral memory space. See 表 6-33 and 表 6-54 for its memory allocation.

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表 6-1. Operating Modes (continued)

| MODE | | AM | LPM0 | LPM3 | LPM4 | LPM3.5 | LPM4.5 |
|---|---|---|---|---|---|---|---|
| | | ACTIVE MODE | CPU OFF | STANDBY | OFF | ONLY RTC COUNTER | SHUTDOWN |
| Peripherals | Timer0_B3 | Optional | Optional | Optional | Off | Off | Off |
| | Timer1_B3 | Optional | Optional | Optional | Off | Off | Off |
| | Timer2_B3 | Optional | Optional | Optional | Off | Off | Off |
| | Timer3_B7 | Optional | Optional | Optional | Off | Off | Off |
| | WDT | Optional | Optional | Optional | Off | Off | Off |
| | eUSCI_A0 | Optional | Optional | Optional | Off | Off | Off |
| | eUSCI_A1 | Optional | Optional | Optional | Off | Off | Off |
| | eUSCI_B0 | Optional | Optional | Optional | Off | Off | Off |
| | eUSCI_B1 | Optional | Optional | Optional | Off | Off | Off |
| | CRC | Optional | Optional | Off | Off | Off | Off |
| | ICC | Optional | Optional | Off | Off | Off | Off |
| | MPY32 | Optional | Optional | Off | Off | Off | Off |
| | ADC | Optional | Optional | Optional | Off | Off | Off |
| | eCOMP0 | Optional | Optional | Optional | Optional | Off | Off |
| | eCOMP1 | Optional | Optional | Optional | Optional | Off | Off |
| | SAC0 (4) | Optional | Optional | Optional | Optional | Off | Off |
| | SAC1 (4) | Optional | Optional | Optional | Optional | Off | Off |
| | SAC2 (4) | Optional | Optional | Optional | Optional | Off | Off |
| | SAC3 (4) | Optional | Optional | Optional | Optional | Off | Off |
| | RTC Counter | Optional | Optional | Optional | Optional | Optional | Off |
| I/O | General digital input/output | On | Optional | State held | State held | State held | State held |

(4) MSP430FR235x devices only

注

XT1CLK and VLOCLK can be active during LPM4 if requested by low-frequency peripherals.


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## 6.3 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FF80h (see 表 6-2). The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

**表 6-2. Interrupt Sources, Flags, and Vectors**

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|---|---|---|---|
| **System Reset**<br>Power up, brownout, supply supervisor<br>External reset RST<br>Watchdog time-out, key violation<br>FRAM uncorrectable bit error detection<br>Software POR, BOR<br>FLL unlock error | SVSHIFG<br>PMMRSTIFG<br>WDTIFG<br>PMMPORIFG, PMMBORIFG<br>SYSRSTIV<br>FLLULPUC | Reset | FFFEh | 63, Highest |
| **System NMI**<br>Vacant memory access<br>JTAG mailbox<br>FRAM access time error<br>FRAM bit-error detection | VMAIFG<br>JMBINIFG, JMBOUTIFG<br>CBDIFG, UBDIFG | Non-Maskable | FFFCh | 62 |
| **User NMI**<br>External NMI<br>Oscillator fault | NMIIFG<br>OFIFG | Non-Maskable | FFFAh | 61 |
| Timer0_B3 | TB0CCR0 CCIFG0 | Maskable | FFF8h | 60 |
| Timer0_B3 | TB0CCR1 CCIFG1, TB0CCR2 CCIFG2, TB0IFG (TB0IV) | Maskable | FFF6h | 59 |
| Timer1_B3 | TB1CCR0 CCIFG0 | Maskable | FFF4h | 58 |
| Timer1_B3 | TB1CCR1 CCIFG1, TB1CCR2 CCIFG2, TB1IFG (TB1IV) | Maskable | FFF2h | 57 |
| Timer2_B3 | TB2CCR0 CCIFG0 | Maskable | FFF0h | 56 |
| Timer2_B3 | TB2CCR1 CCIFG1, TB2CCR2 CCIFG2, TB2IFG (TB2IV) | Maskable | FFEEh | 55 |
| Timer3_B7 | TB3CCR0 CCIFG0 | Maskable | FFECh | 54 |
| Timer3_B7 | TB3CCR1 CCIFG1, TB3CCR2 CCIFG2, TB3CCR3 CCIFG3, TB3CCR4 CCIFG4, TB3CCR5 CCIFG5, TB3CCR6 CCIFG6, TB3IFG (TB3IV) | Maskable | FFEAh | 53 |
| RTC counter | RTCIFG | Maskable | FFE8h | 52 |
| Watchdog timer interval mode | WDTIFG | Maskable | FFE6h | 51 |
| eUSCI_A0 receive or transmit | UCTXCPTIFG, UCSTTIFG, UCRXIFG, UCTXIFG (UART mode)<br>UCRXIFG, UCTXIFG (SPI mode)<br>(UCA0IV)) | Maskable | FFE4h | 50 |
| eUSCI_A1 receive or transmit | UCTXCPTIFG, UCSTTIFG, UCRXIFG, UCTXIFG (UART mode)<br>UCRXIFG, UCTXIFG (SPI mode)<br>(UCA0IV)) | Maskable | FFE2h | 49 |
| eUSCI_B0 receive or transmit | UCB0RXIFG, UCB0TXIFG (SPI mode)<br>UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG,<br>UCBIT9IFG,UCCLTOIFG($I^2C$ mode)<br>(UCB0IV) | Maskable | FFE0h | 48 |

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表 6-2. Interrupt Sources, Flags, and Vectors (continued)

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|---|---|---|---|
| eUSCI_B1 receive or transmit | UCB1RXIFG, UCB1TXIFG (SPI mode) UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG,UCCLTOIFG($I^2C$ mode) (UCB0IV) | Maskable | FFDEh | 47 |
| ADC | ADCIFG0, ADCINIFG, ADCLOIFG, ADCHIIFG, ADCTOVIFG, ADCOVIFG (ADCIV) | Maskable | FFDCh | 46 |
| eCOMP0_eCOMP1 | CPIIFG, CPIFG (CP1IV, CP0IV) | Maskable | FFDAh | 45 |
| SAC0_SAC2(1) | SAC2DACSTS DACIFG (SAC2IV) SAC0DACSTS DACIFG, SAC0IV) | Maskable | FFD8h | 44 |
| SAC1_SAC3(1) | SAC3DACSTS DACIFG (SAC3IV) SAC1DACSTS DACIFG, SAC1IV) | Maskable | FFD6h | 43 |
| P1 | P1IFG.0 to P1IFG.7 (P1IV) | Maskable | FFD4h | 42 |
| P2 | P2IFG.0 to P2IFG.7 (P2IV) | Maskable | FFD2h | 41 |
| P3 | P3IFG.0 to P3IFG.7 (P3IV) | Maskable | FFD0h | 40 |
| P4 | P4IFG.0 to P4IFG.7 (P4IV) | Maskable | FFCEh | 39 |
| Reserved | Reserved | Maskable | FFCCh to FF88h | |

(1) MSP430FR235x devices only

表 6-3 lists the BSL signature settings. The BSL setting on MSP430FR2355 can be customized by using BSL configuration and $I^2C$ address. See the *MSP430 FRAM Device Bootloader (BSL) User's Guide* for more details.

表 6-3. BSL Signatures

| SIGNATURE | WORD ADDRESS |
|---|---|
| BSL I2C Address(1) | FFA0h |
| BSL Config | 0FF8Ah |
| BSL Config Signature | 0FF88h |
| BSL Signature2 | 0FF86h |
| BSL Signature1 | 0FF84h |
| JTAG Signature2 | 0FF82h |
| JTAG Signature1 | 0FF80h |

(1) 7-bit address BSL $I^2C$ interface


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## 6.4 Memory Organization

表 6-4 summarizes the memory map of the devices.

**表 6-4. Memory Organization**

| | ACCESS | MSP430FR2355 | MSP430FR2353 |
|---|---|---|---|
| Memory (FRAM)<br>Main: interrupt vectors and signatures<br>Main: code memory | Read/Write<br>(Optional Write Protect)(1) | 32KB<br>FFFFh to FF80h<br>FFFFh to 8000h | 16KB<br>FFFFh to FF80h<br>FFFFh to C000h |
| RAM | Read/Write | 4KB<br>2FFFh to 2000h | 2KB<br>27FFh to 2000h |
| Information memory (FRAM) | Read/Write(2) | 512 bytes<br>19FFh to 1800h | 512 bytes<br>19FFh to 1800h |
| Driver library and FFT library (ROM) | Read only | 20KB<br>FAC00h to FFBFFh | 20KB<br>FAC00h to FFBFFh |
| Peripherals | Read/Write | 4KB<br>0FFFh to 0020h | 4KB<br>0FFFh to 0020h |
| Tiny RAM | Read/Write | 26 bytes<br>001Fh to 0006h | 26 bytes<br>001Fh to 0006h |
| Reserved(3) | Read | 6 bytes<br>0005h to 0000h | 6 bytes<br>0005h to 0000h |

(1) The program FRAM can be write protected by setting PFWP bit in SYSCFG0 register. See the SYS chapter in *MSP430FR4xx and MSP430FR2xx Family User's Guide* for more details.
(2) The information FRAM can be write protected by setting DFWP bit in SYSCFG0 register. See the SYS chapter in *MSP430FR4xx and MSP430FR2xx Family User's Guide* for more details.
(3) Reads as D032h at 00h (opcode: BIS.W LPM4, SR), reads as 00F0h at 02h (opcode: BIS.W LPM4, SR), and reads as 3FFFh at 04h (opcode: JMP$)

## 6.5 Bootloader (BSL)

The BSL enables users to program the FRAM memory or RAM using a UART or $I^2C$ serial interface. Access to the device memory through the BSL is protected by an user-defined password. Use of the BSL requires four pins (see 表 6-5 and 表 6-6). BSL entry requires a specific entry sequence on the $\overline{\text{RST}}$/NMI/SBWTDIO and TEST/SBWTCK pins. For complete description of the features of the BSL and its implementation, see *MSP430 FRAM Devices Bootloader (BSL) User's Guide*.

**表 6-5. UART BSL Pin Requirements and Functions**

| DEVICE SIGNAL | BSL FUNCTION |
|---|---|
| $\overline{\text{RST}}$/NMI/SBWTDIO | Entry sequence signal |
| TEST/SBWTCK | Entry sequence signal |
| P1.7 | Data transmit |
| P1.6 | Data receive |
| DVCC | Power supply |
| DVSS | Ground supply |

**表 6-6. $I^2C$ BSL Pin Requirements and Functions**

| DEVICE SIGNAL | BSL FUNCTION |
|---|---|
| $\overline{\text{RST}}$/NMI/SBWTDIO | Entry sequence signal |
| TEST/SBWTCK | Entry sequence signal |
| P1.2 | Data receive and transmit |
| P1.3 | Clock |
| DVCC | Power supply |
| DVSS | Ground supply |

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## 6.6 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RST}}$/NMI/SBWTDIO is required to interface with MSP430 development tools and device programmers. 表 6-7 lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*.

**表 6-7. JTAG Pin Requirements and Function**

| DEVICE SIGNAL | DIRECTION | JTAG FUNCTION |
|---|---|---|
| P1.4/UCA0STE/TCK/A4 | IN | JTAG clock input |
| P1.5/UCA0CLK/TMS/OA1O/A5 | IN | JTAG state control |
| P1.6/UCA0RXD/UCA0SOMI/TB0.1/TDI/TCLK/OA1-/A6 | IN | JTAG data input, TCLK input |
| P1.7/UCA0TXD/UCA0SIMO/TB0.2/TDO/OA1+/A7/VREF+ | OUT | JTAG data output |
| TEST/SBWTCK | IN | Enable JTAG pins |
| RST/NMI/SBWTDIO | IN | External reset |
| DVCC | – | Power supply |
| DVSS | – | Ground supply |

## 6.7 Spy-Bi-Wire Interface (SBW)

The MSP430 family supports the two wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. 表 6-8 shows the Spy-Bi-Wire interface pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*.

**表 6-8. Spy-Bi-Wire Pin Requirements and Functions**

| DEVICE SIGNAL | DIRECTION | SBW FUNCTION |
|---|---|---|
| TEST/SBWTCK | IN | Spy-Bi-Wire clock input |
| RST/NMI/SBWTDIO | IN, OUT | Spy-Bi-Wire data input and output |
| DVCC | – | Power supply |
| DVSS | – | Ground supply |

## 6.8 FRAM

The FRAM can be programmed using the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. Features of the FRAM include:

- Byte and word access capability
- Programmable wait state generation
- Error correction coding (ECC)


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## 6.9 Memory Protection

The device features memory protection of user access authority and write protection include:

- Securing the whole memory map to prevent unauthorized access from JTAG port or BSL, by writing JTAG and BSL signatures using the JTAG port, SBW, the BSL, or in-system by the CPU.
- Write protection enabled to prevent unwanted write operation to FRAM contents by setting the control bits with accordingly password in System Configuration register 0. For more detailed information, see the SYS chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

## 6.10 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. All peripherals can be handled by using all instructions in the memory map. For complete module description, see the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

### 6.10.1 Power Management Module (PMM) and On-Chip Reference Voltages

The PMM includes an integrated voltage regulator that supplies the core voltage to the device. The PMM also includes supply voltage supervisor (SVS) and brownout protection. The brownout reset circuit (BOR) is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS circuitry detects if the supply voltage drops below a user-selectable safe level. SVS circuitry is available on the primary supply.

The device contains three on-chip references:

- Internal shared reference (1.5 V, 2.0 V, or 2.5 V)
- 1.2 V for external reference (VREF pin)
- 1.2 V low-power reference for eCOMP

The internal shared reference is controlled by PMM settings to select 1.5 V, 2.0 V, or 2.5 V. This reference is internally connected to ADC channel 13. DVCC is internally connected to ADC channel 15. When DVCC is set as the reference voltage for ADC conversion, the DVCC can be easily represent as 公式 1 by using ADC sampling reference without any external components support.

DVCC = (4095 × reference voltage) ÷ ADC result (1)

The internal shared reference (1.5 V, 2.0 V, or 2.5 V ) is also internally connected to the built-in DAC of the comparator and SAC (MSP430FR235x devices only) built-in 12-bit DAC as the reference voltage. The source can be selected by setting the specific register configuration of each module For more information, see the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

P1.7/UCA0TXD/UCA0SIMO/TB0.2/TDO/OA1+/A7/VREF+ can support a buffered external 1.2-V output when EXTREFEN = 1 in the PMMCTL2 register. ADC channel 7 can also be selected to monitor this voltage. For more information, see the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

An additional low-power 1.2-V reference is internally connected to eCOMP0 and eCOMP1. This reference is activated by enabling eCOMP with the channel as threshold source. See 节 6.10.13 for more details.

### 6.10.2 Clock System (CS) and Clock Distribution

The clock system includes a 32-kHz low-frequency or up to 24-MHz high-frequency crystal oscillator (XT1), an internal very low-power low-frequency oscillator (VLO), an integrated 32-kHz RC oscillator (REFO), an integrated internal digitally controlled oscillator (DCO) that can use frequency-locked loop (FLL) locking with internal or external 32-kHz reference clock, and on-chip asynchronous high-speed clock (MODOSC). The clock system is designed to target cost-effective designs with minimal external components. A fail-safe mechanism is designed for XT1. The clock system module supports the following clock signals.

- Main Clock (MCLK): the system clock used by the CPU and all relevant peripherals accessed by the bus. All clock sources except MODOSC can be selected as the source with a predivider of 1, 2, 4, 8, 16, 32, 64, or 128.

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- Sub-Main Clock (SMCLK): the subsystem clock used by the peripheral modules. SMCLK derives from the MCLK with a predivider of 1, 2, 4, or 8. This means SMCLK is always equal to or less than MCLK.
- Auxiliary Clock (ACLK): this clock derived from the external XT1 clock, internal VLO, or internal REFO clock up to 40 kHz.

All peripherals have one or several clock sources, depending on specific functionality. 表 6-9 lists the clock distribution used in this device.

**表 6-9. Clock Distribution**

| | CLOCK SOURCE SELECT BITS | MCLK | SMCLK | ACLK | MODCLK | VLOCLK | EXTERNAL PIN |
|---|---|---|---|---|---|---|---|
| Frequency Range | | DC to 24 MHz | DC to 24 MHz | DC to 40 kHz | 3.8 MHz ±21% | 10 kHz ±50% | – |
| CPU | N/A | Default | – | – | – | – | – |
| FRAM | N/A | Default | – | – | – | – | – |
| RAM | N/A | Default | – | – | – | – | – |
| CRC | N/A | Default | – | – | – | – | – |
| MPY32 | N/A | Default | – | – | – | – | – |
| ICC | N/A | Default | – | – | – | – | – |
| I/O | N/A | Default | – | – | – | – | – |
| TB0 | TBSSEL | – | 10b | 01b | – | – | 00b (TB0CLK pin) |
| TB1 | TBSSEL | – | 10b | 01b | – | – | 00b (TB1CLK pin) |
| TB2 | TBSSEL | – | 10b | 01b | – | – | 00b (TB2CLK pin) |
| TB3 | TBSSEL | – | 10b | 01b | – | – | 00b (TB3CLK pin) |
| eUSCI_A0 | UCSSEL | – | 10b or 11b | 01b | – | – | 00b (UCA0CLK pin) |
| eUSCI_A1 | UCSSEL | – | 10b or 11b | 01b | – | – | 00b (UCA1CLK pin) |
| eUSCI_B0 | UCSSEL | – | 10b or 11b | 01b | – | – | 00b (UCB0CLK pin) |
| eUSCI_B1 | UCSSEL | – | 10b or 11b | 01b | – | – | 00b (UCB1CLK pin) |
| MFM | N/A | – | Default | – | – | – | – |
| WDT | WDTSSEL | – | 00b | 01b | – | 10b | – |
| ADC | ADCSSEL | – | 10b or 11b | 01b | 00b | – | – |
| RTC Counter | RTCSS | – | 01b(1) | 01b(1) | – | 11b | – |

(1) Controlled by the RTCCKSEL bit in the SYSCFG2 register.

**表 6-10. XTCLK Distribution**

| OPERATION MODE | CLOCK SOURCE SELECT BITS | XTHFCLK AM to LPM0 | XTLFCLK AM to LPM3 | XTLFCLK (LPMx.5) AM to LPM3.5 |
|---|---|---|---|---|
| MCLK | SELMS | 10b | 10b | 10b |
| SMCLK | SELMS | 10b | 10b | 10b |
| REFO | SELREF | 0b | 0b | 0b |
| ACLK | SELA | 0b | 0b | 0b |
| RTC | RTCSS | – | 10b | 10b |


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### 6.10.3 General-Purpose Input/Output Port (I/O)

Up to 44 I/O ports are implemented.

- P1, P2, P3, and P4 are full 8-bit ports; P5 and P6 feature up to 5-bit and 7-bit ports, respectively.
- All individual I/O bits are independently programmable.
- Any combination of input, output, is possible for P1, P2, P3, P4, P5, and P6. Interrupt conditions are possible in P1, P2, P3, and P4.
- Programmable pullup or pulldown on all ports.
- Edge-selectable interrupt and LPM3.5, LPM4 and LPM4.5 wake-up input capability is available in P1, P2, P3, and P4.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise or word-wise in pairs.

注

**Configuration of digital I/Os after BOR reset**

To prevent cross currents during start-up of the device, all port pins are high-impedance with Schmitt triggers and module functions disabled. To enable the I/O functions after a BOR reset, first configure the ports and then clear the LOCKLPM5 bit. For details, see the *Configuration After Reset* section in the *Digital I/O* chapter of the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

### 6.10.4 Watchdog Timer (WDT)

The primary function of the WDT module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as interval timer and can generate interrupts at selected time intervals.

表 6-11 lists the clock sources that can be used by the WDT.

**表 6-11. WDT Clocks**

| WDTSSEL | NORMAL OPERATION (WATCHDOG AND INTERVAL TIMER MODE) |
|---|---|
| 00 | SMCLK |
| 01 | ACLK |
| 10 | VLOCLK |
| 11 | Reserved |

### 6.10.5 System Module (SYS)

The SYS module handles many of the system functions within the device. These include power-on reset (POR) and power-up clear (PUC) handling, NMI source selection and management, reset interrupt vector generators (see 表 6-12), bootloader entry mechanisms, and configuration management (device descriptors). SYS also includes a data exchange mechanism through SBW called a JTAG mailbox that can be used in the application.

表 6-12. System Module Interrupt Vector Registers

| INTERRUPT VECTOR REGISTER | ADDRESS | INTERRUPT EVENT | VALUE | PRIORITY |
|---|---|---|---|---|
| SYSRSTIV, System Reset | 015Eh | No interrupt pending | 00h | |
| | | Brownout (BOR) | 02h | Highest |
| | | RSTIFG $\overline{RST}$/NMI (BOR) | 04h | |
| | | PMMSWBOR software BOR (BOR) | 06h | |
| | | LPMx.5 wake up (BOR) | 08h | |
| | | Security violation (BOR) | 0Ah | |
| | | Reserved | 0Ch | |
| | | SVSHIFG SVSH event (BOR) | 0Eh | |
| | | Reserved | 10h | |
| | | Reserved | 12h | |
| | | PMMSWPOR software POR (POR) | 14h | |
| | | WDTIFG watchdog time-out (PUC) | 16h | |
| | | WDTPW password violation (PUC) | 18h | |
| | | FRCTLPW password violation (PUC) | 1Ah | |
| | | Uncorrectable FRAM bit error detection | 1Ch | |
| | | Peripheral area fetch (PUC) | 1Eh | |
| | | PMMPW PMM password violation (PUC) | 20h | |
| | | Reserved | 22h | |
| | | FLL unlock (PUC) | 24h | |
| | | Reserved | 26h to 3Eh | Lowest |
| SYSSNIV, System NMI | 015Ch | No interrupt pending | 00h | |
| | | SVS low-power reset entry | 02h | Highest |
| | | Uncorrectable FRAM bit error detection | 04h | |
| | | Reserved | 06h | |
| | | Reserved | 08h | |
| | | Reserved | 0Ah | |
| | | Reserved | 0Ch | |
| | | Reserved | 0Eh | |
| | | Reserved | 10h | |
| | | VMAIFG Vacant memory access | 12h | |
| | | JMBINIFG JTAG mailbox input | 14h | |
| | | JMBOUTIFG JTAG mailbox output | 16h | |
| | | Correctable FRAM bit error detection | 18h | |
| | | Reserved | 1Ah to 1Eh | Lowest |
| SYSUNIV, User NMI | 015Ah | No interrupt pending | 00h | |
| | | NMIIFG NMI pin or $SVS_H$ event | 02h | Highest |
| | | OFIFG oscillator fault | 04h | |
| | | Reserved | 06h to 1Eh | Lowest |

### 6.10.6 Cyclic Redundancy Check (CRC)

The 16-bit cyclic redundancy check (CRC) module produces a signature based on a sequence of data values and can be used for data checking purposes. The CRC generation polynomial is compliant with CRC-16-CCITT standard of $x^{16} + x^{12} + x^5 + 1$.


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### 6.10.7 Interrupt Compare Controller (ICC)

The Interrupt Compare Controller (ICC) allows all maskable interrupt sources to be scheduled in a preemptive mechanism. Each interrupt source is specified as a source of ICC module. Each source supports a 4-level software interrupt priority other than the one tired with interrupt vector. When ICC module is enabled, the ISR in lower software priority can be interrupted by higher priority. It is required to enable GIE in ISR for proper ICC operation. For details, see the ICC chapter of the *MSP430FR4xx and MSP430FR2xx Family User's Guide*. 表 6-13 lists the ICC source configurations.

**表 6-13. ICC Interrupt Source Assignments**

| REGISTER | BITS | INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|---|---|---|---|---|---|
| ICCILRS0 | ILSR0 | P4 | P4IFG.0 to P4IFG.7 (P4IV) | Maskable | FFCEh | 39 |
| | ILSR1 | P3 | P3IFG.0 to P3IFG.7 (P3IV) | Maskable | FFD0h | 40 |
| | ILSR2 | P2 | P2IFG.0 to P2IFG.7 (P2IV) | Maskable | FFD2h | 41 |
| | ILSR3 | P1 | P1IFG.0 to P1IFG.7 (P1IV) | Maskable | FFD4h | 42 |
| | ILSR4 | SAC3 DAC, SAC1 DAC(1) | DACIFG, (SAC3IV, SAC1IV)(1) | Maskable | FFD6h | 43 |
| | ILSR5 | SAC2 DAC, SAC0 DAC(1) | DACIFG (SAC2IV, SAC0IV)(1) | Maskable | FFD8h | 44 |
| | ILSR6 | eCOMP1, eCOMP0 | CPIIFG, CPIFG (CP1IV, CP0IV) | Maskable | FFDAh | 45 |
| | ILSR7 | ADC | ADCIFG0, ADCINIFG, ADCLOIFG, ADCHIIFG, ADCTOVIFG, ADCOVIFG (ADCIV) | Maskable | FFDCh | 46 |
| ICCILRS1 | ILSR8 | eUSCI_B1 Receive or Transmit | UCB1RXIFG, UCB1TXIFG (SPI mode) UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG,UCCLTOIFG($I^2C$ mode) (UCB0IV) | Maskable | FFDEh | 47 |
| | ILSR9 | eUSCI_B0 Receive or Transmit | UCB0RXIFG, UCB0TXIFG (SPI mode) UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG,UCCLTOIFG($I^2C$ mode) (UCB0IV) | Maskable | FFE0h | 48 |
| | ILSR10 | eUSCI_A1 Receive or Transmit | UCTXCPTIFG, UCSTTIFG, UCRXIFG, UCTXIFG (UART mode) UCRXIFG, UCTXIFG (SPI mode) (UCA0IV)) | Maskable | FFE2h | 49 |
| | ILSR11 | eUSCI_A0 Receive or Transmit | UCTXCPTIFG, UCSTTIFG, UCRXIFG, UCTXIFG (UART mode) UCRXIFG, UCTXIFG (SPI mode) (UCA0IV)) | Maskable | FFE4h | 50 |
| | ILSR12 | Watchdog Timer Interval mode | WDTIFG | Maskable | FFE6h | 51 |
| | ILSR13 | RTC Counter | RTCIFG | Maskable | FFE8h | 52 |
| | ILSR14 | Timer3_B7 | TB3CCR1 CCIFG1, TB3CCR2 CCIFG2, TB3CCR3 CCIFG3, TB3CCR4 CCIFG4, TB3CCR5 CCIFG5, TB3CCR6 CCIFG6, TB3IFG (TB3IV) | Maskable | FFEAh | 53 |
| | ILSR15 | Timer3_B7 | TB3CCR0 CCIFG0 | Maskable | FFECh | 54 |

(1) MSP430FR235x devices only

表 6-13. ICC Interrupt Source Assignments (continued)

| REGISTER | BITS | INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|---|---|---|---|---|---|
| ICCILRS2 | ILSR16 | Timer2_B3 | TB2CCR1 CCIFG1, TB2CCR2 CCIFG2, TB2IFG (TB2IV) | Maskable | FFEEh | 55 |
| | ILSR17 | Timer2_B3 | TB2CCR0 CCIFG0 | Maskable | FFF0h | 56 |
| | ILSR18 | Timer1_B3 | TB1CCR1 CCIFG1, TB1CCR2 CCIFG2, TB1IFG (TB1IV) | Maskable | FFF2h | 57 |
| | ILSR19 | Timer1_B3 | TB1CCR0 CCIFG0 | Maskable | FFF4h | 58 |
| | ILSR20 | Timer0_B3 | TB0CCR1 CCIFG1, TB0CCR2 CCIFG2, TB0IFG (TB0IV) | Maskable | FFF6h | 59 |
| | ILSR21 | Timer0_B3 | TB0CCR0 CCIFG0 | Maskable | FFF8h | 60 |
| | ILSR22 | N/A | N/A | N/A | N/A | N/A |
| | ILSR23 | N/A | N/A | N/A | N/A | N/A |
| ICCILRS3 | ILSR24 | N/A | N/A | N/A | N/A | N/A |
| | ILSR25 | N/A | N/A | N/A | N/A | N/A |
| | ILSR26 | N/A | N/A | N/A | N/A | N/A |
| | ILSR27 | N/A | N/A | N/A | N/A | N/A |
| | ILSR28 | N/A | N/A | N/A | N/A | N/A |
| | ILSR29 | N/A | N/A | N/A | N/A | N/A |
| | ILSR30 | N/A | N/A | N/A | N/A | N/A |
| | ILSR31 | N/A | N/A | N/A | N/A | N/A |

### 6.10.8 Enhanced Universal Serial Communication Interface (eUSCI_A0, eUSCI_A1, eUSCI_B0, eUSCI_B1)

The eUSCI modules are used for serial data communications (see 表 6-14). The eUSCI_A module supports either UART or SPI communications. The eUSCI_B module supports either SPI or $I^2C$ communications. Additionally, eUSCI_A supports automatic baud-rate detection and IrDA..

表 6-14. eUSCI Pin Configurations

| | PIN | UART | SPI |
|---|---|---|---|
| eUSCI_A0 | P1.7 | TXD | SIMO |
| | P1.6 | RXD | SOMI |
| | P1.5 | – | SCLK |
| | P1.4 | – | STE |
| eUSCI_A1 | **PIN** | **UART** | **SPI** |
| | P4.3 | TXD or $\overline{\text{TXD}}$ | SIMO |
| | P4.2 | RXD or $\overline{\text{RXD}}$ | SOMI |
| | P4.1 | – | SCLK |
| | P4.0 | – | STE |
| eUSCI_B0 | **PIN** | **$I^2C$** | **SPI** |
| | P1.3 | SCL | SOMI |
| | P1.2 | SDA | SIMO |
| | P1.1 | – | SCLK |
| | P1.0 | – | STE |
| eUSCI_B1 | **PIN** | **$I^2C$** | **SPI** |
| | P4.7 | SCL | SOMI |
| | P4.6 | SDA | SIMO |
| | P4.5 | – | SCLK |
| | P4.4 | – | STE |


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The eUSCI_A1 can work as UART in inverting polarity mode by port settings (see 表 6-15). When PSEL = 01b, the normal UART or SPI mode is used. When PSEL = 10b, the inverted UART mode is enabled to transmit and receive data in inverted polarity. In this mode, eUSCI_A1 can also wake up the device from LPM3 by detecting a rising edge of start bit according the falling edge in normal mode.

表 **6-15. eUSCI_A1 UART Polarity Configurations**

| eUSCI_A1 | PSEL = 01b | PSEL = 10b |
|---|---|---|
| P4.3 | TXD | $\overline{\text{TXD}}$ |
| P4.4 | RXD | $\overline{\text{RXD}}$ |

### *6.10.9 Timers (Timer0_B3, Timer1_B3, Timer2_B3, Timer3_B7)*

The Timer0_B3, Timer1_B3, and Timer2_B3 modules are 16-bit timers and counters with three capture/compare registers each. Timer3_B7 is a 16-bit timers with seven capture/compare registers each. Each can support multiple captures or compares, PWM outputs, and interval timing (see 表 6-16, 表 6-17, 表 6-18, and 表 6-19). Each has extensive interrupt capabilities. Interrupts can be generated from the counter on overflow conditions and from each of the capture/compare registers. The CCR0 registers on all timers are not externally connected and can only be used for hardware period timing and interrupt generation. In Up Mode, they can be used to set the overflow value of the counter.

表 **6-16. Timer0_B3 Signal Connections**

| PORT PIN | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---|---|---|---|---|---|
| P2.7 | TB0CLK | TBCLK | Timer | N/A | |
| | ACLK (internal) | ACLK | | | |
| | SMCLK (internal) | SMCLK | | | |
| | N/A | INCLK | | | |
| | From RTC (internal) | CCI0A | CCR0 | TB0 | Not used |
| | ACLK (internal) | CCI0B | | | Timer1_B3 CCI0B input |
| | DVSS | GND | | | |
| | DVCC | $V_{CC}$ | | | |
| P1.6 | TB0.1 | CCI1A | CCR1 | TB1 | TB0.1 |
| | From eCOMP0.O (internal) | CCI1B | | | Timer1_B3 CCI1B input |
| | DVSS | GND | | | |
| | DVCC | $V_{CC}$ | | | |
| P1.7 | TB0.2 | CCI2A | CCR2 | TB2 | TB0.2 |
| | N/A | CCI2B | | | Timer1_B3 INCLK<br>Timer1_B3 CCI2B input,<br>IR carrier input |
| | DVSS | GND | | | |
| | DVCC | $V_{CC}$ | | | |

表 6-17. Timer1_B3 Signal Connections

| PORT PIN | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---|---|---|---|---|---|
| P2.2 | TB1CLK | TBCLK | Timer | N/A | |
| | ACLK (internal) | ACLK | | | |
| | SMCLK (internal) | SMCLK | | | |
| | Timer0_B3 CCR2B output (internal) | INCLK | | | |
| | Timer3_B7 CCR0B output (internal) | CCI0A | CCR0 | TB0 | Not used |
| | Timer0_B3 CCR0B output (internal) | CCI0B | | | Not used |
| | DVSS | GND | | | |
| | DVCC | $V_{CC}$ | | | |
| P2.0 | TB1.1 | CCI1A | CCR1 | TB1 | TB1.1 |
| | Timer0_B3 CCR1B output (internal) | CCI1B | | | To ADC trigger |
| | DVSS | GND | | | |
| | DVCC | $V_{CC}$ | | | |
| P2.1 | TB1.2 | CCI2A | CCR2 | TB2 | TB1.2 |
| | Timer0_B3 CCR2B output (internal) | CCI2B | | | IR coding input |
| | DVSS | GND | | | |
| | DVCC | $V_{CC}$ | | | |

表 6-18. Timer2_B3 Signal Connections

| PORT PIN | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---|---|---|---|---|---|
| P2.7 | TB2CLK | TBCLK | Timer | N/A | |
| | ACLK (internal) | ACLK | | | |
| | SMCLK (internal) | SMCLK | | | |
| | $\overline{\text{TB2CLK}}$ | INCLK | | | |
| | Not used | CCI0A | CCR0 | TB0 | Not used |
| | DVSS | GND | | | |
| | DVCC | $V_{CC}$ | | | |
| | MFM Complete Event | CCI0B | | | MFM start trigger |
| P5.0 | TB2.1 | CCI1A | CCR1 | TB1 | TB2.1 |
| | From eCOMP1.O (internal) | CCI1B | | | To SAC DAC update trigger 10b(1) |
| | DVSS | GND | | | |
| | DVCC | $V_{CC}$ | | | |
| P5.1 | TB2.2 | CCI2A | CCR2 | TB2 | TB2.2 |
| | Not used | CCI2B | | | To SAC DAC update trigger 11b(1) |
| | DVSS | GND | | | |
| | DVCC | $V_{CC}$ | | | |

(1) MSP430FR235x devices only


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表 **6-19. Timer3_B7 Signal Connections**

| PORT PIN | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---|---|---|---|---|---|
| P6.6 | TB3CLK | TBCLK | Timer | N/A | |
| | ACLK (internal) | ACLK | | | |
| | SMCLK (internal) | SMCLK | | | |
| | $\overline{\text{TB3CLK}}$ | INCLK | | | |
| | Not used | CCI0A | CCR0 | TB0 | Not used |
| | Not used | CCI0B | | | To Timer1_B3 CCI0A |
| | DVSS | GND | | | |
| | DVCC | $V_{CC}$ | | | |
| P6.0 | TB3.1 | CCI1A | CCR1 | TB1 | TB3.1 |
| | Not used | CCI1B | | | |
| | DVSS | GND | | | |
| | DVCC | $V_{CC}$ | | | |
| P6.1 | TB3.2 | CCI2A | CCR2 | TB2 | TB3.2 |
| P4.0 | ISORXD | CCI2B | | | AND UCA1TXD ISOTXD |
| | DVSS | GND | | | |
| | DVCC | $V_{CC}$ | | | |
| P6.2 | TB3.3 | CCI3A | CCR3 | TB3 | TB3.3 |
| | Not used | CCI3B | | | |
| | DVSS | GND | | | |
| | DVCC | $V_{CC}$ | | | |
| P6.3 | TB3.4 | CCI4A | CCR4 | TB4 | TB3.4 |
| | Not used | CCI4B | | | Not used |
| | DVSS | GND | | | |
| | DVCC | $V_{CC}$ | | | |
| P6.4 | TB3.5 | CCI5A | CCR5 | TB5 | TB3.5 |
| | Not used | CCI5B | | | Not used |
| | DVSS | GND | | | |
| | DVCC | $V_{CC}$ | | | |
| P6.5 | TB3.6 | CCI6A | CCR6 | TB6 | TB3.6 |
| | Not used | CCI6B | | | Not used |
| | DVSS | GND | | | |
| | DVCC | $V_{CC}$ | | | |

The interconnection of Timer0_B3 and Timer1_B3 can be used to modulate the eUSCI_A pin of UCA0TXD/UCA0SIMO in either ASK or FSK mode, with which a user can easily acquire a modulated infrared command for directly driving an external IR diode. The IR functions are fully controlled by SYS configuration registers 1 including IREN (enable), IRPSEL (polarity select), IRMSEL (mode select), IRDSSEL (data select), and IRDATA (data) bits. For more information, see the SYS chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

The Timer_B module feature the function to put Timer_B all outputs into a high impedance state when the selected source is triggered. The source can be selected from external pin or internal of the device, it is controlled by TBxTRG in SYS. For more information, see the SYS chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

The Timer2_B3 CCR0 is tied with the Manchester function module (MFM).

表 6-20 lists the Timer_B high-impedance trigger sources.

**表 6-20. TBxOUTH**

| TBxTRGSEL | TBxOUTH TRIGGER SOURCE SELECTION | TIMER_B PAD OUTPUT HIGH IMPEDANCE |
|---|---|---|
| TB0TRGSEL = 0 | eCOMP0 output (internal) | P1.6, P1.7 |
| TB0TRGSEL= 1 | P1.2 | |
| TB1TRGSEL = 0 | eCOMP0 output (internal) | P2.0, P2.1 |
| TB1TRGSEL = 1 | P2.3 | |
| TB2TRGSEL = 0 | eCOMP1 output (internal) | P5.0, P5.1 |
| TB2TRGSEL = 1 | P5.3 | |
| TB3TRGSEL = 0 | eCOMP1 output (internal) | P6.0, P6.1, P6.2, P6.3, P6.4, P6.5 |
| TB3TRGSEL = 1 | N/A | |

### 6.10.10 Backup Memory (BKMEM)

The BKMEM supports data retention functionality during LPM3.5 mode. This device provides up to 32 bytes that are retained during LPM3.5.

### 6.10.11 Real-Time Clock (RTC) Counter

The RTC counter is a 16-bit modulo counter that is functional in AM, LPM0, LPM3, LPM4, and LPM3.5. This module can periodically wake up the CPU from LPM0, LPM3, LPM4, and LPM3.5 based on timing from a low-power clock source such as the XT1, ACLK, and VLO clocks. In AM, RTC can be driven by SMCLK to generate high-frequency timing events and interrupts. ACLK and SMCLK both can source to the RTC; however, only one of them can be selected at a time. The RTC overflow events can trigger:

- Timer0_B3 CCI0A
- ADC conversion trigger when ADCSHSx bits are set as 01b


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### 6.10.12 12-Bit Analog-to-Digital Converter (ADC)

The 12-bit ADC module supports fast 12-bit analog-to-digital conversions with single-ended input. The module implements a 12-bit SAR core, sample select control, reference generator and a conversion result buffer. A window comparator with a lower and upper limits allows CPU-independent result monitoring with three window comparator interrupt flags.

The ADC supports 12 external inputs and four internal inputs (see 表 6-21).

表 6-21. ADC Channel Connections

| ADCINCHx | ADC CHANNELS | EXTERNAL PIN OUTPUT |
|---|---|---|
| 0 | A0/Veref+ | P1.0 |
| 1 | A1/ | P1.1 |
| 2 | A2/Veref- | P1.2 |
| 3 | A3 | P1.3 |
| 4 | A4 | P1.4 |
| 5 | A5 | P1.5 |
| 6 | A6 | P1.6 |
| 7 | A7(1) | P1.7 |
| 8 | A8 | P5.0 |
| 9 | A9 | P5.1 |
| 10 | A10 | P5.2 |
| 11 | A11 | P5.3 |
| 12 | On-chip temperature sensor | N/A |
| 13 | Internal shared reference voltage (1.5 V, 2.0 V, or 2.5 V) | N/A |
| 14 | DVSS | N/A |
| 15 | DVCC | N/A |

(1) When A7 is used, the PMM 1.2-V reference voltage can be output to this pin by setting the PMM control register. The 1.2-V voltage can be measured by channel A7.

The analog-to-digital conversion can be started by software or a hardware trigger. 表 6-22 lists the trigger sources that are available.

表 6-22. ADC Trigger Signal Connections

| ADCSHSx | | TRIGGER SOURCE |
|---|---|---|
| BINARY | DECIMAL | |
| 00 | 0 | ADCSC bit (software trigger) |
| 01 | 1 | RTC event |
| 10 | 2 | TB1.1B |
| 11 | 3 | eCOMP0 COUT |

### 6.10.13 Enhanced Comparator

This device features two enhanced comparators: eCOMP0 and eCOMP1. The enhanced comparator is an analog voltage comparator with a built-in 6-bit DAC as an internal voltage reference. The integrated 6-bit DAC can be set to 64 steps for the comparator reference voltage. This module has 4-level programmable hysteresis and configurable power modes: high-power mode or low-power mode.

The eCOMP0 supports a propagation delay up to 1 µs in high-power mode. In low-power mode, eCOMP0 supports 3.2-µs delay with 1.5-µA leakage at room temperature, which can be an ideal wake-up source in LPM3 for a voltage monitor.

The eCOMP1 supports a propagation delay up to 100 ns in high-power mode. In low-power mode, eCOMP1 supports 320-ns delay with 10-µA leakage at room temperature.

Both eCOMP0 and eCOMP1 contains a programmable 6-bit DAC that can use internal shared reference (1.5, 2.0, or 2.5-V) for high precision comparison threshold. In addition to internal shared reference, a low-power 1.2-V reference is fixed at channel 2 of both inverting and non-inverting path that allows the DAC turned off for saving powers.

The eCOMP0 supports external inputs and internal inputs (see 表 6-23) and outputs (see 表 6-25)

**表 6-23. eCOMP0 Input Channel Connections**

| CPPSEL | eCOMP0 CHANNELS | CPNSEL | eCOMP0 CHANNELS |
|---|---|---|---|
| 000 | P1.0/COMP0.0/A0 | 000 | P1.0/COMP0.0/A0 |
| 001 | P1.1/OA0O/COMP0.1/A1 | 001 | P1.1/OA0O/COMP0.1/A1 |
| 010 | Low-power 1.2-V reference | 010 | Low-power 1.2-V reference |
| 011 | N/A | 011 | N/A |
| 100 | N/A | 100 | N/A |
| 101 | P1.1/OA0O/COMP0.1/A1 | 101 | P3.1/OA2O |
| 110 | eCOMP0 6-bit DAC | 110 | eCOMP0 6-bit DAC |

**表 6-24. eCOMP1 Input Channel Connections**

| CPPSEL | eCOMP1 CHANNELS | CPNSEL | eCOMP1 CHANNELS |
|---|---|---|---|
| 000 | P2.5/COMP1.0 | 000 | P2.5/COMP1.0 |
| 001 | P2.4/COMP1.1 | 001 | P2.4/COMP1.1 |
| 010 | Low-power 1.2-V reference | 010 | Low-power 1.2-V reference |
| 011 | N/A | 011 | N/A |
| 100 | N/A | 100 | N/A |
| 101 | P1.5/OA1O/A5 | 101 | P3.5/OA3O |
| 110 | eCOMP1 6-bit DAC | 110 | eCOMP1 6-bit DAC |

**表 6-25. eCOMP0 Output Channel Connections**

| ECOMP0 OUT | EXTERNAL PINOUT, MODULE |
|---|---|
| 1 | P2.0 |
| 2 | TB0.1B, TB0 (TB0OUTH), TB1 (TB1OUTH), ADC trigger |
| 3 | Reserved |
| 4 | Reserved |


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表 6-26. eCOMP1 Output Channel Connections

| ECOMP1 OUT | EXTERNAL PINOUT, MODULE |
|---|---|
| 1 | P2.1 |
| 2 | TB2.1B, TB2 (TB2OUTH), TB3 (TB3OUTH) |
| 3 | Reserved |
| 4 | MFM input |

### 6.10.14 Manchester Function Module (MFM)

The MFM is a dedicated module residing between a pair of pins and eUSCI_B1 to encode and decode Manchester-coded data. For more information, see the MFM chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

When enabled by setting PSEL, the MFM module receives and transmits data through P5.0/TB2.1/MFM.RX/A8 and P5.1/TB2.2/MFM.TX/A9, respectively. The MFM always works in SPI master mode, and the eUSCI_B1 must be configured in 4-wire SPI slave mode.

### 6.10.15 Smart Analog Combo (SAC) (MSP430FR235x Devices Only)

The MSP430FR235x devices integrate four SAC modules: SAC0, SAC1, SAC2, and SAC3. The SAC integrates a high-performance low-power operational amplifier. SAC-L3 supports a hybrid configuration of general-purpose amplifier, 12-bit voltage reference DAC, and a multiplex switch array. For more information, see the SAC chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide*. Only MSP430FR235x devices implement the SAC modules. MSP430FR215x devices do not support SAC modules.

The SAC0 and SAC2 are interconnected and support external inputs and internal inputs (see 表 6-27 and 表 6-28).

表 6-27. SAC0 Channel Connections

| PSEL | SAC0 OA NONINVERTING CHANNELS | NSEL | SAC0 OA INVERTING CHANNELS |
|---|---|---|---|
| 00 | P1.3/OA0+/A3 | 00 | P1.2/OA0-/A2 |
| 01 | SAC0 12-bit DAC | 01 | PGA feedback |
| 10 | P3.1/OA2O, SAC2 OA output | 10 | P3.1/OA2O, SAC2 OA output |
| 11 | N/A | 11 | N/A |

表 6-28. SAC2 Channel Connections

| PSEL | SAC2 OA NONINVERTING CHANNELS | NSEL | SAC2 OA INVERTING CHANNELS |
|---|---|---|---|
| 00 | P3.3/OA2+ | 00 | P3.2/OA2- |
| 01 | SAC2 12-bit DAC | 01 | PGA feedback |
| 10 | P1.1/UCB0CLK/ACLK/OA0O/COMP0.1/A1, SAC0 OA output | 10 | P1.1/UCB0CLK/ACLK/OA0O/COMP0.1/A1, SAC0 OA output |
| 11 | N/A | 11 | N/A |

The SAC1 and SAC3 are interconnected and support external inputs and internal inputs (see 表 6-29 and 表 6-30).

表 6-29. SAC1 Channel Connections

| PSEL | SAC1 OA NONINVERTING CHANNELS | NSEL | SAC1 OA INVERTING CHANNELS |
|---|---|---|---|
| 00 | P1.7/OA1+/A7 | 00 | P1.6/OA1-/A6 |
| 01 | SAC1 12-bit DAC | 01 | PGA feedback |
| 10 | P3.5/OA3O, SAC3 OA output | 10 | P3.5/OA3O, SAC3 OA output |
| 11 | N/A | 11 | N/A |

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表 6-30. SAC3 Channel Connections

| PSEL | SAC3 OA NONINVERTING CHANNELS | NSEL | SAC3 OA INVERTING CHANNELS |
|---|---|---|---|
| 00 | P3.7/OA3+ | 00 | P3.6/OA3- |
| 01 | SAC3 12-bit DAC | 01 | PGA feedback |
| 10 | P1.5/OA1O/A5, SAC1 OA output | 10 | P1.5/OA1O/A5, SAC1 OA output |
| 11 | N/A | 11 | N/A |

Each SAC DAC supports two selectable voltage references (see 表 6-31).

表 6-31. SACx DAC Reference Selection

| DACSREF | SACx DAC REFERENCE SELECTION |
|---|---|
| 0 | DVCC |
| 1 | Internal shared reference (1.5, 2.0, or 2.5 V ) |
| **DACSREF** | **SAC1 DAC REFERENCE** |
| 0 | DVCC |
| 1 | Internal shared reference (1.5, 2.0, or 2.5 V ) |
| **DACSREF** | **SAC2 DAC REFERENCE** |
| 0 | DVCC |
| 1 | Internal shared reference (1.5, 2.0, or 2.5 V ) |
| **DACSREF** | **SAC3 DAC REFERENCE** |
| 0 | DVCC |
| 1 | Internal shared reference (1.5, 2.0, or 2.5 V ) |

Each SAC DAC supports one software trigger and two hardware trigger from chip signals.

表 6-32. SACx DAC Hardware Trigger Selection

| DACLSEL | SAC0 DAC HARDWARE TRIGGER | DACLSEL | SAC1 DAC HARDWARE TRIGGER |
|---|---|---|---|
| 00 | Writing SAC0DACDAT register | 00 | Writing SAC1DACDAT register |
| 01 | N/A | 01 | N/A |
| 10 | TB2.1 | 10 | TB2.1 |
| 11 | TB2.2 | 11 | TB2.2 |
| **DACLSEL** | **SAC2 DAC HARDWARE TRIGGER** | **DACLSEL** | **SAC3 DAC HARDWARE TRIGGER** |
| 00 | Writing SAC2DACDAT register | 00 | Writing SAC3DACDAT register |
| 01 | N/A | 01 | N/A |
| 10 | TB2.1 | 10 | TB2.1 |
| 11 | TB2.2 | 11 | TB2.2 |


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### 6.10.16 eCOMP0, eCOMP1, SAC0, SAC1, SAC2, and SAC3 Interconnection (MSP430FR235x Devices Only)

The high-performance analog modules of eCOMP0, SAC0, and SAC2 are internally connected (see 图 6-1).

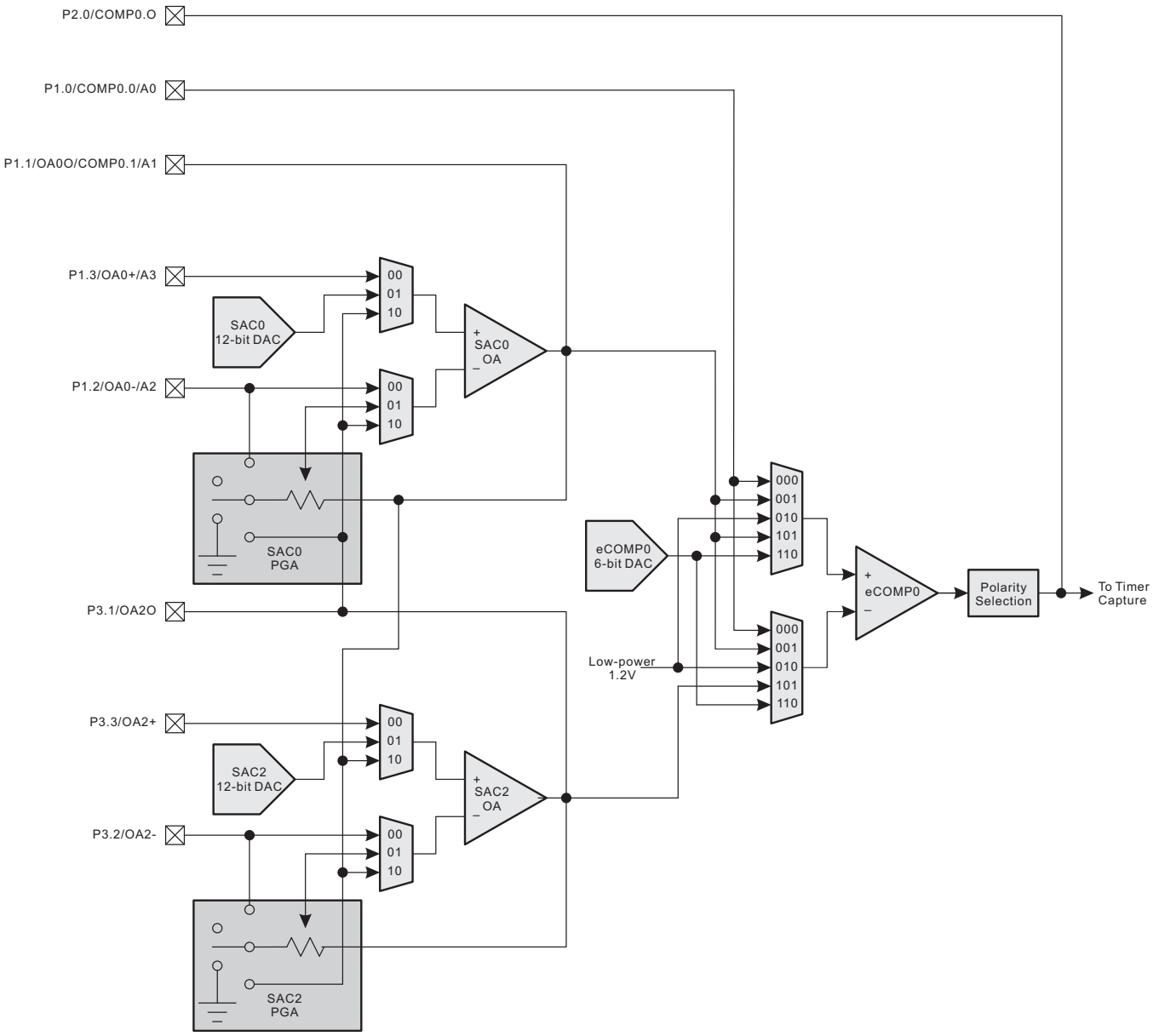



图 6-1. eCOMP0, SAC0, SAC2 Interconnection

The high-performance analog modules of eCOMP1, SAC1, and SAC3 are internally connected (see 图 6-2):

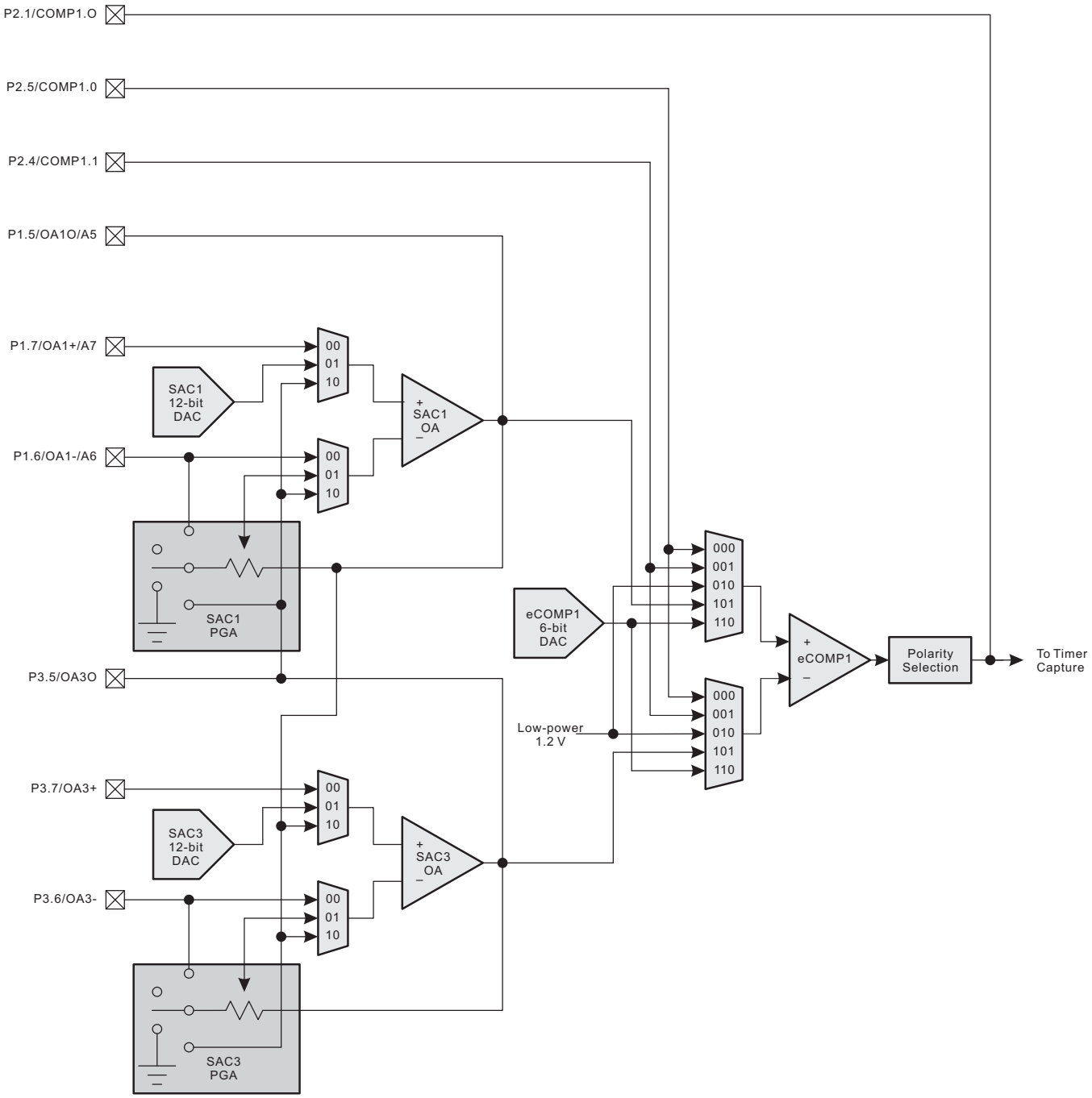



**图 6-2. eCOMP1, SAC1, SAC3 Interconnection**


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### 6.10.17 Cross-Chip Interconnection (SACx are MSP430FR235x Devices Only)

This section describes the cross-chip interconnections in a full-featured view.

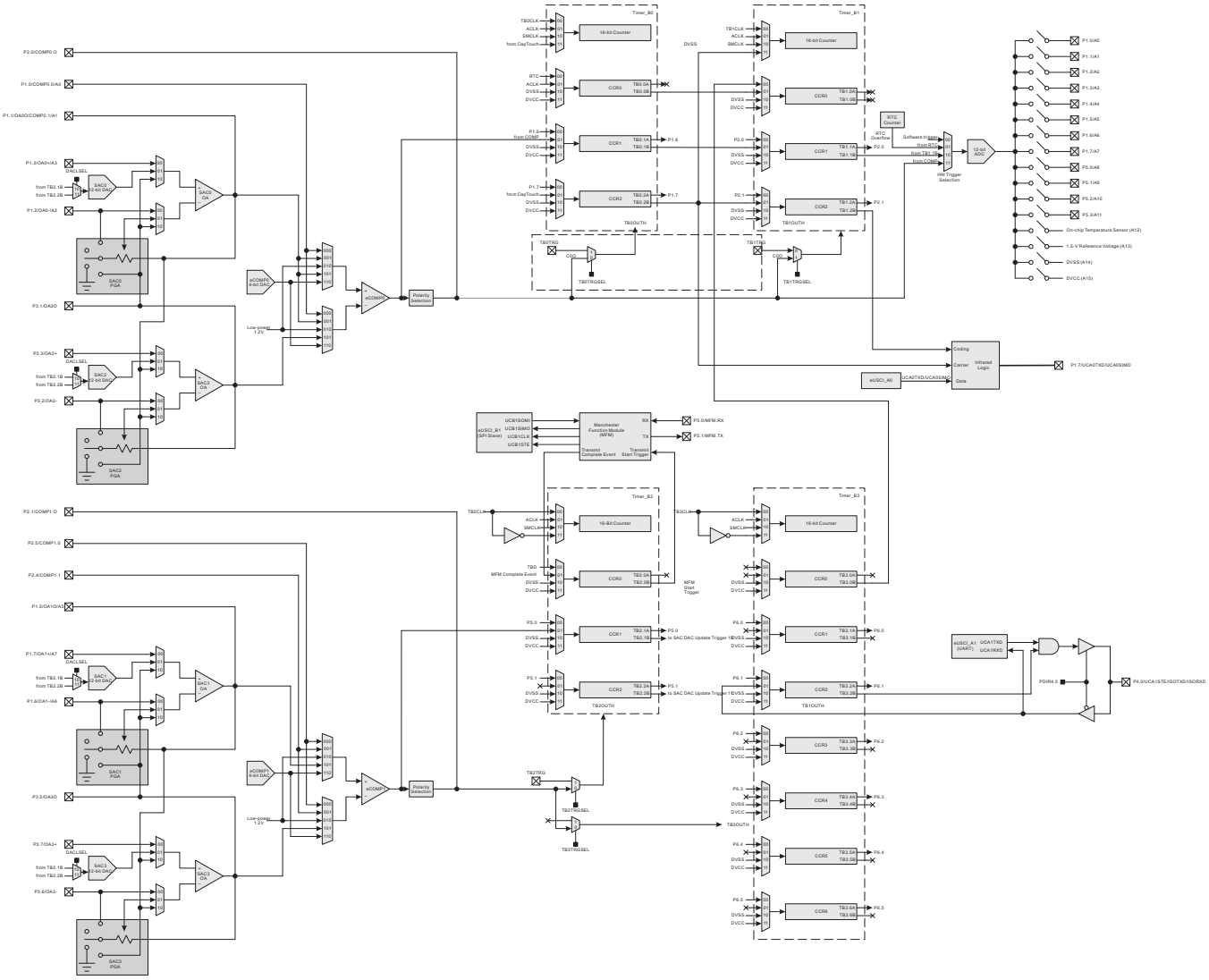


图 6-3. Cross-Chip Interconnection

### 6.10.18 Embedded Emulation Module (EEM)

The EEM supports real-time in-system debugging. The EEM on these devices has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

### 6.10.19 Peripheral File Map

表 6-33 lists the base address and the memory size of each peripheral's registers.

**表 6-33. Peripherals Summary**

| MODULE NAME | BASE ADDRESS | SIZE |
|---|---|---|
| Special Functions (see 表 6-34) | 0100h | 0010h |
| PMM (see 表 6-35) | 0120h | 0020h |
| SYS (see 表 6-36) | 0140h | 0040h |
| CS (see 表 6-37) | 0180h | 0020h |
| FRAM (see 表 6-38) | 01A0h | 0010h |
| CRC (see 表 6-39) | 01C0h | 0008h |
| WDT (see 表 6-40) | 01CCh | 0002h |
| Port P1, P2 (see 表 6-41) | 0200h | 0020h |
| Port P3, P4 (see 表 6-42) | 0220h | 0020h |
| Port P5, P6 (see 表 6-43) | 0240h | 0020h |
| RTC (see 表 6-44) | 0300h | 0010h |
| Timer0_B3 (see 表 6-45) | 0380h | 0030h |
| Timer1_B3 (see 表 6-46) | 03C0h | 0030h |
| Timer2_B3 (see 表 6-47) | 0400h | 0030h |
| Timer3_B7 (see 表 6-48) | 0440h | 0030h |
| MPY32 (see 表 6-49) | 04C0h | 0030h |
| eUSCI_A0 (see 表 6-50) | 0500h | 0020h |
| eUSCI_B0 (see 表 6-51) | 0540h | 0030h |
| eUSCI_A1 (see 表 6-52) | 0580h | 0020h |
| eUSCI_B1 (see 表 6-53) | 05C0h | 0030h |
| Backup Memory (see 表 6-54) | 0660h | 0020h |
| ICC (see 表 6-55) | 06C0h | 0010h |
| ADC (see 表 6-56) | 0700h | 0040h |
| eCOMP0 (see 表 6-57) | 08E0h | 0020h |
| eCOMP1 (see 表 6-58) | 0900h | 0020h |
| SAC0 (see 表 6-59)(1) | 0C80h | 0010h |
| SAC1 (see 表 6-60)(1) | 0C90h | 0010h |
| SAC2 (see 表 6-61)(1) | 0CA0h | 0010h |
| SAC3 (see 表 6-62)(1) | 0CB0h | 0010h |

(1) MSP430FR235x devices only


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表 **6-34. Special Function Registers (Base Address: 0100h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| SFR interrupt enable | SFRIE1 | 00h |
| SFR interrupt flag | SFRIFG1 | 02h |
| SFR reset pin control | SFRRPCR | 04h |

表 **6-35. PMM Registers (Base Address: 0120h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| PMM control 0 | PMMCTL0 | 00h |
| PMM control 1 | PMMCTL1 | 02h |
| PMM control 2 | PMMCTL2 | 04h |
| PMM interrupt flags | PMMIFG | 0Ah |
| PM5 control 0 | PM5CTL0 | 10h |

表 **6-36. SYS Registers (Base Address: 0140h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| System control | SYSCTL | 00h |
| Bootloader configuration area | SYSBSLC | 02h |
| JTAG mailbox control | SYSJMBC | 06h |
| JTAG mailbox input 0 | SYSJMBI0 | 08h |
| JTAG mailbox input 1 | SYSJMBI1 | 0Ah |
| JTAG mailbox output 0 | SYSJMBO0 | 0Ch |
| JTAG mailbox output 1 | SYSJMBO1 | 0Eh |
| User NMI vector generator | SYSUNIV | 1Ah |
| System NMI vector generator | SYSSNIV | 1Ch |
| Reset vector generator | SYSRSTIV | 1Eh |
| System configuration 0 | SYSCFG0 | 20h |
| System configuration 1 | SYSCFG1 | 22h |
| System configuration 2 | SYSCFG2 | 24h |
| System configuration 3 | SYSCFG3 | 26h |

表 **6-37. CS Registers (Base Address: 0180h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| CS control 0 | CSCTL0 | 00h |
| CS control 1 | CSCTL1 | 02h |
| CS control 2 | CSCTL2 | 04h |
| CS control 3 | CSCTL3 | 06h |
| CS control 4 | CSCTL4 | 08h |
| CS control 5 | CSCTL5 | 0Ah |
| CS control 6 | CSCTL6 | 0Ch |
| CS control 7 | CSCTL7 | 0Eh |
| CS control 8 | CSCTL8 | 10h |

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表 6-38. FRAM Registers (Base Address: 01A0h)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| FRAM control 0 | FRCTL0 | 00h |
| General control 0 | GCCTL0 | 04h |
| General control 1 | GCCTL1 | 06h |

表 6-39. CRC Registers (Base Address: 01C0h)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| CRC data input | CRC16DI | 00h |
| CRC data input reverse byte | CRCDIRB | 02h |
| CRC initialization and result | CRCINIRES | 04h |
| CRC result reverse byte | CRCRESR | 06h |

表 6-40. WDT Registers (Base Address: 01CCh)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| Watchdog timer control | WDTCTL | 00h |

表 6-41. Port P1, P2 Registers (Base Address: 0200h)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| Port P1 input | P1IN | 00h |
| Port P1 output | P1OUT | 02h |
| Port P1 direction | P1DIR | 04h |
| Port P1 pulling enable | P1REN | 06h |
| Port P1 selection 0 | P1SEL0 | 0Ah |
| Port P1 selection 1 | P1SEL1 | 0Ch |
| Port P1 interrupt vector word | P1IV | 0Eh |
| Port P1 complement selection | P1SELC | 16h |
| Port P1 interrupt edge select | P1IES | 18h |
| Port P1 interrupt enable | P1IE | 1Ah |
| Port P1 interrupt flag | P1IFG | 1Ch |
| Port P2 input | P2IN | 01h |
| Port P2 output | P2OUT | 03h |
| Port P2 direction | P2DIR | 05h |
| Port P2 pulling enable | P2REN | 07h |
| Port P2 selection 0 | P2SEL0 | 0Bh |
| Port P2 selection 1 | P2SEL1 | 0Dh |
| Port P2 interrupt vector word | P2IV | 1Eh |
| Port P2 complement selection | P2SELC | 17h |
| Port P2 interrupt edge select | P2IES | 19h |
| Port P2 interrupt enable | P2IE | 1Bh |
| Port P2 interrupt flag | P2IFG | 1Dh |


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表 **6-42. Port P3, P4 Registers (Base Address: 0220h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| Port P3 input | P3IN | 00h |
| Port P3 output | P3OUT | 02h |
| Port P3 direction | P3DIR | 04h |
| Port P3 pulling enable | P3REN | 06h |
| Port P3 selection 0 | P3SEL0 | 0Ah |
| Port P3 selection 1 | P3SEL1 | 0Ch |
| Port P3 interrupt vector word | P3IV | 0Eh |
| Port P3 complement selection | P3SELC | 16h |
| Port P3 interrupt edge select | P3IES | 18h |
| Port P3 interrupt enable | P3IE | 1Ah |
| Port P3 interrupt flag | P3IFG | 1Ch |
| Port P4 input | P4IN | 01h |
| Port P4 output | P4OUT | 03h |
| Port P4 direction | P4DIR | 05h |
| Port P4 pulling enable | P4REN | 07h |
| Port P4 selection 0 | P4SEL0 | 0Bh |
| Port P4 selection 1 | P4SEL1 | 0Dh |
| Port P4 interrupt vector word | P4IV | 1Eh |
| Port P4 complement selection | P4SELC | 17h |
| Port P4 interrupt edge select | P4IES | 19h |
| Port P4 interrupt enable | P4IE | 1Bh |
| Port P4 interrupt flag | P4IFG | 1Dh |

表 **6-43. Port P5, P6 Registers (Base Address: 0240h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| Port P5 input | P5IN | 00h |
| Port P5 output | P5OUT | 02h |
| Port P5 direction | P5DIR | 04h |
| Port P5 pulling enable | P5REN | 06h |
| Port P5 selection 0 | P5SEL0 | 0Ah |
| Port P5 selection 1 | P5SEL1 | 0Ch |
| Port P5 complement selection | P5SELC | 16h |
| Port P6 input | P6IN | 01h |
| Port P6 output | P6OUT | 03h |
| Port P6 direction | P6DIR | 05h |
| Port P6 pulling enable | P6REN | 07h |
| Port P6 selection 0 | P6SEL0 | 0Bh |
| Port P6 selection 1 | P6SEL1 | 0Dh |
| Port P6 complement selection | P6SELC | 17h |

表 **6-44. RTC Registers (Base Address: 0300h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| RTC control | RTCCTL | 00h |
| RTC interrupt vector | RTCIV | 04h |
| RTC modulo | RTCMOD | 08h |
| RTC counter | RTCCNT | 0Ch |

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表 6-45. Timer0_B3 Registers (Base Address: 0380h)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| TB0 control | TB0CTL | 00h |
| Capture/compare control 0 | TB0CCTL0 | 02h |
| Capture/compare control 1 | TB0CCTL1 | 04h |
| Capture/compare control 2 | TB0CCTL2 | 06h |
| TB0 counter | TB0R | 10h |
| Capture/compare 0 | TB0CCR0 | 12h |
| Capture/compare 1 | TB0CCR1 | 14h |
| Capture/compare 2 | TB0CCR2 | 16h |
| TB0 expansion 0 | TB0EX0 | 20h |
| TB0 interrupt vector | TB0IV | 2Eh |

表 6-46. Timer1_B3 Registers (Base Address: 03C0h)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| TB1 control | TB1CTL | 00h |
| Capture/compare control 0 | TB1CCTL0 | 02h |
| Capture/compare control 1 | TB1CCTL1 | 04h |
| Capture/compare control 2 | TB1CCTL2 | 06h |
| TB1 counter | TB1R | 10h |
| Capture/compare 0 | TB1CCR0 | 12h |
| Capture/compare 1 | TB1CCR1 | 14h |
| Capture/compare 2 | TB1CCR2 | 16h |
| TB1 expansion 0 | TB1EX0 | 20h |
| TB1 interrupt vector | TB1IV | 2Eh |

表 6-47. Timer2_B3 Registers (Base Address: 0400h)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| TB2 control | TB2CTL | 00h |
| Capture/compare control 0 | TB2CCTL0 | 02h |
| Capture/compare control 1 | TB2CCTL1 | 04h |
| Capture/compare control 2 | TB2CCTL2 | 06h |
| TB2 counter | TB2R | 10h |
| Capture/compare 0 | TB2CCR0 | 12h |
| Capture/compare 1 | TB2CCR1 | 14h |
| Capture/compare 2 | TB2CCR2 | 16h |
| TB2 expansion 0 | TB2EX0 | 20h |
| TB2 interrupt vector | TB2IV | 2Eh |


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表 **6-48. Timer3_B7 Registers (Base Address: 0440h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| TB3 control | TB3CTL | 00h |
| Capture/compare control 0 | TB3CCTL0 | 02h |
| Capture/compare control 1 | TB3CCTL1 | 04h |
| Capture/compare control 2 | TB3CCTL2 | 06h |
| Capture/compare control 3 | TB3CCTL3 | 08h |
| Capture/compare control 4 | TB3CCTL4 | 0Ah |
| Capture/compare control 5 | TB3CCTL5 | 0Ch |
| Capture/compare control 6 | TB3CCTL6 | 0Eh |
| TB3 counter | TB3R | 10h |
| Capture/compare 0 | TB3CCR0 | 12h |
| Capture/compare 1 | TB3CCR1 | 14h |
| Capture/compare 2 | TB3CCR2 | 16h |
| Capture/compare 3 | TB3CCR3 | 18h |
| Capture/compare 4 | TB3CCR4 | 1Ah |
| Capture/compare 5 | TB3CCR5 | 1Ch |
| Capture/compare 6 | TB3CCR6 | 1Eh |
| TB3 expansion 0 | TB3EX0 | 20h |
| TB3 interrupt vector | TB3IV | 2Eh |

表 **6-49. MPY32 Registers (Base Address: 04C0h)**

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| 16-bit operand 1 – multiply | MPY | 00h |
| 16-bit operand 1 – signed multiply | MPYS | 02h |
| 16-bit operand 1 – multiply accumulate | MAC | 04h |
| 16-bit operand 1 – signed multiply accumulate | MACS | 06h |
| 16-bit operand 2 | OP2 | 08h |
| 16 × 16 result low word | RESLO | 0Ah |
| 16 × 16 result high word | RESHI | 0Ch |
| 16 × 16 sum extension | SUMEXT | 0Eh |
| 32-bit operand 1 – multiply low word | MPY32L | 10h |
| 32-bit operand 1 – multiply high word | MPY32H | 12h |
| 32-bit operand 1 – signed multiply low word | MPYS32L | 14h |
| 32-bit operand 1 – signed multiply high word | MPYS32H | 16h |
| 32-bit operand 1 – multiply accumulate low word | MAC32L | 18h |
| 32-bit operand 1 – multiply accumulate high word | MAC32H | 1Ah |
| 32-bit operand 1 – signed multiply accumulate low word | MACS32L | 1Ch |
| 32-bit operand 1 – signed multiply accumulate high word | MACS32H | 1Eh |
| 32-bit operand 2 – low word | OP2L | 20h |
| 32-bit operand 2 – high word | OP2H | 22h |
| 32 × 32 result 0 – least significant word | RES0 | 24h |
| 32 × 32 result 1 | RES1 | 26h |
| 32 × 32 result 2 | RES2 | 28h |
| 32 × 32 result 3 – most significant word | RES3 | 2Ah |
| MPY32 control 0 | MPY32CTL0 | 2Ch |

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表 6-50. eUSCI_A0 Registers (Base Address: 0500h)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| eUSCI_A control word 0 | UCA0CTLW0 | 00h |
| eUSCI_A control word 1 | UCA0CTLW1 | 02h |
| eUSCI_A control rate 0 | UCA0BR0 | 06h |
| eUSCI_A control rate 1 | UCA0BR1 | 07h |
| eUSCI_A modulation control | UCA0MCTLW | 08h |
| eUSCI_A status | UCA0STAT | 0Ah |
| eUSCI_A receive buffer | UCA0RXBUF | 0Ch |
| eUSCI_A transmit buffer | UCA0TXBUF | 0Eh |
| eUSCI_A LIN control | UCA0ABCTL | 10h |
| eUSCI_A IrDA transmit control | lUCA0IRTCTL | 12h |
| eUSCI_A IrDA receive control | lUCA0IRRCTL | 13h |
| eUSCI_A interrupt enable | UCA0IE | 1Ah |
| eUSCI_A interrupt flags | UCA0IFG | 1Ch |
| eUSCI_A interrupt vector word | UCA0IV | 1Eh |

表 6-51. eUSCI_B0 Registers (Base Address: 0540h)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| eUSCI_B control word 0 | UCB0CTLW0 | 00h |
| eUSCI_B control word 1 | UCB0CTLW1 | 02h |
| eUSCI_B bit rate 0 | UCB0BR0 | 06h |
| eUSCI_B bit rate 1 | UCB0BR1 | 07h |
| eUSCI_B status word | UCB0STATW | 08h |
| eUSCI_B byte counter threshold | UCB0TBCNT | 0Ah |
| eUSCI_B receive buffer | UCB0RXBUF | 0Ch |
| eUSCI_B transmit buffer | UCB0TXBUF | 0Eh |
| eUSCI_B I2C own address 0 | UCB0I2COA0 | 14h |
| eUSCI_B I2C own address 1 | UCB0I2COA1 | 16h |
| eUSCI_B I2C own address 2 | UCB0I2COA2 | 18h |
| eUSCI_B I2C own address 3 | UCB0I2COA3 | 1Ah |
| eUSCI_B receive address | UCB0ADDRX | 1Ch |
| eUSCI_B address mask | UCB0ADDMASK | 1Eh |
| eUSCI_B I2C slave address | UCB0I2CSA | 20h |
| eUSCI_B interrupt enable | UCB0IE | 2Ah |
| eUSCI_B interrupt flags | UCB0IFG | 2Ch |
| eUSCI_B interrupt vector word | UCB0IV | 2Eh |


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表 6-52. eUSCI_A1 Registers (Base Address: 0580h)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| eUSCI_A control word 0 | UCA1CTLW0 | 00h |
| eUSCI_A control word 1 | UCA1CTLW1 | 02h |
| eUSCI_A control rate 0 | UCA1BR0 | 06h |
| eUSCI_A control rate 1 | UCA1BR1 | 07h |
| eUSCI_A modulation control | UCA1MCTLW | 08h |
| eUSCI_A status | UCA1STAT | 0Ah |
| eUSCI_A receive buffer | UCA1RXBUF | 0Ch |
| eUSCI_A transmit buffer | UCA1TXBUF | 0Eh |
| eUSCI_A LIN control | UCA1ABCTL | 10h |
| eUSCI_A IrDA transmit control | lUCA1IRTCTL | 12h |
| eUSCI_A IrDA receive control | lUCA1IRRCTL | 13h |
| eUSCI_A interrupt enable | UCA1IE | 1Ah |
| eUSCI_A interrupt flags | UCA1IFG | 1Ch |
| eUSCI_A interrupt vector word | UCA1IV | 1Eh |

表 6-53. eUSCI_B1 Registers (Base Address: 05C0h)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| eUSCI_B control word 0 | UCB1CTLW0 | 00h |
| eUSCI_B control word 1 | UCB1CTLW1 | 02h |
| eUSCI_B bit rate 0 | UCB1BR0 | 06h |
| eUSCI_B bit rate 1 | UCB1BR1 | 07h |
| eUSCI_B status word | UCB1STATW | 08h |
| eUSCI_B byte counter threshold | UCB1TBCNT | 0Ah |
| eUSCI_B receive buffer | UCB1RXBUF | 0Ch |
| eUSCI_B transmit buffer | UCB1TXBUF | 0Eh |
| eUSCI_B I2C own address 0 | UCB1I2COA0 | 14h |
| eUSCI_B I2C own address 1 | UCB1I2COA1 | 16h |
| eUSCI_B I2C own address 2 | UCB1I2COA2 | 18h |
| eUSCI_B I2C own address 3 | UCB1I2COA3 | 1Ah |
| eUSCI_B receive address | UCB1ADDRX | 1Ch |
| eUSCI_B address mask | UCB1ADDMASK | 1Eh |
| eUSCI_B I2C slave address | UCB1I2CSA | 20h |
| eUSCI_B interrupt enable | UCB1IE | 2Ah |
| eUSCI_B interrupt flags | UCB1IFG | 2Ch |
| eUSCI_B interrupt vector word | UCB1IV | 2Eh |

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表 6-54. Backup Memory Registers (Base Address: 0660h)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| Backup memory 0 | BAKMEM0 | 00h |
| Backup memory 1 | BAKMEM1 | 02h |
| Backup memory 2 | BAKMEM2 | 04h |
| Backup memory 3 | BAKMEM3 | 06h |
| Backup memory 4 | BAKMEM4 | 08h |
| Backup memory 5 | BAKMEM5 | 0Ah |
| Backup memory 6 | BAKMEM6 | 0Ch |
| Backup memory 7 | BAKMEM7 | 0Eh |
| Backup memory 8 | BAKMEM8 | 10h |
| Backup memory 9 | BAKMEM9 | 12h |
| Backup memory 10 | BAKMEM10 | 14h |
| Backup memory 11 | BAKMEM11 | 16h |
| Backup memory 12 | BAKMEM12 | 18h |
| Backup memory 13 | BAKMEM13 | 1Ah |
| Backup memory 14 | BAKMEM14 | 1Ch |
| Backup memory 15 | BAKMEM15 | 1Eh |

表 6-55. ICC Registers (Base Address: 06C0h)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| ICC status and control | ICCSC | 00h |
| ICC mask virtual stack | ICCMVS | 02h |
| ICC interrupt level setting 0 | ICCILSR0 | 04h |
| ICC interrupt level setting 1 | ICCILSR1 | 06h |
| ICC interrupt level setting 2 | ICCILSR2 | 08h |
| ICC interrupt level setting 3 | ICCILSR3 | 0Ah |

表 6-56. ADC Registers (Base Address: 0700h)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| ADC control 0 | ADCCTL0 | 00h |
| ADC control 1 | ADCCTL1 | 02h |
| ADC control 2 | ADCCTL2 | 04h |
| ADC window comparator low threshold | ADCLO | 06h |
| ADC window comparator high threshold | ADCHI | 08h |
| ADC memory control 0 | ADCMCTL0 | 0Ah |
| ADC conversion memory | ADCMEM0 | 12h |
| ADC interrupt enable | ADCIE | 1Ah |
| ADC interrupt flags | ADCIFG | 1Ch |
| ADC interrupt vector word | ADCIV | 1Eh |


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表 6-57. eCOMP0 Registers (Base Address: 08E0h)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| Comparator control 0 | CP0CTL0 | 00h |
| Comparator control 1 | CP0CTL1 | 02h |
| Comparator interrupt | CP0INT | 06h |
| Comparator interrupt vector | CP0IV | 08h |
| Comparator built-in DAC control | CP0DACCTL | 10h |
| Comparator built-in DAC data | CP0DACDATA | 12h |

表 6-58. eCOMP1 Registers (Base Address: 0900h)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| Comparator control 0 | CP1CTL0 | 00h |
| Comparator control 1 | CP1CTL1 | 02h |
| Comparator interrupt | CP1INT | 06h |
| Comparator interrupt vector | CP1IV | 08h |
| Comparator built-in DAC control | CP1DACCTL | 10h |
| Comparator built-in DAC data | CP1DACDATA | 12h |

表 6-59. SAC0 Registers (Base Address: 0C80h, MSP430FR235x Devices Only)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| SAC0 OA control | SAC0OA | 00h |
| SAC0 PGA control | SAC0PGA | 02h |
| SAC0 DAC control | SAC0DAC | 04h |
| SAC0 DAC data | SAC0DAT | 06h |
| SAC0 DAC status | SAC0DATSTS | 08h |
| SAC0 interrupt vector | SAC0IV | 0Ah |

表 6-60. SAC1 Registers (Base Address: 0C90h, MSP430FR235x Devices Only)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| SAC1 OA control | SAC1OA | 00h |
| SAC1 PGA control | SAC1PGA | 02h |
| SAC1 DAC control | SAC1DAC | 04h |
| SAC1 DAC data | SAC1DAT | 06h |
| SAC1 DAC status | SAC1DATSTS | 08h |
| SAC1 interrupt vector | SAC1IV | 0Ah |

表 6-61. SAC2 Registers (Base Address: 0CA0h, MSP430FR235x Devices Only)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| SAC2 OA control | SAC2OA | 00h |
| SAC2 PGA control | SAC2PGA | 02h |
| SAC2 DAC control | SAC2DAC | 04h |
| SAC2 DAC data | SAC2DAT | 06h |
| SAC2 DAC status | SAC2DATSTS | 08h |
| SAC2 interrupt vector | SAC2IV | 0Ah |

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表 6-62. SAC3 Registers (Base Address: 0CB0h, MSP430FR235x Devices Only)

| REGISTER DESCRIPTION | ACRONYM | OFFSET |
|---|---|---|
| SAC3 OA control | SAC3OA | 00h |
| SAC3 PGA control | SAC3PGA | 02h |
| SAC3 DAC control | SAC3DAC | 04h |
| SAC3 DAC data | SAC3DAT | 06h |
| SAC3 DAC status | SAC3DATSTS | 08h |
| SAC3 interrupt vector | SAC3IV | 0Ah |


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## 6.11 Input/Output Diagrams

### 6.11.1 Port P1 Input/Output With Schmitt Trigger

图 6-4 shows the port diagram. 表 6-63 summarizes the selection of the port function.

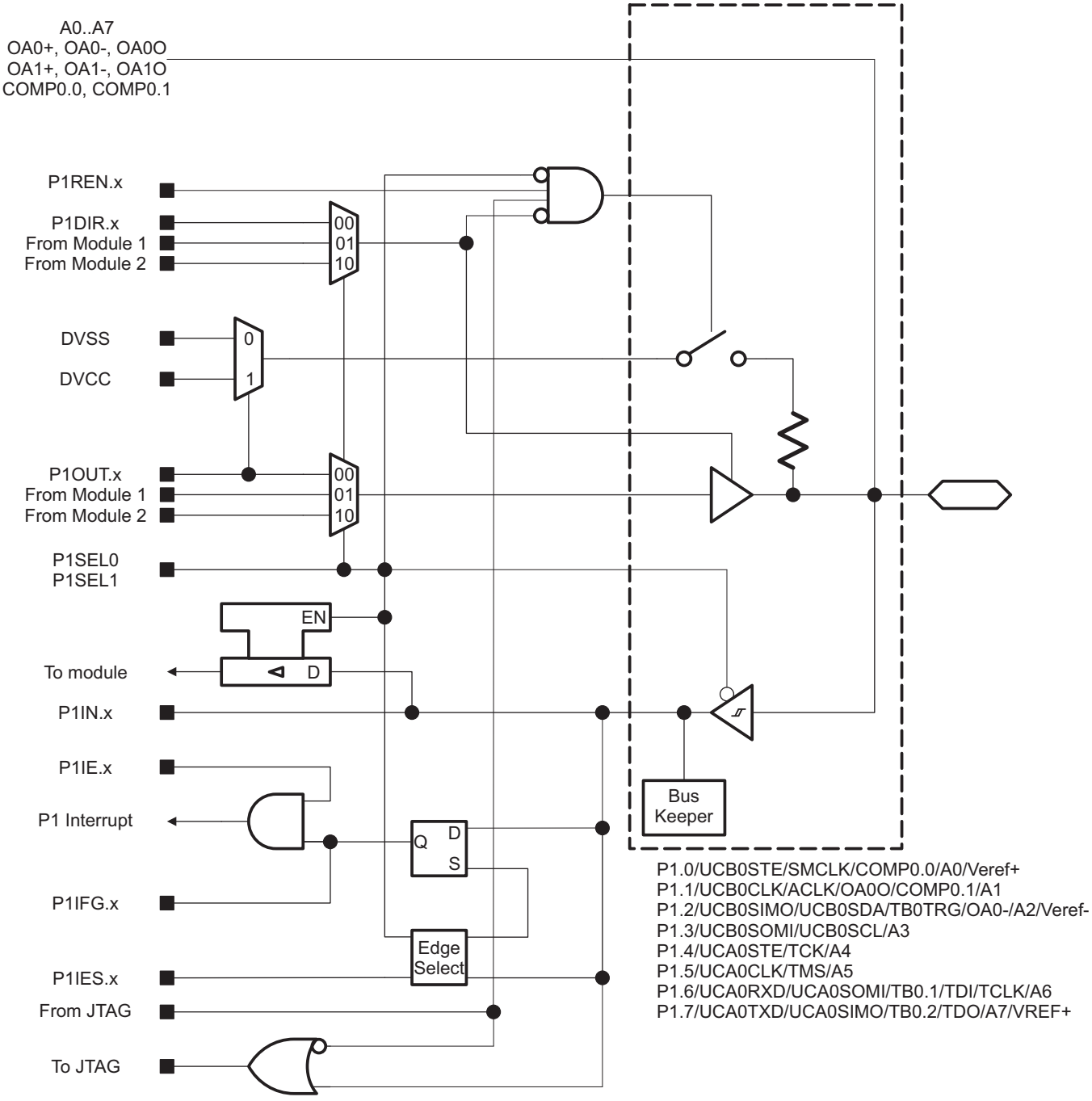



图 6-4. Port P1 Input/Output With Schmitt Trigger

表 6-63. Port P1 Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS AND SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P1DIR.x | P1SELx | JTAG |
| P1.0/UCB0STE/SMCLK/ COMP0.0/A0/Veref+ | 0 | P1.0 (I/O) | I: 0; O: 1 | 00 | N/A |
| | | UCB0STE | X | 01 | N/A |
| | | SMCLK | 1 | 10 | N/A |
| | | VSS | 0 | | |
| | | COMP0.0, A0/Veref+ | X | 11 | N/A |
| P1.1/UCB0CLK/ACLK/ OA0O/COMP0.1/A1 | 1 | P1.1 (I/O) | I: 0; O: 1 | 0 | N/A |
| | | UCB0CLK | X | 01 | N/A |
| | | ACLK | 1 | 10 | N/A |
| | | VSS | 0 | | |
| | | OA0O(2), COMP0.1, A1 | X | 11 | N/A |
| P1.2/UCB0SIMO/ UCB0SDA/TB0TRG/ OA0-/A2/Veref- | 2 | P1.2 (I/O) | I: 0; O: 1 | 00 | N/A |
| | | UCB0SIMO/UCB0SDA | X | 01 | N/A |
| | | TB0TRG | 0 | 10 | N/A |
| | | OA0-(2), A2/Veref- | X | 11 | N/A |
| P1.3/UCB0SOMI/ UCB0SCL/OA0+/A3 | 3 | P1.3 (I/O) | I: 0; O: 1 | 00 | N/A |
| | | UCB0SOMI/UCB0SCL | X | 01 | N/A |
| | | OA0+(2), A3 | X | 11 | N/A |
| P1.4/UCA0STE/TCK/A4 | 4 | P1.4 (I/O) | I: 0; O: 1 | 00 | Disabled |
| | | UCA0STE | X | 01 | Disabled |
| | | A4 | X | 11 | Disabled |
| | | JTAG TCK | X | X | TCK |
| P1.5/UCA0CLK/TMS/ OA1O/A5 | 5 | P1.5 (I/O) | I: 0; O: 1 | 00 | Disabled |
| | | UCA0CLK | X | 01 | Disabled |
| | | OA1O(2), A5 | X | 11 | Disabled |
| | | JTAG TMS | X | X | TMS |
| P1.6/UCA0RXD/ UCA0SOMI/TB0.1/TDI/ TCLK/OA1-/A6 | 6 | P1.6 (I/O) | I: 0; O: 1 | 00 | Disabled |
| | | UCA0RXD/UCA0SOMI | X | 01 | Disabled |
| | | TB0.CCI1A | 0 | 10 | Disabled |
| | | TB0.1 | 1 | | |
| | | OA1-(2), A6 | X | 11 | Disabled |
| | | JTAG TDI/TCLK | X | X | TDI/TCLK |
| P1.7/UCA0TXD/ UCA0SIMO/TB0.2/TDO/ OA1+/A7/VREF+ | 7 | P1.7 (I/O) | I: 0; O: 1 | 00 | Disabled |
| | | UCA0TXD/UCA0SIMO | X | 01 | Disabled |
| | | TB0.CCI2A | 0 | 10 | Disabled |
| | | TB0.2 | 1 | | |
| | | OA1+(2), A7, VREF+ | X | 11 | Disabled |
| | | JTAG TDO | X | X | TDO |

(1) X = don't care
(2) MSP430FR235x devices only


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### 6.11.2 Port P2 Input/Output With Schmitt Trigger

图 6-5 shows the port diagram. 表 6-64 summarizes the selection of the port function.

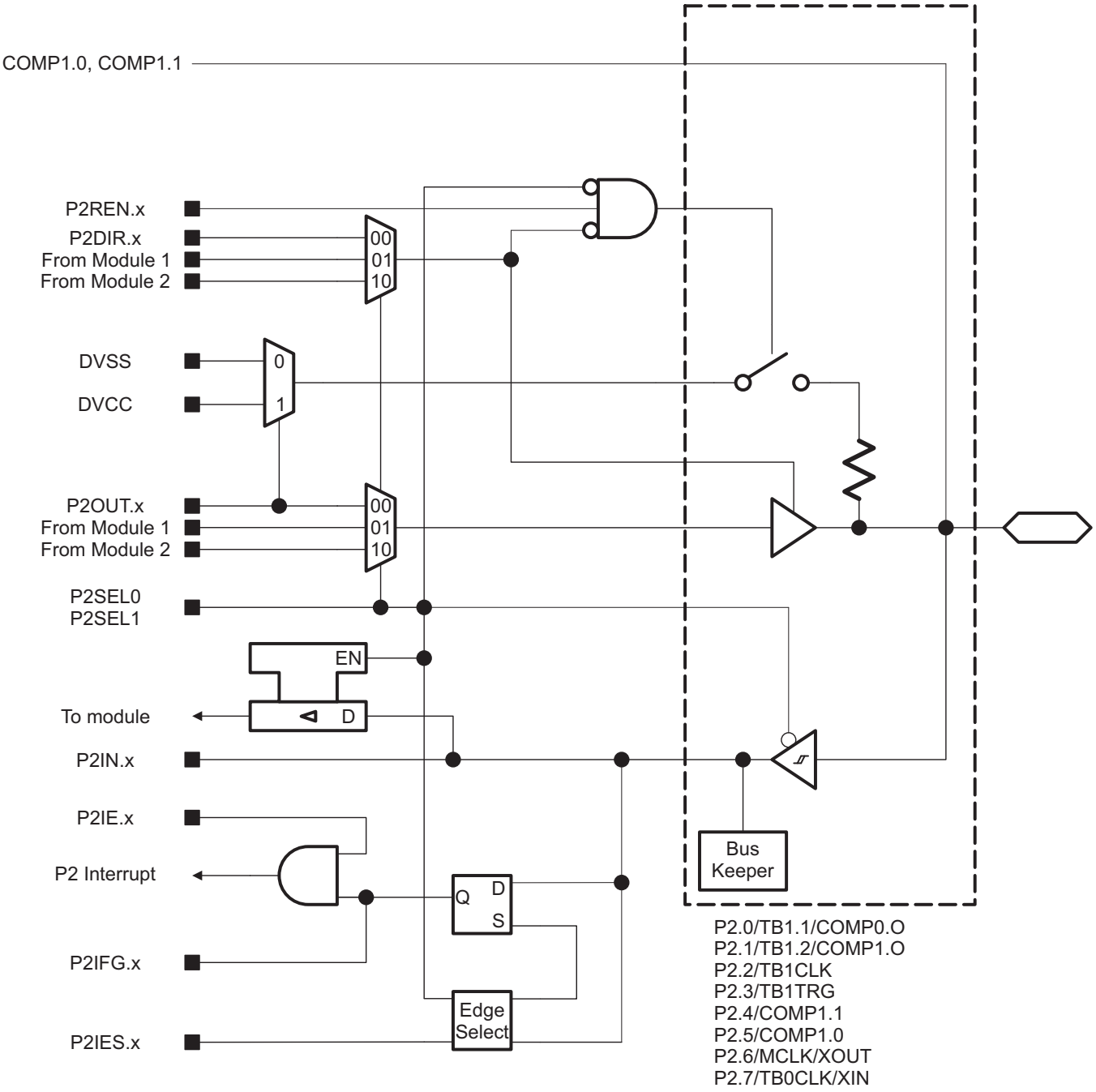



**图 6-5. Port P2 Input/Output With Schmitt Trigger**

表 6-64. Port P2 Pin Functions

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS AND SIGNALS(1) | |
|---|---|---|---|---|
| | | | P2DIR.x | P2SELx |
| P2.0/TB1.1/COMP0.O | 0 | P2.0 (I/O) | I: 0; O: 1 | 00 |
| | | TB1.CCI1A | 0 | 01 |
| | | TB1.1 | 1 | |
| | | COMP0.O | 1 | 10 |
| P2.1/TB1.2 | 1 | P2.1 (I/O)0 | I: 0; O: 1 | 00 |
| | | TB1.CCI2A | 0 | 01 |
| | | TB1.2 | 1 | |
| | | COMP1.O | 1 | 10 |
| P2.2/TB1CLK | 2 | P2.2 (I/O) | I: 0; O: 1 | 00 |
| | | TB1CLK | 0 | 01 |
| P2.3/UCB0CLK/TB1TRG | 3 | P2.3 (I/O) | I: 0; O: 1 | 00 |
| | | TB1TRG | 0 | 01 |
| | | VSS | 1 | |
| P2.4/COMP1.1 | 4 | P2.4 (I/O) | I: 0; O: 1 | 00 |
| | | COMP1.1 | X | 11 |
| P2.5/COMP1.0 | 5 | P2.5 (I/O) | I: 0; O: 1 | 00 |
| | | COMP1.0 | X | 11 |
| P2.6/MCLK/XOUT | 6 | P2.6 (I/O) | I: 0; O: 1 | 00 |
| | | MCLK | 1 | 01 |
| | | VSS | 0 | |
| | | XOUT | X | 10 |
| P2.7/TB0CLK/XIN | 7 | P2.7 (I/O) | I: 0; O: 1 | 00 |
| | | TB0CLK | 0 | 01 |
| | | VSS | 1 | |
| | | XIN | X | 10 |

(1) X = don't care


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### 6.11.3 Port P3 Input/Output With Schmitt Trigger

图 6-6 shows the port diagram. 表 6-65 summarizes the selection of the port function.

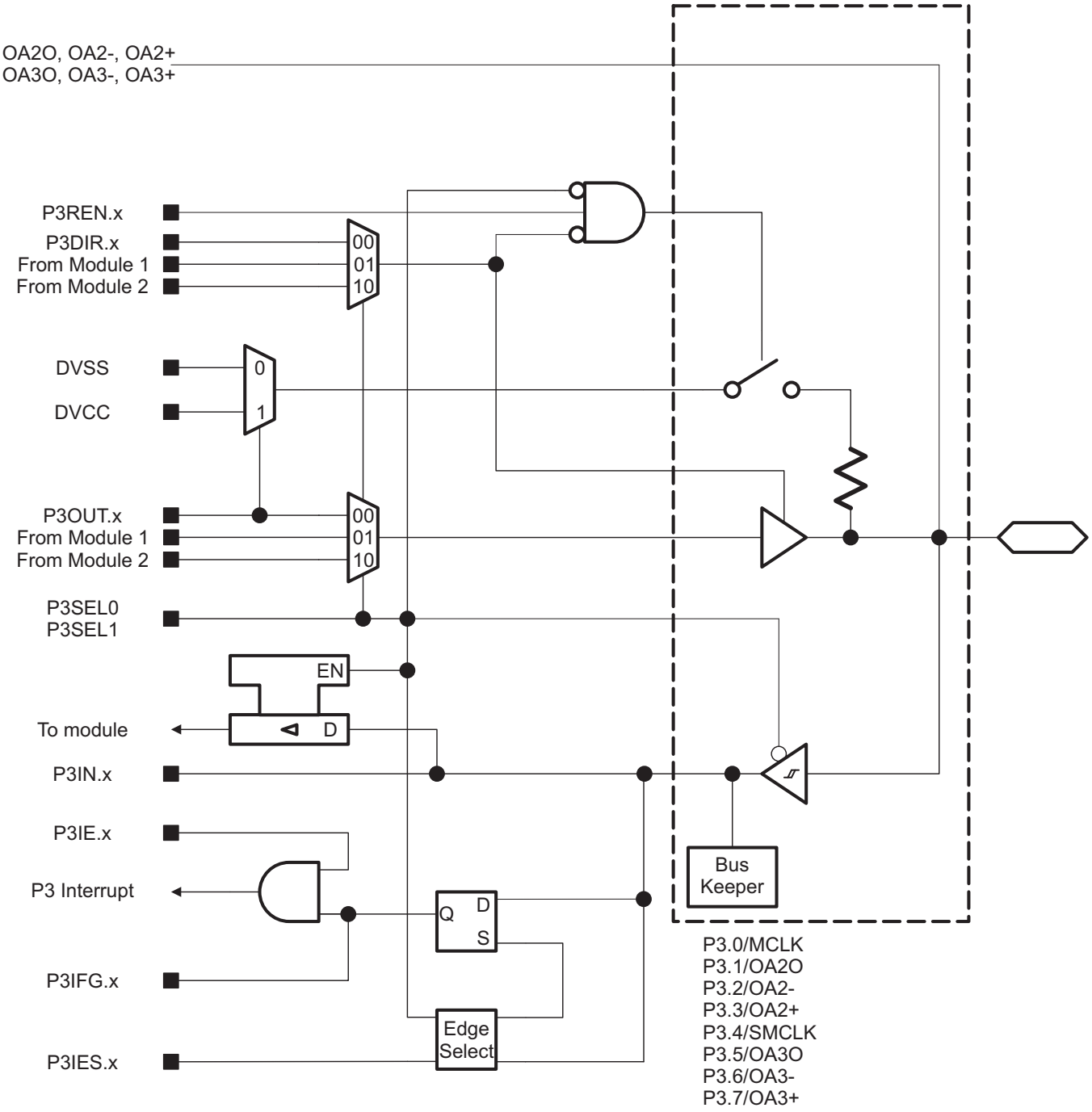



**图 6-6. Port P3 Input/Output With Schmitt Trigger**

表 6-65. Port P3 Pin Functions

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS AND SIGNALS(1) | |
|---|---|---|---|---|
| | | | P3DIR.x | P3SELx |
| P3.0/MCLK | 0 | P3.0 (I/O) | I: 0; O: 1 | 00 |
| | | MCLK | 1 | 01 |
| | | VSS | 0 | |
| P3.1/OA2O | 1 | P3.1 (I/O) | I: 0; O: 1 | 00 |
| | | OA2O(2) | X | 11 |
| P3.2/OA2- | 2 | P3.2 (I/O) | I: 0; O: 1 | 00 |
| | | OA2-(2) | X | 11 |
| P3.3/OA2+ | 3 | P3.3 (I/O) | I: 0; O: 1 | 00 |
| | | OA2+(2) | X | 11 |
| P3.4/SMCLK | 4 | P3.4 (I/O) | I: 0; O: 1 | 00 |
| | | SMCLK | 1 | 01 |
| | | VSS | 0 | |
| P3.5/OA3O | 5 | P3.5 (I/O) | I: 0; O: 1 | 00 |
| | | OA3O(2) | X | 11 |
| P3.6/OA3- | 6 | P3.6 (I/O) | I: 0; O: 1 | 00 |
| | | OA3-(2) | X | 11 |
| P3.7/OA3+ | 7 | P3.7 (I/O) | I: 0; O: 1 | 00 |
| | | OA3+(2) | X | 11 |

(1) X = don't care
(2) MSP430FR235x devices only


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### 6.11.4 Port P4 Input/Output With Schmitt Trigger

图 6-7 shows the port diagram. 表 6-66 summarizes the selection of the port function.

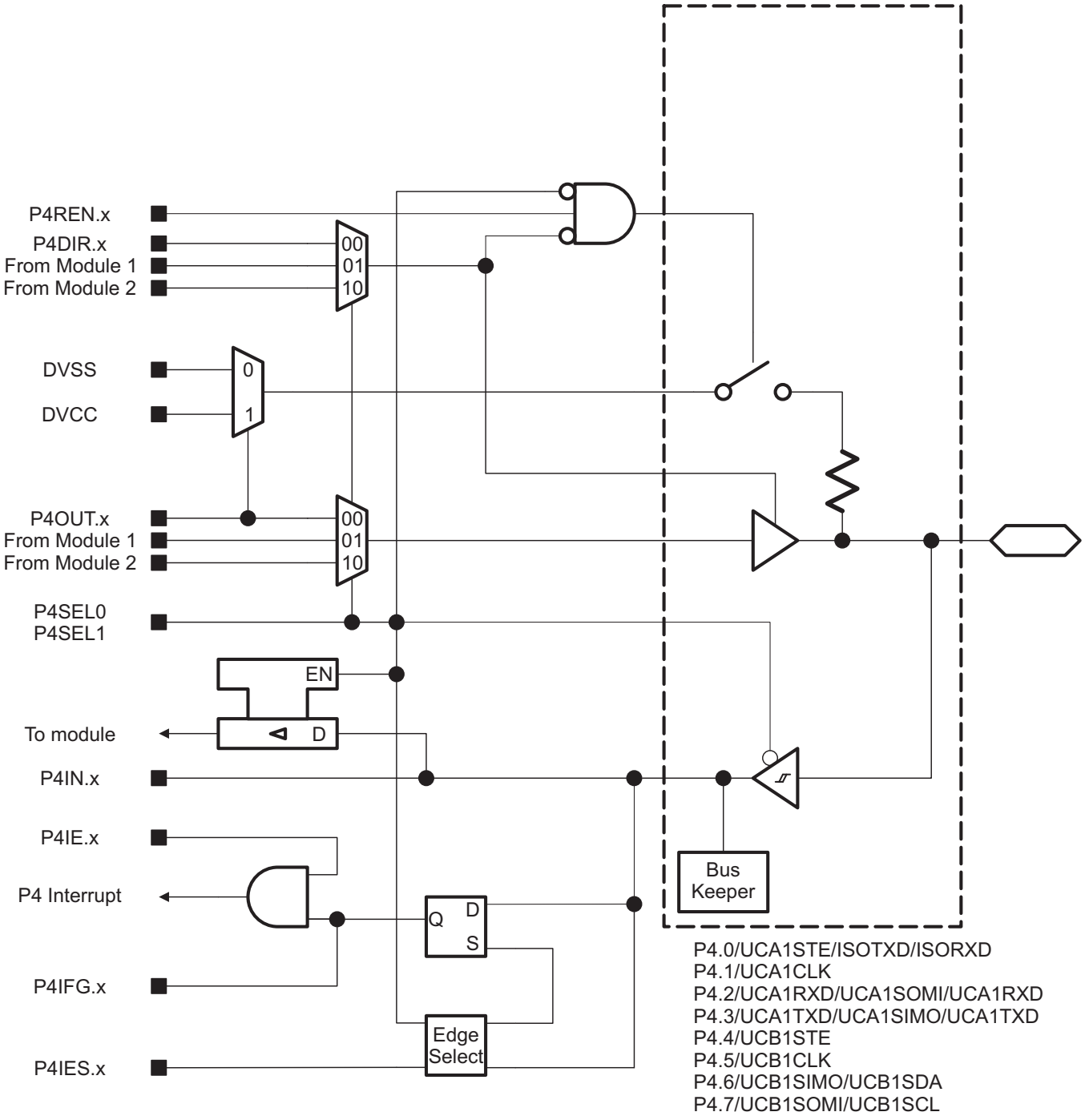



**图 6-7. Port P4 Input/Output With Schmitt Trigger**

表 6-66. Port P4 Pin Functions

| PIN NAME (P4.x) | x | FUNCTION | CONTROL BITS AND SIGNALS(1) | |
|---|---|---|---|---|
| | | | P4DIR.x | P4SELx |
| P4.0/UCA1STE | 0 | P4.0 (I/O) | I: 0; O: 1 | 00 |
| | | UCA1STE | X | 01 |
| | | UCA1RXD, TB3.CCI2B | 0 | 10 |
| | | UCA1TXD logic-AND TB3.2B | 1 | |
| P4.1/UCA1CLK | 1 | P4.1 (I/O) | I: 0; O: 1 | 00 |
| | | UCA1CLK | X | 01 |
| P4.2/UCA1RXD/ UCA1SOMI/$\overline{\text{UCA1RXD}}$ | 2 | P4.2 (I/O) | I: 0; O: 1 | 00 |
| | | UCA1RXD/UCA1SOMI | X | 01 |
| | | $\overline{\text{UCA1RXD}}$ | X | 10 |
| P4.3/UCA1TXD/ UCA1SIMO/$\overline{\text{UCA1TXD}}$ | 3 | P4.3 (I/O) | I: 0; O: 1 | 00 |
| | | UCA1TXD/UCA1SIMO | X | 01 |
| | | $\overline{\text{UCA1TXD}}$ | X | 10 |
| P4.4/UCB1STE | 4 | P4.4 (I/O) | I: 0; O: 1 | 00 |
| | | UCB1STE | X | 01 |
| P4.5/UCB1CLK | 5 | P4.5 (I/O) | I: 0; O: 1 | 00 |
| | | UCB1CLK | X | 01 |
| P4.6/UCB1SIMO/UCB1SDA | 6 | P4.6 (I/O) | I: 0; O: 1 | 00 |
| | | UCB1SIMO/UCB1SDA | X | 01 |
| P4.7/UCB1SOMI/UCB1SCL | 7 | P4.7 (I/O) | I: 0; O: 1 | 00 |
| | | UCB1SOMI/UCB1SCL | X | 01 |

(1) X = don't care


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### 6.11.5 Port P5 Input/Output With Schmitt Trigger

图 6-8 shows the port diagram. 表 6-67 summarizes the selection of the port function.

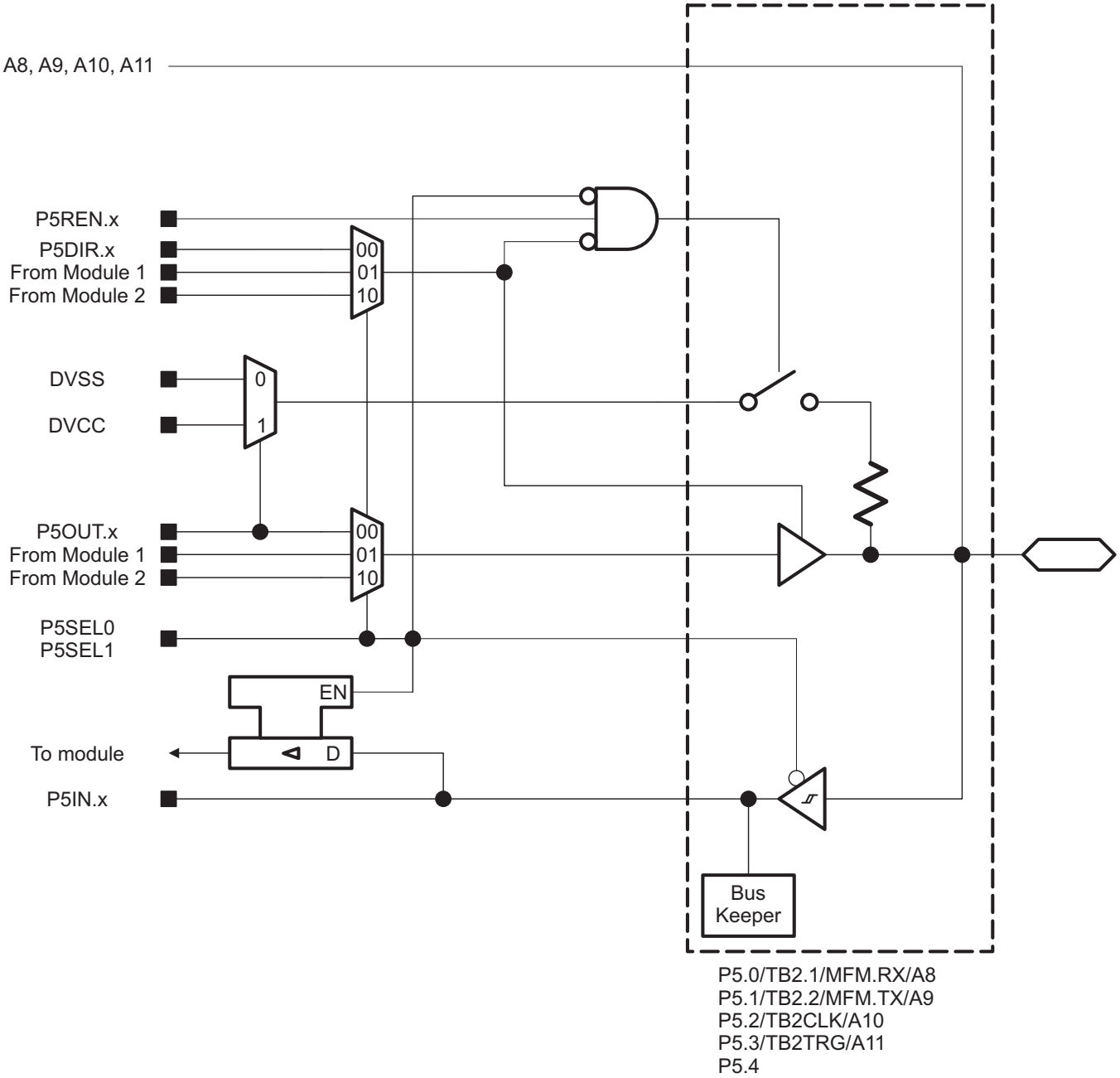



**图 6-8. Port P5 Input/Output With Schmitt Trigger**

表 6-67. Port P5 Pin Functions

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS AND SIGNALS(1) | |
|---|---|---|---|---|
| | | | P5DIR.x | P5SELx |
| P5.0/TB2.1/MFM.RX/A8 | 0 | P5.0 (I/O) | I: 0; O: 1 | 00 |
| | | TB2.CCI1A | I | 01 |
| | | TB2.1 | O | |
| | | MFM.RX | X | 10 |
| | | A8 | X | 11 |
| P5.1/TB2.2/MFM.TX/A9 | 1 | P5.1 (I/O) | I: 0; O: 1 | 00 |
| | | TB2.CCI2A | I | 01 |
| | | TB2.2 | O | |
| | | MFM.TX | X | 10 |
| | | A9 | X | 11 |
| P5.2/TB2CLK/A10 | 2 | P5.2 (I/O) | I: 0; O: 1 | 00 |
| | | TB2CLK | I | 01 |
| | | VSS | O | |
| | | A10 | X | 11 |
| P5.3/TB2TRG/A11 | 3 | P5.3 (I/O) | I: 0; O: 1 | 00 |
| | | TB2TRG | I | 01 |
| | | VSS | O | |
| | | A11 | X | 11 |
| P5.4 | 4 | P5.4 (I/O) | I: 0; O: 1 | 00 |

(1) X = don't care


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### 6.11.6 Port P6 Input/Output With Schmitt Trigger

图 6-9 shows the port diagram. 表 6-68 summarizes the selection of the port function.

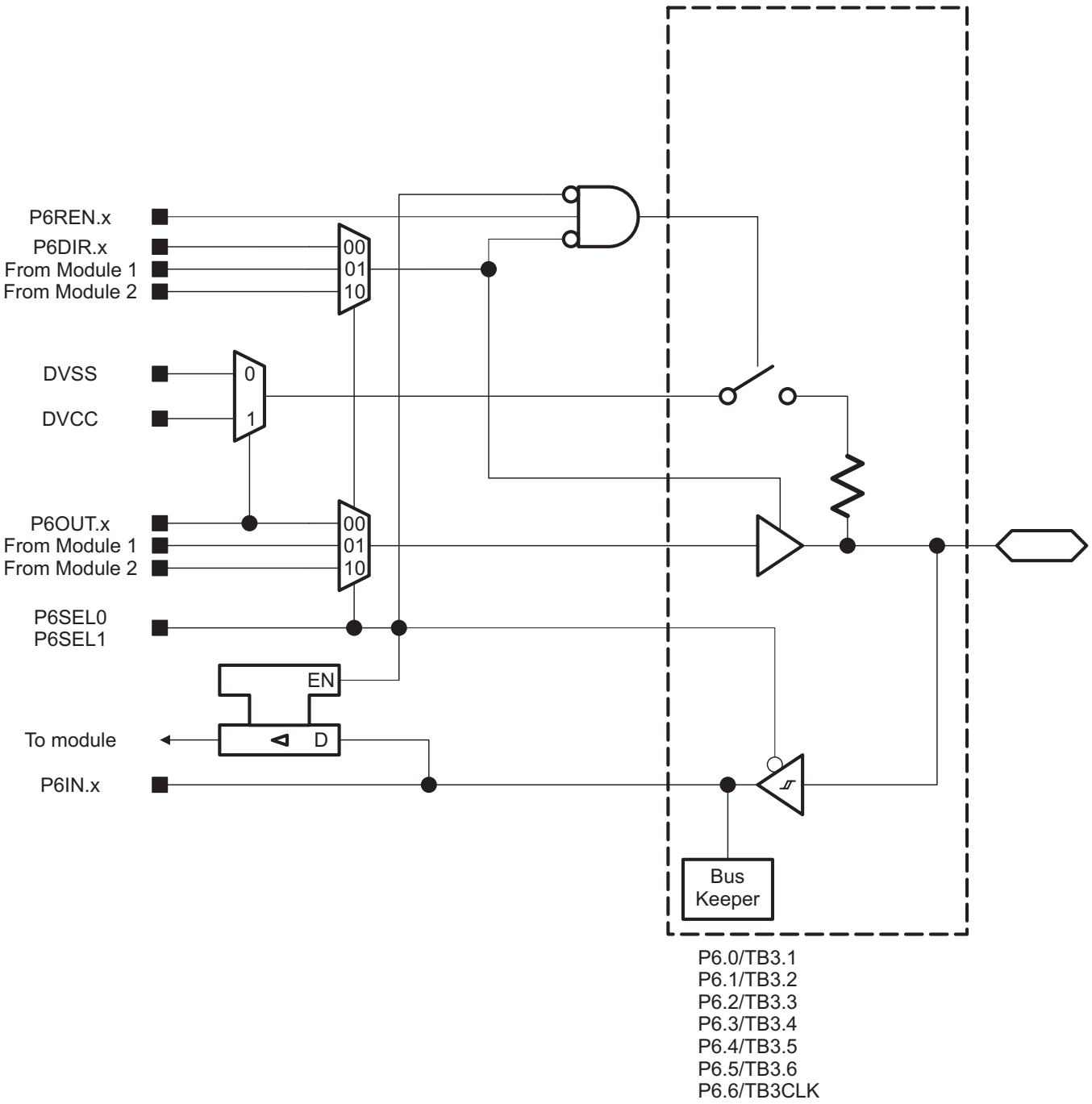



**图 6-9. Port P6 Input/Output With Schmitt Trigger**

表 6-68. Port P6 Pin Functions

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS AND SIGNALS(1) | |
|---|---|---|---|---|
| | | | P6DIR.x | P6SELx |
| P6.0/TB3.1 | 0 | P6.0 (I/O) | I: 0; O: 1 | 00 |
| | | TB3.CCI1A | 0 | 01 |
| | | TB3.1 | 1 | |
| P6.1/TB3.2 | 1 | P6.1 (I/O) | I: 0; O: 1 | 00 |
| | | TB3.CCI2A | 0 | 01 |
| | | TB3.2 | 1 | |
| P6.2/TB3.3 | 2 | P6.2 (I/O) | I: 0; O: 1 | 00 |
| | | TB3.CCI3A | 0 | 01 |
| | | TB3.3 | 1 | |
| P6.3/TB3.4 | 3 | P6.3 (I/O) | I: 0; O: 1 | 00 |
| | | TB3.CCI4A | 0 | 01 |
| | | TB3.4 | 1 | |
| P6.4/TB3.5 | 4 | P6.4 (I/O) | I: 0; O: 1 | 00 |
| | | TB3.CCI5A | 0 | 01 |
| | | TB3.5 | 1 | |
| P6.5/TB3.6 | 5 | P6.5 (I/O) | I: 0; O: 1 | 00 |
| | | TB3.CCI6A | 0 | 01 |
| | | TB3.6 | 1 | |
| P6.6/TB3CLK | 6 | P6.6 (I/O) | I: 0; O: 1 | 00 |
| | | TB3CLK | 0 | 01 |
| | | VSS | 1 | |

(1) X = don't care


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## 6.12 Device Descriptors (TLV)

表 6-69 lists the Device IDs. 表 6-70 lists the contents of the device descriptor tag-length-value (TLV) structure.

**表 6-69. Device IDs**

| DEVICE | DEVICE ID | |
|---|---|---|
| | 1A04h | 1A05h |
| MSP430FR2355 | 0C | 83 |
| MSP430FR2353 | 0D | 83 |
| MSP430FR2155 | 1E | 83 |
| MSP430FR2153 | 1D | 83 |

**表 6-70. Device Descriptors**

| DESCRIPTION | | ADDRESS | VALUE |
|---|---|---|---|
| Information block | Info length | 1A00h | 06h |
| | CRC length | 1A01h | 06h |
| | CRC value(1) | 1A02h | Per unit |
| | | 1A03h | Per unit |
| | Device ID | 1A04h | See (2) |
| | | 1A05h | |
| | Hardware revision | 1A06h | Per unit |
| | Firmware revision | 1A07h | Per unit |
| Die record | Die record tag | 1A08h | 08h |
| | Die record length | 1A09h | 0Ah |
| | Lot wafer ID | 1A0Ah | Per unit |
| | | 1A0Bh | Per unit |
| | | 1A0Ch | Per unit |
| | | 1A0Dh | Per unit |
| | Die X position | 1A0Eh | Per unit |
| | | 1A0Fh | Per unit |
| | Die Y position | 1A10h | Per unit |
| | | 1A11h | Per unit |
| | Test result | 1A12h | Per unit |
| | | 1A13h | Per unit |

(1) CRC value covers the checksum from 0x1A04h to 0x1AF7h by applying CRC-CCITT-16 polynomial of $x^{16} + x^{12} + x^5 + 1$
(2) MSP430FR235x devices only

表 6-70. Device Descriptors (continued)

| DESCRIPTION | | ADDRESS | VALUE |
|---|---|---|---|
| ADC calibration | ADC calibration tag | 1A14h | 11h |
| | ADC calibration length | 1A15h | 10h |
| | ADC gain factor | 1A16h | Per unit |
| | | 1A17h | Per unit |
| | ADC offset | 1A18h | Per unit |
| | | 1A19h | Per unit |
| | ADC internal shared 1.5-V reference, temperature 30°C | 1A1Ah | Per unit |
| | | 1A1Bh | Per unit |
| | ADC internal shared 1.5-V reference, high temperature (3) | 1A1Ch | Per unit |
| | | 1A1Dh | Per unit |
| | ADC internal shared 2.0-V reference, temperature 30°C | 1A1Eh | Per unit |
| | | 1A1Fh | Per unit |
| | ADC internal shared 2.0-V reference, high temperature (3) | 1A20h | Per unit |
| | | 1A21h | Per unit |
| | ADC internal shared 2.5-V reference, temperature 30°C | 1A22h | Per unit |
| | | 1A23h | Per unit |
| | ADC internal shared 2.5-V reference, high temperature (3) | 1A24h | Per unit |
| | | 1A25h | Per unit |
| Reference and DCO calibration | Calibration tag | 1A26h | 12h |
| | Calibration length | 1A27h | 0Ah |
| | Internal shared 1.5-V reference factor | 1A28h | Per unit |
| | | 1A29h | Per unit |
| | Internal shared 2.0-V reference factor | 1A2Ah | Per unit |
| | | 1A2Bh | Per unit |
| | Internal shared 2.5-V reference factor | 1A2Ch | Per unit |
| | | 1A2Dh | Per unit |
| | DCO tap settings for 16 MHz, temperature 30°C | 1A2Eh | Per unit |
| | | 1A2Fh | Per unit |
| | DCO tap settings for 24 MHz, temperature 30°C (4) | 1A30h | Per unit |
| | | 1A31h | Per unit |

(3) The calibration value is device dependent at 105°C.
(4) This value can be directly loaded into the DCO bits in the CSCTL0 register to get an accurate 24-MHz frequency at room temperature, especially when MCU exits from LPM3 and below. TI also suggests to use a predivider to decrease the frequency if the temperature drift might result an overshoot faster than 24 MHz.


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## 6.13 Identification

### 6.13.1 Revision Identification

The device revision information is shown as part of the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to all of the errata sheets for the devices in this data sheet, see 节 8.4.

The hardware revision is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Hardware Revision" entries in 节 6.12.

### 6.13.2 Device Identification

The device type can be identified from the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to all of the errata sheets for the devices in this data sheet, see 节 8.4.

A device identification value is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Device ID" entries in 节 6.12.

### 6.13.3 JTAG Identification

Programming through the JTAG interface, including reading and identifying the JTAG ID, is described in detail in the *MSP430 Programming With the JTAG Interface*.

# 7 Applications, Implementation, and Layout

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their implementation to confirm system functionality.

## 7.1 Device Connection and Layout Fundamentals

This section discusses the recommended guidelines when designing with the MSP430 MCU. These guidelines are to make sure that the device has proper connections for powering, programming, debugging, and optimum analog performance.

### 7.1.1 Power Supply Decoupling and Bulk Capacitors

It is recommended to connect a combination of a 10-µF plus a 100-nF low-ESR ceramic decoupling capacitor to the DVCC pin. Higher-value capacitors can be used but can impact supply rail ramp-up time. Place the decoupling capacitors as close as possible to the pins that they decouple (within a few millimeters).

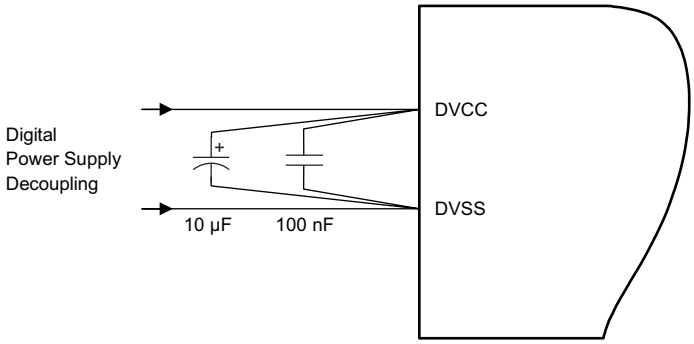



图 7-1. Power Supply Decoupling

### 7.1.2 External Oscillator

Depending on the device variant (see 节 3), the device can support a low-frequency crystal (32 kHz) on the LFXT pins, a high-frequency crystal on the HFXT pins, or both. External bypass capacitors for the crystal oscillator pins are required.

It is also possible to apply digital clock signals to the LFXIN and HFXIN input pins that meet the specifications of the respective oscillator if the appropriate LFXTBYPASS or HFXTBYPASS mode is selected. In this case, the associated LFXOUT and HFXOUT pins can be used for other purposes. If they are left unused, they must be terminated according to 节 4.6.

图 7-2 shows a typical connection diagram.

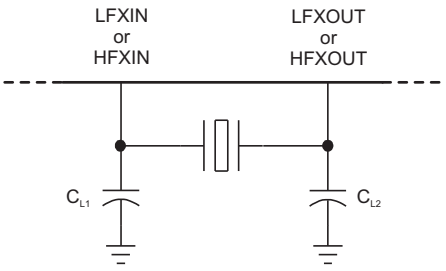



图 7-2. Typical Crystal Connection


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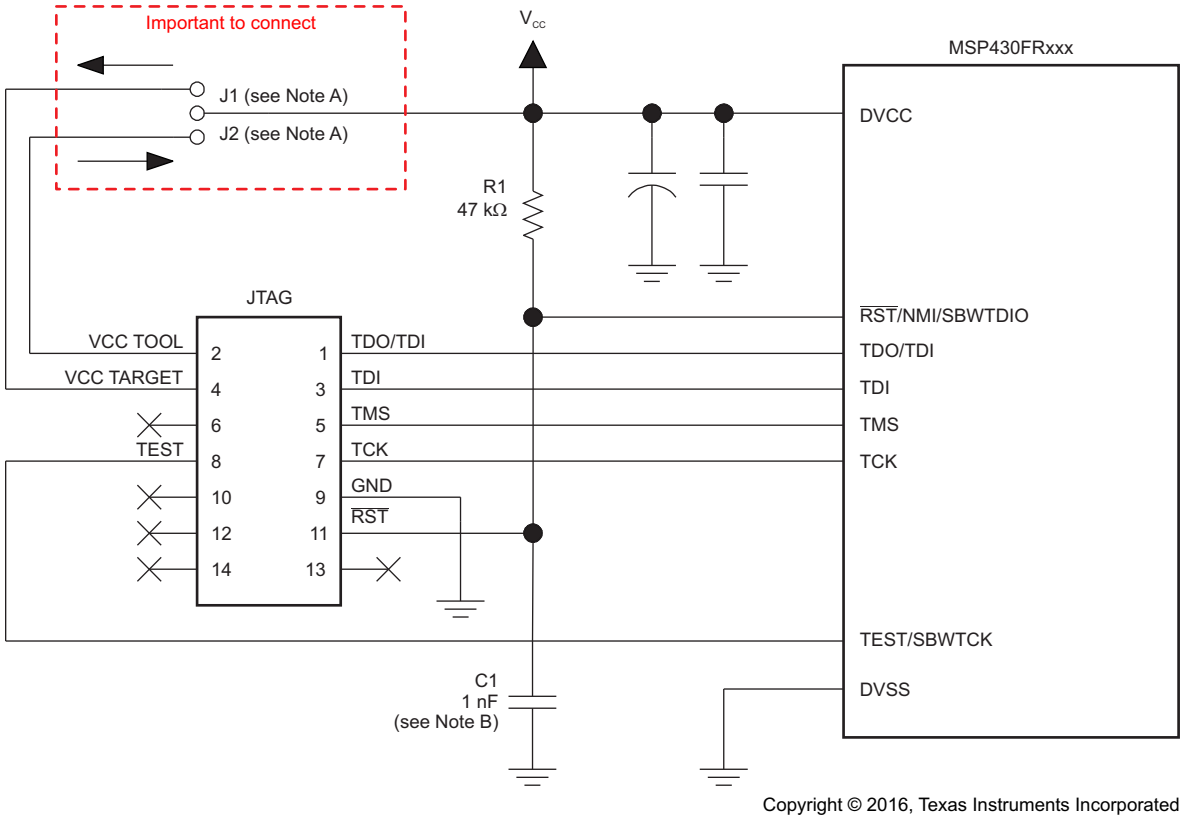
See *MSP430 32-kHz Crystal Oscillators* for more information on selecting, testing, and designing a crystal oscillator with MSP430 MCUs.

### 7.1.3 JTAG

With the proper connections, the debugger and a hardware JTAG interface (such as the MSP-FET or MSP-FET430UIF) can be used to program and debug code on the target board. In addition, the connections also support the MSP-GANG production programmers, thus providing an easy way to program prototype boards, if desired. 图 7-3 shows the connections between the 14-pin JTAG connector and the target device required to support in-system programming and debugging for 4-wire JTAG communication. 图 7-4 shows the connections for 2-wire JTAG mode (Spy-Bi-Wire).

The connections for the MSP-FET and MSP-FET430UIF interface modules and the MSP-GANG are identical. Both can supply $V_{CC}$ to the target board (through pin 2). In addition, the MSP-FET and MSP-FET430UIF interface modules and MSP-GANG have a $V_{CC}$ sense feature that, if used, requires an alternate connection (pin 4 instead of pin 2). The VCC-sense feature senses the local $V_{CC}$ present on the target board (that is, a battery or other local power supply) and adjusts the output signals accordingly. 图 7-3 and 图 7-4 show a jumper block that supports both scenarios of supplying $V_{CC}$ to the target board. If this flexibility is not required, the desired $V_{CC}$ connections can be hard-wired to eliminate the jumper block. Pins 2 and 4 must not be connected at the same time.

For additional design information regarding the JTAG interface, see the MSP430 hardware tools user's guide.

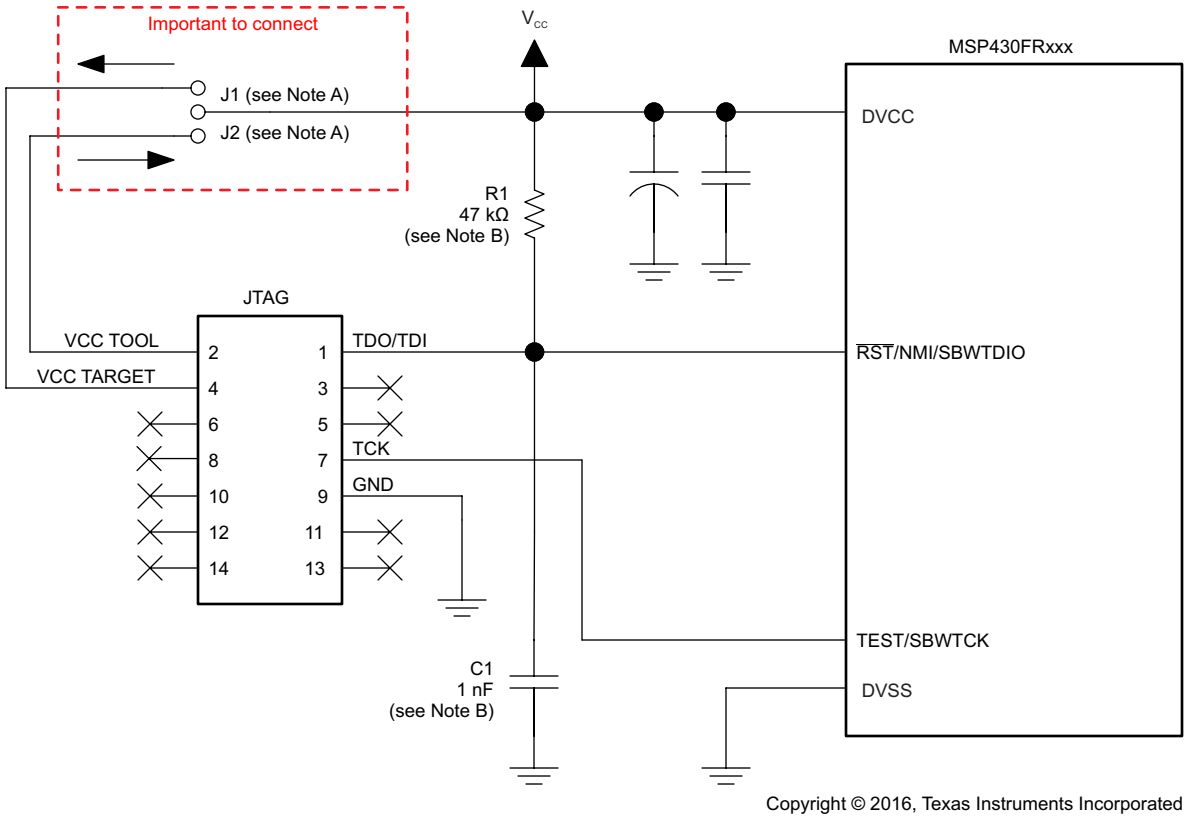



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A. If a local target power supply is used, make connection J1. If power from the debug or programming adapter is used, make connection J2.

B. The upper limit for C1 is 1.1 nF when using current TI tools.

**图 7-3. Signal Connections for 4-Wire JTAG Communication**




A. Make connection J1 if a local target power supply is used, or make connection J2 if the target is powered from the debug or programming adapter.

B. The device $\overline{\text{RST}}$/NMI/SBWTDIO pin is used in 2-wire mode for bidirectional communication with the device during JTAG access, and any capacitance that is attached to this signal can affect the ability to establish a connection with the device. The upper limit for C1 is 1.1 nF when using current TI tools.

**图 7-4. Signal Connections for 2-Wire JTAG Communication (Spy-Bi-Wire)**

### 7.1.4 Reset

The reset pin can be configured as a reset function (default) or as an NMI function in the special function register (SFR), SFRRPCR.

In reset mode, the $\overline{\text{RST}}$/NMI pin is active low, and a pulse applied to this pin that meets the reset timing specifications generates a BOR-type device reset.

Setting SYSNMI causes the $\overline{\text{RST}}$/NMI pin to be configured as an external NMI source. The external NMI is edge sensitive, and its edge is selectable by SYSNMIIES. Setting the NMIIE enables the interrupt of the external NMI. When an external NMI event occurs, the NMIIFG is set.

The $\overline{\text{RST}}$/NMI pin can have either a pullup or pulldown that is enabled or not. SYSRSTUP selects either pullup or pulldown, and SYSRSTRE causes the pullup (default) or pulldown to be enabled (default) or not. If the $\overline{\text{RST}}$/NMI pin is unused, it is required either to select and enable the internal pullup or to connect an external 47-kΩ pullup resistor to the $\overline{\text{RST}}$/NMI pin with a 2.2-nF pulldown capacitor. The pulldown capacitor should not exceed 1.1 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers.

See the *MSP430FR4xx and MSP430FR2xx Family User's Guide* for more information on the referenced control registers and bits.

### 7.1.5 Unused Pins

For details on the connection of unused pins, see节 4.6.


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### 7.1.6 General Layout Recommendations

- Proper grounding and short traces for external crystal to reduce parasitic capacitance. See *MSP430 32-kHz Crystal Oscillators* for recommended layout guidelines.
- Proper bypass capacitors on DVCC, AVCC, and reference pins if used.
- Avoid routing any high-frequency signal close to an analog signal line. For example, keep digital switching signals such as PWM or JTAG signals away from the oscillator circuit and ADC signals.
- Proper ESD level protection should be considered to protect the device from unintended high-voltage electrostatic discharge. See *MSP430 System-Level ESD Considerations* for guidelines.

### 7.1.7 Do's and Don'ts

During power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in the Absolute Maximum Ratings section. Exceeding the specified limits can cause malfunction of the device including erroneous writes to RAM and FRAM.

## 7.2 Peripheral- and Interface-Specific Design Information

### 7.2.1 ADC Peripheral

#### 7.2.1.1 Partial Schematic

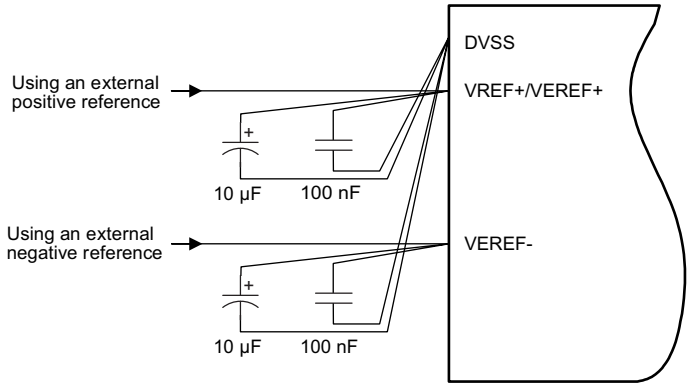



图 7-5. ADC Grounding and Noise Considerations

#### 7.2.1.2 Design Requirements

As with any high-resolution ADC, appropriate printed-circuit-board layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. This current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. The general guidelines in 节 7.1.1 combined with the connections shown in 图 7-5 prevent these offset voltages.

In addition to grounding, ripple and noise spikes on the power-supply lines that are caused by digital switching or switching power supplies can corrupt the conversion result. TI recommends a noise-free design using separate analog and digital ground planes with a single-point connection to achieve high accuracy.

图 7-5 shows the recommended decoupling circuit when an external voltage reference is used. The internal reference module has a maximum drive current as described in the sections *ADC Pin Enable* and *1.2-V Reference Settings* of the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

The reference voltage must be a stable voltage for accurate measurements. The capacitor values that are selected in the general guidelines filter out the high- and low-frequency ripple before the reference voltage enters the device. In this case, the 10-µF capacitor buffers the reference pin and filters low-frequency ripple, and the 100-nF bypass capacitor filters high-frequency noise.

#### 7.2.1.3 Layout Guidelines

Components that are shown in the partial schematic (see 图 7-5) should be placed as close as possible to the respective device pins to avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal.

Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal.

## 7.3 ROM Libraries

The MSP430FR235x and MSP430FR215x devices in the MSP430FR4xx family have MSP430 Driver Library and FFT Library in ROM.

MSP430 software libraries in ROM are tested to work with both Code Composer Studio and IAR Embedded Workbench toolchains.

- For the ROM image to be compatible between CCS and IAR tool chains, there are certain project properties restrictions. See the TI.com attribute guide for more details.
- To use DriverLib in ROM, #include "rom_driverlib.h". Header file checks continue to provide helpful hints at build time until the user application adheres to __cc_rom.
- To use FFTLib in ROM, #include "DSPLib.h". FFTLib is a subset of the MSP software library DSPLib.
- For more information, see the MSP430 Driver Library for MSP430FR2xx_4xx ROM README and MSP DSP Library ROM README in MSP430Ware. The library ROM image is located above the 64KB memory address. Application code using ROM must be large code model (20-bit address pointer rather than 16-bit address pointer).

Benefits of ROM library use include:

- Code execution at clock speeds that exceed 8 MHz is faster from ROM than from FRAM, because the code avoids FRAM wait states (except FRAM controller cache hits). Without FRAM wait states, code execution performance is limited by only the processor clock, which is generally faster than other subsystems. Executing code from RAM gives comparable performance, but the available RAM size is typically more limited.
- More nonvolatile storage (FRAM) available in the device is left for application code.

## 7.4 Typical Applications

表 7-1 lists TI reference designs that use the MSP430FR235x devices in real-world application scenarios. Consult these designs for additional guidance regarding schematic, layout, and software implementation. For the most up-to-date list of available TI reference designs, visit the TI reference designs library.

**表 7-1. Tools and Reference Designs**

| DESIGN NAME | LINK |
|---|---|
| 4- to 20-mA Loop-Powered RTD Temperature Transmitter Reference Design With MSP430 Smart Analog Combo | TIDM-01000 |
| MSP430FR2355 LaunchPad development kit | MSP-EXP430FR2355 |


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# 8 器件和文档支持

## 8.1 使用入门

有关 MSP430™ 系列器件以及开发协助工具和库的更多信息，请访问 MSP430 超低功耗传感和测量 MCU 概述。

## 8.2 器件命名规则

为了标示产品开发周期所处的阶段，TI 为所有 MSP MCU 器件的部件号分配了前缀。每个 MSP MCU 商用系列产品成员都具有以下两个前缀之一：MSP 或 XMS。这些前缀代表了产品开发的发展阶段，即从工程原型 (XMS) 直到完全合格的生产器件 (MSP)。

**XMS** - 实验器件，不一定代表最终器件的电气规格

**MSP** - 完全合格的生产器件

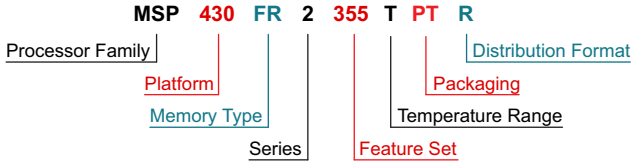
XMS 器件在供货时附带如下免责声明：

“开发中的产品用于内部评估用途。”

MSP 器件的特性已经全部明确，并且器件的质量和可靠性已经完全论证。TI 的标准保修证书对该器件适用。

预测显示原型器件 (XMS) 的故障率大于标准生产器件。由于这些器件的预计最终使用故障率尚不确定，德州仪器 (TI) 建议不要将它们用于任何生产系统。请仅使用合格的生产器件。

TI 器件的命名规则还包括一个带有器件系列名称的后缀。此后缀表示温度范围、封装类型和配送形式。图 8-1 提供了解读完整器件名称的图例。




| | | |
|---|---|---|
| Processor Family | MSP = Mixed-Signal Processor<br>XMS = Experimental Silicon | |
| Platform | 430 = MSP430 16-Bit Low-Power Microcontroller | |
| Memory Type | FR = FRAM | |
| Series | 2 = FRAM 2 Series, up to 24 MHz without LCD | |
| Feature Set | **First and Second Digits:**<br>SAC Level / ADC Channels / COMP / 16-bit Timers / I/Os<br>35 = SAC-L3 / Up to 12 / 2 / 4 / Up to 44<br>15 = No SAC / Up to 12 / 2 / 4 / Up to 44 | **Third Digit:**<br>FRAM (KB) / SRAM (KB)<br>5 = 32 / 4<br>3 = 16 / 2 |
| Temperature Range | T = –40°C to 105°C | |
| Packaging | http://www.ti.com/packaging | |
| Distribution Format | T = Small reel<br>R = Large reel<br>No marking = Tube or tray | |

图 **8-1.** 器件命名规则

## 8.3 工具和软件

请参阅《*适用于 MSP430™ MCU 的 Code Composer Studio™ IDE 用户指南*》，以了解有关可用 功能）的详细信息。

表 8-1 列出了 MSP430FR235x 和 MSP430FR215x 微控制器所 支持的 调试特性。

**表 8-1. 硬件 特性**

| MSP430 架构 | 四线制 JTAG | 两线制 JTAG | 断点 (N) | 范围断点 | 时钟控制 | 状态序列发生器 | 跟踪缓冲器 | LPMx.5 调试支持 | EEM 版本 |
|---|---|---|---|---|---|---|---|---|---|
| MSP430Xv2 | 有 | 有 | 3 | 有 | 是 | 否 | 否 | 否 | S |

设计套件与评估模块

MSP430FR2355 LaunchPad 开发套件

MSP-EXP430FR2355 LaunchPad 开发套件是一个易于使用的评估模块 (EVM)，该模块包含了在超低功耗 MSP430FR215x 和 MSP430FR235x FRAM 微控制器系列上开始进行开发所需要的所有资源，包括用于编程、调试和能量测量的板载调试探针。

MSP-TS430PT48 目标开发板

MSP-TS430PT48 目标开发板是一款 48 引脚 ZIF 插座目标板，用于通过 JTAG 接口或 Spy-Bi-Wire（双线制 JTAG）协议对 MSP430 MCU 进行系统内编程和调试。

软件

MSP430Ware™ 软件

MSP430Ware 软件集合了所有 MSP430 器件的代码示例、数据表以及其他设计资源，打包提供给用户。除了提供已有 MSP430 设计资源的完整集合外，MSP430Ware 软件还包含名为 MSP 驱动程序库的高级 API。借助该库可以轻松地对 MSP430 硬件进行编程。MSP430Ware 软件以 CCS 组件或独立软件包两种形式提供。

MSP430FR235x 和 MSP430FR215x 代码示例

根据不同应用需求配置各集成外设的每个 MSP 器件均具备相应的 C 代码示例。

MSP 驱动程序库

MSP 驱动程序库的抽象 API 提供易用的函数调用，无需直接操纵 MSP430 硬件的位与字节。完整的文档通过具有帮助意义的 API 指南交付，其中包括有关每个函数调用和经过验证的参数的详细信息。开发人员可以使用驱动程序库功能，以最低开销编写完整项目。

MSP EnergyTrace™ 技术

适用于 MSP430 微控制器的 EnergyTrace 技术是基于电能的代码分析工具，适用于测量和显示应用的电能系统配置并帮助优化应用以实现超低功耗。

ULP（超低功耗）Advisor

ULP Advisor™软件是一款辅助工具，旨在指导开发人员编写更为高效的代码，从而充分利用 MSP430 和 MSP432 微控制器 独特 的超低 功耗™特性。ULP Advisor 的目标人群是微控制器的资深开发者和开发新手，可以根据详尽的 ULP 检验表检查代码，以便最大限度地减少应用程序的能耗。在编译时，ULP Advisor 会提供通知和备注以突出显示代码中可以进一步优化的区域，进而实现更低功耗。

适用于 MSP 超低功耗微控制器的 FRAM 嵌入式软件实用程序

FRAM 实用程序旨在作为不断扩充的嵌入式软件实用程序集合，其中的实用程序充分利用 FRAM 的超低功耗和近乎无限次的写入寿命。这些实用程序适用于 MSP430FRxx FRAM 微控制器并提供示例代码协助应用程序开发。其中的实用程序包含功耗计算实用程序 (CTPL)。CTPL 是一套实用程序 API 集，通过 CTPL 能够轻松使用 LPMx.5 低功耗模式以及强大的关断模式，允许应用程序在检测到功率损耗时节约能耗并恢复关键的系统元件。

IEC60730 软件包


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IEC60730 MSP430 软件包经过专门开发，用于协助客户达到 IEC 60730-1:2010（家用及类似用途的自动化电气控制 - 第 1 部分：一般要求）B 类产品的要求。其中涵盖家用电器、电弧检测器、电源转换器、电动工具、电动自行车及其他诸多产品。IEC60730 MSP430 软件包可以嵌入在 MSP430 MCU 中 运行的客户应用， 从而帮助客户简化其消费类器件在功能安全方面遵循 IEC 60730-1:2010 B 类规范的认证工作。

### 适用于 MSP 的定点数学库

MSP IQmath 和 Qmath 库是为 C 语言开发者提供的一套经过高度优化的高精度数学运算函数集合，能够将浮点算法无缝嵌入 MSP430 和 MSP432 器件的定点代码中。这些例程通常用于计算密集型实时 应用， 而优化的执行速度、高精度以及超低能耗通常是影响这些实时应用的关键因素。与使用浮点数学算法编写的同等代码相比，使用 IQmath 和 Qmath 库可以大幅提高执行速度并显著降低能耗。

### 适用于 MSP430 的浮点数学库

TI 在低功耗和低成本微控制器领域锐意创新，为您提供 MSPMATHLIB。此标量函数的浮点数学库，能够充分利用器件的智能外设，使速度最高达到标准 MSP430 数学函数的 26 倍。Mathlib 能够轻松集成到您的设计中。该运算库免费使用并集成在 Code Composer Studio IDE 和 IAR Embedded Workbench IDE 中。

## 开发工具

### 适用于 MSP 微控制器的 Code Composer Studio™ 集成开发环境

Code Composer Studio (CCS) 集成开发环境 (IDE) 支持所有 MSP 微控制器器件。CCS 包含一整套用于开发和调试嵌入式 应用的工具。它包含了优化的 C/C++ 编译器、源代码编辑器、项目构建环境、调试器、描述器以及其他多种 功能。

### IAR Embedded Workbench® IDE

适用于 MSP430 MCU 的 IAR Embedded Workbench IDE 是一套用于构建和调试基于 MSP430 微控制器的嵌入式 应用 的完整 C/C++ 编译器工具链。该调试器可用于源代码和反汇编代码，而且支持复杂代码和数据断点。它还提供了硬件仿真器，可在未连接实际目标的情况下进行调试。

### Uniflash 独立闪存工具

UniFlash 独立闪存工具用于在 TI MCU 上对片上闪存进行编程。Uniflash 具有 GUI、命令行和脚本界面。Uniflash 软件工具支持两种使用方式：TI 云工具或者从 TI 网页下载的桌面应用。

### MSP MCU 编程器和调试器

MSP-FET 是一款强大的仿真开发工具（通常称为调试探针），可帮助用户在 MSP 低功耗微控制器 (MCU) 中快速开发应用。创建 MCU 软件通常需要将生成的二进制程序下载到 MSP 器件中，从而进行验证和调试。

### MSP-GANG 生产编程器

MSP Gang 编程器是一款 MSP430 或 MSP432 器件编程器，可同时对多达八个完全相同的 MSP430 或 MSP432 闪存或 FRAM 器件进行编程。MSP Gang 编程器可使用标准的 RS-232 或 USB 连接与主机 PC 相连并提供灵活的编程选项，允许用户完全自定义流程。

### TIREX Resource Explorer (TIRex)

用于查找器件和开发板的示例、库、可执行代码和文档的在线门户。您可以直接在 Code Composer Studio IDE 内访问 TIRex，也可以在“TI 云工具”中访问 TIRex。

### TI 云工具

快速在 dev.ti.com 上开始开发。首先使用 Resource Explorer 界面快速找到您需要的所有文件。然后使用行业领先的 Code Composer Studio Cloud IDE 在云中编辑、生成和调试嵌入式 应用 。

### GCC - 适用于 MSP 的编译器

MSP430 和 MSP432 GCC 开源包是一个完整的调试器和开源 C/C++ 编译器工具链，用于基于 MSP430 和 MSP432 微控制器构建和调试嵌入式 应用 。这些免费的 GCC 编译器支持所有 MSP430 和 MSP432 器件且没有代码大小限制。此外，这些编译器可以通过命令行独立使用，也可在 Code Composer Studio v6.0 或更高版本中使用。不管您使用的是 Windows®、 Linux® 还是 macOS®环境，马上开始吧。

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## 8.4 文档支持

以下文档介绍了 MSP430FR235x 和 MSP430FR215x 微控制器。

### 接收文档更新通知

要接收文档更新通知（包括芯片勘误表），请转至 ti.com.cn 上您的器件对应的产品文件夹（关于产品文件夹的链接，请参见节 8.5）。请单击右上角的“通知我”按钮。点击注册后，即可收到产品信息更改每周摘要（如有）。有关更改的详细信息，请查看任意修订文档的修订历史记录。

### 勘误表

《MSP430FR2355 器件勘误表》

介绍了这款器件所有芯片修订版本的功能规格的已知例外情况。

《MSP430FR2353 器件勘误表》

介绍了这款器件所有芯片修订版本的功能规格的已知例外情况。

《MSP430FR2155 器件勘误表》

介绍了这款器件所有芯片修订版本的功能规格的已知例外情况。

《MSP430FR2153 器件勘误表》

介绍了这款器件所有芯片修订版本的功能规格的已知例外情况。

### 用户指南

《MSP430FR4xx 和 MSP430FR2xx 系列用户指南》

详细 说明 了该器件系列提供的所有模块和外设。

《MSP430 FRAM 器件引导加载程序 (BSL)》用户指南

MSP430 MCU 上的引导加载程序 (BSL) 允许用户在原型设计、投产和维护等各阶段与 MSP430 MCU 中的嵌入式存储器进行通信。可编程存储器（FRAM 存储器）和数据存储器 (RAM) 均可按要求予以修改。

《通过 JTAG 接口对 MSP430 进行编程》

此文档介绍了使用 JTAG 通信端口擦除、编程和验证基于 MSP430 闪存和 FRAM 的微控制器系列的存储器模块所需的功能。此外，该文档还介绍了如何编程所有 MSP430 器件上均具备的 JTAG 访问安全保险丝。此文档介绍了使用标准四线制 JTAG 接口和两线制 JTAG 接口（也称为 Spy-Bi-Wire (SBW)）的器件访问。

《MSP430 硬件工具用户指南》

此手册介绍了 TI MSP-FET430 闪存仿真工具 (FET) 的硬件。FET 是针对 MSP430 超低功耗微控制器的程序开发工具。文中对提供的接口类型，即并行端口接口和 USB 接口进行了说明。

### 应用报告

《MSP430 32kHz 晶体振荡器》

选择合适的晶体、正确的负载电路和适当的电路板布局是实现稳定的晶体振荡器的关键。该应用报告总结了晶体振荡器的功能，介绍了用于选择合适的晶体以实现 MSP430 超低功耗运行的参数。此外，还给出了正确电路板布局的提示和示例。此外，为了确保振荡器在大规模生产后能够稳定运行，还可能需要进行一些振荡器测试，该文档中提供了有关这些测试的详细信息。

《MSP430 系统级 ESD 注意事项》

随着芯片技术向更低电压方向发展以及设计具有成本效益的超低功耗组件的需求的出现，系统级 ESD 要求变得越来越苛刻。该应用报告介绍了不同的 ESD 主题，旨在帮助电路板设计人员和 OEM 理解并设计出稳健耐用的系统级设计。

## 8.5 相关链接

表 8-2 列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。


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表 **8-2.** 相关链接

| 器件 | 产品文件夹 | 立即订购 | 技术文档 | 工具和软件 | 支持和社区 |
|---|---|---|---|---|---|
| MSP430FR2355 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430FR2353 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430FR2155 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430FR2153 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |

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## 8.6 商标

LaunchPad, MSP430, MSP430Ware, Code Composer Studio, E2E, EnergyTrace, ULP Advisor, 功耗, 适用于 MSP 微控制器的 Code Composer Studio are trademarks of Texas Instruments.
macOS is a registered trademark of Apple, Inc.
IAR Embedded Workbench is a registered trademark of IAR Systems.
Linux is a registered trademark of Linus Torvalds.
Windows is a registered trademark of Microsoft Corporation.

## 8.7 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 8.8 Glossary

**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.


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# 9 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430FR2153TDBT | ACTIVE | TSSOP | DBT | 38 | 50 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | 430FR2153 | Samples |
| MSP430FR2153TDBTR | ACTIVE | TSSOP | DBT | 38 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | 430FR2153 | Samples |
| MSP430FR2153TPT | ACTIVE | LQFP | PT | 48 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 105 | 430FR2153 | Samples |
| MSP430FR2153TPTR | ACTIVE | LQFP | PT | 48 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 105 | 430FR2153 | Samples |
| MSP430FR2153TRHAR | ACTIVE | VQFN | RHA | 40 | 2500 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 105 | FR2153 | Samples |
| MSP430FR2153TRHAT | ACTIVE | VQFN | RHA | 40 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 105 | FR2153 | Samples |
| MSP430FR2153TRSMR | ACTIVE | VQFN | RSM | 32 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | FR2153 | Samples |
| MSP430FR2153TRSMT | ACTIVE | VQFN | RSM | 32 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | FR2153 | Samples |
| MSP430FR2155TDBT | ACTIVE | TSSOP | DBT | 38 | 50 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | 430FR2155 | Samples |
| MSP430FR2155TDBTR | ACTIVE | TSSOP | DBT | 38 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | 430FR2155 | Samples |
| MSP430FR2155TPT | ACTIVE | LQFP | PT | 48 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 105 | 430FR2155 | Samples |
| MSP430FR2155TPTR | ACTIVE | LQFP | PT | 48 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 105 | 430FR2155 | Samples |
| MSP430FR2155TRHAR | ACTIVE | VQFN | RHA | 40 | 2500 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 105 | FR2155 | Samples |
| MSP430FR2155TRHAT | ACTIVE | VQFN | RHA | 40 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 105 | FR2155 | Samples |
| MSP430FR2155TRSMR | ACTIVE | VQFN | RSM | 32 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | FR2155 | Samples |
| MSP430FR2155TRSMT | ACTIVE | VQFN | RSM | 32 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | FR2155 | Samples |
| MSP430FR2353TDBT | ACTIVE | TSSOP | DBT | 38 | 50 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | 430FR2353 | Samples |
| MSP430FR2353TDBTR | ACTIVE | TSSOP | DBT | 38 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | 430FR2353 | Samples |
| MSP430FR2353TPT | ACTIVE | LQFP | PT | 48 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 105 | 430FR2353 | Samples |
| MSP430FR2353TPTR | ACTIVE | LQFP | PT | 48 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 105 | 430FR2353 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430FR2353TRHAR | ACTIVE | VQFN | RHA | 40 | 2500 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 105 | FR2353 | Samples |
| MSP430FR2353TRHAT | ACTIVE | VQFN | RHA | 40 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 105 | FR2353 | Samples |
| MSP430FR2353TRSMR | ACTIVE | VQFN | RSM | 32 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | FR2353 | Samples |
| MSP430FR2353TRSMT | ACTIVE | VQFN | RSM | 32 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | FR2353 | Samples |
| MSP430FR2355TDBT | ACTIVE | TSSOP | DBT | 38 | 50 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | 430FR2355 | Samples |
| MSP430FR2355TDBTR | ACTIVE | TSSOP | DBT | 38 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | 430FR2355 | Samples |
| MSP430FR2355TPT | ACTIVE | LQFP | PT | 48 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 105 | 430FR2355 | Samples |
| MSP430FR2355TPTR | ACTIVE | LQFP | PT | 48 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 105 | 430FR2355 | Samples |
| MSP430FR2355TRHAR | ACTIVE | VQFN | RHA | 40 | 2500 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 105 | FR2355 | Samples |
| MSP430FR2355TRHAT | ACTIVE | VQFN | RHA | 40 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 105 | FR2355 | Samples |
| MSP430FR2355TRSMR | ACTIVE | VQFN | RSM | 32 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | FR2355 | Samples |
| MSP430FR2355TRSMT | ACTIVE | VQFN | RSM | 32 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | FR2355 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

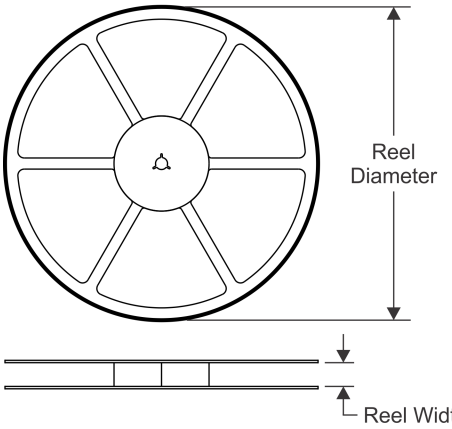
**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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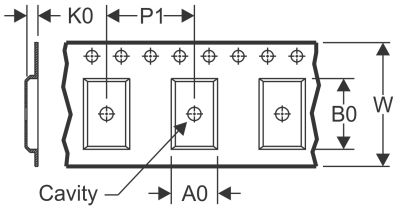
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

REEL DIMENSIONS

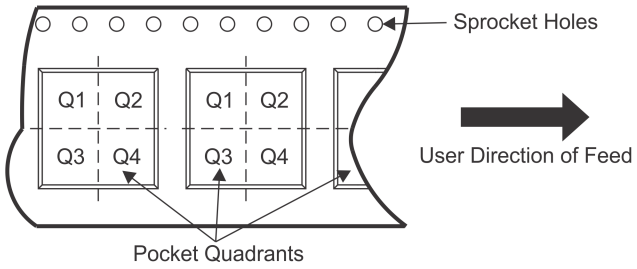



TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

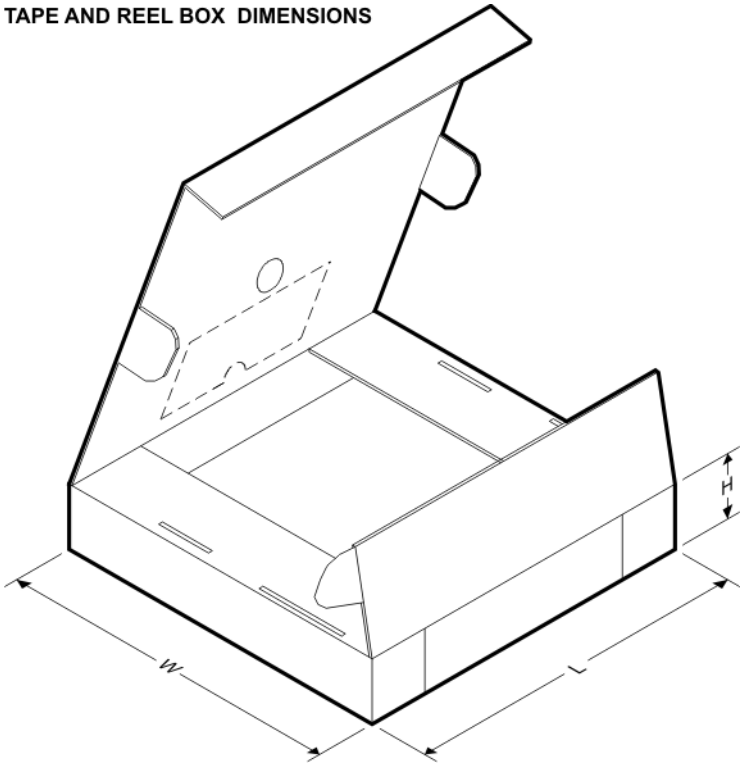



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430FR2153TDBTR | TSSOP | DBT | 38 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| MSP430FR2153TPTR | LQFP | PT | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.9 | 12.0 | 16.0 | Q2 |
| MSP430FR2153TRHAR | VQFN | RHA | 40 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSP430FR2153TRHAT | VQFN | RHA | 40 | 250 | 180.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSP430FR2153TRSMR | VQFN | RSM | 32 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430FR2153TRSMT | VQFN | RSM | 32 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430FR2155TDBTR | TSSOP | DBT | 38 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| MSP430FR2155TPTR | LQFP | PT | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.9 | 12.0 | 16.0 | Q2 |
| MSP430FR2155TRHAR | VQFN | RHA | 40 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSP430FR2155TRHAT | VQFN | RHA | 40 | 250 | 180.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSP430FR2155TRSMR | VQFN | RSM | 32 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430FR2155TRSMT | VQFN | RSM | 32 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430FR2353TDBTR | TSSOP | DBT | 38 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| MSP430FR2353TPTR | LQFP | PT | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.9 | 12.0 | 16.0 | Q2 |
| MSP430FR2353TRHAR | VQFN | RHA | 40 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSP430FR2353TRHAT | VQFN | RHA | 40 | 250 | 180.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSP430FR2353TRSMR | VQFN | RSM | 32 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430FR2353TRSMT | VQFN | RSM | 32 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430FR2355TDBTR | TSSOP | DBT | 38 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| MSP430FR2355TPTR | LQFP | PT | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.9 | 12.0 | 16.0 | Q2 |
| MSP430FR2355TRHAR | VQFN | RHA | 40 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSP430FR2355TRHAT | VQFN | RHA | 40 | 250 | 180.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSP430FR2355TRSMR | VQFN | RSM | 32 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430FR2355TRSMT | VQFN | RSM | 32 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |

**TAPE AND REEL BOX DIMENSIONS**

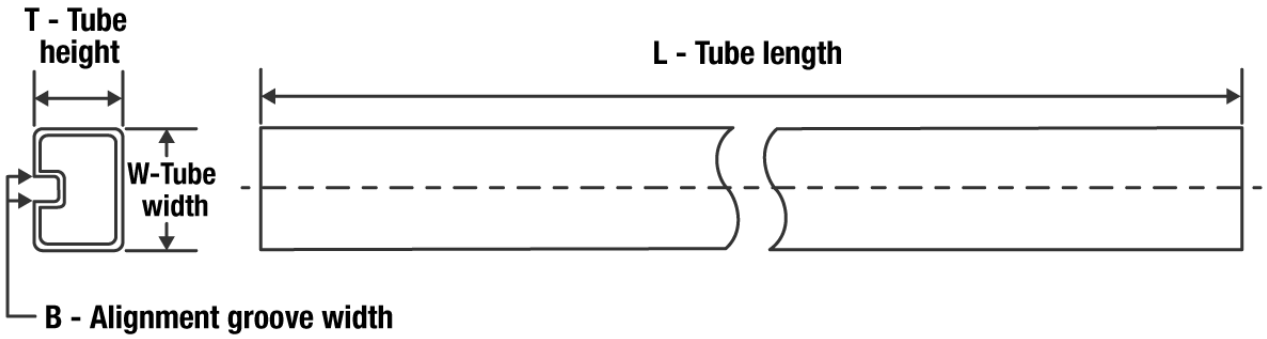



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| MSP430FR2153TDBTR | TSSOP | DBT | 38 | 2000 | 350.0 | 350.0 | 43.0 |
| MSP430FR2153TPTR | LQFP | PT | 48 | 1000 | 336.6 | 336.6 | 31.8 |
| MSP430FR2153TRHAR | VQFN | RHA | 40 | 2500 | 367.0 | 367.0 | 35.0 |
| MSP430FR2153TRHAT | VQFN | RHA | 40 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430FR2153TRSMR | VQFN | RSM | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| MSP430FR2153TRSMT | VQFN | RSM | 32 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430FR2155TDBTR | TSSOP | DBT | 38 | 2000 | 350.0 | 350.0 | 43.0 |
| MSP430FR2155TPTR | LQFP | PT | 48 | 1000 | 336.6 | 336.6 | 31.8 |
| MSP430FR2155TRHAR | VQFN | RHA | 40 | 2500 | 367.0 | 367.0 | 35.0 |
| MSP430FR2155TRHAT | VQFN | RHA | 40 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430FR2155TRSMR | VQFN | RSM | 32 | 3000 | 367.0 | 367.0 | 35.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| MSP430FR2155TRSMT | VQFN | RSM | 32 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430FR2353TDBTR | TSSOP | DBT | 38 | 2000 | 350.0 | 350.0 | 43.0 |
| MSP430FR2353TPTR | LQFP | PT | 48 | 1000 | 336.6 | 336.6 | 31.8 |
| MSP430FR2353TRHAR | VQFN | RHA | 40 | 2500 | 367.0 | 367.0 | 35.0 |
| MSP430FR2353TRHAT | VQFN | RHA | 40 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430FR2353TRSMR | VQFN | RSM | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| MSP430FR2353TRSMT | VQFN | RSM | 32 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430FR2355TDBTR | TSSOP | DBT | 38 | 2000 | 350.0 | 350.0 | 43.0 |
| MSP430FR2355TPTR | LQFP | PT | 48 | 1000 | 336.6 | 336.6 | 31.8 |
| MSP430FR2355TRHAR | VQFN | RHA | 40 | 2500 | 367.0 | 367.0 | 35.0 |
| MSP430FR2355TRHAT | VQFN | RHA | 40 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430FR2355TRSMR | VQFN | RSM | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| MSP430FR2355TRSMT | VQFN | RSM | 32 | 250 | 210.0 | 185.0 | 35.0 |

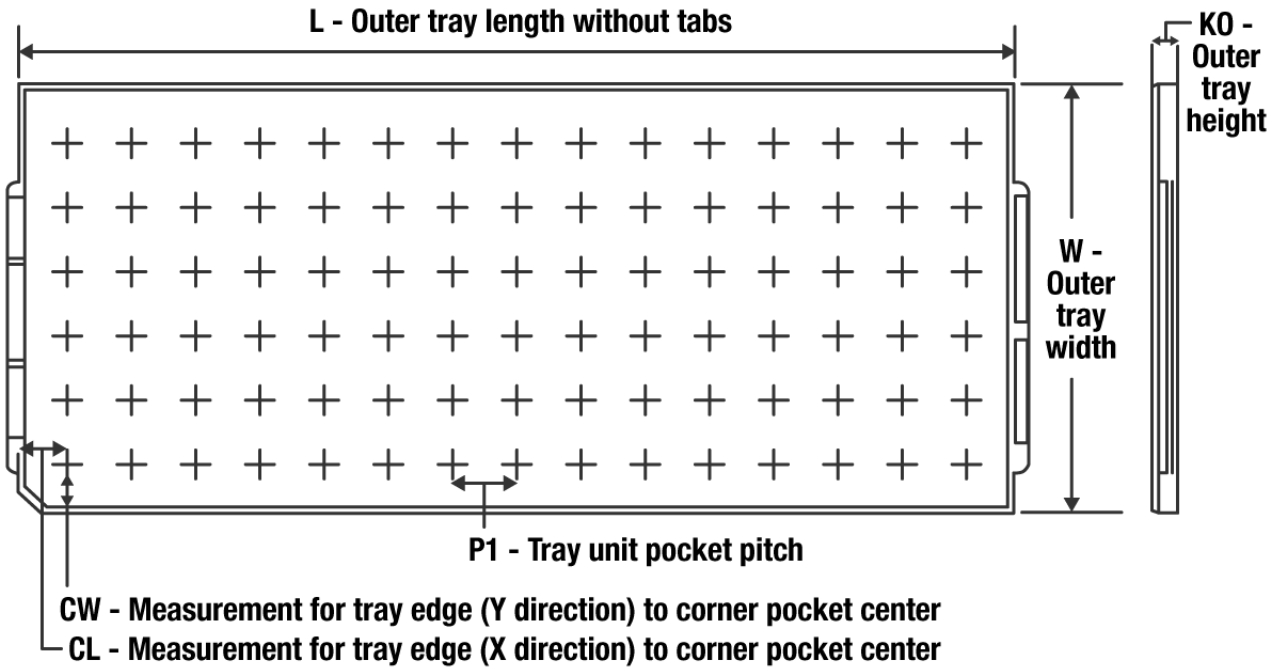
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| MSP430FR2153TDBT | DBT | TSSOP | 38 | 50 | 530 | 10.2 | 3600 | 3.5 |
| MSP430FR2155TDBT | DBT | TSSOP | 38 | 50 | 530 | 10.2 | 3600 | 3.5 |
| MSP430FR2353TDBT | DBT | TSSOP | 38 | 50 | 530 | 10.2 | 3600 | 3.5 |
| MSP430FR2355TDBT | DBT | TSSOP | 38 | 50 | 530 | 10.2 | 3600 | 3.5 |

## TRAY




Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

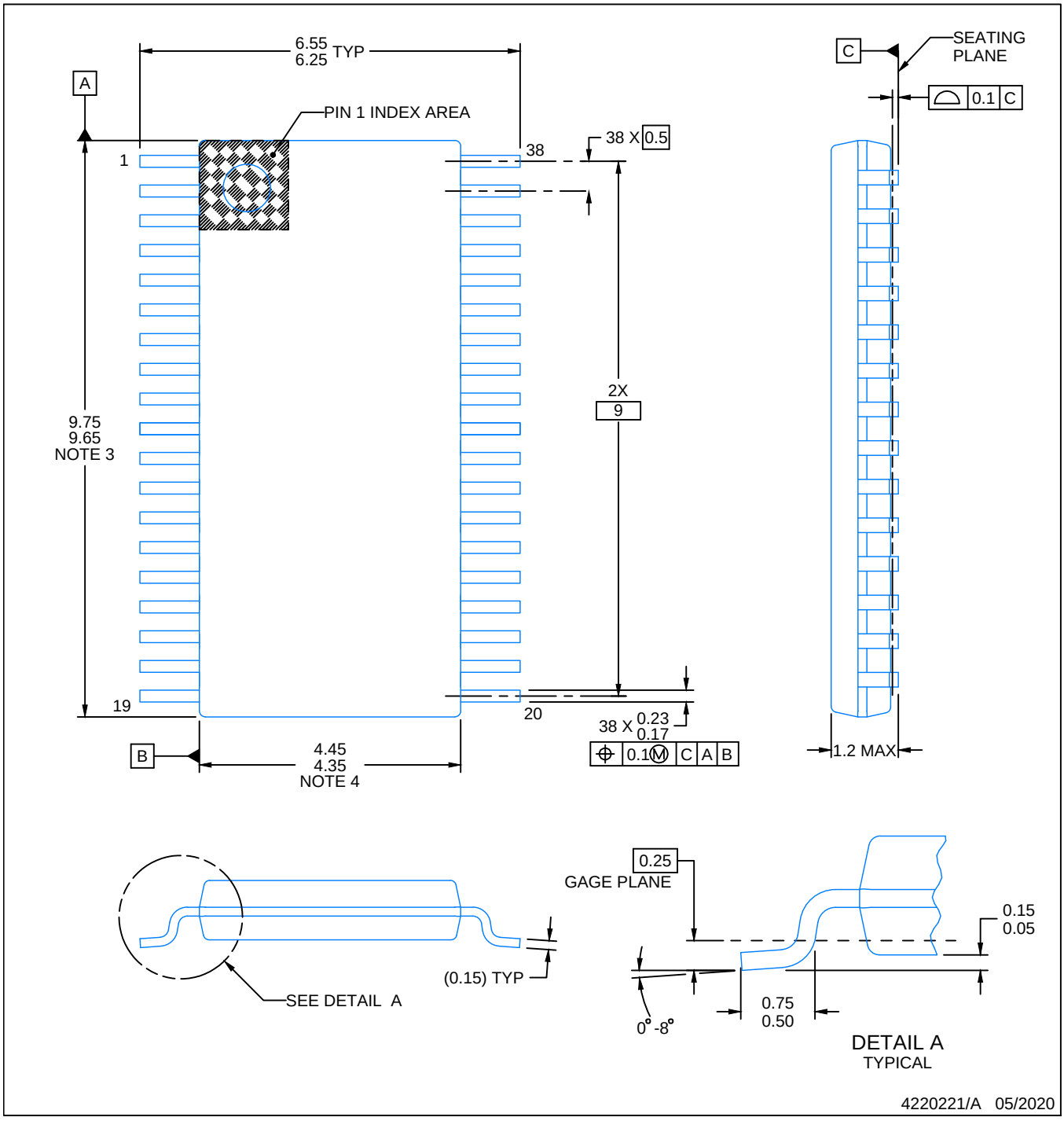
| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430FR2153TPT | PT | LQFP | 48 | 250 | 10 x 25 | 150 | 315 | 135.9 | 7620 | 12.2 | 11.1 | 11.25 |
| MSP430FR2153TPT | PT | LQFP | 48 | 250 | 10 x 25 | 150 | 315 | 135.9 | 7620 | 12.2 | 11.1 | 11.25 |
| MSP430FR2155TPT | PT | LQFP | 48 | 250 | 10 x 25 | 150 | 315 | 135.9 | 7620 | 12.2 | 11.1 | 11.25 |
| MSP430FR2155TPT | PT | LQFP | 48 | 250 | 10 x 25 | 150 | 315 | 135.9 | 7620 | 12.2 | 11.1 | 11.25 |
| MSP430FR2353TPT | PT | LQFP | 48 | 250 | 10 x 25 | 150 | 315 | 135.9 | 7620 | 12.2 | 11.1 | 11.25 |
| MSP430FR2353TPT | PT | LQFP | 48 | 250 | 10 x 25 | 150 | 315 | 135.9 | 7620 | 12.2 | 11.1 | 11.25 |
| MSP430FR2355TPT | PT | LQFP | 48 | 250 | 10 x 25 | 150 | 315 | 135.9 | 7620 | 12.2 | 11.1 | 11.25 |
| MSP430FR2355TPT | PT | LQFP | 48 | 250 | 10 x 25 | 150 | 315 | 135.9 | 7620 | 12.2 | 11.1 | 11.25 |

# PACKAGE OUTLINE

## DBT0038A

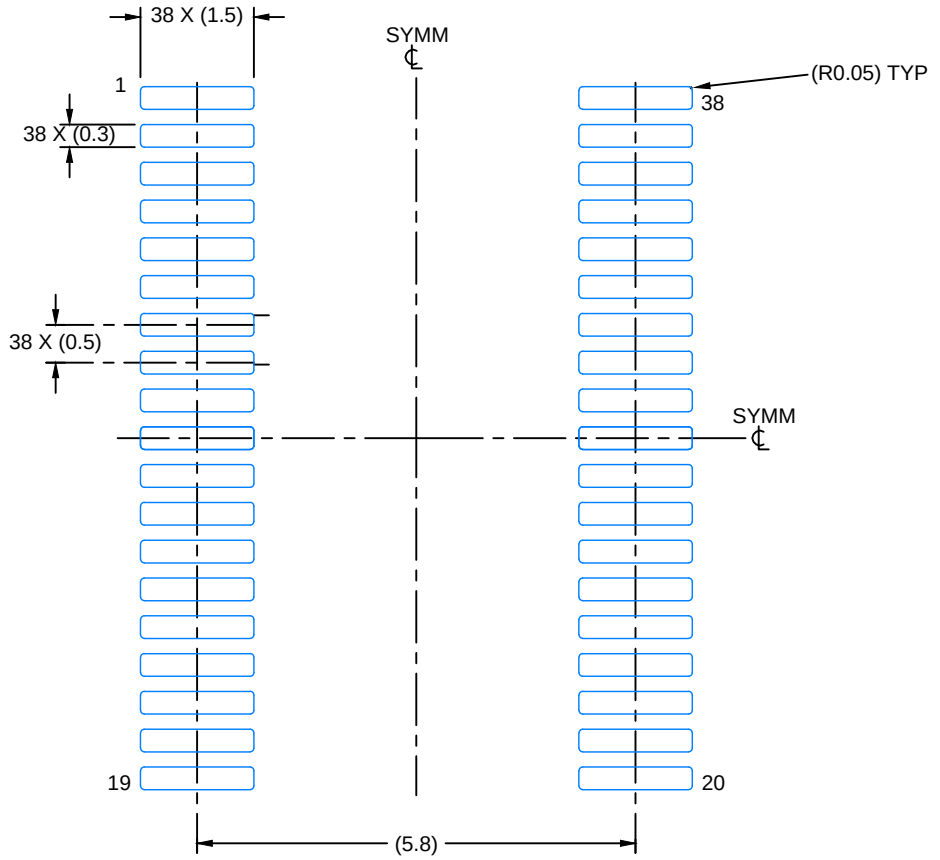
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

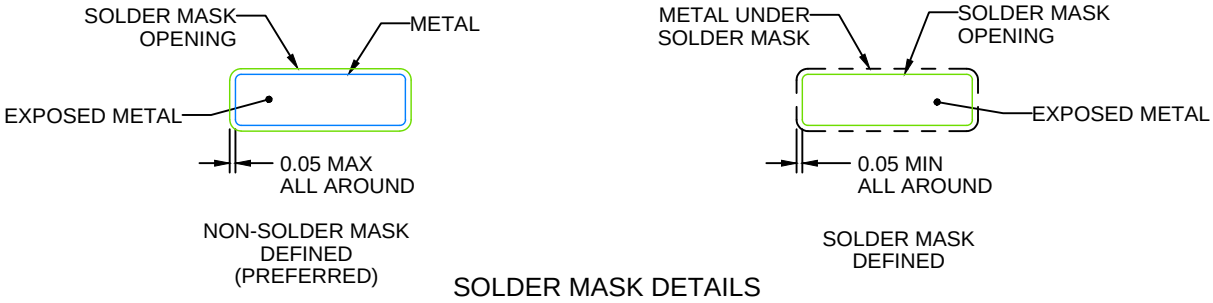



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

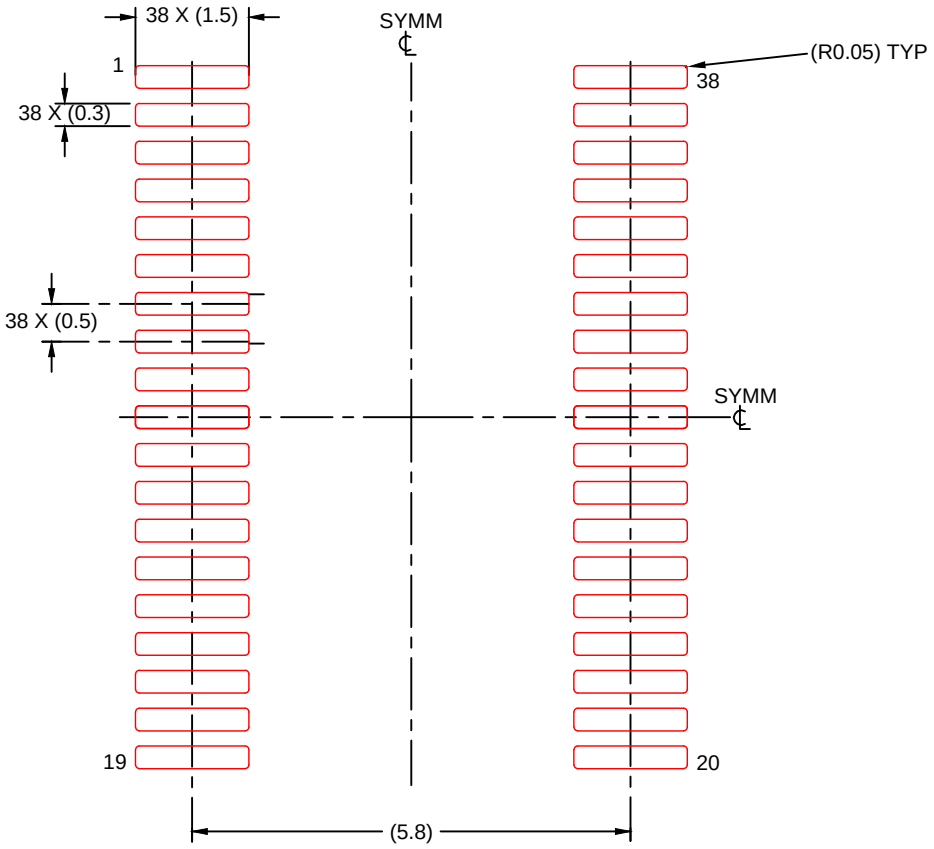



SOLDER MASK DETAILS

4220221/A 05/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220221/A 05/2020

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

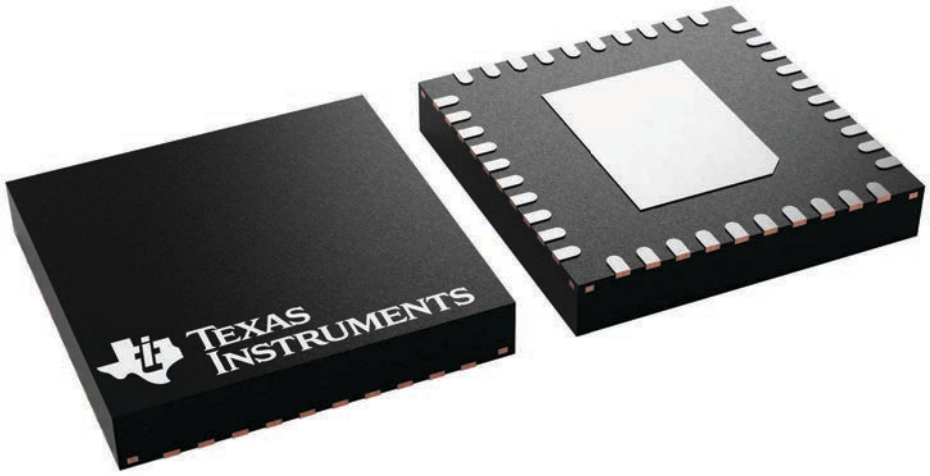
## RHA 40

## VQFN - 1 mm max height

**6 x 6, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



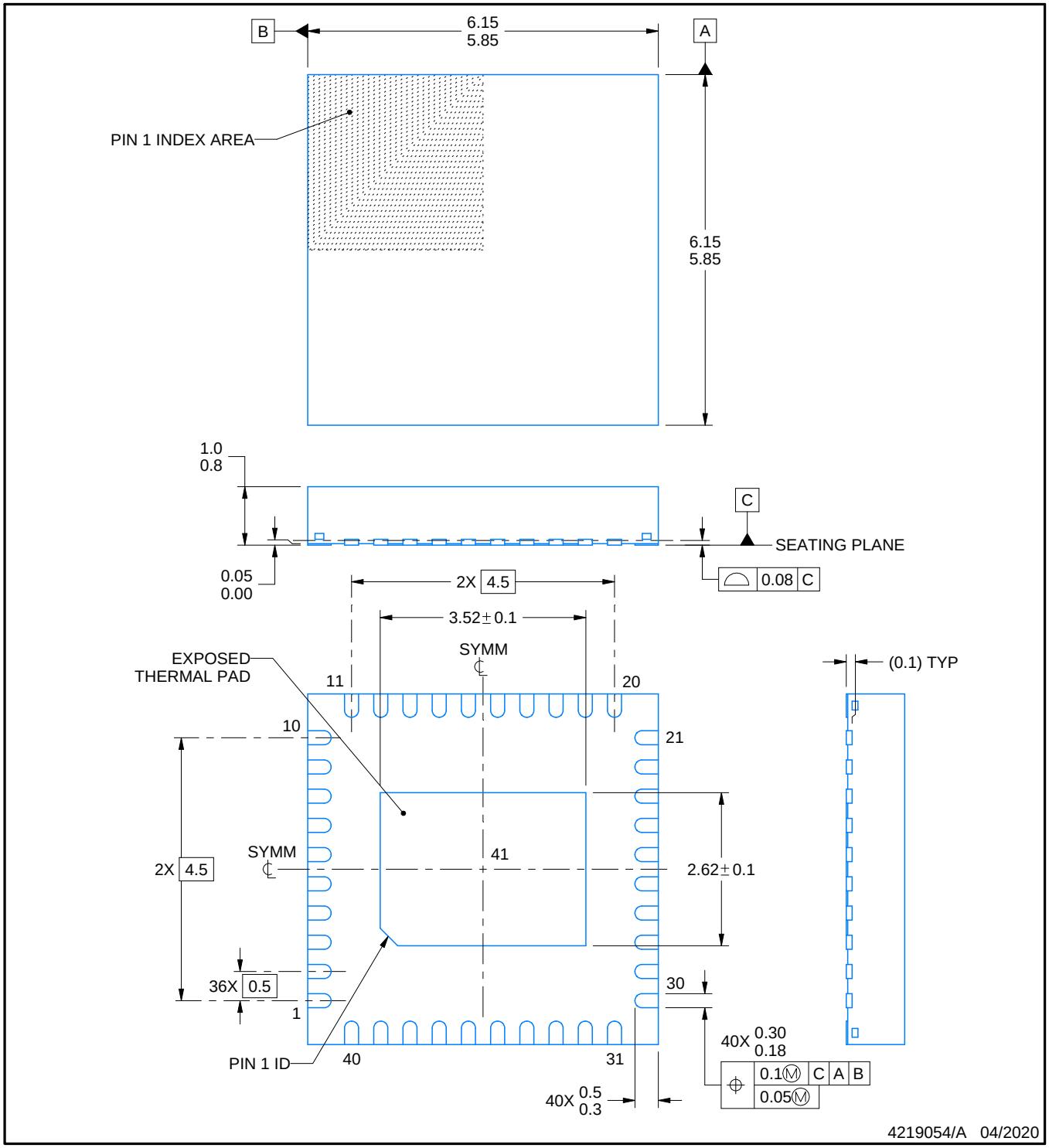

4225870/A

# RHA0040E

# PACKAGE OUTLINE

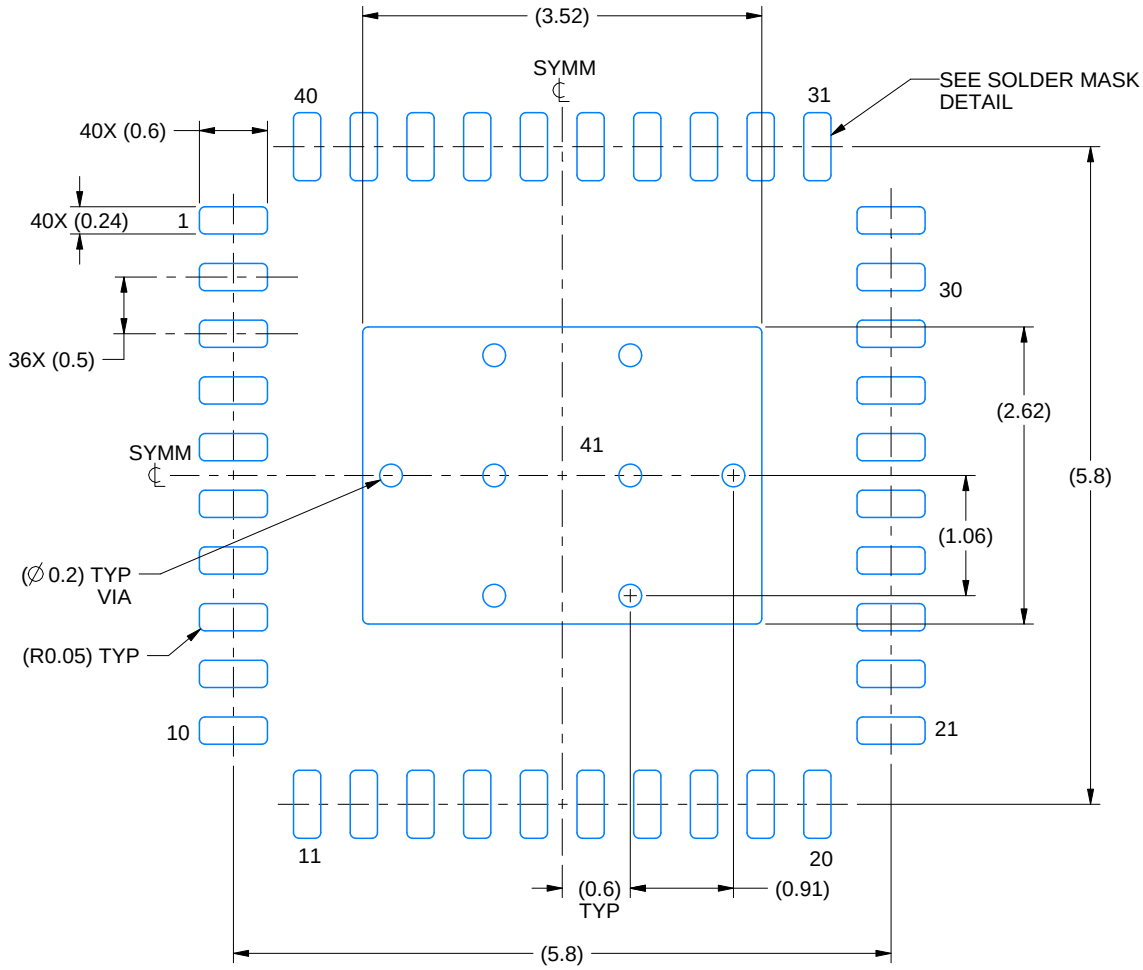
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

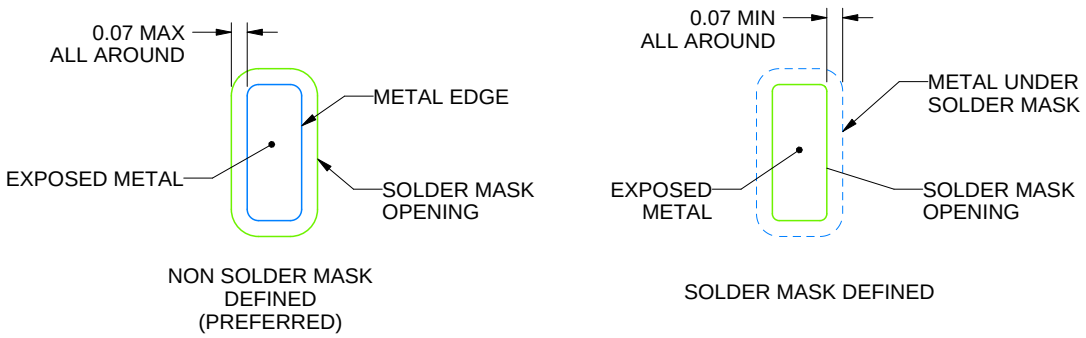



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

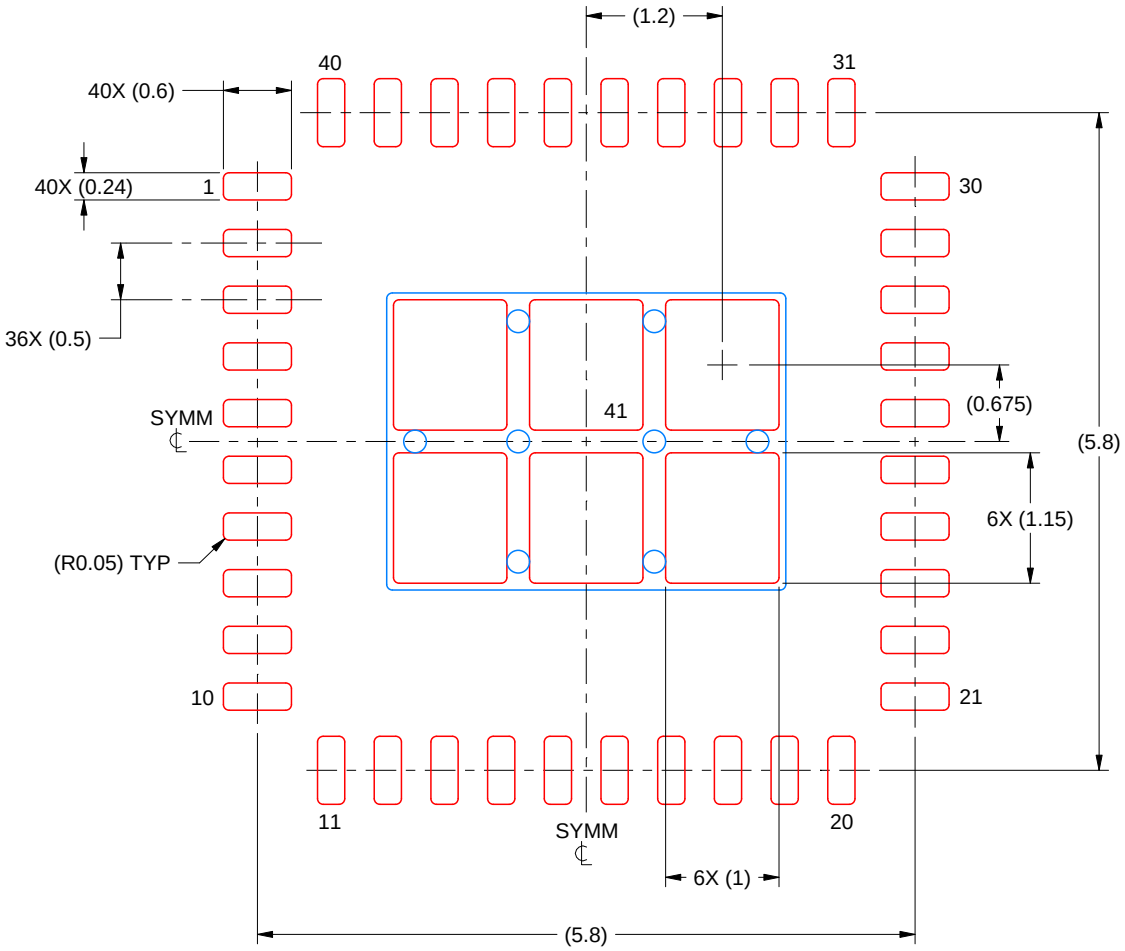



SOLDER MASK DETAILS

4219054/A 04/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 41
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

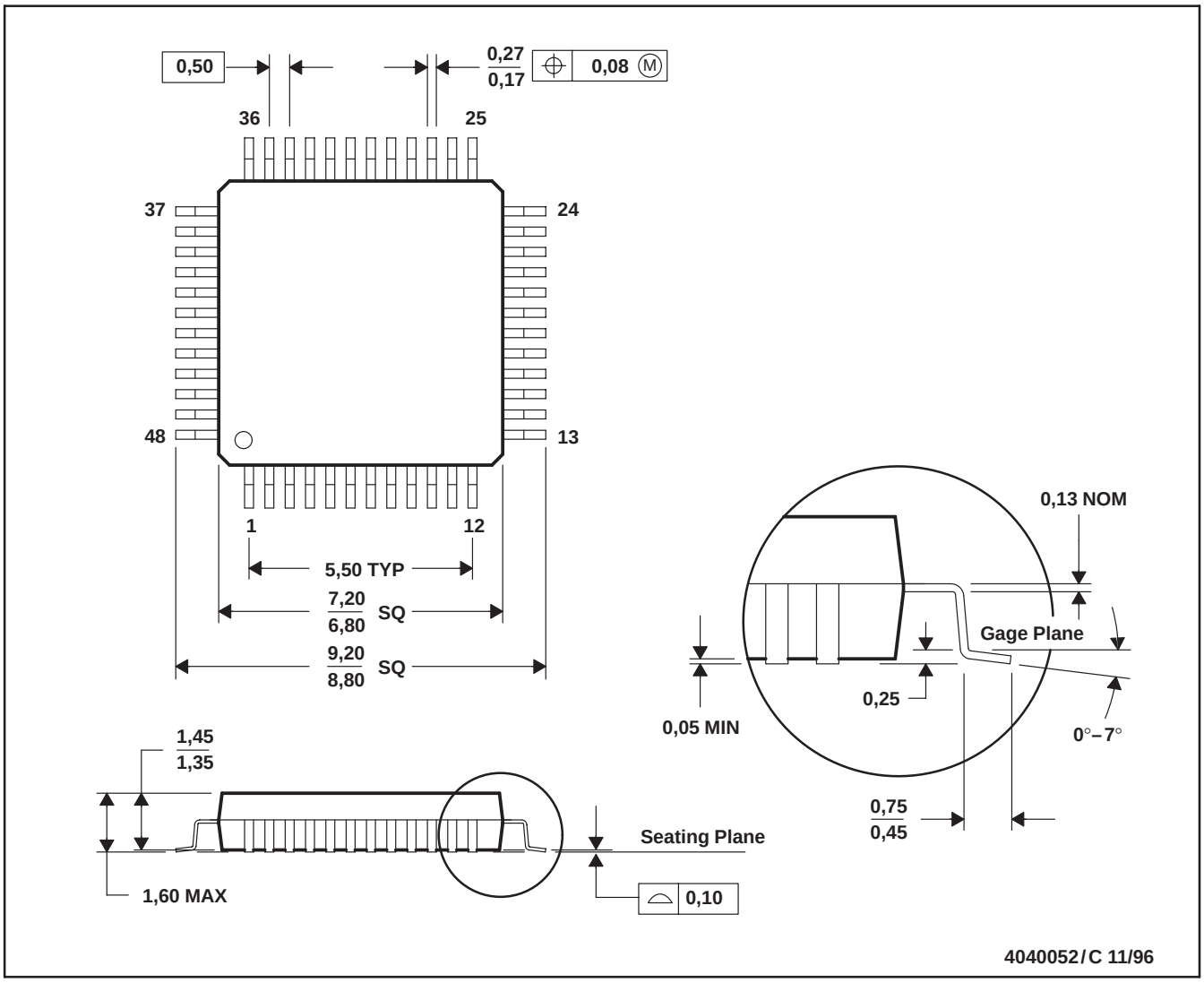
4219054/A 04/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MTQF003A – OCTOBER 1994 – REVISED DECEMBER 1996

**PT (S-PQFP-G48)** **PLASTIC QUAD FLATPACK**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. This may also be a thermally enhanced plastic package with leads conected to the die pads.

# GENERIC PACKAGE VIEW

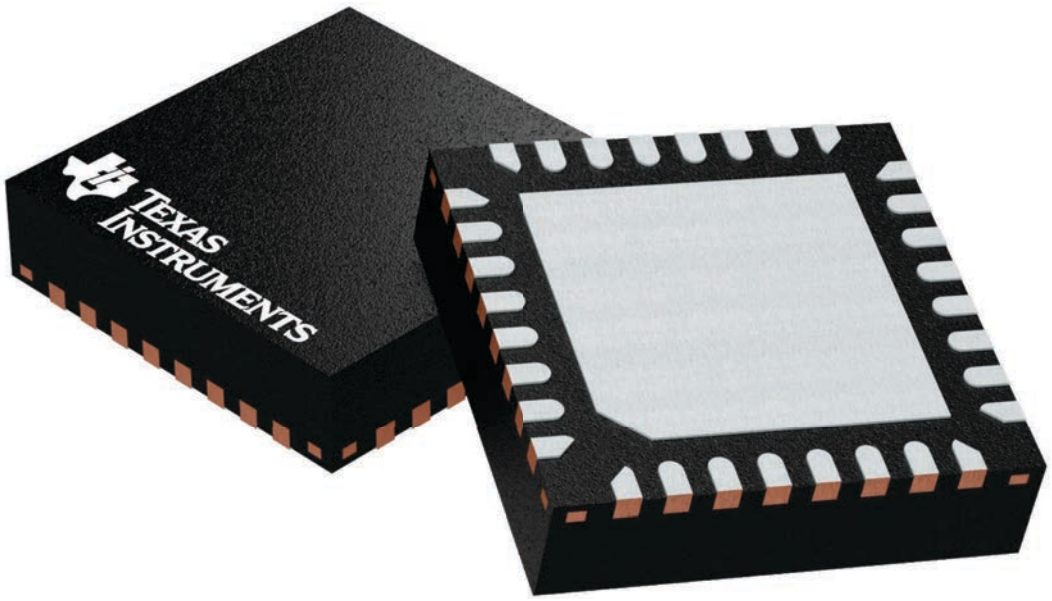
## RSM 32

## VQFN - 1 mm max height

**4 x 4, 0.4 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



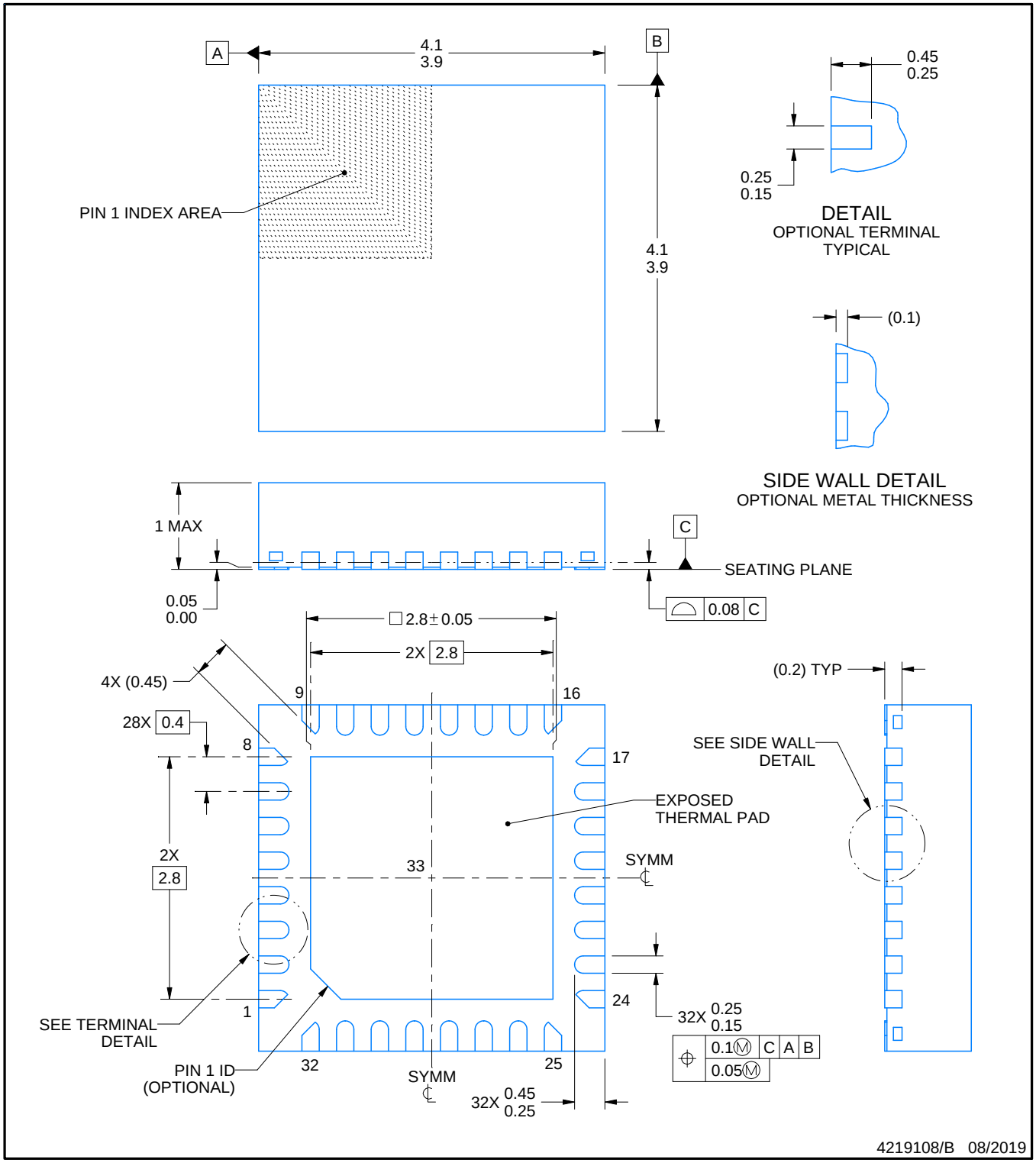

4224982/A

# PACKAGE OUTLINE

## RSM0032B

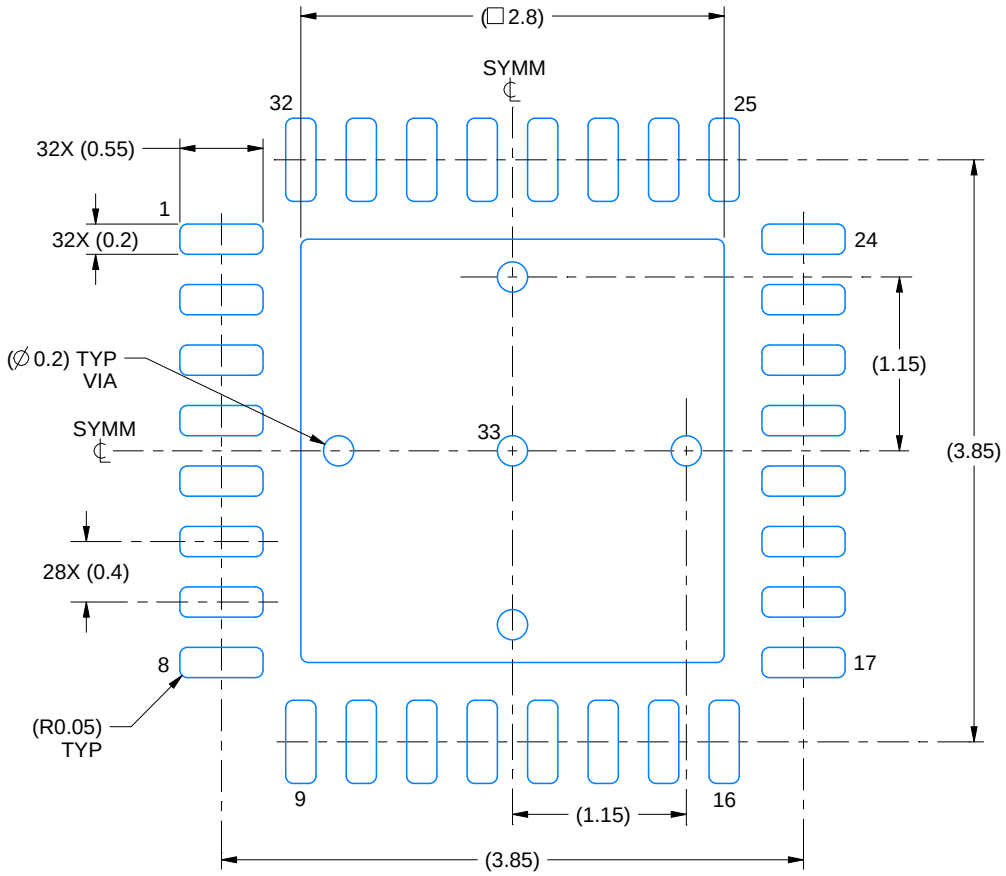
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

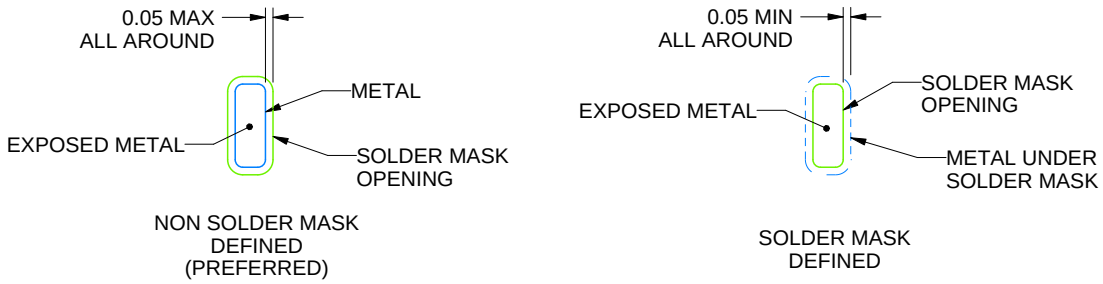



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

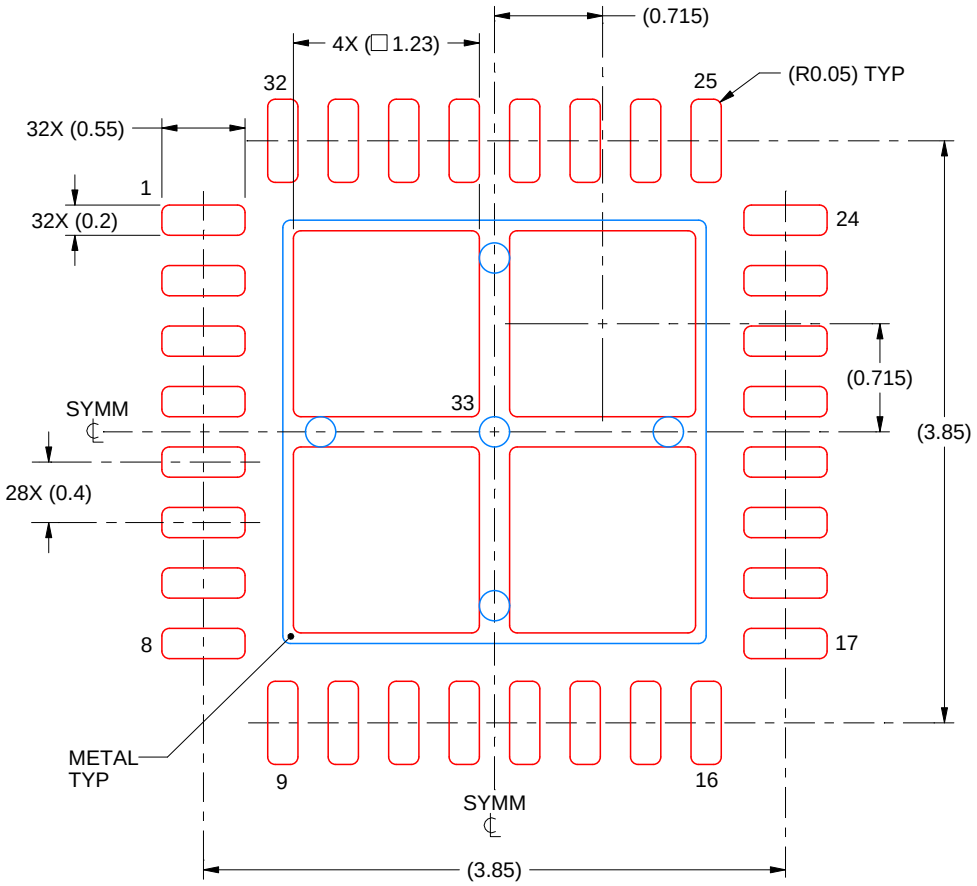



SOLDER MASK DETAILS

4219108/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219108/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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